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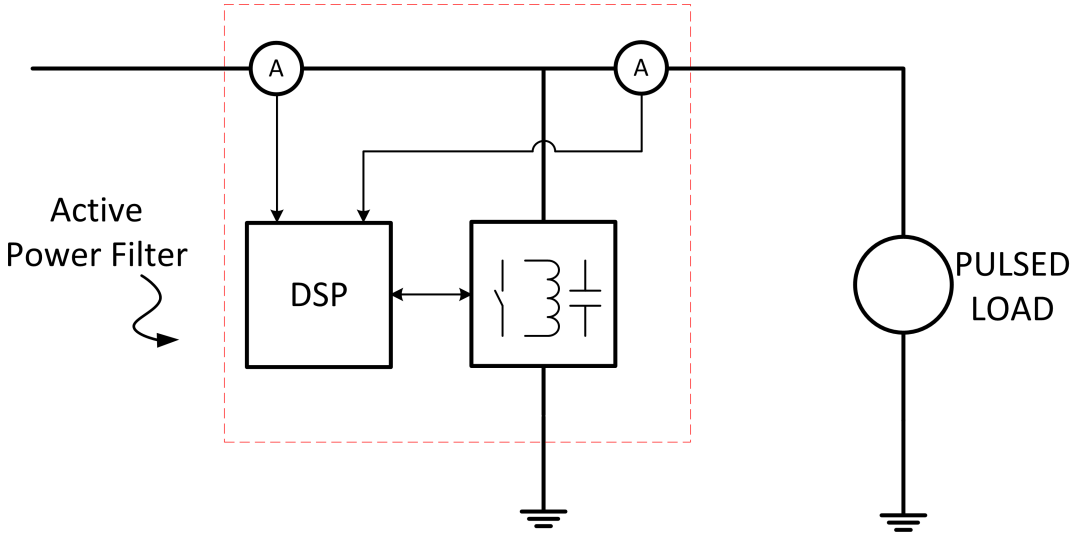

Digitally Controlled Active Power Filter for AESA Radar

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2013

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Abstract

This master thesis demonstrate a digitally controlled Active Power Filter, which is used for eliminating low frequency distortion from a pulsating load. As a result, the current on the power supply will be uniform. The main tasks in this master thesis was to design a circuit, build a prototype, program a Digital Signal Processor, do a verification and make an evaluation. The Active Power Filter is average inductance current controlled, with a voltage controller as an outer loop. A state space representation was used for creating a model for the Active Power Filter and a controller. The Active Power Filter with the controller was simulated in SIMULINK in order to evaluating the controller performance. Thereafter, the controller parameter was implemented in a microprocessor and verified with the Active Power Filter, a pulsating load and DC/DC-converter. The Active Power Filter has not been integrated with the existing DC/DC-converter except for the switching frequency being the same. Therefore, there are some conflicts between the controllers in the two devices.

The result of this master thesis show that by combining a passive-filter, active-filter and a DC/DC-converter, it is possible to get an undisturbed power supply on the input of the DC/DC-converter. It has also been shown that it is possible to decrease 300Hz distortion. Also by using a digital control it is possible to create an adaptive system. As a result, the pulsating load characteristics can vary and the Digital Signal Processor will adjust the reference value for that specific load.

Index Terms: Active Power Filter, Active Ripple Filter, Digital Control, Modeling a Hybrid Circuit, Compensator Design, Controller Design, Simulink Simulation, Average Current Control and Power Electronics.

Acknowledgements

We would like to express our deepest gratitude to Valter Nilsson and Johan Ringqvist, our research supervisors, for their patient guidance, enthusiastic encouragement and useful critiques of this research work. Their willingness to give their time so generously has been very much appreciated.

We would also like to thank Stefan Linders, Torbjörn Thiringer and employers of SAAB Electronic Defence Systems.

Daniel Glenting
Daniel Samuel
Göteborg, Sweden, 2013

Contents

Glossary

ADC Analog to Digital Converter. 14, 15, 24–27

AESA Active Electronically Scanned Array. 2, 5, 8, 9

APF Active Power Filter. 2–7, 9, 13, 14, 17, 18, 21, 23–28, 30–32, 34, 35, 37–42, 53, 54, 56

CCM Continuous Conduction Mode. 10, 12

CMPA CoMPare register A. 15, 25

CPU Central Processing Unit. 15, 25

DAC Digital to Analog Converter. 15

DSP Digital Signal Processor. 2, 3, 14, 15, 23–28, 30, 31, 41, 42

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 9–13, 27, 28, 40, 41

OP AMP Operational Amplifier. 15

PCB Printed Circuit Board. 30

PPF Passive Power Filter. 2, 4, 30, 34, 35, 41

PRF Pulse Repetition Frequency. 9

PRI Pulse Repetition Interval. 9

PWM Pulse Width Modulation. 14, 15, 25, 42, 55

RF Radio Frequency. 2, 9

SISOTOOL Single-Input Single-Output tool. 21, 31

T/R Transmitter/Receiver. 8, 9

TF Transfer Function. 16, 18, 19, 21

USB Universal Serial Bus. 24

ZCS Zero-Current-Switching. 41

ZVS Zero-Voltage-Switching. 41

Chapter 1

Introduction

1.1 Background

The military aircraft industry is always in a race of achieving new functionality, lower cost and better performance. For this reason, the number of electrical equipment on board is increasing and this is a challenge for the electronic engineers. One of the challenges is delivering power to radar systems, where the transmitters often are operated in pulsed mode. Radio Frequency (RF) pulses of the Active Electronically Scanned Array (AESA) radar are repeatedly transmitted to propagate in free space towards a target. The radar receiver collects RF energy reflected from the target in order to make it possible to determine data on the target such as range, bearing and speed. The pulsed wave is unfortunately reflected back as a pulsed load on the power supply, which have negative impact on the performance and also could be harmful to other systems. For this reason, power engineers place Passive Power Filter (PPF) at the output and input of a device, so it will mitigate the disturbance. The components of a PPF is usually large in physical size, as well as heavy and this is undesirable in aircrafts. As a result new ways of dealing with disturbance have been developed. One example is to insert switching components with the passive filter and use digital/analog control. This configuration is called Active Power Filter (APF) and makes it possible to obtain a smaller volume compared to the passive solution.

Over the past years there has been an increasing interest for digital control for power applications. The reason for that is the benefits compared with the analog solution, since it is easier to implement changes, decreases the total size and cost efficient in large scale installation. In addition, component values are changing with age, usage and surrounding environment. Also with an analog solution the components value needs to be larger than necessary, so those parts will manage the task in the upcoming years. The flexibility of the Digital Signal Processor (DSP) makes it easy to implement features that otherwise would require additional components.

1.2 Previous work

In a previous work ”Digitally controlled power supply in radar transmitter” [9] the goal was to accomplish uniform current on the power supply, which contain distortion because of a pulsating load. The project investigated the possibility of controlling an existing DC/DC buck converter for manage the noise, which was done by removing the analog control and replacing it with a digital one. The conclusion of that master thesis was that it is possible to decrease the input current variations by controlling the existing converter in a more sophisticated way. The current mitigation was also much better by keeping the existing passive filter.

In the present project, ”Digitally Controlled Active Power Filter for AESA Radar”, a solution will be tested by installing an external device in an effort to reduce the size of the PPF. The benefit with this external device is that space can be saved in the aircraft by decreasing the size of the power filter components and it will also require less modification of the existing power supply.

1.3 Purpose

The aim of this thesis work is to build a digitally controlled APF for a pulsating load that will keep the supply system undisturbed, minimize current fluctuations, have high power efficiency and give a low current ripple. Additional goal is to create self-adjustable controller that will adapt for load changes. Moreover, to build a test set-up and test the results experimentally.

1.4 Scope

In this master thesis, the focus will be on a digitally controlled APF that will be realized in a circuit design and a hardware prototype. This is due to the fact that the main goal with this project is to investigate the possibilities of digital control. In this project the size of the prototype is not of importance.

The APF will be evaluated only by a resistive pulsating load. Delfino F28335 DSP with its experiment-board will be use in this project, because the supervisor has experience of using it and it has all the needed modules. When programming the DSP, C language will be used because of its ease to use over assembler language.

Chapter 2

Preliminary Study

2.1 Passive versus Active -power filter

PPF can consist of inductances, resistors and capacitors. The APF components in addition to the ones in the PPF also includes components such as semiconductor switches, operational amplifier and gyrators.

The PPF capacitor is usually bigger in physical size compared to the active solution. This is because with an APF it is possible to boost the voltage over the capacitor with a boost converter topology and in doing so the capacitance value decreases

$$C = \frac{Q}{U} \qquad Q = i \cdot t \tag{2.1}$$

where Q is the total amount of charge that the load needs during one period, U is the voltage that the capacitor have stored, i is the load current and t is the load step time. Figure 2.1 shows the voltage ripple over the capacitor plotted versus the capacitance value for a given value of charge Q.

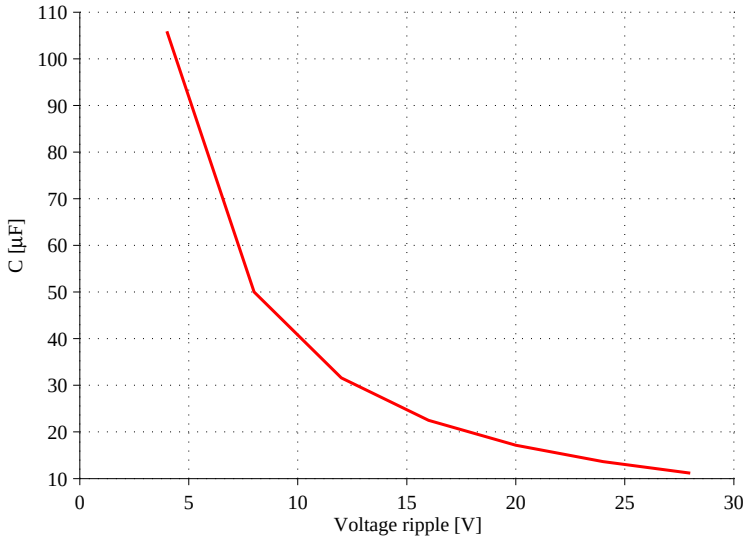

Fig. 2.1 The capacitor value change with the voltage over it for a given charge Q=0.45mC.

Component values are not constant under their life time, on the contrary, components values will change over the years. The alteration rate depends on the surrounding environment and use. Therefore, during the selection of component values, engineers need to take into account the possibility of parameter change. But with the APF it is possible to get a more optimized component value, because the APF can adapt to changes.

One more advantage with the APF is that it can better take care of the distortion without the need of a large capacitor. This can also be solved by several passive filters that take care of the different frequencies, which will take up more space [2].

2.2 Location of active filter

The APF can be installed in four possible location on the DC-power distribution for the AESA radar, which can be seen in the Fig. 2.2.

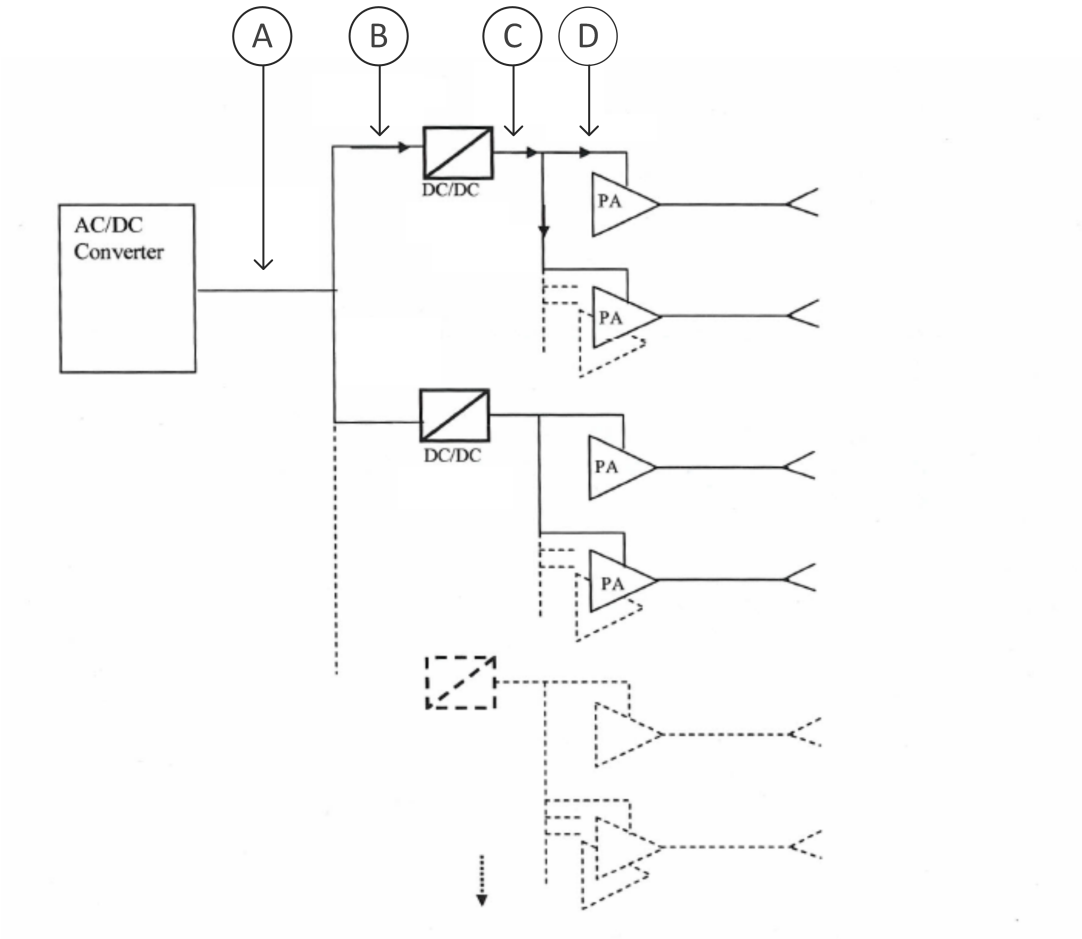

Fig. 2.2 Power supply architecture for the transceivers in an AESA radar.

The decision of where to place the APF will be carried out from a study of the following factors:

- Current level
- Voltage level
- Requirements of quiet input/output
- Power loss
- Number of APF

Placement A

In this placement only one device will be needed, but because of the high power it will be difficult to design a prototype. It also means that the current ripple that the load creates will go through the DC/DC converter, which will cause power losses.

Placement B

By placing the APF at the input of the DC/DC converter it is possible to use the higher voltage level, which in turn gives a smaller value of the power capacitor (chapter 2.1). But the distortion will pass the DC/DC converter before reaching the APF, which will cause power losses in the converter. Compare with placement A, placement B has lower power levels, which will ease a design of a prototype.

Placement C

By placing the APF at the output of the DC/DC converter it will prohibit the disturbance from reaching the DC/DC converter, which in turn lower the power losses. One more advantage with placing it near the DC/DC output instead of near the load (placement D) is that it will decrease the number of devices that are required.

Placement D

Usually filters should be placed as close as possible to the load. But the disadvantage of that would be the amount of devices, which demand larger space in the aircraft.

For this reason, the APF is placed at the output of the DC/DC converter as seen in placement C. As mentioned earlier it will lower the power losses and the amount of devices.

2.3 Method for Active Power Filtering

Different methods for mitigating current distortion using APF exists such as series or parallel connected switched capacitor devices.

The series APF is connected between the source and the load according to Fig. 2.3. The active filter can be implemented by one boost and one buck converter in series and one storage capacitor in between. The boost converter is working in a mode where the input current is regulated and the voltage over the storage capacitor is varied and is always greater than the output voltage of the buck converter. The buck converter is in turn regulating the voltage to dc-bus level in case of location A, C and D in Fig. 2.2. If location B could have been chosen, the buck-converter between location B and C could be modified to cowork with the APF, eliminating the need of an additional buck-converter. Therefore, this solution is only suitable for location B in order to minimize power dissipation.

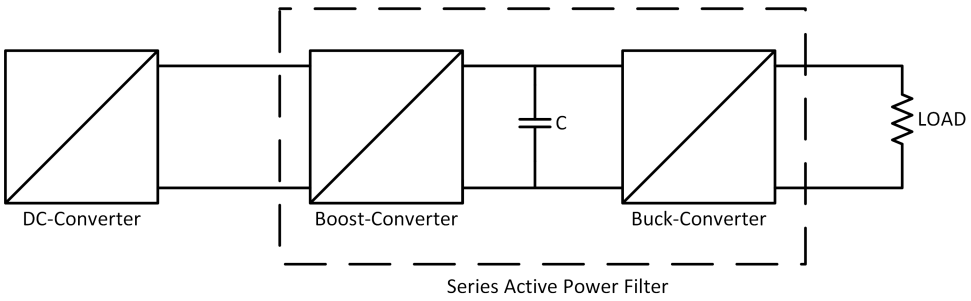

Fig. 2.3 A DC-bus with an APF connected in series between the DC-converter and the load.

The parallel connected APF will be in parallel with a load working as a controlled current source, sourcing and sinking the current in a dc-bus on demand. This topology is shown in Fig. 2.4. Both half- and full-bridge switching stages can be used in the device depending on if it should work in two or four quadrant mode. In two quadrant mode it is only possible to boost the voltage over the capacitor above the DC-bus voltage. In four quadrant mode it is possible to have an arbitrary voltage over the capacitor to get a higher voltage swing during the charge and discharge phase. In this case, the size of the capacitor could be decreased even further. This solution can be implemented at any of the locations in Fig. 2.2.

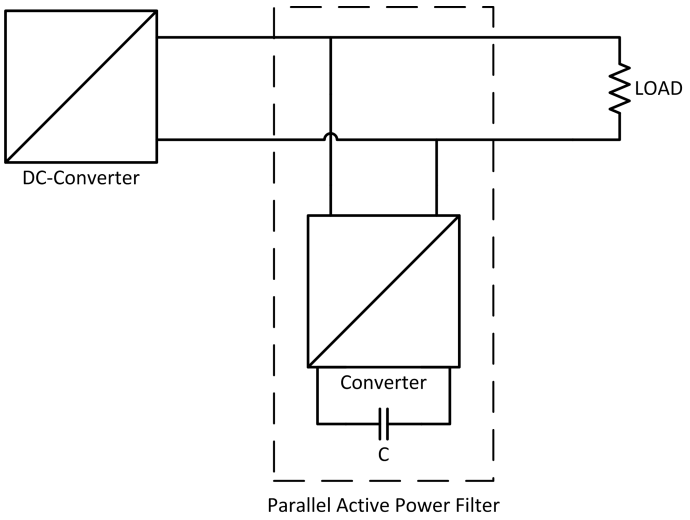

Fig. 2.4 A DC-bus with an APF connected in parallel with the load.

In order to draw a constant current at the DC-bus, the capacitor in both cases mentioned above needs to be charged for the period when there are no load pulse. Then, when a load step is applied, it needs to be discharged. By doing this in a controlled pattern it is possible to control the current drawn from the DC-Converter.

In the previous section, it was considered that the best location for placing an APF is at location C. Because the series APF solution is best when located at position B where it can cooperate with the buck converter for the bus, the parallel solution will be investigated in this thesis.

2.4 Analog versus digital

In this subchapter a short comparison between analog an digital control will be carried out by pointing out advantages and disadvantages. Designers of analog systems continuously need to deal with four issues.

- Instability and the drift in the controller components due to temperature variation
- When working in the dynamic range, a nonlinear behavior will occur
- Choice of adequate frequency range
- Inaccuracies when using components for calculations (For example calculating Duty cycle)

The advantage with the analog control compared with the digital is that it is a well known technique with many engineers that have experience in that area. Also analog control is probably a cheaper solution when it comes to small-medium scale [3]. Analog is also preferable when there is a need for faster control and high frequency bandwidth.

The digital controller offers more optimized solutions for those difficulties than the analog system and furthermore, error in the calculation is negligible in digital compared with the analog [3]. In analog the calculation operation is done by the use of components, which changes during time and vary due to different operation points [3]. It is more flexible for redesign due to modification mostly done in software. Today's processor speed is very fast and the performance is nearly equal with continues monitoring [3]. Also, digital processors are getting more attractive in new areas because of new functions, decreasing price and improvements of performance. In today's market situation it is cheaper with digital control when it comes to large scale integration systems. Where the analog solution, as mentioned earlier is more cost efficient when it comes to small-medium scale [3].

Chapter 3

Theory

3.1 Load characteristics of AESA-radar

In this section a brief introduction of AESA radars will be presented together with the load characteristics and how this load characteristics is defined in this thesis.

One of the advantages of the AESA radar over more conventional radar systems is that it requires no mechanical moving parts for scanning and can simultaneous inquire booth ground and air targets at the same time. In addition, tracking is done very quickly, in order of milliseconds [8].

The AESA radar antenna is made of several hundreds or even up to a couple of thousands of Transmitter/Receiver (T/R) modules, each with its own antenna element. Each T/R can be controlled individually in order to produce a scanning radar beam and the radar antenna can be divided into several groups of T/R modules which then could be given different tasks which could produce multiple radar beams. This also gives the AESA radar the benefit of having redundancy properties where up to maybe 5% of the T/R may malfunction without the functionality of the radar will be reduced and only with a small decrease of performance [5]. In Fig. 3.1 a basic schematic is shown for an AESA radar working in receiver mode with n number of T/R modules. The angle Θ of the radar beam to the right in the figure can be varied by changing the phase and amplitude of the different T/R modules. This can be done in a digital processor by multiplying the signal from the antenna elements with a factor

$$W_i = a_i e^{j\Theta_i} \tag{3.1}$$

where a_i is the amplitude factor and Θ_i is the phase shift of the different T/R modules. For a zero degree theta in Fig. 3.1, all elements are in phase. The same method is valid in transmitter mode.

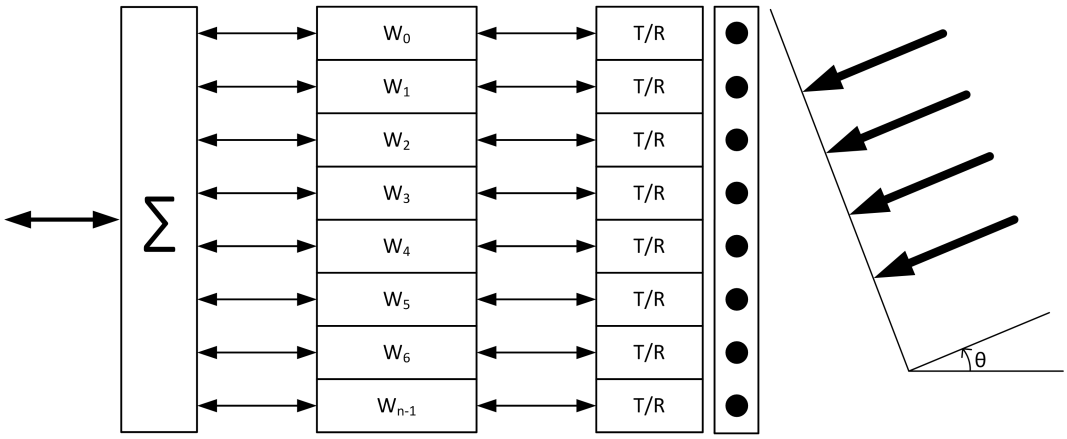

Fig. 3.1 Several T/R modules form a beam front of Θ degree elevation to the right. Radar elements are shown as dots in the middle box, connected to the T/R modules.

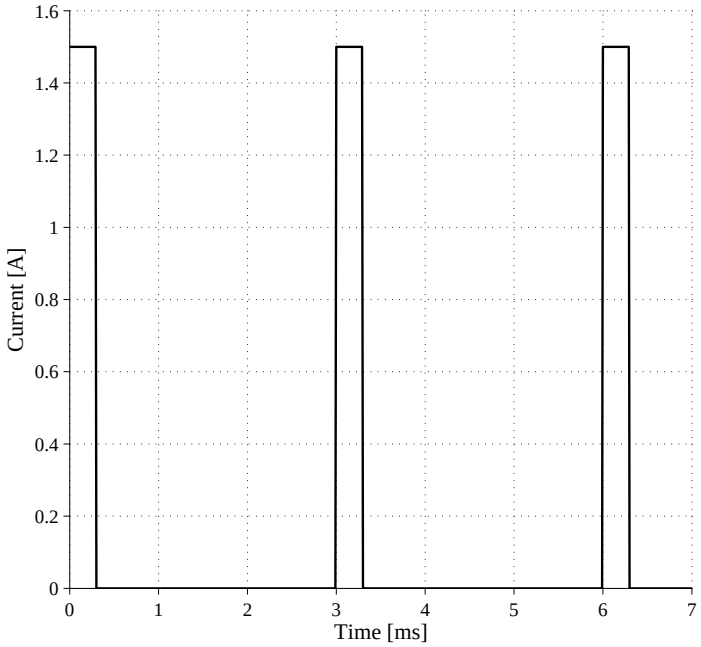

Fig. 3.2 Figure showing the load characteristics of the AESA radar working in low PRF mode.

A common method is to put a switch at the input of each T/R module, that will turn on and turn off the power to the RF transmitter power amplifier. This makes the current to the load to have a pulsed appearance. The current in this thesis is defined as

$$i_{load} = \begin{cases} I_{load} & 0 < t < t_{sw,load} \\ 0 & t_{sw,load} < t < T_{load} \end{cases} \tag{3.2}$$

where $t_{sw,load}$ is the load time under which I_{load} is drawn from the DC-bus and T_{load} is the load time period also called Pulse Repetition Interval (PRI). In Fig. 3.2 the radar is working in low PRF mode with a PRI of $3ms$, a load duty cycle of 10% and an amplitude I_{load} of $1.5A$.

3.2 Active power filter topology

This section will go through the fundamental work of one commonly used topology, the parallel APF. First part will be concerned with a brief review of the theory behind it, namely the boost and buck converters. The second part will describe the working method of the parallel APF:s.

3.2.1 Boost converter

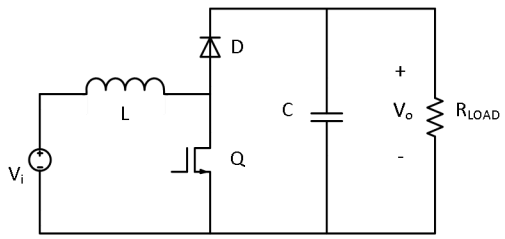

Fig. 3.3 A basic boost converter that consist of a MOSFET, diode, inductor and a capacitor.

In Fig. 3.3 a basic boost converter is shown. This basic circuit is made up of an inductor (L), a switch (Q) (in this case a MOSFET), one diode (D) and a capacitor (C) with a load resistor (R_{LOAD}) in parallel. The voltage over the capacitor and load are always equal or greater than the input voltage. This is possible by switching the MOSFET on and off. Consider the two cases or states when the switch is on and when it is off. Figure 3.4 and 3.5 shows the equivalent circuits for the two cases. In the first case when the switch is on, the inductor will be connected in parallel with the input voltage supply and an input current will start to energizing the inductor. The diode will be blocked because of the higher voltage at its cathode. During this state, the load will be supplied solely by the capacitor. When the switch is turned off, the voltage at the anode of the diode will be higher then the cathode due to the fact that the inductor now will be de-energized and the voltage over the inductor will be added to the input voltage. The capacitor and the load will be charged with energy from both the supply of the converter as well as from the inductor. The pattern is then repeated [11].

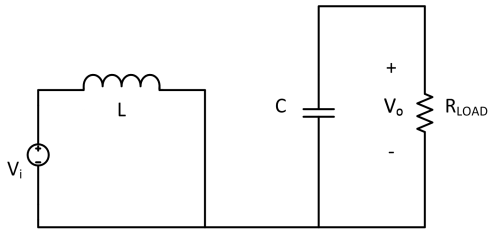

Fig. 3.4 The equivalent circuit for a basic boost converter during MOSFET switched on.

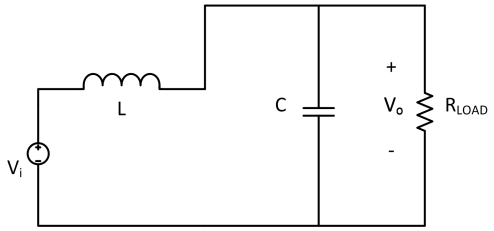

Fig. 3.5 The equivalent circuit for a basic boost converter during MOSFET switched off.

A duty cycle is an expression for the ratio between the on and off state during one switching period and is defined as

$$D = \frac{t_{on}}{T_{sw}} \tag{3.3}$$

where D is the duty cycle, t_{on} is the time when the switch is on and T_{sw} is the switching period time. If Continuous Conduction Mode (CCM) is assumed which is a mode where the inductor current never is zero continuously. The inductor voltage time integral must be zero in steady state over one switching period,

$$V_L = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)dt = \frac{1}{T_{sw}} \int_0^{t_{on}} V_i dt + \frac{1}{T_{sw}} \int_{t_{on}}^{t_{off}} (V_i - V_o)dt = 0 \tag{3.4}$$

where V_L is the mean inductor voltage, V_i is the voltage at the converter input, V_o is the load or capacitor voltage and t_{off} is the time when the switch is turned off. Evaluating the integrals in (3.4) yield

$$V_i t_{on} + (V_i - V_o)t_{off} = 0 \tag{3.5}$$

The voltage over the inductor and the current through it is shown in Fig. 3.6 for the two switching states.

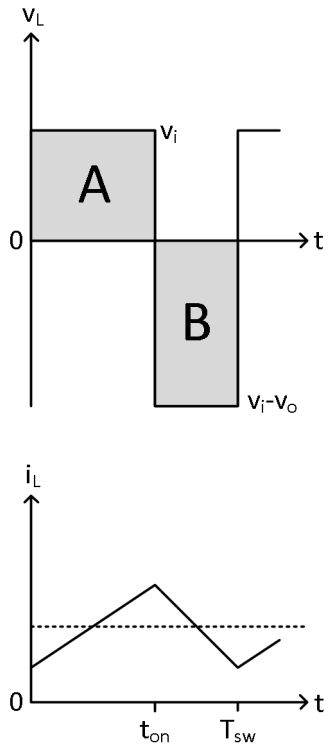

Fig. 3.6 The voltage over the inductor and the current through it during MOSFET on and off.

By dividing (3.5) with T_{sw} and use the identity (3.3), the relation between input voltage V_i and output voltage V_o is

$$V_o = \frac{1}{1-D} V_i \tag{3.6}$$

If ideal components are used, no losses in the circuit will appear, shaded area A and B in Fig. 3.6 will be equal and

$$P_i = V_i I_i = V_o I_o = P_o \tag{3.7}$$

where P_i is the input power, P_o the output power and I_i and I_o the input and output current. Then

$$I_o = (1-D) I_i \tag{3.8}$$

With ideal components, the output voltage in (3.6) can give an infinitely high output voltage by choosing a D close to one. In reality, the voltage can not be infinitely high due to limitations in real components, for example parasitic elements [11].

3.2.2 Buck converter

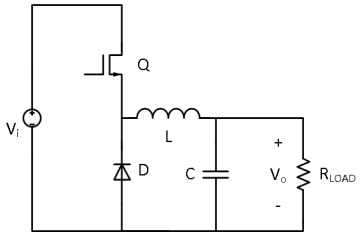

Fig. 3.7 A basic buck converter that consist of a MOSFET, diode, inductor and a capacitor.

Figure 3.7 shows a basic buck converter made up of similar components as the boost converter but at different locations. In this circuit the voltage over the capacitor (C) and load (R_{LOAD}) are always equal or lower than the input voltage. As with the boost converter, consider the two cases when the MOSFET is on and when it is off. Figure 3.8 and 3.9 shows the equivalent circuits for the two cases. In the first case when the switch (Q) is on, the inductor (L) will be connected in series with the input voltage supply. A current will start to flow and charge the capacitor and supply the load. When the switch turns off the inductor current will continue to flow in the same direction, but because the MOSFET now is off the inductor current will pass through the diode instead. This pattern is then repeated.

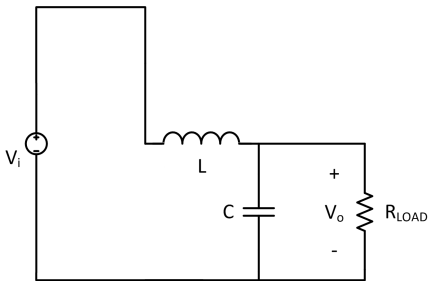

Fig. 3.8 The equivalent circuit for a basic buck converter during MOSFET switched on.

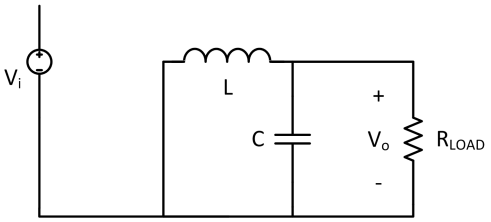

Fig. 3.9 The equivalent circuit for a basic buck converter during MOSFET switched off.

With the definition of the duty cycle in (3.3) and assuming CCM the inductor voltage time integral over one switching period for the buck converter

$$V_L = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)dt = \frac{1}{T_{sw}} \int_0^{t_{on}} (V_i - V_o)dt + \frac{1}{T_{sw}} \int_{t_{on}}^{t_{off}} V_i dt = 0 \tag{3.9}$$

must be zero. Evaluating the integrals of (3.9) gives

$$(V_i - V_o)t_{on} + V_i t_{off} = 0 \tag{3.10}$$

Inserting (3.3) into (3.10) an expression for the input voltage to output voltage can be described

$$V_o = DV_i \tag{3.11}$$

The voltage over the inductor and the current through it is shown in Fig. 3.10 for the two switching states.

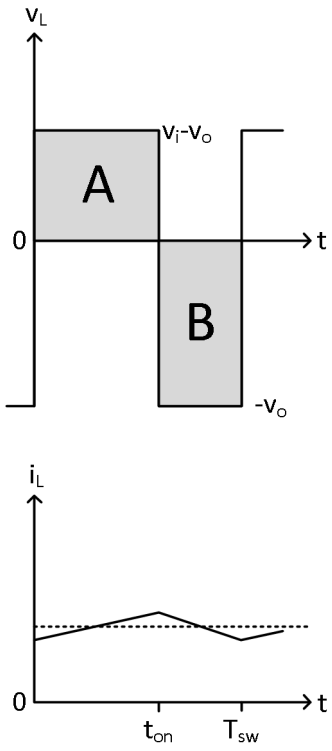

Fig. 3.10 The voltage over the inductor and the current through it during MOSFET on and off.

Assuming no losses in the circuit, the shaded area A and B in Fig. 3.10 should be the same and

$$P_i = V_i I_i = V_o I_o = P_o \tag{3.12}$$

and

$$I_o = \frac{I_i}{D} \tag{3.13}$$

3.2.3 Parallel Active Power Filter

The parallel APF is build up on the principle of the boost and buck converter. Figure 3.11 shows the parallel APF connected to a dc bus and a pulsed load. Compared with Fig. 3.3 the parallel APF has no load over the capacitor and the diode is interchanged with another MOSFET to make it possible to transfer energy in both direction to- and from the capacitor.

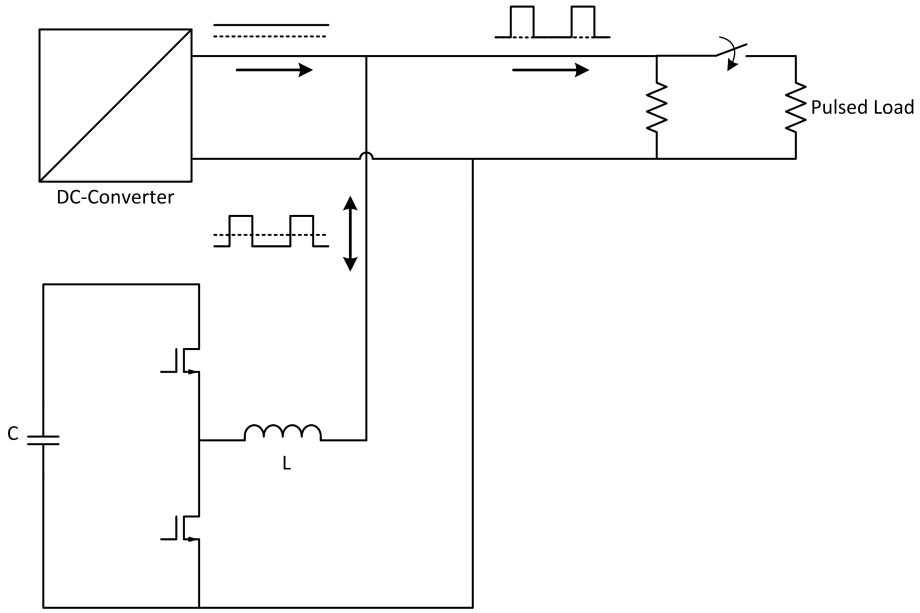

Fig. 3.11 A parallel connected APF connected to a DC-bus. The straight arrows show the direction of the current in the circuit.

With a pulsating load at the dc-bus it is possible to supply a significant part of the load power from the APF:s storage capacitor during the load pulse (APF working in buck mode) and then charge the storage capacitor slowly during no load (APF working in boost mode). This makes the DC-bus supply see the total load (APF and pulsed load) as a constant load with less current harmonics in the supply chain.

3.3 Digital Signal Processor

In this chapter a general overview will be carried out on the different modules that will be used in the project. The main use of the DSP is usually to control a unit that works in the continuous time. The DSP work in discrete time and gets digital values from the Analog to Digital Converter (ADC) module, which converts continuous time samples to digital. The DSP is then processing the data and then convert the processed digital signal back to a continuous time signal through a Pulse Width Modulation (PWM) unit.

3.3.1 Analog Digital Converter

This conversion is done by using the ADC internal ”sample and hold” circuit, which can be seen in Fig. 3.12.

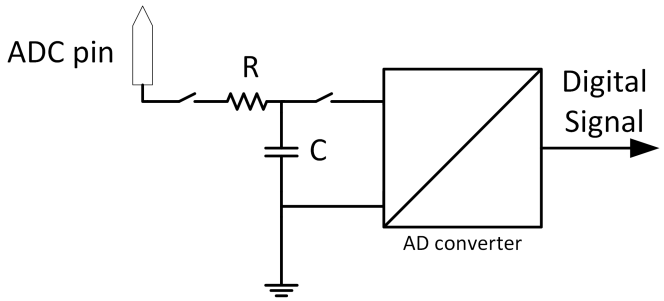

Fig. 3.12 Analog Digital converter with a sample and hold RC circuit to the left in the figure.

The conversion is done periodically by controlling the switches, where the switching frequency is the same as the sample speed. The sample speed depends on the ADC conversion time and the RC constant in Fig. 3.12. It is also important to have a low impedance source, which can be achieved by using an Operational Amplifier (OP AMP).

The ADC resolution depends on amount of bits per value. For example, if a 12 bit ADC is used, the resolution will be

$$Resolution = 2^{12} = 4096 \tag{3.14}$$

and if the input range is between 0-3V, then minimum measurable voltage change will be

$$\Delta V = \frac{range}{resolution} = \frac{3}{4096} = 0.73\frac{mV}{step} \tag{3.15}$$

3.3.2 Pulse Width Modulation

The PWM module can be seen as a kind of Digital to Analog Converter (DAC). The duty cycle will be obtained by calculating a reference and compare it with the PWM ramp. When the PWM ramp reached the same level as the reference, the DSP will change the states to high/low for the two signals Sw1 and Sw2 in Fig. 3.13.

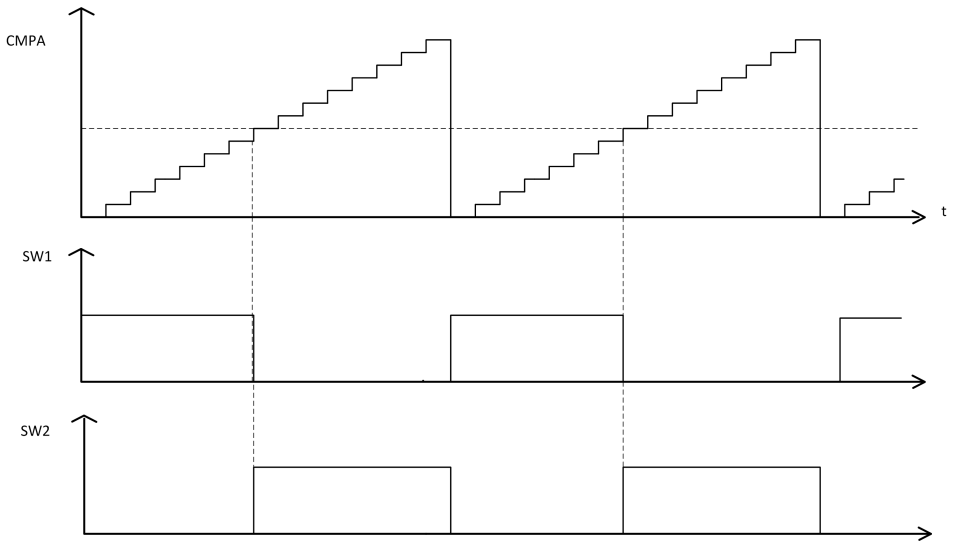

Fig. 3.13 Pulse Width Modulation counter with a specific duty cycle reference and the states of two switches.

The PWM resolution that can be seen in Fig. 3.13 depends on the Central Processing Unit (CPU) frequency and the desired PWM frequency. CoMPare register A (CMPA) is a build in function in the DSP for Counter Compare the PWM steps with a reference. In addition, the PWM module also have a Dead-Time generator, which can be useful in order to avoid excessive current from simultaneous conduction of both switches, which could break the switches.

3.4 Low-Pass Sallen-Key Filter

OP AMPs will be used in this project as measurement signal amplifier and low pass filter. The Sallen-Key Architecture , which is a Second-Order-Low-Pass filter will be used. The guideline of designing a butterworth filter is used for planing the Sallen-key Architecture filter. The frequency response of the Butterworth Filter is as flat as mathematically possible, with no ripples . The Low-Pass filter Sallen-Key Architecture is presented in Fig. 3.14.

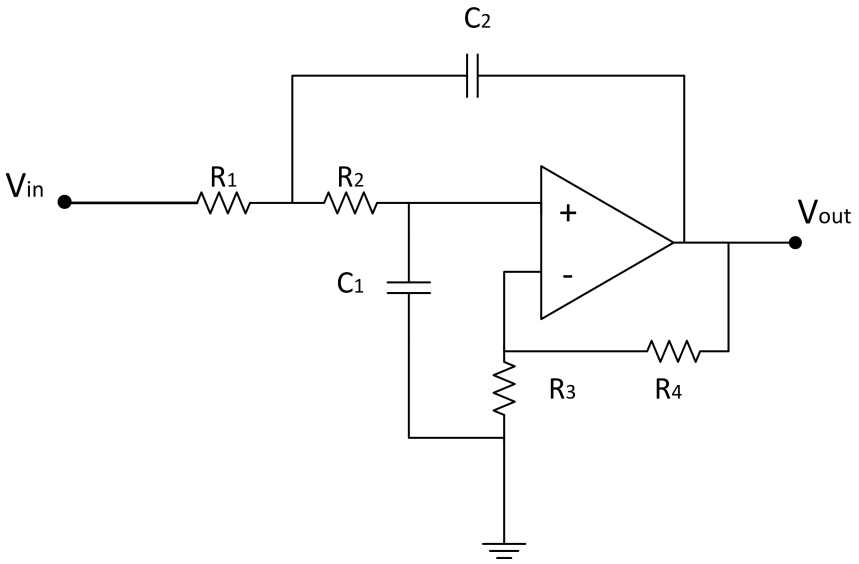

Fig. 3.14 A Low-Pass filter Sallen-Key architecture for measurement signal filtering.

The Transfer Function (TF) of a Second-Order-Low-Pass filter can be used for deciding the cutoff frequency, the stability and the gain

$$\begin{aligned} H(f) &= -\frac{Gain}{(\frac{f}{f_C})^2+\frac{1}{Q}\frac{jf}{f_C}+1} \\ K &= \frac{R3+R4}{R3} \\ f_C &= \frac{1}{2\pi\sqrt{R1R2C1C1}} \\ Q &= \frac{\sqrt{R1R2C1C2}}{R1C1+R2C1+R1C2(1-K))} \end{aligned} \tag{3.16}$$

in those equations, f is the frequency, f_c is the cutoff frequency and K is the Gain of the transfer function.

Chapter 4

Case Set-Up

4.1 Control Method

In this Master Thesis the APF will be controlled by an average inductance current method, more about this method can be found in [1]. Therefore, the DC-converter current i_{DC} and the load current i_{Load} will be monitored, which is seen in Fig. 4.1

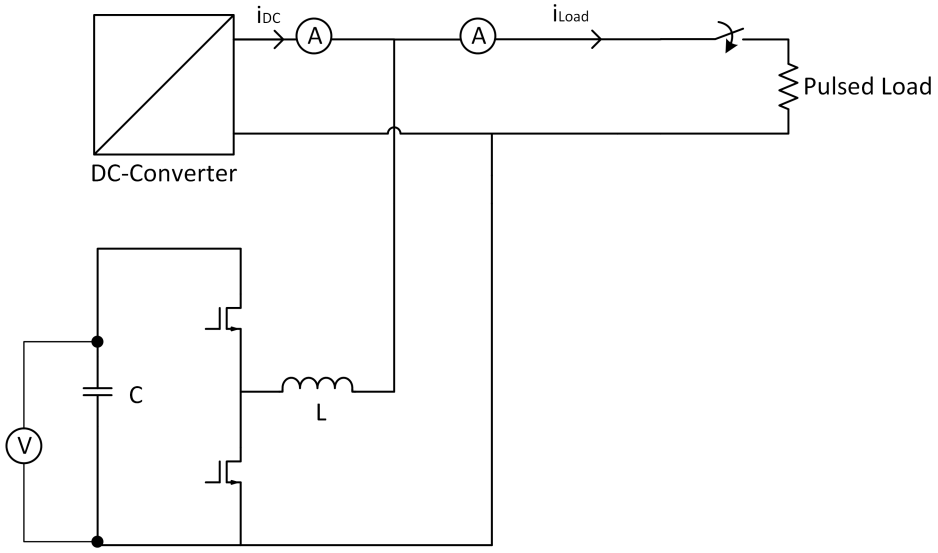

Fig. 4.1 The system measurement points.

The load current i_{Load} measurement is used for calculation of the current reference i_{ref} in the controller that is seen in Fig. 4.2. It is also used for detecting if the load is switched on or off, which is useful information for the controller and that will explained in the next chapter.

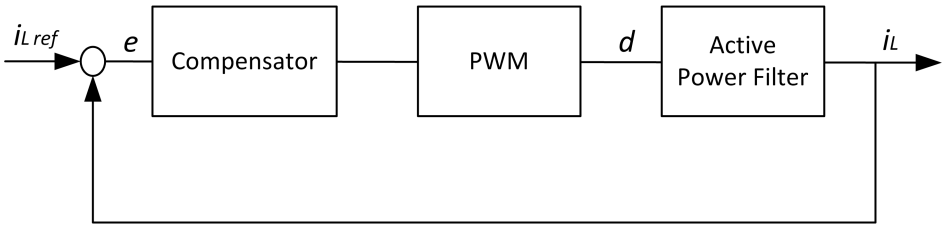

Fig. 4.2 Current control system for the APF using negative feedback.

The controller is using the DC-converter current i_{DC} and the load current i_{Load} measurement to determine the actual inductor current i_L, which will be compared with the reference value $i_{L.ref}$ and produce an error signal. Thereafter, the error signal will be used in the regulator. The regulator will determine a duty cycle d which will control the APF switches.

4.2 Modeling Of Active Power Filter

In this chapter two models will be derived to describe the APF. The Boost-Mode model which will manage the storing of energy and the Buck-Mode model will manage the discharging. Since the APF is controlled by the inductor current, the TF of the inductor current will be derived from the models. The TF for those models will be used later in section 4.3.

4.2.1 Boost-Mode Model

In the following steps, an explanation will be given of how to create a model for an APF in the Boost-Mode.

1. Describe each circuit state with state space,

$$\dot{x} = Ax + Bu \tag{4.1}$$

$$y = Cu \tag{4.2}$$

$$x = \begin{bmatrix} i_L \\ V_C \end{bmatrix} \tag{4.3}$$

$$u = [V_{in}] \tag{4.4}$$

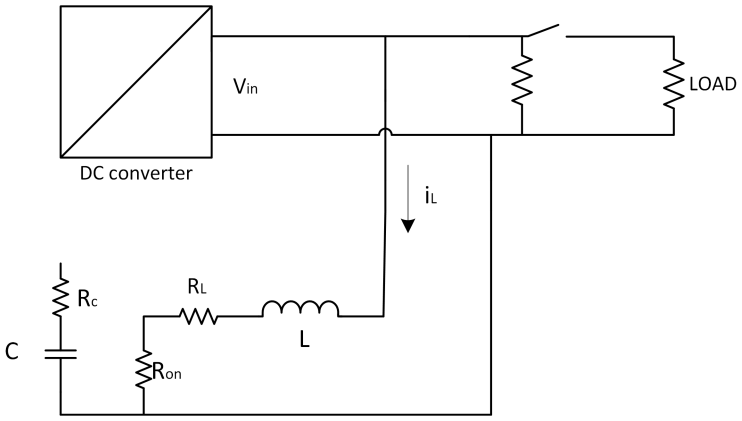

Fig. 4.3 Boost-Mode, First state.

In the first state, matrixes A, B and C can be described by rearranging the circuit equation, which derive from Fig. 4.3 to

$$\frac{di_L}{dt} = \frac{1}{L}(V_{in} - i_L(R_L + R_{on})) \tag{4.5}$$

$$\frac{dV_C}{dt} = 0 \tag{4.6}$$

Where A, B and C will be

$$A_1 = \begin{bmatrix} \frac{-(R_L+R_{on})}{L} & 0 \\ 0 & 0 \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, C_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{4.7}$$

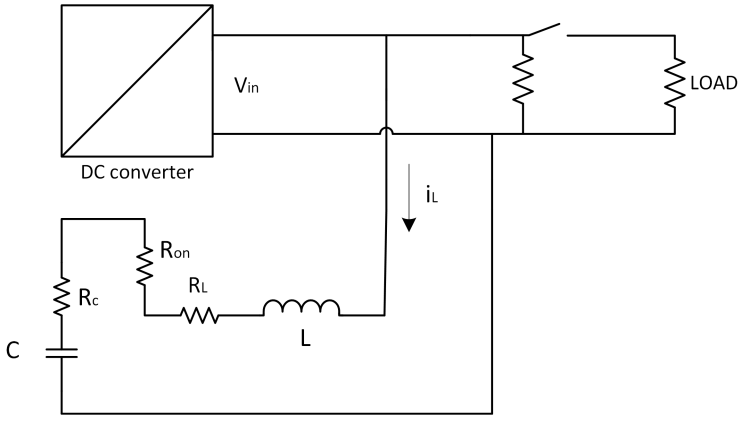

Fig. 4.4 Boost-Mode, Second state.

For the second state in Fig. 4.4, matrixes A, B and C will be

$$\frac{di_L}{dt} = \frac{1}{L}(V_{in} - i_L R_{total} + V_C) \tag{4.8}$$

$$\frac{dV_C}{dt} = \frac{i_L}{C} \tag{4.9}$$

$$A_2 = \begin{bmatrix} -\frac{R_{total}}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, C_2 = \begin{bmatrix} 1 & 0 \\ R_C & 1 \end{bmatrix} \tag{4.10}$$

2. Averaging the state space by using the duty cycle,

$$\begin{aligned} A_{AVG} &= A_1 d + A_2(1-d) \\ B_{AVG} &= B_1 d + B_2(1-d) \\ C_{AVG} &= C_1 d + C_2(1-d) \end{aligned} \tag{4.11}$$

3. Dividing signals to AC and DC components and using Laplace transformation

$$\begin{aligned} x &= X + \tilde{x} \\ d &= D + \tilde{d} \\ y &= Y + \tilde{y} \\ u &= U \end{aligned} \tag{4.12}$$

where the uppercase letters represent the steady state quantities and the small ac perturbations are represent by tilde notation.

4. Transfer function for small signal

Thereafter by integrating (4.1)-(4.12) together, dividing to DC and AC and using laplace transformation. The TF for small current changes will look like

$$\frac{\tilde{i_L}}{\tilde{d}} = \frac{s\frac{R_C I_L + V_C}{L} + \frac{I_L(1-D)}{LC}}{s^2 - s\frac{R_C D - R_{total}}{L} + \frac{(1-D)^2)}{LC}} \tag{4.13}$$

Where I_L is the steady state value, D and V_C is the initial values. The procedure for obtaining (4.13) is explained in more detail in [11].

4.2.2 Buck-Mode Model

The same procedure as for the Boost-Mode will be used in this section. But for creating a Buck-Model some simplification will be needed. The load current and the DC converter current will be summarize together. Therefore, by using this generalization a typical Buck-model can be used, which can be seen at Fig.4.5.

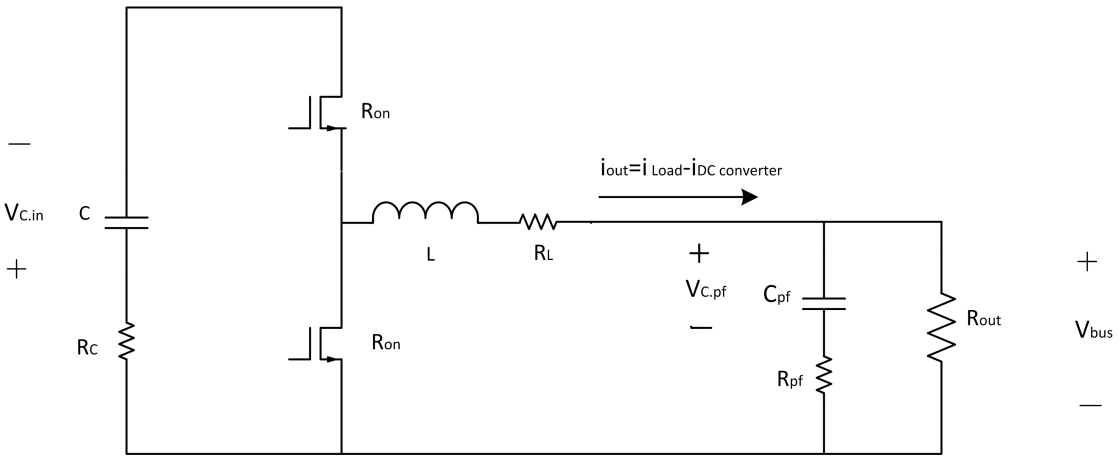

Fig. 4.5 Buck-Mode.

Where C will be the supply voltage in the model, C_{pf} is the passive filter, which is needed for taking care of the switching disturbance and R_{out} is the resistance for getting the desired i_{out}. The equation for the Buck-Mode during turn-on is derived from Fig. 4.5 and Fig. 3.8.

$$V_C = L\frac{di_L}{dt} + i_L(R_{on} + R_L) + V_{bus} \tag{4.14}$$

$$i_{out} = \frac{V_{bus}}{R_{out}} \tag{4.15}$$

$$V_{out} = V_C + R_C i_C \tag{4.16}$$

$$i_C = C\frac{dV_C}{dt} \tag{4.17}$$

then by using those equations, matrix A1, B1 and C1 can be derived.

$$A_1 = \begin{bmatrix} -\frac{1}{L}\left(R_{on} + R_L + \frac{R_{pf}R_{out}}{R_{pf}+R_{out}}\right) & -\frac{1}{L}\left(\frac{R_{out}}{R_{load}+R_{pf}}\right) \\ \frac{1}{C_{pf}}\left(1 - \frac{R_{pf}}{R_{pf}+R_{out}}\right) & -\frac{1}{C_{pf}}\left(\frac{1}{R_{pf}+R_{out}}\right) \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, C_1 = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{4.18}$$

During the turn-off time only one equation will be changed compared with the turn-on,

$$L\frac{di_L}{dt} = -i_L(R_{on} + R_L) - V_{bus} \tag{4.19}$$

therefore, matrix A2, B2 and C2 will look like

$$A_2 = \begin{bmatrix} -\frac{1}{L}\left(R_{on} + R_L + \frac{R_{pf}R_{out}}{R_{pf}+R_{out}}\right) & -\frac{1}{L}\left(\frac{R_{out}}{R_{load}+R_{pf}}\right) \\ \frac{1}{C_{pf}}\left(1 - \frac{R_{pf}}{R_{pf}+R_{out}}\right) & -\frac{1}{C_{pf}}\left(\frac{1}{R_{pf}+R_{out}}\right) \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, C_2 = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{4.20}$$

As a result of the new matrixes, the TF for the inductance current will be

$$\frac{\tilde{i_L}}{d} = \frac{\frac{V_{C.in}}{L}\left(s + \frac{V_{C.pf}}{V_{C.pf}C_{pf}(R_{pf}+R_{out})} + \frac{1-\frac{V_{C.pf}}{V_{C.in}}}{C_{pf}(R_{pf}+R_{out})}\right)}{\frac{R_L+R_{out}+R_{on}}{LC_{pf}(R_{pf}+R_{out})} + s\left(\frac{R_L}{L} + \frac{1}{C_{pf}(R_{pf}+R_{out})} + \frac{R_{pf}R_{out}}{L(R_{pf}+R_{out})} + \frac{R_{on}}{L}\right) + s^2} \tag{4.21}$$

where $V_{C.in}$ is decreasing as the capacitor discharge during the buck mode, which will impact the gain of the controller. Therefore, there is a need for a feedforward that will modify the gain of the regulator depending on the voltage level.

4.3 Simulations

This chapter presents how the design of both controllers(Buck/Boost) and the simulations have been execute. Simulations are done both in real- and discreet-time by using MATLAB SIMULINK.

4.3.1 Current Control Design

Since there are two different APF models, there are going to be two regulator. By using the TF from (4.13) and (4.21) in MATLAB toolbox Single-Input Single-Output tool (SISOTOOL), the regulator design process will be more simple. Both controller will be proportional-integral-derivative controller (PID controller). In this project the desired bandwidth frequency for the controller is 20kHz. This is because there is a need for a fast controller, but it should not be close to the switching frequency and the measurement system frequency. So by using a controller with 20kHz, the measurement system can have a bandwidth of 100kHz and the switching frequency 500kHz.

Figure 4.6 shows the open-loop diagram of the APF in Boost-Mode together with the regulator. The bandwidth frequency is around 20kHz and the phase margin is 80 degrees. It is important to have a phase margin around 80-90 degrees. Because when the controller is discretized the phase margin can be reduced by 20-40 degrees.

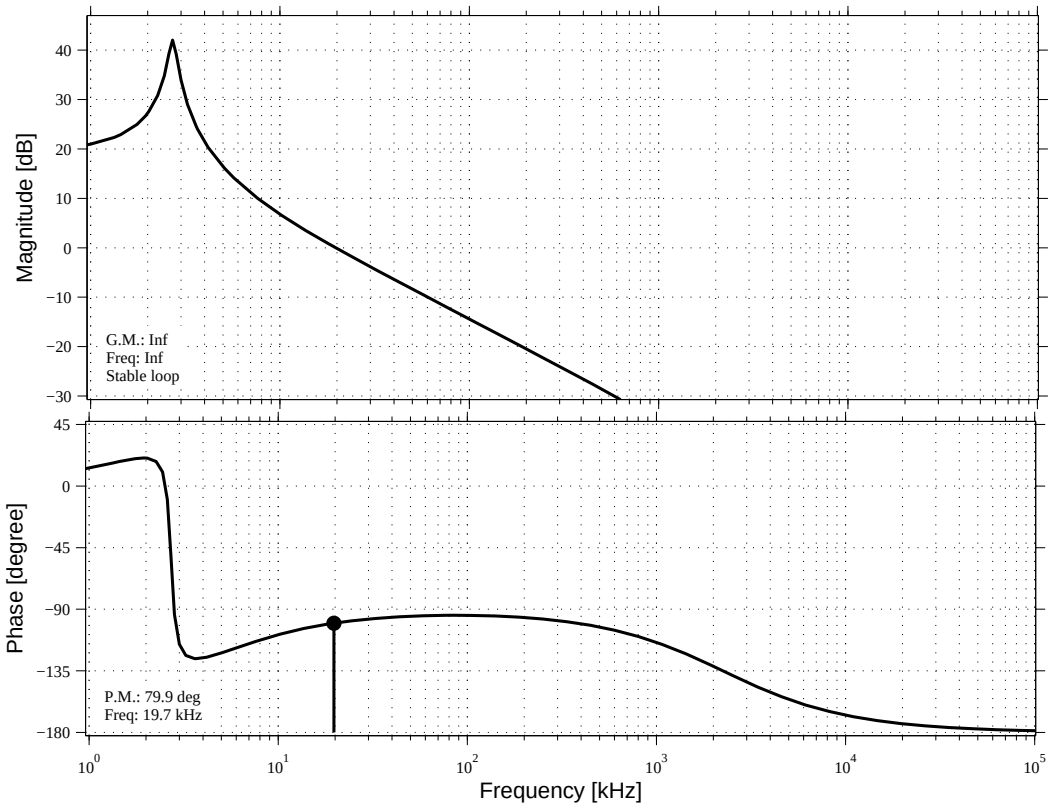

Fig. 4.6 Continues time Boost-Mode (Open-loop of the system with a regulator).

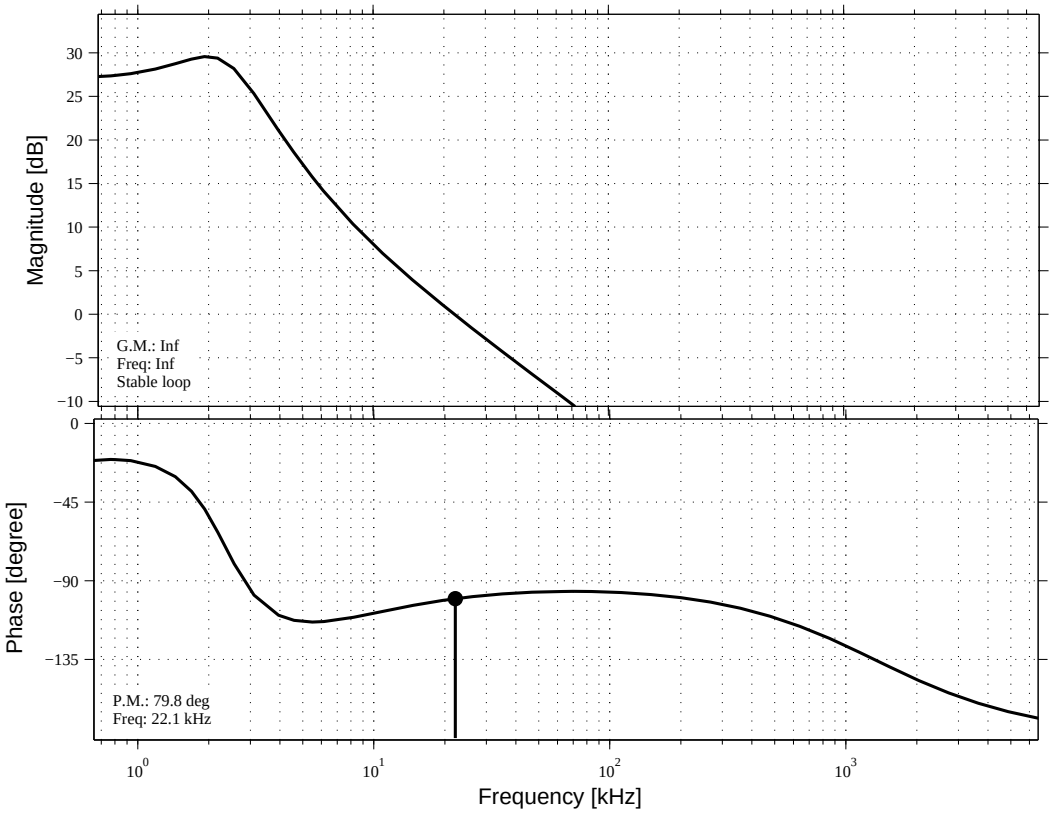

Fig. 4.7 Continues time Buck-Mode (Open-loop of the system with a regulator).

Figure 4.7 shows that the buck controller has a bandwidth frequency of 22kHz and a phase margin of 80 degrees. The completed Simulink model of the current controller(both Buck and Boost controller) that will be used for simulation can be seen in Fig. 4.8. In appendix C.1 there are more details about the subsystem contents.

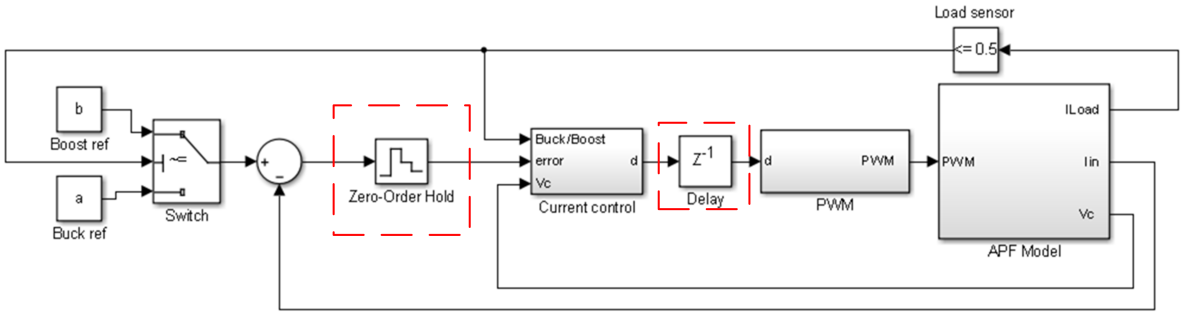

Fig. 4.8 Discrete time simulation of the current controller in Simulink.

The current controller is simulated in discrete time with the same sample frequency as the DSP. Where the red marks in Fig. 4.8 are the blocks that are needed for a discrete simulation. By erasing those blocks a continues time simulation can be carried out. The controller is discretized by MATLAB function $sysd = c2d(sys, Ts, 'tustin')$.

4.3.2 Voltage Control Design

The voltage control will be used for modifying the current reference when it get near the bus voltage and the rated voltage. The voltage control will be the outer loop, which can be seen in Fig. 4.9.

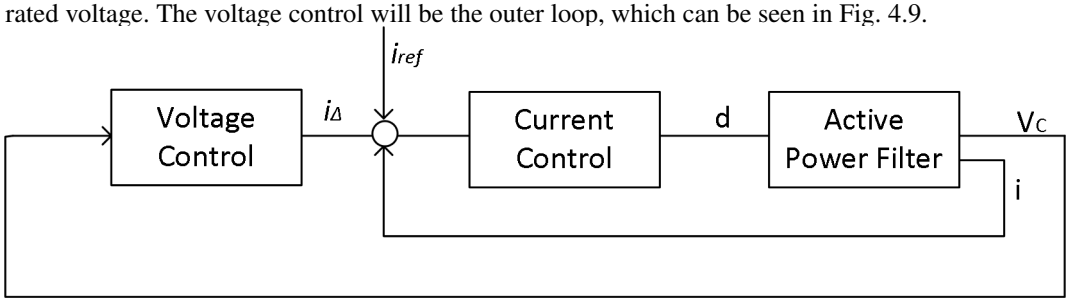

Fig. 4.9 The hole system with the Voltage Controller as the outer loop and the current controller as the inner loop.

The controller will compare the capacitor voltage with decided voltage limits. If the voltage will increase/decrease beyond those limits, the controller will modify the reference and by that decrease/increase the capacitor voltage after a couple periods.

4.3.3 Soft start design

Before the APF is turned on there is a need for charging the capacitor to the bus voltage. For this reason a soft start mechanism is introduced into the hardware, simulation and the DSP, Fig. 4.10.

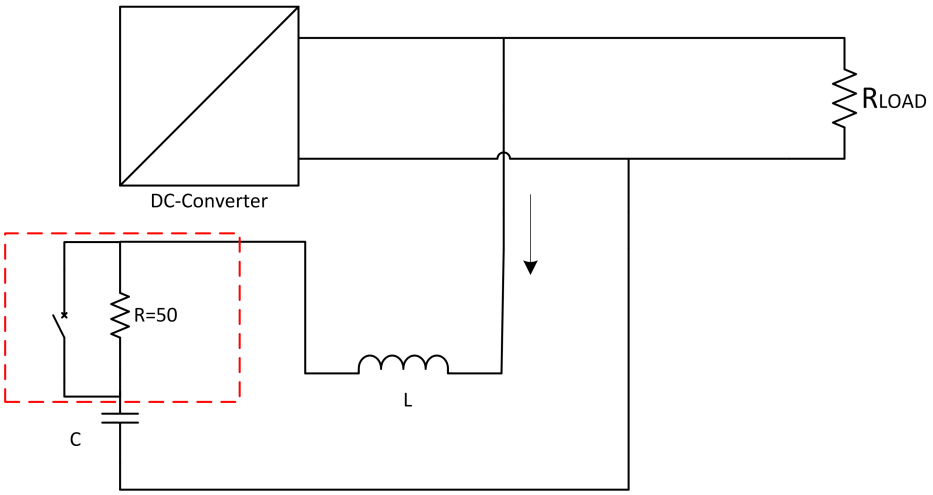

Fig. 4.10 Soft start setup during the startup of the APF.

A resistance is series connected with the capacitor during the charging time, which is limiting the current according to

$$I = \frac{V_{in}}{R} e^{-\frac{t}{RC}} \tag{4.22}$$

where V_{in} is the bus voltage. When the current reach zero then the capacitor is fully charged, which occur when $t > 4RC$. When the capacitor is charged a switch will disconnect the resistance. A resistance of 50Ω will cause a peak current of 0.64A ($I = 32V/50\Omega$), which is an acceptable value.

4.4 Digital Processor and Experiment Board

4.4.1 Choice of DSP

Today DSP market does not differ so much from last year. But there are some exciting products in development, which is expected to be released this year. Dual core DSPs exists, but there are no experimental kits with integrated ADC modules for these devices. Therefore, they will not be considered in this thesis due to the fact that main focus will be on the fundamental of digital controlled APF and not on DSPs. As a consequence, the same DSP as in last years master thesis [9] will be used. This is because there are no DSP that have considerable better clock frequency with the same modules integrated, which is required in this project. In addition, with this DSP, it is possible to use knowledge from [9], facilitating the set-up and programming.

Properties of the Delfino F28335 DSP:

- 150MHz clock frequency
- 1 dual 12-bits ADC modules: 80ns conversion time, 16 channels.
- 6 PWM modules
- 6 HR-PWM outputs
- 3 32-bits CPU timers
- Serial Peripheral Interface (SPI)
- 88 General Purpose I/O pins (shared)
- 3.3V output
- Floating-point-unit

4.4.2 Experiment Board

In this thesis an experimental kit for the DSP will be used, TMSDOCK28335. It contains a breakout board for all necessary pins on the processor as well as a Universal Serial Bus (USB) programming and debugging

interface.

4.4.3 DSP Set-Up

It is possible to synchronize and phase shift the switching signals of the APF with the DC/DC-converter at the bus in order to make some of the switching components to cancel each other out. Therefore, the same switching frequency of 500kHz will be used in the APF. But due to lack of CPU cycles per PWM period, there have not been any effort of integrating the APF with the DC/DC-converter. The number of CPU cycles per PWM cycle will be [10]

$$N = \frac{f_{CPU}}{f_{PWM}} = 300 \tag{4.23}$$

Most of the CPU operations are done in one or two clock cycles. Some floating point instructions, such as multiplication and division needs several clock cycles to operate. The program structure is shown in block diagram form in Fig. 4.11. The left block column shows the normal operation in the DSP upon turn on of the processor and during idling. Non time critical code is processed in an infinite loop in the Main function of the code. When an interrupt occurs from the PWM module, the right column of the blocks in Fig. 4.11 are processed. When all code is done in the interrupt routine, the processor returns to the same point in the infinite loop as it was before the interrupt occurred.

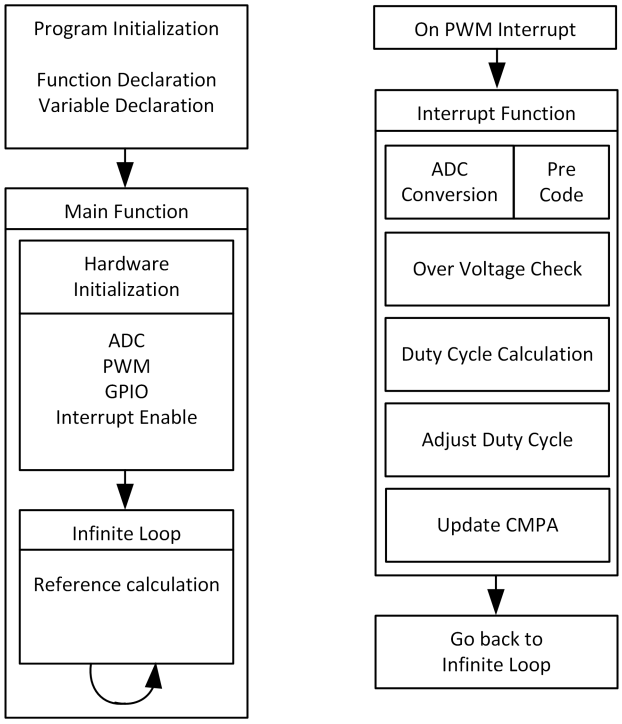

Fig. 4.11 Block diagram over the DSP program layout. Left blocks show the startup and idle code block. Right blocks show the interrupt routine trigged by the PWM module.

The DSP execution process need to be planed, so there will be a sufficient time for all the needed processing during the PWM cycle. How this is done is shown in Fig. 4.12. At every CMPA hit, the ADC is started as well as the PWM interrupt routine, which contains all program code necessary to calculate a new duty cycle to be loaded into the CMPA register before next PWM cycle.

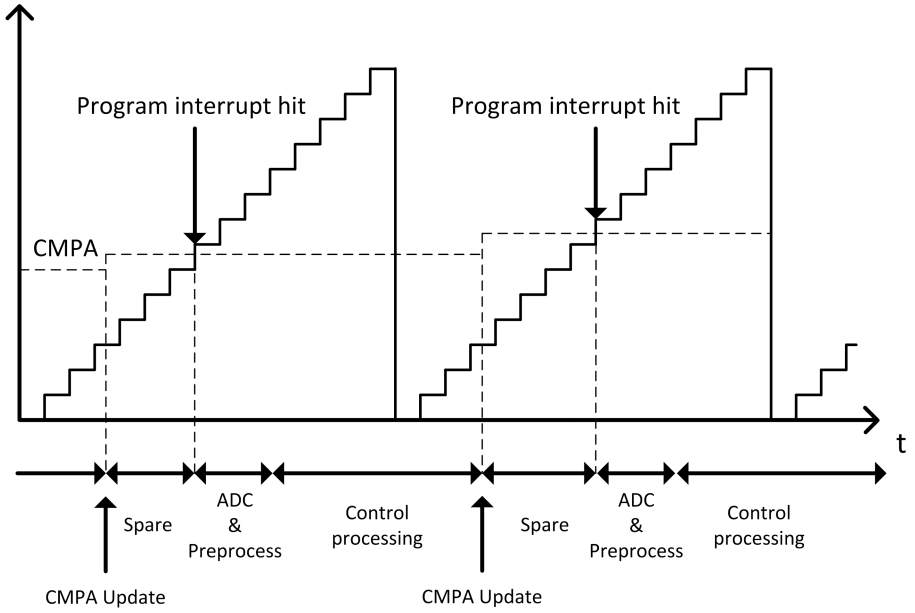

Fig. 4.12 Pulse Width Modulation during a couple of periods showing were the ADC module and control code starts in order to calculate the duty cycle for next coming period.

As mention at chapter 4.2.2 there is a need for a feedforward loop for modifying the gain of the regulator dependent on the capacitor voltage. But because the lack of operation cycles this feature will not be included in the DSP. As a result, there are going to be some error in the current when the voltage decrease.

For programming the DSP, a software development program from Texas instruments, Code Composer Studio v5, has been used. The program code that has been used for controlling the APF can be seen at Appendix A.1.

4.5 Hardware

4.5.1 Measurement System

For controlling the APF three measurement points are required, the DC/DC converter output current, load current and the storage capacitor voltage. Figure 4.1 shows where those points are located. The measurement signals are sent to the DSP through four coaxial cables. This makes it possible to isolate the measurement signals from noisy environment i.e. disturbance in the vicinity of switching components and the inductance.

Current measurement

The load current and the current before the APF will be measured by installing two resistors on the DC bus side. By using the differential amplifier setup it is possible to measure the voltage drop over the resistor.

For designing the current measurement system on the DC bus side, the common-mode voltage is needed to be considered, which is 32V. Also this project DSP can manage input signals between 0-3V. Therefore, a supply voltage of 3V will be used to the selected differential amplifier. As a result of supplying voltage of 3V and common mode voltage of 32V there are going to be a distortion in the signal. Therefore, a current sense-amplifier LMP8640HV has been chosen. It has a common-mode range of between -2V and 76V(independent of the supply voltage), rail to rail voltage and has a bandwidth filter of 950kHz. For this reason, a supplementary low pass filter will be added for damping the switching frequency 500kHz. It also have a build in gain of 20.

The maximum current drawn from the DC/DC converter is around 1.5A, which is the peak load current. When the APF is working as it should, the input current will be constant around 0.15A. Therefore, the selection of the sensor resistance will be calculated by

$$V_{SENSE} = \frac{V_{DSP,MAX}}{Gain} = \frac{3V}{20} = 0.15V$$
$$R_{SENSOR} = \frac{V_{SENSE,MAX}}{I_{MAX}} = \frac{0.15V}{1.5A} = 0.1\Omega \tag{4.24}$$

0.1Ω is a good value because it will be less sensitive to distortion and will give acceptable power loss of 2.25mW. As mentioned before the ADC use 12 bit resolutions, which gives up to 4096 steps (chapter 3.15). Thereby with 3V maximum input voltage to the DSP, the minimum voltage step will be according to (3.15) 0.73mV.

Therefore, if the DC-converter is sending out 0.15A the voltage drop over the sensor resistance is 15mV. Due to the 20 gain, this will result to 0.3V signal to the DSP. This signal will give a resolution of 410. It is desired to come closer to the available range 4096. But because it is important to have the possibility of measuring currents up to 1.5A (current overshoots and so on) no additional gain will be added. By using Pspice and the information from chapter 3.4, a desirable bandwidth could be acquired. The frequency is desired to be around a factor five lower then the switching frequency and a factor five higher then the controller, according to chapter 4.3.

It is worth to mention that this type of design can be modified later by changing the sensor resistance and in this way modify to a new specific current range. The load current measurement can be executed with the same setup as for the input current, just different sensor resistance is needed if a higher current is desired to be measured.

Voltage measurement

For the capacitor voltage measurement the voltage can be as high as 80V and the DSP can manage input voltage of 3V,

$$V_{out} = V_{in}\frac{R_2}{R_2+R_1}$$
$$\frac{V_{out}}{V_{in}} = \frac{3V}{80V} = \frac{R_2}{R_2+R_1} = 0.038 \tag{4.25}$$

where V_{out} is the DSP input signal and V_{in} is the voltage over the capacitor. It is also important consider that the resistors size should be in magnitude of $10k\Omega$, for preventing the current to flow through the voltage divider. Also low pass filters will be added with the gain one and bandwidth frequency that is factor ten lower then the switching frequency.

4.5.2 Switching Stage

MOSFETs will be used as they are considered the best choice when it comes to low power application with high switching frequency [7]. Therefore, a comparison between a couple of MOSFETs will be made in this section regarding power dissipation properties.

	FAIRCHILD FDS86140	VISHAY SI4100DY-T1-GE3
V_{DS}	$100V$	$100V$
I_D	$11.2A$	$6.8A$
R_{on}	$8.1m\Omega$	$51m\Omega$
C_{oss}	$440pF$	$90pF$
$W_{on,0.2A}$	$1.6nJ$	$10.0nJ$
$W_{on,1.5A}$	$12.15nJ$	$76.50nJ$
$W_{sw,32V}$	$225.2nJ$	$46.1nJ$
$W_{sw,55V}$	$665.5nJ$	$136.1nJ$

Table 4.1: A comparison between two MOSFETs.

A low on-resistance, R_{on}, in the MOSFET is desirable to get low conduction losses in the circuit, but a low resistance is also associated with large chip size. Large chip size is in turn related with high output capacitance between drain and source of the MOSFET, C_{oss} [11]. A consideration must be taken between low R_{on} and a low C_{ds}. Two MOSFET compared is shown in Table 4.1 with different parameters, one with low R_{on} but high C_{oss} and one with high R_{on} but low C_{oss}. Both transistor have a V_{DS} of 100V in order to handle the voltage of up to 80V over the storage capacitor in the APF. The energy dissipation during conduction with a t_{on} time of $1\mu s$ and a drain current, I_D of 0.2A respective 1.5A during a switching period

$$W_{on} = I_D^2 R_{on} t_{on} \tag{4.26}$$

is calculated for the two transistors and shown in the table. The output capacitance energy dissipation during a switching period

$$W_{sw} = \frac{C_{oss} V_{DS}^2}{2} \tag{4.27}$$

with two different voltages, 32V and 55V is also shown in the table. The Fairchild MOSFET in the table suffer of high losses due to the output capacitance. Therefore, the MOSFET VISHAY SI4100DY-T1-GE3 was chosen. Other MOSFET exists with even lower C_{oss} but they comes with lower current handling properties. Rise and fall time switching losses are about the same for the two different MOSFETs with only a slightly higher loss in the chosen one.

4.5.3 Drive Circuit

In this project the switching stage of the APF will only need to work in two quadrants so a half bridge will be implemented. In switching applications it is of great importance that the turn on and turn off times are as short as possible. This is important for low power losses during switching. Due to the capacitive nature of the gate in a MOSFET a fast turn on will need a high current pulse to charge the gate capacitor under as short time as possible. The $3.3V$ logic signal from the DSP is a low current 4mA signal that needs to be amplified by the use of a gate driver circuit. For the MOSFET chosen in this project VISHAY SI4100DY-T1-GE3, the total gate charge is around $14nC$ [4]. With an arbitrary chosen turn on time of 30ns a gate current pulse of

$$I_G = \frac{Q_G}{t_{SW,ON}} = \frac{14nC}{30ns} = 0.47A \tag{4.28}$$

will be needed, where Q_G is the total gate charge and $t_{sw,ON}$ is the time for the MOSFET to turn on. The gate driver circuit HIP4081A can deliver this gate current for up to four switches [6]. Two outputs will be needed for the half bridge upper and lower MOSFET and one output will supply the soft start bypass transistor.

Other important features that the drive circuit will handle are level shifting and boot strap charging. Due to the different voltage levels in the circuit where the MOSFETs are connected, the gate driver needs to adapt the control signals to these voltages. This feature is integrated into the HIP4081A but the boot strap will need additional external components such as diodes and capacitors. The boot strap circuit is used to supply the gate driver for the upper transistor in the half-bridge converter. The capacitor will act as an elevated $15V$ source over the DC-bus voltage supply during the time when one upper MOSFET is on, during a switching period. While the off period, the capacitor will be charged from the drive circuit power supply through a diode.

4.5.4 Passive Filter, Choke Inductance and Storage Capacitor

- Storage Capacitor

  Consider the discussion at Chapter 2.1, where Fig. 2.1 shows the different capacitor values versus the voltage ripple over the capacitor. A capacitor of value $22\mu F$ is selected, which need a voltage ripple of 18V for storing the needed load energy.

  One of the project requirements is to select a capacitor with a good voltage marginal from the rated voltage. Consider that, 100V voltage rating and operation voltage range up to 80V has been decided.

The reason for 80V is because the voltage controller at the moment is not complete and the voltage may not decrease to the bus voltage 32V before the load step is passed. Due to this, the next load period the voltage will get higher and so on. However the voltage controller will manage to keep the voltage between 32V and 80V.

- Inductance

For making it possible to increase the voltage over the storage capacitor an inductor need to be connected in series. The value of the inductor is critical in this project. The inductor value will effect the current ripple in steady state and the current slope. Both are crucial. The current ripple due to switching frequency and inductor value, should not be too large during the Buck-mode, Because then the inductor current will pass the zero axis. The slope is important for the rise/fall-time when the load is turned on/off. The inductor minimum value can be calculated when the load is low, which is when the current is closest to zero

$$V_L = L\frac{di}{dt}$$

$$\Delta i_{MAX} = 2i_{LOW.LOAD.AVG} = 0.3A = \frac{V_L}{2f_{SW}L} = \frac{32V}{2 \cdot 500kHz \cdot L} \tag{4.29}$$

$$L \geq 107\mu H$$

so by using as small inductor as possible the current slope will be more steep. Steeper current slope will give fast current response when the load is turned on/off. Therefore, the inductor with a value close to $107\mu H$ will be used. The behavior of the current can be seen in Fig. 4.13.

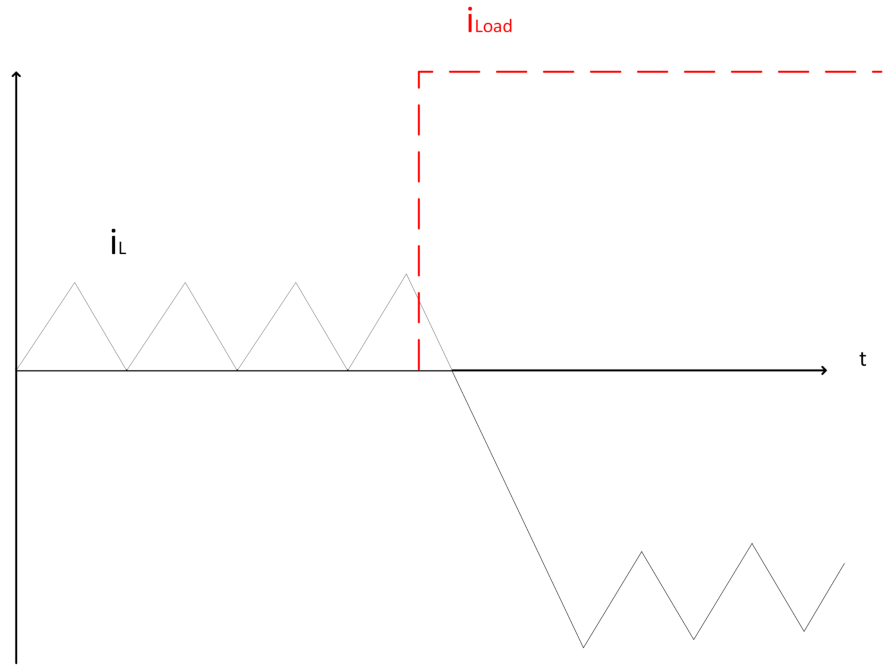

Fig. 4.13 The behavior of the inductance current when L=$107\mu F$ and switching frequency of 500kHz.

Figure 4.13 shows that it is important to have steep slope, but because of limitation that comes from the current ripple, the performance can not be better in this case. One suggestions for improving the rise/fall-time is to increase the switching frequency. However this will not be done in this Master Thesis.

- LC Filter

There is also need to consider the switching frequency distortion. Such distortion can impact the APF's measurement signals and effect the APF controller. Therefore, a passive filter will be used. The inductance that already exists in the circuit can be used as part of the LC Filter, the only additional component that is required is a capacitor. The placement of the additional capacitor can be seen in Fig. 4.14.

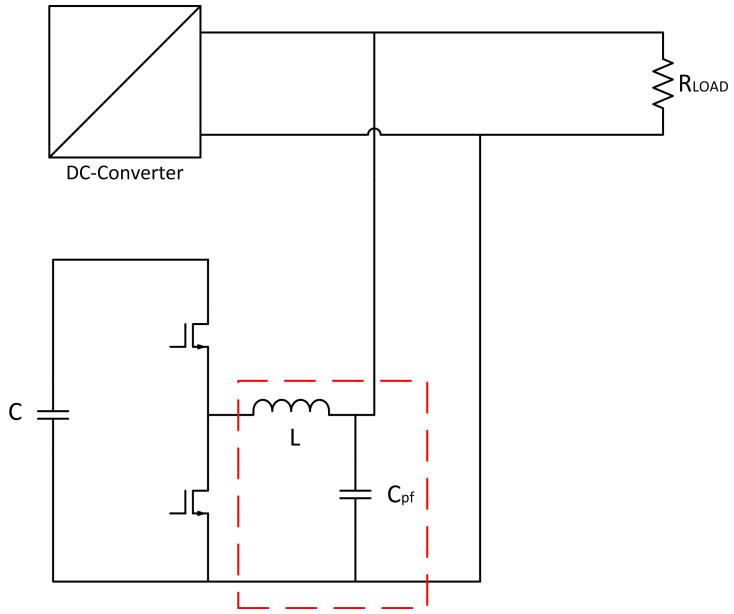

Fig. 4.14 Passive Filter setup with the APF.

Where C_{PF} is the passive filter capacitor. The value of the Passive Filter capacitor is calculated from

$$i = C\frac{dV}{dt} \tag{4.30}$$

$$C = \frac{i_C}{\Delta V 2f} = \frac{0.3A}{10mV \cdot 2 \cdot 500kHz} = 30\mu F \tag{4.31}$$

where I_C is the current ripple that cause of the inductance, ΔV is the allowed voltage ripple and f is the switching frequency.

4.5.5 Printed Circuit Board

In order to realize the APF in a hardware prototype, a Printed Circuit Board (PCB) was designed. The computer program Eagle 6.4.0 Student Edition was used to make a layout. First a two layer card with the power components on the top and the measurement system on the bottom layer was made. Unfortunately, capacitive effects was noticed in the current measurement signal, caused by switching currents in the PCB traces to and from the inductance on top. By this fact and that measurement signals must be kept away from the noisy environment caused by the switching components in the circuit, a separate current measurement card was designed. The latter card contains the current sensed amplifiers and filters with coaxial connection to the DSP, as well as the PPF for the bus. A complete overview of the PCBs can be found in the Appendix B.1. It should also be noted that the PCB is not a minimized solution and has extra space for additional components for modification purposes.

4.6 Evaluation of the Active Power Filter

This chapter will go through how the hardware and software have been evaluated and tested.

- Measurement System
  At first, a signal generator was used for generating a signal with a varying frequency between 10-500kHz over the sensor resistor/voltage-divider, where the output signals to the DSP was examined. After verifying the bandwidth frequency, the next step was to inspect the measurement system when the APF is up and running. If the DSP signals from the measurement system was stable, no additional tests were made.

- APF Performance
  The current mitigating performance on the DC-bus was evaluated with a DC current prob connected to an oscilloscope. It was connected to different measurement points, arranged and numbered as in Fig. 4.15. The voltage over the capacitor and at the DC-bus was also acquired. The 32V voltage level is from the DC/DC-converter used in [9], but with an analog regulator, thereafter connected to a laboratory 56V supply. The pulsed load was simulated with an electronic load connected to the bus and the setup was according to Fig. 4.15.

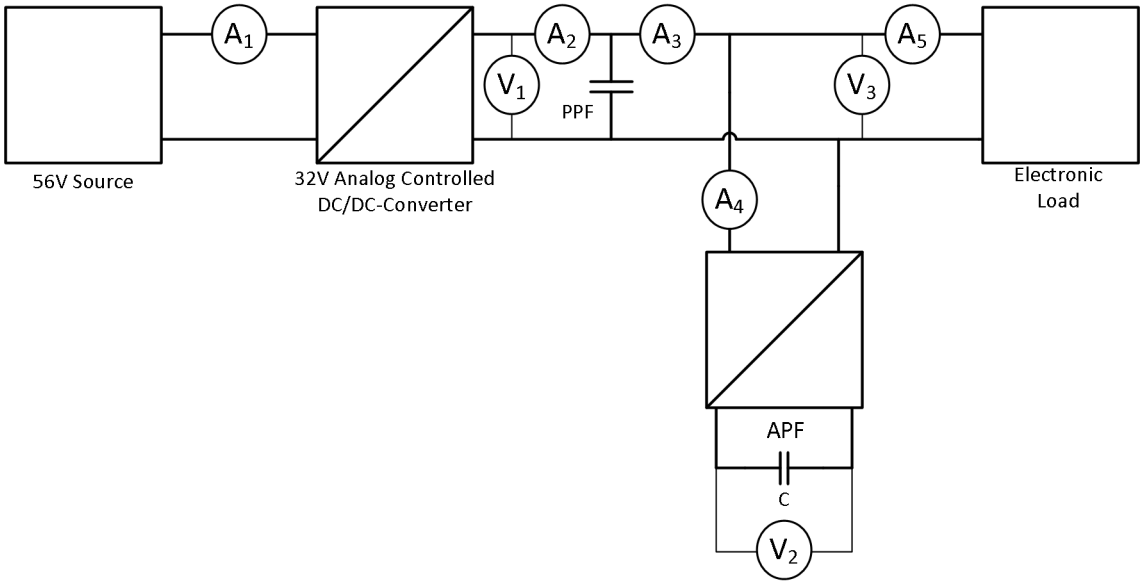

Fig. 4.15 Measurement points, which have been used in the laboratory.

During the APF run-up, it was noticed that when the load step came, oscillations occurred on the inductor current. This is because of inaccuracies in the buck-model, which used in SISOTOOL to acquire the PID-controller. Therefore, adjustments of the parameters was performed by trial and error tweaking by tuning the coefficient of the differential equation in the DSP. This was done in real time with the APF running.

- Efficiency
  The efficiency of the APF was evaluated with the help of four Fluke multimeters arranged at points A_2, A_5, V_1 and V_3. Where the input power was compared with the power delivered to the load.

Chapter 5

Results

In this chapter the results of simulation and measurement will be presented and evaluated. The simulation and the APF parameter is seen in Table 5.1.

L	$100\mu H$
C	$22\mu F$
$C_{passive.filter}$	$1100\mu F$
$C_{SW.passive.filter}$	$44\mu F$
$R_{SW.passive.filter}$	1Ω
R_L	0.1Ω
R_C	$8m\Omega$

Table 5.1: The parameter values that has been used in the simulation of the APF.

5.1 Simulation

In this part the results from simulations of the current control will be presented. The simulation of the APF is done by using Simulink, which is using ideal components. Therefore, the DC-converter is called DC-source in this chapter.

Three plots will be presented: the inductor current, the DC-Source current and the storage capacitor voltage. Figure 5.1 shows the DC-Source current and the load current over one load period. The placement of the measurement can be seen in figure 4.15 at point A_2 and A_5.

When the load is at its low state in Fig.5.1, the ripple of the DC-source current is around the reference value 0.17A, which is a good result. During the load step, an inrush from the DC source current will occur, this is due to selection of the inductor size, which have been explained at the section 4.5.4. But otherwise the results during the Buck-Mode is sufficient.

Figure 5.2 present the inductor current and the load current, where the placement of the measurement can be seen in figure 4.15 at point A_4 and A_5.

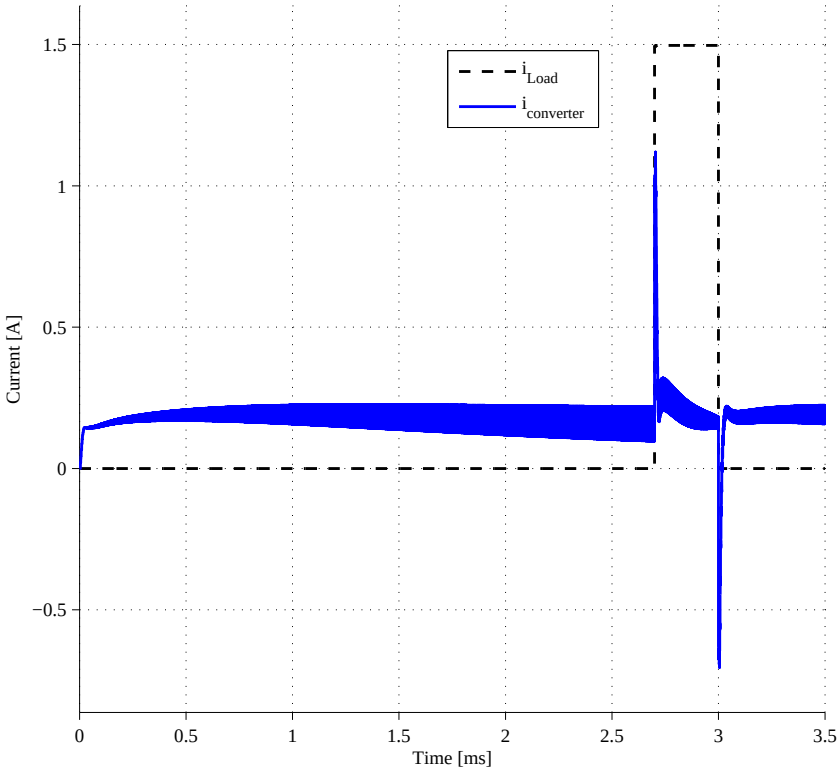

Fig. 5.1 Plot of the DC-source current and the load current over one load period.

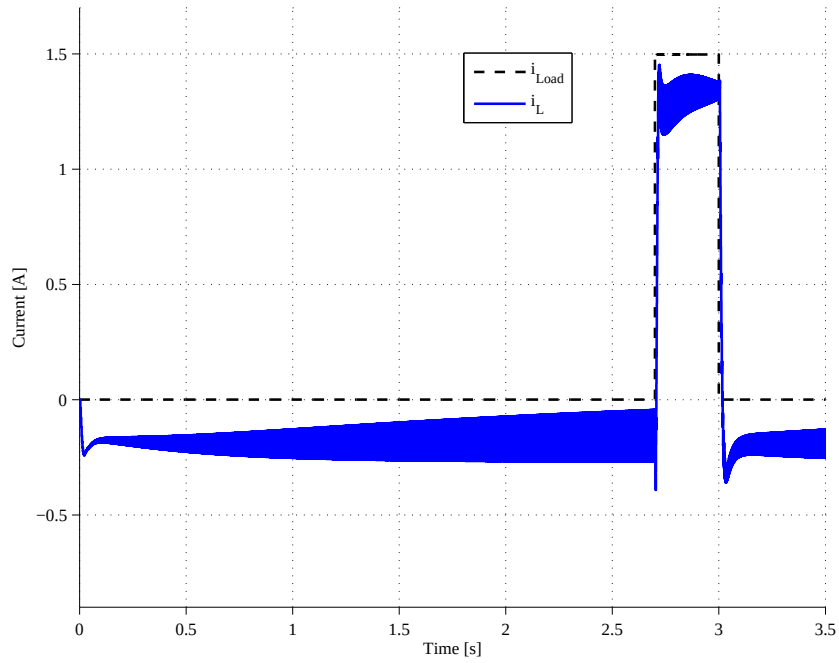

Fig. 5.2 Plot of inductance current and the load step over one load period.

Figure 5.2 shows how the APF is storing/relesing energy, which is seen on the current sign and the amplitude. The overshoot that occurs at the start and in the end of the load step is due to the regulator design, which was a difficult task to improve further. The overshot in the beginning of the load step occurs due to the inductor current slope, which creates a large error signal to the regulator.

Figure 5.3 presents the voltage over the capacitor during two load periods. The voltage controller is not implemented in this simulation. Also an incorrect current reference is used in this simulation for demonstrating the effects.

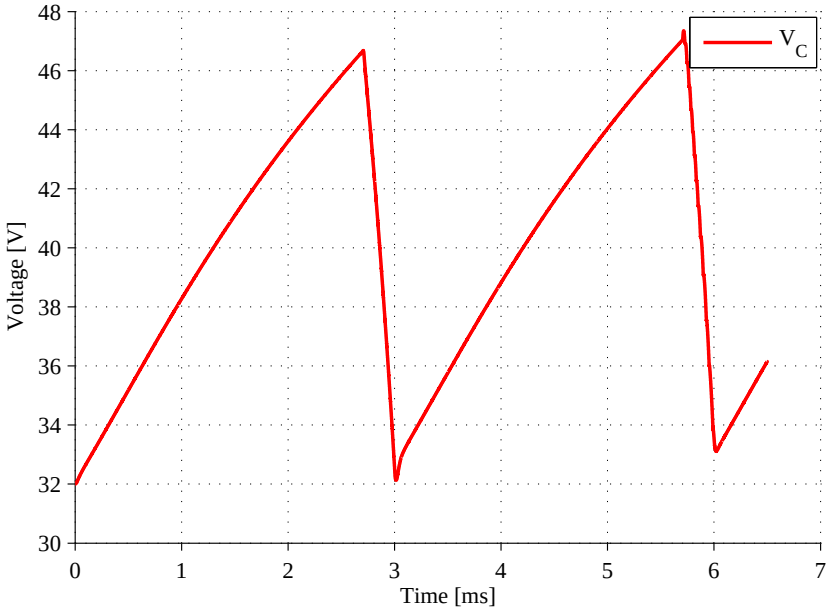

Fig. 5.3 The storage capacitor voltage with a too high reference value.

Figure 5.3 shows how the voltage over the storage capacitor is increasing/decreasing, which is indicating the charging/dichagring of energy when the load is high/low. It should also be noted that the voltage over the storage capacitor has reached a higher state in the second period and it will get higher for each period. This can be explained by the use of an incorrect current reference. Results point out the need of an outer control loop that adjusts the reference value, so that the capacitor voltage will be under control. For this reason, a voltage controller has been introduced in this thesis work, which is explained at section 4.3.2.

5.2 Passive Power Filter

Before presenting the APF performance, figures of how the current behaves with a PPF will be demonstrated. Figure 5.4 shows the current on the 56V bus without the APF been activated. However, the passive filter that the APF is using is connected, which is in the magnitude of $C = 1100\mu F$. The measurement is carried out at placement A_1 at Fig. 4.15.

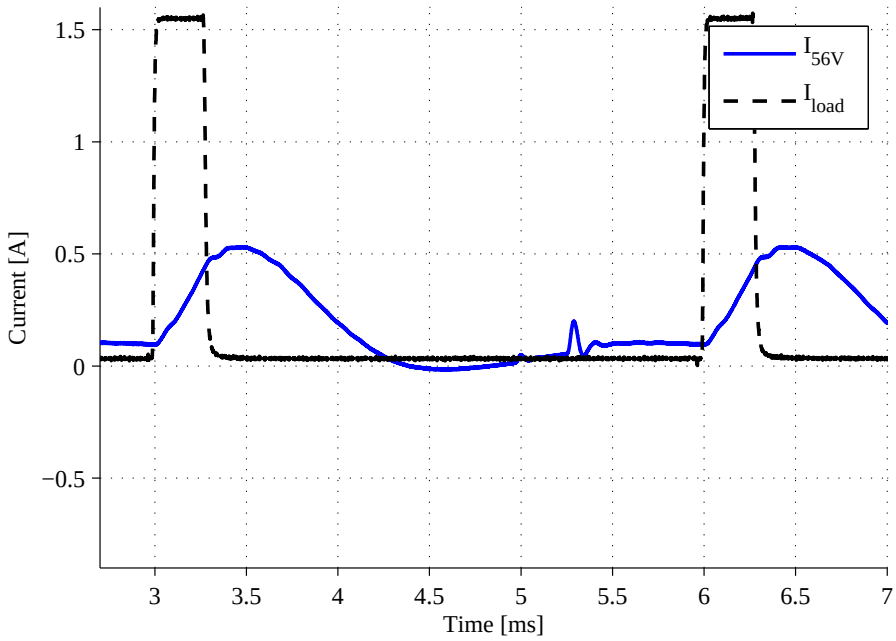

Fig. 5.4 Shows the Current on the 56V bus when the APF is not active, but with the PPF ($C = 1100\mu F$).

Figure 5.5 shows the output current from the DC/DC converter. The measurement is carried out at placement A_2 at Fig. 4.15.

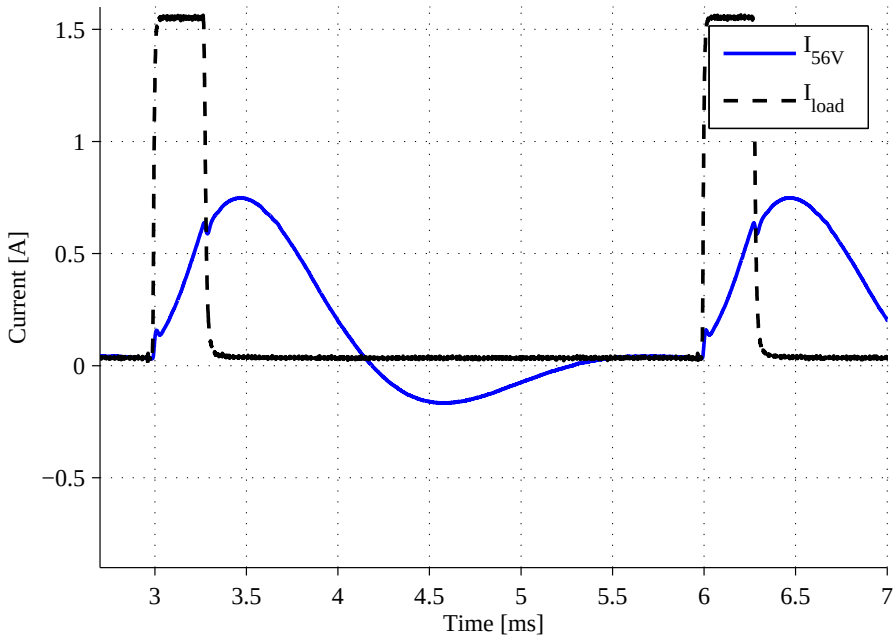

Fig. 5.5 Shows the output current from the DC/DC converter when the APF is not active, but with the PPF ($C = 1100\mu F$).

The reason for the current to differ from Fig. 5.4 is because the DC/DC converter has input capacitor which acts as buffer. In conclusion, the DC/DC converter with the passive filter do not take care of the low frequency ripple. Owing to this, there is a need for improvement.

5.3 Active Power Filter

5.3.1 Filter performance

The performance of the filter will be presented by showing the results from the oscilloscope measurement. Figure 5.6 presents the current from the 56V voltage source, that supplies the DC/DC-converter. The measurement is carried out at placement A_1 Fig. 4.15.

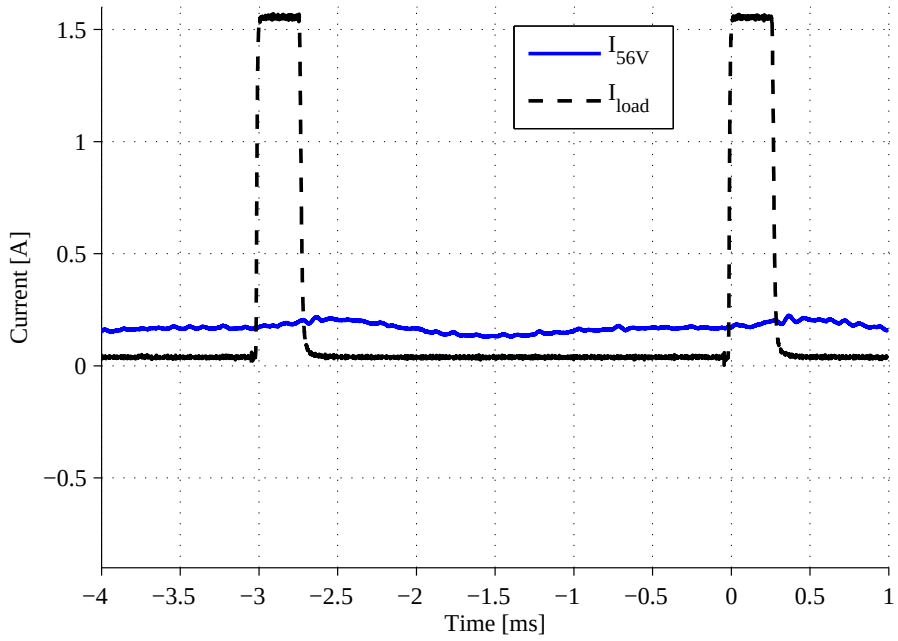

Fig. 5.6 Current from the 56V voltage source.

The current in Fig 5.6 oscillates between 0.13A and 0.22A, which is caused by a conflict with the DC-converter controller, which is trying to keep the bus voltage constant. Otherwise, the effects from the load step is properly attenuated.

Figure 5.7 shows the output current from the DC/DC-converter , on the 32V voltage side. The measurement is carried out at placement A_2 Fig. 4.15.

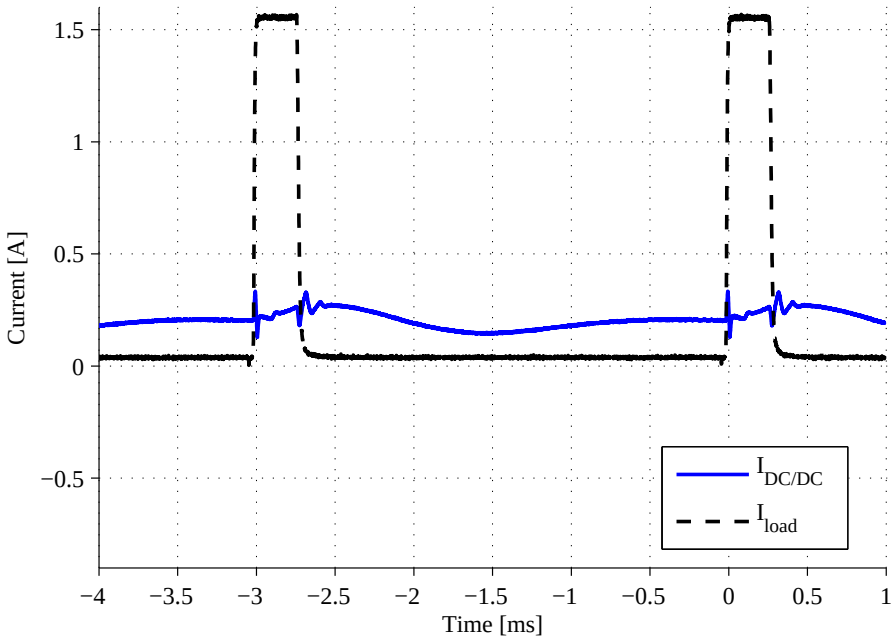

Fig. 5.7 Current output from the DC/DC converter to the 32V bus.

Figure 5.7 shows the similar behavior as recorded at the 56V-side. The significant different compare with the 56V side is that on the 32V side has visible overshoots. The reasons for the overshoots to be damped on the 56V-side is that the DC/DC converter has input capacitors, which acts as buffers.

Figure 5.8 shows how the current between the external passive filter and the APF looks like. The measurement is placed at A_3, Fig. 4.15. In other words, this is how it would look like at the output of the DC/DC-converter without the external passive filter.

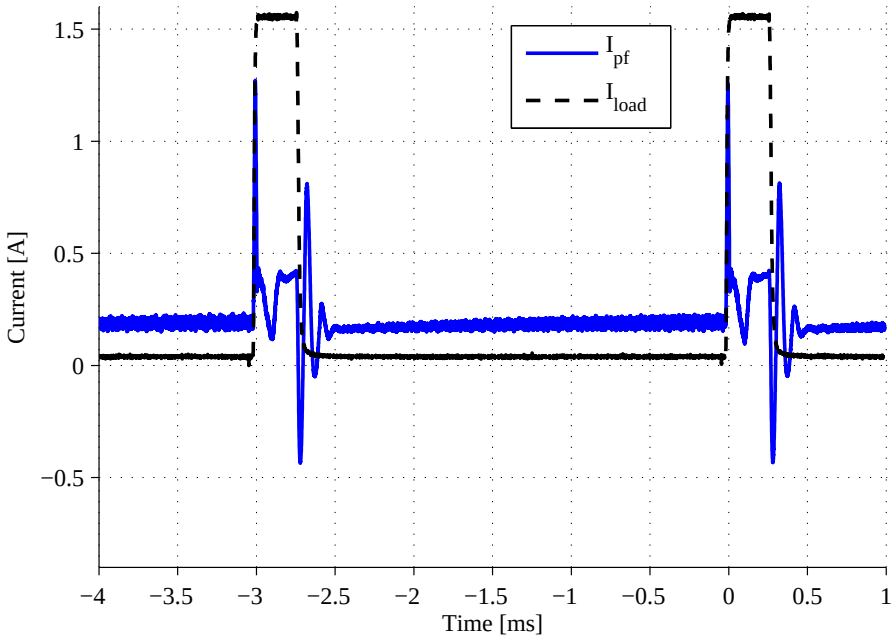

Fig. 5.8 The current between the passive filter and the APF.

The plot show that in the Buck-Mode there are some error in the steady state value. The current settles around 0.4A, which is far from the reference value of 0.15A. One reason for that, could be that the gain adjustment feedforward loop had not been implemented, which was pointed out in chapter 4.4.3. Another reason could be that the digital control parameter was modified for damping the current oscillation, chapter 4.6. These parameter modification comes with a cost which could be what is seen in the Fig. 5.8.

Figure 5.9 presents the inductance current, which is the current that goes in/out from the APF. The measurement is carried out at placement A_4 Fig. 4.15.

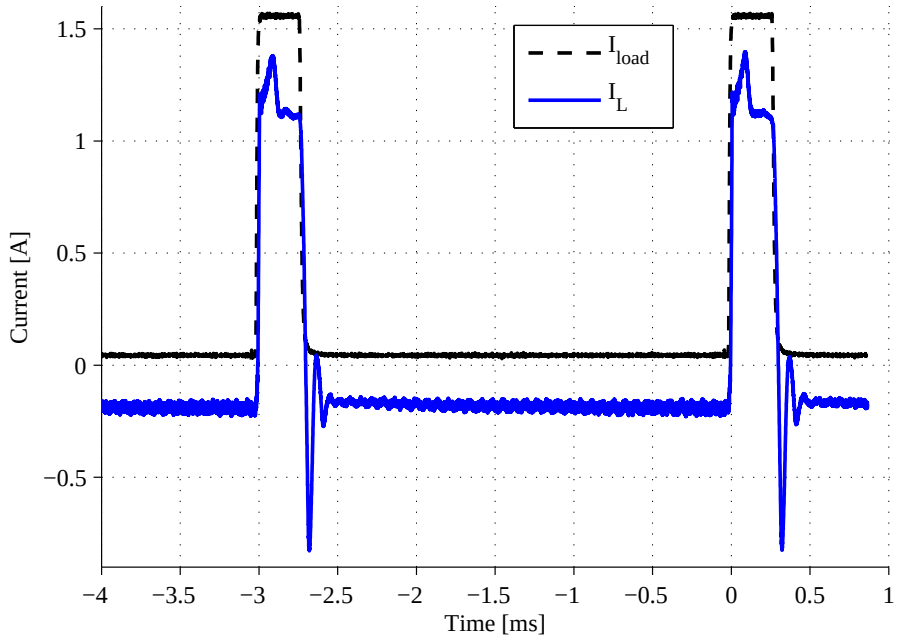

Fig. 5.9 Inductor current, which is the current from the APF.

Figure 5.9 shows how the APF is storing energy during the Boost-Mode and releasing energy during the Buck-Mode, so in overall the device is doing its design purpose. It also shows a peak placement. This peak placement is depending on the current references value. In this case the reference was tweaked manually. Yet the peak value at the beginning and the end of the load step are not larger then the load step amplitude. Therefore, the results of the APF is sufficient.

Figure 5.10 shows the voltage over the storage capacitor. It also shows how the storage capacitor is charging energy and releasing energy. The measurement is carried out at placement V_2 Fig. 4.15.

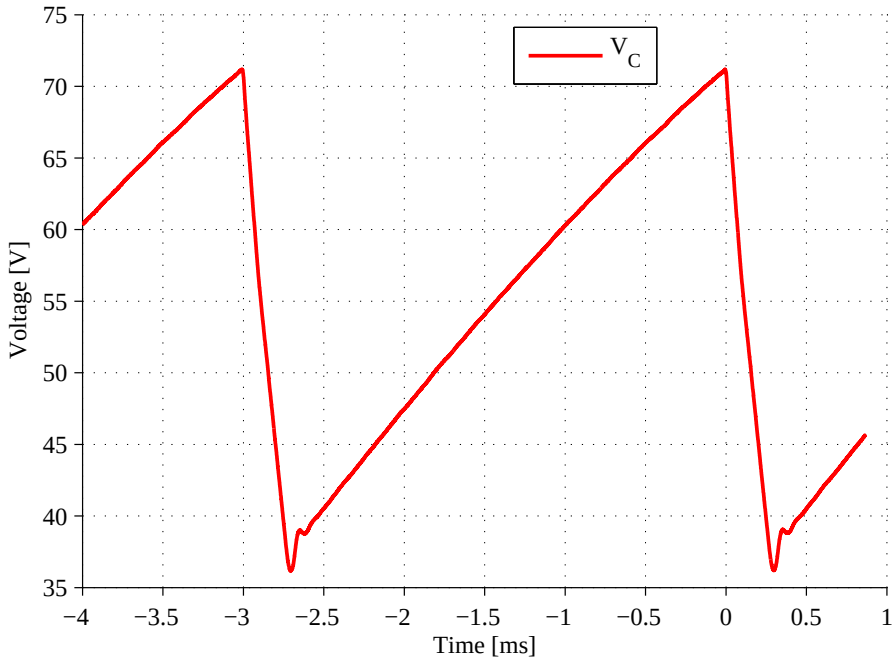

Fig. 5.10 The energy storage capacitor voltage.

It can be seen that the peak value is the same and that the system is working in stable state. That means that the reference value is stable and that the voltage controller is working properly. This test was also performed over longer time and the results showed to be the same. At the end of the load step it can be noted that the voltage ”jumps-up” in the beginning of the next period. This is caused by the current overshoot from the APF (Fig. 5.9) which has the magnitude of 0.9A.

Figure 5.11 show the AC voltage on the 32V bus. The measurement is carried out at placement V_3 Fig. 4.15.

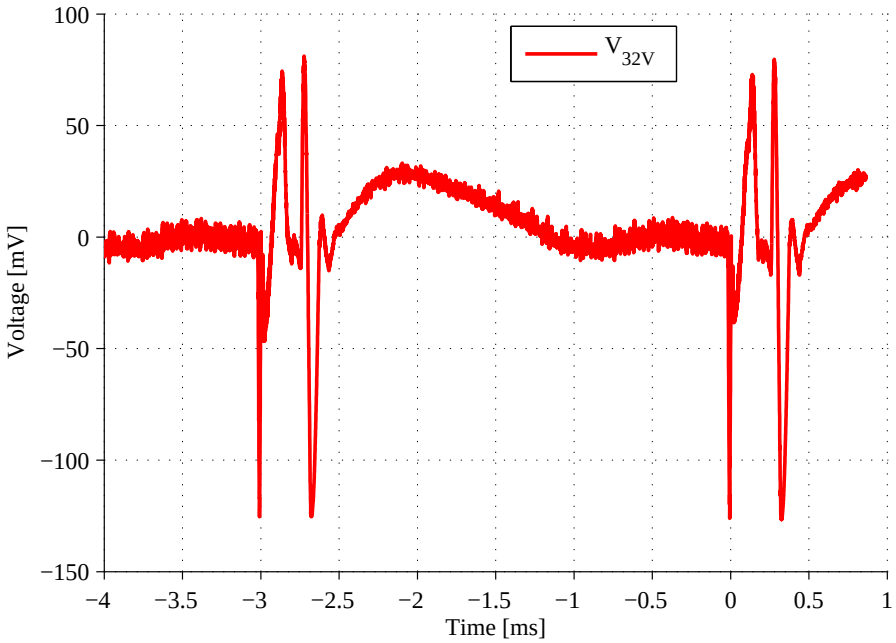

Fig. 5.11 The AC voltage on the 32V bus.

It can also be noted that during the load step the voltage on the bus will drop with 120mV and also oscillates between -120 and 80mV. The DC/DC converter will try to decrease this voltage drop. This will cause a conflict with the APF control, which can be seen on the voltage after the load step is finished. This can also be seen on the current on the bus at Fig. 5.6-5.7. One way to solve this is to synchronize the switching frequencies of the devices and phase shift one of the devices with 180 degrees.

5.3.2 Efficiency

The efficiency of the APF was measured with the setup as in Fig. 4.15. When a precalculated current reference was used an efficiency of 78% was measured. When the autonomous system was used, an efficiency of 77% was acquired. The poor efficiency depends on high losses in the MOSFETs during switching, mostly in the upper one. A too large gate restor slowed down the rise and fall time of the transistor and when a smaller one was used the efficiency was increased to 87%. Because of the higher efficiency, it was not possible to use the APF without the autonomous system by the reason that it was hard calculate a reference without reaching the voltage limits of the capacitor.

It could be noticed that when running the switching stage as a boost converter, with a resistive load in parallel with the storage capacitor, the efficiency was 97%. The duty cycle was fixed to 0.48 which gave a voltage over the storage capacitor of 60V. Therefore, no further improvement on the hardware was done and the reason of the lower efficiency of the APF was due to the control system.

Chapter 6

Discussion

In the present APF an average current control method was used both for the boost mode as well as for the buck mode. To control the system with this method, it is necessary to calculate a current reference from the load current so it is not possible that the APF can start working properly until a number of load cycles have been recorded. An alternative control method could be to remove the DC component of the measured current in order to use a zero reference control system. In this case it is not necessary to measure the load current in order to acquire a reference, only the dc-bus current and the voltage over the capacitor needs to be measured and a zero will be used as a reference when the filter is working in buck mode. In boost mode the voltage over the capacitor is ramped up to a specified limit. If this limit is not met before the next load step occurs the slope of the ramp will be increased or vise versa. The problem with this kind of control comes when the voltage at the capacitor reach the limit, the current drawn from the dc-supply will abruptly fall and cause harmonics. In a second solution, it could be possible to use a voltage control method even for the buck mode by measuring the voltage over the PPF over the DC bus and keep it regulated by the use of the APF. This requires that the APF controller is faster than the DC/DC converter controller for the bus. A disadvantage is that an increase in bandwidth of the controller will require a higher switching frequency and that sets a higher demand on the DSP which already is loaded to the limit.

The residual error and overshoot in the step response of the APF in this project could probably be attenuated by improving or using an other type of regulator controller. The state space method used to model the APF which is a hybrid buck/boost converter may not be accurate enough for both types. A sliding mode or even more preferable a fuzzy controller may solve the residual error and make a fast step response without overshot possible. But this requires a far more complex analysis and knowledge of the behaviour of the APF.

The focus in this thesis has been to implement a basic APF to study the current distortion mitigation, but other more advanced topologies have also been discussed. One topology discussed was to use an additional switching leg in addition to the existing one in the APF of this project. With four MOSFETs in the APF it will be possible to work in four quadrant mode. This makes it possible to use a larger voltage range over the capacitor from zero volt up to the specified voltage limit. A lower voltage value could be used and by that a lower rated capacitor voltage. It may also be possible to use lower rated MOSFETs with a smaller chip size in order to get higher efficiency. This topology could possible make the storage capacitor size decrease even further.

Regarding the power efficiency in the APF, it is established that this losses are mostly switching losses and not conduction losses in the MOSFETs. A way to deal with this could be to decrease the switching frequency and in this way lowering the switching losses. But this will come with the expenses of lower filter performance and larger filter components. An other more feasible solution could be to use a more advanced converter topology, for example a resonant converter with either Zero-Voltage-Switching (ZVS) and or Zero-Current-Switching (ZCS). However, more components will be needed to implement this type of converter. Silicon based MOSFETs was used in this project and some improvements of the efficiency could be done by interchanging them with devices made of for example gallium nitride or silicon carbide.

Chapter 7

Conclusions

This master thesis demonstrate a stand alone product for taking care of low frequency distortion. The results of this master thesis show that it is possible to decrease 300Hz distortion by an APF with a digital controller. It has been shown that by combining a passive-filter, an active-filter and a DC/DC converter, it is possible to get an undisturbed power supply on the 56V-side. Accordingly, to Fig 5.6 the current amplitude has been mitigated with 86% and behaves as a uniform current. The current is oscillating between 0.16A and 0.22A. In other words, there is only 0.06A ripple. Another way to study the results is to compare the different RMS currents. The load step has a RMS current of 0.4716A, with the external passive filter it went down to 0.2372A and when the APF is activated it has decreased to 0.1681A, which is close to the load average value 0.15A.

The regulator for the releasing energy mode can be improved, which will decrease the overshoot and the rise time. As a result, the size of the external passive filter will be reduced, which task is to take care of the overshoots and oscillation. It has also been shown that with a digital control it is possible to create an adaptive system. As a result, the load can vary and the DSP will adjust the reference value for that specific load.

The APF has not been integrated with the existing DC/DC converter more then the switching frequency is the same. Therefore, there are some conflicts between the controller in the two devices. But those can be solved by synchronizing the switch frequency of the devices and phase shift one of the devices with 180 degrees. As mention in Chapter 4.4.3 a high switching frequency will give a less amount of operation cycle per PWM period. As a result from this, one function has not been included, which had a small effect on the results, as discuses at Chapter 4.4.3.In short, a more powerful DSP should be used if it is desirable to work at 500kHz, which is eligible for integration with the existing DC/DC converter.

The state space representation used for modelling the APF circuit, which proved to be a useful tool and gives acceptable results. The APF models are used for creating regulators, but for the Buck-Mode there have been some difficulties. The error observed during the laboratory run up and the control parameter had to be modified manually. The outcome was sufficient after the modification and the efficiency of the APF was measured to 89%.

7.1 Future work

The next step in the area of current mitigation in a power supply, would be to create a new digital control system that regulates the existing APF and the DC/DC converter. Different methods of controller should be simulated and compared, one method could be a fuzzy controller. The efficiency of the APF should be better then 95%.

One future goal could also be to build a DSP card with desired modules. This will give the possibility of using the fastest and the newest DSP in the market.

But in the end the main goal would be to have a none detectable current ripple on the 56V bus, if the devices are not the limiting factor. If there is a current ripple, it should have larger frequency then 100kHz, so it will be easy to manage with a external passive filter. But the passive filter should be much smaller then the one that is used in this thesis.

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Appendix A

Digital Control

A.1 Program code in C

```
//###########################################################################
//
// FILE: converterControl.c
//
// TITLE: Active Power Filter Control Program
//
// DESCRIPTION: Boost/Buck average current controller with automatic
//     reference setting
//
// Author: Daniel Glenting, Daniel Samuel
//
//###########################################################################
// $Release Date: June 25, 2013 $
//###########################################################################

#include "DSP28x_Project.h"
#include "stdbool.h"

//Declaration of ePWM pointer:
typedef struct
{
    volatile struct EPWM_REGS *EPwmRegHandle;
}EPWM_INFO;

//Constants and References:
#define EPWM1_TIMER_TBPRD   300   //Time Period for ePWM1 (300 for 500kHz)
#define I_LOAD_THREASHOLD  0.35
#define DEAD_BAND_LOWER_MOS  0x6   //Dead Band time delay (0x6 = 50ns)
#define DEAD_BAND_UPPER_MOS  0x3   //Dead Band time delay (0x3 = 50ns)
#define DUTY_MAX    0.99  //Max boundary for Duty limiter
#define DUTY_MIN    0.0001  //Min boundary for Duty limiter
//#define REF_BUCK    -0.06  //Initial iRef value
//#define REF_BOOST    0.2   //Initial iRef value
#define REF_BUCK    0.15  //Initial iRef value
#define REF_BOOST    0.15  //Initial iRef value
#define V_CAP_MAX    80.0  //Maximum allowed capacitor voltage
#define V_CAP_HI_BOUND_1  70   //Upper boundary level of capacitor 1
#define V_CAP_HI_BOUND_2  68   //Upper boundary level of capacitor 2
#define V_CAP_LO_BOUND_1  32.5  //Lower boundary level of capacitor 1
#define V_CAP_LO_BOUND_2  32   //Lower boundary level of capacitor 2
#define AVERAGE_CALC_PERIOD  50000

//Correction factors for AD converter:
#define I_IN_CORRECTION_FACTOR  0.00037985
#define I_LOAD_CORRECTION_FACTOR 0.00073764
#define V_CAP_CORRECTION_FACTOR  0.02928
#define V_BUS_CORRECTION_FACTOR  0.01897
```

```
//ADC setting parameters:
#define ADC_MODCLK 0x3
#define ADC_CKPS 0x1
#define ADC_SHCLK 0x1

//Control Parameters Boost (2013−06−05):
#define B2_BOOST (−0.1656)
#define B1_BOOST 0.0077
#define B0_BOOST 0.1733
#define A2_BOOST 0.1298
#define A1_BOOST 0.8702
#define GAIN_BOOST 1.0

//Control Parameters Buck (2013−06−05):
#define B2_BUCK  (−0.339)
#define B1_BUCK  0.038
#define B0_BUCK  0.35
#define A2_BUCK  0.79
#define A1_BUCK  0.223
#define GAIN_BUCK 0.44

//Declaration of functions:
void initEPwm1(void);   //Initialization function for ePWM1 module
void initAdcSeq1(void);   //Initialization function for ADCSeq1 module
void initPeriGpio(void);  //Initialization function for peripheral GPIO−pins
interrupt void epwm1Isr(void); //Interrupt function for interrupt on ePWM1 module

EPWM_INFO epwm1_info;   //Handle for ePWM1 module

//Declaration of variables:

//Flag variables:
Uint16 upAndRunning = false;
Uint16 start = false;
Uint16 stop = false;
Uint16 voltageFault = false;
Uint16 currentFault = false;
Uint16 buckMode = false;
Uint16 boostMode = false;
Uint16 voltageAdjustEnable = false;
Uint16 averageCalcEnable = false;

//Counters:
Uint16 intPwmCount = 0;
Uint16 averageCalcCount = 0;

//Measurement variables:
float vBus = 0.0;
float vC = 0.0;
float iIn = 0.0;
float iLoad = 0.0;

//Control variables:
float duty = DUTY_MIN;
float dutyN_1 = DUTY_MIN;
float dutyN_2 = DUTY_MIN;
float error = 0.0;
float errorN_1 = 0.0;
float errorN_2 = 0.0;
float iRefBoost = REF_BOOST;
float iRefBuck = REF_BUCK;
float iLoadSum = 0.0, iLoadAvg = 0.0;
float iLoadSumFinal = 0.0;
float iDeltaRef = 0.0;
Uint16 intPwmCountFinal = 0;

float b2Buck = B2_BUCK;
float b1Buck = B1_BUCK;
```

```
float b0Buck = B0_BUCK;
float a2Buck = A2_BUCK;
float a1Buck = A1_BUCK;
float gainBuck = GAIN_BUCK;

float b2Boost = B2_BOOST;
float b1Boost = B1_BOOST;
float b0Boost = B0_BOOST;
float a2Boost = A2_BOOST;
float a1Boost = A1_BOOST;
float gainBoost = GAIN_BOOST;


//Main function:
void main(void)
{

        InitSysCtrl();      //Initialize System Control

        EALLOW;
        SysCtrlRegs.HISPCP.all = ADC_MODCLK; // HSPCLK = SYSCLKOUT/ADC_MODCLK
        EDIS;

        InitEPwm1Gpio();     //Initialization of ePWM1 module
        initPeriGpio();      //Initialization of peripheral GPIO-pins

        DINT;       //Disable Global Interrupt

    InitPieCtrl();      //Initialize Pie Control System Registers

    IER = 0x0000;       //Interrupt Enable Register
    IFR = 0x0000;       //Interrupt Flag Register


        InitPieVectTable();     //Initialize Pie Vector Table

        EALLOW;
        PieVectTable.EPWM1_INT = &epwm1Isr;  //Initiate epwm1Isr interrupt routine (load the address of interrupt routine
            epwm1Isr to the PIE table)
        SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
        EDIS;

        initEPwm1();      //Initialize ePWM1 module with user defined settings

        EALLOW;
        SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
        EDIS;

        IER |= M_INT3;

        PieCtrlRegs.PIEIER3.bit.INTx1 = 1;

        InitAdc();       //Init the ADC

        EINT;       //Enable Global interrupt
        ERTM;       //Enable Global realtime interrupt

        initAdcSeq1();      //Initialization of ADCSeq1 module

        //Infinite loop:
        for (;;) {

                //Start control system and PWM:
                if (start) {
                        start = false;
                        currentFault = false;
                        voltageFault = false;
                        upAndRunning = true;
```

```
                EPwm1Regs.DBCTL.bit.POLSEL = 0x2;
                EPwm1Regs.AQCSFRC.bit.CSFA = 0;   // 0 = Set channel A to normal (Lower MOSFET) Low
                EPwm1Regs.AQCSFRC.bit.CSFB = 0;   // 0 = Set channel B to normal (Upper MOSFET) Low
                GpioDataRegs.GPASET.bit.GPIO4 = 1;  // SS−Switch off
        }

        //Stop control system and PWM:
        if (stop) {
                stop = false;
                upAndRunning = false;
                EPwm1Regs.DBCTL.bit.POLSEL = 0x0;
                EPwm1Regs.AQCSFRC.bit.CSFA = 1;   // 1 = Force channel A (Lower MOSFET) Low
                EPwm1Regs.AQCSFRC.bit.CSFB = 1;   // 1 = Force channel B (Upper MOSFET) Low
                GpioDataRegs.GPACLEAR.bit.GPIO4 = 1; // SS−Switch on
        }

        //Calculate average load current:
        if (averageCalcCount >= AVERAGE_CALC_PERIOD) {
                averageCalcCount = 0;
                GpioDataRegs.GPBTOGGLE.bit.GPIO34 = 1;
                iLoadAvg = iLoadSumFinal / intPwmCountFinal;

                if (averageCalcEnable == true && (iLoadAvg >= 0.01 || iLoadAvg <= 0.2) && upAndRunning == true)
                        {
                          iRefBoost = iLoadAvg;
                          iRefBuck = iLoadAvg;
                }
                else {
                          iRefBoost = REF_BOOST;
                          iRefBuck = REF_BUCK;
                }
        }

        ++averageCalcCount;

    } //infinite loop

} //main()

//PWM interrupt function:
interrupt void epwm1Isr(void)
{

    ++intPwmCount;      //Count number of PWM cycles for average calculation

    //Old values are saved
    errorN_2 = errorN_1;
    errorN_1 = error;
    dutyN_2 = dutyN_1;
    dutyN_1 = duty;

    if (vC > V_CAP_MAX) {
            EPwm1Regs.DBCTL.bit.POLSEL = 0x0;
            EPwm1Regs.AQCSFRC.bit.CSFA = 1;   // Force channel A Low
            GpioDataRegs.GPACLEAR.bit.GPIO4 = 1;  // SS−Switch on
            upAndRunning = false;
            voltageFault = true;
    }

    iIn = AdcMirror.ADCRESULT0 * I_IN_CORRECTION_FACTOR;
    iLoad = AdcMirror.ADCRESULT1 * I_LOAD_CORRECTION_FACTOR;
    vC = AdcMirror.ADCRESULT2 * V_CAP_CORRECTION_FACTOR;
    vBus = AdcMirror.ADCRESULT3 * V_BUS_CORRECTION_FACTOR;

    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;

    iLoadSum += iLoad;
```

```
//Control modes:
if (iLoad >= I_LOAD_THREASHOLD) { //Buck mode
        if (buckMode == false) {
                buckMode = true;
                boostMode = false;

                if (voltageAdjustEnable == true) {
                        if (vC >= V_CAP_HI_BOUND_1) {
                                iDeltaRef -= 0.005;
                        }
                        else if (vC >= V_CAP_HI_BOUND_2){
                                iDeltaRef -= 0.01;
                        }
                }
                else {
                        iDeltaRef = 0.0;
                }
        }

        //Differential equation Buck:
        error = iRefBuck - iIn + iDeltaRef;
        duty = a1Buck*dutyN_1 + a2Buck*dutyN_2 + (b0Buck*error + b1Buck*errorN_1 + b2Buck*errorN_2)* gainBuck
                ;
}
else {    //Boost mode
        if (boostMode == false) {
                buckMode = false;
                boostMode = true;
                iLoadSumFinal = iLoadSum;
                intPwmCountFinal = intPwmCount;
                iLoadSum = 0.0;
                intPwmCount = 0;

                if (voltageAdjustEnable == true) {
                        if (vC <= V_CAP_LO_BOUND_1) {
                                iDeltaRef += 0.005;
                        }
                        else if (vC <= V_CAP_LO_BOUND_2) {
                                iDeltaRef += 0.01;
                        }
                }
                else {
                        iDeltaRef = 0.0;
                }
        }

        //Differential equation Buck:
        error = iRefBoost - iIn + iDeltaRef;
        duty = a1Boost*dutyN_1 + a2Boost*dutyN_2 + (b0Boost*errorN_1 + b1Boost*errorN_1 + b2Boost*errorN_2) *
                gainBoost;
        boostMode = true;
        buckMode = false;

}

//Check if duty reaches bounds
if (duty >= DUTY_MAX) {
        duty = DUTY_MAX;
}
else if (duty <= DUTY_MIN) {
        duty = DUTY_MIN;
}


epwm1_info.EPwmRegHandle->CMPA.half.CMPA = duty * EPWM1_TIMER_TBPRD;

//Clear INT flag and SOCA flag
```

```
        EPwm1Regs.ETCLR.bit.INT = 0x1;
        EPwm1Regs.ETCLR.bit.SOCA = 0x1;

        //Acknowledge this interrupt to receive more interrupts from group 3
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;

        GpioDataRegs.GPCTOGGLE.bit.GPIO84 = 1;

} //epwm1Isr()

//Initialisation of GPIO (LED1, LED2, Soft Start−switch etc.):
void initPeriGpio(void)
{
        EALLOW;
        GpioCtrlRegs.GPAMUX2.bit.GPIO31 = 0;  //Led1
        GpioCtrlRegs.GPADIR.bit.GPIO31 = 1;  //Set as output
        GpioDataRegs.GPASET.bit.GPIO31 = 1;  //SET = LED1 off

        GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0;  //Led2
        GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1; //Set as output
        GpioDataRegs.GPBSET.bit.GPIO34 = 1;  //SET = LED2 off

        GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 0;  //Soft Start−switch
        GpioCtrlRegs.GPADIR.bit.GPIO4 = 1; //Set as output
        GpioDataRegs.GPACLEAR.bit.GPIO4 = 1; //CLEAR = off (50 Ohm resistor enabled)

        GpioCtrlRegs.GPCMUX2.bit.GPIO84 = 0; //For time measurement purpose
        GpioCtrlRegs.GPCDIR.bit.GPIO84 = 1;  //Set as output
        GpioDataRegs.GPCCLEAR.bit.GPIO84 = 1; //Set low
        EDIS;

} //initPeriGpio()

//Initialisation of ePwm module 1
void initEPwm1()
{
        //Setup TBCLK:
        EPwm1Regs.TBPRD = EPWM1_TIMER_TBPRD;   // Time Base Period
        EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;  //
        EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;   //
        EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;   // Count up mode of sawtooth wave
        EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;   // Disable phase loading
        EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;  //
        EPwm1Regs.TBCTR = 0x0000;   // Clear Time Base counter

        EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_IMMEDIATE; //Load CMPA immediately

        //Set Actions Qualifiers:
        EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;  // Set PWM1A on Zero
        EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;  // Clear PWM1A on event A, up count
        EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;  // Set PWM1B on Zero
        EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;  // Clear PWM1B on event B, up count
        EPwm1Regs.AQSFRC.bit.RLDCSF = 0x3;    //
        EPwm1Regs.AQCSFRC.bit.CSFA = 1;    //Force A low
        EPwm1Regs.AQCSFRC.bit.CSFB = 1;    //Force B low

        //Dead−Band Generation:
        EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
        EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
        EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
        EPwm1Regs.DBRED = DEAD_BAND_LOWER_MOS;
        EPwm1Regs.DBFED = DEAD_BAND_UPPER_MOS;

        //ADC SOC on CMPA hit event:
        EPwm1Regs.ETSEL.bit.SOCASEL = ET_CTRU_CMPA; // Select SOC from from CPMA on upcount
        EPwm1Regs.ETSEL.bit.SOCAEN = 1;    // Enable SOC on A group
        EPwm1Regs.ETPS.bit.SOCAPRD = ET_1ST;  // Generate pulse on 1st event
```

```
        //Interrupt to update CMPA under next period:
        EPwm1Regs.ETSEL.bit.INTSEL = ET_CTRU_CMPA;  // Select INT on CMPA event
        EPwm1Regs.ETSEL.bit.INTEN = 1;  // Enable INT
        EPwm1Regs.ETPS.bit.INTPRD = ET_1ST;  // Generate INT on 1st event

        epwm1_info.EPwmRegHandle = &EPwm1Regs;  // Set the pointer to the ePWM module

} //initEPwm1()


//Initialisation of AD module:
void initAdcSeq1(void)
{
        //initialisation of AD converter
        AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;   // Set sample window size to min
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 0x1;   // Reset the Seq1 to start from CONV00
        AdcRegs.ADCTRL2.bit.INT_MOD_SEQ1 = 0x0;   //
        AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 0x1;  //
        AdcRegs.ADCMAXCONV.all = 0x3;     // Setup 4 conv's on SEQ1
        AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;  //
        AdcRegs.ADCTRL3.bit.SMODE_SEL = 0x1;   //
        AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0;    // Setup conv from ADCINA0 &amp;amp; ADCINB0
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1;    // Setup conv from ADCINA1 &amp;amp; ADCINB1

} //initAdcSeq1()
```

Appendix B

PCB

B.1 PCB with components

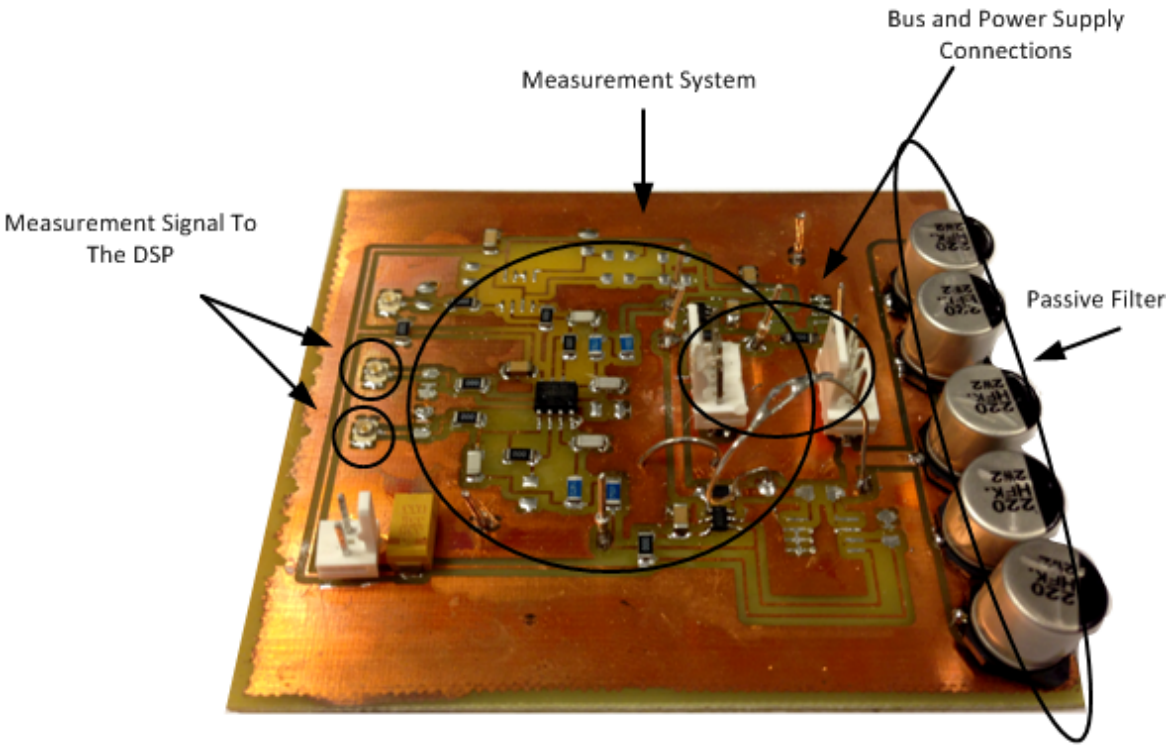

Fig. B.1 Measurement card, which was design in the software Eagle and made at Chalmers University.

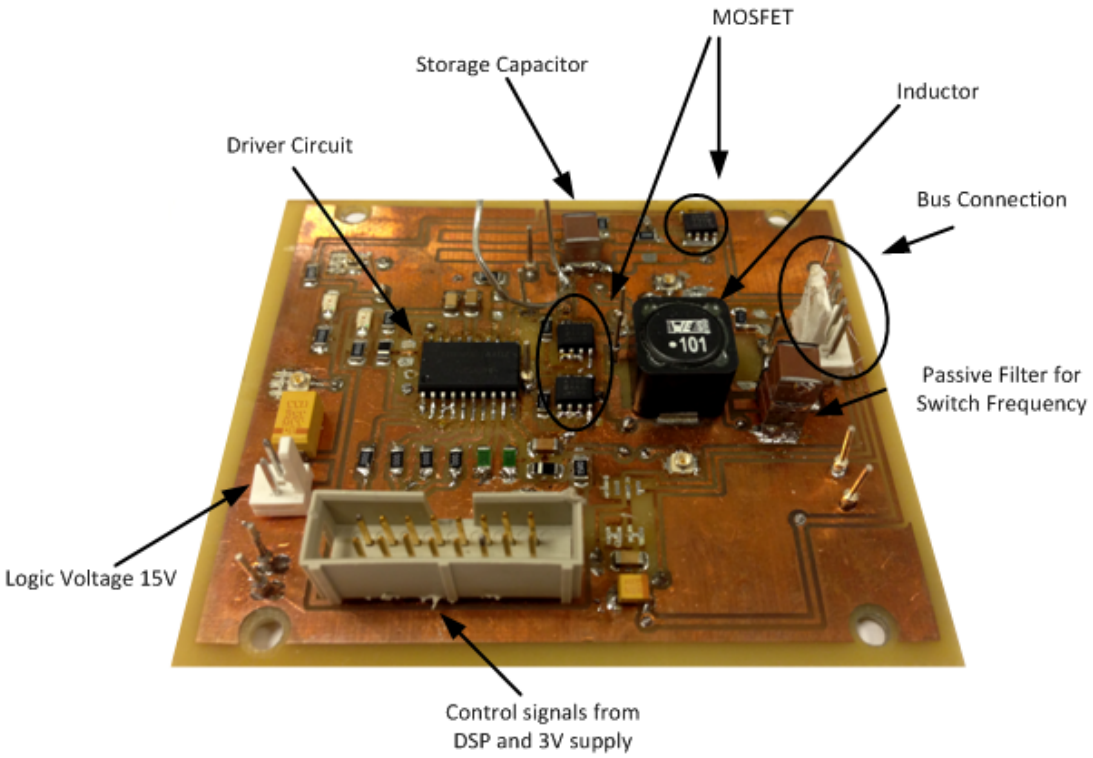

Fig. B.2 APF card, which was design in the software Eagle and made at Chalmers University.

B.2 Schematic Drawing

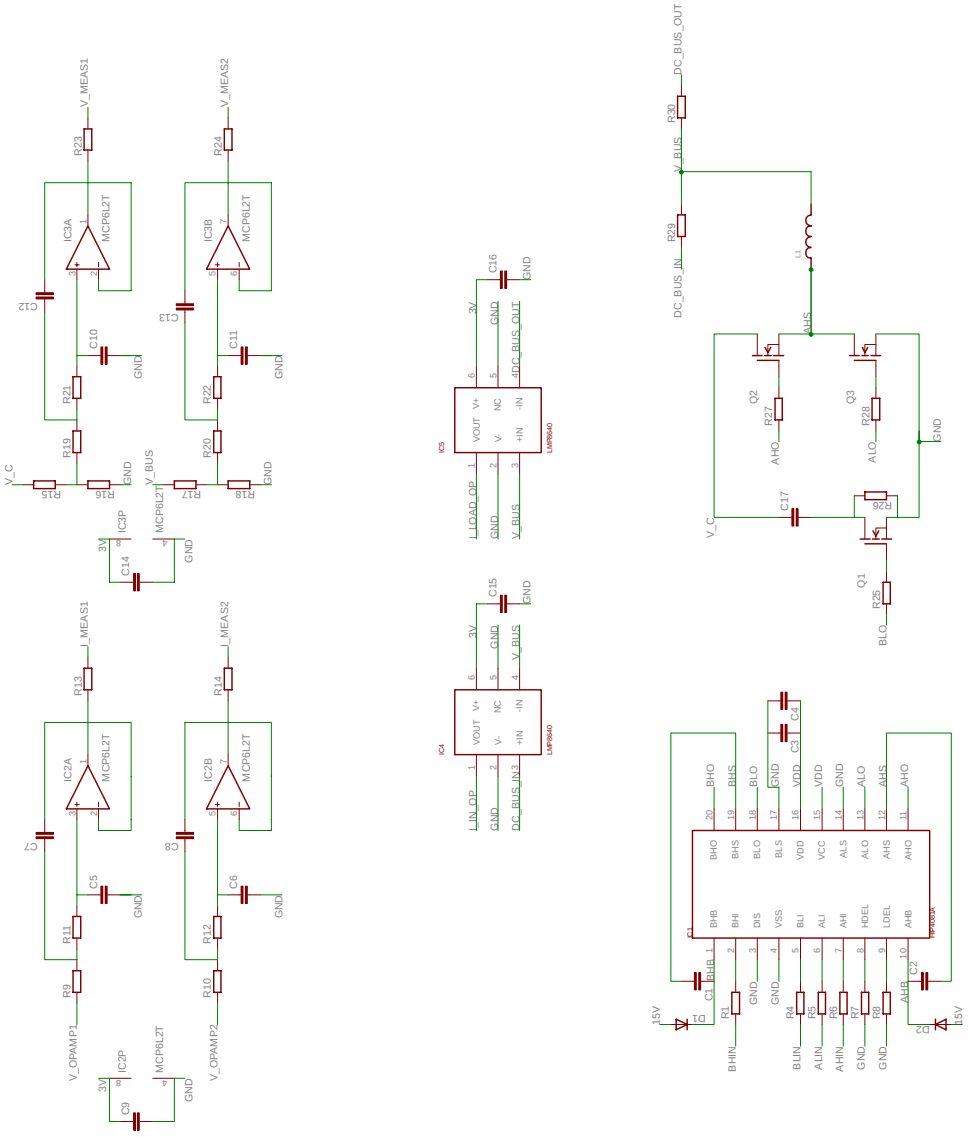

Fig. B.3 Schematic drawing over the APF, with switching stage and measurement system.

Appendix C

Simulation

C.1 Simulink

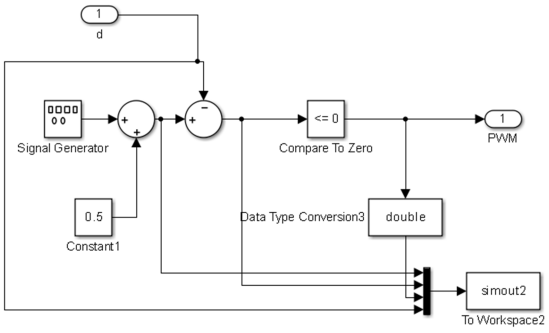

Fig. C.1 PWM.

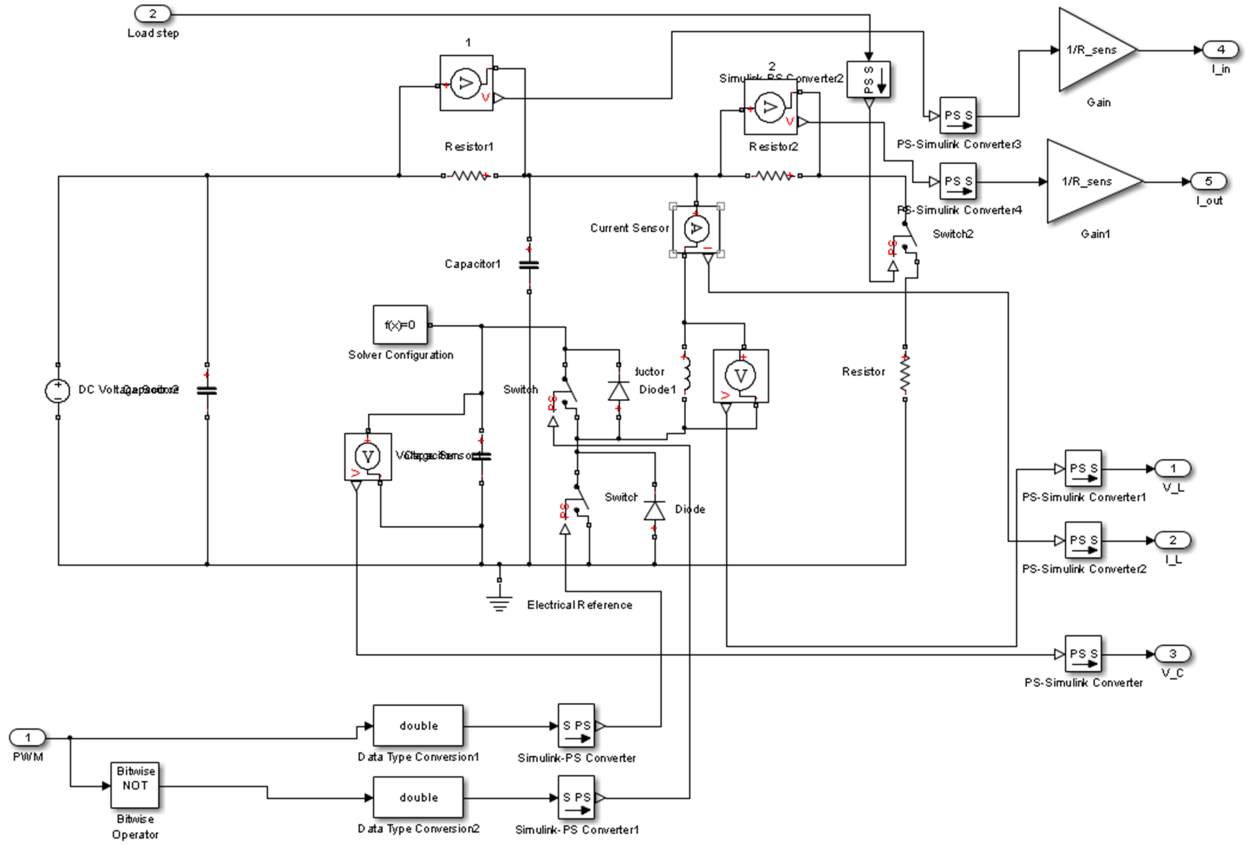

Fig. C.2 APF model in Simulink.

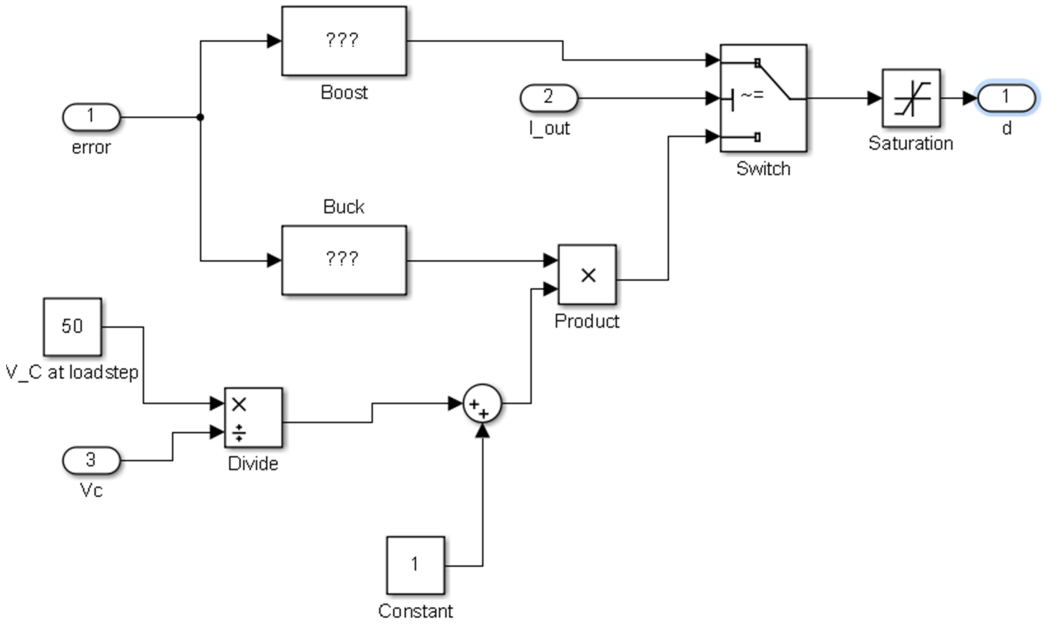

Fig. C.3 Controller block in Simulink.

C.1.1 Simulink parameter

```
Ts = 2e-6; %Sampling time
R_load = 21.3;
R_sens = 0.1/5;
iIn = 0.2; %Referens
iLoad=1.5;

%Konverterparametrar
Rcin = 8e-3; %Storage capacitor resistance
Rcut=1000e-3; % passive filter resistance
RL = 0.1; %inductor resistor
Ron = 51e-3; %MOSFET Ron
Cin = 22e-6; %Storage capacitor
Cut = 44e-6; %passive filter for taking care of SW freq
L = 100e-6;
R = (Rcin+RL+Ron);
Vbus=32;
Vc_start=32;
d_upper_limit = 0.99; %Duty cycle Upper limit
d_lower_limit = 0.0001; %Duty cycle Lower limit

%%
% Boost:
il0 = 0;
Vc0 = 40;

D = 1-32/Vc0;
num_Boost = [(Rcin*il0+Vc0)/L il0*(1-D)/(L*Cin)];
dnum_Boost = [1 (R-Rcin*D)/L (1-D)^2/(L*Cin)];
G_Boost = tf(num_Boost, dnum_Boost);
 sisotool(G_Boost,1,1,1)


%%
%Buck:
il0=0.15;
Vc0 = 55;
d=32/Vc0;

num_Buck = [Vc0/L Vbus*Vc0/(Cut*L*Vc0*(Rcut+R_load))+Vc0*(1-Vbus/Vc0)/(Cut*L*(Rcut+R_load))];
dnum_Buck=[1 (Ron/L+Rcut*R_load/((Rcut+R_load)*L)+1/(Cut*(Rcut+R_load))+RL/L) (RL+R_load+Ron)/(Cut*L*(Rcut+R_load)
        )];

G_Buck = tf(num_Buck, dnum_Buck);
 sisotool(G_Buck,1,1,1)


 %%

%Diskretisering
discopts = c2dOptions('Method','tustin','PrewarpFrequency',100);
buckD = c2d(buck,Ts,discopts);
boostD = c2d(boost,Ts,discopts);
[bucknum,buckdnum] = tfdata(buckD, 'v')
[boostnum,boostdnum] = tfdata(boostD,'v')
```