CHALMERS

Transmission Line based Envelope Amplifier for Envelope Tracking in PA Systems

Study based on an inverse class F GaN PA

Master of Science Thesis

JONATAN ERIKSSON
FREDRIK PERSSON

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2013

Transmission Line based Envelope Amplifier for Envelope Tracking in PA Systems

Study based on an inverse class F GaN PA

JONATAN ERIKSSON
FREDRIK PERSSON

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2013

Transmission Line based Envelope Amplifier for Envelope Tracking in PA Systems
Study based on an inverse class F GaN PA
JONATAN ERIKSSON
FREDRIK PERSSON

Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology
SE–412 96 Göteborg
Sweden
Telephone +46 (0)31–772 1000

Chalmers Bibliotek, Reproservice
Göteborg, Sweden 2013

Transmission Line based Envelope Amplifier for Envelope Tracking in PA Systems
Study based on an inverse class F GaN PA
JONATAN ERIKSSON
FREDRIK PERSSON
Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology

Abstract

The aim of this thesis was to investigate the possibility of using a transmission line (TL) based converter as an envelope amplifier (EA) for envelope tracking in a radio frequency power amplifier (RF PA) system. A TL based EA can supply fast voltage modulation but requires impedance match between the characteristic impedance of the TL, and the PA's supply terminal impedance (STI). Hence, a first step in this thesis was to investigate the characteristics of the PA's STI. A second step was to construct a prototype of an EA, using a lumped transmission line as energy accumulator. The EA was then tested together with the PA in order to draw further conclusions whether a TL based EA is suitable for ET of PA systems.

The result from the PA characterization provided two descriptions of the STI. However, the EA prototype was designed after the STI description that seemed to enable a beneficial ET operation. Despite the PA characterization it was, and still is, a bit unclear what features of the STI a pulsed supply voltage would excite during an EA to PA integration. However, the result from the integration indicated a non beneficial STI behavior. The conclusion from this report is that the studied inverse class F GaN PA does not seem to be suitable for ET with a TL based EA.

Index Terms: envelope amplifier, envelope tracking, inverse class F GaN HEMT PA, lumped transmission line, transmission line

Acknowledgements

First and foremost we would like to thank our tutors Christian Fager and Sverker Sander, both of which has spent a lot of time and effort helping us during our thesis work. We would like to thank Torbjörn Thiringer for feedback and guidance of the report. We would also like to thank Andreas Karvonen for checking up on us from time to time. We would like to thank Faraz Mahmood whom has frequently helped us borrowing equipment. Lastly, we want to thank the Board Power Unit and the Radio Design Center at Ericsson Lindholmen, as well as the Department of Microtechnology and Nanosicence at Chalmers, for supplying us with all the resources that was used during the thesis work. This work has been carried out partly at Ericsson AB and partly at the Department of Microtechnology and nanoscience at Chalmers University of Technology. The financial support is given by Ericsson AB.

Fredrik Persson
Jonatan Eriksson
Göteborg, Sweden, 2013

Abbreviations

DSM	dynamic supply modulation
EA	envelope amplifier
EER	envelope elimination and restoration
ET	envelope tracking
GaN HEMT	gallium nitride high electron mobility transistor
LTL	lumped transmission line
PAE	power added efficiency
PCB	printed circuit board
RF PA	radio frequency power amplifier
ST	supply terminal
STI	supply terminal impedance
TL	transmission line

Contents

Chapter 1

Introduction

During 2009-2011 there have been some projects at Ericsson AB, related to the use of transmission lines (TL) in power electronic converters. One hallmark of this topology in EA applications is that the slew rate of the converter output voltage is only determined by the switch turn on time. This is not the case in an inductor based converter, since the inductor holds energy for a number of previous switch cycles.

At the same time there is a major ongoing work on decreasing the energy consumption of power amplifiers (PA) in radio base stations, driven by economical and environmentally purposes. Therefore Ericsson is also involved in a cross-disciplinary project together with Chalmers University of Technology, as well as other companies. In this project new high efficiency power amplifier architectures are investigated. One technique for efficiency enhancement is envelope tracking (ET). In ET an envelope amplifier (EA), which is a switched power converter, is connected to the supply terminal (ST) of the PA. The EA modulates the supply voltage of the PA according to the input power variations. Due to this the PA is always operated at near max power added efficiency (PAE). However this put demands on a fast modulated supply.

This master thesis is devoted to investigate the possibilities of using a TL based EA for ET in radio frequency power amplifiers (RF PA). A TL based converter seems beneficial for ET due to a fast and energy efficient modulation of the PA system.

1.1 Problem background & Previous work

Today there exist many different architectures among envelope amplifiers. The common principle is however to use a converter with an inductance as energy storage device. Moreover, in order to obtain fast output voltage modulation, a linear amplifier is often added in series or in parallel [5]. An EA with a linear amplifier in series is illustrated in Figure 1.1.

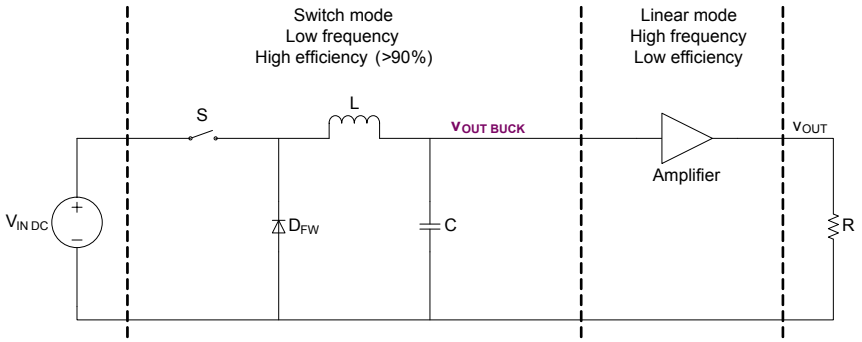

Fig. 1.1 Conventional EA with inductor and linear amplifier.

The drawbacks of this conceptual solution is that there will be a minimum value of the slew rate, t_{rise}, and that there will be a steady state ripple, V_{pkpk}, in the buck converter output voltage, see Figure 1.2.

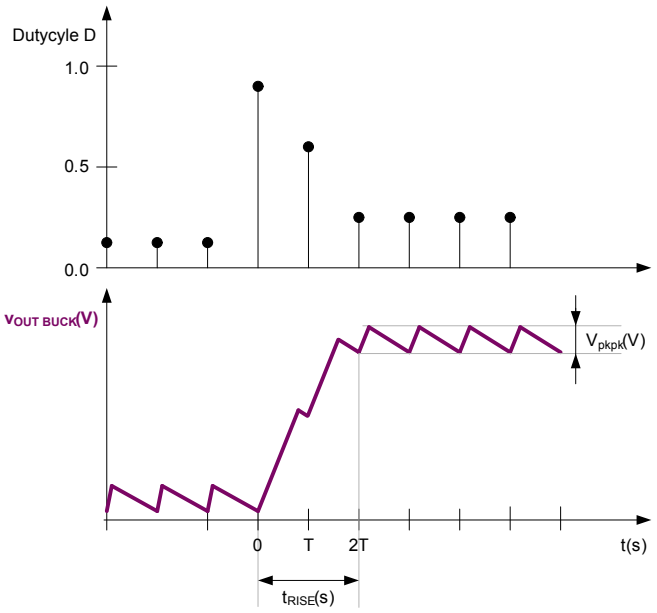

Fig. 1.2 Typical output voltage curve from the EA shown in Figure 1.1.

Moreover, due to the added linear amplifier in Figure 1.1 the overall efficiency of the EA is reduced. According to [5], current ways to improve the performance of the EA is to let it consist of a converter which is based on a multi-input, multi-phase or multi-level architecture. Ericsson AB has investigated different TL based converter configurations, based on the derivations in [13]. It has been shown that different features are obtained depending on how fast the switches is modulated in comparison to the propagation delay of the TL. Example of such features is the possibility to share switches in case of multiple output voltages, which requires less semiconductors than conventional converters do. Other features are inverting and noninverting polarity capabilities, and the possibility to form simple and highly efficient pulsed radio transmitters, [13].

Figure 1.3 depicts an ideal version of the prototype converter which have been used as an EA in this thesis.

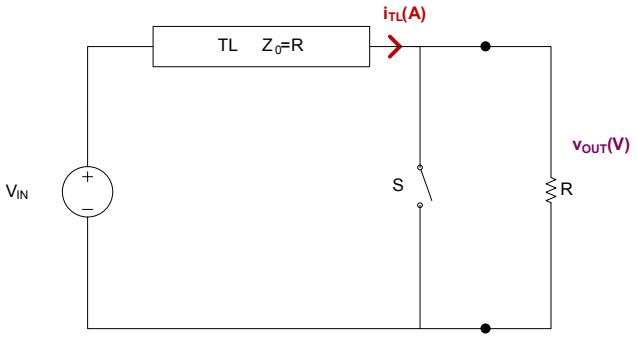

Fig. 1.3 Ideal circuit model of the EA which have been used during the thesis project.

In Figure 1.3 Z_0 is the characteristic impedance of the EA, while R is an arbitrary resistive load. Note in the example in Figure 1.3 that $Z_0 = R$. In the thesis R is supposed to be replaced with the supply terminal of the PA. To avoid reflections, and thereby enable a reasonable easily voltage control, a design goal is therefore to achieve load match between the characteristic impedance of the EA and the STI of the PA. Moreover, note that the EA in Figure 1.3 is of single phase type. Hence the output voltage takes the form of separate pulses.

In Figure 1.4 the principal output voltage and TL current wave forms of the EA presented in Figure 1.3 are visualized with solid curves. The dashed curve represents the current if the TL in Figure 1.3 was replaced with an inductor.

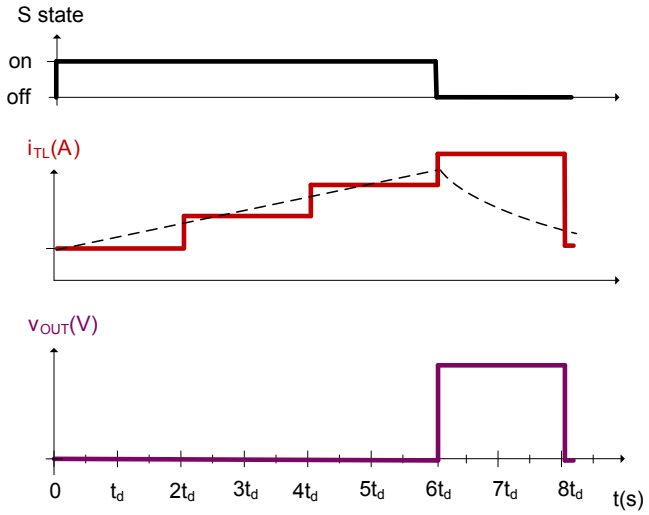

Fig. 1.4 Principal wave forms of the TL based EA (solid curves) compared to its inductor based counterpart (dashed curve).

Note in Figure 1.4 at $t = 6t_d$ how the slew rate is improved in the TL based converter compared to v_{out} in Figure 1.2. If the operation of a multi phase, TL based EA could be verified it would be possible to obtain a continuous output voltage. The output voltage would then also ideally be ripple free. From an ET perspective this would give the TL based EA a further advantage compared to its inductor based counterpart: the problem of spurious in RF systems would be reduced or eliminated. Spurious will otherwise occur when a ripply supply voltage interfere with the RF signal and distorts the sending information, [2].

1.2 Purpose & Objectives

To investigate, and thereby acquire knowledge, in the principle of using a TL based EA in ET of PA systems. This involves a characterization of the PA in terms of its supply terminal impedance (STI). Based on the characterization outcome, what are the limitations and possibilities for a TL based EA when it comes to ET? Further on it should be investigated if it is possible to find a suitable characteristic impedance of the EA, Z_0, that matches the STI of the PA. Based on Z_0 an EA should be designed and constructed. The EA should be integrated with the PA. The purpose of the integration is to reveal if the results in the previous steps can be verified, and/or if further conclusions can be drawn.

1.3 Outline

Chapter 2 contains a more detailed explanation of the operation of the TL based EA that will be implemented in this thesis. Chapter 2 is important, since it contains theory which constitutes a prerequisite for the content in the following Chapters. As mentioned in Section 1.1 the design goal is to achieve impedance match between Z_0 of the EA and the STI of the PA. Therefore, in Chapter 3, the PA will be characterized through different measurements to reveal the features of the STI. Based on the results from the PA characterization, Chapter 4 describes how the EA has been reconfigured and designed. In Chapter 5 the verification of the EA performance is described. Chapter 6 contains the results from the integration of the EA and the PA. The results from the integration combined with the previous results are then used to form the conclusions in the end of the report. Note that all theory, and all description of measurement setups are distributed to each corresponding Chapter. All Chapters are ended with its own relevant analysis and the end of the report contains a closing analysis part.

Chapter 2

Transmission Line based Envelope Amplifier

This Chapter is intended to give a basic understanding of the principle function of TL based EAs in general and, in particular, the EA used in this thesis. In the end of the Chapter some basic TL theory are summarized. However, the theory is extended to include lumped transmission lines (LTL), since this is what is implemented in this thesis.

2.1 Operation characteristics of TL based EA

Figure 2.1 depicts and ideal version of the EA to be used in this thesis project together with a load R.

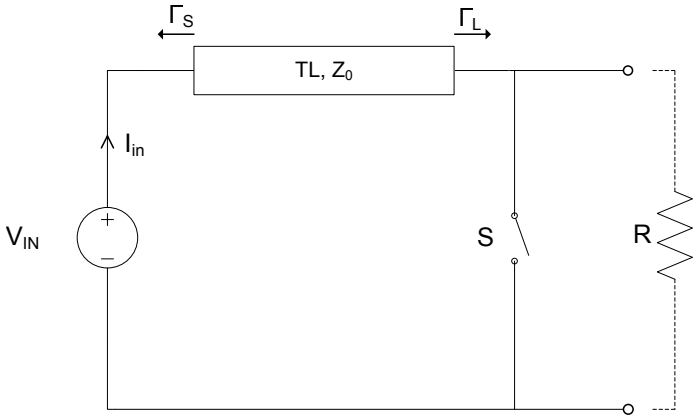

Fig. 2.1 Ideal circuit model of the EA to be used.

In Figure Γ_L is the reflection coefficient seen towards the load, and Γ_S is the reflection coefficient seen towards the source. The reflection coefficients are defined as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.1}$$

and

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.2}$$

where Z_L is the load impedance and Z_S is the source impedance. Further on, note that the reflection coefficient for current is the voltage reflection coefficient with opposite sign, [3].

Figure 2.2 visualises the different operational states of the EA.

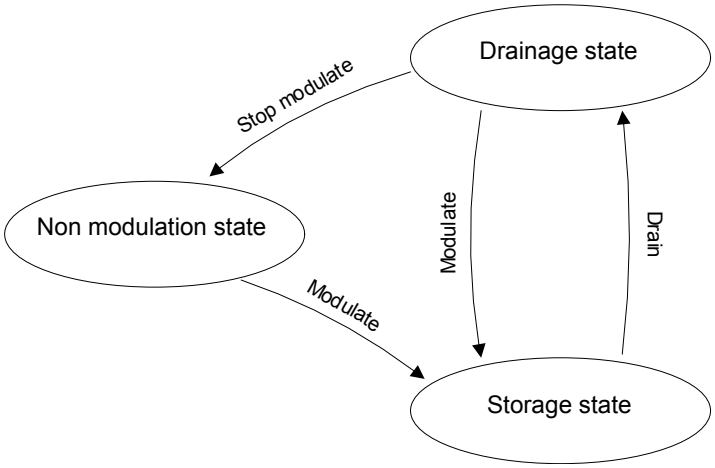

Fig. 2.2 Operational states of the EA.

Consider Figures 2.1 and 2.2 and let $R = Z_L = Z_0$. In the non modulation state the switch, S, is turned off. This implies that $V_{out} = V_{in}$ and $I_{out} = \frac{V_{in}}{R}$, where V_{out} and I_{out} are the voltage and current at the load. By turning on the switch the modulation is initiated and the EA is operating in its storage state. In general the EA can be operated in the storage state for an arbitrary time duration. However, in this thesis, the EA is always operated in the storage state for a multiple $2t_d$ duration. When the switch is turned off the modulation is aborted and the EA is operated in its drainage state. The TL will always be fully drained after a $2t_d$ duration in the drainage state, assuming $R = Z_0$. After a complete drainage period the EA will immediately return to its non modulating state, unless the switch is turned on. More details of the TL current, TL voltage and output voltage and current are described, by a modulation example, in Figures 2.3 and 2.4, with corresponding analysis.

Figure 2.3 and Figure 2.4 show how the voltage and current is distributed on the TL for a particular modulation cycle with a storage time of $2t_d$ and a drainage time of $2t_d$. The TL is drained to a matched load, R.

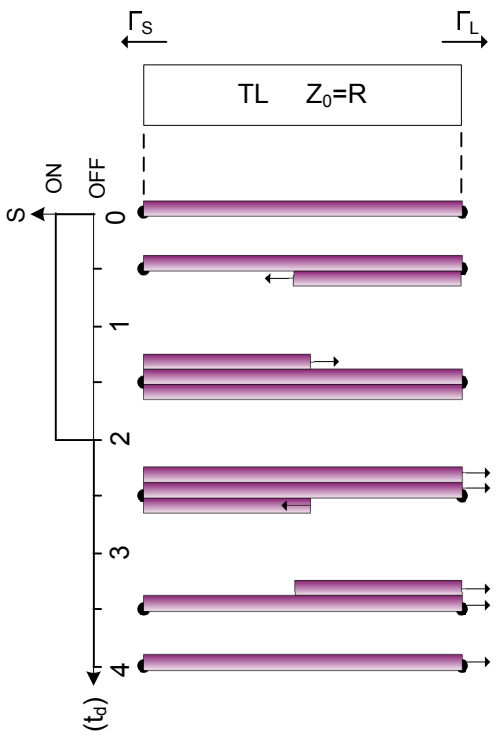

Fig. 2.3 Voltage distribution along the TL.

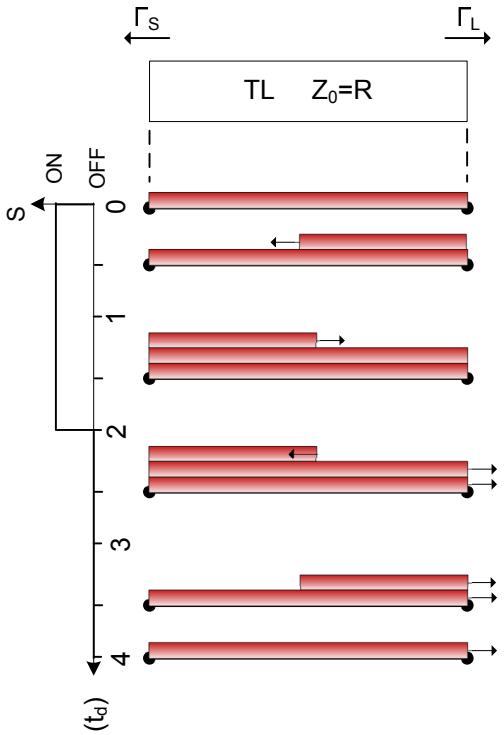

Fig. 2.4 Current distribution along the TL.

Consider Figure 2.3 and Figure 2.4. At $t < 0$ the entire TL is initially charged with $V = V_{in}$ and

$I_{in} = \frac{V_{in}}{Z_0}$. At $t = 0$ the switch is turned on which implies $\Gamma_L = -1$. This means that the voltage wave and current wave traveling towards the generator are $V_{in} \cdot \Gamma_L = -V_{in}$ and $\frac{V_{in}}{Z_0} \cdot (-\Gamma_L) = \frac{V_{in}}{Z_0}$, respectively. At time $t = 1.5t_d$ the voltage wave and current wave have been reflected with $\Gamma_S = -1$ and $-\Gamma_S = 1$ respectively. At time $t = 2t_d$ the switch is turned off implying that $\Gamma_L = 0$. Then the waves traveling towards Γ_L is no longer maintaining the waves traveling towards Γ_S. Hence, at time $t = 2.5t_d$ it is visible that the waves for both voltage and current traveling towards Γ_S are drained. At time $t = 3.5t_d$ the TL is draining the last of its stored energy and at time $t = 4t_d$, after $2t_d$ seconds of drainage, the TL has reached its initial state where the entire TL voltage and current is V_{in} and $\frac{V_{in}}{Z_0}$, respectively.

Figure 2.5 depicts V_{out} and I_{out} for the modulation example presented in Figures 2.3 and 2.4.

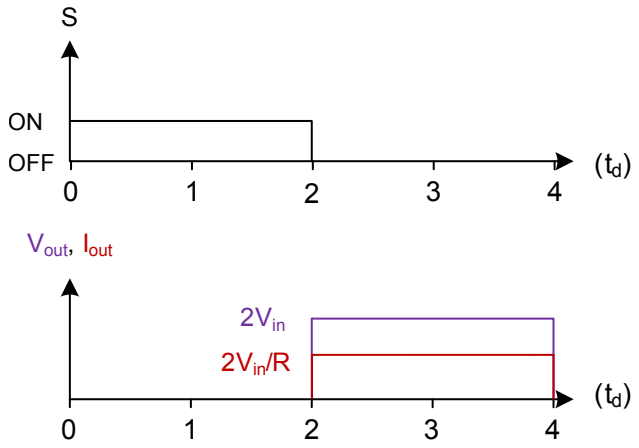

Fig. 2.5 Switch state and output wave forms for the modulation example presented in Figures 2.3 and 2.4.

Figures 2.3 and 2.4 illustrates a particular modulation example. However, V_{out} can be boosted to an arbitrary multiple of V_{in}. Hence, if the modulation principle is extended it is from Figure 2.3 possible to see that

$$V_{out} = V_{in} + \frac{t_{on}}{2t_d} V_{in} \tag{2.3}$$

where

$$t_{on} = 0, 2t_d, 4t_d, 6t_d, ... \tag{2.4}$$

From Figure 2.4 it is possible to realize that

$$I_{out} = \frac{V_{in}}{Z_0} + \frac{t_{on}}{2t_d} \cdot \frac{V_{in}}{Z_0} = \frac{V_{out}}{Z_0} \tag{2.5}$$

where

$$t_{on} = 0, 2t_d, 4t_d, 6t_d, ... \tag{2.6}$$

2.2 TL Theory

As seen in Section 2.1 the pulse duration is proportional to the propagation delay, t_d of the TL. In reality, one condition for obtaining a good pulse shape quality is a pulse duration much larger than the power switch turn on time. Any microstrip TL of reasonable physical size would have put extreme demands on switch performance. Therefore the TL is instead replaced by a lumped transmission line (LTL). An LTL is a number of LC filter segments connected together to emulate TL properties. The LTL is under specific conditions a good approximation of the TL. The LTL combines a reasonable physical size and, for this thesis, suitable value of t_d. One further advantage of the LTL is that its characteristics can easily be adjusted, since it consists of discrete components. The similarities and differences between a TL and a LTL are further described below in this Section.

Figure 2.6 shows a generic circuit model of an infinitesimal length element of a TL [3].

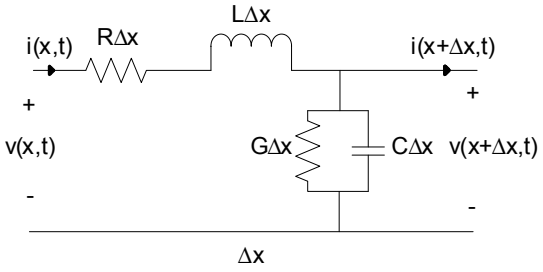

Fig. 2.6 Generic circuit model of an infinitesimal length element of a TL.

This model can according to [3] be used in the derivation of general TL theory. In this theory the TL parameters R,L,C and G are considered as distributed quantities; R is the series resistance per unit length, L is the series inductance per unit length, C is the capacitance per unit length and G is the conductance per unit length.

Figure 2.7 depicts a simplified circuit model of an LTL.

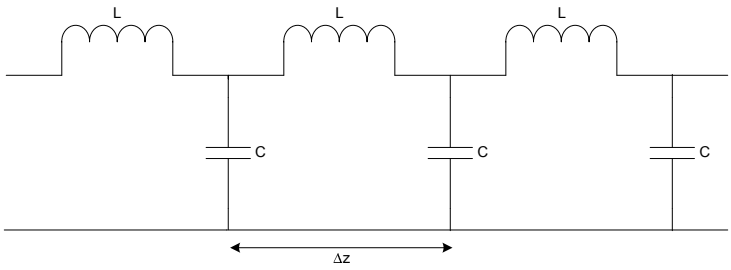

Fig. 2.7 Simplified model for a few impedance sections of an LTL.

The difference between Figure 2.7 compared to Figure 2.6 is that the circuit elements in the latter one is not distributed but discrete lumped components. If, according to [1], the wavelength of the waves travelling in the LTL is much longer than the length of each physical LC-element, Δz, the LTL becomes an approximation of a TL. Under these assumptions the characteristic impedance of a LTL can be described as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.7}$$

where losses are neglected.

Similarly to the TL, the LTL has features like reflection coefficients, see (2.1) and (2.2). Regarding the LTL it can also be shown [1] that there exist a maximum possible frequency for the waves propagating on the LTL:

$$f_{max} = \frac{1}{\pi \cdot \sqrt{LC}} \tag{2.8}$$

According to [7] the propagation time delay of a LTL can be calculated as

$$t_d = N\sqrt{LC} \tag{2.9}$$

where N is the number of discrete LC elements.

Considering (2.7) and (2.9) it is possible to find beneficial integers of N such that Z_0 and t_d can be changed independently.

Chapter 3

PA characterization

This Chapter will present the results and analysis from characterizations of the STI of the PA. The characterizations are divided into two parts: the first part contains measurements to reveal a large signal, resistive representation of the STI. This part is referred to as the dc characterization. The second part consists of ac measurements to obtain a small signal, complex representation of the STI. This part is referred to as the ac characterization. However, this Chapter begins with some theory to explain the function and benefit of envelope tracking: an increased power added efficiency (PAE).

In this thesis project a specific 3.5GHz inverse class-F GaN HEMT power amplifier has been studied. Former research on the specific PA is described in [12].

3.1 Theory

3.1.1 Background of Envelope Tracking

Envelope tracking (ET) is one technique among a few other used for efficiency enhancement of RF PAs. According to [4] there exist mainly four such techniques: Doherty amplifiers, outphasing, envelope elimination and restoration (EER) and ET. The first two ones rely on dynamic load modulation (DLM) as a way to achieve higher efficiency. EER and ET, on the other hand, rely on dynamic supply modulation (DSM).

Figure 3.1 principally depicts the block scheme of a modern ET system.

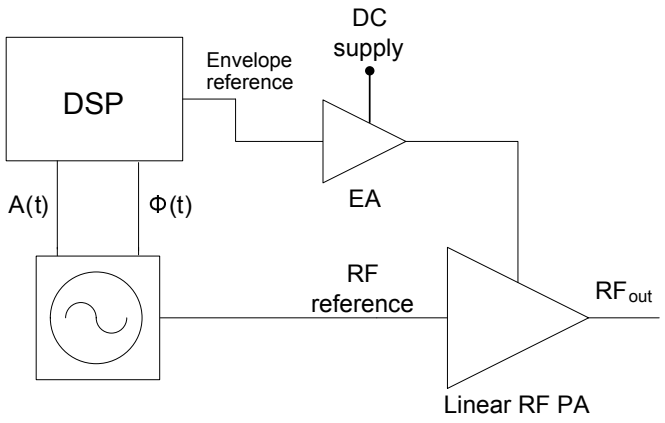

Fig. 3.1 Schematic of a modern DSP controlled ET system.

In an ET system the supply voltage is changed according to the RF input signal envelope. Due to the variations in supply voltage the gain and phase characteristics of the PA will change, [4]. If these changes can be modeled they can be compensated for by a digital pre distorting (DPD) mechanism. The DPD functionality is then implemented in a digital signal processor (DSP), see Figure 3.1. Thereby the DSP controls the phase and amplitude of the RF input signal.

Figure 3.2 shows the typical relationship between power added efficiency (PAE) and P_{out} for RF PAs together with a typical output power probability density function (pdf) for the RF signals [6].

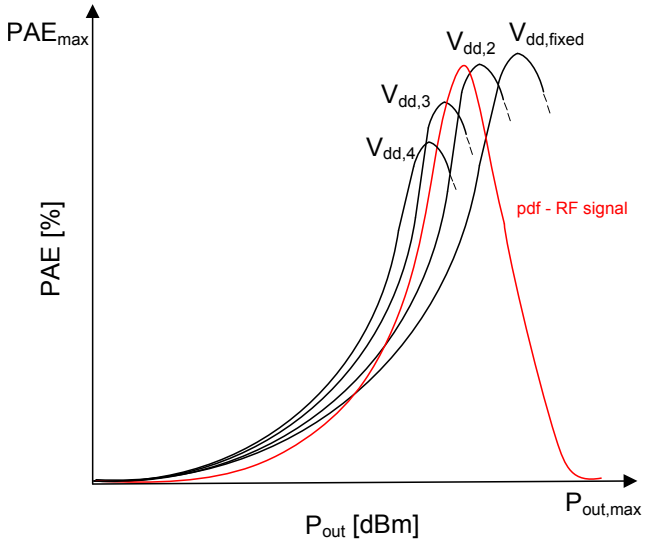

Fig. 3.2 Drain modulation effect on PAE characteristics and probability density function for the RF signal.

The PAE is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} - P_{in}}{V_{dd} I_{dd}} \tag{3.1}$$

where P_{out} and P_{in} are the output and input RF power, respectively, and V_{dd} and I_{dd} are the voltage and current at the supply terminal, respectively.

According to [4] the maximum efficiency point for conventional PAs occurs at near maximum output power. Assume the PA is first supplied at $V_{dd,fixed}$, see Figure 3.2. As can be seen in Figure 3.2 the efficiency decreases when the output power is reduced. However, if the supply voltage is modulated according to the RF signal amplitude, see $V_{dd,2}$, $V_{dd,3}$ and $V_{dd,4}$ in Figure 3.2, the PAE at each $P_{out} < P_{out,max}$ can be improved. By looking at the typical pdf in Figure 3.2, which describes how the signal power is statistically distributed, it can be understood that the average PAE will hence be improved.

The connection between PAE, supply voltage and output power of a PA can be further understood by considering Figures 3.3, 3.4 and 3.5. Figure 3.3 depicts the principal circuit of a class B PA.

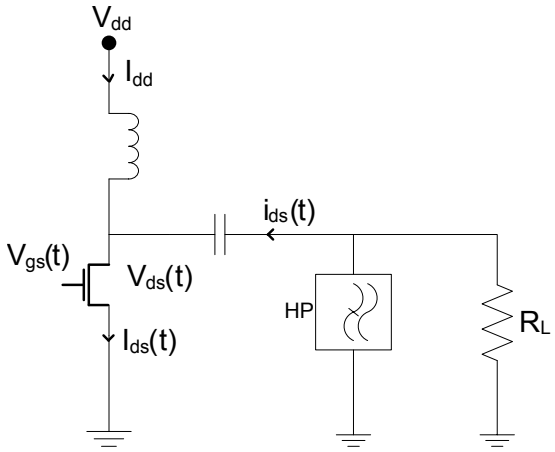

Fig. 3.3 Principal Circuit of a class B amplifier.

In Figure 3.3

$$V_{ds}(t) = V_{dd} + v_{ds}(t) \tag{3.2}$$

and

$$I_{ds}(t) = I_{dd} + i_{ds}(t) \tag{3.3}$$

Figure 3.4 and Figure 3.5 visualizes the load lines for the amplifier in Figure 3.3 at two different supply voltage rates, $V_{dd,1}$ and $V_{dd,2}$, respectively.

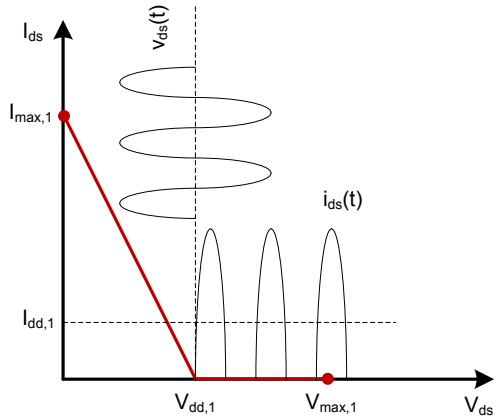

Fig. 3.4 Load line, output RF entities and supply voltage $V_{dd,1}$ for the amplifier in Figure 3.3.

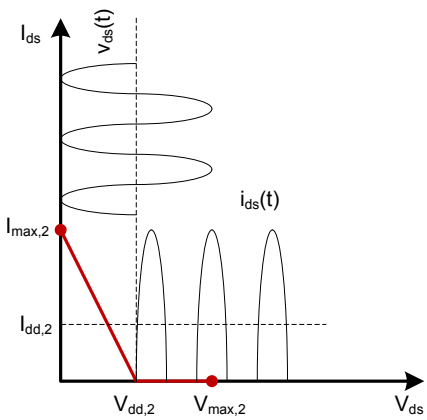

Fig. 3.5 Load line, output RF entities and supply voltage $V_{dd,2}$ for the amplifier in Figure 3.3.

Consider Figures 3.4 and 3.5 and note that

$$\frac{V_{max,1}}{I_{max,1}} = \frac{V_{max,2}}{I_{max,2}} = R_L \tag{3.4}$$

Further on, note that $\max(v_{ds}(t)) = \hat{v}_{ds}$ and $\max(i_{ds}(t)) = \hat{i}_{ds}$.

In Figure 3.4, the load line is not fully utilized since $\max(V_{ds}(t)) < V_{max,1}$ and $\max(I_{ds}(t)) < I_{max,1}$. The output power can be written as

$$P_{out,1} \propto \hat{v}_{ds} \cdot \hat{i}_{ds} \tag{3.5}$$

The input dc power is

$$P_{dc,1} = V_{dd,1} \cdot I_{dd,1} \tag{3.6}$$

The motivation for ET is that since the load line in Figure 3.4 is not fully utilized , V_{dd} can be decreased to, in this case $V_{dd,2}$, as in Figure 3.5. Then, still

$$P_{out,2} = P_{out,1} \propto \hat{v}_{ds} \cdot \hat{i}_{ds} \tag{3.7}$$

but

$$P_{dc,2} = V_{dd,2} \cdot I_{dd,2} < P_{dc,1} \tag{3.8}$$

Hence, by assuming high gain, that is $P_{out,1} >> P_{in,1}$ and $P_{out,2} >> P_{in,2}$

$$PAE_2 \approx \frac{P_{out,2}}{P_{dc,2}} > \frac{P_{out,1}}{P_{dc,1}} = PAE_1 \tag{3.9}$$

Hence, if the PA is not operated in full rail to rail swing, the PAE can for a certain output power be increased by decreasing V_{dd}.

3.1.2 PA model

Figure 3.6 shows a schematic overview of the PA, indicating the STI. Figure 3.7 depicts a circuit model of the STI of the studied PA.

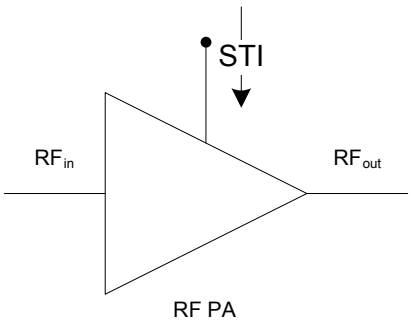

Fig. 3.6 Schematic overview of PA.

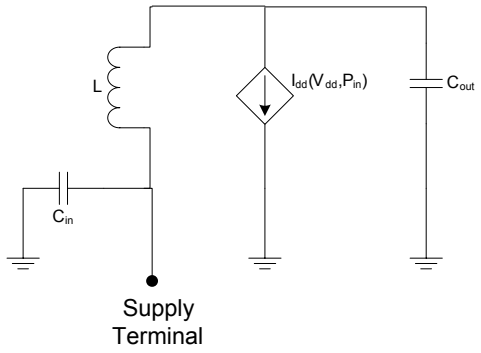

Fig. 3.7 Circuit model of the supply terminal of the PA.

In Figure 3.7 C_{out} represents the transistor output capacitance, C_{in} a low frequency decoupling and L a RF blocking. The basic model in Figure 3.7 served as a motivation for the dc characterization measurements: during dc measurements the STI can be seen as a resistance, see Section 3.1.3. Moreover, in the simulations the designed EA is connected to the circuit model in Figure 3.7, see Section 4.2.2.

3.1.3 Background Theory for DC and AC Characterization

In general for all PAs, I_{dd} is a function of both V_{dd} and P_{in}. In both the dc and ac characterization measurements of the STI, V_{dd} and P_{in} are independently varied over a certain interval. The dc characterization of the PA contains static, large signal measurement of the real part of the STI, R_{ST}. Hence

$$R_{ST} = \frac{V_{dd}}{I_{dd}\left(V_{dd}, P_{in}\right)} \tag{3.10}$$

is calculated at each operating point.

The difference in the ac characterization measurements is that a super imposed ac signal, $\Delta V_{dd} = v_{ac}sin(\omega t)$, is present at the supply terminal. Hence

$$V_{dd} = V_{DD} + \Delta V_{dd} \tag{3.11}$$

and

$$I_{dd} = I_{DD} + \Delta I_{dd} \tag{3.12}$$

where V_{DD} and I_{DD} are bias points. An arbitrary operating point can therefore be described as $(V_{dd} + \Delta V_{dd}, P_{in})$. The effect of ΔV_{dd} on I_{dd} can be understood by a first order Taylor expansion:

$$\begin{aligned} I_{dd}(V_{dd}, P_{in}) = I_{dd}(V_{DD} + \Delta V_{dd}, P_{in}) &= I_{dd}(V_{DD}, P_{in}) + \Delta I_{dd} \\ &\approx I_{dd}(V_{DD}, P_{in}) + \frac{\partial I_{dd}}{\partial V_{dd}}\Big|_{V_{DD}, P_{in}} \Delta V_{dd} \end{aligned} \tag{3.13}$$

$$\Rightarrow \Delta I_{dd} \approx \frac{\partial I_{dd}}{\partial V_{dd}}\Big|_{V_{DD}, P_{in}} \Delta V_{dd} = \frac{\partial I_{dd}}{\partial V_{dd}}\Big|_{V_{DD}, P_{in}} v_{ac}sin(\omega t) \tag{3.14}$$

A complex, small signal representation of the STI, $Z_{ST,ss}(\omega)$, is then calculated as

$$\Rightarrow |Z_{ST,ss}(\omega)| = \frac{\left|\Delta V_{dd}\right|}{\left|\Delta I_{dd}\right|} = \frac{1}{\frac{\partial I_{dd}}{\partial V_{dd}}} \tag{3.15}$$

and

$$\angle Z_{ST,ss}(\omega) = \angle \Delta V_{dd} - \angle \Delta I_{dd} \tag{3.16}$$

According to (3.15), the small signal impedance can be described as the inverse of a differential conductance.

3.2 Measurement Setups

In this Section the laboratory setups for both dc and ac characterization measurements will be presented with drawings, tables and photos.

3.2.1 Setup for DC Characterization

Figure 3.8 depicts a schematic overview of the laboratory equipment setup that was used in the dc characterization measurements.

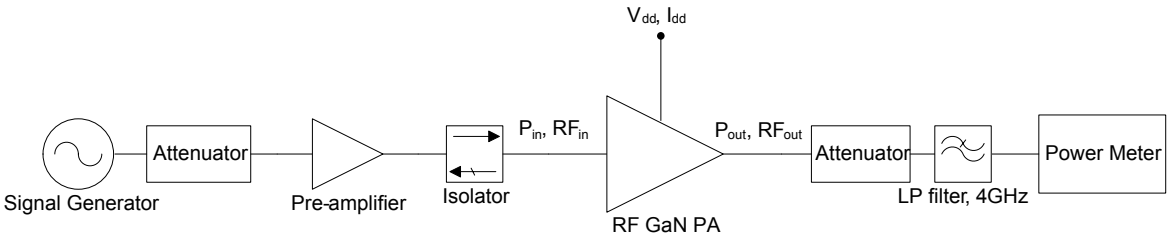

Fig. 3.8 Measurement setup for the dc characterization measurements.

The attenuators in Figure 3.8 were used in order to operate the rest of the instruments at proper power levels. The isolator was used in order to prevent reflections from propagating back to the pre-amplifier and the signal generator. By using the low-pass filter it was ensured that only the fundamental frequency component was measured. During the measurements the signal generator was operated at $3.5GHz$ and V_{gs} was held fixed at $-2.5V$.

Figure 3.9 is a photo corresponding to the measurements setup shown in Figure 3.8.

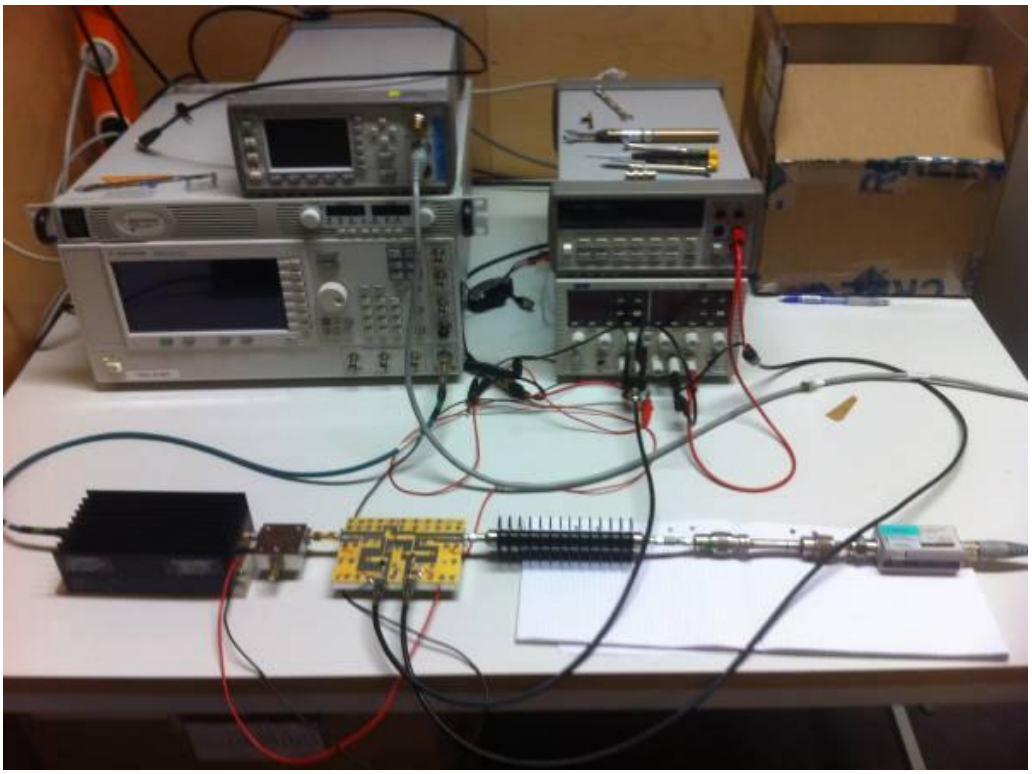

Fig. 3.9 Photo of the dc characterization measurement setup.

Table 3.2.1 contains the instruments used in the dc characterization measurements.

Table 3.1: Instrument setup for dc characterization measurements.

Type	Name	Function
Analog Signal Generator	Agilent Technologies PSG, E8257C	P_{in}
DC Power Supply	Agilent Technologies N5749A	$V_{pre-amp}$
DC Power Supply	TT CPX400DP	V_{gs}, V_{dd}
EPM Series Power Meter	Hewlett Packard E4419B	P_{out}
Power Sensor	Agilent Technologies E4413A	P_{out}
Multimeter	Agilent Technologies 34401A	I_{dd}
Pre-amplifier	Mini-circuits 15542, ZHL-42W-SMA	
Isolator	Quest Microwave Inc. SM2040C09	
LP Filter	Microlab/FXR Rosenberger, LA-40N 4000 Mc.	
30dB Attenuator	Weinschel Associates, WA47-30	
2 X 10dB Attenuators	SMA, 2W	
6dB Attenuator	SMA, 2W	

Table 3.2.1 contains the instruments used in the renewed dc characterization measurements.

Table 3.2: Instrument setup for new dc characterization measurements.

Type	Name	Function
Signal Generator	Rhode & Schwartz, SMR 20	P_{in}
Power Meter	Rhode & Schwartz, NRVS 1020.1809.02	P_{out}
Power Sensor	TDMA ModelNRV-Z31	P_{out}
DC Power Supply	Topward 6303 AS	V_{dd}, V_{gs}
DC Power Supply	LTRONIX B502D	$V_{pre-amp}$
Dual Display Multimeter	Fluke 45	V_{dd}
Dual Display Multimeter	Fluke 45	I_{dd}
True RMS Multimeter	Fluke 87	V_{gs}
Pre-amplifier	Mini-circuits 15542, ZHL-42W-SMA	
Isolator	ISO-001	
LP Filter	Microlab/FXR Rosenberger, LA-40N 4000 Mc.	
6dB Attenuator	SMA, 2W	
2 X 10dB Attenuators	SMA, 2W	
30dB Attenuator	Weinschel Corp. Model 47-30-43	

3.2.2 Setup for AC Characterization

Similarly to the dc characterization, where R_{ST} were measured with respect to both supply voltage and input power, $Z_{ST,ss}(\omega)$ has to be measured while the PA is up and running for various V_{DD} and P_{in}. One measurement method, found in [2], was to feed the PA with a dc supply and at the same time inject a superimposed ac voltage with the help of a transformer. $Z_{ST,ss}(\omega)$ should then be estimated by measuring the voltage and current at the supply terminal with a voltage probe and a current probe, respectively. Information about the voltage and current magnitudes as well as the phase between the voltage and current could then be used to calculate $Z_{ST,ss}(\omega)$ at each operating point, see Section 3.1.3.

Figure 3.10 shows the measurement setup for the $Z_{ST,ss}(\omega)$ measurements of the PA. The transformer as well as the capacitor C_{inj}, and the biasing voltage is referred to as the injection circuit, see Figure 3.10. The voltage and current at the ST of the PA were measured with oscilloscope probes. More information about how the $Z_{ST,ss}(\omega)$ were carried out can be found in Appendix A.

Figure 3.10 is a schematic overview of the measurement setup for the ac characterization measurements.

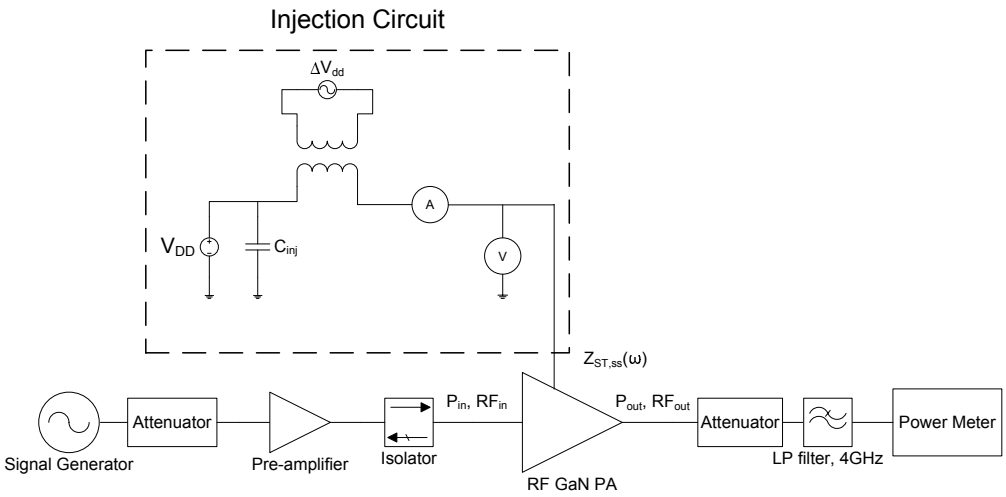

Fig. 3.10 Measurement setup for the ac characterization measurements.

Figure 3.11 is a photo corresponding to the measurements setup shown in Figure 3.10.

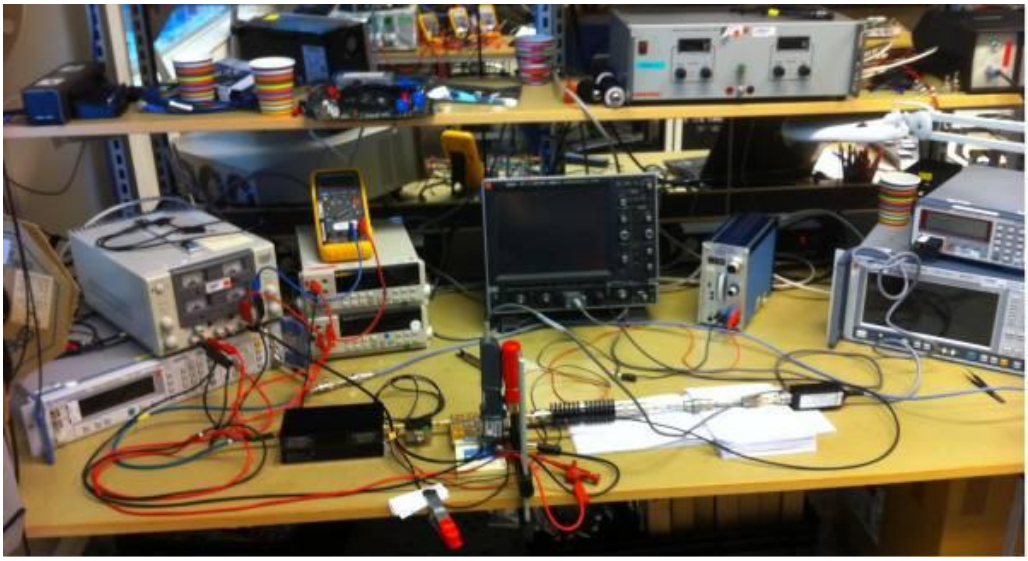

Fig. 3.11 Overview photo of the ac characterization measurements setup.

Figures 3.12-3.13 are two visualizations of the connection between the injection circuit and the PA.

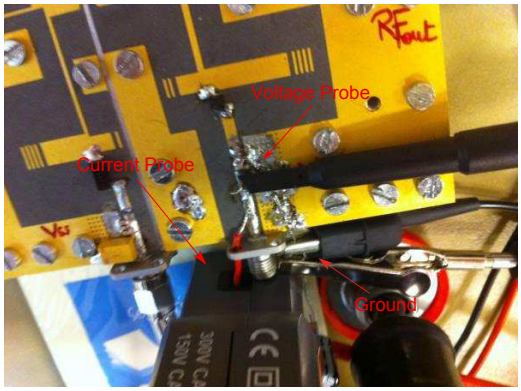

Fig. 3.12 Connection between injection circuit and PA with current and voltage probes.

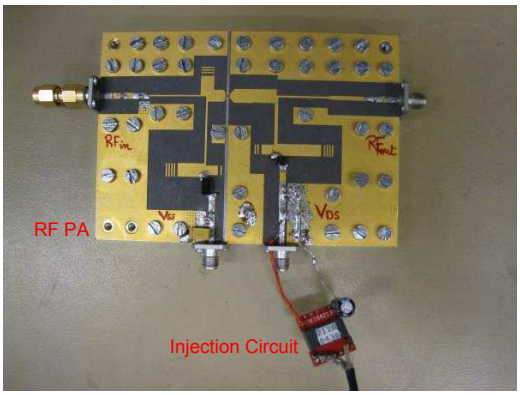

Fig. 3.13 Connection between injection circuit and PA.

Table 3.3 summarizes the instruments used in the ac characterization measurements.

Table 3.3: Instrument setup for ac characterization measurements.

Type	**Name**	**Function**
Signal Generator	Rhode & Schwartz, SMR 20	P_{in}
Signal Generator	Rhode & Schwartz, SMIQ 03B	ΔV_{dd}
Power Meter	Rhode & Schwartz, NRVS 1020.1809.02	P_{out}
Power Sensor	TDMA ModelNRV-Z31	P_{out}
DC Power Supply	Topward 6303 AS	V_{DD}, V_{gs}
DC Power Supply	LTRONIX B502D	$V_{pre-amp}$
2 Dual Display Multimeter	Fluke 45	V_{DD}, I_{DD}
True RMS Multimeter	Fluke 87	V_{gs}
Oscilloscope	LeCroy Wave Surfer 44MXs-A	$\Delta V_{dd}, \Delta I_{dd}$
Current Probe	LeCroy AP015	
Probe	LeCroy PP009	
Pre-amplifier	Mini-circuits 15542, ZHL-42W-SMA	
Isolator	ISO-001	
6dB Attenuator	SMA, 2W	
LP Filter	Microlab/FXR Rosenberger, LA-40N 4000 Mc.	
2 X 10dB Attenuators	SMA, 2W	
30dB Attenuator	Weinschel Corp. Model 47-30-43	
ER Planar Transformer	EGMTC AB, KER 184212	Injection Circuit
Electrolytic capacitor, (C_{inj})	Jamicon: SKR220M2AE11VU	Injection Circuit

3.3 Measurement Results

3.3.1 DC Characterization

Measurement points were taken by independently sweeping V_{dd} and P_{in} from 1V to 28V and from 0dBm to 29dBm, respectively. For each combination of V_{dd}, P_{in}, together with I_{dd} and V_{dd}, the PAE and R_{ST} were calculated. PAE was calculated as in (3.1) and R_{ST} as

$$R_{ST} = \frac{V_{dd}}{I_{dd}(V_{dd}, P_{in})} \tag{3.17}$$

Figure 3.14 is visualizing the result obtained from the dc characterization measurements.

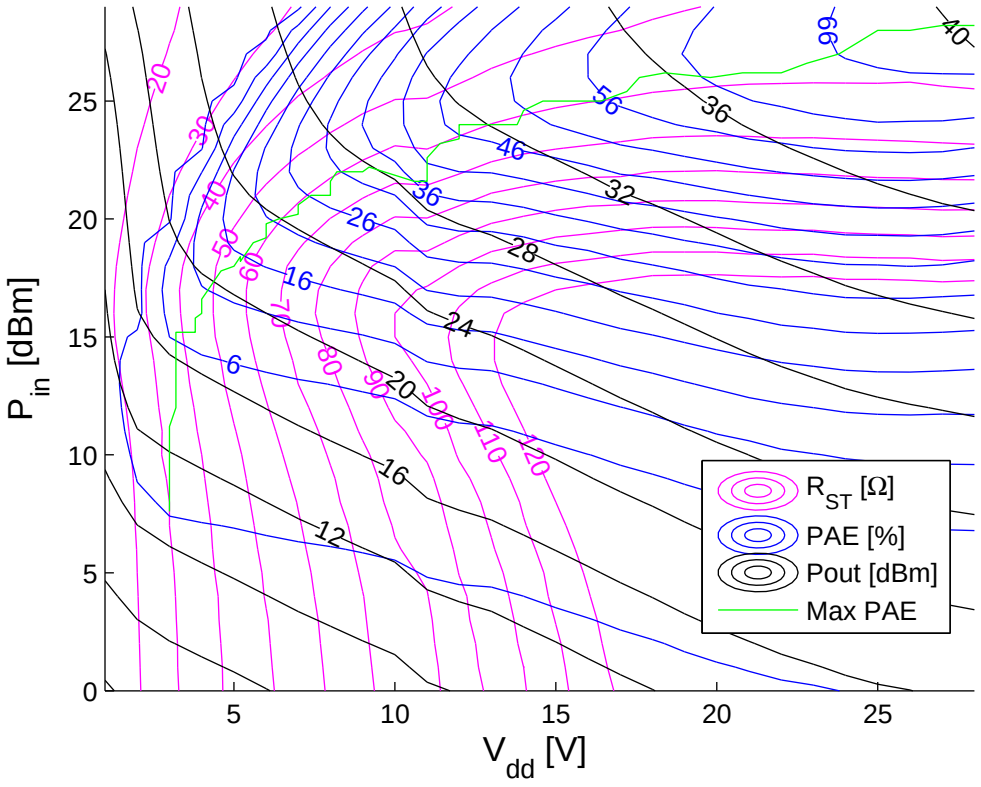

Fig. 3.14 Iso curves of measured R_{ST}, PAE and P_{out} together with maximum PAE trajectory.

In Figure 3.14 the visible range of iso levels in R_{ST} is chosen to $20 - 120\Omega$. The max PAE trajectory is added in Figure 3.14 in order to show the maximum PAE values for each constant P_{out} curve. Note that the max PAE trajectory to some extent correlates with the $R_{ST} = 60\Omega$ curve. The principal behaviour of P_{out} and PAE depicted in Figure 3.14 seems to correlate well with the result presented in [9].

Figure 3.15 shows new dc characterization measurements which were taken in conjunction with the ac characterization measurements. The reason for redoing the dc characterization measurements was because the PA, at some point in the laboratory measurements, suddenly seemed to have changed its characteristics. (After some rough control measurements it seemed that the threshold voltage had changed a bit for some unclear reason.)

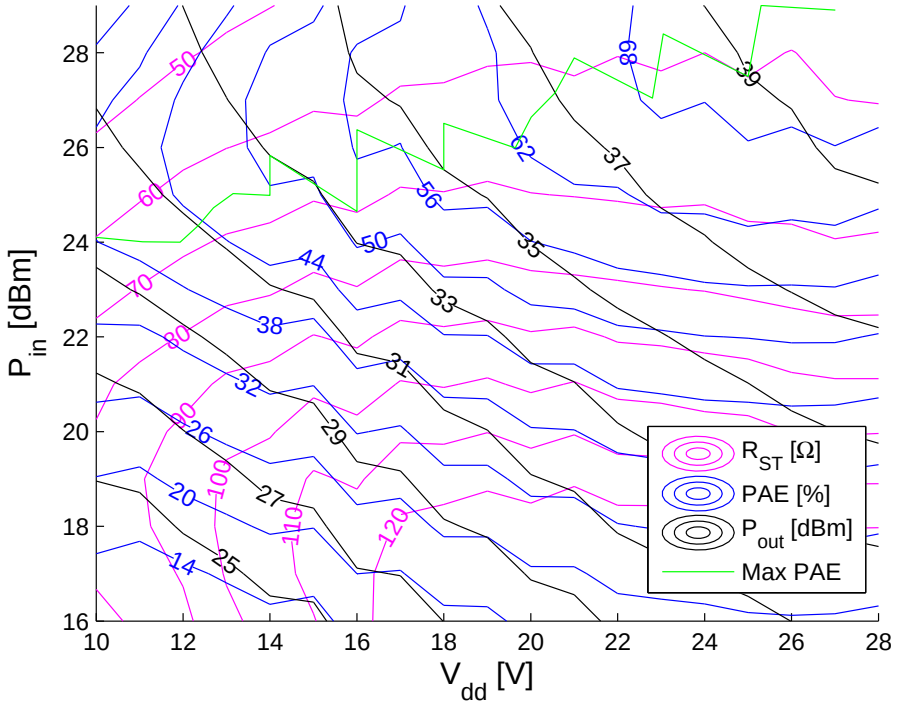

Fig. 3.15 Iso curves of measured R_{ST}, PAE and P_{out}, together with the max PAE trajectory.

In Figure 3.15 the visible range of iso levels in R_{ST} is chosen to $50 - 120\Omega$. Note in Figure 3.15 that the (V_{dd}, P_{in}) region is decreased as compared to Figure 3.14. The reason is that this is the area where the integrated EA-PA system were chosen to be tested.

3.3.2 AC Characterization

Figure 3.16 shows how the iso curves of $|Z_{ST,ss}(\omega)|$, PAE and P_{out} is oriented in the (V_{dd}, P_{in}) plane. In the ac characterization measurements the frequency of the superimposed ac signal was stepped from $0.5MHz$ to $2MHz$ with an increment of $0.5MHz$. Figure 3.16 depicts $|Z_{ST,ss}(\omega)|$ at $2MHz$, but the behaviour at the three other measured frequencies is very similar, see Appendix B.

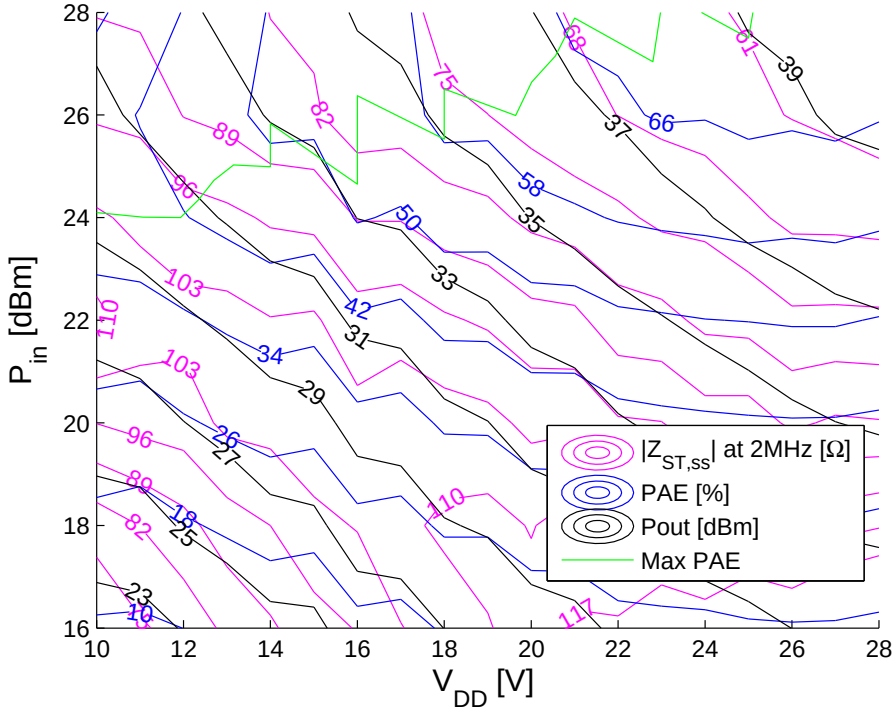

Fig. 3.16 Iso curves of measured $|Z_{ST,ss}(\omega)|$ at $2MHz$ together with PAE and P_{out}.

The grid region in Figures 3.16 and 3.17 is the same as in Figure 3.15.

Figure 3.17 depicts how the phase is oriented in the (V_{dd}, P_{in}) plane in relation to $|Z_{ST,ss}(\omega)|$. The phase appearance at the other frequencies can be seen in Appendix B.

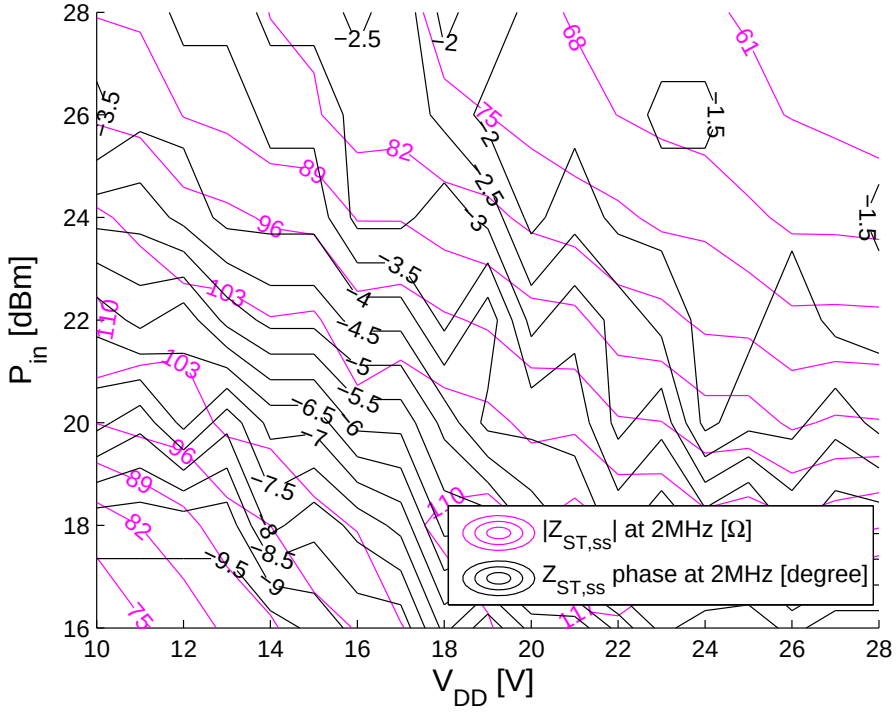

Fig. 3.17 Iso curves of $|Z_{ST,ss}(\omega)|$ and $Z_{ST,ss}(\omega)$ phase at $2MHz$.

Note how the phase varies with V_{DD} and P_{in} in Figure 3.17.

3.4 Analysis

This Section begins with an investigation to determine the plausibility of the results obtained in the dc and the ac characterization measurements. Thereafter the guidelines for the EA design is stated.

3.4.1 Analysis of DC Characterization

From Figure 3.14 and Figure 3.15 it is possible to see that the max PAE trajectory more or less is aligned with a certain constant R_{ST} line. Even though an inverse class F PA was used, this behaviour could be explained with the help of the load line of the class B amplifier, see Section 3.1. This analysis is based on two operating points on the max PAE trajectory, where the PA is operating in full rail to rail swing, see Figure 3.18 and Figure 3.19.

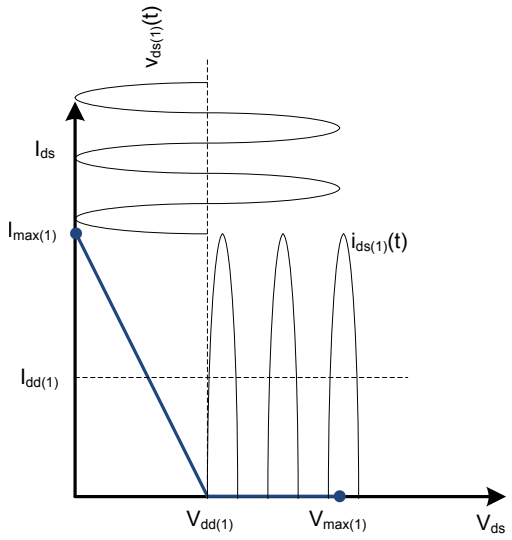

Fig. 3.18 Load line and RF output entities for operating point $V_{dd(1)}$.

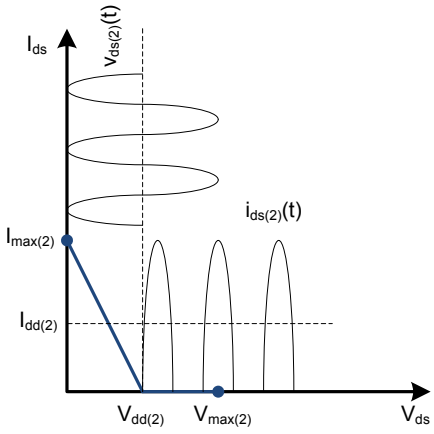

Fig. 3.19 Load line and RF output entities for operating point $V_{dd(2)}$.

By considering Figures 3.18 and 3.19 it is assumed that

$$\begin{cases} V_{max(2)} = \frac{V_{max(1)}}{x} \\ I_{max(2)} = \frac{I_{max(1)}}{x} \end{cases} \tag{3.18}$$

for some $x > 1$. From the load line corresponding to the bias point $V_{dd(1)}$ it can be stated that

$$P_{out(1)} \propto V_{max(1)} \cdot I_{max(1)} \tag{3.19}$$

and

$$R_{ST(1)} = \frac{V_{dd(1)}}{I_{dd(1)}} \tag{3.20}$$

If we chose another operational point of the PA, $V_{dd(2)}$, we can from the corresponding load line state that

$$P_{out(2)} \propto V_{max(2)} \cdot I_{max(2)} = \frac{V_{max(1)}}{x} \cdot \frac{I_{max(1)}}{x} = \frac{P_{out(1)}}{x^2} \tag{3.21}$$

However, assuming the same load line slope

$$R_{ST(2)} = \frac{V_{dd(2)}}{I_{dd(2)}} = \frac{\frac{V_{dd(1)}}{x}}{\frac{I_{dd(1)}}{x}} = R_{ST(1)} \tag{3.22}$$

Hence, theoretically R_{ST} is the same for the two different operating points, even if P_{out} has changed. Based on the analysis it seems reasonable that the max PAE trajectory correlates with a certain R_{ST} contour, even though the analysis is based on the class B PA.

3.4.2 Analysis of AC Characterization

In this Section an attempt to test the plausibility of the ac characterization measurements, with the help of the dc characterization measurements, is described. Figure 3.20 depicts I_{dd} as a function of V_{dd} for a set of constant P_{in}. Figure 3.20 is intended to describe how the following analysis of the ac characterization measurements have been carried out.

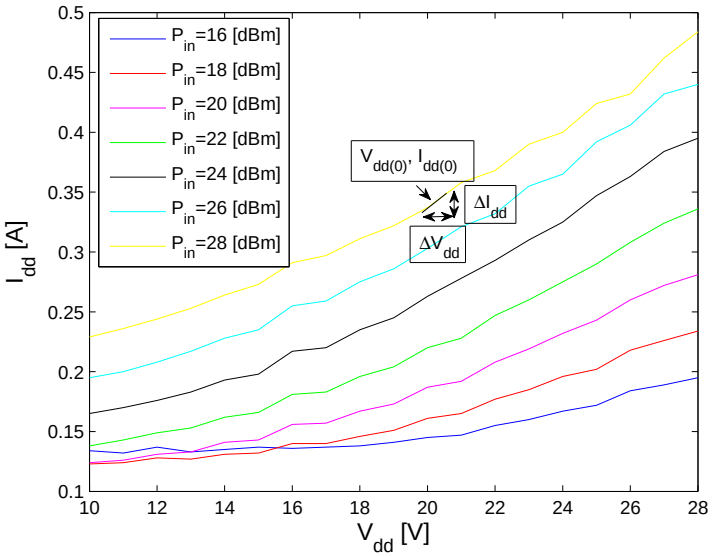

Fig. 3.20 $I_{dd}(V_{dd})$ for constant P_{in}.

In Figure 3.20 $(V_{dd(0)}, I_{dd(0)})$ represents an arbitrary operating point. The inverse slope of a straight line connecting origin and $(V_{dd(0)}, I_{dd(0)})$ would represent one of the R_{ST} values obtained from the dc characterization measurements. Hence

$$R_{ST(0)} = \frac{V_{dd(0)}}{I_{ds(0)}} \tag{3.23}$$

In Figure 3.20 ΔV_{dd} and ΔI_{dd} represent the super imposed ac signals which were applied in each operating point during the ac characterization measurements where

$$|Z_{ST,ss}(\omega)| = \frac{\left|\Delta V_{dd}\right|}{\left|\Delta I_{dd}\right|} \tag{3.24}$$

The ac signals ΔV_{dd} and ΔI_{dd} formed the basis for small signal measurements. In order to analyze the correctness of the ac characterization measurements it was decided to calculate a small signal resistance, $R_{ST,ss}$, based on the curves in Figure 3.20. $R_{ST,ss}$ could then be compared to the real part of $Z_{ST,ss}$.

The curves in Figure 3.20 were first fitted with polynomials of order 4, using Matlab. The polynomial functions together with their respective coefficients were then differentiated to obtain the conductance as a function of V_{dd} for each P_{in}. Taking the inverse of the conductance in each point gave the $R_{ST,ss}$ values.

In Figure 3.21 $R_{ST,ss}$ is plotted with iso curves. For comparison, the real part of $Z_{ST,ss}$ at 2MHz is plotted with iso curves in Figure 3.22.

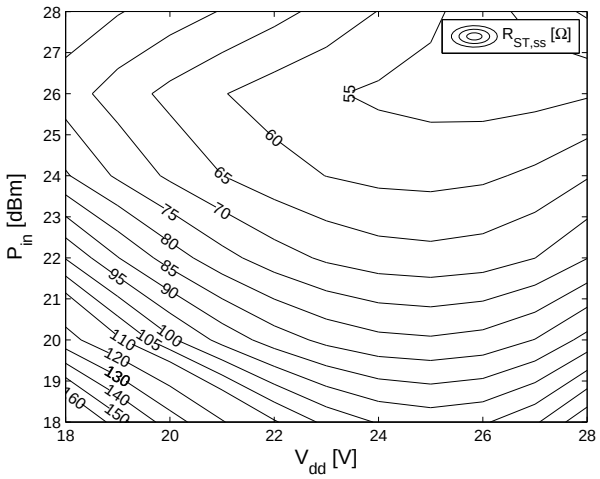

Fig. 3.21 Iso curves of $R_{ST,ss}$.

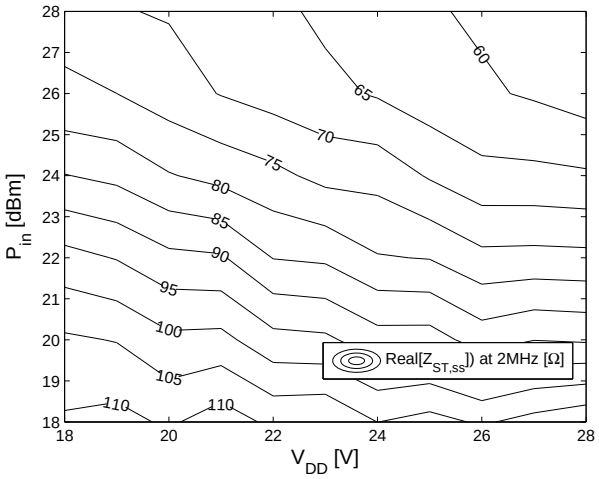

Fig. 3.22 Iso curves of $\Re Z_{ST,ss}(\omega)$ at 2MHz.

As an alternative way of comparison, a contour plot of the difference between $R_{ST,ss}$ and $\Re Z_{ST,ss}(\omega)$ is presented in Figure 3.23.

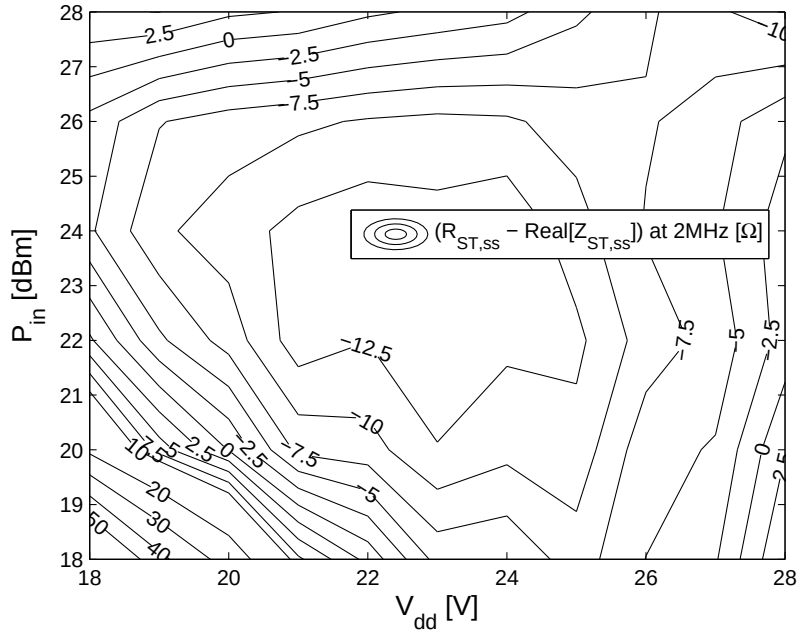

Fig. 3.23 Iso curves of the difference between $R_{ST,ss}$ and the real part of $Z_{ST,ss}(\omega)$ in the (V_{dd}, P_{in}) plane.

The grid area in Figure 3.21, 3.22 and 3.23 had to be decreased a bit compared to Figure 3.16 to avoid outliers. Even though the iso curves in Figure 3.21 and Figure 3.22 is not aligned, which can more easily be seen with the help of Figure 3.23, the behaviour in Figures 3.21 and 3.22 are considered similar. Based on Figures 3.21, 3.22 and 3.23 the results from the ac characterization measurements are considered trustworthy. This conclusions would justify the behaviour in Figures 3.16 and 3.17. The injection circuit measurements introduced some uncertainty and mainly perhaps for reactive elements, see Appendix A. The phase measurements of $Z_{ST,ss}$ are seemed as trustworthy. Since the phase values in Figure 3.17 are conceived as small, the reactive component of $Z_{ST,ss}$ is considered as small. Therefore the measurement results of $|Z_{ST,ss}|$ are considered valid.

3.4.3 Discussion and Guidelines for EA design

The ST of the PA is, in this thesis, supposed to be fed with a pulsed voltage supply. It is unclear what characteristics of the STI that a pulsed voltage supply would excite. However, the pulsed voltage supply was considered mainly as a large signal injection at the ST. Therefore, the measurement results of R_{ST} in Figure 3.15 were considered the most trustworthy description of the STI, for a pulsed voltage supply. Based on Figure 3.15, it was decided to design Z_0 of the EA to be 60Ω. This since R_{ST} is more or less constant 60Ω for a suitable choice of P_{in} and voltages above $15V$. By using a suitable constant P_{in} and create voltage pulses of $15V$, $20V$ and $25V$ it could in the integration then be tested if match could be obtained for the different voltage pulses. If match could be obtained, the result would indicate that R_{ST} best describes the STI, for a pulsed voltage supply. Moreover, if this would be the case, the choice of Z_0 would also enable an operation of the PA close to the max PAE trajectory. Assuming R_{ST} best describes the STI during a pulsed voltage supply. Then, in a real ET system, P_{in} and V_{dd} could have been carefully co controlled to follow the max PAE trajectory, while maintaining a more or less constant STI.

It is not known to what extent an imaginary part of the STI would affect the pulse shape during a pulsed supply. Even if it would excite the small signal features of the STI to some extent, for higher values of P_{in} the imaginary part is relatively small. Assuming the STI would be best described by $Z_{ST,ss}$. Tracking the max PAE trajectory would not preserve constant $|Z_{ST,ss}|$, see Figure 3.16. If a co control of supply voltage and P_{in} would have been applied to preserve constant $|Z_{ST,ss}|$, the PAE would increase as the supply voltage decreases, but the PA would be forced to operate in a limited P_{out} range.

Regardless if Figure 3.15 or Figure 3.17 best describes the STI at a pulsed voltage supply, any voltage pulse is likely to cross contours of constant impedance. Probably such an affect would mainly influence the shape of the pulse flanks.

Chapter 4

Design of Envelope Amplifier

This Chapter will describe the design of an LTL based EA. Initially, as a starting point for the EA construction, there was a prototype of an LTL based converter at hand. In Section 4.1 it will be described how the converter was reconfigured and in Section 4.2.2 the simulation results of the designed EA performance is presented with corresponding analysis.

4.1 Circuit Reconfiguration

In this Chapter, an EA of the principal form shown in Figure 4.2 was designed and reconfigured from the circuit in Figure 4.1.

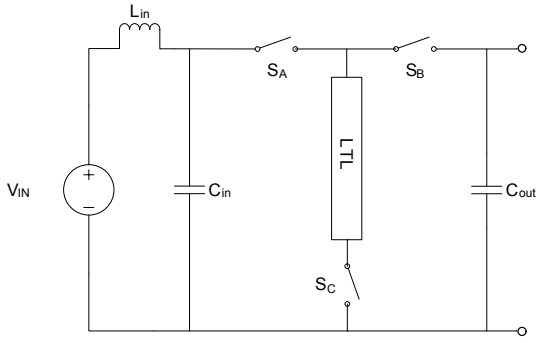

Fig. 4.1 Circuit model of a buck-boost derived LTL converter.

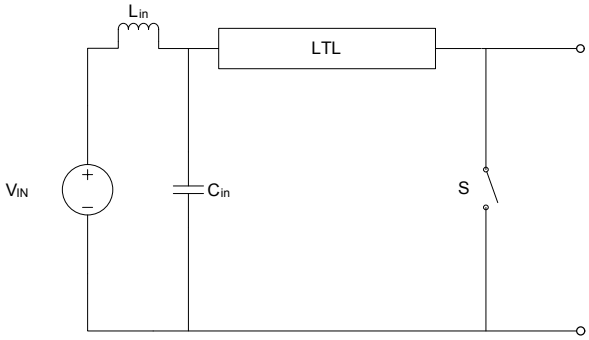

Fig. 4.2 Circuit model of the boost derived EA to be used.

The LTL in the circuit shown in Figure 4.1 had 40 LC sections connected in series. The EA in Figure 4.2 will use the same LTL structure of 40 elements. The input filter, (L_{in}, C_{in}), was unchanged in the reconfiguration. The LTL inductances were kept but the LTL capacitors were changed as well as the switch type. More details of the reconfiguration can be seen in Section 4.1.1.

4.1.1 Component Selection

Table 4.1 summarizes component data for the LTL and the switches used in the converter depicted in Figure 4.1.

Table 4.1: Component data for the LTL and the switches used in the converter in Figure 4.1.

LTL capacitor	**LTL inductor**	**Switch** (S_A, S_B, S_C)
Manufacturer: Murata (C=560pF)	Manufacturer: Coilcraft (L=100nH)	Manufacturer: Infineon
Product name: GRM1555C1H561J	Product name: SLC7530S-101ML	Product name: IPB027N10N3G

As can be seen in Table 4.1 the LC sections in the LTL of the converter in Figure 4.1 had an inductance value of $100nH$ and a capacitor value of $560pF$. Consequently according to (2.7) the characteristic impedance was 13.4Ω. As mentioned in Section 3.4.2 a guideline in the EA design would be

$Z_0 = R_{ST} = 60\Omega$, since this would be beneficial for obtaining high PAE. Regarding the LTL it was decided to keep the inductors and to change the capacitors. According to (2.7) the new capacitor value is given by

$$C = \frac{L}{Z_0^2} = \frac{100 \cdot 10^{-9}}{3600} \approx 27.8pF \tag{4.1}$$

In the EA configuration a large C_{ds} would be a problem when the switch turns off: the output pulse would meet the load in parallel with C_{ds}. In order to obtain fast switching, another criteria for the new switch was a low C_{gs}. Table 4.2 contains the selected LTL capacitor and EA switch.

Table 4.2: Selected components in the EA design.

LTL capacitor	**Switch**
Manufacturer: Murata (C=27pF)	Manufacturer: IRF
Product name: GRM1555C1H270JA01D	Product name: IRFS3806PBF

The new switch in Table 4.2 has lower C_{ds} and C_{gs} than the switch in Table 4.1. The value of the new LTL capacitor is $27pF$. Theoretically the new Z_0 would be

$$Z_0 = \sqrt{\frac{100 \cdot 10^{-9}}{27 \cdot 10^{-12}}} \approx 60.9\Omega \tag{4.2}$$

Moreover, f_{max} and t_d would be

$$f_{max} = \frac{1}{\pi \cdot \sqrt{100 \cdot 10^{-9} \cdot 27 \cdot 10^{-12}}} \approx 194MHz \tag{4.3}$$

and

$$t_d = 40 \cdot \sqrt{100 \cdot 10^{-9} \cdot 27 \cdot 10^{-12}} \approx 66ns \tag{4.4}$$

respectively.

4.1.2 Estimation of Transistor Losses

The power losses in the switch will be calculated for the modulation cycle seen in Figure 4.3.

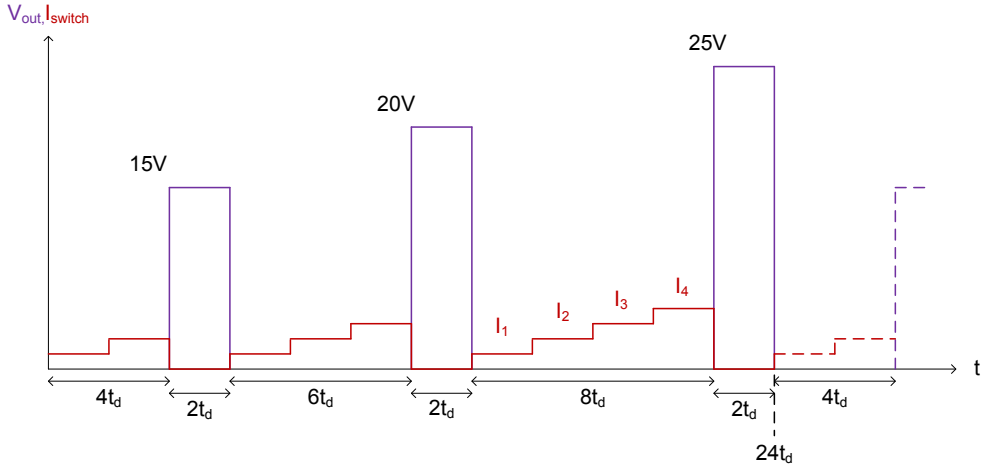

Fig. 4.3 Modulation cycle which the calculated transistor losses will be based on.

The switch current during the storage state will be used for estimation of the conduction losses, see I_{switch} in Figure 4.3. The generic formula, [8], for conduction losses is given by

$$P_{on} = \frac{t_{on}}{T} I_o^2 R_{ds,on} \tag{4.5}$$

where T is the switching period.

When it comes to switching losses in power electronics, a very typical situation is as follows: an input voltage drives an inductive load current when the power switch is on, and when the switch is off the current falls off through a diode [8]. At turn on the switch must take over the hole load current before the diode can stop conducting and the switch voltage can go to zero. At turn off the switch voltage must increase to the input voltage before the diode can take over the current and the switch can stop conducting.

The derivation of switching losses presented in [8] will however not be valid when it comes to the converter presented in Figure 4.2. In the case of turn off the switch voltage does not have to increase to the input voltage in order for the load to start taking over the current because the drain is connected to zero voltage. At turn on the voltage will start to fall as soon as the current start to increase through the switch. Considering Figure 4.3 it can be stated that the switching losses occur at both positive and negative flanks of all pulses and can be calculated as

$$P_{sw} = (W_{t,on(1)} + W_{t,off(1)})f_s + (W_{t,on(2)} + W_{t,off(2)})f_s + (W_{t,on(3)} + W_{t,off(3)})f_s \tag{4.6}$$

where the numbers 1, 2 and 3 in (4.6) refer to the number of pulses in Figure 4.3.

In order to find the expressions for the different energy losses at turn on and turn off in (4.6) it is assumed that the curves of switch voltage and switch current during turn on and turn off can be described as in Figure 4.4 and 4.5.

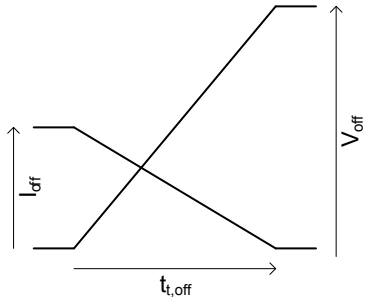

Fig. 4.4 Assumed voltage and current wave forms at turn off.

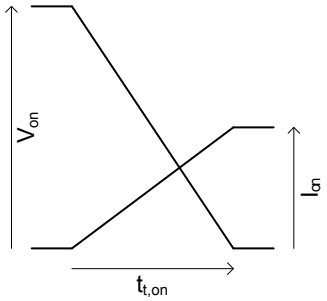

Fig. 4.5 Assumed voltage and current wave forms at turn on.

Based on the analysis in Figure 2.3 and Figure 2.4 the general expressions for V_{on}, I_{on}, V_{off} and I_{off} for any modulation cycle of multiple $2t_d$-length are summarized in Table 4.3.

Table 4.3: General expressions for the magnitudes defined in Figure 4.4 and Figure 4.5.

$\mathbf{V_{on}}$	$\mathbf{I_{on}}$	$\mathbf{V_{off}}$	$\mathbf{I_{off}}$
V_{in}	$2 \cdot \frac{V_{in}}{Z_0}$	V_{out}	$\frac{t_{on}}{t_d}\frac{V_{in}}{Z_0}$

To simplify it is assumed that $t_{t,on} = t_{r,g}$ and $t_{t,off} = t_{f,g}$, where $t_{r,g}$ and $t_{f,g}$ are the rise and fall times of the gate, respectively. According to [10], $t_{r,g}$ and $t_{f,g}$ are specified for certain conditions and for certain values of load capacitor, C_L. In this thesis it is assumed that $C_L = C_{gs}$. Moreover, the characteristics

$$\begin{cases} C_{iss} = C_{gs} + C_{gd} \\ C_{rss} = C_{gd} \\ C_{oss} = C_{ds} + C_{gd} \quad \text{if } V_{gs} = 0V, f = 1MHz, C_{ds} = 0V. \end{cases} \tag{4.7}$$

are collected from the switch datasheet, [11]. The characteristics corresponding to (4.7) have been used to find C_{gs} at both turn on and turn off. According to the switch datasheet, assuming (4.7), the C_{gs} is considered as being more or less constant around $1000pF$. Consequently, according to the driver datasheet, $t_{t,on} \approx 12ns$ and $t_{t,off} \approx 3ns$.

Considering Figure 4.4 the switch voltage and switch current can during the turn off transition be described as

$$v(t) = V_{off}\frac{t}{t_{t,off}} \tag{4.8}$$

and

$$i(t) = I_{off}(1 - \frac{t}{t_{t,off}}) \tag{4.9}$$

respectively.

A general expression for the turn-off energy dissipated in the switch is

$$\begin{aligned} W_{off} &= \int_0^{t_{t,off}} v(t)i(t)dt = V_{off}I_{off} \int_0^{t_{t,off}} \frac{t}{t_{t,off}}(1 - \frac{t}{t_{t,off}})dt \\ &= \frac{V_{off}I_{off}}{t_{t,off}} \int_0^{t_{t,off}} tdt - \frac{V_{off}I_{off}}{t_{t,off}^2} \int_0^{t_{t,off}} t^2dt \\ &= \frac{V_{off}I_{off}}{t_{t,off}} \cdot \frac{t_{t,off}^2}{2} - \frac{V_{off}I_{off}}{t_{t,off}^2} \cdot \frac{t_{t,off}^3}{3} \\ &= \frac{V_{off}I_{off}t_{t,off}}{6}[J] \end{aligned} \tag{4.10}$$

The corresponding expression for the turn on energy will be

$$W_{on} = \frac{V_{on}I_{on}t_{t,on}}{6} \tag{4.11}$$

Using (4.10), (4.11) and the expressions presented in Table 4.3

$$W_{t,on(1)} = W_{t,on(2)} = W_{t,on(3)} = \frac{5 \cdot 2 \cdot \frac{5}{60} \cdot 12 \cdot 10^{-9}}{6} \approx 1.7nJ \tag{4.12}$$

$$W_{t,off(1)} = \frac{15 \cdot 4 \cdot \frac{5}{60} \cdot 3 \cdot 10^{-9}}{6} \approx 2.5nJ \tag{4.13}$$

$$W_{t,off(2)} = \frac{20 \cdot 6 \cdot \frac{5}{60} \cdot 3 \cdot 10^{-9}}{6} \approx 5nJ \tag{4.14}$$

$$W_{t,off(3)} = \frac{25 \cdot 8 \cdot \frac{5}{60} \cdot 3 \cdot 10^{-9}}{6} \approx 8.3nJ \tag{4.15}$$

Based on the modulation presented presented in Figure 4.3 and (4.4) the fundamental modulation frequency will be

$$f_{f,m} = \frac{1}{24 \cdot 66 \cdot 10^{-9}} \approx 630kHz \tag{4.16}$$

Using (4.6) the switching losses become

$$P_{sw} = (3 \cdot 1.7nJ + 2.5nJ + 5nJ + 8.3nJ) \cdot f_m \approx 13.2mW \tag{4.17}$$

Based on Figure 2.4 it is possible to realize that each continued modulation cycle of multiple length of $2t_d$ will result in a step wise increase in the switch current of $2 \cdot \frac{V_{in}}{Z_0}$. These current steps are indicated in Figure 2.4. It is possible to see that

$$I_x = 2 \cdot x \cdot \frac{V_{in}}{Z_0} \tag{4.18}$$

Based on Figure 4.3, and based on (4.5) and (4.18) the conduction losses for the modulation cycle of length $24t_d$ can be calculated as

$$\begin{aligned} P_{on} &= \frac{6t_d}{24t_d}I_1^2R_{ds,on} + \frac{6t_d}{24t_d}I_2^2R_{ds,on} + \frac{4t_d}{24t_d}I_3^2R_{ds,on} + \frac{2t_d}{24t_d}I_4^2R_{ds,on} \\ &= \frac{1}{24}\left(6(2 \cdot \frac{5}{60})^2 + 6(4 \cdot \frac{5}{60})^2 + 4(6 \cdot \frac{5}{60})^2 + 2(8 \cdot \frac{5}{60})^2\right) 15.8 \cdot 10^{-3} \\ &\approx 1.8mW \end{aligned} \tag{4.19}$$

Hence the total power dissipation in the switch is

$$P_{tot} = 1.8mW + 13.2mW = 15mW \tag{4.20}$$

The transistor is supposed to be mounted on a printed circuit board (PCB). According to the datasheet of the transistor the relevant thermal resistance, $R_{\Theta JA}$, for PCB mounting is stated to be maximum $\frac{40^\circ C}{W}$. The maximum allowable junction temperature is stated to be $175^\circ C$. Hence the maximal tolerated power dissipation is

$$P_{max} = \frac{T_{max} - T_A}{R_{\Theta JA}} = \frac{175 - 25}{40} = 3.75W \tag{4.21}$$

which indicates that the switch is operated with a large thermal marginal.

4.2 Simulations of EA

4.2.1 Simulation Setup

LTspice is a free simulation tool developed by Linear Technology. Before reconfiguring the PCB, LTspice was used in order to study the performance of the EA circuit. Figure 4.6 is depicting the circuit that was used in the simulations.

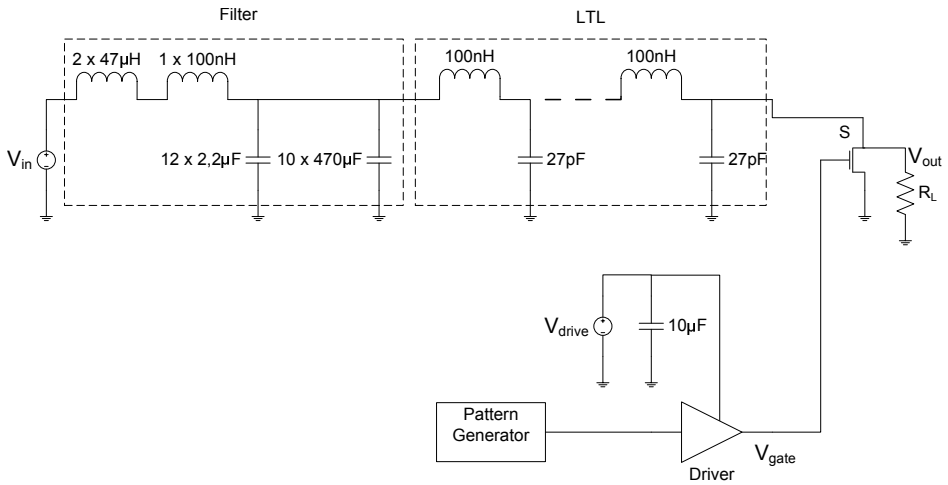

Fig. 4.6 Principal circuit of the EA used in LTspice software.

The EA was simulated with all its components, with the exception of an isolator circuit which in reality is placed between the drive circuit and the external pattern generator. A list of the components can be seen in Table 4.4. Models of the switch and the drive circuit were retrieved from the manufacture's homepages. All passive elements contain parasitic properties. The input voltage, V_{in}, was set to $5V$ and the supply voltage of the driver, V_{drive} was set to $6V$. In the simulations both t_{on} and t_{off} will be expressed in proportions to t_d. In the simulations $t_d = 66ns$, as in the theoretical case. The load connected at the end of the LTL has a value that theoretically would give match, namely 60.86Ω.

Table 4.4 contains the components used in the LTspice simulations as well as on the physical EA circuit.

Table 4.4: Component list for the LTspice simulations.

InputFilter
$L = 47\mu H$, Manufacturer: Vishay, Product number: IHLP-6767GZ-11, $DCR = 40.7m\Omega$, $C_p = 958pF$
$L = 100nH$, Manufacturer: Coilcraft, Product number: SLC7530S-101ML, $DCR = 0.123m\Omega$, $C_p = 18fF$
$C = 2.2\mu F$, Manufacturer: Murata, Product number: GRM32ER72A225K, $ESR = 0.007\Omega$, $ESL = 0.98nH$
$C = 470\mu F$, Manufacturer: NIPPON, Product number: EMVY630ADA471MLH0S, $ESR = 0.024m\Omega$, $ESL = 7nH$
LTL
$L = 100nH$, Manufacturer: Coilcraft, Product number: SLC7530S-101ML, $DCR = 0.123m\Omega$, $C_p = 18fF$
$C = 27pF$, Manufacturer: Murata, Product number: GRM1555C1H270JA01D, $ESR = 0.787\Omega$, $ESL = 0.48nH$
Switch
Manufacturer: International Rectifier, Product number: IRFS3806PbF
Driver
Driver: Maxim, MAX5048A
$C = 10\mu F$, Manufacturer: Murata, Product number: GRM32DR71E106K, $ESR = 0.023\Omega$, $ESL = 0.44nH$

4.2.2 Simulation Results

Pulse Shapes

In Figure 4.7 V_{out} and V_{gate} are plotted after simulating a pulse sequence where $V_{out} = 15V$, $20V$ and $25V$, subsequently. V_{gate} is plotted with a 30 volt bias and is submitted to clarify the modulation pattern. The modulation starts after $2t_d$ and after that, V_{gate} receives the following pattern: $t_{on} = 4t_d, t_{off} = 2.1t_d, t_{on} = 6t_d, t_{off} = 2.1t_d, t_{on} = 8t_d, t_{off} = 2t_d$.

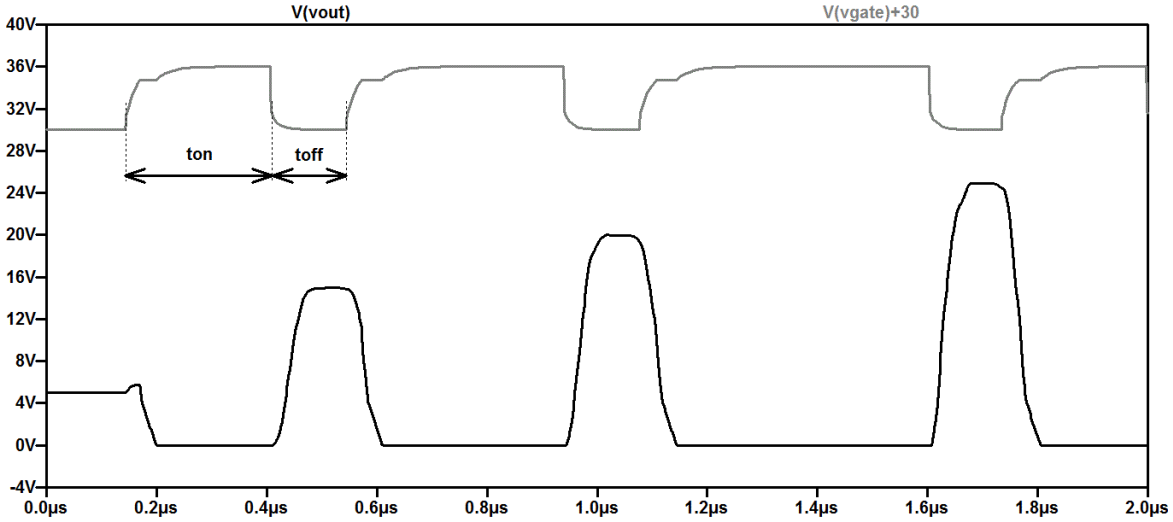

Fig. 4.7 Grey curve indicating V_{gate} and black curve indicating V_{out} for a modulation cycle where $V_{out} = 15V$, $20V$ and $25V$, subsequently.

Figure 4.8 contains subplots showing an zoomed view of the same pulses that was generated in Figure 4.7. Each subplot has drawings that indicates voltage level, rise time and fall time. Rise and fall time is measured as the time between 10% and 90% of the final voltage level.

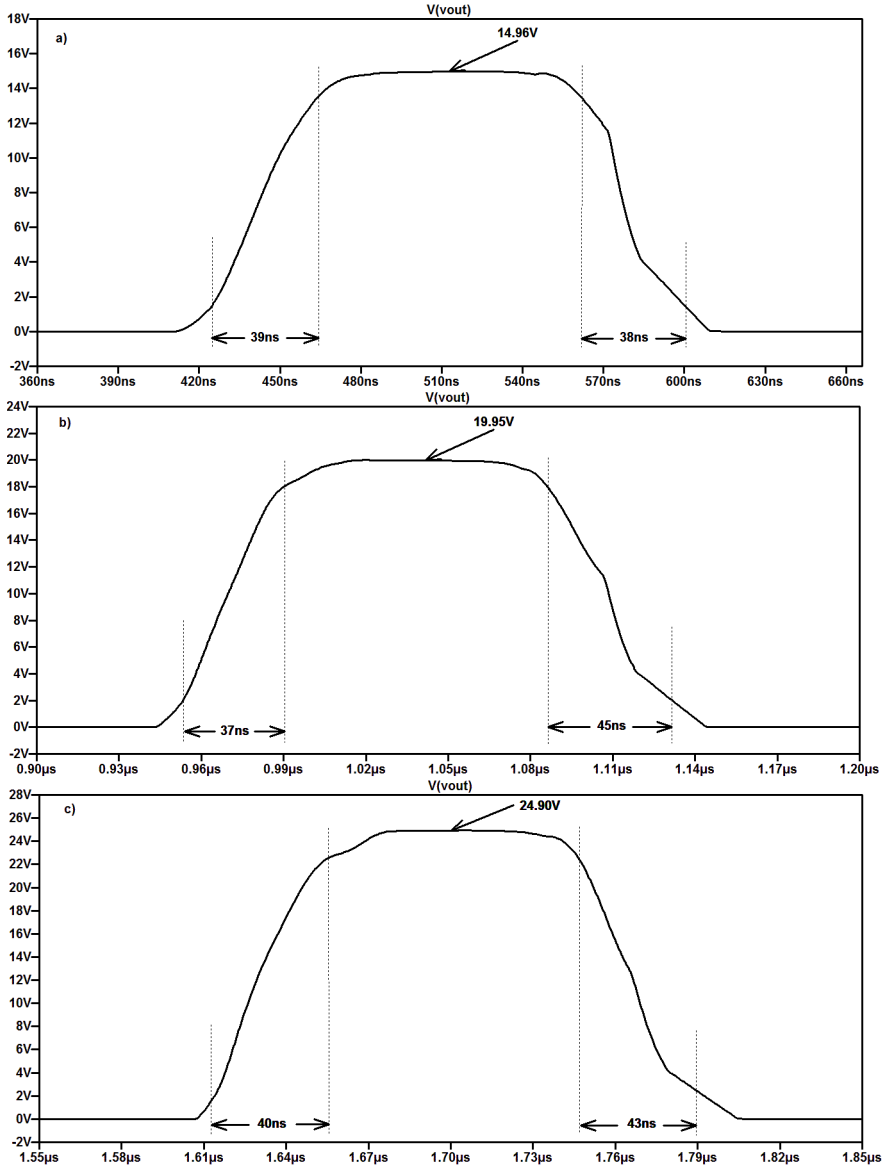

Fig. 4.8 a), b) and c) displays the separate voltage pulses that was generated in Figure 4.7.

Figure 4.9 depicts V_{out} for three sequences of the same V_{gate} pattern as in Figure 4.7. After the first sequence the pulses get an unwanted ripple on top of the pulses.

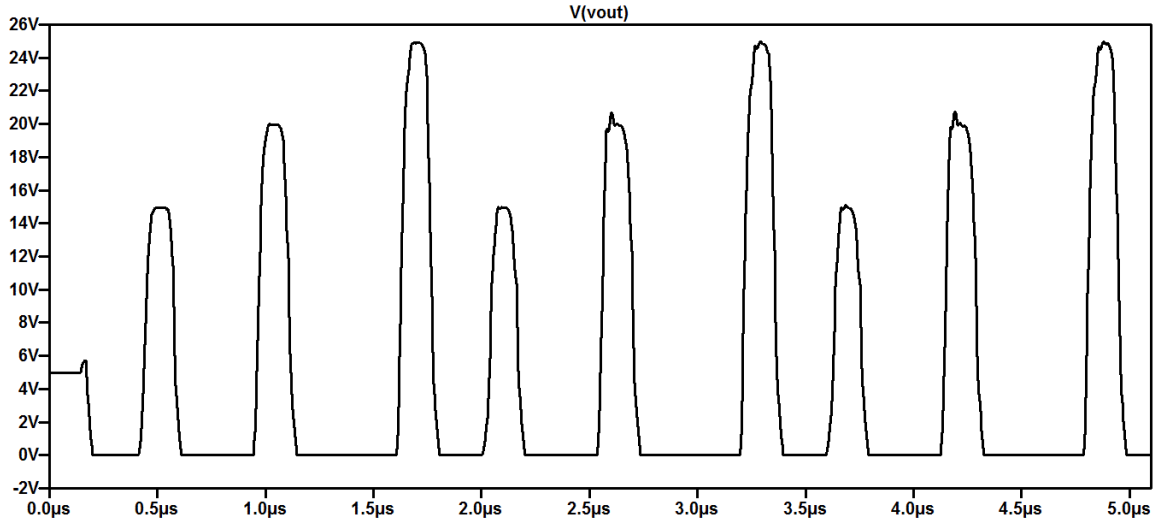

Fig. 4.9 V_{out} for three sequences of the same V_{gate} pattern as in Figure 4.7.

Figure 4.10 visualizes the simulation result for V_{out} when accumulating a pulse train where $V_{out} = 15V$. The pattern follows $t_{on} = 4t_d$, $t_{off} = 2.1t_d$.

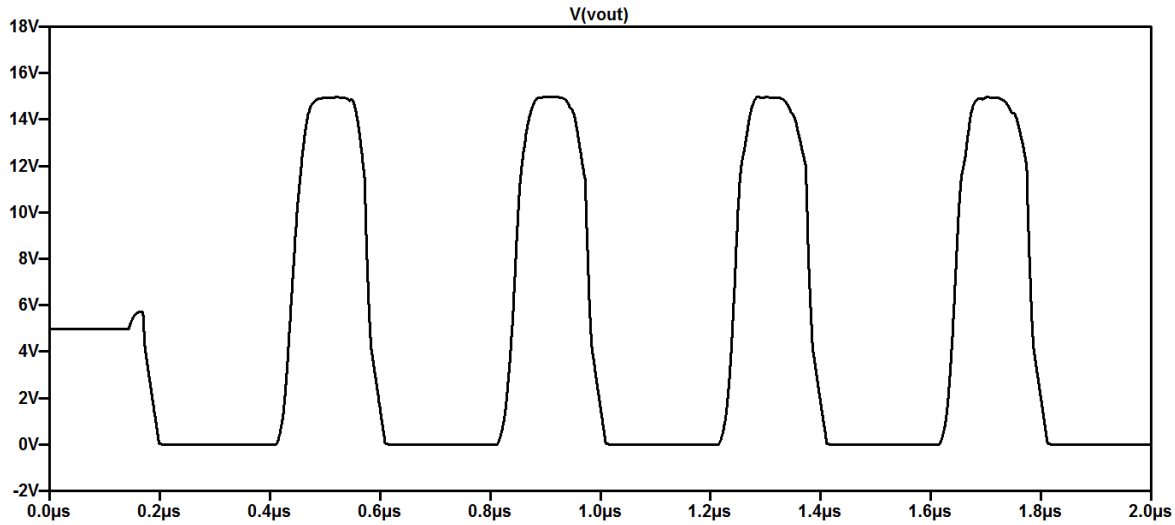

Fig. 4.10 Pulse train where $V_{out} = 15V$.

Figure 4.11 depicts the simulated transistor voltage and current at turn off.

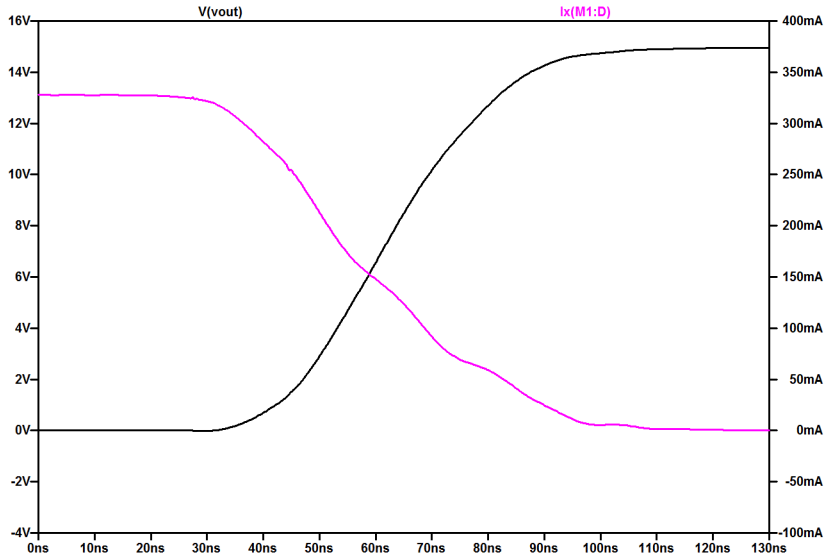

Fig. 4.11 Transistor voltage (black) and current (pink) during turn off.

Figure 4.12 depicts the simulated transistor voltage and current at turn on.

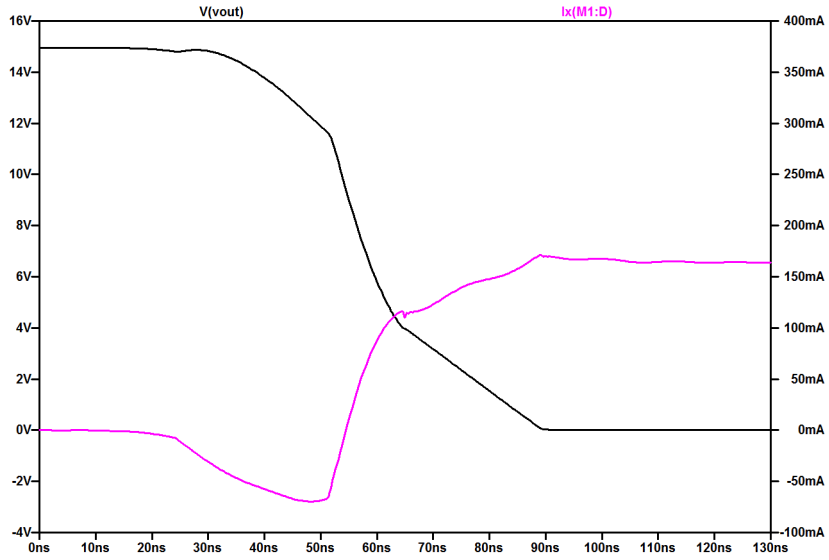

Fig. 4.12 Transistor voltage (black) and current (pink) during turn on.

Note that the wave forms in Figure 4.11 and Figure 4.12 can be compared to the assumed wave forms in Figures 4.4-4.5.

Efficiency Simulations for matched load

In LTspice the power consumption of different elements in the EA were simulated as well as the overall efficiency.

The efficiency measurement was made over the modulation cycle presented in Figure 4.13.

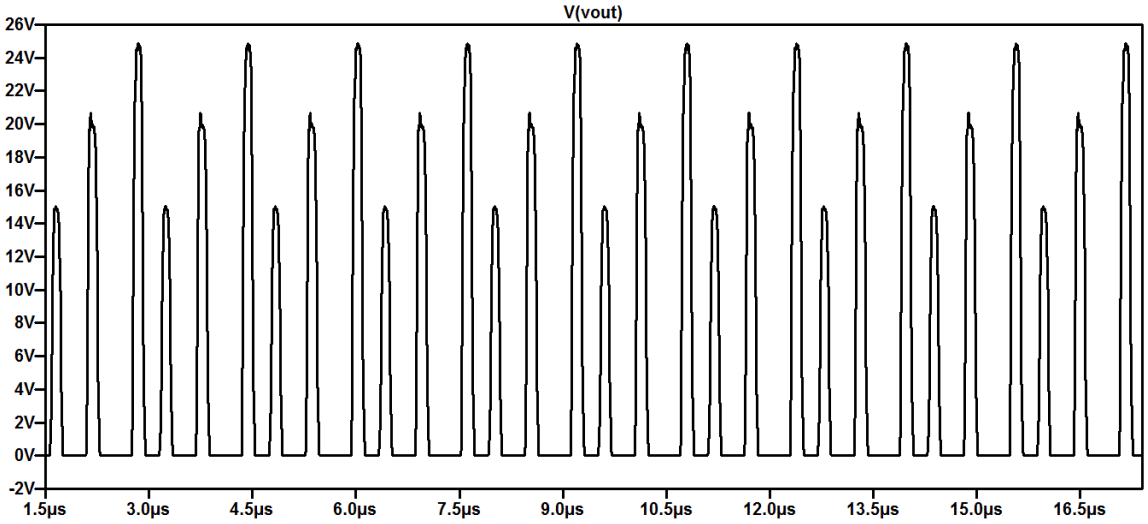

Fig. 4.13 Modulation cycle window used for the efficiency simulations.

The result is summarized in Table 4.5.

Table 4.5: Summary of LTspice simulations for the modulation cycle presented in Figure 4.13.

$\mathbf{P_{dc}}$	$\mathbf{P_{drive}}$	$\mathbf{P_{load}}$	$\mathbf{P_{T,ds}}$	$\mathbf{P_{T,gate}}$	$\mathbf{P_{drive,loss}}$	$\mathbf{P_{LTL}}$	$\mathbf{P_{filter}}$	**Efficiency** $\left(\frac{100 \cdot P_{load}}{P_{dc}+P_{drive}}\right)$	**Power stage efficiency** $\left(100 \cdot \frac{P_{load}}{P_{dc}}\right)$
$1.549W$	$0.161W$	$1.477W$	$0.062W$	$0.087W$	$0.074W$	$0.003W$	$0.009W$	86.4%	95.4%

In Table 4.5 $P_{T,ds}$ is the drain losses of the transistor: the conduction and switching losses except the gate losses. Note that $P_{T,ds} = 0.062W$ is somewhat larger than what was calculated in (4.20).

Table 4.6 displays the losses from the LTspice simulations in Figure 4.13 relative to the total power losses.

Table 4.6: Relative loss distribution for the LTspice simulations of the modulation cycle presented in Figure 4.13. The values are relative to the total loss.

$\mathbf{P_{T,ds}}$	$\mathbf{P_{T,gate}}$	$\mathbf{P_{drive,loss}}$	$\mathbf{P_{LTL}}$	$\mathbf{P_{filter}}$
26.4%	37%	31.5%	1.3%	3.8%

Note that the LTL losses are relatively small.

Simulation of EA connected to the STI Circuit Model

In Figure 4.14 a pulse pattern of 15V, 20V and 25V is fed to the circuit model of the ST shown in Figure 3.7.

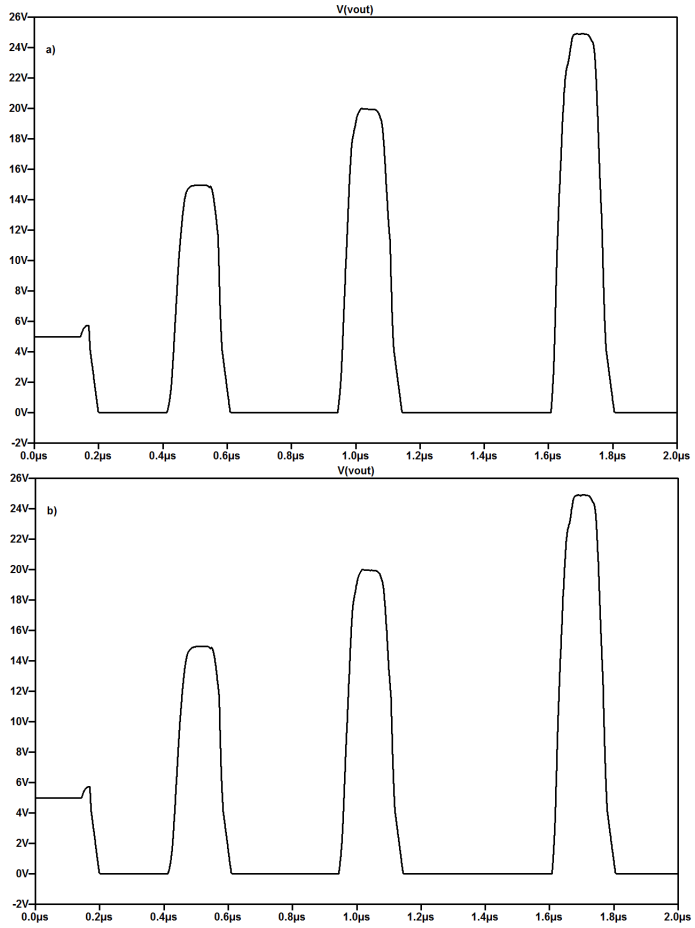

Fig. 4.14 a): V_{out} for a matched resistive load. b): V_{out} when the EA is feeding the circuit model shown in Figure 3.7

For comparison Figure 4.14a depicts V_{out} for a matched load. Figure 4.14b depicts V_{out} when the STI circuit model is the load. In the STI model the reactive component values were taken from the physical PA. This means that $L = 8nH$, $C_{out} = 5pF$ and $C_{in} = 10pF$, see Figure 3.7.

4.2.3 Simulation Analysis

The pulse shapes had the best shape when t_{on} was equal to the theoretical, calculated time. This indicates that the delay of the simulated LTL relates well to what was calculated theoretically. The voltages in the simulation, 14.96V, 19.95V and 24.9V, are close to the expected values: 15V, 20V and 25V, respectively. This indicates that the theoretical value for load match also gives a good match in the simulations. Consider a pulse train: ideally a pulse should not be affected by the previous ones, with the assumption of a matched load. This is however complicated to achieve when the generated pulses do not have sharp flanks, see Figure 4.8. The problem gets even worse when subsequent pulses have different magnitude. The reason for the ripple in Figure 4.9 at $t > 2.5\mu s$ could stem from poor timing in t_{on} and t_{off} but also, or maybe in combination, with some triggered resonance between the many L and C elements in the circuit. If a pulse train of equal magnitude is created, the ripple seen in Figure 4.9 is not present. However, the pulses are still somewhat affected by the former ones, as can be seen in Figure 4.10. The performance of a pulse train of 20V and 25V was similar. In general, based on the simulations of the EA, the quality of the generated pulses was considered adequate with respect to the purpose of the project.

As can be seen in Figure 4.14, the difference between Figure 4.14a and Figure 4.14b is very small. This would indicate that at least the known physical reactive components in the STI model in Figure 3.7 do not pose any problems regarding the pulse quality of the supply voltage, during an integration.

Based on the simulation results it is considered that the principle behaviour of the wave forms in Figures 4.11-4.12, in essence confirm the corresponding assumed wave forms in Figures 4.4-4.5; at least in the turn off case is the correlation considered good. However, as can be seen in Figures 4.11-4.12 the transition

times is larger than the corresponding assumed values in Figures 4.11-4.12. However, the explanation is probably due to that the assumptions of (4.7), $t_{t,on} = t_{r,g}$ and $t_{t,off} = t_{f,g}$, in Section 4.1.2, implies a too great simplification of reality. The larger transition times in the simulation could explain why the simulated transistor losses were 4 times higher than the estimated value, see (4.20).

Otherwise, the overall efficiency in Table 4.5 is similar to what was measured in [13].

Chapter 5

Verification of EA

This Chapter aims at presenting and analyzing the results obtained from the verification of the EA performance. Section 5.1, contains derived theory which have been used in the verification process. Section 5.2 summarizes the instruments which have been used. At the end of Chapter 5 it is described how the integration was proceeded.

5.1 Supporting Theory used in Verification

5.1.1 Detecting Mismatch from Constant Voltage Pulse Train

The theory derived in this Section explains how a pulse train of constant magnitude is affected for a resistive mismatched load. The conclusions from the theory is visualized in Figure 5.1. The theory is based on the assumptions that

- the switch is on for exactly some multiple $2t_d$-duration, and at least one $2t_d$-duration
- the switch is off for exactly $2t_d$.
- the same modulation scheme is constantly repeated
- the TL is ideal

Consider Figure 2.3. Let n denote the number of multiple $2t_d$ storage periods and $\Gamma_{L,m}$ the load reflection coefficient for a general mismatched load. Then $V_{nom} = n \cdot V_{in}$ where V_{nom} is the output voltage for a matched load. After one storage period the pulse meets the mismatched load $\Gamma_{L,m}$ and the output voltage will be $V_{out} = V_{nom}(1 + \Gamma_{L,m})$. The corresponding reflected wave will be $R_1 = V_{nom} \cdot \Gamma_{L,m}$. If $t_{drain,0}$ denotes where the drainage period starts then during $t \in (t_{drain,0}, t_{drain,0} + 2t_d)$ the reflected wave will travel towards the source side, at $t = t_{drain,0} + t_d$ meet $\Gamma_S = -1$, and travel back to the switch/load at $t = t_{drain,0} + 2t_d$. Since the modulation scheme is of multiple $2t_d$-length and since $\Gamma_S = \Gamma_L = -1$ during the storage period, the reflected wave will repeatedly travel back and forth in the LTL and change sign at every bounce, b. For each $2t_d$ modulation scheme the reflected wave will bounce 2 times in the LTL. Hence, the total number of bounces starting from $t_{drain,0} < t < (t_{drain,0} + t_d)$ will be $b = 1 + 2 \cdot n$. Let $\hat{R}_k$ denote the reflected wave immediately before it meets the load at the end of the storage period. Then

$$\hat{R}_k = (-1)^b \cdot R_{k-1} = (-1)^{2 \cdot n+1} \cdot R_{k-1} = -R_{k-1} \tag{5.1}$$

where k is the number of reflections that have been created in the modulation process. The output voltage, created at each drainage state where $k \geq 2$, can be seen as a sum of two terms. The first term, $V_{nom}(1 + \Gamma_{L,m})$, is always present and is due to the main output voltage pulse. The second term is maintained by the previous reflection, which has been kept inside the LTL. The second terms contribution in V_{out} is according to (5.1) $-R_{k-1}(1 + \Gamma_{L,m})$. Hence

$$V_{out,k} = \begin{cases} V_{nom}(1 + \Gamma_{L,m}) & \text{if } k = 1, \\ V_{nom}(1 + \Gamma_{L,m}) + (-R_{k-1})(1 + \Gamma_{L,m}) & \text{if } k \geq 2. \end{cases} \tag{5.2}$$

From (5.2) it is possible to distinguish a general expression for the reflected waves created in the modulation process.

$$R_k = \begin{cases} V_{nom}\Gamma_{L,m} & \text{if } k = 1, \\ V_{nom}\Gamma_{L,m} + (-R_{k-1})\Gamma_{L,m} & \text{if } k \geq 2. \end{cases} \tag{5.3}$$

Assuming some $k \geq 2$ and evaluating R_k:

$$\begin{aligned} R_k &= V_{nom}\Gamma_{L,m} - \Gamma_{L,m}R_{k-1} = V_{nom}\Gamma_{L,m} - \Gamma_{L,m}(V_{nom}\Gamma_{L,m} - \Gamma_{L,m}R_{k-2}) \\ &= V_{nom}\Gamma_{L,m} - \Gamma_{L,m}\left(V_{nom}\Gamma_{L,m} - \Gamma_{L,m}(V_{nom}\Gamma_{L,m} - \Gamma_{L,m}R_{k-3})\right) \\ &= V_{nom}\Gamma_{L,m} - \Gamma_{L,m}(V_{nom}\Gamma_{L,m} - V_{nom}\Gamma_{L,m}^2 + \Gamma_{L,m}^2 R_{k-3}) \\ &= V_{nom}\Gamma_{L,m} - V_{nom}\Gamma_{L,m}^2 + V_{nom}\Gamma_{L,m}^3 - \Gamma_{L,m}^3 R_{k-3} \\ &= V_{nom}\Gamma_{L,m} - V_{nom}\Gamma_{L,m}^2 + V_{nom}\Gamma_{L,m}^3 - \Gamma_{L,m}^3(V_{nom}\Gamma_{L,m} - \Gamma_{L,m}R_{k-4}) \\ &= V_{nom}\Gamma_{L,m} - V_{nom}\Gamma_{L,m}^2 + V_{nom}\Gamma_{L,m}^3 - V_{nom}\Gamma_{L,m}^4 + ... + (-1)^{k-1}V_{nom}\Gamma_{L,m}^k \\ &= V_{nom}\sum_{i=1}^{k}(-1)^{i-1}\Gamma_{L,m}^i \end{aligned} \tag{5.4}$$

Consequently in (5.2)

$$R_{k-1} = V_{nom}\sum_{k=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i \tag{5.5}$$

With the help of the result in (5.5) a general expression for V_{out} can be derived omitting the otherwise recursive behaviour in (5.2). In (5.2) the term $V_{nom}(1 + \Gamma_{L,m})$ will always be present regardless the size of k. The other term, $(-R_{k-1})(1 + \Gamma_{L,m})$ will however expand recursively depending on the size of k. Equation (5.4) is a sum of powers in $\Gamma_{L,m}$ where the sign of each term changes. Multiplying $\Gamma_{L,m}$ with (5.4) creates a new sum which in some sense is very similar to (5.4) except that the term containing $\Gamma_{L,m}$ is missing, all signs are changed and that a new last term has occurred:

$$\Gamma_{L,m} \cdot V_{nom}\sum_{i=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i = V_{nom}\left(-\left(\sum_{i=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i - \Gamma_{L,m}\right) + (-1)^k\Gamma_{L,m}^k\right) \tag{5.6}$$

Consequently

$$\begin{aligned} &(1 + \Gamma_{L,m}) \cdot V_{nom}\sum_{i=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i \\ &= V_{nom}\left(\sum_{i=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i - \left(\sum_{i=1}^{k-1}(-1)^{i-1}\Gamma_{L,m}^i - \Gamma_{L,m}\right) + (-1)^k\Gamma_{L,m}^k\right) \\ &= V_{nom}\left(\Gamma_{L,m} + (-1)^k\Gamma_{L,m}^k\right) \end{aligned} \tag{5.7}$$

Hence in (5.2)

$$\begin{aligned} V_{out,k} &= V_{nom}\left(1 + \Gamma_{L,m} - (\Gamma_{L,m} + (-1)^k\Gamma_{L,m}^k)\right) \\ &= V_{nom}(1 - (-1)^k\Gamma_{L,m}^k) \end{aligned} \tag{5.8}$$

The interpretation of (5.8) is that for a matched load

$$V_{out,1} = V_{out,2} = V_{out,3} = ... = V_{out,k} = V_{nom} \tag{5.9}$$

while for a mismatched load

$$V_{out,k} = \begin{cases} V_{nom}(1 - (-1)\Gamma_{L,m}^1) & \text{if } k = 1, \\ V_{nom}(1 - \Gamma_{L,m}^2) & \text{if } k = 2, \\ V_{nom}(1 - (-1)\Gamma_{L,m}^3) & \text{if } k = 3, \\ ... \\ ... \end{cases} \tag{5.10}$$

If ϵ_k denotes the error between V_{nom} and $V_{out,k}$ then

$$\epsilon_k = V_{nom} - V_{nom}\left(1 - (-1)^k \Gamma_{L,m}^k\right) = V_{nom} \cdot (-1)^k \Gamma_{L,m}^k \tag{5.11}$$

and

$$\lim_{k\to\infty} \epsilon_k = 0 \tag{5.12}$$

since $|\Gamma_{L,m}| < 1$ for a mismatched load.

The result in (5.8), (5.9) and (5.10) has been helpful in the laboratory measurements; due to non ideal pulse shapes in reality, it can, when judging load match, be helpful to view several subsequent V_{out} pulses rather than just one.

Figure 5.1 further demonstrates how the wave form of a pulse train feeding a load $|Z_L| > |Z_0|$ is principally expected to look like.

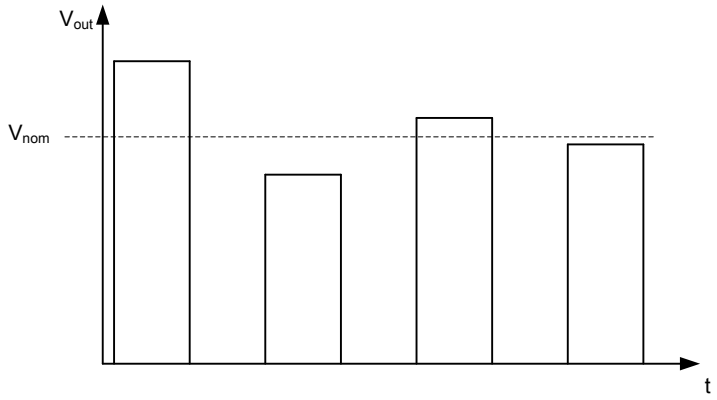

Fig. 5.1 V_{out} where a pulse train feeds a load $|Z_L| > |Z_0|$, where $Z_L \in \mathbf{R}$ and $Z_0 \in \mathbf{R}$.

Note in Figure 5.1 that $V_{out}(t)$ alternates to be larger and smaller around V_{nom}. Finally however $V_{out} = V_{nom}$.

5.1.2 Under and Over modulation

Based on the examples described in Figures 5.2 and 5.4, the pulse shape appearance will be explained when a single pulse is feeding a resistive load, if t_{on} is not a integer multiple of $2t_d$. Let $t_{on,nom} = n \cdot 2t_d$, where n is some integer. Consider the case where $t_{on} = t_{on,nom} - t_{missing}$. This case will be referred to as under modulation. Figure 5.2 is illustrating the LTL voltage for an under modulation case where $n = 2$.

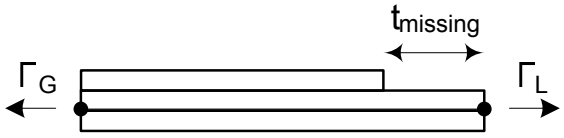

Fig. 5.2 Under modulation

Figure 5.3 depicts the principal appearance of an under modulated pulse.

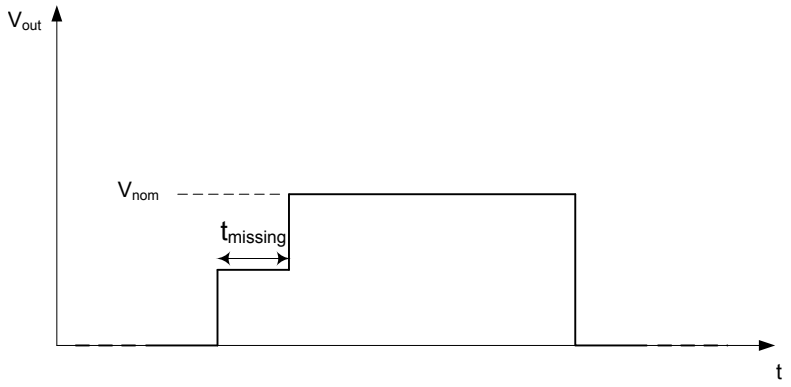

Fig. 5.3 Principal pulse shape corresponding to the under modulation in Figure 5.2.

In general V_{out} is affected as

$$\begin{cases} V_{out} = V_{in}(1 + (\frac{t_{on,nom}}{2t_d} - 1)) = V_{nom} - V_{in} & \text{if } 0 < t_{off} < t_{missing}, \\ V_{out} = V_{in}(1 + \frac{t_{on,nom}}{2t_d}) = V_{nom} & \text{if } t_{missing} < t_{off} < 2t_d. \end{cases} \tag{5.13}$$

Now consider the case where $t_{on} = t_{on,nom} + t_{exceed}$. This case will be referred to as over modulation. Figure 5.4 is illustrating the LTL voltage for an over modulation case where $n = 2$.

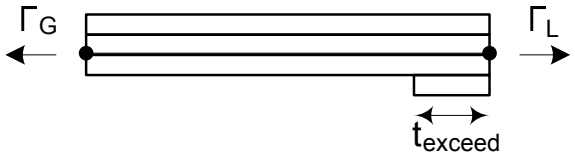

Fig. 5.4 Over modulation

Figure 5.3 depicts the principal appearance of an over modulated pulse.

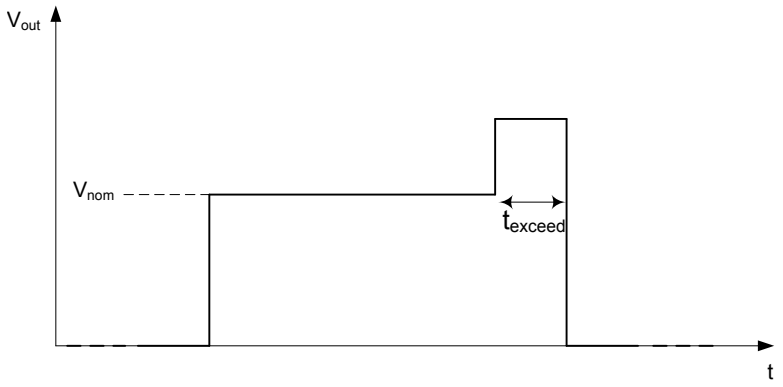

Fig. 5.5 Principal pulse shape corresponding to the over modulation in Figure 5.4.

In general V_{out} is affected as

$$\begin{cases} V_{out} = V_{in}(1 + \frac{t_{on,nom}}{2t_d}) = V_{nom} & \text{if } 0 < t_{off} < 2t_d - t_{exceed}, \\ V_{out} = V_{in}(1 + (\frac{t_{on,nom}}{2t_d} + 1)) = V_{nom} + V_{in} & \text{if } 2t_d - t_{exceed} < t_{off} < 2t_d. \end{cases} \tag{5.14}$$

The theory of under and over modulation has been helpful when tuning pulse shapes in the verification measurements.

5.2 Measurement Setup

Figure 5.6 visualizes an overview of the instruments used for the EA measurements. Figure 5.7 indicates the different components on the EA circuit board.

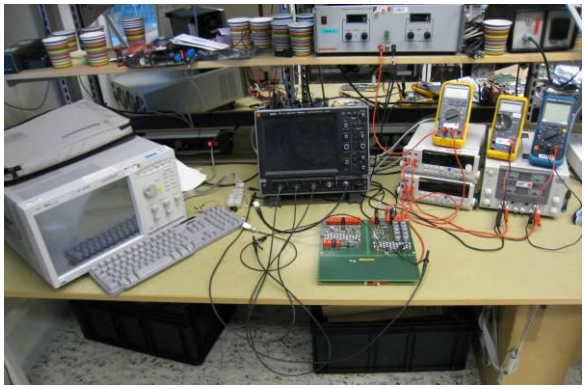

Fig. 5.6 Overview photo of the EA measurements setup.

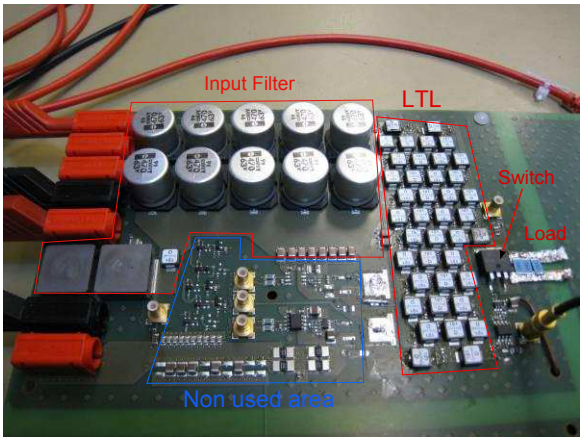

Fig. 5.7 EA with indicated Non used area (blue), LTL (red), Input Filter (red), Switch (red) and Load (red).

Table 5.1 summarizes the instruments used for the verification of the EA.

Table 5.1: Instruments used for verification record of EA.

Type	**Name**	**Function**
Logic Analysis System	Agilent 16903A	
Pattern Generator (module)	Agilent 16720A	$V_{gate}, Trigger$
Output Cable	Agilent 16522-61601	
3-state TTL / 3.3V Data Pod	Agilent 10466A	
Power Supply	Powerbox L6405	V_{in}
Power Supply	Topward 6303AS	V_{drive}, V_{iso}
Dual Display Multimeter	Fluke 45	I_{drive}
Dual Display Multimeter	Fluke 45	I_{iso}
True RMS Multimeter	Fluke 87	I_{in}
Series II Multimeter	Fluke 75	V_{iso}
True RMS Multimeter	Tektronix TX3	V_{drive}
400MHz Oscilloscope	LeCroy WaveSurfer 44MXs-A	V_{in}, I_{in}, V_{out}
DC-50MHz Current Probe	LeCroy AP015	
500MHz Probe	LeCroy PP005A	
500MHz Probe	LeCroy PP009	
Coaxial cable 50Ω	RG174 SMB-BNC	

Table 5.2 compiles the instruments used for the LTL measurements.

Table 5.2: Instruments used for verification measurements on LTL.

Type	**Name**
Series Network Analyzer	Agilent Technologies E5061B ENA
Cable	PhaseFlex, W.L. Gore, 3GW40
Cable	FA147A0010M2020, BUA01H 0146

5.3 Measurement Results & Analysis

Measurements of the EA performance revealed that the behaviour was not what would have been expected from theory and simulations. This Section contains both a summary of the performance/problems of the physical EA as well as a corresponding analysis. In the EA measurements $V_{in} = 5V$, $V_{drive} = 6V$ and $V_{iso} = 3.3V$.

5.3.1 Delay

Accumulating pulses, using the theoretical time of t_{on}, i.e multiples of $2 \cdot 66ns = 132ns$, did create poor pulse shapes. Figure 5.8 reveals the result of V_{out} when trying to create a 15V pulse, where $t_{on} = 4 \cdot 66ns = 264ns$ and $Z_L = 61\Omega$.

Fig. 5.8 V_{out} versus time where $t_{on} = 4 \cdot 66ns = 264ns$ and $Z_L = 61\Omega$.

Since the modulation in Figure 5.8 only creates a single pulse, V_{out} should reach V_{in} after dissipating the stored energy over the load. In Figure 5.8, at the beginning of the drainage state, V_{out} is less than the nominal voltage. Based on the theory in Section 5.1, the shape of the pulse indicates under modulation.

What further on can be seen in Figure 5.8 is that V_{out} reaches a level larger than 15V and that it does not reach 5V immediately after the drainage state. Both these observations suggest that a reflection has been created during the dissipation of the pulse. Another discrepancy is that V_{out} is slightly negative during the storage state - around -0.3V. There is also a negative spike of -3V at the beginning of the drainage state.

Concentrating on the delay time, Figure 5.9 depicts the measurement of the voltage at the middle of the LTL, V_{LTL}, and V_{out} when trying to create a 25V pulse. In Figure 5.9 $t_{on} = 8 \cdot 66ns = 528ns$.

Fig. 5.9 C1: Voltage at the middle of the LTL. C2: V_{out} when trying to create a 25V pulse when $Z_L = 61\Omega$.

Figure 5.10 displays only V_{LTL} from the same measurement as in Figure 5.9.

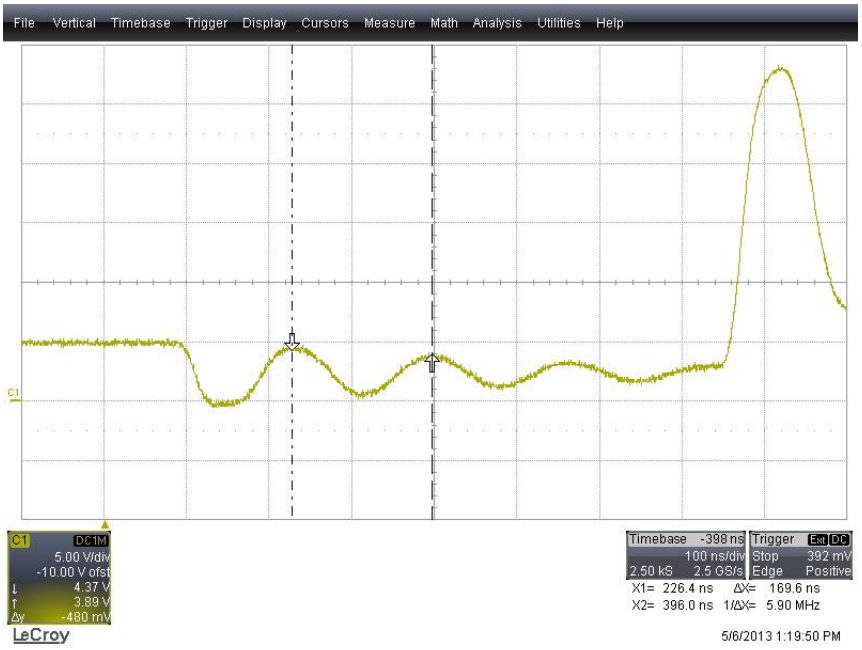

Fig. 5.10 Voltage at the middle of the LTL for the same modulation pattern as in Figure 5.9. $Z_L = 61\Omega$.

Consider Figure 2.3 in Section 2.1: if the accumulations were to continue for some time, the voltage seen at the middle of the LTL would alternate between zero and V_{in}. The alternation would occur every t_d. Hence, the time between two equal peaks in the middle of the LTL would measure $2t_d$. The time between to peaks in Figure 5.10, indicated with cursors, are measured to be around 170ns, which is 2.57 times the theoretical value of t_d. This further indicates that the accumulation time for generating a 15V pulse is too short.

Figure 5.11 shows the simulated voltage at the middle of the LTL when creating a 25V pulse. The time between two equal peaks are measured to be $2 \cdot 66ns = 132ns$. What also can be seen is that the pulses in Figure 5.11 do not have the attenuated behavior that can be seen from the measurement in Figure 5.10. Further on the pulses in Figure 5.11 are more ideally square shaped than in Figure 5.10.

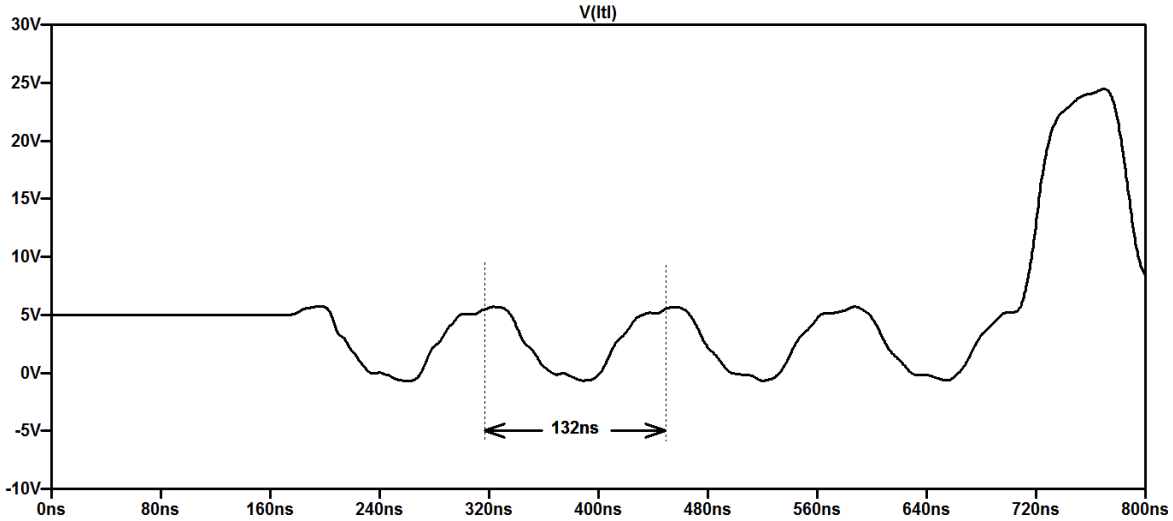

Fig. 5.11 Simulated voltage at the middle of the LTL. The cursor indicates the theoretical value of $2t_d$. $Z_L = 61\Omega$.

5.3.2 Mismatch

With the knowledge that the real t_d is not the same as theoretical one, and the knowledge of how a pulse will look like if it is under or over modulated, see Section 5.1.2, the 15V pulse was again generated but with a new tuned $t_{on} = 4.4 \cdot 66ns = 290ns$. By observations $t_{on} = 4.4 \cdot 66ns = 290ns$ seemed to generate the best pulse shape.

Figure 5.12 depicts the measurement of V_{out} when $t_{on} = 4.4 \cdot 66ns = 290ns$.

Fig. 5.12 V_{out} versus time where $t_{on} = 4.4 \cdot 66ns = 290ns$, $Z_L = 61\Omega$.

The pulse shape in Figure 5.12 is somewhat improved compared to the case in Figure 5.8. Still there are some non idealities. The peak value of the pulse is 1.7V higher than 15V, which indicates a mismatch between Z_0 and Z_L. From the theory of reflection coefficients, it seems like $|Z_0| < |Z_L|$. To further verify this suspicion, a pulse train was generated.

Figure 5.13 visualizes the measurement of V_{out} when creating a pulse train of the pattern where $t_{on} = 4.4 \cdot 66ns = 290ns$ and $t_{off} = 3.54 \cdot 66ns = 234ns$.

Based on the theory of how a pulse train of constant magnitude is affected of mismatch in Section 5.1, see Figure 5.1, the behavior of the three pulses indicates a mismatch where $|Z_0| < |Z_L|$.

Fig. 5.13 Pulse train of V_{out} versus time, where $t_{on} = 4.4 \cdot 66ns = 290ns$, $t_{off} = 3.54 \cdot 66ns = 234ns$ and $Z_L = 61\Omega$.

New measurement results, with the same patterns as in Figures 5.12 and 5.13, where the load is changed to 50Ω, can be seen in Figure 5.14 and Figure 5.15, respectively.

Fig. 5.14 V_{out} versus time where $t_{on} = 4.4 \cdot 66ns = 290ns$ and $Z_L = 50\Omega$.

Fig. 5.15 V_{out} versus time where $t_{on} = 4.4 \cdot 66ns = 290ns$, $t_{off} = 3.54 \cdot 66ns = 234ns$ and $Z_L = 50\Omega$.

The voltage shapes of the three pulses in Figure 5.15 are still indicating that there might be some mismatch. However, the interesting thing is that the pulses are much closer to 15V than in Figure 5.13, where the load was the same as the theoretical value, 61Ω.

5.3.3 LTL

Based on the verification measurements of the EA, it was considered that the delay was longer and the characteristic impedance was smaller than their respective theoretical values. To investigate the underlying reason, measurements on the LTL was conducted.

In the LTL measurements, a network analyzer was used to obtain a two port representation of the LTL, see Figure 5.16.

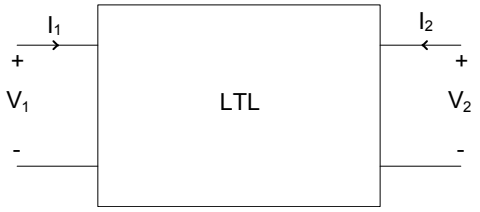

Fig. 5.16 Principal two port representation of the LTL.

From the two port measurements, the Y parameters were obtained:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5.15}$$

The two port representation in (5.15) were reformulated as a Π net, see Figure 5.17.

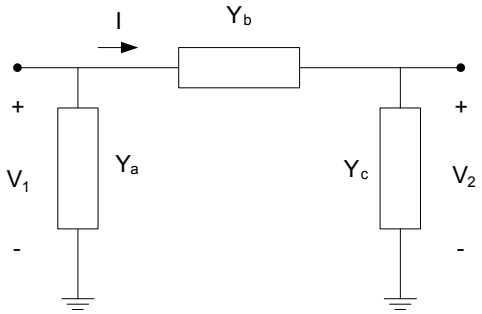

Fig. 5.17 Π net model of the LTL. At port 2 a load were attached, see (5.16) and (5.17).

where

$$\begin{cases} Y_a = Y_{11} + Y_{12} \\ Y_b = -Y_{12} \\ Y_c = Y_{22} + Y_{12} + Y_L \end{cases} \tag{5.16}$$

and

$$Y_L = \frac{1}{Z_L} = \frac{1}{60.9\Omega} \tag{5.17}$$

is a load admittance added in the software after the measurements.

Based on Figure 5.17 and (5.16),

$$\begin{cases} I = V_2 \cdot Y_c \\ I = V_1 \cdot Y_b // Y_c \end{cases} \Rightarrow \frac{V_2}{V_1} = \frac{Y_b // Y_c}{Y_c} = \frac{Y_b}{Y_b + Y_c} \tag{5.18}$$

The delay were then calculated as

$$\theta = \angle \frac{Y_b}{Y_b + Y_c} \Rightarrow delay = \frac{\theta}{\omega} \tag{5.19}$$

Figure 5.18 shows the LTL delay from measurements together with the simulated LTL delay. In the simulation, a model of 40 LC sections were used including stray capacitances and stray inductances.

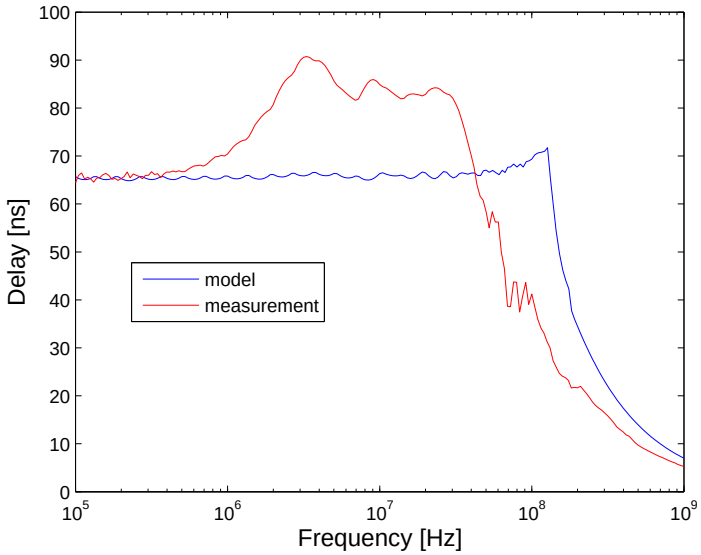

Fig. 5.18 Measured LTL delay and simulated LTL model delay.

In Figure 5.18 the delay is a measure of the time each sinusoidal component takes to travel along the LTL. The most interesting frequencies are the ones equal to the fundamentals of pulse trains of 15V, 20V

and 25V: theoretically $2.5MHz, 1.9MHz$ and $1.5MHz$, respectively. At these frequencies the difference between model and measurements is large.

With the help of (5.16) the input impedance of the LTL, Z_{in}, can be calculated as

$$Z_{in} = \frac{1}{Y_{in}} = \frac{1}{Y_a + Y_b//Y_c} \tag{5.20}$$

Figure 5.19 depicts the measured and simulated $|Z_{in}(\frac{\omega}{2\pi})|$ of the LTL.

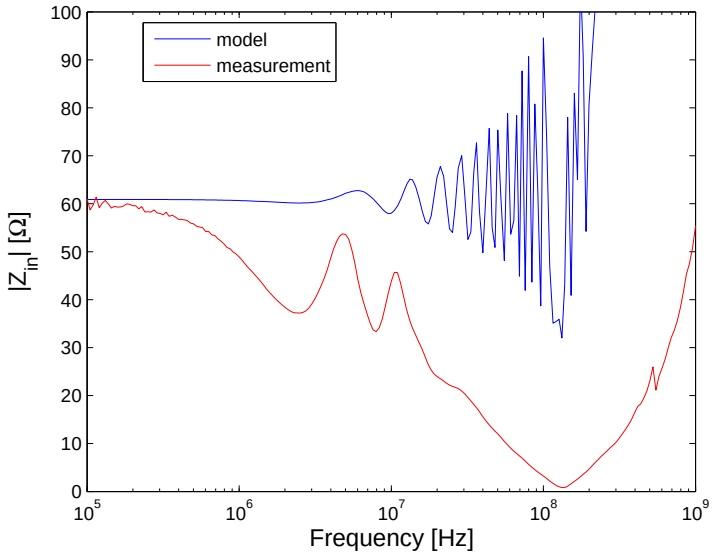

Fig. 5.19 Measured $|Z_{in}(\frac{\omega}{2\pi})|$ of the LTL and simulated $|Z_{in}(\frac{\omega}{2\pi})|$ of the LTL model.

In Figure 5.19, $|Z_{in}(\frac{\omega}{2\pi})|$ is the input impedance seen into port one of the Π net in Figure 5.17. At $2.5MHz, 1.9MHz$ and $1.5MHz$ the difference between model and measurements is large.

5.3.4 Closing Analysis and Discussion of EA Performance

Ideally the delay should be constant for all frequencies up to f_{max}. According to (4.3), f_{max} is theoretically 194MHz. In Figure 5.18 it can be seen that, in the simulations t_d is more or less 66ns up to a frequency close to f_{max}. This is clearly not the case in the measurements. This confirms the suspicion made in in Section 5.3.1: the delay deviates from the theoretical value. Since the delay is different for different frequencies, it can be stated that the injected pulse shapes will not be preserved since they clearly contains harmonics. This might explain why the shape of the voltage measured in the middle of the LTL becomes more and more rounded and attenuated, see Figure 5.10.

$|Z_{in}(\frac{\omega}{2\pi})|$ is not a direct measure of Z_0 but the conclusion is still that Z_0 is not what it should be, since the measured Z_{in} does not correlate well with the simulated Z_{in}. The behavior confirms the suspicion arisen in Section 5.3.2 that Z_0 deviates from its theoretical value. Since $|Z_{in}(\frac{\omega}{2\pi})|$ is different for different frequencies corresponding to the fundamental of pulse trains of 15V, 20V and 25V, this might indicate that the voltages get different match. However, more understanding on how to translate Z_{in} into Z_0 is needed to draw this conclusion.

The reason for the discovered non idealities of the LTL is not fully investigated, but it seems likely that the behaviour occurred when the LTL capacitor value became too small, during the circuit reconfiguration. The EA performance has been proven better when higher values, $(560pF)$, of the capacitors where used. It might be that the PCB layout renders stray capacitance, which value is comparable to the LTL capacitors. The negative voltage during the accumulation phase raise additional, unanswered questions. Wether it is caused by the same origin that caused the LTL to have bad performance or wether it is caused by the transistor is uncertain.

In summary the EA performance is poor and it has been hard to obtain good pulse shapes in general. Instead of solving the problems it was decided to move on to an EA to PA integration, see Section 5.4.

5.4 Resolution

The original plan of the integration procedure was to test if load match could be obtained for voltage pulses of 15V, 20V and 25V, and a certain P_{in}, where R_{ST} would be more or less 60Ω. Since the characteristic impedance of the EA turned out to give poor match for 60Ω, the integration procedure had to be revised. Based on the result from the EA measurements, match seems to occur at less than 50Ω. Therefore, by considering Figure 3.15 it would not be possible to generate pulses of 15V, 20V and 25V while accomplish load match during an integration. Measurements showed that when generating a 10V pulse, the EA seemed to give good match around 48Ω, see Figures 5.20 and 5.21.

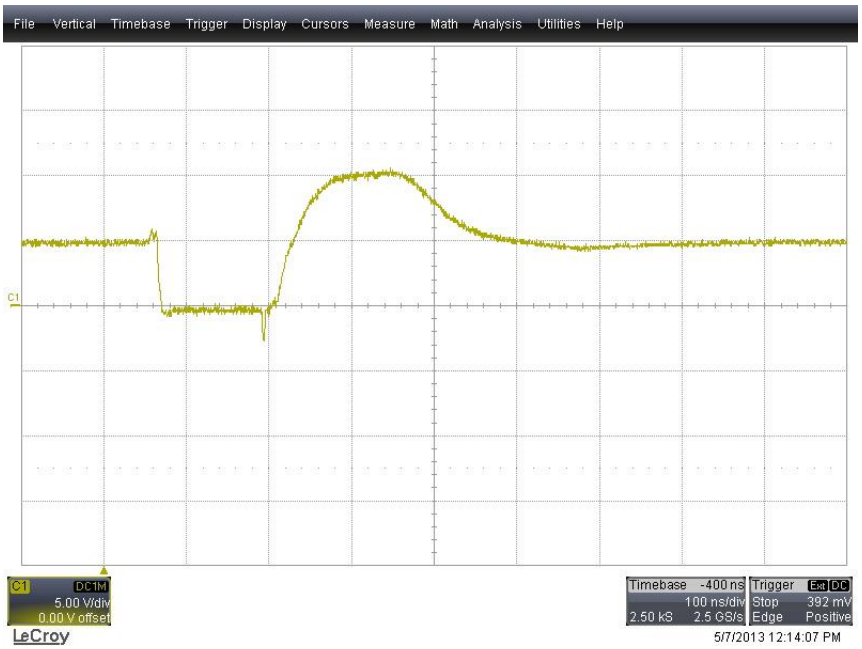

Fig. 5.20 V_{out} versus time when $Z_L = 47.6\Omega$.

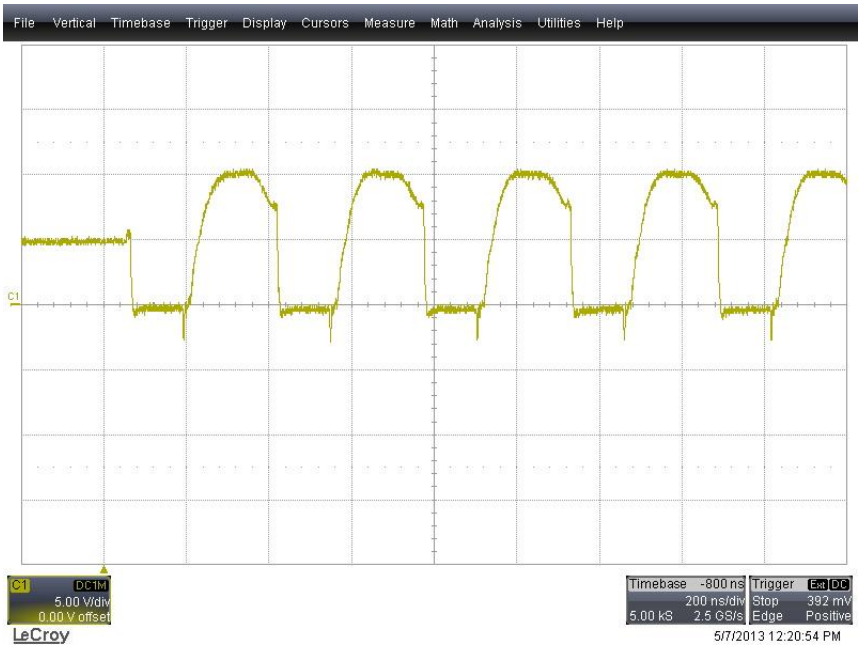

Fig. 5.21 V_{out} versus time when $Z_L = 47.6\Omega$ and where $t_{on} = 1.9 \cdot 66ns = 125ns$ and $t_{off} = 3.5 \cdot 66ns = 231ns$, respectively.

In Figure 5.21 the rise time and fall time were measured to $60ns$ and $20ns$, respectively.

Figure 5.22 depicts the magnitude fast Fourier transform (FFT) of the pulse train in Figure 5.21.

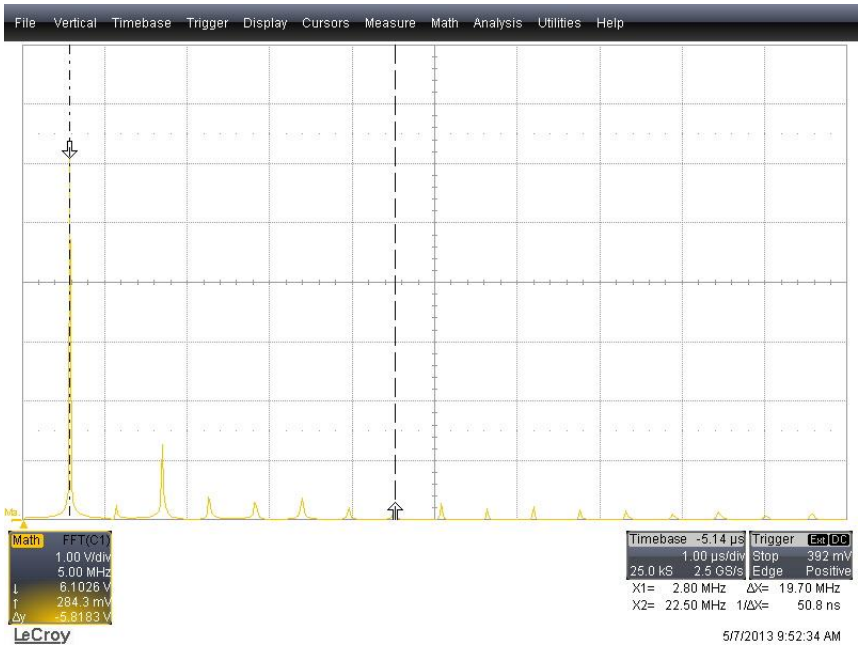

Fig. 5.22 Fast Fourier transform (FFT) of the pulse train generated in Figure 5.21.

Note that the fundamental frequency is indicated at $2.8MHz$.

Regarding the PA, in Figure 3.15, there exists an operating point where $V_{DD} = 10V$ and $R_{ST} \approx 48\Omega$, for a certain P_{in}. Therefore it was decided to use this P_{in}, feed the PA with the pulses in Figure 5.21, and test if load match could be obtained. Using the EA to produce pulse trains of constant magnitude, instead of using it to create modulation patterns of different voltage levels, would ease the analysis of the measurement results.

An efficiency measurement of the EA is described in Section 5.4.1.

5.4.1 Measured Efficiency of EA

The efficiency of the EA was measured when generating a pulse train of 10V. A constant K was introduced to be used when calculating the instantaneous output power in the oscilloscope software:

$$K = \frac{1}{Z_L} = \frac{1}{47.6\Omega} \approx 21 \cdot 10^{-3} \tag{5.21}$$

The instantaneous output power was then calculated as

$$P_{out}(t) = \frac{V_{out}^2}{Z_L} = K \cdot V_{out}^2 = 21 \cdot 10^{-3} \cdot V_{out}^2 \tag{5.22}$$

Figure 5.23 depicts how (5.22) is implemented in the oscilloscope.

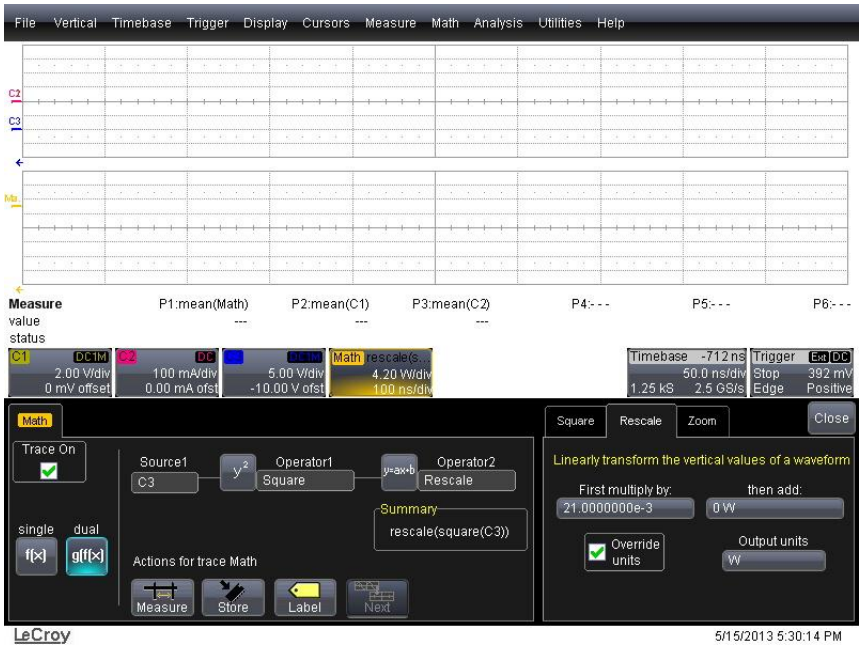

Fig. 5.23 Oscilloscope setup during the efficiency measurements of the EA.

The average output power, $P_{out,av}$, was also calculated in the oscilloscope. The integration time was selected by letting the oscilloscope display at least 10 modulation periods, see Figure 5.24.

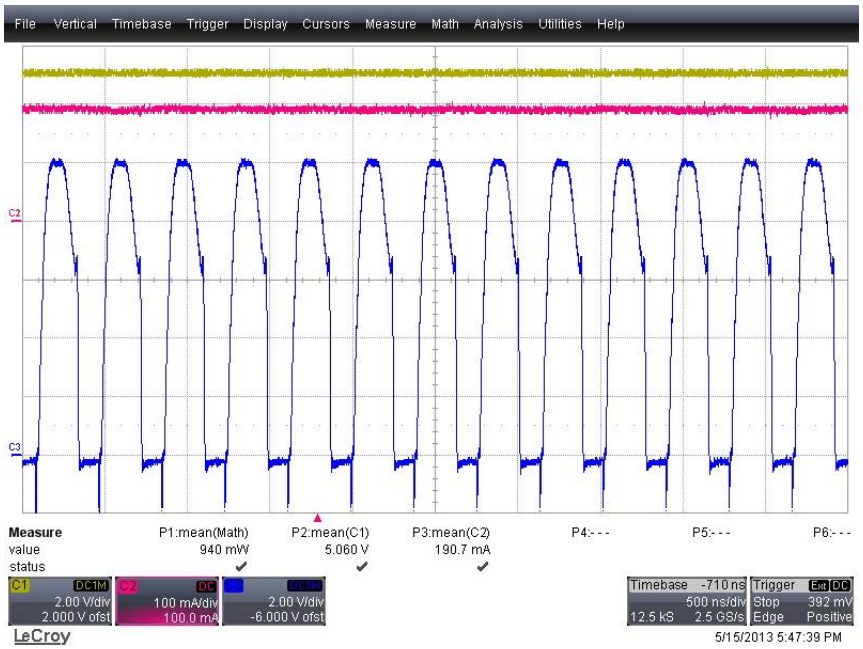

Fig. 5.24 Oscilloscope screen during the efficiency measurements of the EA.

During the efficiency measurements the following values in Table 5.3 were gathered with the help of Figure 5.24 and the different multimeters.

Table 5.3: Data collected during efficiency measurements of EA.

$\mathbf{V_{in}}$	5.06V
$\mathbf{I_{in}}$	190.7mA
$\mathbf{V_{drive}}$	5.98V
$\mathbf{I_{drive}}$	40.05mA
$\mathbf{V_{iso}}$	3.306V
$\mathbf{I_{iso}}$	0.54mA
$\mathbf{P_{out,av}}$	0.94W

By letting

$$P_{in} = P_{PwTr} + P_{aux} = [V_{in} \cdot I_{in}] + [V_{drive} \cdot I_{drive} + V_{iso} \cdot I_{iso}] \tag{5.23}$$

the efficiency is

$$\eta = 100 \cdot \frac{P_{out,av}}{P_{PwTr} + P_{aux}} \approx 77.9\% \tag{5.24}$$

and the power train efficiency is

$$\eta_{PwTr} = 100 \cdot \frac{P_{out,av}}{P_{PwTr}} \approx 97.4\% \tag{5.25}$$

Even if the simulated and measured efficiency were not based on the same modulation patterns, it can be noted that the measured efficiency is lower than the simulated one. However, regarding the power stage efficiency, the simulation results and measurements results are quite similar.

Chapter 6

Integration of Envelope Amplifier and Power Amplifier

In Chapters 3 and 4 R_{ST} and $Z_{ST,ss}$ were measured and simulated with corresponding analysis. The measurements in this Chapter tries to reveal the features of the STI. In Section 6.2 it was tested if load match could be obtained under certain conditions, corresponding to where R_{ST} would give match. In Section 6.2.2 further tests were performed as a way to indicate whether R_{ST} or $Z_{ST,ss}$ best describes the STI. The combined results from the measurements in Section 6.2 and Section 6.2.2 indicated that $Z_{ST,ss}$ best describes the STI for a pulsed voltage supply.

6.1 Measurement Setup

Figure 6.1 is visualizing the measurement setup for the integration measurements.

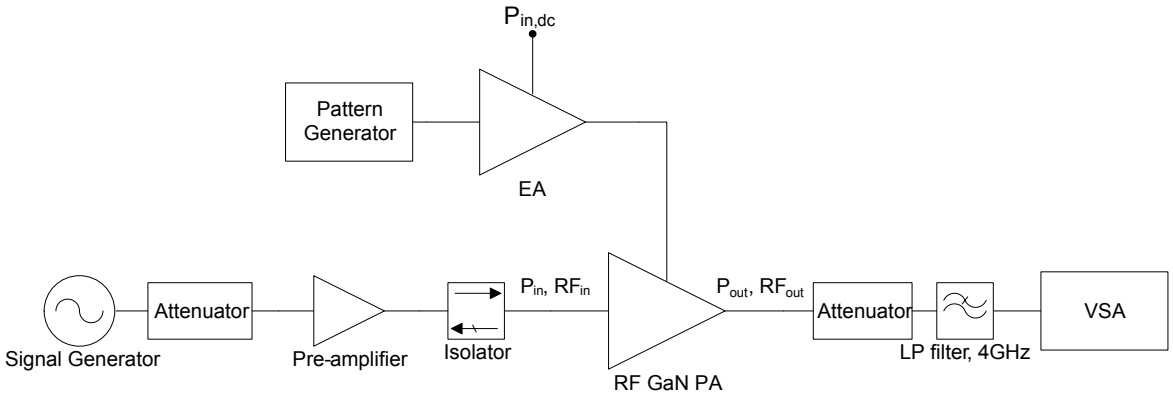

Fig. 6.1 Measurement setup for the integration measurements.

Table 6.1 summarizes the instruments used for the integration.

Table 6.1: Instruments used for Integration measurements.

Type	Name	Function
Logic Analysis System	Agilent 16903A	
Pattern Generator (module)	Agilent 16720A	$V_{gate,EA}, Trigger$
Output Cable	Agilent 16522-61601	
3-state TTL / 3.3V Data Pod	Agilent 10466A	
Power Supply	Powerbox L6405	V_{in}
Power Supply	Topward 6303AS	V_{drive}, V_{iso}
RF Power Meter	HP E4419B EPM series	P_{out}
RF Power Sensor	HP E4412A E Series	P_{out}
Signal & Spectrum Analyzer	R& S FSW 2Hz-26.5GHz	P_{out}
Power Supply	LTronix B502D	$V_{gate,PA}$
Signal Generator	R & S SMR20	P_{in}
Power Supply	Power Box 3000B	$V_{pre-amp}$
400MHz Oscilloscope	LeCroy WaveSurfer 44MXs-A	V_{ST}
DC-50MHz Current Probe	LeCroy AP015	
500MHz Probe	LeCroy PP005A	
500MHz Probe	LeCroy PP009	
Series II Multimeter	Fluke 79	V_{gs}
Dual Display Multimeter	Fluke 45	I_{drive}
Dual Display Multimeter	Fluke 45	I_{iso}
True RMS Multimeter	Fluke 87	V_{in}
True RMS Multimeter	Fluke 87	I_{in}
True RMS Multimeter	Fluke 87	V_{iso}
True RMS Multimeter	Fluke 87	V_{drive}
Series II Multimeter	Fluke 75	$I_{pre-amp}$
LP Filter	Microlab/FXR Rosenberger, LA-40N 4000 Mc.	
Pre-amplifier	Mini-circuits 15542, ZHL-42W-SMA	
Isolator	ISO-001	
2 X 10dB Attenuator	Suhner 6810.19A	
20dB Attenuator	Aeroflex/Weinschel Model: 48-20-34	
20dB Attenuator	Suhner 6620.19.AB	
Coaxial cable 50Ω	RG174 SMB-BNC Cable Assembly 1	

Figure 6.2 depicts an overview of the instruments used in the integration. Figure 6.3 shows the connection between the EA and the PA.

Fig. 6.2 Overview photo of the integration measurement setup.

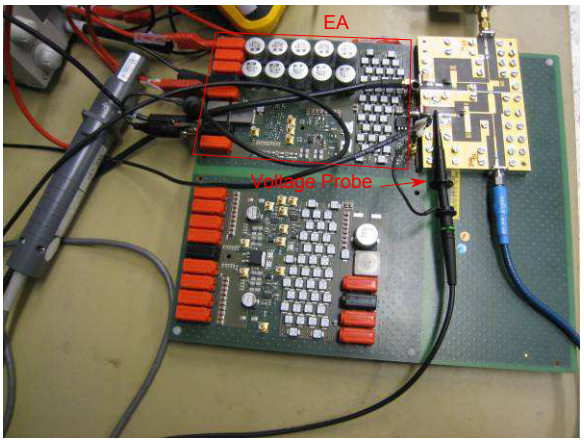

Fig. 6.3 EA to PA connection. The voltage probe measures the voltage at the supply terminal, V_{ST}.

6.2 Measurement Results

As previous mentioned in Chapter 5, the EA seemed to give match when $Z_L \approx 48\Omega$ at $V_{out} = 10V$. By considering Figure 3.15 it was noticed that a value of $R_{ST} \approx 48\Omega$ could statically be obtained with $V_{dd} = 10V$ and a suitable P_{in}. In Section 6.2.1 the idea was to test if this was the case even for a pulsed supply. Section 6.2.1 displays pulse shapes of both voltage and output power. Section 6.2.2 describes further measurements, which were conducted on the PA as well as on various resistive loads. In Section 6.2.2 pulse shapes of voltage are displayed.

6.2.1 Initial Integration

Before the initial integration measurements, the PA was supplied with $V_{dd} = 10V$ and P_{in} was varied until R_{ST} reached 48Ω, at $P_{in} = 27dBm$. In all measurements in this Section $P_{in} = 27dBm$.

In Figure 6.4 the result when feeding the ST with a single pulse, V_{ST}, can be seen. For comparison $V_{EA,(47.6\Omega)}$ has been added, which is the voltage when the EA is feeding a resistive load of 47.6Ω.

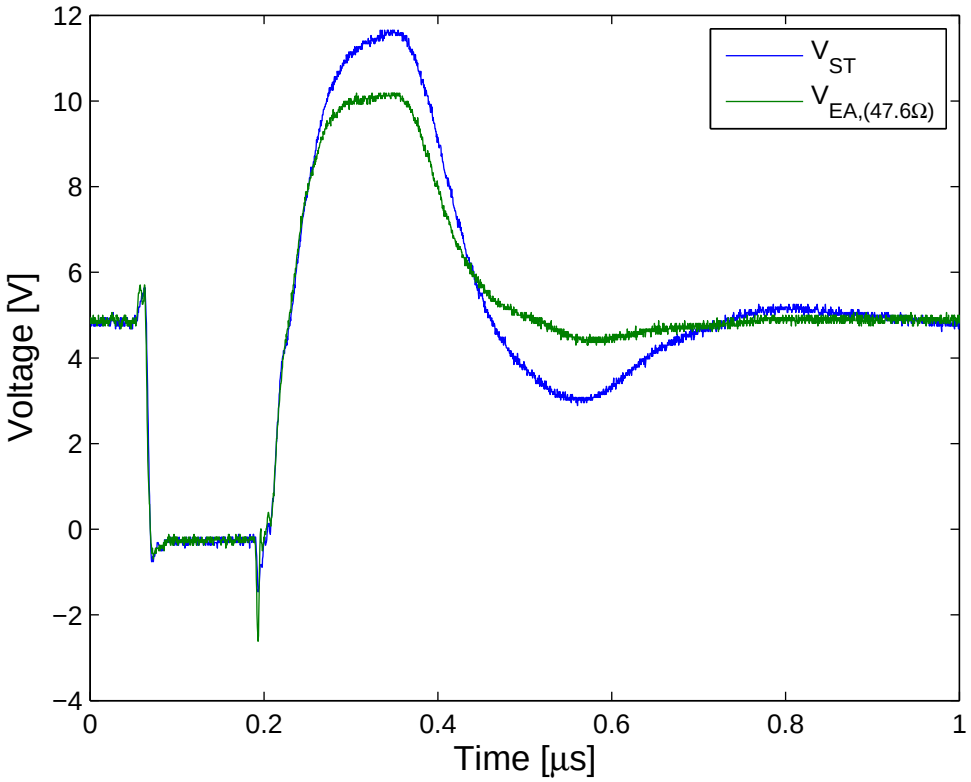

Fig. 6.4 Pulse shape comparison when the EA feeds a resistive load of 47.6Ω and the ST of the PA, respectively.

Note that the pulse in V_{ST} is higher than the pulse in $V_{EA,(47.6\Omega)}$. This indicates that the STI is higher than 48Ω for the conditions in Figure 6.4.

In Figure 6.5 the same type of comparison as in Figure 6.4 is visualized, but now for a pulse train.

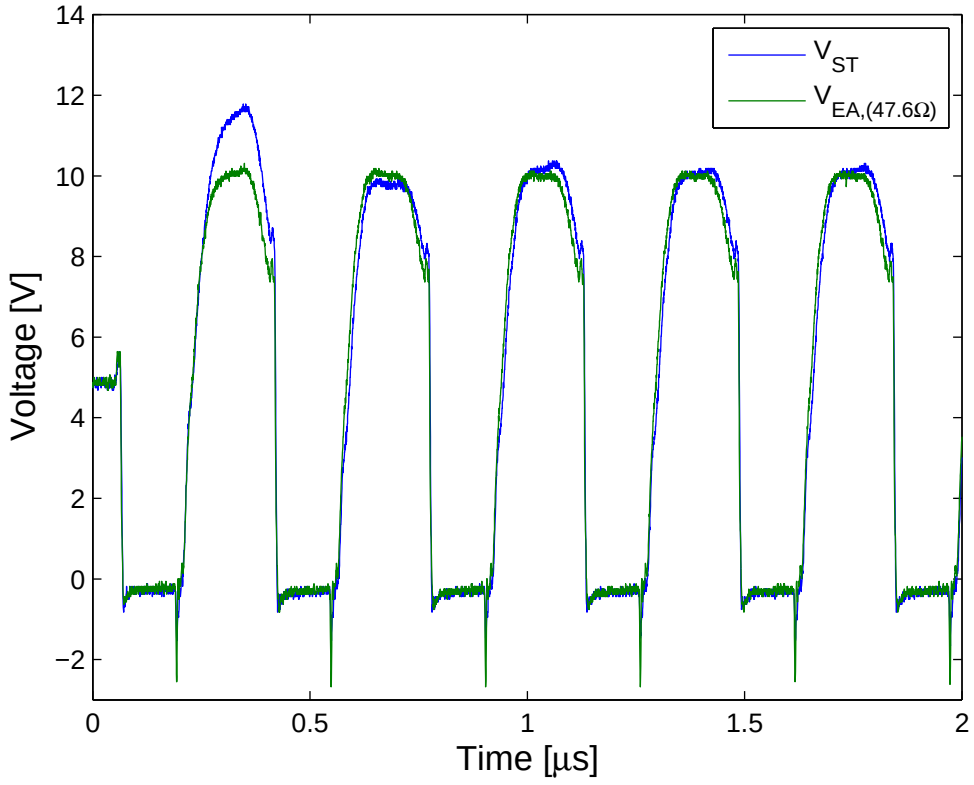

Fig. 6.5 Pulse shape comparison when the EA feeds a resistive load of 47.6Ω and the ST of the PA, respectively.

Note how the behaviour in Figure 5.1 is visible in V_{ST} in Figure 6.5.
Figure 6.6 depicts how P_{out} was statically measured as a function of V_{dd} at $P_{in} = 27dBm$.

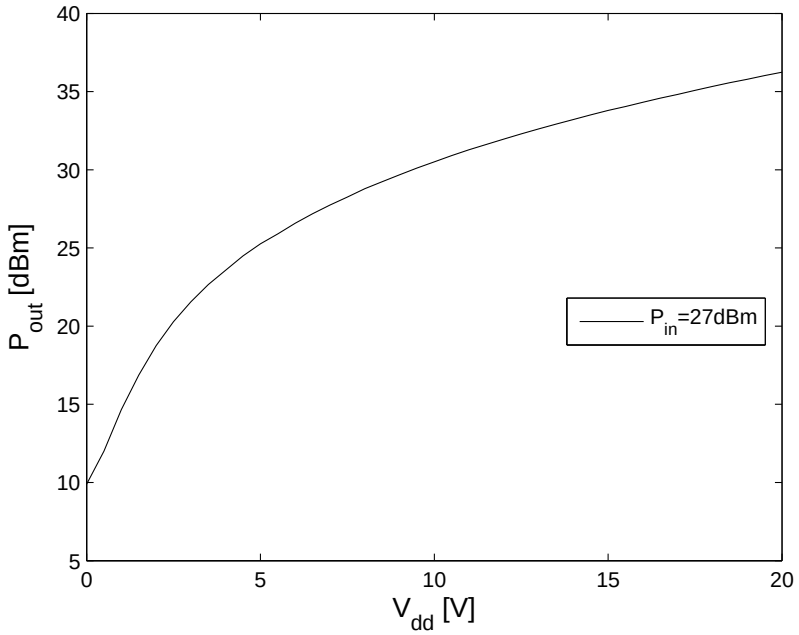

Fig. 6.6 Static data for $P_{out}(V_{dd})$ when $P_{in} = 27dBm$.

With the data in Figure 6.6, a curve fitting tool was used to generate a function, $f_{P,est} = P_{out}(V_{dd})$. The function $f_{P,est}$ is a fourth order polynomial in V_{dd}. In Figure 6.7 $P_{out,m}$ is the measured output power

corresponding to the voltage data V_{ST} in Figure 6.4. $P_{out,est}$ is an estimate of the output power which have been calculated from $f_{P,est}$, using the voltage data V_{ST} from Figure 6.4.

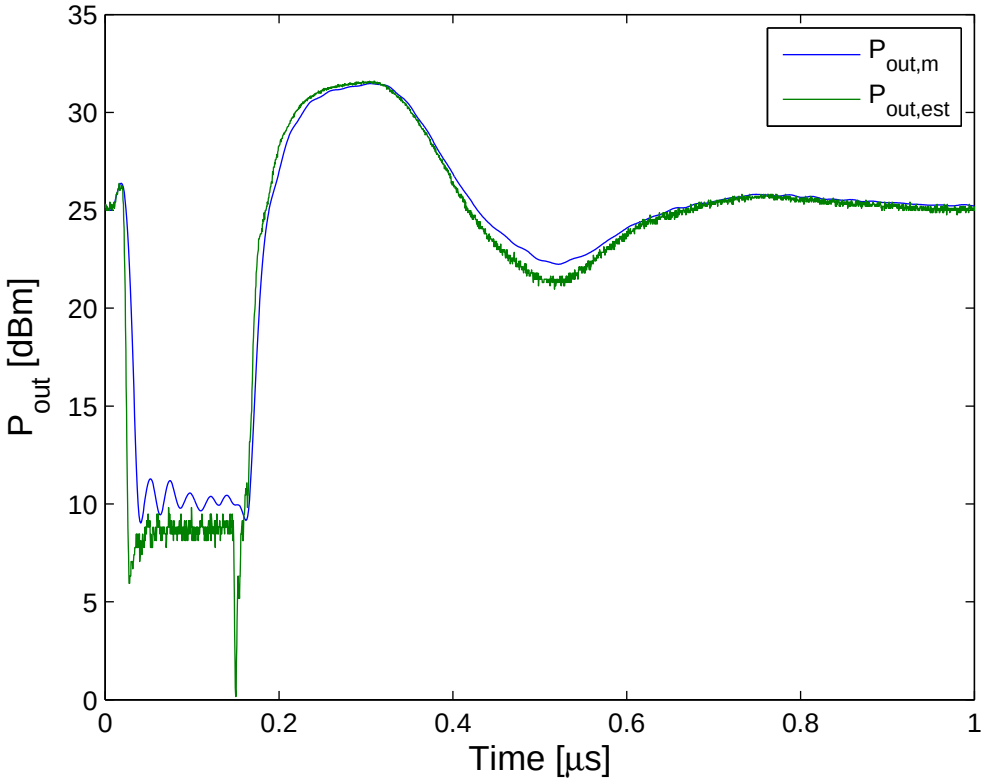

Fig. 6.7 Measured output power, $P_{out,m}$ and estimated output power, $P_{out,est}$ from the V_{ST} data in Figure 6.4.

Figure 6.8 is depicting the same type of comparison as in Figure 6.7, using the voltage data V_{ST} in Figure 6.5.

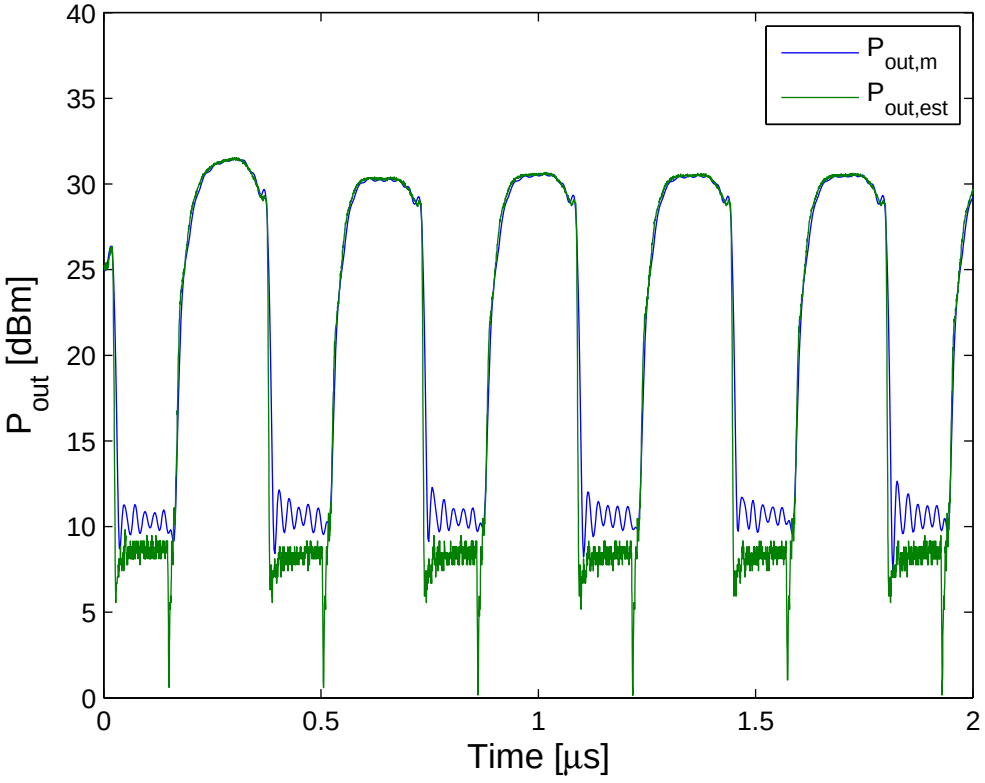

Fig. 6.8 Measured output power, $P_{out,m}$ and estimated output power, $P_{out,est}$ from the V_{ST} data in Figure 6.5.

It is important to note that $f_{P,est}$ is actually not relevant for $V_{dd} < 0V$ even if V_{ST} from both Figures 6.4 and 6.5 contain negative values. Therefore the values in Figures 6.7 and 6.8 below $10.1dBm$ is not relevant.

Analysis

By considering Figure 6.4 it is obvious that the STI is not equal to 48Ω at the chosen operation point. It is not considered likely that an uncertainty in the measurements, which should have put the PA in a slightly different operating point, can explain the large extent of mismatch in Figure 6.4. According to Figure 6.4 and 6.5 R_{ST} does not seem to be a good description of the STI for the given operating point. Otherwise, the appearance of the V_{ST} pulse train in Figure 6.5 correlates well with the theoretical case, where a pulse train of constant magnitude is feeding a mismatched resistive load, see Figure 5.1. Despite the mismatch, the pulse shapes of $V_{EA,(47.6\Omega)}$ in Figures 6.4 and 6.5 seems to be very similar to the corresponding shapes of V_{ST}. Note that the flanks of V_{ST} and $V_{EA,(47.6\Omega)}$ in Figures 6.4 and 6.5 are aligned even though the flanks most likely have met different values of the STI during rise or fall transition, see Section 3.4.3.

Regarding the output power, note that $P_{out,est}$ is very similar to $P_{out,m}$. This means that the instantaneous power of the PA is more or less equal, regardless if the PA is fed with a set of static supply voltages, or with the same voltage set contained in a pulse modulated pattern; the V_{dd} to P_{out} bandwidth of the PA does not seem to be reached with the pulse pattern in Figures 6.4 and 6.5.

6.2.2 Extended Integration

As a way to compare if the results in Figure 3.15 (R_{ST}) or Figure 3.17 ($Z_{ST,ss}$) best describes the STI it was decided to perform measurements to imitate the pulse shapes obtained during the integration measurements at four different operating points. One impedance value from Figure 3.15 and one impedance value from Figure 3.16 was extracted at each of the four operating points. Figures 6.11-6.12 with corresponding Tables 6.4-6.5 shows the result of the comparison together with the extracted and implemented load values. All implemented loads are resistive.

Figure 6.9 visualizes the voltage when the EA is feeding three different loads, based on the PA operating point $(P_{in} = 27dBm, V_{dd} = 10V)$.

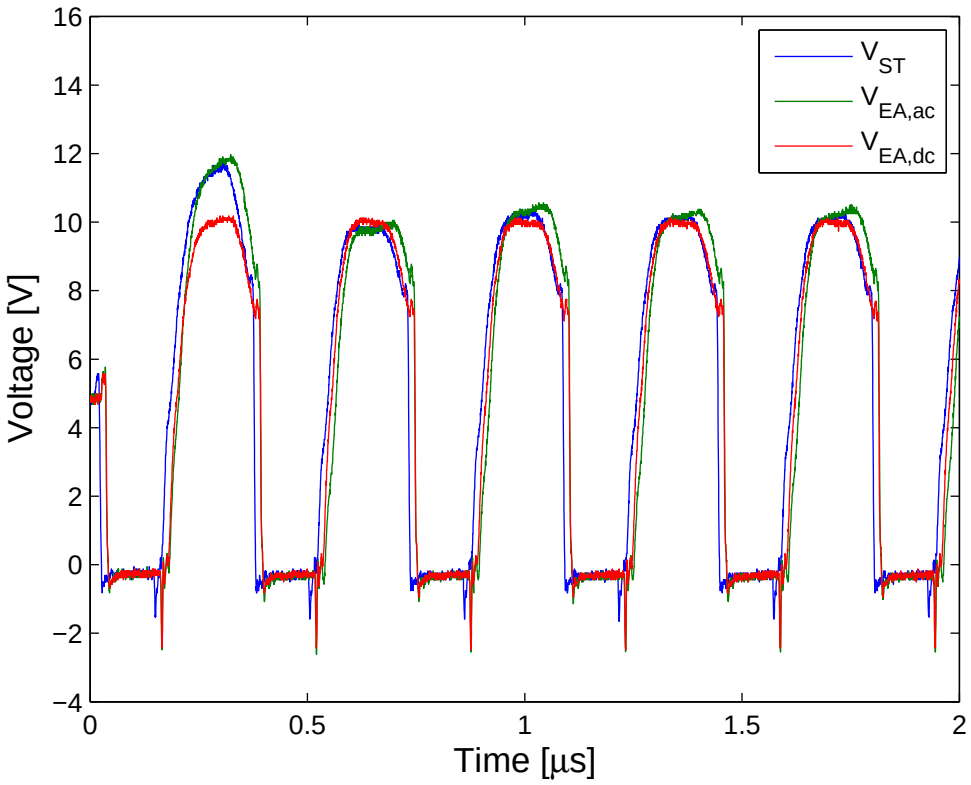

Fig. 6.9 Pulse train for various loads: V_{ST} is the voltage when the EA feeds the STI, $V_{EA,ac}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the ac characterization measurements measurements, see Table 6.2. $V_{EA,dc}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the dc characterization measurements measurements, see Table 6.2.

In Figure 6.9 the first two pulses of $V_{EA,ac}$ is most similar to V_{ST} .
Table 6.2 contains the data which have been used for the measurement in Figure 6.9.

Table 6.2: Extracted and implemented impedances at $(P_{in} = 27dBm, V_{dd} = 10V)$.

Extracted Value	**Implemented Value**
$\mathbf{R_{ST}}$: 48Ω	47.6Ω
$\lvert\mathbf{Z_{ST,ss}}(2MHz)\rvert$, $(\angle\mathbf{Z_{ST,ss}}(2MHz))$: $92\Omega, (-3.6°)$	92.7Ω

Figure 6.10 visualizes the voltage when the EA is feeding three different loads, based on the PA operating point $(P_{in} = 27dBm, V_{dd} = 15V)$.

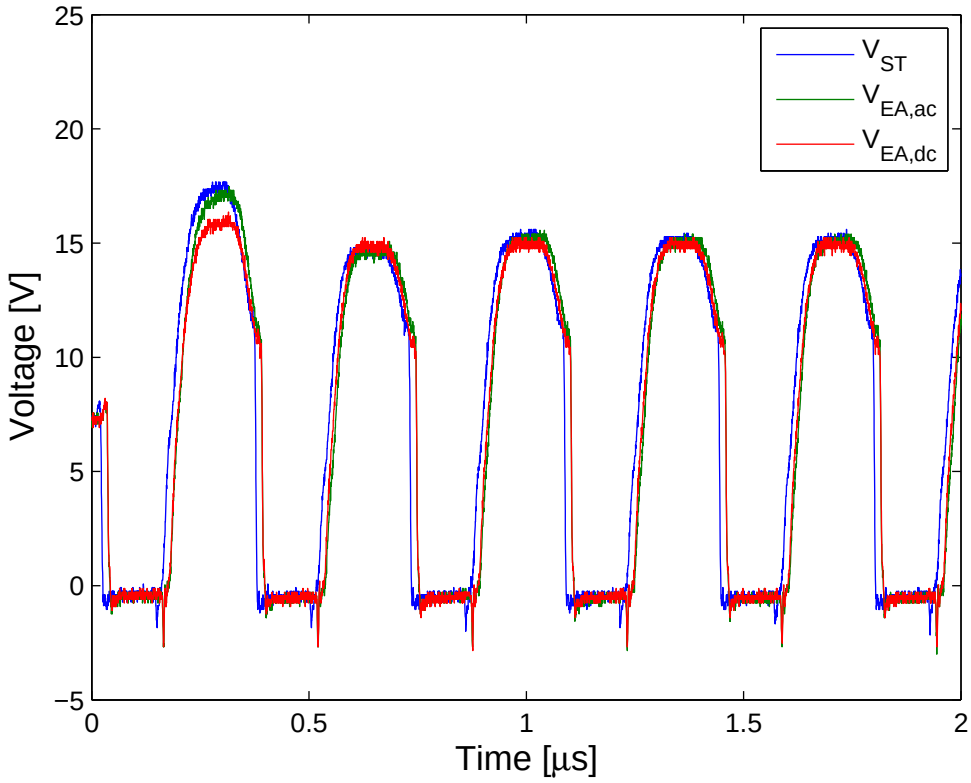

Fig. 6.10 Pulse train for various loads: V_{ST} is the voltage when the EA feeds the STI, $V_{EA,ac}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the ac characterization measurements, see Table 6.3. $V_{EA,dc}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the dc characterization measurements, see Table 6.3.

Note that the nominal voltage of the pulse train in Figure 6.10 is $15V$ ($V_{in} = 7.3V$). In Figure 6.10 $V_{EA,ac}$ is most similar to V_{ST}.

Table 6.3 contains the data which have been used for the measurement in Figure 6.10.

Table 6.3: Extracted and implemented impedances at $(P_{in} = 27dBm, V_{dd} = 15V)$.

Extracted Value	**Implemented Value**
$\mathbf{R_{ST}}$: 59Ω	60.1Ω
$\lvert\mathbf{Z_{ST,ss}}(2MHz)\rvert,\ (\angle\mathbf{Z_{ST,ss}}(2MHz))$: $82\Omega, (-3.1°)$	82.6Ω

Figure 6.11 depicts the voltage when the EA is feeding three different loads, based on the PA operating point $(P_{in} = 22dBm, V_{dd} = 10V)$.

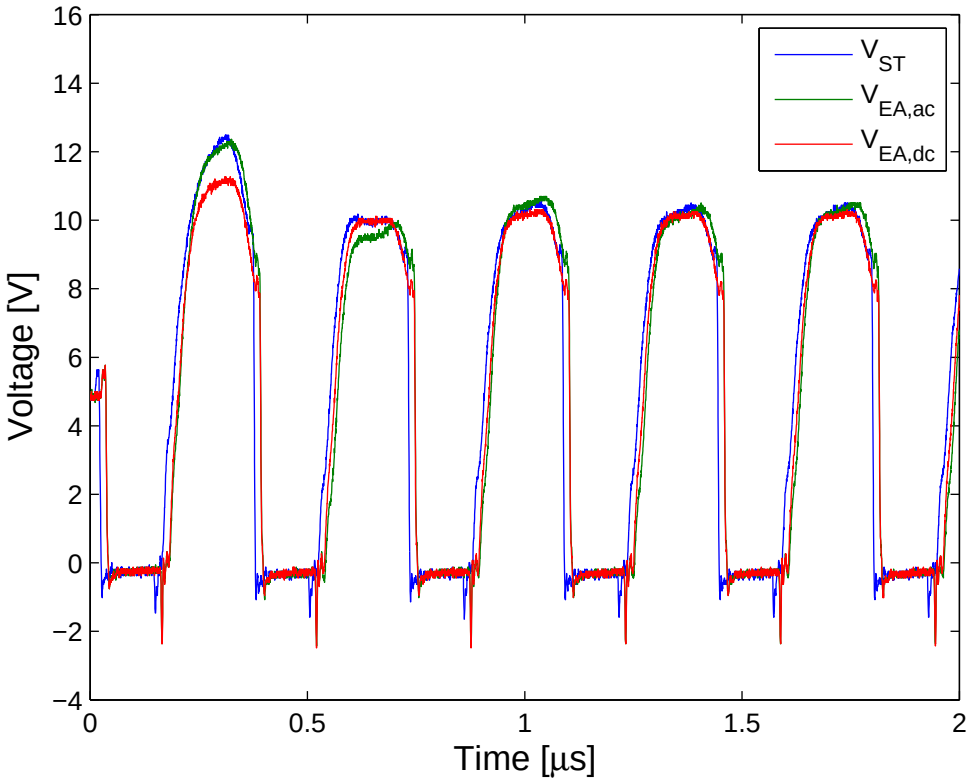

Fig. 6.11 Pulse train for various loads: V_{ST} is the voltage when the EA feeds the STI, $V_{EA,ac}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the ac characterization measurements, see Table 6.4. $V_{EA,dc}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the dc characterization measurements, see Table 6.4.

In Figure 6.11 the first pulse of $V_{EA,ac}$ is most similar to V_{ST}. Regarding the second pulse $V_{EA,dc}$ is most similar to V_{ST}.

Table 6.4 contains the data which have been used for the measurement in Figure 6.11.

Table 6.4: Extracted and implemented impedances at $(P_{in} = 22dBm, V_{dd} = 10V)$.

Extracted Value	**Implemented Value**
$\mathbf{R_{ST}}$: 72Ω	72Ω
$\lvert\mathbf{Z_{ST,ss}}(2MHz)\rvert,\ (\angle\mathbf{Z_{ST,ss}}(2MHz))$: $110\Omega, (-6.25°)$	110.1Ω

Figure 6.12 visualizes the voltage when the EA is feeding three different loads, based on the PA operating point $(P_{in} = 18dBm, V_{dd} = 10V)$.

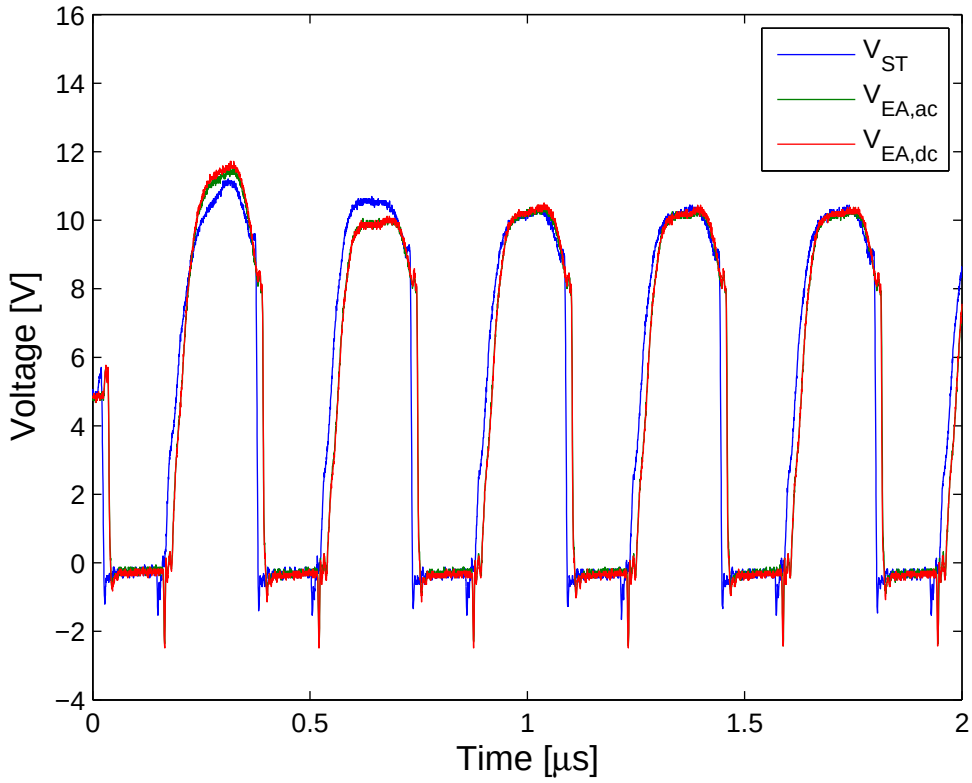

Fig. 6.12 Pulse train for various loads: V_{ST} is the voltage when the EA feeds the STI, $V_{EA,ac}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the ac characterization measurements, see Table 6.5. $V_{EA,dc}$ is the voltage when the EA feeds a resistive load (implemented value) extracted from the ac characterization measurements, see Table 6.5

Note that V_{ST} in Figure 6.12 does not correlate with the behaviour in Figure 5.1: both the first and the second pulse in Figure 6.12 are above V_{nom}. Moreover the behaviour of the first pulse in Figure 6.12 differs from its counterparts in Figures 6.11-6.10.

Table 6.5 contains the data which have been used for the measurement in Figure 6.12.

Table 6.5: Extracted and implemented impedances at $(P_{in} = 18dBm, V_{dd} = 10V)$.

Extracted Value	**Implemented Value**
$\mathbf{R_{ST}}$: 82Ω	82.6Ω
$\lvert\mathbf{Z_{ST,ss}}(2MHz)\rvert,\ (\angle\mathbf{Z_{ST,ss}}(2MHz))$: $78\Omega, (-9.25°)$	78.6Ω

Analysis

The results in Figures 6.11-6.12 indicates that $Z_{ST,ss}$ seems to describe the STI better than R_{ST} does. As can be seen in Tables 6.4-6.5, the implemented resistances differ somewhat from the corresponding extracted values. However, this discrepancy is considered too small to affect the outcome. The measurement uncertainties in $Z_{ST,ss}$ is neither considered to affect the outcome. The ac characterization measurements were carried out up to $2MHz$. Even if the fundamental of the 10V pulse train was measured to be $2.8MHz$, see Section 5.4, this is not believed to affect the conclusion, since $Z_{ST,ss}$ is relatively constant from $0.5MHz - 2MHz$, see Appendix B.

The difference between V_{ST}, $V_{EA,ac}$ and $V_{EA,dc}$ is more clear if considering the first pulse in each pulse train in Figures 6.9-6.11: $V_{EA,ac}$ correlates better with V_{ST} than $V_{EA,dc}$ does. However, note that $V_{EA,ac}$ was not closest to V_{ST} for all pulses in Figures 6.9-6.11. It is important to note that all implemented impedances in the extended measurements have been resistive. Hence, the imaginary parts extracted from the $Z_{ST,ss}$ values have not been imitated. It is hard to say how this will affect the comparison. The pulse

shape of the first pulse of V_{ST} in Figure 6.12 seems to differ compared to its counterparts in Figures 6.9-6.11. If $Z_{ST,ss}$ is considered as a better description of the STI than $V_{EA,dc}$ is, this unusual pulse shape could perhaps be explained by that the phase shift in Figure 3.16 at $(P_{in} = 18dBm, V_{dd} = 10V)$ is larger, $(-9.25°)$, than for the other operating points; compare Table 6.5 with Tables 6.2-6.4. In summary it is considered that R_{ST} is not a good description of the STI during pulse supply and that $Z_{ST,ss}$ is better than R_{ST} in that respect.

Chapter 7

Conclusions

The performance of the constructed EA was limited: it was hard to achieve a good pulse shape quality for different voltage levels, since the characteristic impedance seemed to differ over frequency, see Section 5.3. Never the less the EA measurements demonstrated the possibility of achieving high efficiency and high slew rate for the TL based converter, see Section 5.4.

From the integration results it was found that R_{ST} is an uncorrect description of the STI for a pulsed voltage supply. Hence, for the studied PA, ET operation with a TL based EA cannot be based on the behaviour in Figures 3.14 or 3.15. It is unclear exactly how the STI magnitude and phase contours looks like in the (V_{dd}, P_{in}) area. However, the measurement results from the EA to PA integration indicates that $Z_{ST,ss}$ describes the STI better than R_{ST} does, during a pulsed voltage supply. This result has however only been shown for a few operating points of the PA. More measurements would help to consolidate the indication. If, however it is assumed that this result is correct, it would not be beneficial to use a TL based EA for ET of the studied inverse class F GaN PA, see Section 3.4.3.

7.1 Future work

A future work would be to further investigate the underlying EA performance problems. In integration measurements of the STI, an EA of more ideal performance would ease the corresponding analysis. With further integration measurements it can be tested if the, in this thesis, indication of the STI features can be consolidated. Indirect STI measurements with a pulsed supply could also be combined with more thorough $Z_{ST,ss}$ measurements, which would be taken over a much larger frequency interval. Future work could also be to characterize different PAs' STI to possibly find a PA with beneficial characteristics for ET with a TL based EA.

References

[1] "Artificial (Lumped Element) Transmission Line." [Online]. Available: http://hibp.ecse.rpi.edu/~connor/education/Fields/lumpline.pdf

[2] C. Anderson and D. Runesson, "Methods for determining power supply requirements based on RF spurious level on consumers," diploma thesis, Chalmers University of Technology, Chalmers Tvärgata 1, 412 96 Göteborg, 2006.

[3] D. Cheng, *Field and Wave Electromagnetics*. Boston: Addison-Wesley, 1983.

[4] S. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, Incorporated, 2006.

[5] O. Garcia, M. Vasic, P. Alou, J. A. Oliver, and J. A. Cobos, "An overview of fast dc-dc converters for envelope amplifier in RF transmitters." in *Applied Power Electronics Conference and Exposition APEC, 2012 Twenty-Seventh annual IEEE.*, Feb. 2012, pp. 1313–1318.

[6] B. Herrmann, "Supply modulation study for Ericsson MINI LINK," diploma thesis, Chalmers University of Technology, Chalmers Tvärgata 1, 412 96 Göteborg, 2011.

[7] M. Kiprianoff, "Prime DC/AC Buck-boost Converter - Derivation of mathematical models and evaluation of lumped transmission lines with focus on size and efficiency." diploma thesis, Chalmers University of Technology.

[8] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics*. 111 River Street, Hoboken, NJ: John Wiley & Sons, Incorporated, 2003.

[9] H. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Characterization of switched mode LDMOS and GaN power amplifiers for optimal use in polar transmitter architectures." in *Microwave Symposium Digest, 2008 IEEE MTT-S International.*, June. 2008, pp. 1505–1508.

[10] M. I. Products, "Maxim 7.6A, 12ns, SOT23 MOSFET," May 2003. [Online]. Available: http://datasheet.eeworld.com.cn/pdf/MAXIM/124467_MAX5048BAUT-T.pdf

[11] I. Rectifier, "Irfb3806pbf," February 2008. [Online]. Available: http://www.irf.com/product-info/datasheets/data/irfs3806pbf.pdf

[12] P. Saad, C. Fager, H. M. Nemati, C. Haiying, H. Zirath, and K. Andersson, "A highly efficiency 3.5 GHz inverse class-F GaN HEMT power amplifier," *International Journal of Microwave and Wireless Technologies*, 2010.

[13] S. Sander, "Buck and Boost Converters With Transmission Lines," *IEEE Transactions on Power Electronics.*, vol. 27, no. 7, pp. 4013–4020, 2012.

Appendix A

AC characterization measurements with current probe

This Appendix describes the work which was carried out before performing the ac characterization measurements; it indicates the discovered measurement issues and the limitations imposed on the ac characterization measurements.

Before performing the real STI measurements, the measurement setup in Figure 3.10 was tested against three different impedances. These impedance objects had previously been measured with an LCR meter. It turned out that there was a difference between the phase measured with the LCR meter and the phase measured with the probes. However, it was found that the phase difference was very similar regardless of which impedance object that was tested; somehow a frequency dependent offset was created in the oscilloscope probe measurements. The offset behaviour is depicted in Figure A.1.

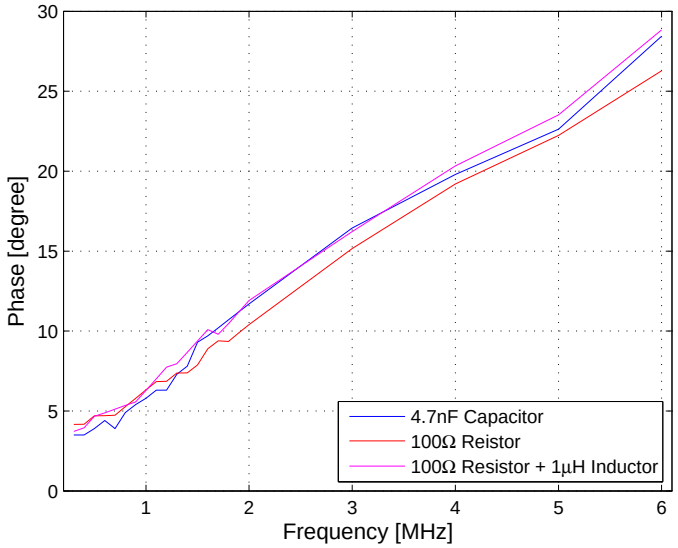

Fig. A.1 Frequency dependent phase offset between LCR measurements and current probe measurements for three different impedance objects.

The magnitude difference between the probe measurements and the LCR measurements did not show any correlated difference for the three test impedances, see Figure A.2 and Figure A.3.

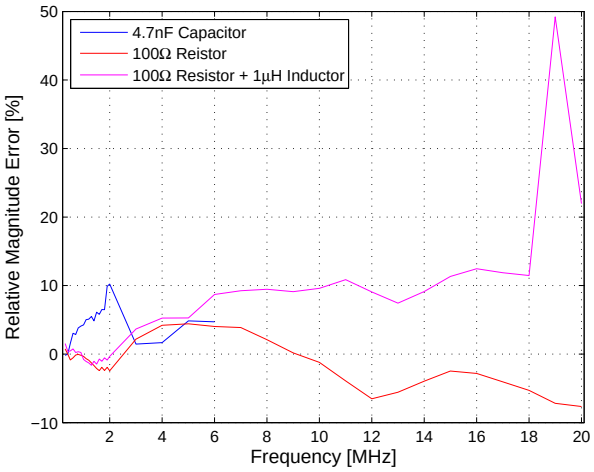

Fig. A.2 Relative magnitude error between current probe measurements and LCR measurements for three different impedance objects.

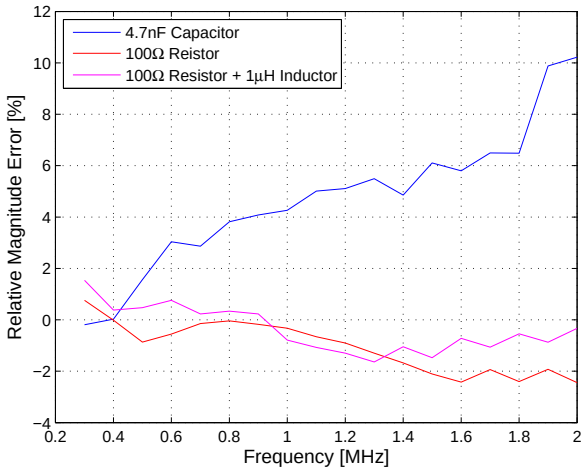

Fig. A.3 Relative magnitude error between current probe measurements and LCR measurements for three different impedance objects.

In Figures A.2-A.3 the relative magnitude error is calculated as $\frac{Probe\ value - LCR\ value}{LCR\ value}$. As can be seen in Figure A.3 the relative magnitude error for the capacitor reaches 10% at $2MHz$. The reason for this might be that the absolute impedance decreases with frequency, see Figure A.4.

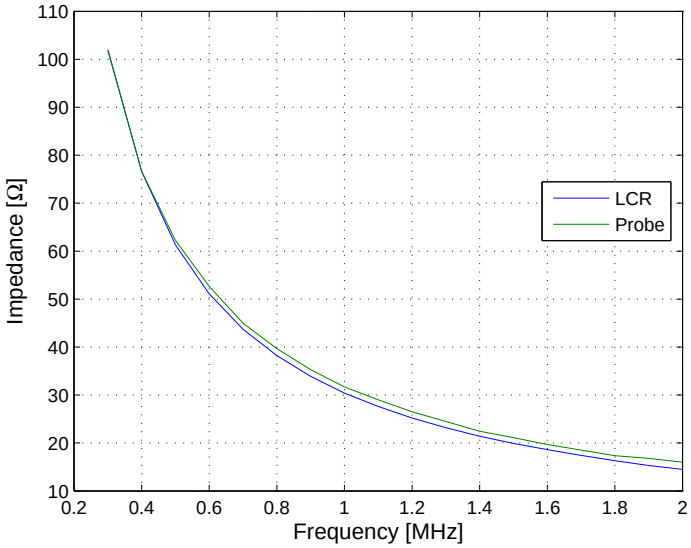

Fig. A.4 Impedance of the test capacitor.

However, up to $2MHz$ the magnitude error was considered sufficiently small: consequently the ac characterization measurements were carried out up to $2MHz$, treating the magnitude as correct but adjusting the phase values with their pre-characterized offset at each frequency. The impedance plots for the resistor and the resistor plus inductor is visualized in Figure A.5-A.6.

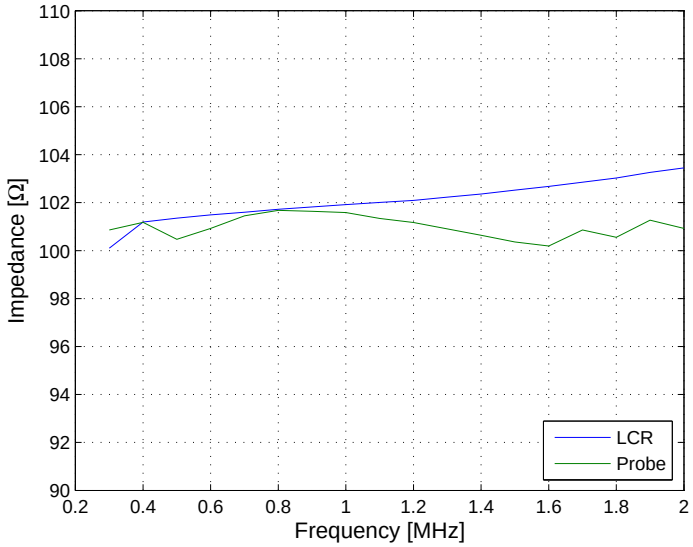

Fig. A.5 Impedance of the test resistor.

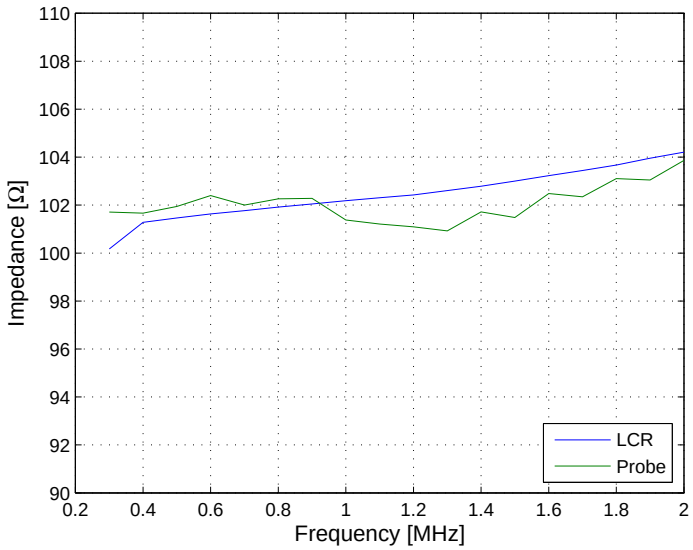

Fig. A.6 Impedance of the test resistor plus inductor.

Appendix B

Results from the AC characterization measurements

This Appendix shows magnitude and phase plots from the the ac characterization measurements.

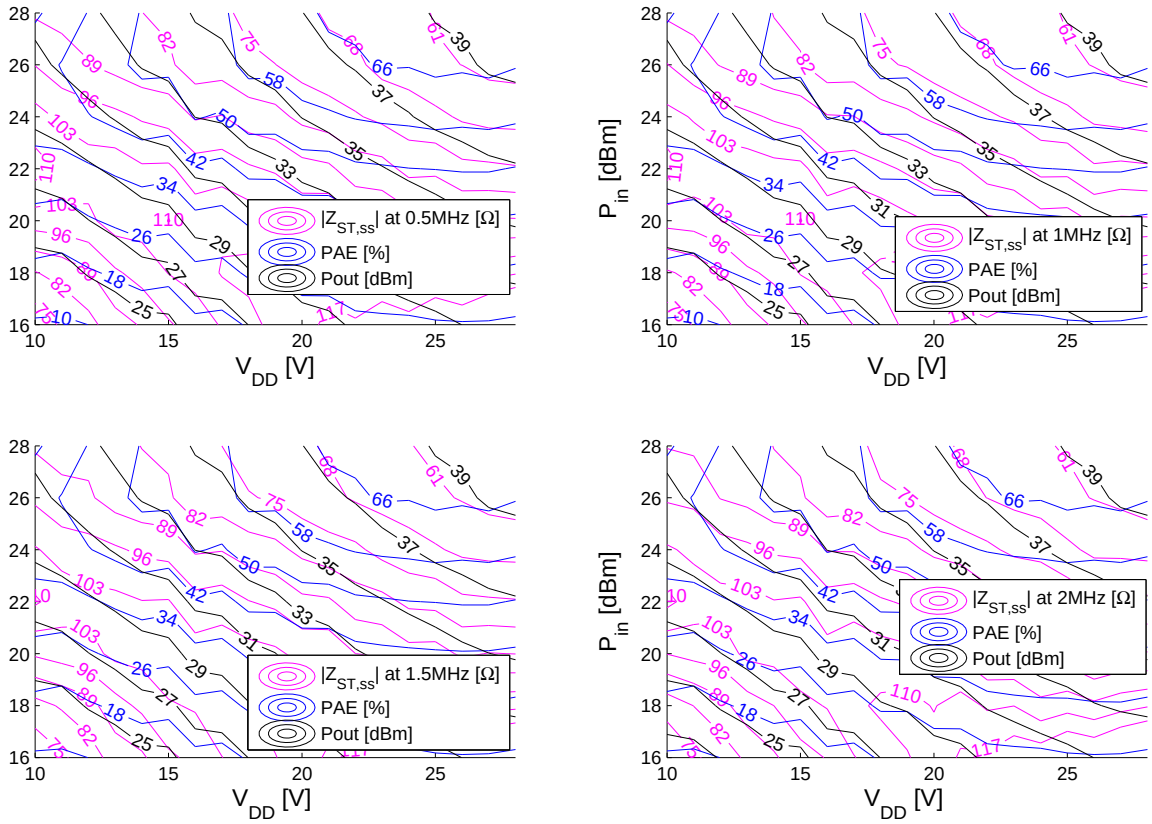

Fig. B.1 Iso curves of measured $|Z_{ST,ss}|$, PAE and P_{out}.

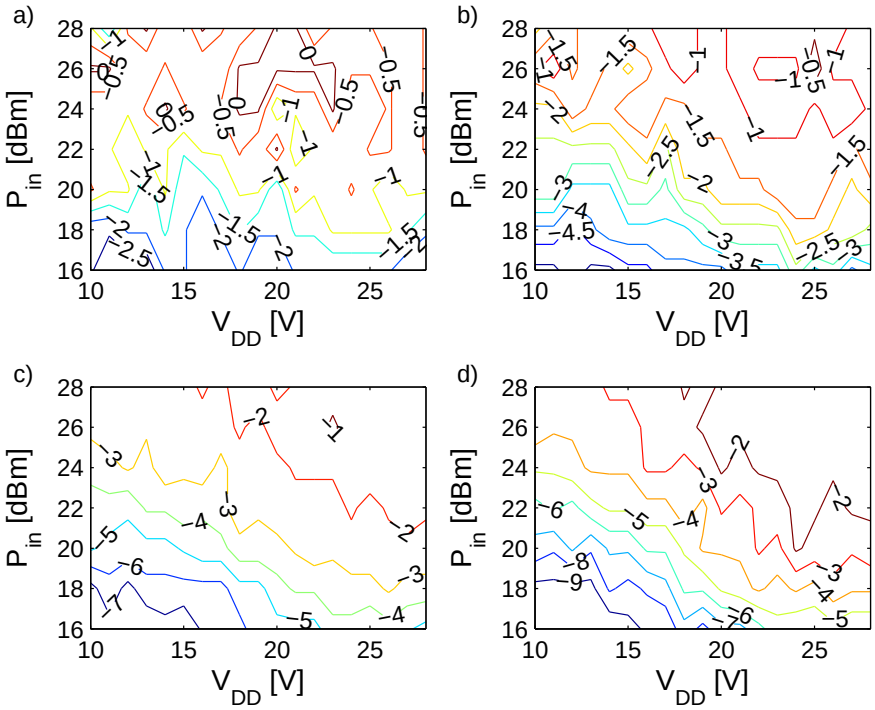

Fig. B.2 Iso curves of measured $Z_{ST,ss}$ phase. Sub Figures a, b, c and d corresponds to frequencies $0.5MHz$, $1MHz$, $1.5MHz$ and $2MHz$, respectively.