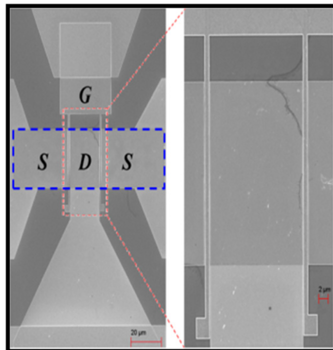
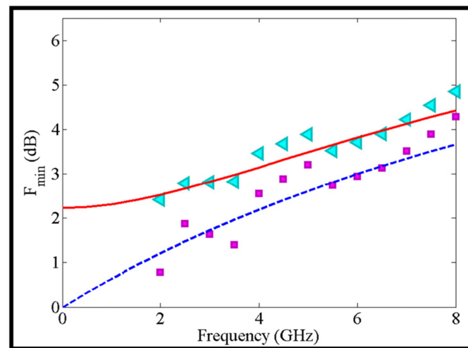
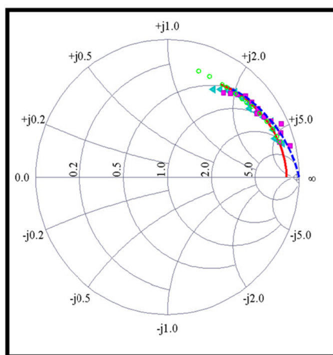
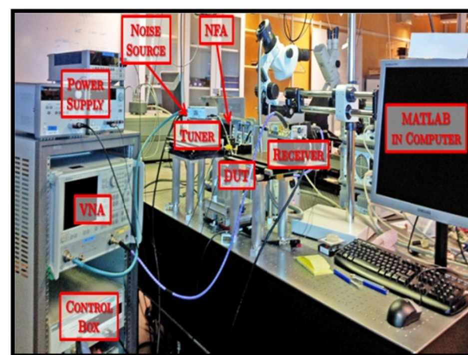
CHALMERS









Noise Parameter Characterisation of Graphene Field Effect Transistors in the 2-8 GHz Frequency Range

Thesis for Erasmus Mundus Master of Science in Nanoscience and Nanotechnology

MEHBUBA TANZID

Department of Microtechnology and Nanoscience
Terahertz and Millimetre Wave Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden, 2013

ERASMUS MUNDUS

Thesis for the degree of

Erasmus Mundus Master of Nanoscience and Nanotechnology

Noise Parameter Characterisation of Graphene Field Effect Transistors in the 2-8 GHz Frequency Range

---

Author:
Mehbuba Tanzid

Supervisor:
Michael Andersson

Promoter:
Prof. Jan Stake, Chalmers

Co-promoter:
Prof. Marc Heyns, KU Leuven

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience
Chalmers University of Technology

2013

Noise Parameter Characterisation of Graphene Field Effect Transistors in the 2-8 GHz Frequency Range
MEHBUBA TANZID

© Mehbuba Tanzid, 2013

Terahertz and Millimetre Wave Laboratory
Department of Microtechnology and Nanoscience - MC2
Chalmers Univeristy of Technology
SE-412 96 Göteborg
Sweden
Telephone + 46 (0)31-772 1000

Cover:
Clockwise: SEM image of GFET, measured and modelled minimum noise figure of extrinsic and intrinsic GFET, noise measurement setup, measured and modelled Γ_{opt} of extrinsic and intrinsic GFET with Γ_s for MSG.

This report is written in LaTeX

Printed by Chalmers Reproservice
Göteborg, Sweden 2013

To Abbu, Ammu, Kinzol, Ontika and Tanbir

Abstract

Graphene is promising for being used as a channel material in high frequency and low noise field effect transistors (FETs). This is facilitated by its superior near-room temperature mobility (10^5 cm^2/V·s) for both type of carriers and predicted high value of saturation velocity (4×10^7 cm/s).

This thesis presents noise parameter characterisation of graphene field effect transistors (GFETs) using source-pull measurement technique in the 2 to 8 GHz frequency range. Commencing from cleanroom fabrication, all stages of the work including measurement and modelling for device characterisation are dealt with in this study. In the first part of the thesis, a procedure for GFET fabrication utilising CVD graphene is developed. The device properties such as gate leakage, contact resistance, and annealing condition are optimised. The obtained contact resistance is 135 $\Omega \cdot \mu$m which is state-of-the-art. GFETs fabricated using CVD graphene on silicon dioxide (300 nm)/silicon substrate with 1 μm long and 2×30 μm wide graphene channels are characterised to obtain the noise performance at device level. The cut-off frequency and the maximum frequency of oscillation of the GFETs are on the order of 10.5 GHz and 13 GHz, respectively. The measured minimum noise figure was 2.4 to 4.9 dB for the extrinsic device with a corresponding associated gain of 10.6 to 2 dB in this frequency range. The intrinsic device has minimum noise figure of 0.8 to 4.3 dB after de-embedding the parasitic noise contribution using noise correlation matrices. Subsequent application of Pospieszalski two-temperature noise model provided a drain noise temperature of 1950 K and a gate noise temperature of 700 K.

Keywords: Graphene FET (GFET), Microwave FET, Noise measurements, Noise Figure

Acknowledgements

At first I would like to thank the almighty Allah for giving me the ability to finish this thesis. I would like to thank Prof. Jan Stake for providing me the opportunity to work in this really interesting and challenging topic and also for his valuable guidance. I would like to take this occasion to express my sincere gratitude to Mr. Michael Andersson for sharing his expertise on processing and measurement techniques and his knowledge in microwave engineering. I also thank him for his constant guidance, valuable suggestions along with the encouragement and support he has generously extended throughout the progress of my work. Without his continuous supervision, this work would have been impossible.

I would like to thank Mr. Omid Habibpour for helping with the GFET layout and Mr. Olle Axelsson for his help with noise measurements. I would also like to thank all my colleagues at the Terahertz Millimetre Wave Laboratory and all the staff in the Nanofabrication Laboratory, MC2 for being very helpful and supportive.

I express my gratitude to Prof. Marc Heyns for being my co-promoter at KU Leuven. I apologise that discussion was not possible more often due to the constraints in time and space.

I would like to acknowledge the European commission for providing me the opportunity for pursuing this Erasmus Mundus masters programme. I would like to thank Prof. Guido Groeseneken, Prof. Göran Johansson, Ms. Elke Delfosse, Ms. Anouck Brouwers and all other members of the EMMNano programme for their support and guidance during the programme. I would also like to thank all my friends in EMMNano and KU Leuven with whom I have spent two memorable years.

Lastly, I would like to express my heartiest gratitude to my family. They always guided me to the path of right and just and supported me with all they could. Without their support I could not have done anything.

M. Tanzid
Göteborg
August 26, 2013

Contents

Abstract **v**

Acknowledgements **vii**

List of Tables **xi**

List of Figures **xiii**

List of Symbols and Abbreviations **xv**

1 Introduction **1**

1.1 Microwave and Terahertz FETs 1
1.2 Noise in Microwave FETs 2
1.3 Graphene 3
1.4 Graphene FETs in Microwave 4
1.5 Noise in GFETs 5
1.6 Thesis outline 6

2 Theoretical Background **7**

2.1 Two-Port System 7
2.2 Field Effect Transistors 8
2.2.1 DC Characteristics 8
2.2.2 Small Signal FET Model 11
2.2.3 Parasitic Extraction and De-embedding Techniques . . . 12
2.3 Noise 15
2.3.1 Noise Parameters 15
2.3.2 Noise Correlation Matrix 17
2.3.3 Pospieszalski Noise Model 17

2.4 FET Figure of Merits . . . 18
2.4.1 Stability and Gain . . . 18
2.4.2 FET f_T and f_{max} . . . 20
2.4.3 Minimum Noise Figure . . . 20

3 Processing and Measurement Techniques 23
3.1 Device Fabrication . . . 23
3.1.1 CVD Graphene . . . 23
3.1.2 GFET Fabrication . . . 25
3.2 Device Optimisation . . . 27
3.2.1 Annealing . . . 27
3.2.2 Gate Leakage . . . 29
3.2.3 Contact Resistance . . . 30
3.3 Device Measurement . . . 31

4 Results and Discussions 35
4.1 DC Characteristics . . . 35
4.2 Small Signal Characteristics . . . 36
4.2.1 Parasitic Components . . . 36
4.3 Noise Characteristics . . . 37
4.3.1 Noise Modelling . . . 37
4.3.2 Comparison of Γ_{opt} with Γ_s for Maximum Gain . . . 38
4.4 Discussions . . . 39

5 Conclusion 49
5.1 Summary . . . 49
5.2 Outlook . . . 49

Bibliography 51

A Journal Manuscript 61

List of Tables

4.1 Parameters for Mobility Extraction 35
4.2 Extracted Parasitic Components of GFET 37
4.3 Intrinsic GFET Parameters for Noise Model and Obtained Noise Temperatures 38
4.4 Noise Performance Comparison of Different FET Technologies at $f = 2$ GHz in RT 39

List of Figures

1.1 Crystal structure and dispersion relation close to the Dirac point of (a) large area graphene and (b) graphene nanoribbon. 3

1.2 (a) f_T of graphene MOSFETs versus L along with f_T performance of the best CNT FET, InP HEMTs, GaAs mHEMTs, GaAs pHEMTs (pseudomorphic HEMT), and Si MOSFETs. (b) f_{max} of graphene MOSFETs versus L along with f_{max} performance of InP HEMTs, GaAs mHEMTs, GaAs pHEMTs, and Si MOSFETs. Updated from [28]. 5

2.1 Two-port network system 7

2.2 (a)Transfer characteristic at $V_{DS} = 10$ V and (b)output characteristics of MOSFET, $k = \mu C_{ox}\frac{W}{L}$. The dashed line separates the triode and saturation region. 9

2.3 Small signal equivalent circuit of the GFET. 12

2.4 Small signal equivalent circuit of the (a) open and (b) short structures. 14

2.5 Noise representation in two port network by (a) current source at input and output and (b) voltage and current source at input. 16

3.1 Schematic of the cold-wall CVD system. [56] 24

3.2 Schematic illustration of the frame assisted H_2 bubbling transfer. (a) Gluing of the plastic frame on top of the sample with PMMA A4 resist. (b) Separation of the frame/PMMA/graphene from the Cu foil by H_2 bubbles induced by electrolysis of H_2O. (c) Removal of the frame after transferring graphene on desired substrate. [57] 26

3.3 Schematic of the GFET fabrication steps. 27

3.4 (a) SEM image of the complete GFET (scale bar 20 μm) and zoomed image of the active region (scale bar 2 μm), $L = 1$ μm, $W = 60$ μm. 28
3.5 Transfer Characteristics of GFETs with different annealing treatment. 29
3.6 I-V Characteristics of MOS capacitors with varying thickness of Al_2O_3. 30
3.7 Transfer Characteristics of GFETs with varying L_a. 31
3.8 Noise Measurement Setup. 32
3.9 Schematic of Noise Measurement Setup. 33

4.1 Transfer characteristic and transconductance of GFET at $V_{DS} = -1.5$ V. 41
4.2 Output characteristic of GFET at $V_{GS} = -2$ to 2 V. 41
4.3 Measured and modelled transfer characteristic of GFET at $V_{DS} = -0.1$ V. 42
4.4 Measured and modelled GFET S-parameters from 2 to 8 GHz at the bias point of $V_{GS} = 0.08$ V and $V_{DS} = -1.5$ V. 42
4.5 Calculated short-circuit current gain and Mason's unilateral power gain of the GFET at the bias point of $V_{GS} = 0.08$ V and $V_{DS} = -1.5$ V. 43
4.6 Determination of contact resistance from TLM measurement with corrected contact spacing from SEM measurement. 43
4.7 Measured and modelled minimum noise figure of the extrinsic GFET for three measurements. 44
4.8 Measured and modelled minimum noise figure of the extrinsic and de-embedded GFET. 44
4.9 Measured and modelled noise resistance of the extrinsic and de-embedded GFET. 45
4.10 Measured and modelled optimum source reflection coefficient of the extrinsic and de-embedded GFET. 45
4.11 Validation of Pospieszalski noise model for measured noise parameters of GFET. 46
4.12 Stability factors of GFET. 46
4.13 Transducer power gain, available power gain and maximum stable gain of GFET with $\Gamma_s = \Gamma_{opt}$ and $\Gamma_L = 0$. 47

List of Symbols and Abbreviations

Γ_s, Γ_L	Source and load reflection coefficient
Γ_{opt}	Source reflection coefficient for minimum noise
μ_e, μ_h	Electron and hole mobility
ρ_c	Metal to graphene contact resistivity
ρ_g	Gate material resistivity
a	Lattice constant
B	Noise bandwidth
C_D	Noise correlation matrix of the intrinsic device
C_P	Noise correlation matrix of the parasitic network
C_q	Quantum capacitance
C_{ox}	Gate oxide capacitance per area
C_{PD}	Noise correlation matrix of the extrinsic device
F	Noise figure
f_T	Cut-off frequency
f_{max}	Maximum frequency of oscillation
F_{min}	Minimum noise figure
G_a	Associated gain
g_d	Output conductance

g_m	Transconductance
g_n	Noise conductance
h	Gate height
I_{DS}	Drain current
k	Boltzmann constant
L	Gate length
L_a	Length of the ungated access region of GFET
L_c	Contact separation for TLM measurement
n_0	Residual carrier density
P_N	Available noise power
P_S	Available signal power
q	Charge of electron
R_a	Resistance in the ungated access region of GFET
R_c	Metal-graphene contact resistance for each contact (TLM)
R_g	Gate resistance
R_n	Noise resistance
R_s, R_d	Source and drain contact resistances
R'_s, R'_d	Source and drain metal resistance
R_{ch}	Shorted channel resistance
R_{DS}	Drain to source resistance
R_{ext}	Extra resistance at metal-graphene contact for electron as channel carrier
R_{m-g}	Metal to graphene contact resistance

R_{pg}, R_{pd}	Substrate leakage resistances through gate and drain pads
R_{sheet}	Sheet resistivity of graphene
R_{tot}	Total measured resistance (TLM)
T_d	Drain noise temperature
T_g	Gate noise temperature
T_{min}	Minimum noise temperature
V_{dirac}	Voltage at Dirac point
V_{DS}	Drain voltage
V_{GS}	Gate voltage
V_{th}	Threshold voltage
W	Gate width
W_c	Contact width for TLM measurement
W_f	Gate finger width
Z_0	Reference impedance
Z_s, Z_L	Source and load impedance
FET	Field Effect Transistor
GFET	Graphene Field Effect Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterojunction Field Effect Transistor
LNA	Low Noise Amplifier
MESFET	Metal-Semiconductor Field Effect Transistor
mHEMT	metamorphic High Electron Mobility Transistor
MISFET	Metal Insulator Semiconductor Field Effect Transistor

MSG	Maximum Stable Gain
pHEMT	pseudomorphic High Electron Mobility Transistor
TLM	Transmission Line Model

Chapter 1

Introduction

Since the advent of the breakthrough paper [1] on graphene, this carbon-based 2D (two-dimensional) material has attracted enormous attention in basic and applied research as well as in electron device arena. In a single package, graphene comes with many exquisite electrical and mechanical properties such as current density (highest reported: $10^8 A/cm^2$ [2]), carrier mobility (up to 2×10^5 cm^2/V·s at low temperature [3]) and thermal conductivity [4] (5×10^3 W/mK). Consequently, graphene possesses great potential to be used as a channel material in field effect transistor (FET), whose performance can greatly benefit from the high carrier velocity of graphene. It also has the added benefit of being planar and compatible with current silicon technology. As a result graphene is promising for being used in microwave ($0.3 - 300$ GHz) as well as terahertz ($0.1 - 10$ THz) applications.

1.1 Microwave and Terahertz FETs

Use of microwave is integrated in the day-to-day life of modern age. From wireless communication for mobile phones and high speed internet extending to satellite communication, microwave is used everywhere. With technological advancements, the ability to reach terahertz frequencies has opened the door for innovative applications in security, space and imaging technology as well. Indivisible to such applications are microwave and terahertz FETs. Although the principle of FET was demonstrated in 1952 by W. Shockley [5], the first microwave transistor [6] was reported much later by W. Hooper and W. I. Lehrer in 1967 using epitaxial GaAs metal-semiconductor field effect transistor

(MESFET) with a maximum frequency of oscillation, $f_{max} = 3$ GHz. The issue in concern with this technology is that the operating frequency of transistors is limited to $f < 50$ GHz. The performance of microwave transistors can be improved mainly from three aspects: optimising structure, introducing device with new structure or introducing new material with better electronic properties. The first method is approached e.g. by scaling the gate length in many researches. In 1980, a new structure which is high electron mobility transistor (HEMT) [7] using GaAs was introduced. This enabled the gradual development towards transistors operating in the terahertz frequency range. Later on, InP substrates were introduced which allowed higher mobility channels as a result of being lattice matched with higher In content materials. For the last 20 years, InP HEMTs have held the record of frequency response in f_{max}. The reported highest f_{max} for InP HEMT is 1.2 THz [8] and the record cut-off frequency (f_T) is 688 GHz [9] for InGaAs mHEMTs. Although the mHEMT uses GaAs substrate but a thick InAlAs buffer with graded doping allows larger mismatch and higher In content in the device channel, and thus higher mobility. Eventually, the maturity of the current technologies has been reached by approaching the limit of gate length downscaling (~30 nm) and the InP HEMT channels being pure InAs. Nonetheless, the increasing need for transistors to operate at even higher frequency resulted increasing efforts to explore new structures such as nanowires and new materials such as graphene.

1.2 Noise in Microwave FETs

Low noise amplifier (LNA) is one of the crucial building blocks of any communication system. Being the first element of a low noise receiver system, the LNA sets the noise figure of the complete chain. As a result, the noise parameters, especially the minimum noise figure (F_{min}), of a microwave FET is just as important figure-of-merit as f_T and f_{max} [10].

For designing low-noise microwave FETs, it is crucial to have knowledge of the sources and magnitude of noise generated in the transistor in the operating frequency range. Various noise sources in electronics include thermal noise or Johnson-Nyquist noise [11,12], shot noise [13], flicker or $1/f$ noise etc. Thermal noise, which is unavoidable in any electronic system, originates from the thermal agitation of the charge carriers (usually the electrons) inside an

electrical conductor at equilibrium, which happens regardless of any applied voltage. In FETs, thermal noise is mainly generated from different contact resistances. Shot noise and $1/f$ noise become important for FETs with large gate leakage current [14]. The physical origin of high frequency noise in MESFETs or HEMTs is fluctuations in the carrier density and/or the carrier drift velocity in the conducting channel and in the parasitic resistances [11, 12]. These fluctuations cause random variations of the current passing through the transistor, or, equivalently, of the voltage drop across it.

1.3 Graphene

Graphene is the name given to the arrangement of carbon atoms in a hexagonal honeycomb lattice (lattice constant, $a = 1.42$ Å) that is exactly one atom thick ($d \simeq 0.3$ nm) as shown in Fig. 1.1(a). It is this arrangement and symmetry of carbon atoms that gives unique properties to graphene [15]. The dispersion relation of graphene was derived long ago in 1947 by Wallace [16] as building block of graphite. As shown in Fig. 1.1(a), the conical band structure of graphene is found by solving the Dirac equation. The conduction and valence bands touch at the charge neutrality or 'Dirac' point. As a result, the term 'semimetal' is used for graphene which shows zero bandgap, and consequently, zero mass of carriers near Dirac point.

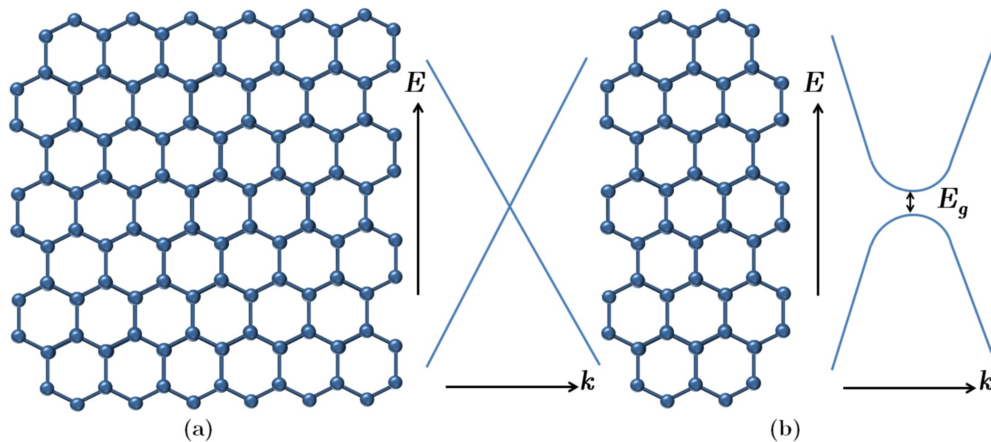


Figure 1.1: Crystal structure and dispersion relation close to the Dirac point of (a) large area graphene and (b) graphene nanoribbon.

1.4 Graphene FETs in Microwave

The good electronic properties of graphene such as high electron mobility, low effective mass, and high carrier saturation velocity make it a promising candidate to produce high frequency and low noise FETs. Moreover, devices with extreme thin channels are achieved due to the atomical thickness of graphene sheets. This can allow the graphene field effect transistor (GFET) to be scaled to very short channel length and high speed without encountering short-channel effect [17], ensuring efficient gate control of the channel. In addition, the compatibility of graphene with silicon technology also makes it attractive for transistors.

In reality, potential applications for graphene are limited to microwave rather than logic circuits in high speed electronics. The reason behind this is that the bandgap of graphene is zero (see Fig. 1.1(a)). FETs with a large-area graphene channel cannot be switched off and as a result power consumption occur even in the off state. Hence, they are not suitable for logic applications. For high frequency applications, a high performance GFET needs to be realised. However, this is not straightforward to accomplish. The challenges arise when graphene is in contact with different layers for manufacturing FETs. For example the process of the gate-dielectric formation degrades the carrier mobility severely, going down to ∼1000-3000 $cm^2/V{\cdot}s$ [18]. Although several methods have been developed to decrease this effect [19, 20] reaching upto 15,000 $cm^2/V{\cdot}s$, the carrier mobility of graphene in GFETs is still far from its potential. Moreover, charge traps at the graphene/dielectric interface introduces hysteresis in GFETs [21, 22]. In addition, high sheet resistivity of graphene degrades the high frequency performance of GFETs by increasing contact and access resistances [23]. Furthermore, zero band gap of graphene becomes problematic also in high frequency application where a small bandgap is required to achieve pinch-off in FETs and enhance operational on-off ratios. To open a bandgap (up to 200 meV) in graphene, quantum confinement can be used, e.g. patterning graphene as nanoribbons (GNR) or in nanoscale structures [24–26] as shown in Fig. 1.1(b). However, rough edges of the GNR results in undesirable FET characteristic and also reducing the width of the nanoribbons gives rise to a parabolic bandstructure which increases the effective carrier mass and thereby decreases the carrier mobility [27].

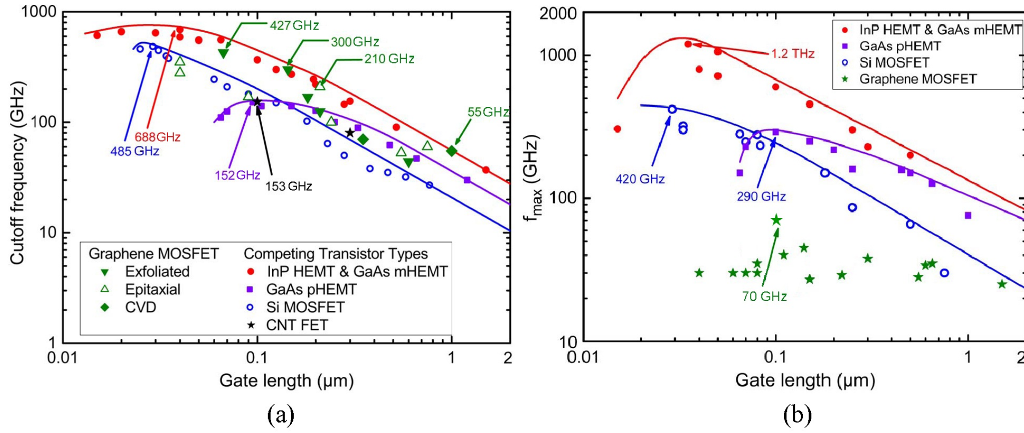


Figure 1.2: (a) f_T of graphene MOSFETs versus L along with f_T performance of the best CNT FET, InP HEMTs, GaAs mHEMTs, GaAs pHEMTs (pseudomorphic HEMT), and Si MOSFETs. (b) f_{max} of graphene MOSFETs versus L along with f_{max} performance of InP HEMTs, GaAs mHEMTs, GaAs pHEMTs, and Si MOSFETs. Updated from [28].

To improve the performance of GFETs the above mentioned obstacles need to be overcome. Numerous efforts have been put towards this goal and hence, the highest intrinsic f_{max} value reported for a GFET is 70 GHz [29] and the highest intrinsic cut-off frequency (f_T) reported is 427 GHz [30] till date. The value of f_{max} is comparatively lower due to the lack of current saturation in GFETs. The frequency performance so far achieved by GFETs is compared with that of competing microwave FETs (HEMT, Si MOSFET) in Fig. 1.2 [28]. From the comparison it is apparent that at present GFETs might only compete with Si MOSFET due to its inferior f_{max} than other technologies.

1.5 Noise in GFETs

Electronic noise or low frequency noise in GFETs have been studied extensively so far in the literature. Phase noise and $1/f$ noise in GFETs have been investigated in [31]. A study of low-frequency noise and hysteresis in GFETs was performed in [32]. However, in the case of noise in RF or microwave frequency range, only the noise characterisation of an amplifier [33] and a resistive subharmonic mixer [34] utilising GFETs have been reported to date. The F_{min} of a 1 μm GFET was predicted in [33] to be $\sim$ 3.3 dB and $\sim$ 1 dB at 1 GHz for

extrinsic and intrinsic device, respectively [35]. Nonetheless, the device level noise characteristic of GFET from direct measurements is still to be reported in the literature. Thus, F_{min} requires to be determined with the highest possible accuracy, which requires source-pull measurements. In addition, such device level noise measurements provide all four noise parameters [35]. This knowledge enables the extraction of a more appropriate noise model, compared to only 50 Ω noise figure. Moreover, it allows the de-embedding of measured noise figure using correlation matrices [36].

1.6 Thesis outline

In this thesis, the noise parameter characterisation of GFETs is performed through source-pull measurements. Chapter 2 layouts the theoretical background required to perform this task. The subsequent chapter deals with the processing and measurement techniques to fabricate the GFETs and measure the relevant DC, small signal and noise properties. Chapter 4 presents the obtained results with extensive discussion on their significance. Finally, concluding remarks of the topic is depicted with possible future work in the last chapter.

Chapter 2

Theoretical Background

In this chapter the theoretical background is built up starting from two-port network system, moving on to field effect transistors, and continuously including the eccentricities of GFETs. Eventually the theoretical basis for intrinsic noise calculation and noise modelling is discussed. In the end, a brief overview of the important figure of merits for FETs is depicted.

2.1 Two-Port System

A microwave transistor can be treated as a two-port network system [37]. Such a system can be described by the measured data of transfer and impedance functions through impedance (Z-parameters), admittance (Y-parameters), hybrid (h-parameters) or the chain (ABCD parameters) matrix. But the determination of these parameters becomes complicated at high frequency since required short and open circuit tests are difficult to achieve over a broadband range of microwave frequencies. The two-port system can be completely characterised in terms of travelling wave in the microwave frequency range through another set of parameters, namely, the scattering matrix (S-parameters). In

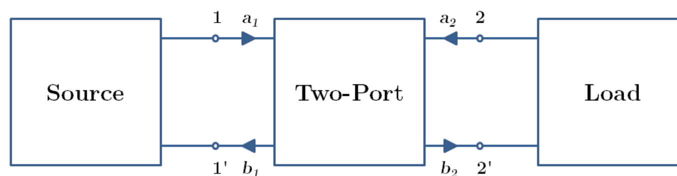


Figure 2.1: Two-port network system

Fig. 2.1 a two-port network characterised by S-parameters is shown. The

scattering matrix for this network can be described as follows:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

In general large values of the 21-parameters are desirable which indicates the transistor's ability to control and amplify input signals [10]. Two other terms, which are useful to define at this point, are the source and load reflection coefficients of the two-port network as follows [37]:

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{2.2a}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.2b}$$

where Z_s and Z_L are the source and load impedances, respectively, and Z_0 is the reference impedance.

2.2 Field Effect Transistors

Field effect transistors are three terminal devices where the conductivity of the channel, namely the region between two of the terminals (source and drain), is controlled by a field bias induced capacitively by the other terminal (gate) [5]. The gate capacitor for FETs can be realised either by an insulating capacitor (metal-insulator-semiconductor FET, MISFET) or by a Schottky barrier junction (metal-semiconductor FET, MESFET) [38]. In MISFET, an insulating barrier can be achieved through an oxide layer (MOSFET) or a large bandgap semiconductor layer (heterojunction FET, HFET). Although the FET channel can be either p-type or n-type depending on the type of carrier being electron or hole, for high frequency applications n-type channel is the most common due to superior electron mobility. Also depending on the state of the channel without any gate bias, the FET can be either enhancement (normally on) or depletion (normally off) mode device. In the current study, the GFETs are essentially MOSFETs. Due to the electron-hole duality in graphene, GFETs can be operated as a p-type or n-type FET depending on the gate voltage.

2.2.1 DC Characteristics

The DC characteristic of a FET is described by the drain current (I_{DS}) vs gate voltage (V_{GS}) (transfer characteristic) and the drain current (I_{DS}) vs drain

voltage (V_{DS}) (output characteristic) behaviour. The output characteristics of a MOSFET can be divided into triode and saturation regions which are defined by the equations [39]:

$$I_{DS} = \mu C_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{ds} - \frac{V_{DS}^2}{2}\right] \quad for\ V_{DS} < V_{GS} - V_{th} \quad [\mathrm{A}] \quad (2.3a)$$

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \quad for\ V_{DS} > V_{GS} - V_{th} \quad [\mathrm{A}] \quad (2.3b)$$

where μ = mobility, C_{ox} = gate oxide capacitance per area, W = channel width, L = channel length, and V_{th} = threshold voltage. The ideal DC characteristics of a n-type enhancement mode MOSFET are shown in Fig. 2.2.

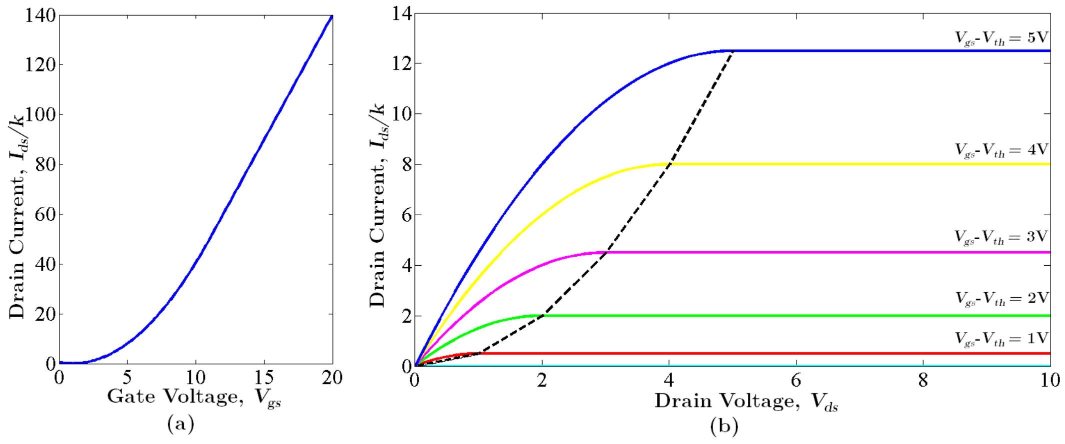


Figure 2.2: (a)Transfer characteristic at V_{DS} = 10 V and (b)output characteristics of MOSFET, $k = \mu C_{ox}\frac{W}{L}$. The dashed line separates the triode and saturation region.

In the case of a GFET, the DC transfer characteristic can be described by the following equation with highest accuracy away from the Dirac point where only one carrier type contributes to the current [19]:

$$\begin{aligned} R_{DS} &= \begin{cases} (R_s + R_d) + R_{ext} + \frac{L}{Wq\mu_e\sqrt{n^2+n_0^2}} & \text{for electron} \\ (R_s + R_d) + \frac{L}{Wq\mu_h\sqrt{n^2+n_0^2}} & \text{for hole} \end{cases} & [\Omega] \\ n &= \frac{C_{gate}}{q}(V_{gs} - V_{dirac}) & [\mathrm{cm}^{-2}] \quad (2.4) \\ C_{gate} &= \left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right)^{-1} & [\mathrm{F/cm}^2] \end{aligned}$$

where R_{DS} is drain to source resistance, R_s and R_d are source and drain contact resistances, R_{ext} is an extra resistance arising from p-n barrier formation due to opposite type of carrier in the GFET channel and the carrier type transferred during ohmic contact formation [40], q is the charge of electron, $\mu_{e,h}$ are electron and hole mobilities, n_0 is the residual carrier density, V_{dirac} is the voltage at maximum R_{DS}, and C_{gate} is the gate capacitance which consists of oxide capacitance, C_{ox} and quantum capacitance, C_q. C_q arises from the residual charge density at Dirac point [27], and needs to be considered only in the case of ultra-thin gate oxide [41].

The two important parameters which can be deduced from DC characteristics are transconductance, g_m and output conductance, g_d. They are the slopes of the transfer and output characteristics, respectively and can be expressed as follows:

$$g_{m,ex} = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const} \quad [\mathrm{S}] \tag{2.5}$$

$$g_{d,ex} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=const} \quad [\mathrm{S}] \tag{2.6}$$

The '*ex*' subscript denotes that the values are obtained from the measured slopes of DC characteristics, and are extrinsic values which include the effects of parasitics. The intrinsic parameters, $g_{m,in}$ and $g_{d,in}$, can be extracted via small signal models as will be described in the following section 2.2.2. A high input transconductance denotes high degree of gate control on the channel and is beneficial for good frequency performance. On the contrary, low output conductance is essential for voltage and power gain in FETs and can be obtained through current saturation at the output.

However, in GFETs, due to the high contact and access resistances there is a considerable difference between the intrinsic and extrinsic g_m and g_d. For the same reason, GFETs with a long gate length, L>1-2 μm generally exhibit a higher $g_{m,ex}$ [42] than shorter gate-length devices, L<200 nm. Moreover, because of the nonuniformity of CVD and epitaxial graphene, GFETs fabricated using these materials have lower $g_{m,ex}$ per channel width in comparison to GFETs with mechanically exfoliated graphene at a certain V_{DS}. Conversely, high frequency operation relies on short gate length devices which means GFETs should respond quickly to gate variations. Therefore, it is necessary to enhance $g_{m,ex}$ for short gate length devices. On the other hand, due

to the lack of bandgap, GFETs generally exhibit lack of current saturation and consequently high output conductances [43, 44].

2.2.2 Small Signal FET Model

Small signal amplifier is among the most common uses of a microwave FET. The small signal equivalent circuit of a GFET is shown in Fig. 2.3 which is similar to a standard FET equivalent circuit. The substrate leakage resistances through gate and drain pads, R_{pg} and R_{pd}, arise from the insufficiently insulating silicon substrate used in this work. Generally they are omitted in other technologies due to the use of insulating or semi-insulating substrates such as GaAs, InP etc. The intrinsic part of the device is marked by a dashed rectangle.

Analytical expressions for the intrinsic Y-parameters of the small signal model have been derived as following [45]:

$$Y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \qquad \text{[S]} \qquad (2.7a)$$

$$Y_{12} = -j\omega C_{gd} \qquad [S] \qquad (2.7b)$$

$$Y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \qquad \text{[S]} \qquad (2.7c)$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega(C_{ds} + C_{gd}) \qquad \text{[S]} \qquad (2.7d)$$

$$D = 1 + \omega^2 C_{gs}^2 R_i^2 \qquad (2.7e)$$

where $g_m = g_{m,in}$. As stated earlier in section 2.2.1, the intrinsic g_m and g_d can be obtained utilising the extrinsic values using the relations [46]:

$$g_{m,in} = \frac{g_{m,ex}}{1 - R_s g_{m,ex} - (R_s + R_d) g_{d,ex}} \qquad \text{[S]} \qquad (2.8)$$

$$g_{d,in} = \frac{g_{d,ex}}{1 - R_s g_{d,ex} - (R_s + R_d) g_{m,ex}} \qquad \text{[S]} \qquad (2.9)$$

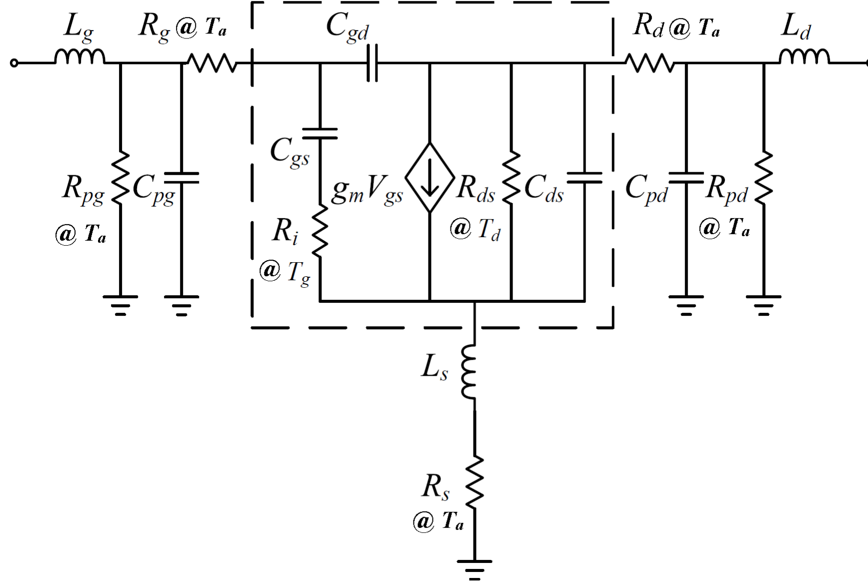


Figure 2.3: Small signal equivalent circuit of the GFET.

From Eq. 2.7 intrinsic elements of the small signal model can be obtained through the expressions [47]:

$$C_{gd} = \frac{-\operatorname{Im}(Y_{12})}{\omega} \quad [\mathrm{F}] \tag{2.10a}$$

$$C_{gs} = \frac{\operatorname{Im}(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{\operatorname{Re}(Y_{11})^2}{(\operatorname{Im}(Y_{11}) - \omega C_{gd})^2}\right) \quad [\mathrm{F}] \tag{2.10b}$$

$$R_i = \frac{Re(Y_{11})}{(\operatorname{Im}(Y_{11}) - \omega C_{gd})^2 + \operatorname{Re}(Y_{11})^2} \quad [\Omega] \tag{2.10c}$$

$$g_m = \sqrt{(\operatorname{Re}(Y_{21})^2 + (\operatorname{Im}(Y_{21}) + \omega C_{gd})^2)\,(1 + \omega^2 C_{gs}^2 R_i^2)} \quad [\mathrm{S}] \tag{2.10d}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \operatorname{Im}(Y_{21}) - \omega C_{gs} R_i \operatorname{Re}(Y_{21})}{g_m}\right) \quad [\mathrm{S}] \tag{2.10e}$$

$$C_{ds} = \frac{\operatorname{Im}(Y_{22}) - \omega C_{gd}}{\omega} \quad [\mathrm{F}] \tag{2.10f}$$

$$g_d = \operatorname{Re}(Y_{22}) = \frac{1}{R_{ds}} \quad [\Omega] \tag{2.10g}$$

2.2.3 Parasitic Extraction and De-embedding Techniques

De-embeddding procedure for FETs was introduced in [48]. To de-embed the GFET towards obtaining the intrinsic Y-parameters in Eq. 2.7, the para-

sitic components as shown in Fig. 2.3 need to be extracted. To begin with, the source and drain contact resistances can be expressed as $R_s = R_d = R_a + R_{m-g}$ where $R_a = R_{sheet}L_a/W$ is the resistance coming from the ungated access region and $R_{m-g} = \rho_c/W$ is the metal to graphene contact resistance. R_s and R_d can be considered to be equal if the fabricated GFET has a symmetric device layout. It is possible to obtain the values of R_s and R_d from the fit of the Eq. 2.4 with measured DC transfer characteristics. For more accurate determination of these resistances, 4-point transmission line model (TLM) measurement technique [49, 50] can be utilised. The technique involves making a series of metal-semiconductor, or in this case metal-graphene, contacts separated by various distances (L_c). Two probes are applied to each contact, and the resistance between them is measured by driving a current through the metal-graphene junctions by one pair of the contacts and measuring voltage across them using the other pair. The total measured resistance can be written as:

$$R_{tot} = 2R_c + R_{sheet}\frac{L_c}{W_c} \qquad [\Omega] \qquad (2.11)$$

where R_c ($= \rho_c/W_c$) is the metal-graphene contact resistance for each contact, R_{sheet} is the sheet resistance of graphene in-between the contacts and W_c is the width of the contacts. Consequently, a linear plot of R_{tot} versus L_c can be obtained from several such measurements of contact pairs that are separated by different L_c. The intercept of the line with Y-axis will be $2R_c$ and the slope will be R_{sheet}/W_c. In this method, the specific contact resistivity and sheet resistance are measured without any effect from the underlying semiconductor or the contacting metal conductor.

The ohmic resistance of the gate can be described by a quantity called dc end-to-end resistance which can be expressed by the following equation for a rectangular gate [10]:

$$R_{g,dc} = \rho_g\frac{W}{Lh} \qquad [\Omega] \qquad (2.12)$$

where ρ_g is the resistivity of the gate material and h is the height of the gate. For a multifinger MOSFET, the gate resistance, R_g within small-signal consideration can be determined from the expression [10]:

$$R_g = \rho_g\frac{W_f^2}{3WLh} \qquad [\Omega] \qquad (2.13)$$

where W_f is the gate finger width . The factor 3 in the denominator of Eq. 2.13 arises from the fact that when gate voltage varies, charges move in and out of the gate but not all charges have to move from the feed point to the very end of the gate due to their distributed nature.

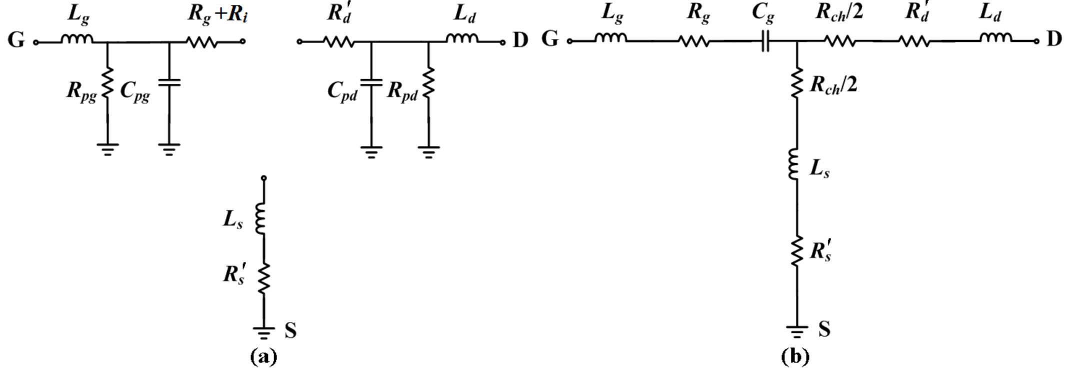


Figure 2.4: Small signal equivalent circuit of the (a) open and (b) short structures.

The remaining parasitic components of the GFET can be extracted through separate open and short structures of same layout, since it is not possible to completely turn on/off the graphene channel as conventional FETs. Using the equivalent circuits of these structures, as shown in Fig. 2.4, the values of the parasitic components can be calculated. In the figure, the parameters R_s' and R_d' are the resistances from source and drain metals and R_{ch} is the shorted channel resistance. According to the extraction technique described in [51] the parasitic inductances can be obtained using the Z-parameters of the short structure as follows:

$$L_s = \text{Im}(Z_{12,short}) \qquad [\text{H}] \qquad (2.14a)$$

$$L_d = \text{Im}(Z_{22,short}) - L_s \qquad [\text{H}] \qquad (2.14b)$$

$$L_g = \frac{\omega_x \,\text{Im}(Z_{11,short,x}) - \omega_y \,\text{Im}(Z_{11,short,y}) - (\omega_x^2 - \omega_y^2) L_s}{\omega_x^2 - \omega_y^2} \qquad [\text{H}] \qquad (2.14c)$$

where subscripts x and y denote values of two different frequency points. The inductances are then subtracted from the Z-matrix of the open structure. Consequently the parasitic capacitances and resistances can be extracted from the

Y-parameters of the open structure using the expressions:

$$C_{pg} = \frac{\mathrm{Im}(Y_{11,open})}{\omega} \qquad [\mathrm{F}] \qquad (2.15a)$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{22,open})}{\omega} \qquad [\mathrm{F}] \qquad (2.15b)$$

$$G_{pg} = \mathrm{Re}(Y_{11,open}) = \frac{1}{R_{pg}} \qquad [\Omega] \qquad (2.15c)$$

$$G_{pd} = \mathrm{Re}(Y_{22,open}) = \frac{1}{R_{pd}} \qquad [\Omega] \qquad (2.15d)$$

From the extrinsic GFET, the parasitics are subsequently de-embedded following a similar method as depicted in [45] to obtain the intrinsic Y-parameters. Afterwards, the intrinsic components of the small signal model are calculated using Eq. 2.10.

2.3 Noise

As described in section 1.2, there can be different sources of noise in a microwave FET. But for determining the noise parameters of the GFETs in the present study, considering only thermal noise is sufficient as will be apparent in the coming chapters. Thermal noise in microwave FETs can be described by equivalent noise temperatures of different resistive elements. A noisy resistor can be modelled by a noiseless resistor and a noise voltage with root mean square (RMS) value of:

$$v_n = \sqrt{4kTBR} \qquad [\mathrm{V}] \qquad (2.16)$$

where k is the Boltzmann constant, T is the resistor noise temperature, and B is the noise bandwidth [37]. The available noise power is then $P_N = v_n^2/4R = kTB$. This concept is utilised to quantify the noise performance of a microwave FET.

2.3.1 Noise Parameters

The noise figure of a microwave FET is defined as the ratio of the total available noise power at the output to the available noise power at the output due to thermal noise from input termination R which is at $T = T_0 = 290$ K [37]. In

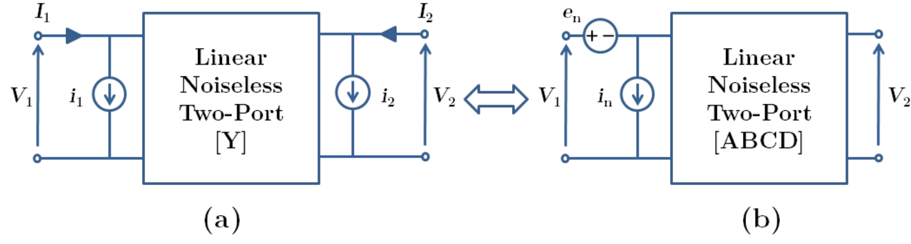


Figure 2.5: Noise representation in two port network by (a) current source at input and output and (b) voltage and current source at input.

other words it can also be expressed as the degradation of signal-to-noise power ratio from input to output as follows:

$$F = \frac{P_{S,in}/P_{N,in}}{P_{S,out}/P_{N,out}} > 1 \qquad [\text{dB}] \tag{2.17}$$

It is also possible to describe the noise performance of a transistor by a set of four parameters. Knowing the value of these parameters is sufficient for determining the noise figure. This set of parameters can be represented in different forms depending on how the noise in a two-port network is presented. For admittance representation as in Fig. 2.5(a) the noise parameters are [35]:

$$G_1 = \frac{\overline{|i_1^2|}}{4kT_0B} \qquad G_2 = \frac{\overline{|i_2^2|}}{4kT_0B} \qquad \rho_{corr} = \frac{\overline{i_1^* i_2}}{\sqrt{\overline{|i_1|^2}\,\overline{|i_2|^2}}} \tag{2.18}$$

where ρ_{corr} ($= |\rho_{corr}|e^{\phi_{corr}}$) represents correlation coefficient between the noise sources at the input and output of the two-port network. For ABCD-matrix representation as in Fig. 2.5(b) the noise parameters are [35]:

$$R_n = \frac{\overline{|e_n^2|}}{4kT_0B} \qquad g_n = \frac{\overline{|i_n^2|}}{4kT_0B} \qquad \rho = \frac{\overline{e_n^* i_n}}{\sqrt{\overline{|e_n|^2}\,\overline{|i_n|^2}}} \tag{2.19}$$

where R_n is noise resistance and g_n is noise conductance. But the most useful representation for describing noise parameters of FETs consists of minimum noise temperature (T_{min}), optimal source impedance ($Z_{opt} = R_{opt} + jX_{opt}$) and g_n. According to this representation the noise temperature of a two port network is:

$$T_n = T_{min} + T_0\frac{g_n}{R_s}|Z_s - Z_{opt}|^2 \qquad [\text{K}] \tag{2.20}$$

where $Z_s = R_s + jX_s$ is the source impedance.

2.3.2 Noise Correlation Matrix

To evaluate the intrinsic noise performance of the device, intrinsic noise parameters need to be known through de-embedding of parasitic noise contribution. This can be performed by following the noise correlation approach in [36] where the noise correlation matrix of the parasitic network (C_P) is de-embedded from the noise correlation matrix of the extrinsic device (C_{PD}) to calculate the noise correlation matrix of the intrinsic device (C_D). In ABCD representation the noise correlation matrix of the intrinsic device can be expressed as [36]:

$$C_D = \begin{pmatrix} R_n & \frac{T_{min}}{2T_0} - R_n Y_{opt}^* \\ \frac{T_{min}}{2T_0} - R_n Y_{opt} & R_n Y_{opt}^2 \end{pmatrix} \tag{2.21}$$

where $Y_{opt} = G_{opt} + jB_{opt} = 1/Z_{opt}$.

2.3.3 Pospieszalski Noise Model

The noise from the intrinsic device can be divided into drain thermal noise and induced gate noise. The gate noise is also interpreted as thermal and uncorrelated with the drain noise in the Pospieszalski two temperature noise model [35]. This model has been verified for both HEMTs and MOSFETs. The two noise temperatures T_d of g_{ds} (representing the intrinsic channel noise) and T_g of R_i of this model can be obtained through optimisation to the intrinsic noise parameters. In addition, for the Pospieszalski model to be valid for a certain device the following condition needs to be fulfilled [35]:

$$1 \leq \frac{4NT_0}{T_{min}} < 2 \tag{2.22}$$

where $N = G_{opt}R_n$. In [35], C_{gd} is not included in the derivation of noise parameters. As a first hand approximation, without including C_{gd}, the obtained noise correlation matrix of the intrinsic device can be expressed in admittance form as [52]:

$$C_Y = \begin{pmatrix} \langle i_1^2 \rangle & \langle i_1 i_2^* \rangle \\ \langle i_1^* i_2 \rangle & \langle i_2^2 \rangle \end{pmatrix} \tag{2.23}$$

where the elements are:

$$\begin{aligned}
\langle i_1^2 \rangle &= 4kT_g BR_i \left| \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_i} \right| \\
\langle i_2^2 \rangle &= 4kBR_i \left(T_d \frac{1}{R_{ds}} + T_g R_i \left| \frac{g_m}{1 + j\omega C_{gs} R_i} \right|^2 \right) \\
\langle i_1 i_2^* \rangle &= 4kT_g B \frac{g_m^* j\omega C_{gs} R_i}{|1 + j\omega C_{gs} R_i|^2}
\end{aligned} \quad (2.24)$$

But to utilise the Pospieszalski noise model [35] for the intrinsic GFET in Fig. 2.3, C_{gd} needs to be included into the noise parameters. This can be accomplished algebraically by following the procedure as described in [53]. The obtained noise parameters including C_{gd} are:

$$T_{min} = \frac{2}{|A|^2} \left(\sqrt{PQ - \mathrm{Im}(H)^2} + \mathrm{Re}(H) \right) \quad [\mathrm{K}] \quad (2.25a)$$

$$g_n = \frac{P}{T_0 |A|^2} \quad [\mathrm{S}] \quad (2.25b)$$

$$Z_{opt} = \frac{1}{P} \left(\sqrt{PQ - \mathrm{Im}(H)^2} + j\,\mathrm{Im}(H) \right) \quad [\Omega] \quad (2.25c)$$

where

$P = \frac{T_d}{R_{ds}} \left[\frac{\omega^2 (C_{gd} + C_{gs})^2}{R_i^2} + \omega^4 C_{gd}^2 C_{gs}^2 \right] + \frac{T_g}{R_i} (\omega^4 C_{gd}^2 C_{gs}^2 + \omega^2 g_m^2 C_{gd}^2)$

$Q = T_g \frac{g_m^2}{R_i} + \frac{T_d}{R_{ds}} \left(\frac{1}{R_i^2} + \omega^2 C_{gs}^2 \right)$

$H = -T_g \frac{g_m}{R_i} \left[\omega^2 C_{gd} C_{gs} - j\omega g_m C_{gd} \right] - \frac{T_d}{R_{ds}} \left[\frac{1}{R_i} - j\omega C_{gs} \right] \left[\omega^2 C_{gd} C_{gs} - \frac{j\omega}{R_i} (C_{gd} + C_{gs}) \right]$

$A = \frac{j\omega}{R_i} C_{gd} - \omega^2 C_{gd} C_{gs} - \frac{g_m}{R_i}$

Using Eq. 2.25, the noise temperatures, T_d and T_g, can be obtained by following an optimisation procedure as indicated in [35].

2.4 FET Figure of Merits

The figures of merit for microwave FETs are stability, maximum stable and maximum available gain, cut-off frequency (f_T), maximum frequency of oscillation (f_{max}), minimum noise figure (F_{min}) etc. The high frequency performance is mainly benchmarked by f_T and f_{max} and the noise performance by F_{min}.

2.4.1 Stability and Gain

In applications of FETs as amplifiers, oscillation is not desired. A transistor is unconditionally stable i.e. not prone to oscillation at any source and load

impedances, if it fulfils the following necessary and sufficient conditions:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.26}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.27}$$

If K<1, the transistor is said to be potentially unstable and a simultaneous conjugate match for maximum available gain does not exist.

At low frequency using a simplified small signal model for GFET where the contact resistances, R_s and R_d, are included in $g_{m,ex}$ and $g_{d,ex}$ respectively and the frequency dependent elements are ignored, the gain can be written as:

$$S_{21} = -\frac{2Z_0 g_{m,ex}}{Z_0 g_{d,ex} + 1} \quad \text{[dB]} \tag{2.28}$$

The explanation of the terms $g_{m,ex}$ and $g_{d,ex}$ are given in section 2.2.1 with Eqs. 2.5 and 2.6, respectively. From Eq. 2.28 it is clear that, a high g_m and a low g_d is necessary for achieving high gain.

Different definition of gain exists depending on the input and output reference planes in a two-port network. The transducer power gain, G_t, is defined as the ratio between the power delivered to the load and the power available from the source which can be expressed as follows [37]:

$$G_T = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{in}\Gamma_s|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad \text{[dB]} \tag{2.29}$$

where

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.30}$$

Available power gain is the ratio between the power available at the output of the transistor and the source which can be derived as [54]:

$$G_A = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1}{1 - |\Gamma_{out}|^2} \quad \text{[dB]} \tag{2.31}$$

where

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{2.32}$$

In relation with stability concern, the maximum stable gain of a ťpotentially unstable transistor is defined as [37]:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \tag{2.33}$$

2.4.2 Cut-off Frequency and Maximum Frequency of Oscillation

The cut-off frequency is the frequency at which the short-circuit current gain (h_{21}) is unity (or 0 dB) which can be calculated from the S-parameters using the expression [38]:

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \qquad [\text{dB}] \qquad (2.34)$$

The analytical expression for f_T can be obtained in terms of the elements in Fig. 2.3 as follows:

$$f_T = \frac{g_m}{2\pi((C_{gs}+C_{gd})(1+g_d(R_d+R_s)R_{ds})+C_{gd}g_m(R_d+R_s)+C_{pg})} \qquad [\text{Hz}] \qquad (2.35)$$

In an ideal scenario where the parasitics can be neglected, this expression can be simplified as:

$$f_T \simeq \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad [\text{Hz}] \qquad (2.36)$$

On the other hand, f_{max} is the frequency at which the unilateral or Mason's power gain [55] becomes unity (or 0 dB). The unilateral power gain can be calculated as:

$$U = \frac{|S_{21}-S_{12}|^2}{\det\left[I-SS^*\right]} \qquad [\text{dB}] \qquad (2.37)$$

The f_{max} can be expressed analytically in terms of f_T by the equation:

$$f_{max} = \frac{f_T}{2\sqrt{g_{d,in}(R_g+R_s+R_i)+2\pi R_g C_{gd} f_T}} \qquad [\text{Hz}] \qquad (2.38)$$

Thus, it is apparent that for a high f_{max}, the gate resistance needs to be reduced. It is also necessary to have good current saturation to achieve a high f_{max}.

2.4.3 Minimum Noise Figure

An amplifier amplifies both signal and noise coming to its input being unable to distinguish between them. In addition to that it also has some intrinsic noise. Noise figure helps to quantify the amount of intrinsic noise produced by a FET and thus it becomes an important figure of merit for the transistor.

The magnitude of noise figure depends on the matching condition at the input, bias condition and frequency. The noise figure obtained from the FET biased and matched for minimum noise ($Z_s = Z_{opt}$) is called the minimum noise figure (F_{min}). At this point the noise source reflection coefficient also becomes optimum ($\Gamma_s = \Gamma_{opt}$). The noise figure of a two port amplifier can be described by these noise parameters by the expression:

$$F = F_{min} + \frac{4r_n|\Gamma_s - \Gamma_{opt}|^2}{(1 - |\Gamma_s|^2)|1 + \Gamma_{opt}|^2} \qquad \text{[dB]} \tag{2.39}$$

where $r_n = R_n/Z_0$ is the equivalent normalised noise resistance. Consequently F_{min} is analogous to T_{min} by the relation:

$$F_{min} = \frac{T_{min}}{T_0} + 1 \qquad \text{[dB]} \tag{2.40}$$

The power gain at this minimum noise condition is called the associated gain (G_a) which can be obtained from Eq. 2.31 by setting $\Gamma_s = \Gamma_{opt}$.

Chapter 3

Processing and Measurement Techniques

In this chapter, the processing and fabrication details of the GFETs are discussed. Additionally, the methods followed for device optimisation, characterisation, and parameter extraction are also introduced.

3.1 Device Fabrication

For GFET fabrication, initially mechanically exfoliated and later on CVD graphene was used. Although exfoliated graphene is still better in quality, it is not suitable for fabrication on a large scale. For different stages of the device optimisation mainly mechanically exfoliated graphene was utilised. The devices used for actual measurement were fabricated using CVD graphene.

3.1.1 CVD Graphene

The chemical vapour deposition process described in [56] was used for growing graphene. Graphene was transferred onto SiO_2 (300 nm)/Si substrate following the bubbling transfer procedure as in [57].

Graphene Synthesis

Graphene was produced in a cold-wall low-pressure CVD system specially designed for carbon nanomaterial deposition (Black Magic, AIXTRON Nanoinstruments Ltd.), as illustrated in Fig. 3.1. The samples were directly clamped

onto a low-mass Joule heater which is capable of rapid thermal ramp rates. The temperature was measured by a thermocouple (TC) contacting the heater. In this process, graphene was grown on 25μm-thick copper (Cu) foil (99.9%, GoodFellow) which works as the catalyst. The gas mixture was premixed and introduced uniformly across the substrate surface by a quartz shower head. The main precursor gas was a high purity methane (CH_4) (99.9995%) prediluted with Ar to 5%. By the virtue of having only one C atom per molecule and a high decomposition temperature [58], CH_4 is advantageous to be used as the precursor and provides the best graphene quality. The Cu foils were first cleaned in acetic acid, acetone, and isopropanol to remove the native oxides and organic contaminations. Afterwards, they were heated to 1000°C at 300°C/min and annealed for 5 min, under a flow of 20 sccm hydrogen (H_2) and 1000 sccm argon (Ar) to remove any residuals not removed in wet cleaning and increase grain size of Cu for better graphene quality. Subsequently, 30 sccm prediluted CH_4 was introduced into the chamber to initiate graphene growth. The partial pressure P_{CH_4} was 9×10^{-3} mbar at the total pressure P of 6.35 mbar. This partial pressure corresponds to 150 graphene layers grown per second assuming the 100% efficiency of CH_4 decomposition and C sticking to the surface. But the growth on Cu foil is a self-limiting process where 95% is single layer graphene [59]. The three gases were stopped after 5 min of deposition and the system was evacuated to < 0.1 mbar. In the end, the samples were cooled at 300°C/min to room temperature under 20 sccm H_2 and 1000 sccm Ar.

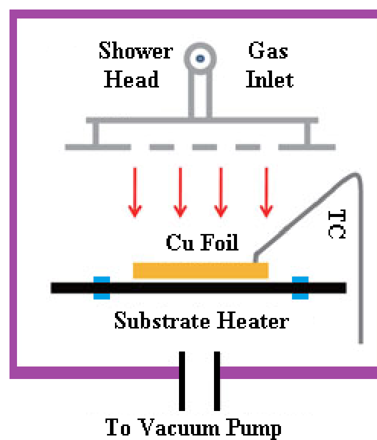


Figure 3.1: Schematic of the cold-wall CVD system. [56]

Graphene Transfer

The transfer procedure is illustrated in Fig. 3.2. First, poly(methyl methacrylate) (PMMA) A4 resist (1000 rpm, 1 min, cure at 160°C for 5 min) was spin coated on graphene on top of the Cu foil so that the resist works as the supporting polymer thin film. For the supporting frame, 100-200 μm thick polyethylene terephthalate (PET) thermal releasing tape was used, even though any semi-rigid plastics that are inert during the electrolysis would be suitable. Some resist was put around the PET frame for gluing. It was then attached to the resist/graphene/Cu foil stack on a hot plate at 160°C. Subsequently, the frame/PMMA/graphene/Cu-bundle was used as the cathode of an electrolytic cell with a solution made from 25 ml NaOH and 20 ml H_2SO_4 in 1000 ml H_2O. A platinum electrode was used (see Fig. 3.2(b)) as the anode. To start the process, the current was ramped to $\sim$ 1A and maintained at that level until the graphene was completely separated from the Cu foil by the H_2 bubbling. The typical time required for separation is around few minutes. The separation was accelerated by clearing the resist from the edges by a sharp object. After separation, the frame/PMMA/graphene-bundle was picked up and rinsed in several deionised water baths. It was then placed on the target substrates (e.g., Si with 300 nm SiO_2) and left at room temperature until it gets dry. The frame was easily removed simply by cutting through the PMMA at the inside borders (Fig. 3.2(c)). Afterwards, the samples were baked at 160°C for 5 mins to remove water residue and improve adhesion. In the end the PMMA film was dissolved by acetone.

3.1.2 GFET Fabrication

Four steps of electron beam (e-beam) lithography was used to fabricate the GFET. The step by step GFET fabrication procedure is shown by schematic diagram in Fig. 3.3 and described briefly as following.

- Double resist layers consisting of 400 nm thick MMA EL10 (developer MIBK:IPA 1:1) and 120 nm thick ZEP520A 1:1 Anisole (developer Hexyl Acetate) is used to facilitate lift-off of evaporated metal (Fig. 3.3(a)). In the first e-beam step source/drain contacts are patterned (Fig. 3.3(b)). Source/drain metallisation is done using 1 nm Ti/15 nm Pd/100 nm Au

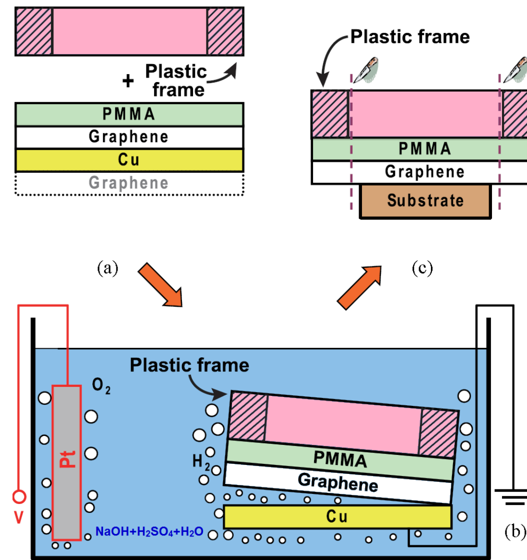


Figure 3.2: Schematic illustration of the frame assisted H_2 bubbling transfer. (a) Gluing of the plastic frame on top of the sample with PMMA A4 resist. (b) Separation of the frame/PMMA/graphene from the Cu foil by H_2 bubbles induced by electrolysis of H_2O. (c) Removal of the frame after transferring graphene on desired substrate. [57]

evaporation by electron beam (Fig. 3.3(b)) and lifted off. Afterwards, graphene is annealed in 1000 sccm Ar-flow at 230°C.

- Subsequently, two 1 nm thick Al layer was evaporated all over the chip and oxidised on a hotplate at 170°C for 5 mins (Fig. 3.3(c)).
- Negative resist ma-N 2405 (developer ma-D 525) is used in the next e-beam step. Mesas were patterned just to cover the area where the active device will be and oxide was etched by HCl (10 s/nm). Afterwards, graphene was removed from all other places by 20 s oxygen plasma etch (Fig. 3.3(d)). The alignment is crucial to minimise gate leakage current and also for drain-source current I_{DS} to flow only through the channel and in turn increase transconductance g_m.
- The 1 nm Al evaporation and oxidation step was repeated five times so that the total thickness of the Al_2O_3 gate oxide is $\sim$ 10 nm (Fig. 3.3(e)).
- Gate fingers were patterned in the subsequent e-beam step with some larger square patterns on both ends of the fingers so that the gate stack

does not collapse after metallisation. As gate stack, 10 nm Ti and 300 nm Au was evaporated and lifted off (Fig. 3.3(f)).

- In the last e-beam step, larger source/drain/gate pads for probing were patterned. First oxide was etched from the overlap area of the smaller contacts using HCl. Subsequently, 10 nm Ti/305 nm Au was evaporated and lifted off (Fig. 3.3(g)).

The SEM image of a final device is shown in Fig. 3.4 along with a zoomed in image of the active region. The gate length of the GFET is $L = 1$ μm and width is $W = 2 \times 30$ μm. The drain length is 20 μm. The access distance between gate fingers and source/drain contact is $L_a = 100$ nm. Two chips with 128 GFETs were fabricated and used for measurements.

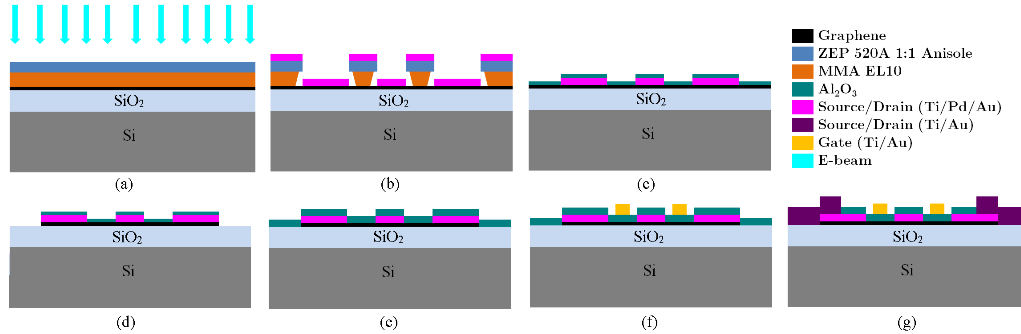


Figure 3.3: Schematic of the GFET fabrication steps.

3.2 Device Optimisation

For accurate noise characterisation at device level, certain device parameters and performance need to be optimised. This includes minimising p-type doping of graphene, gate leakage, contact resistance etc. The measures taken to achieve each of these performance goals are described briefly below.

3.2.1 Annealing

Unintentional p-type doping of graphene by fixed charge from various sources results in an increase in carrier scattering, reducing the field effect mobility of graphene [60]. Moreover, the operating gate voltage is usually chosen at a

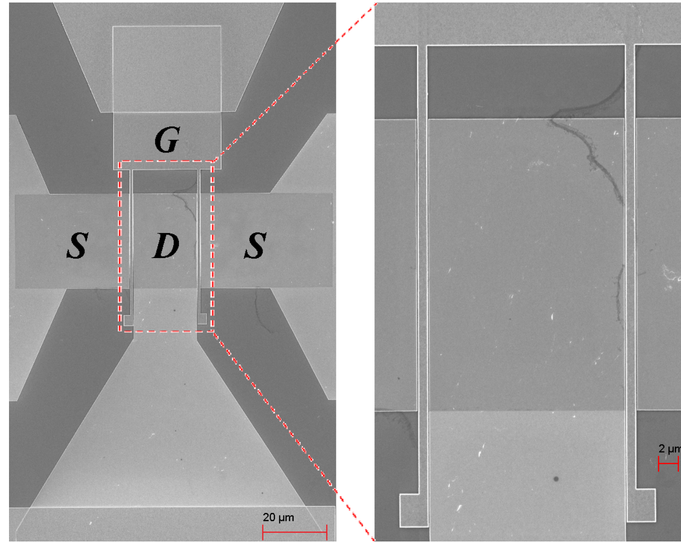


Figure 3.4: (a) SEM image of the complete GFET (scale bar 20 μm) and zoomed image of the active region (scale bar 2 μm), $L = 1$ μm, $W = 60$ μm.

certain level where the GFET provides maximum g_m and also sustain without the gate dielectric breaking down. For this reason, it is essential to have the Dirac point of the graphene close to 0 V i.e. to minimise the p-type doping of graphene. Graphene can become unintentionally doped once it comes in contact with the atmospheric O_2 and H_2O [61], resist (PMMA) [60,62], solvents [63] and also through charge transfer from the SiO_2 substrate [64]. In the initial processing steps, it is not fully possible to prevent the graphene surface from being exposed in the ambient atmosphere. Annealing is one of the ways for reducing the doping effect from other sources. It is especially required to reduce p-type doping from PMMA in different processing steps, although complete removal is not possible [62].

As mentioned in section 3.1.2, after the first source and drain lift off step, annealing is performed. Different annealing temperature (200°C, 250°C, 300°C) and gas (Ar, N_2) was used with several GFETs using exfoliated graphene. The transfer characteristic in three different annealing condition is shown in Fig. 3.5. As mentioned in [62], higher-temperature annealing (>250°C) does not really yield a much cleaner surface, but at the risk of structural damages when graphene is free-standing. Although in our case graphene is not free standing but the charge transfer from SiO_2 substrate might increase at higher temperature [64]. For this reason annealing in Ar flow at 230°C was used finally.

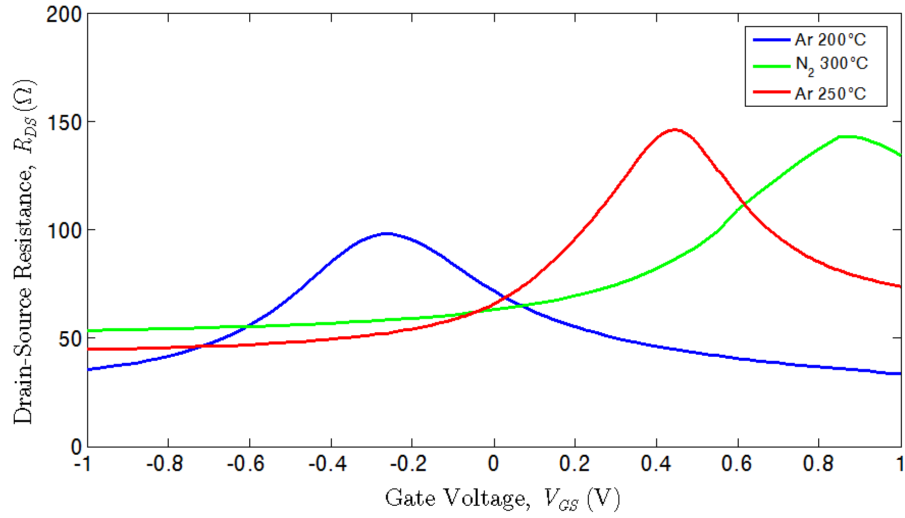


Figure 3.5: Transfer Characteristics of GFETs with different annealing treatment.

3.2.2 Gate Leakage

Leakage current through gate oxide needs to be minimised so that shot noise contribution becomes negligible at measured noise level. For this purpose, the oxide quality needs to be improved at the same time minimising the carrier mobility degradation in graphene as much as possible. Several gate dielectrics were compared in terms of their κ-value and resulting mobility in graphene after top-gate dielectric formation in GFETs in [65]. From this comparison Al_2O_3 seemed to provide reasonable trade-off. For this reason in this study, layer-by-layer deposition of Al_2O_3 was used.

The leakage current per area for MOS capacitors with various thickness of Al_2O_3 including 3×2 nm, 4×2 nm, 4×1.5 nm, 4×1 nm and 10×0.5 nm is shown in Fig. 3.6. It can be clearly seen that thinner oxidation thickness provides lower leakage current value. The reason behind this is, once the native oxide is formed on the top of the Al-layer it does not penetrate further inside. As a result thicker Al-layers are not fully oxidised which gives rise to a metal/oxide layer instead of a full oxide layer. Such alternative metal/oxide layers result in leakage through Ohmic conduction. On the other hand, too thin deposition thickness results in island formation instead of a continuous Al film which degrades the oxide quality and increases leakage, as can be seen in the case of 10×0.5 nm thick Al_2O_3. Within the possible gate voltage operating range,

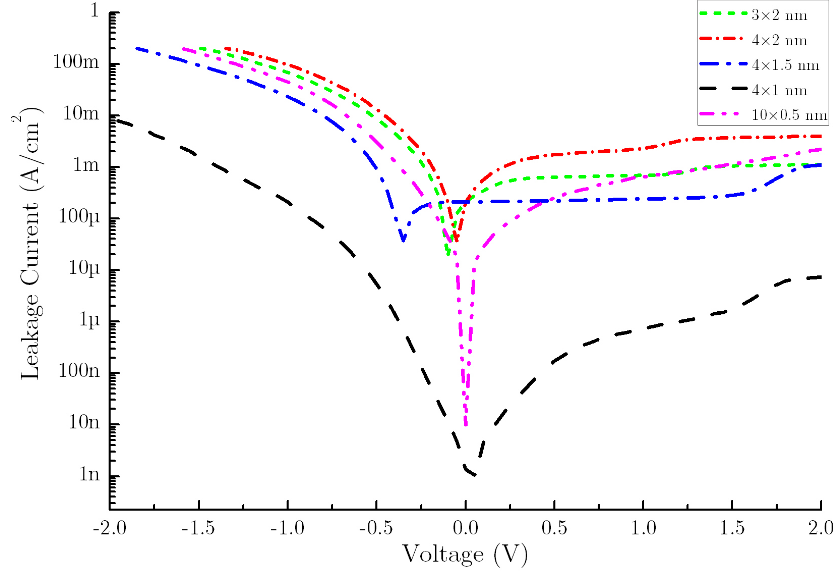


Figure 3.6: I-V Characteristics of MOS capacitors with varying thickness of Al_2O_3.

which should be low for thin oxide (-1 V to 1 V), Al_2O_3 with 4×1 nm thickness gives three orders of magnitude improvement in the leakage current. So the MOS capacitor with 1 nm oxidation layer was chosen for GFET fabrication. As mentioned in section 3.1.2, 7×1 nm Al_2O_3 was used. The first two layers were deposited to protect the graphene during mesa formation, and subsequently, five more layers were deposited with an optimum deposition time and oxide thickness. With 60 μm^2 gate area, the total gate leakage at -1 V will be in the order of 1 nA. Whereas in comparison, at optimum low noise bias, the InP HEMT exhibits a gate current density of 200 nA/mm at 300 K, which is considered to be very low [66]. This is equivalent to a total leakage current of 12 nA for 60 μm gate width.

3.2.3 Contact Resistance

Another important issue which needs to be optimised is the high source and drain contact resistances (R_s and R_d) which results in a large discrepancy between the extrinsic and intrinsic characteristics of GFET. As indicated in a previous study [65], using Ti/Pd/Au as contact metal stack gives comparatively lower contact resistance [67]. Reducing the access region distance should reduce

R_A and consequently reduce R_s and R_d, where a self-alignment process is the limiting case [67].

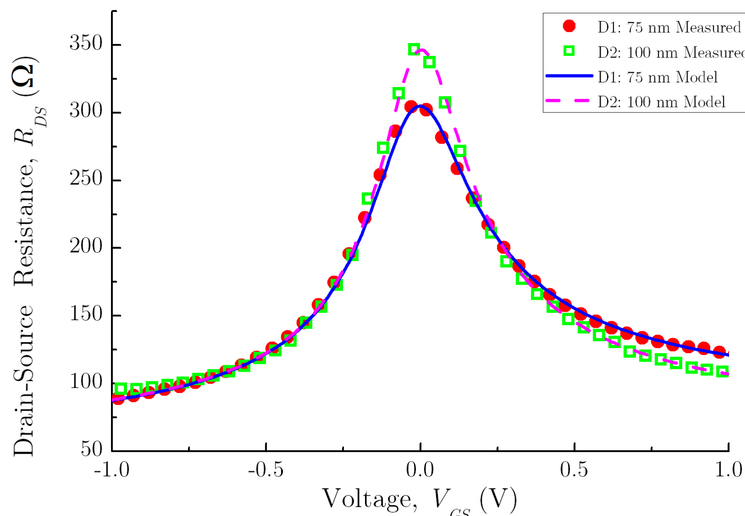


Figure 3.7: Transfer Characteristics of GFETs with varying L_a.

Several GFETs have been made using exfoliated graphene with different L_a including 100 nm (D1), 75 nm (D2) and 50 nm (D3). As can be seen from Fig. 3.7, reducing L_a did not improve the device characteristics significantly. In reality, D3 with L_a =50 nm was not patterned correctly which indicates increased uncertainty in alignment. So for the actual device for measurement, L_a = 100 nm was used.

3.3 Device Measurement

The measurements were performed in three steps. First, DC measurements were performed to select devices with comparatively higher g_m and low gate leakage so that it could provide enough gain during noise measurements and thus reduced measurement uncertainty [68]. Subsequently, S-parameters of some of these devices were performed to confirm the requirement $|S_{21}| > 1$. Finally, noise measurements were performed on those devices.

The DC characterisation of the GFETs was performed using Keithley 4200 semiconductor characterisation system. Even after annealing the CVD graphene was p-doped. As a result the optimum gate bias was mainly on the positive

voltage side where maximum g_m was achieved. The GFETs drain bias was kept negative so that g_m, and thus S_{21}, were positive.

An S-parameter measurement was performed on a representative GFET from 0.5-20 GHz using Agilent N5230A network analyser. From this measurement, the values of f_T and f_{max} could be extracted.

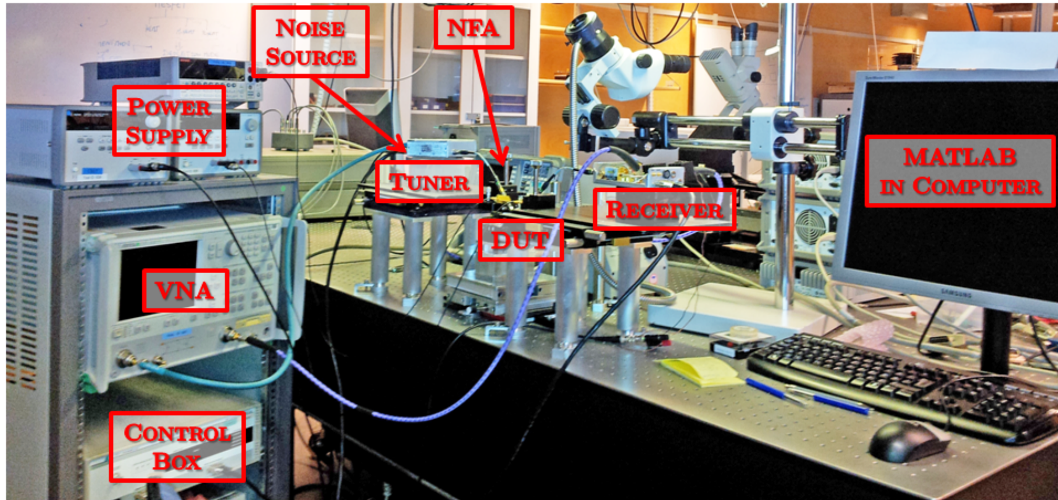


Figure 3.8: Noise Measurement Setup.

The noise measurements were performed at an optimum gate voltage, $V_{GS} = 0.08$ V, to obtain the highest possible g_m at a drain bias of $V_{DS} = -1.5$ V and $I_{DS} = 22$ mA in the 2-8 GHz frequency range at room temperature. The on-wafer measurement setup is shown in Fig. 3.8. A schematic diagram of the setup is shown in Fig. 3.9. The device-under-test (DUT) was connected to an electronic mismatch source tuner A433067 (2-26.5 GHz) with an Agilent 3318A04727 noise source of 5 dB ENR (0.01-18 GHz) on the gate side through a bias tee. A remote receiver module 2-26.5 GHz ([S]/NF switch) was connected on the drain side through another bias tee. The device was biased from a DC power supply with dual output. The S-parameters were measured and displayed through Anritsu 37397C vector network analyser (VNA). An Agilent N8975A noise figure analyser (NFA) controlled the noise source and measured the noise figure. The receiver module was connected to the NFA through a 30-dB low noise amplifier (LNA) biased at +15 V, 208 mA and a 10-dB SMA attenuator. An NP5 Wafer Probe Test Set (control box) controlled the tuner states and switched the receiver module between the VNA and NFA. All the frequency points were measured for 17 tuner states. In each state, the

mismatch source tuner presented a different source impedance to the DUT at each frequency. The VNA, NFA and the control box were in turn calibrated

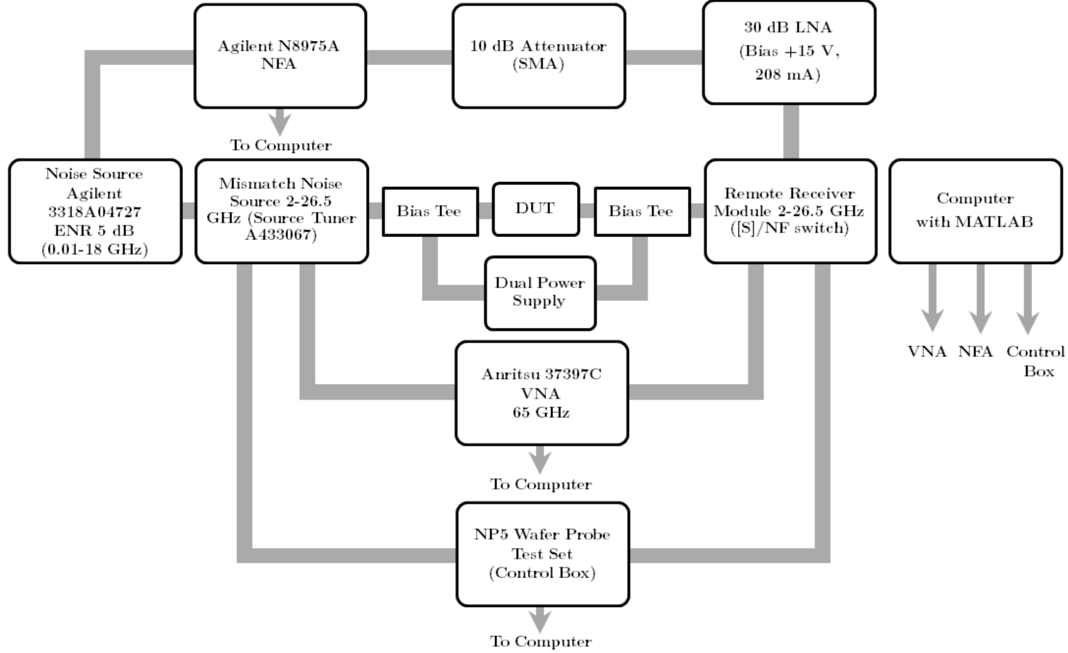


Figure 3.9: Schematic of Noise Measurement Setup.

and controlled by the computer through MATLAB commands. The gate leakage current was monitored throughout the measurement with a Keithley 2425 sourcemeter (not shown in the setup). The noise measurement was done at least three times for the same device to avoid the non-systematic uncertainty in measurement.

Chapter 4

Results and Discussions

This chapter outlines the results obtained from the DC, small signal, and eventually, noise parameter characterisation of the GFETs. The corresponding modelling outcomes are also presented alongside. In addition, the results are discussed by relating with possible physical mechanism and consequences.

4.1 DC Characteristics

The DC transfer characteristic of a representative GFET at $V_{ds} = -1.5$ V is shown in Fig. 4.1 along with the corresponding transconductance. The performance is degraded due to the stress exerted on the GFET from noise measurements. The output characteristic is shown in Fig. 4.2. From small signal measurements, initial values of the extrinsic transconductance is determined to be $g_{m,ex} = 14.6$ mS and output conductance is $g_{d,ex} = 7.4$ mS.

From the DC characteristic of the GFET, carrier mobilities can be extracted using Eq. 2.4. The fitting of the transfer characteristic of the same device at $V_{ds} = -0.1$ V is shown in Fig. 4.3 where the measured values were obtained before noise characterisation i.e. before stress. The fitting parameters along with the extracted carrier mobilities are shown in Table 4.1.

Table 4.1: Parameters for Mobility Extraction

R_{ext}	n_0	C_{gate}	μ_e	μ_h	V_{dirac}
72 Ω	2.1×10^{12} cm^{-2}	600 nF/cm^2	1300 cm^2/V·s	450 cm^2/V·s	2.05 V

4.2 Small Signal Characteristics

The measured S-parameters of the same GFET at a bias point of $V_{gs} = 0.08$ V and $V_{ds} = -1.5$ V in the frequency range of 2 to 8 GHz are shown in Fig. 4.4. Also shown are the modelled S-parameters using the small-signal model in Fig. 2.3. Using the measured S-parameters in a longer frequency range (100 MHz-20 GHz) for a similar device, the short circuit current gain and Mason's unilateral power gain are calculated from Eqs. 2.34 and 2.37. As shown in Fig. 4.5, the f_T (f at $|h_{21}|^2 = 0$ dB) and f_{max} (f at $U = 0$ dB) of the GFET are obtained to be on the order of 10.5 GHz and 13 GHz, respectively. The Mason's gain is flat at low frequency due to R_{pg} and R_{pd}.

4.2.1 Parasitic Components

To obtain R_s and R_d, the sheet resistivity of graphene (R_{sheet}) and contact resistivity (ρ_c) are extracted through TLM measurement. For this purpose, contact pads separated by 100-850 nm (with 50 nm increment) were fabricated with graphene as the conducting channel and the pad metallisation was kept same as the source/drain (1 nm Ti/ 15 nm Pd/ 90 nm Au) of GFETs. Such small contact distances are chosen to mimic the ungated access area in GFET as closely as possible. This is essential to keep the doping level from the charge transfer of the source/drain contacts similar to GFETs. Later on, the contact spacings were measured with SEM and plotted with correction in Fig. 4.6. Although such small contact spacing might seem unconventional for TLM measurement, but the high sheet resistance of graphene results in a reasonably well measurement accuracy. Subsequently, the sheet resistance of graphene, $R_{sheet} = 583\ \Omega/\square$ and contact resistivity, $\rho_c = 76\ \Omega \cdot \mu$m are extracted from Fig. 4.6. Although R_{sheet} is considerably higher than the values of highly doped III-V cap layers in HEMTs but the value $R_s = R_d = 135\ \Omega \cdot \mu$m is comparable to state-of-the-art HEMT technology [66].

The gate resistance is obtained to be 54 Ω/mm from DC end-to-end measurement using separately fabricated extended gates of 1 μm length and 200 μm width with same metallisation as the gate (10 nm Ti/300 nm Au).

The remaining parasitic components of the GFET are extracted using separately fabricated open and short structures excluding the graphene channel. The short was obtained using 20 nm thick Au layer between source, gate and

drain contacts. S-parameter measurement was performed on these open and short structures in the same procedure as in section 3.3. From this, using the method depicted in section 2.2.3, the values of the parasitic components are obtained. Subsequently, from the extrinsic GFET, the parasitics are de-embedded to evaluate the intrinsic device parameters. The extracted values of the parasitic components of the GFET are listed in Table 4.2.

Table 4.2: Extracted Parasitic Components of GFET

L_g	R_g	L_s	L_d	R_s/R_d	C_{pg}	C_{pd}	R_{pg}	R_{pd}
27 pH	1 Ω	10 pH	70 pH	2.2 Ω	27 fF	23 fF	4000 Ω	4800 Ω

4.3 Noise Characteristics

As stated in section 3.3, the noise measurements were performed at least three times and from Fig. 4.7, it can be seen that the three measurements mostly coincide. Thus, the nonsystematic uncertainty in measurement is avoided. The measured noise parameters, namely, F_{min}, optimum source reflection coefficient, Γ_{opt} and noise resistance, R_n are shown in Fig. 4.8, Fig. 4.9, and Fig. 4.10, respectively. During the noise measurement, the gate leakage was $I_g \approx$ 100 pA, which is beneficial to have a minimum level of shot noise [14] and thus negligible contribution at the measured noise level.

4.3.1 Noise Modelling

The parasitic components are de-embedded from the extrinsic GFET as described in section 2.2.3 to obtain the corresponding intrinsic device parameters which are listed in Table 4.3. Subsequently, the intrinsic noise parameters of Fig. 4.8-4.10 are obtained following the noise correlation matrix approach as depicted in section 2.3.2. As can be seen from Fig. 4.11, the condition as described by Eq. 2.22 is valid for the measured noise parameters and thus the validation of Pospieszalski two temperature noise model is confirmed for the GFET. Finally, the noise temperatures of Pospieszalski noise model (see section 2.3.3) are obtained by optimising the values of T_d and T_g for Eq. 2.25 in a mean square error sense to the de-embedded noise parameters from Eq.

2.21. The model fits using the obtained noise temperatures $T_d = 1950$ K and $T_g = 700$ K are also presented in Fig. 4.8-4.10.

Table 4.3: Intrinsic GFET Parameters for Noise Model and Obtained Noise Temperatures

C_{ds}	C_{gs}	C_{gd}	g_m	R_i	R_{ds}	T_a	T_d	T_g
5 fF	130 fF	86 fF	16 mS	18 Ω	123 Ω	297 K	1950 K	700 K

As can be seen from Fig. 4.8, the modelled minimum extrinsic noise figure ($F_{min,ex}$) does not go through 0 dB at zero frequency. This is due to parasitic noise contribution from the insufficiently insulating substrate. De-embedding of R_{pg} results in a intrinsic minimum noise figure, $F_{min,in} = 0$ dB at zero frequency for the intrinsic GFET, as shown by the modelled intrinsic device behavior. For the same reason, in Fig. 4.10, measured Γ_{opt} does not go through $Z = \infty$ at low frequency whereas the Γ_{opt} for intrinsic device does follow the ideal behavior after de-embedding.

4.3.2 Comparison of Γ_{opt} with Γ_s for Maximum Gain

The stability factor K and $|\Delta|$ are plotted in Fig. 4.12 for the same GFET. As can be seen from the figure, both K and $|\Delta|$ are less than unity which imply that the GFET is potentially unstable. Nonetheless, as was pointed out in a previous study of GFET small signal amplifier [33], a conjugately matched output ($\Gamma_L = \Gamma^*_{out}$) does not have much contribution to gain in GFETs. For these reasons, it is convenient to consider the source reflection coefficient, Γ_s, for maximum stable gain, MSG, which is plotted in Fig. 4.10. From this, it is apparent that the required Γ_s for maximum gain do not differ much from Γ_{opt} for minimum noise. This is also visible in Fig. 4.13 where the values of different gains differ $< (1-2)$ dB from each other. In this figure, the transducer power gain (G_T) and available power gain (G_A) are calculated by setting $\Gamma_s = \Gamma_{opt}$ and $\Gamma_L = 0$ for 50 Ω termination in Eqs. 2.29 and 2.31, respectively. Maximum stable gain (MSG) is calculated using Eq. 2.33.

4.4 Discussions

To compare the noise performance of GFETs with other technologies a particular frequency $f = 2$ GHz is chosen which is appropriate considering the GFETs' f_T and f_{max}. For matured technologies, reported measurement frequency in the literature is generally higher. So for comparison, another figure of merit $F_{min}/f/L$ [69] is used. The comparison of cut-off frequency, minimum noise figure, and $F_{min}/f/L$ of different microwave FET technologies with GFETs at room temperature is presented in Table 4.4. The intrinsic and extrinsic F_{min} are similar for matured technologies.

For GFETs at 2 GHz, $F_{min,ex} = 2.4$ dB and $F_{min,in} = 0.8$ dB with an associated gain $G_a = 10.6$ dB. which is superior to Si CMOS [70] technology and comparable to GaAs MESFETs [71] with similar channel length. For the initial stages of Si CMOS RF technology [70], the degradation in F_{min} was mainly due to pad parasitics. In case of GFET, we get similar degradation due to pad parasitics. Nevertheless, in comparison to the latest 45 nm Si CMOS technology where metal gate is used to reduce such parasitic effects [72], GFET performs better in terms of noise as can be seen from the $F_{min,in}/f/L$ value. Subtracting the parasitic noise contribution makes the $F_{min,in}/f/L$ value for GFET comparable to other III-V technologies as well.

Table 4.4: Noise Performance Comparison of Different FET Technologies at $f = 2$ GHz in RT

Technology	L (μm)	f (GHz)	f_T (GHz)	$F_{min,in}$ (dB)	$F_{min,ex}(dB)$ (dB)	$F_{min,in}/f/L$ (dB/GHz/μm)
GFET	1	2	10.5	0.8	2.4	0.40
Si CMOS [70]	0.97	2	10	1.1	3.2	∼1
Si CMOS [72]	0.045	2	395	–	0.1	1.11
GaAs MESFET [71]	0.90	2	10.5	–	0.6	0.33
GaAs HEMT [73]	0.15	18	65.9	–	1.5	0.33
GaAs pHEMT [74]	0.25	2	100	–	0.2	0.40
InP HEMT [75]	0.15	93	186	–	2.5	0.18

The extracted values of T_d and T_g are comparable to GaAs HEMTs [76] and GaAs pHEMTs [53] at similar bias current level. The value of T_g is close to ambient temperature in most of the technologies. A T_g elevated from room

temperature is attributed to self-heating, generally occurring at very high I_{DS} [76]. Choosing a more thermally conducting substrate might improve T_g and thus F_{min} but at the same time it also needs to provide enough electrical insulation.

The inferior noise characteristics of GFETs compared to GaAs or InP HEMTs can be attributed to the reduced electron and hole mobilities which were extracted from the DC characteristics to be 1300 and 450 $\mathrm{cm}^2/\mathrm{V{\cdot}s}$, respectively. An observed mobility increase at cryogenic temperatures in graphene [28] is likely to provide reduced noise figure at low temperatures in GFETs.

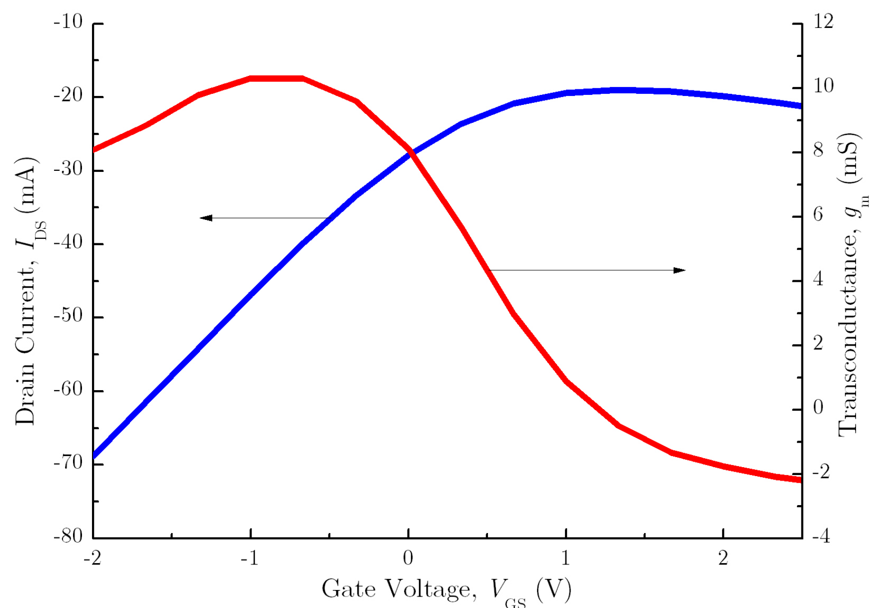


Figure 4.1: Transfer characteristic and transconductance of GFET at $V_{DS} = -1.5$ V.

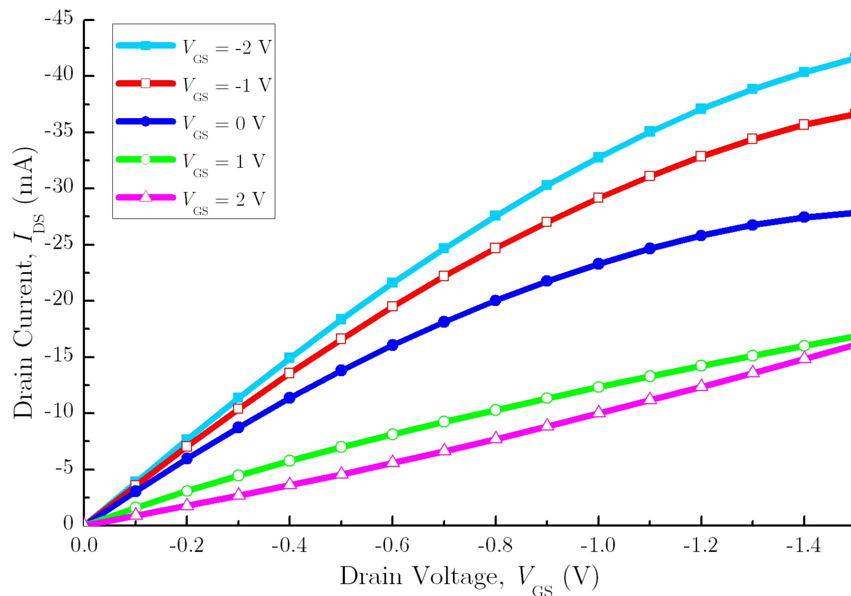


Figure 4.2: Output characteristic of GFET at $V_{GS} = -2$ to 2 V.

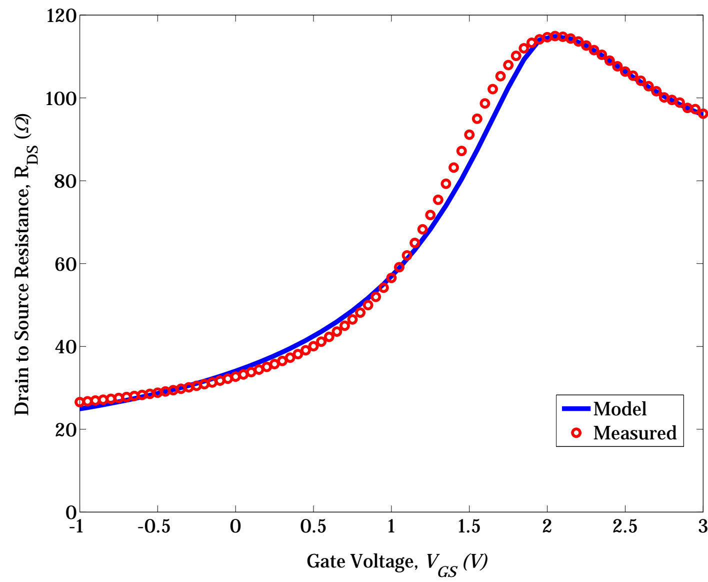


Figure 4.3: Measured and modelled transfer characteristic of GFET at $V_{DS} = -0.1$ V.

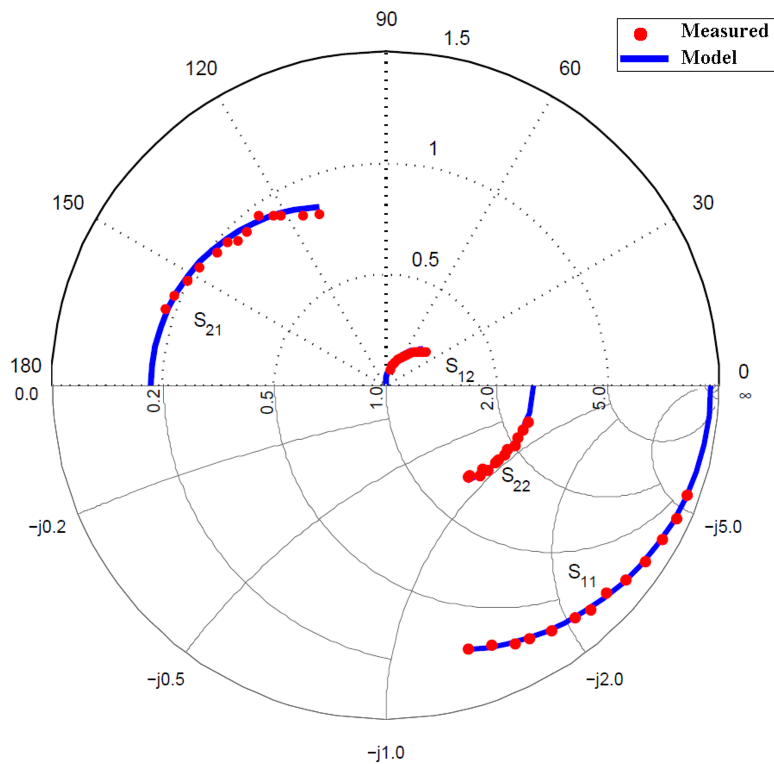


Figure 4.4: Measured and modelled GFET S-parameters from 2 to 8 GHz at the bias point of $V_{GS} = 0.08$ V and $V_{DS} = -1.5$ V.

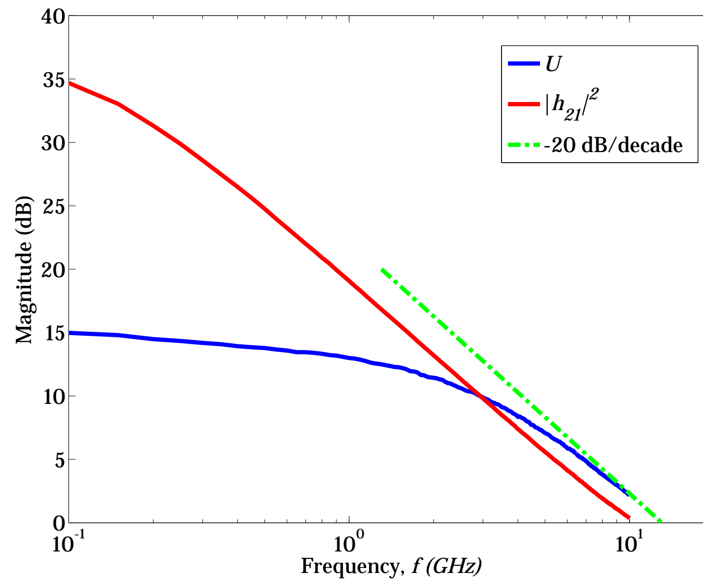


Figure 4.5: Calculated short-circuit current gain and Mason's unilateral power gain of the GFET at the bias point of $V_{GS} = 0.08$ V and $V_{DS} = -1.5$ V.

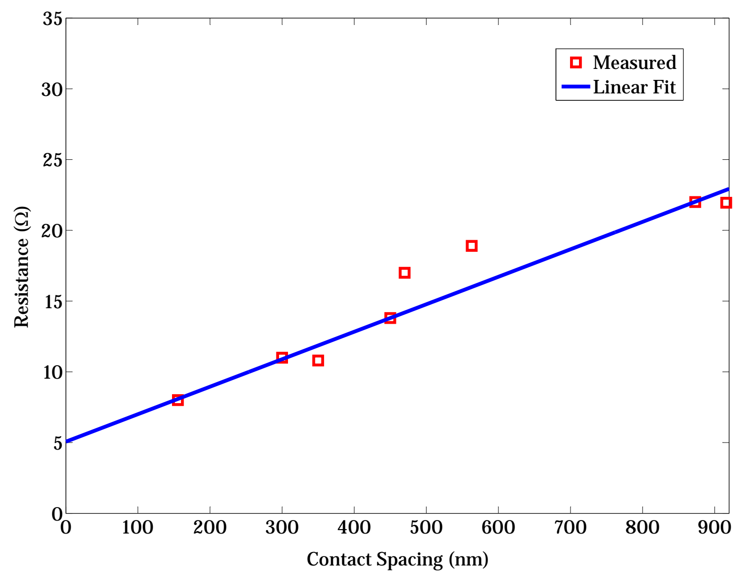


Figure 4.6: Determination of contact resistance from TLM measurement with corrected contact spacing from SEM measurement.

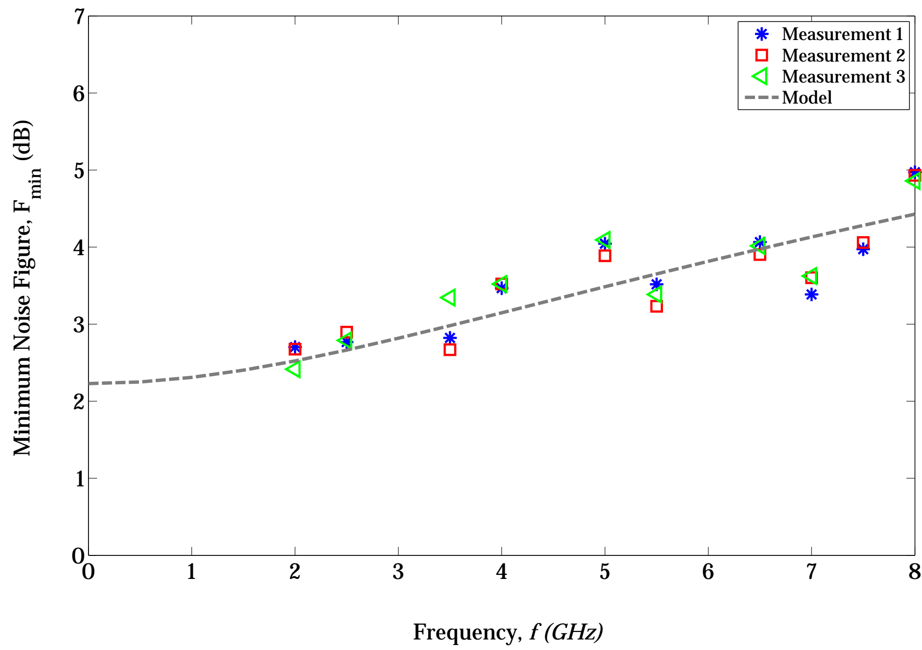


Figure 4.7: Measured and modelled minimum noise figure of the extrinsic GFET for three measurements.

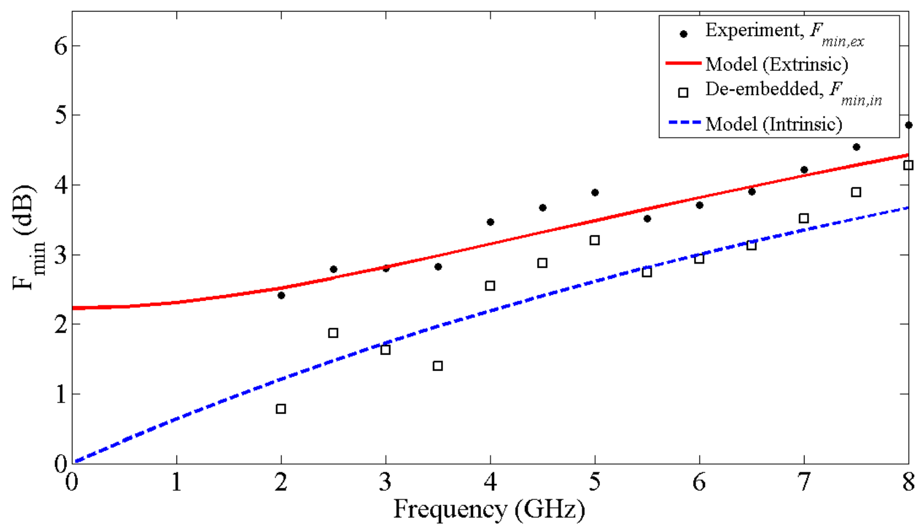


Figure 4.8: Measured and modelled minimum noise figure of the extrinsic and de-embedded GFET.

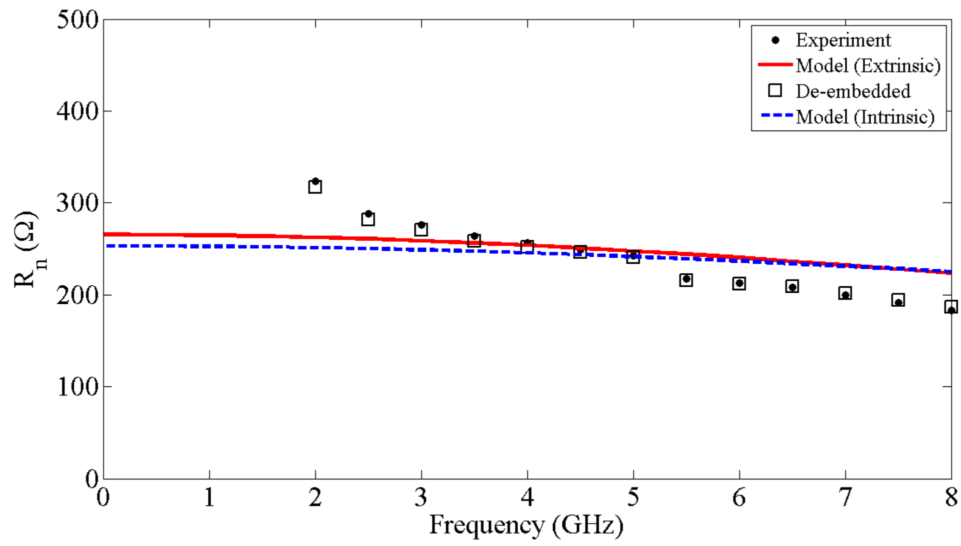


Figure 4.9: Measured and modelled noise resistance of the extrinsic and de-embedded GFET.

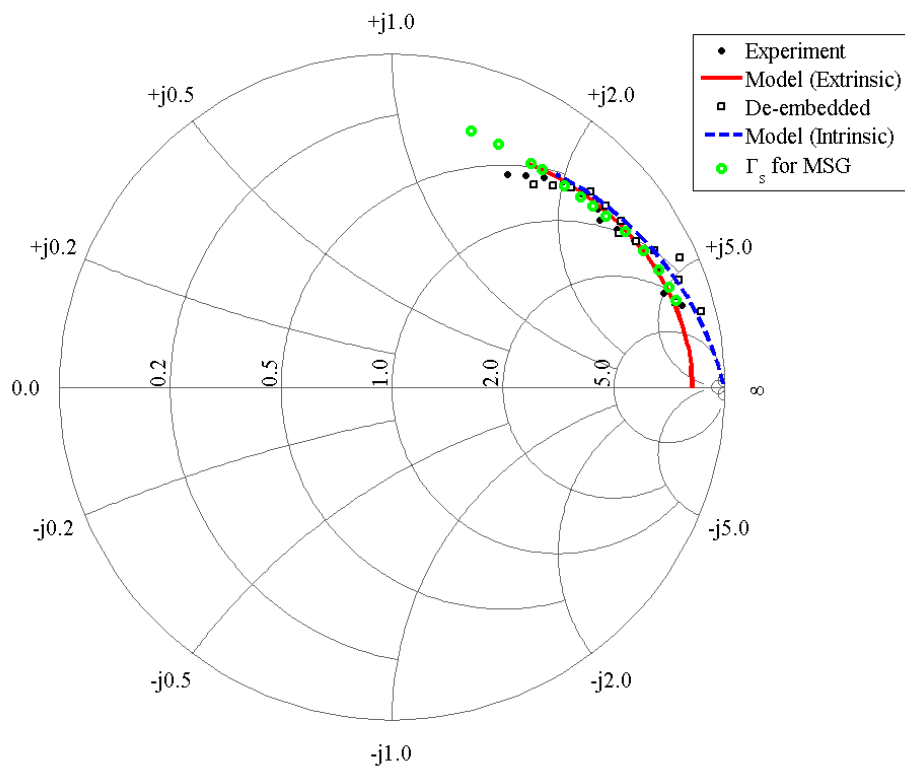


Figure 4.10: Measured and modelled optimum source reflection coefficient of the extrinsic and de-embedded GFET.

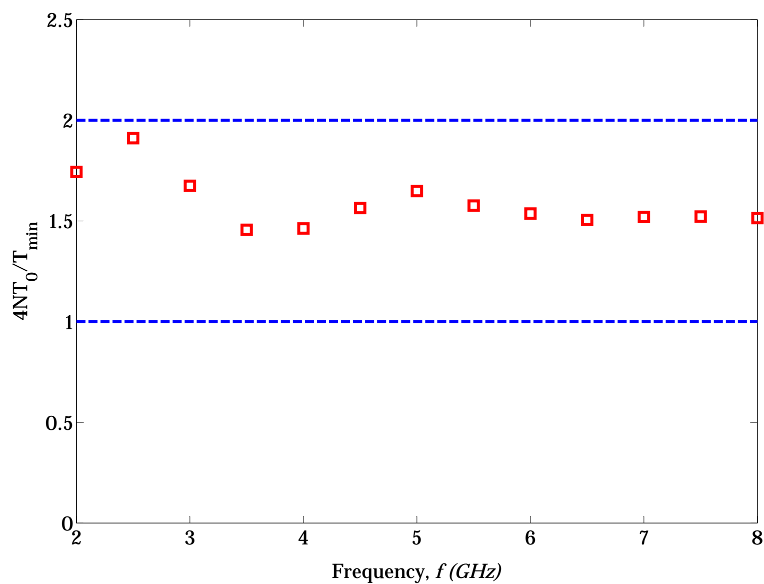


Figure 4.11: Validation of Pospieszalski noise model for measured noise parameters of GFET.

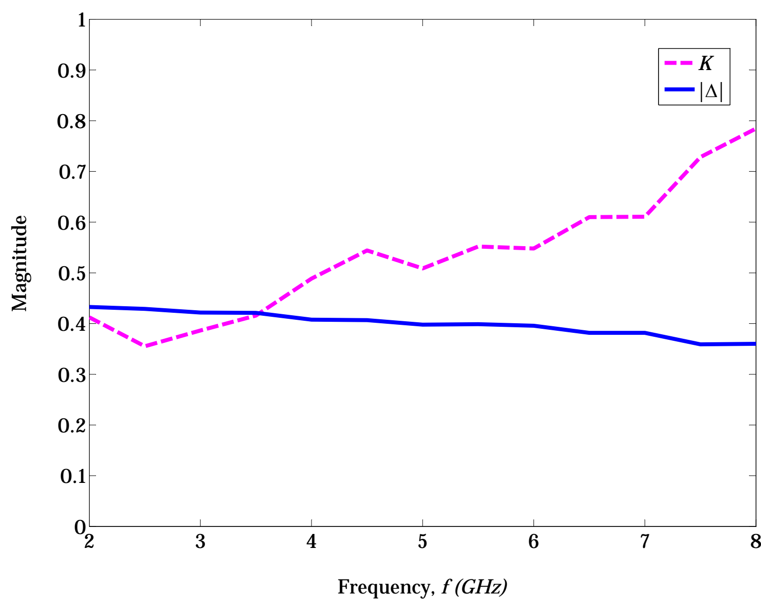


Figure 4.12: Stability factors of GFET.

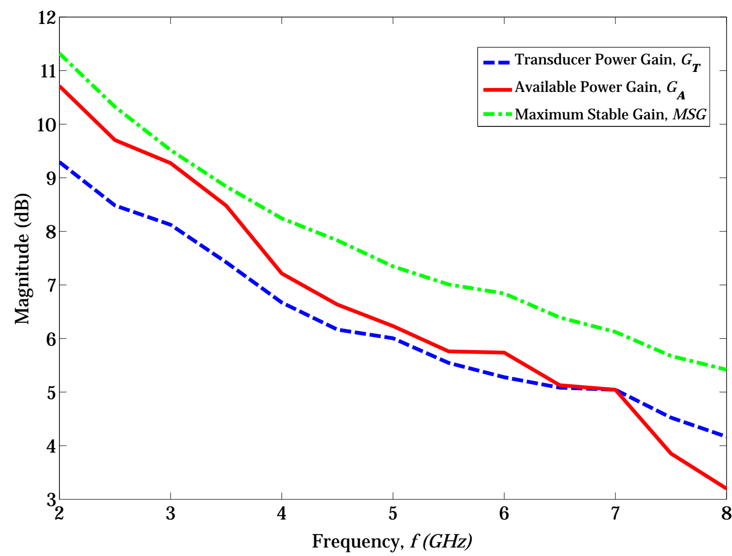


Figure 4.13: Transducer power gain, available power gain and maximum stable gain of GFET with $\Gamma_s = \Gamma_{opt}$ and $\Gamma_L = 0$.

Chapter 5

Conclusion

5.1 Summary

The first device level noise parameter characterisation of GFETs at microwave frequencies is demonstrated in this thesis. Initially, an optimised process has been developed to fabricate GFETs using CVD graphene. The performance of the GFET has been optimised through minimising gate leakage, contact resistance and unwanted doping of graphene. Use of CVD graphene has ensured large scale reproducibility. The extrinsic GFET has displayed a minimum noise figure $F_{min,ex}$ = 2.4-4.9 dB with an associated gain G_a = 10.6-2 dB in the 2-8 GHz frequency range. Through parasitic extraction and de-embedding, the minimum noise figure of the intrinsic GFET has been estimated to be $F_{min,in}$ = 0.8-4.3 dB in the same frequency range. Subsequent noise modelling has provided an equivalent drain noise temperature T_d = 1950 K and an equivalent gate noise temperature T_g = 700 K.

5.2 Outlook

By utilising the knowledge of all four noise parameters obtained from the present study, the immediate extension would be to design an LNA. Through this, cryogenic noise characterisation of GFETs could be realised.

At present, GFETs provide comparable noise performance with respect to Si CMOS technology which indicates possible integration with Si technology for RF applications. To be comparable to GaAs [74,76] or InP HEMTs [66], further improvement of the noise performance and extension to higher frequencies need

to be accomplished. To reach this goal, reducing the gate length of GFETs is necessary which can provide comparable f_T and f_{max} [29,30]. Improvement in f_{max} will translate into a lower T_d [69] and consequently, will provide better noise performance. Additionally, better channel carrier dynamics needs to be achieved by approaching the room temperature mobility of intrinsic graphene in GFETs.

Bibliography

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, “Electric field effect in atomically thin carbon films,” *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] D.-H. Chae, B. Krauss, K. von Klitzing, and J. H. Smet, “Hot phonons in an electrically biased graphene constriction,” *Nano Letters*, vol. 10, no. 2, pp. 466–471, 2010.

[3] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, “Approaching ballistic transport in suspended graphene,” *Nature Nanotechnology*, vol. 3, no. 8, pp. 491–495, 2008.

[4] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, “Superior thermal conductivity of single-layer graphene,” *Nano Letters*, vol. 8, no. 3, pp. 902–907, 2008.

[5] W. Shockley, “A unipolar "field-effect" transistor,” *Proceedings of the IRE*, vol. 40, no. 11, pp. 1365–1376, 1952.

[6] W. Hooper and W. Lehrer, “An epitaxial GaAs field-effect transistor,” *Proceedings of the IEEE*, vol. 55, no. 7, pp. 1237–1238, 1967.

[7] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, “A new field-effect transistor with selectively doped GaAs/n-$Al_xGa_{1-x}As$ heterojunctions,” *Japanese Journal of Applied Physics*, vol. 19, no. 5, pp. L225–L227, 1980.

[8] L. Samoska, “An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime,” *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 9–24, 2011.

[9] D.-H. Kim, B. Brar, and J. del Alamo, "f_t = 688 GHz and f_{max} = 800 GHz in L_g = 40 nm $In_{0.7}Ga_{0.3}As$ MHEMTs with $g_{m,max}$>2.7 ms/μm," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 13.6.1–13.6.4, 2011.

[10] F. Schwierz, *Modern Microwave Transistors: Theory, Design and Performance*. John Wiley & Sons, Inc., 2003.

[11] J. B. Johnson, "Thermal agitation of electricity in conductors," *Physical Review*, vol. 32, pp. 97–109, Jul 1928.

[12] H. Nyquist, "Thermal agitation of electric charge in conductors," *Physical Review*, vol. 32, pp. 110–113, Jul 1928.

[13] G. H. Hanson and A. van der Ziel, "Shot noise in transistors," *Proceedings of the IRE*, vol. 45, no. 11, pp. 1538–1542, 1957.

[14] S. Maas, *Noise in linear and nonlinear circuits*. Artech House, 2005.

[15] A. K. Geim, "Graphene: Status and prospects," *Science*, vol. 324, no. 5934, pp. 1530–1534, 2009.

[16] P. R. Wallace, "The band theory of graphite," *Physcal Review*, vol. 71, pp. 622–634, May 1947.

[17] F. Schwierz, "Graphene transistors," *Nature Nanotechnology*, vol. 5, no. 7, pp. 487–496, 2010.

[18] M. C. Lemme, T. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, 2007.

[19] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Applied Physics Letters*, vol. 94, no. 6, pp. 062107–062107–3, 2009.

[20] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios, "BN/Graphene/BN transistors for RF applications," *IEEE Electron Device Letters*, vol. 32, no. 9, pp. 1209–1211, 2011.

[21] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, "Hysteresis of electronic transport in graphene transistors," *ACS Nano*, vol. 4, no. 12, pp. 7221–7228, 2010.

[22] Y. G. Lee, C. G. Kang, U. J. Jung, J. J. Kim, H. J. Hwang, H.-J. Chung, S. Seo, R. Choi, and B. H. Lee, "Fast transient charging at the graphene/SiO_2 interface causing hysteretic device characteristics," *Applied Physics Letters*, vol. 98, no. 18, p. 183508, 2011.

[23] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1–4, 2009.

[24] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Physical Review Letters*, vol. 98, p. 206805, May 2007.

[25] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, 2008.

[26] Y. Lu, B. Goldsmith, D. R. Strachan, J. H. Lim, Z. Luo, and A. T. C. Johnson, "High-on/off-ratio graphene nanoconstriction field-effect transistor," *Small*, vol. 6, pp. 2748–2754, 2010.

[27] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Applied Physics Letters*, vol. 91, no. 9, p. 092109, 2007.

[28] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1567–1584, 2013.

[29] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, and W. A. de Heer, "Record maximum oscillation frequency in c-face epitaxial graphene transistors," *Nano Letters*, vol. 13, no. 3, pp. 942–947, 2013.

[30] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proceedings of the National Academy of Sciences*, vol. 109, no. 29, pp. 11588–11592, 2012.

[31] J. S. Moon, D. Curtis, D. Zehnder, S. Kim, D. K. Gaskill, G. Jernigan, R. L. Myers-Ward, J. Eddy, C.R., P. M. Campbell, K.-M. Lee, and P. Asbeck, "Low-phase-noise graphene FETs in ambipolar RF applications," *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 270–272, 2011.

[32] S. A. Imam, S. Sabri, and T. Szkopek, "Low-frequency noise and hysteresis in graphene field-effect transistors on oxide," *IET Micro Nano Letters*, vol. 5, no. 1, pp. 37–41, 2010.

[33] M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier," *Electronics Letters*, vol. 48, no. 14, pp. 861–863, 2012.

[34] M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Resistive graphene FET subharmonic mixers: Noise and linearity assessment," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 4035–4042, 2012.

[35] M. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340–1350, 1989.

[36] R. A. Pucel, W. Struble, R. Hallgren, and U. L. Rohde, "A general noise de-embedding procedure for packaged two-port linear active devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 11, pp. 2013–2024, 1992.

[37] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Prentice Hall, 2 ed., 1997.

[38] S. M. Sze, *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., 2006.

[39] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 5 ed., 2004.

[40] O. Habibpour, J. Vukusic, and J. Stake, "A large-signal graphene FET model," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 968–975, 2012.

[41] J. Xia, F. Chen, J. Li, and N. Tao, "Measurement of the quantum capacitance of graphene," *Nature Nanotechnology*, vol. 4, no. 8, pp. 505–509, 2009.

[42] Y. Q. Wu, D. Farmer, A. Valdes-Garcia, W. J. Zhu, K. A. Jenkins, C. Dimitrakopoulos, P. Avouris, and Y. M. Lin, "Record high RF performance for epitaxial graphene transistors," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 23.8.1–23.8.3, 2011.

[43] Y. Wu, Y.-m. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, no. 7341, pp. 74–78, 2011.

[44] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, 2010.

[45] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, 1988.

[46] S. Chou and D. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's," *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 448–450, 1987.

[47] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 7, pp. 891–895, 1990.

[48] J. Bauer, R.F. and P. Penfield, "De-embedding and unterminating," *IEEE Transactions on Microwave Theory and Techniques*, vol. 22, no. 3, pp. 282–288, 1974.

[49] H. Berger, “Contact resistance on diffused resistors,” in *Digest of Technical Papers IEEE International Solid-State Circuits Conference*, vol. XII, pp. 160–161, 1969.

[50] H. Murrmann and D. Widmann, “Current crowding on metal contacts to planar devices,” *IEEE Transactions on Electron Devices*, vol. 16, no. 12, pp. 1022–1024, 1969.

[51] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rohde, “A new and reliable direct parasitic extraction method for MESFETs and HEMTs,” in *23rd European Microwave Conference*, pp. 451–453, 1993.

[52] P. Heymann, M. Rudolph, H. Prinzler, R. Doerner, L. Klapproth, and G. Bock, “Experimental evaluation of microwave field-effect-transistor noise models,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 2, pp. 156–163, 1999.

[53] M. Garcia, J. Stenarson, K. Yhland, H. Zirath, and I. Angelov, “A new extraction method for the two-parameter FET temperature noise model,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1679–1685, 1998.

[54] H. Fukui, “Available power gain, noise figure, and noise measure of two-ports and their graphical representations,” *IEEE Transactions on Circuit Theory*, vol. 13, no. 2, pp. 137–142, 1966.

[55] S. Mason, “Power gain in feedback amplifier,” *Transactions of the IRE Professional Group on Circuit Theory*, vol. CT-1, no. 2, pp. 20–25, 1954.

[56] J. Sun, N. Lindvall, M. T. Cole, K. Angel, T. Wang, K. Teo, D. H. C. Chua, J. Liu, and A. Yurgens, “Low partial pressure chemical vapor deposition of graphene on copper,” *IEEE Transactions on Nanotechnology*, vol. 11, no. 2, pp. 255–260, 2012.

[57] C. J. L. de la Rosa, J. Sun, N. Lindvall, M. T. Cole, Y. Nam, M. Löffler, E. Olsson, K. B. K. Teo, and A. Yurgens, “Frame assisted H_2O electrolysis induced H_2 bubbling transfer of large area graphene grown by chemical vapor deposition on cu,” *Applied Physics Letters*, vol. 102, no. 2, p. 022101, 2013.

[58] A. Ismach, C. Druzgalski, S. Penwell, A. Schwartzberg, M. Zheng, A. Javey, J. Bokor, and Y. Zhang, "Direct chemical vapor deposition of graphene on dielectric surfaces," *Nano Letters*, vol. 10, no. 5, pp. 1542–1548, 2010.

[59] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, 2009.

[60] A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff, and R. M. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO_2," *Applied Physics Letters*, vol. 99, no. 12, p. 122108, 2011.

[61] S. Ryu, L. Liu, S. Berciaud, Y.-J. Yu, H. Liu, P. Kim, G. W. Flynn, and L. E. Brus, "Atmospheric oxygen binding and hole doping in deformed graphene on a SiO_2 substrate," *Nano Letters*, vol. 10, no. 12, pp. 4944–4951, 2010.

[62] Y.-C. Lin, C.-C. Lu, C.-H. Yeh, C. Jin, K. Suenaga, and P.-W. Chiu, "Graphene annealing: How clean can it be?," *Nano Letters*, vol. 12, no. 1, pp. 414–419, 2012.

[63] A. Jacobsen, F. M. Koehler, W. J. Stark, and K. Ensslin, "Towards electron transport measurements in chemically modified graphene: effect of a solvent," *New Journal of Physics*, vol. 12, no. 12, p. 125007, 2010.

[64] A. Nourbakhsh, M. Cantoro, A. Klekachev, F. Clemente, B. SoreÌĄe, M. H. van der Veen, T. Vosch, A. Stesmans, B. Sels, and S. De Gendt, "Tuning the Fermi level of SiO_2-supported single-layer graphene by thermal annealing," *The Journal of Physical Chemistry C*, vol. 114, no. 15, pp. 6894–6900, 2010.

[65] M. Andersson, "Noise characterisation of graphene FETs," Master's thesis, Chalmers University of Technology, 2012.

[66] J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P.-A. Nilsson, J. Starski, N. Wadefalk, H. Zirath, and J. Grahn, "Ultralow-power cryogenic InP HEMT with minimum noise temperature of 1 K at 6 GHz," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 664–666, 2012.

[67] D. B. Farmer, Y.-M. Lin, and P. Avouris, "Graphene field-effect transistors with self-aligned gates," *Applied Physics Letters*, vol. 97, no. 1, p. 013103, 2010.

[68] Agilent Application Note, *Noise Figure Measurement Accuracy - The Y-Factor Method*, 57-2 ed.

[69] B. Hughes, "A temperature noise model for extrinsic FETs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 9, pp. 1821–1832, 1992.

[70] C. Biber, M. Schmatz, T. Morf, U. Lott, E. Morifuji, and W. Bachtold, "Technology independent degradation of minimum noise figure due to pad parasitics," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 145–148 vol.1, 1998.

[71] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Transactions on Electron Devices*, vol. 26, no. 7, pp. 1032–1037, 1979.

[72] C. H. Jan, M. Agostinelli, H. Deshpande, M. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala, J. Lin, Y.-L. Lu, S. Mudanai, J. Park, A. Rahman, J. Rizk, W.-K. Shin, K. Soumyanath, H. Tashiro, C. Tsai, P. Vandervoorn, J. Y. Yeh, and P. Bai, "RF CMOS technology scaling in high-k/metal gate era for RF SoC (system-on-chip) applications," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 27.2.1–27.2.4, 2010.

[73] K. H. G. Duh, S. M. J. Liu, L. Lester, P. Chao, P. Smith, M. Das, B. Lee, and J. Ballingall, "Ultra-low noise characteristics of millimeter-wave high electron mobility transistors," *IEEE Electron Device Letters*, vol. 9, no. 10, pp. 521–523, 1988.

[74] J. Wenger, "Quarter-micrometer low-noise pseudomorphic GaAs HEMTs with extremely low dependence of the noise figure on drain-source current," *IEEE Electron Device Letters*, vol. 14, no. 1, pp. 16–18, 1993.

[75] P. Chao, A. J. Tessmer, K. H. G. Duh, P. Ho, M.-Y. Kao, P. Smith, J. Ballingall, S. Liu, and A. Jabra, "W-band low-noise inalas/ingaas lattice-matched hemts," *IEEE Electron Device Letters*, vol. 11, no. 1, pp. 59–62, 1990.

[76] M. Pospieszalski and A. Niedzwiecki, "FET noise model and on-wafer measurement of noise parameters," in *IEEE MTT-S International Microwave Symposium Digest*, pp. 1117–1120 vol.3, 1991.

Appendix A

Journal Manuscript

Noise Parameter Characterization of Graphene Field Effect Transistors in the 2-8 GHz Frequency Range