CHALMERS

Design and analysis of multi-band transmitters for wireless communications

Master's Thesis in Wireless, Photonics and Space Engineering

SEBASTIAN GUSTAFSSON

Department of Microtechnology and Nanoscience - MC2
Microwave Electronics Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

The purpose of this thesis is to analyze a transistor under multi-band operation and investigate how termination of the intermodulation products affect device performance. A multi-band active load-pull system is used for device measurements, and the two frequencies of interest are 2.14 GHz and 2.65 GHz, which represent two LTE bands. From measured results, two amplifiers are designed, fabricated and evaluated. The first amplifier is a dual-band power amplifier (DBPA) while the other is designed as a concurrent dual-band power amplifier (CDBPA) and implements proper intermodulation termination.

It is shown that the optimal load reflection coefficient for highest efficiency changes between single band transmission and concurrent band transmission for the two frequencies. Depending on the termination of the intermodulation products, located at 1.63 GHz and 3.16 GHz, the efficiency varies between 41.5% and 46%. The fabricated amplifiers show peak efficiencies of 54% and 45% at concurrent transmission for the DBPA and CDBPA, respectively. Using a 5 MHz OFDM signal, the amplifiers show average efficiencies of 26% and 20%, respectively.

Keywords: Microwave, Power Amplifier, Load-Pull, Multi-Band

Preface

The master thesis presented here is the final act of my studies and concludes five years of studying at the Electrical Engineering programme at Chalmers University of Technology. Being a student of the Wireless, Photonics and Space Master's Programme, I was naturally drawn to the Microwave field.

The six month journey has given me a lot of valuable experience and I am very pleased with both my supervision and the results obtained. I have been able to test my knowledge and creativity throughout the thesis.

This work has been performed at the Department of Microtechnology and Nanoscience, MC2, Chalmers. Dr. Mattias Thorsell has supervised the project and Dr. Hans Hjelmgren has been the examiner of the thesis. The time frame of the project was between January 14$^{\text{th}}$ and May 31$^{\text{st}}$.

Acknowledgements

This thesis would not have been possible without all of the support from my supervisor, family, colleagues and friends.

First of all, I would like to thank Mattias Thorsell for giving me the opportunity of this thesis, sharing his knowledge and encouraging me in times when things would not simply work. Your help has been indispensable and many of the good results obtained would not be possible without you. I would like to give a special thanks to Carl-Magnus Kihlman for providing mechanical fixtures for my amplifiers. Also, I would like to thank Per Landin for assisting me in a couple of measurements. Thanks to all my colleagues at MEL and friends for good times and for their help and support. Last, but not least, thanks to my girlfriend for supporting and encouraging me, you are the best!

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Göteborg June 2013
Sebastian Gustafsson

Notations and abbreviations

Notations

C	Capacitance
f	Frequency
I	Inductance
P_{del}	Delivered power
P_{in}	Input power
P_{out}	Output power
P_{sat}	Saturated output power
R	Resistance
S-parameters	Scattering parameters
V	Voltage
η_{tot}	Total efficiency
Γ_L	Load reflection coefficient

Abbrevations

ACLR	Adjacent channel leakage ratio
ADC	Analog to digital converter
AWG	Arbitrary waveform generator
CDBPA	Concurrent dual-band power amplifier
CW	Continuous wave
DBPA	Dual-band power amplifier
DC	Direct current
DPA	Doherty power amplifier
DPD	Digital predistortion
DUT	Device under test
EM	Electromagnetic
GaN	Gallium Nitride
GMP	Generalized memory polynomial
HEMT	High electron mobility transistor
IF	Intermediate frequency
IM	Intermodulation
IM3	Third order intermodulation
IV	Current/voltage
LSNA	Large signal network analyzer
LTE	Long term evolution
NVNA	Non-linear vector network analyzer
OFDM	Orthogonal frequency-division multiplexing
PA	Power amplifier
PCB	Printed circuit board
RBS	Radio base station

RF	Radio frequency
SMT	Surface mount technology
SNR	Signal to noise ratio
SOLT	Short, open, load, through
TL	Transmission line

Contents

Chapter 1

Introduction

1.1 Background

Mobile communications has drastically changed our daily life. We expect, and are expected to have constant access to services like e-mail, social networks and cloud computing. With a rapid growth of users being involved in the connected society, mobile technology must evolve in the same pace to meet the requirements. It is predicted that the data traffic will increase almost exponentially to 11.2 exabytes (10^{18}) per month by 2017 [1]. To meet this demand, mobile network operators together with the microwave industry have begun to implement advanced solutions. Pico-cell Radio Base Stations (RBSs) and local Wi-Fi networks help offloading macro RBSs. As from the LTE-Advanced standard and for future mobile standards, increased channel bandwidth and carrier aggregation are solutions to increase the capacity of mobile network systems.

There is no doubt that the demand of high speed mobile networks will continue to grow. However, with the growing demand and more RBSs being deployed, the power consumption increases. Power consumption directly translates into cost and CO2 emissions, with at least the former being an important factor for mobile network operators. It is estimated that cellular communication systems worldwide account for approximately 3% of the total CO2 emission [2]. This might not sound like much, but it is comparable to CO2 emissions from civil aircraft, which accounts for 2% of the total emissions [3]. The main power consumer in a RBS is the power amplifier (PA) and therefore a lot of research has been conducted to improve the PA efficiency. Decreasing the power consumption does not only save money and help minimizing the CO2 footprint, it also improves long term reliability.

Not only is the power consumption affecting the environment. With each new generation of mobile connectivity, new frequency bands have been introduced. New frequency bands means that the old equipment has to be replaced in order to be compatible, thus further increasing the environmental impact. To increase the flexibility of mobile communication equipment, multi-band PAs have recently gained a lot of attention. Apart from the increase in flexibility, multiple carrier access enables increased data throughput.

1.2 Survey of the field

Multi-band transmitters is today a hot research topic with many different approaches and new ideas being presented each year. It is hard to get a complete overview of the field and comparing different results is not trivial due to different frequencies, power levels, linearity, etc.

The main problem of designing multi-band transmitters is to create matching networks that work for several bands, in order to have good matching and high performance in each frequency band. Extensive research about multi-band transmitters has previously been performed and some realizations of concurrent dual-band power amplifiers are introduced in [4],

[5], [6] and [7]. In [8] an interesting design approach is made where the device switches between operating classes, depending on the frequency. Increasing the efficiency in output power backoff can be done with Doherty Power Amplifiers (DPAs), and some concurrent dual-band DPAs are presented in [9], [10], [11] and [12].

For all of the studied dual-band power amplifiers, they are either based on model simulations or load-pull measurements. No analysis or consideration of the device operation at concurrent transmission is made and none of them implement proper intermodulation termination.

1.3 Thesis contributions

To the best knowledge of the author, this thesis has contributed to one of the first multi-band load-pull measurements performed. Other measurement systems have wideband or harmonic load-pull capabilities, but the measurement system used in this thesis uses frequencies that can be individually controlled. The complexity of multi-signal load-pull has been discussed and some future research directions have been pointed out. The thesis has successfully implemented measurement results into the design of two power amplifiers, with performance comparable to other published work. The importance of proper third order intermodulation termination has been demonstrated in the load-pull measurements.

1.4 Thesis outline

The focus of this thesis is on device characterization, heavily relying on load-pull measurements. Brief load-pull theory, including passive and active load-pull, and examples of active load-pull systems are covered in Chapter 2. Chapter 3 presents an active load-pull system with multi-band capabilities, which is used for measurements in this thesis. The multi-band load-pull system is used in Chapter 4 to characterize a microwave transistor under multi-band operation. Power amplifier design is covered in Chapter 5 and the measured results for the fabricated power amplifier are presented in Chapter 6. Chapter 7 discusses the results obtained and Chapter 8 concludes the work and suggests some future work to be done within the research area.

Chapter 2

Large signal transistor characterization

This chapter will start out by describing some basic load-pull theory, different load-pull methods and later on compare different load-pull measurement setups.

2.1 Load-pull theory

The most common way to characterize a microwave transistor is to measure its S-parameters. The S-parameters are often given in the data sheet of commercial transistors, and provide a complete linear model. However, the S-parameters do not include any information about the DC-characteristics of the device and are therefore not suitable for large signal analysis. Take Figure 2.1 as an example.

If the generator resistance is purely real, matching for highest gain results in a load resistance of the same value as the internal generator resistance. However, this does not automatically mean that the device is matched for maximum output power since no IV-information is given with the S-parameters. The maximum voltage swing and maximum current swing is limited by device properties such as breakdown voltage and electron velocity. Maximizing the output power from a device is therefore not as straight-forward as gain matching. The output power is maximized when the current and voltage swing is maximized, as shown in Figure 2.1.

Figure 2.2 illustrates the difference in maximum gain and output power for maximum gain match and maximum output power match. Typically, a conjugate matched amplifier will have higher initial gain but will experience gain compression earlier and have lower saturated

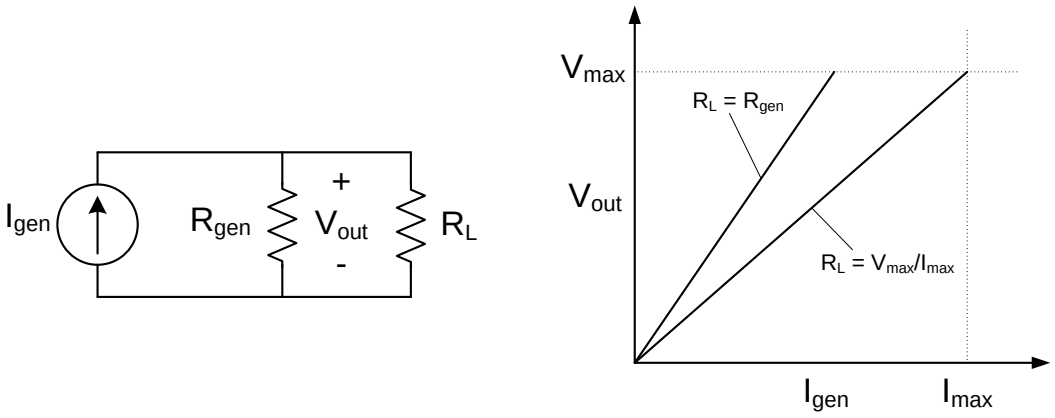


Figure 2.1: The loadline approach. The optimal resistive load will maximize the current and voltage swing and thus maximize the output power.

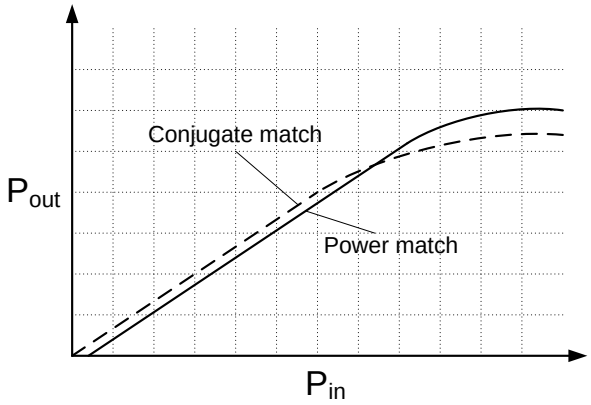


Figure 2.2: Comparison between conjugate matching and power matching in terms of output power versus input power.

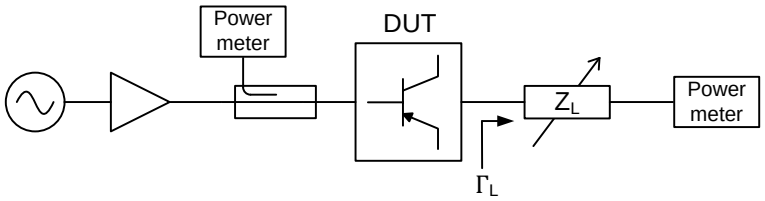


Figure 2.3: A passive load-pull setup utilizing a mechanical tuner.

output power. Various tools are available for the PA designer to maximize the performance of the transistor, load-pull measurements among others.

The load-pull measurement is a common method to determine certain measures of performance versus the load impedance seen by the device. The load impedance is varied, either with a mechanical tuner, or by active injection. By varying the load impedance, measures such as maximum output power, maximum efficiency, and maximum gain are obtained. Source-pull measurements can also be performed in order to maximize the power gain of a device.

2.1.1 Passive load-pull

Passive load-pull implies that a mechanical tuner, or another tunable passive network, determines the load impedance. A typical setup is shown in Figure 2.3. Load-pull using a mechanical tuner is the current industry standard because of the high power handling capabilities and setup simplicity. However, there are several drawbacks using a passive setup. The major drawback is losses between the tuner and the device under test (DUT) in the passive setup, especially problematic when performing harmonic load-pull and on-wafer measurements. The losses limit the magnitude of the load reflection coefficient seen by the DUT [13].

2.1.2 Active load-pull

Rather than reflecting the outgoing voltage wave (b_2) from the transistor in an impedance tuner, one can inject the reflected wave by using active injection [14]. Active injection load-pull overcomes the issue with losses by having pre-amplifiers generating the load reflection coefficient. The principle with active load-pull can be seen in the expression for the load refection coefficient, given by:

$$\Gamma_L = \frac{a_2(f_1)}{b_2(f_1)} = \frac{Ae^{j(2\pi f_1+\theta)}}{b_2(f_1)}. \tag{2.1}$$

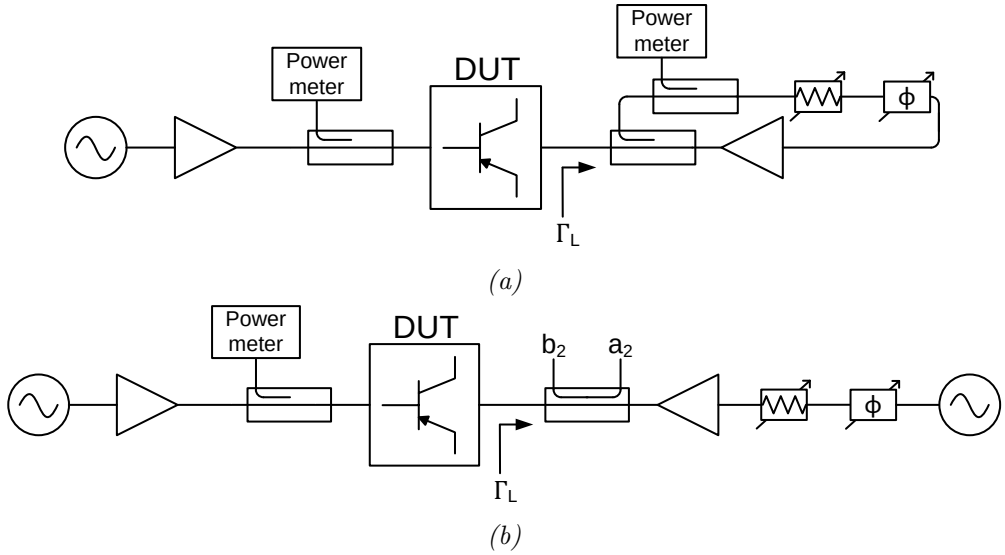


Figure 2.4: Two common types of active load-pull setups. (a), closed loop, (b), open loop.

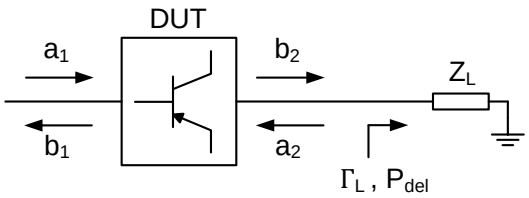


Figure 2.5: DUT with an arbitrary load reflection coefficient and delivered power.

Measuring $b_2(f_1)$ and adjusting the phase and amplitude of $a_2(f_1)$ can therefore present an arbitrary load impedance to the device. The way how the backward travelling wave, $a_2(f_1)$, is generated varies, and usually two types of active load-pull are discussed. The two used methods are often referred to as open loop and closed loop active load-pull [13], and typical setups are shown in Figure 2.4.

Active closed-loop load-pull systems, Figure 2.4a, couples a portion of the wave generated by the DUT. The coupled signal is adjusted in both magnitude and phase and amplified through an amplifier in order to present the wanted load impedance. The response time of the loop is in general short and real-time load-pull with fast characterization is possible. A major drawback with having a closed loop configuration is that it can cause oscillations and special filtering techniques have to be used [15].

Active open-loop load-pull systems inject signals that are generated from another signal source, and is therefore not prone to oscillation. Presenting the wanted load reflection coefficient is however not trivial, especially not for highly non-linear systems. Open-loop systems require a couple of measurement iterations which makes them slower in comparison to a closed-loop system. Algorithms for speeding up open-loop load-pull systems have been proposed and require just a few iterations [16].

Depending on the magnitude of the load reflection coefficient and the delivered power by the device, the power needed from pre-amplifiers will vary accordingly. To estimate the needed power level, consider the setup illustrated in Figure 2.5.

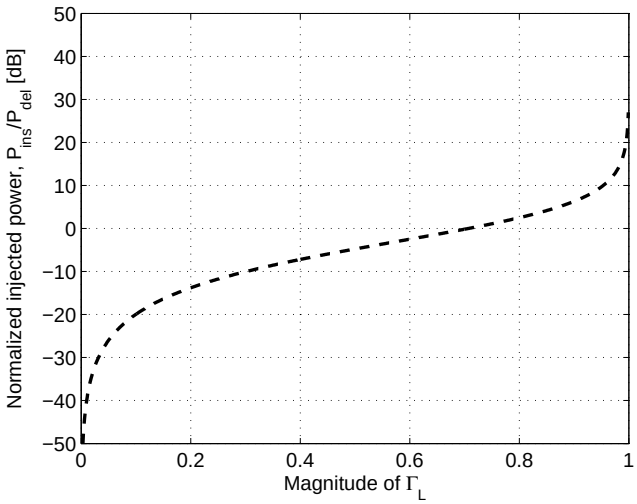


Figure 2.6: Required normalized injected power plotted against the magnitude of the load reflection coefficient.

The load reflection coefficient and delivered power to the load are expressed as

$$|\Gamma_L| = \frac{|a_2|}{|b_2|} \tag{2.2}$$

$$P_{del} = \frac{|b_2^2| - |a_2^2|}{2Z_L}. \tag{2.3}$$

Re-organizing the equations yields the relationship

$$P_{ins} \equiv \frac{|a_2^2|}{2Z_0} = \frac{P_{del} \cdot |\Gamma_L|^2}{1 - |\Gamma_L|^2}. \tag{2.4}$$

For $Z_0 = 50\,\Omega$, this can be visualized as in Figure 2.6. As seen, when injecting the same amount of power into the device as the device itself delivers to the load, a load reflection coefficient with a magnitude of $1/\sqrt{2}$ is seen by the device. Therefore, high power devices that require a load reflection coefficient close to one in magnitude set very high output power requirements on the pre-amplifiers. However, the problem can partly be solved by using an impedance transformer [17].

2.2 Examples of active load-pull systems

Load-pull is today a widespread concept and commercial load-pull systems exist with high accuracy and high performance. More complex systems handling multi-harmonic load-pull and modulated signals exist and are constantly being developed [13], [18], [19], [20]. For the signal acquisition, load-pull systems often use a large signal network analyzer (LSNA) or a nonlinear vector network analyzer (NVNA).

2.2.1 LSNA based load-pull systems

Figure 2.7 illustrates a typical LSNA-based load-pull setup. To reduce the need of high-speed analog-to-digital converters (ADCs), harmonic samplers are used before the analog to digital converters. The harmonic samplers use undersampling, also referred to as harmonic sampling or bandpass sampling, to downconvert the radio frequency (RF) spectrum to an intermediate

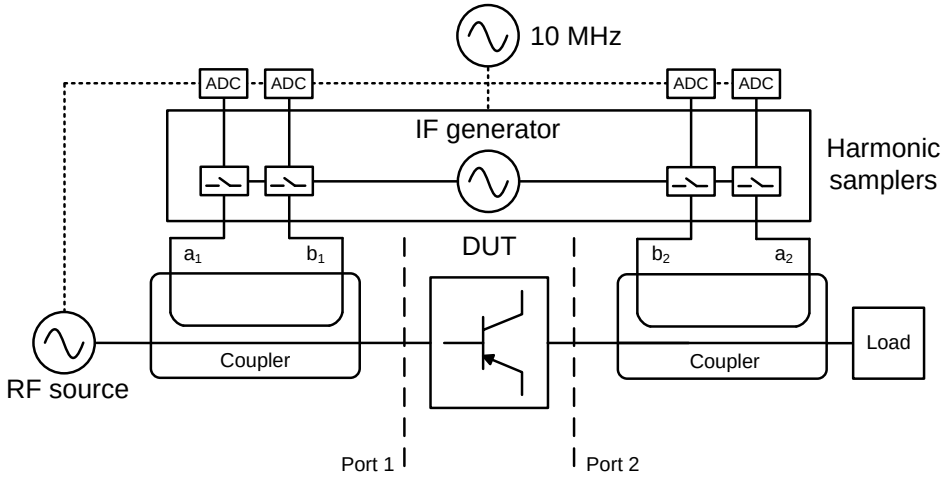


Figure 2.7: Typical LSNA load-pull configuration.

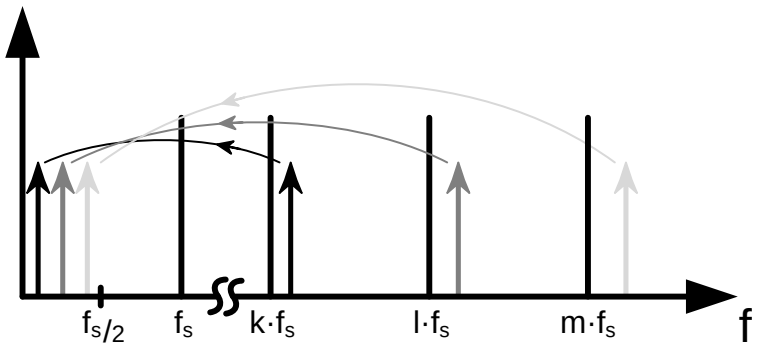


Figure 2.8: Harmonic sampling working principle.

frequency (IF) measurable by the ADCs. Figure 2.8 illustrates the working principle of harmonic sampling. By choosing the sampling frequency of the harmonic samplers carefully, in other words avoiding frequency overlapping, a compressed RF spectrum can be measured by the ADCs. However, all of the frequency components of interest must be known and specified in order to calculate a suitable sample frequency. Performing a short, open, load, thru (SOLT) calibration together with a power calibration and phase calibration at the DUT ports gives full description of the travelling waves a_1, b_1, a_2 and b_2 in terms of magnitude and phase.

Some advantages of an LSNA are [21]:

- The compressed RF spectrum is sampled in one shot, minimizing the acquisition time and eliminating phase synchronization problems
- It is very suitable for CW measurements and modulated measurements are easy to perform

Some disadvantages of an LSNA are [21]:

- Low signal-to-noise ratio (SNR) compared to an NVNA-based solution
- Depending on the harmonic phase reference used, the phase calibration grid is set thereafter

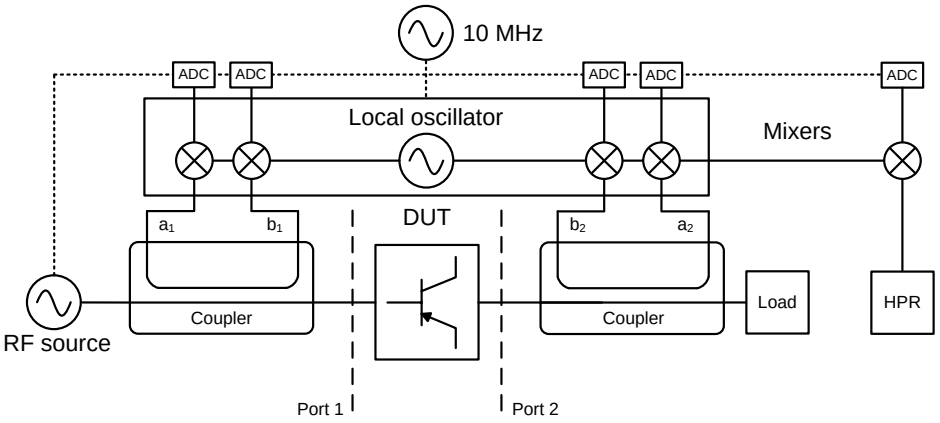


Figure 2.9: Typical NVNA load-pull configuration, HPR: harmonic phase reference.

2.2.2 NVNA based load-pull systems

An NVNA-based setup is shown in Figure 2.9. Compared to the LSNA, the NVNA is based on heterodyne mixers where the local oscillator is swept according to the wanted spectral components. Each frequency is therefore measured independently which introduces phase synchronization problems. To enable correct reconstruction of the waveforms, a known synchronization signal needs to be measured by a fifth measurement receiver, a harmonic phase reference (HPR). Performing a SOLT calibration and a power and phase calibration allows for description of the travelling waves in both magnitude and phase.

Some advantages of an NVNA are [21]:

- Higher SNR than an LSNA-based solution
- Very suitable for CW measurements

Some disadvantages of an NVNA are [21]:

- Each spectral component is measured separately which increases acquisition time
- Modulated measurements are possible but not as straight-forward as with an LSNA

Chapter 3

Multi-band active load-pull system

In this thesis a new type of measurement system is used, shown in Figure 3.1. A picture taken of the multi-band active load-pull system is shown in Figure 3.2. The multi-band load-pull principle is illustrated in Figure 3.3. The main system components are an Oscilloscope (Rohde & Schwarz RTO1044) for waveform acquisition and an Arbitrary Waveform Generator (AWG) (Agilent Technologies M8190A). These two instruments gives the system its multi-band load-pull capabilities [22].

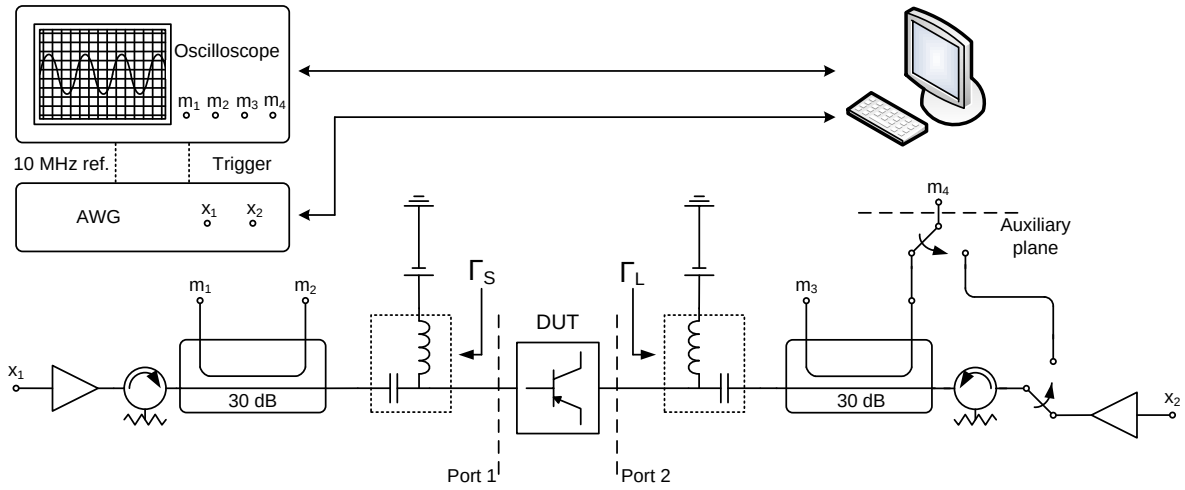


Figure 3.1: Schematic of the multi-band active load-pull system.

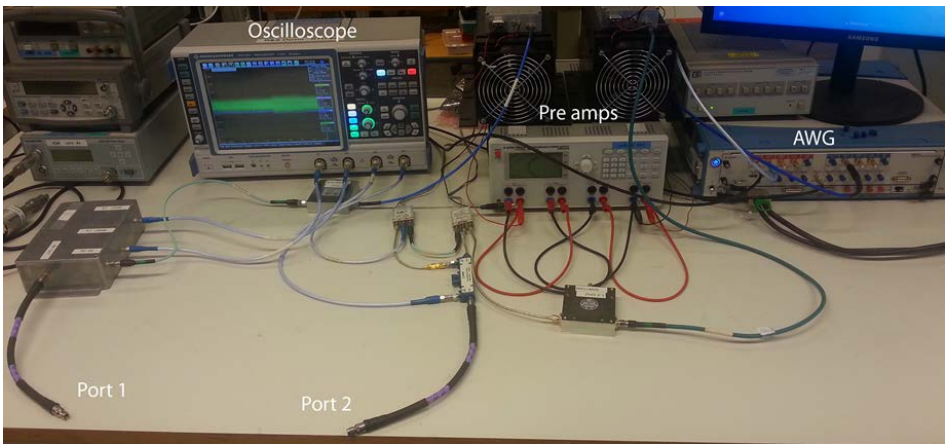


Figure 3.2: Full setup of the multi-band active load-pull system.

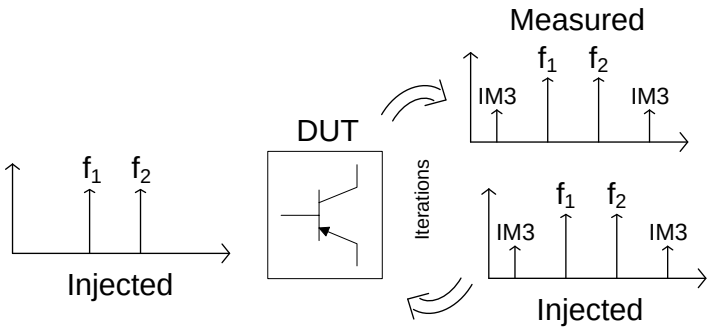


Figure 3.3: Injection of a two tone signal into a non-linear device, and the multi-band load-pull working principle.

3.1 Bandwidth and frequency resolution

In an oscilloscope the complete waveform is instantaneously sampled, either with one high speed ADC or by several interleaved ADCs. By setting a certain sample frequency, f_s, and number of samples, $N_{samples}$, a measurement bandwidth and frequency resolution is automatically set. The frequency resolution is given by

$$\Delta f = \frac{f_s}{N_{samples}}. \tag{3.1}$$

The frequency resolution can be very narrow, since it is only limited by the amount of memory available in the oscilloscope. The oscilloscope has an analog bandwidth which limits the maximum measurable frequency, in this case 4 GHz. The signals are generated with a two channel 8 GSa/s, 14-bit resolution AWG. It has a bandwidth of 4 GHz and thus covering the whole bandwidth of the oscilloscope. A unique property of the AWG is that a multi-tone excitation across the entire bandwidth can be performed.

3.2 Calibration and calibration verification

A SOLT calibration is first performed at the two DUT ports of the system. The calibration algorithm is based on the methods presented in [23] and [24]. An auxiliary plane is then introduced at the fourth oscilloscope port, m_4 in Figure 3.1. A through standard is connected between port 1 and port 2, and the states of the switches are changed, providing a direct path for the forward travelling wave. A SOL calibration is performed at the new reference plane together with a power and phase calibration.

For verification, a power meter was connected to port 1 and 2 and the input power was swept from 0 dBm to 38 dBm. The difference between the power measured with the power meter and the power measured with the measurement system is plotted in Figure 3.4. The error varies approximately $\pm$ 0.1 dB over the power sweep. This is fully acceptable since the measurement uncertainty of a power meter is usually larger [25].

3.3 Design and manufacturing of a diplexer

Due to power limitations of available pre-amplifiers for the load-pull system, two amplifiers with different frequency ranges were combined to obtain higher input power at each frequency band. A low loss diplexer was found to be the most suitable solution to combine the different amplifiers. A diplexer is a three-port passive component and it is the simplest form of a multiplexer. A multiplexer splits the input signal in frequency domain from one common port to several ports by filtering. Therefore, there must be a frequency offset between the desired signals so that the filtering works correctly. A bias-tee is a common type of diplexer.

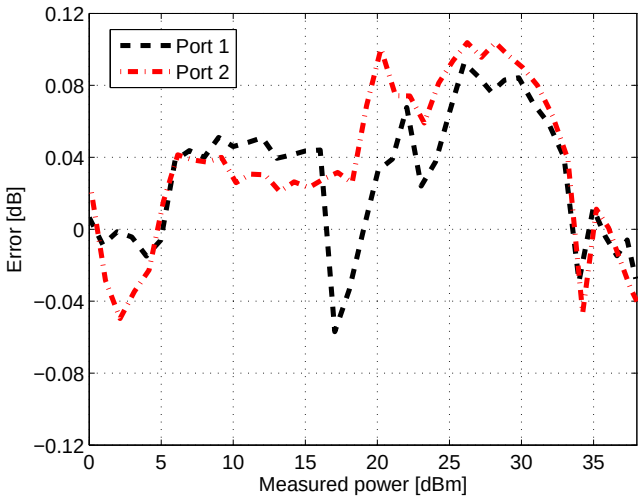


Figure 3.4: Power calibration verification against a power meter.

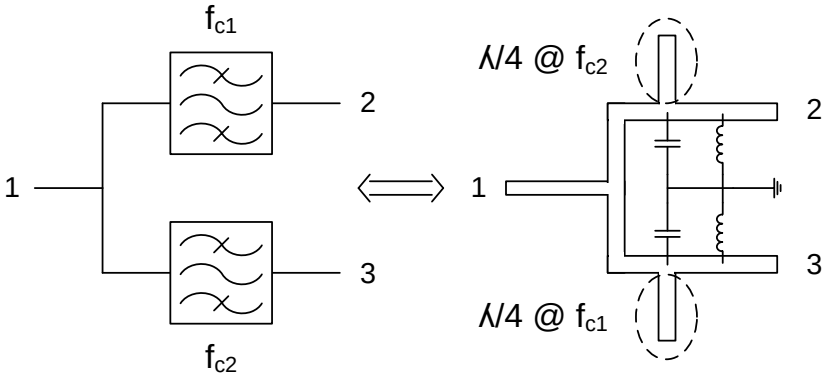


Figure 3.5: Left, working principles behind a diplexer, right, its implemented equivalent.

No commercial diplexers at the specific frequencies of interest were available and therefore a diplexer had to be designed and manufactured. The specifications for the diplexer was 1.63-2.14 GHz on the first port, 2.65-3.16 GHz on the second port and an insertion loss below 1.5 dB at the desired frequencies.

3.3.1 Diplexer theory

The most common types of diplexers are based on stub filters or Lange coupler filters. In this case, an open stub solution combined with an LC-resonance circuit is used, as illustrated in Figure 3.5. The open stub acts as a quarter-wave transformer which short circuits the frequency of interest. However, two open stubs in parallel would short circuit both frequencies at the same time, and thus some transmission line is needed in between in order to get the desired filtering effect. The circuit can be theoretically analyzed by simplifying the problem and looking at one branch at a time and removing the resonance circuits, as shown in Figure 3.6.

Using the formula for impedance propagation for a lossless transmission line

$$Z_{in} = Z_c \frac{Z_L + jZ_c tan(\beta l)}{Z_c + jZ_L tan(\beta l)}, \tag{3.2}$$

the lengths of the transmission lines L_1, L_2, L_3 and L_4 fulfilling the requirements can be

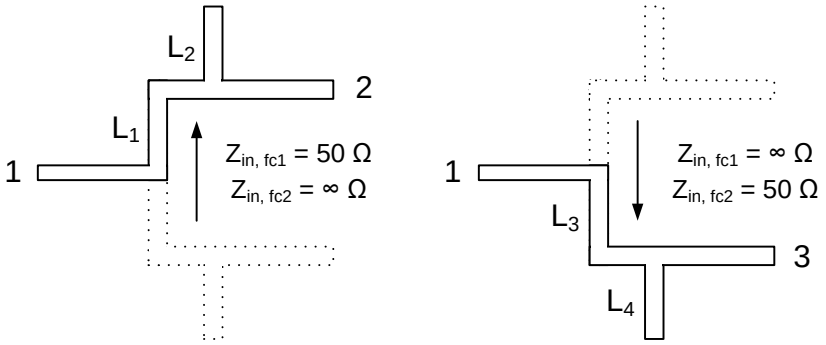


Figure 3.6: Left, requirements for port 2, right, requirements for port 3.

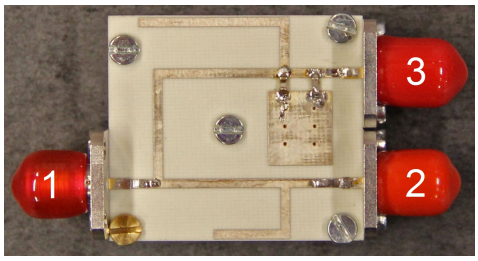


Figure 3.7: Assembled diplexer. Input port, left, output port 1.63-2.14 GHz, lower right, output port 2.65-3.16 GHz, upper right.

found. The calculations are straight-forward for a single branch, however analytically solving the equations for two branches in parallel is not possible and the problem becomes a matter of optimization.

3.3.2 Design and layout

Using the optimization tool in ADS, the transmission lines on port 2 were found to be $L_1 = 16.8$ mm and $L_2 = 12.5$ mm. The lengths on port 3 were $L_3 = 14.0$ mm and $L_4 = 22.5$ mm. EM simulations almost resulted in the same lengths. Some space was conserved by folding the open stub transmission lines parallel with the branches. A picture of the fully assembled diplexer is shown in Figure 3.7. The diplexer PCB was mounted on a 1 cm thick aluminium fixture and a 1 pF capacitor and 100 nH inductor were soldered on the transmission line at port 3. The design is very compact and the fixture measures only 26.55 mm x 30 mm.

3.3.3 S-parameter measurements

The S-parameters of the device were measured with a calibrated VNA and compared with simulations. The results are shown in Figure 3.8. In overall, measurements and simulations show very good agreement. The most important result is the insertion loss, seen in Figure 3.8a. The insertion loss at the frequencies of interest is summarized in Table 3.1. The design goals of the diplexer were met for all frequencies except 3.16 GHz. This will not affect the measurements significantly, since it is an intermodulation frequency and low power will be generated by the device at that frequency.

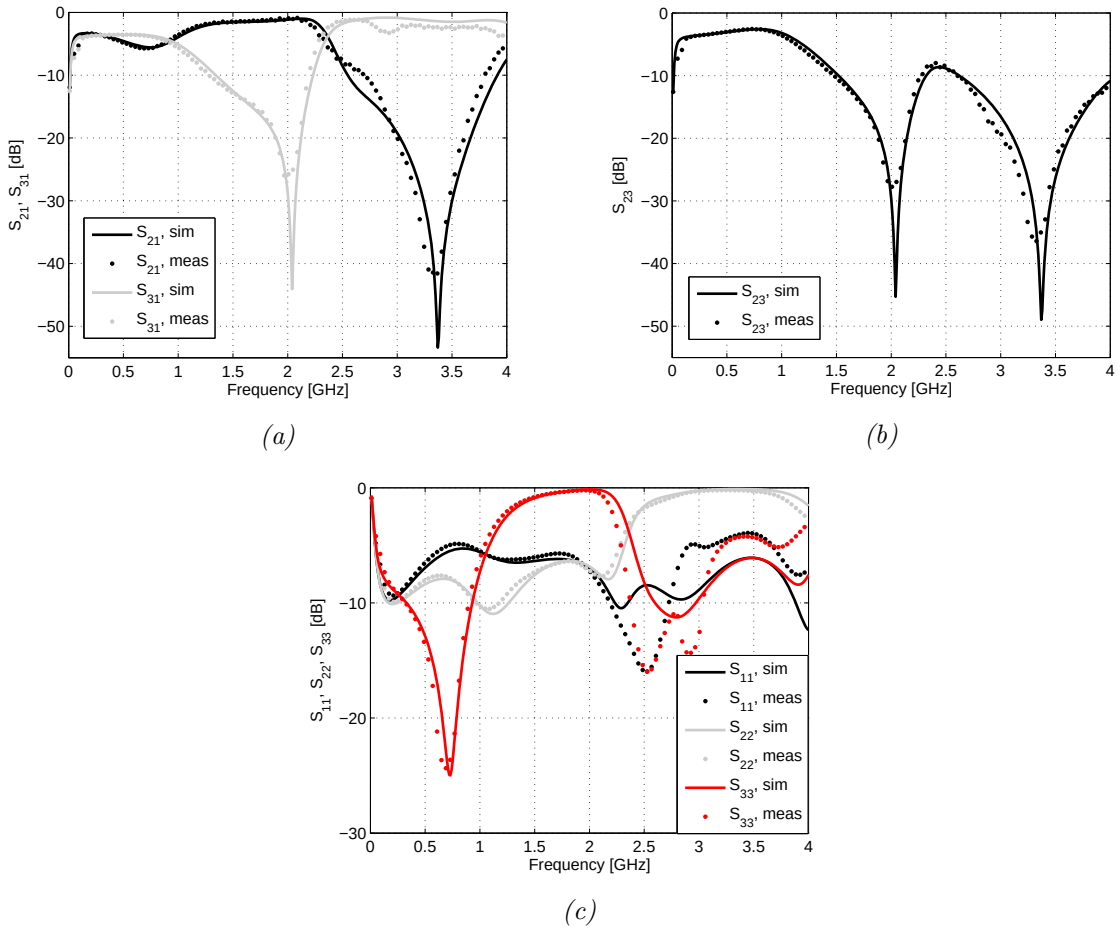


Figure 3.8: Simulated and measured S-parameters of the diplexer. (a), insertion loss, (b), isolation between the output ports, (c), S_{11}, S_{22} and S_{33}.

Table 3.1: Insertion loss of diplexer at frequencies of interest

Frequency	Loss [dB]
1.63 GHz	1.4
2.14 GHz	1.3
2.65 GHz	1.2
3.16 GHz	2.1

Chapter 4

Device characterization

This thesis involves the study of a commercially available Cree 6 W RF Power GaN HEMT, model number CGH40006P. The transistor comes in a packaged form and is suited for general purpose, broadband applications. The typical drain bias condition is 28 V and it has a gate threshold voltage between -3.8 V and -2.3 V. The device is very rugged due to the GaN technology, and can withstand drain voltage peaks up to 120 V. The transistor provides a minimum of 10 dB small signal gain over the frequency range 500 MHz to 6 GHz and a minimum output power of 7 W.

Simulations and measurements of the device were carried out at the frequencies 2.14 GHz and 2.65 GHz. They represent carrier frequencies at two LTE bands and the spacing between them is larger than the bandwidth of a LTE channel (typically 5 or 20 MHz). Furthermore, the available lab equipment is well suited to measure at these frequencies.

The gate bias voltage of the device was chosen to obtain a flat gain versus input power. This corresponded to a voltage of -2.7 V for the measured device, and -3.15 V for the simulations. The drain bias voltage was set to 25 V, because of power limitations in the pre-amplifiers.

An ADS model of the device is provided by the manufacturer and this chapter will start with model simulations and some brief non-linear theory followed by device measurements and model verification.

4.1 Device simulations

A number of device simulations have been conducted in the simulation software Agilent ADS 2009, and include one tone and two tone load-pull simulations. In order to verify both the theory as well as measurements, two different classes of operation, class A and class AB, were evaluated in the load-pull simulations.

4.1.1 Simulated DC characteristics

The simulated DC characteristics of the device is plotted in Figure 4.1.

The device model has an erronous thermal model, which is seen at high drain and gate voltages. It is unlikely that the simulations are affected since those operating conditions are extremely rare. An estimate of the RF power and optimal resistive load can be carried out with a few calculations. According to [26] the RF power from a transistor can be calculated as

$$P_{fund} = \frac{V_{dc} - V_{knee}}{\sqrt{2}} \cdot \frac{I_{fund}}{\sqrt{2}} = \frac{V_{dc} - V_{knee}}{4\pi} \cdot I_{max} \frac{\alpha - sin(\alpha)}{1 - cos(\alpha/2)}, \tag{4.1}$$

where V_{dc} is the drain bias voltage, I_{max} the maximum possible current available from the device and α the conduction angle. The device has a knee voltage, V_{knee}, which limits the

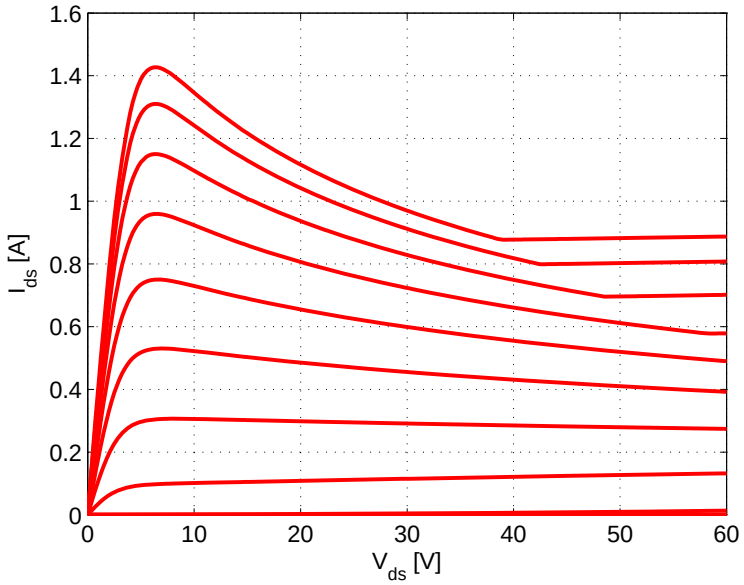


Figure 4.1: DC characteristics of the Cree GaN HEMT from the ADS model illustrating a model error at high gate and drain bias.

voltage swing and therefore reduces the output power. For simplicity, class A bias condition is assumed with a conduction angle of 2π at a drain bias voltage of 28 V. The maximum current of the device is 1.4 A, and a knee voltage of 6 V is extracted from Figure 4.1. The RF power is then

$$P_{fund} = \frac{28-6}{4\pi} \cdot 1.4 \frac{2\pi}{1-(-1)} = 7.7 \text{ W}. \tag{4.2}$$

An estimation of the optimal resistive load, also known as Cripps load, can be done with Equation 4.3.

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_{dc}} = \frac{28-6}{0.7} = 31.4\Omega. \tag{4.3}$$

4.1.2 One tone load-pull simulations

The one tone load-pull environment was set up using the default design guide in ADS, as illustrated in Figure 4.2.

The load impedance was swept over a circular area centered in the second quadrant of the Smith chart, covering the 50 Ω centerpoint and low impedance states. The delivered power to the load was measured with a power meter and is calculated as

$$P_{del} = \Re\left(\frac{V \cdot I^*}{2}\right). \tag{4.4}$$

The efficiency is calculated according to the following formula.

$$\eta_{tot} = \frac{P_{RF,out}}{P_{DC} + P_{RF,in}} \tag{4.5}$$

Driving the transistor with a 24 dBm, 2.14 GHz signal results in the load-pull contour plot shown in Figure 4.3. At this input power, the optimal load reflection coefficient for highest delivered power and highest efficiency coincide, located at $\Gamma_L = 0.28\angle 135°$. The maximum

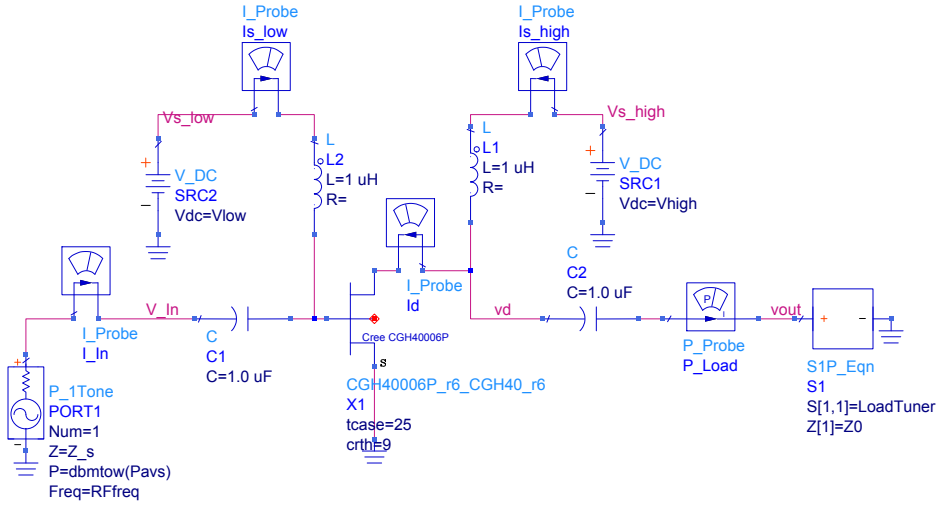
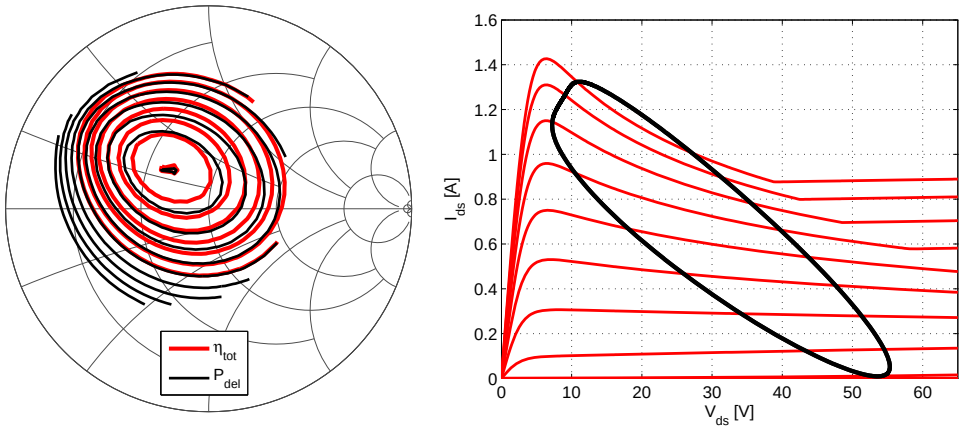


Figure 4.2: One tone load-pull setup in ADS.



(a) *(b)*

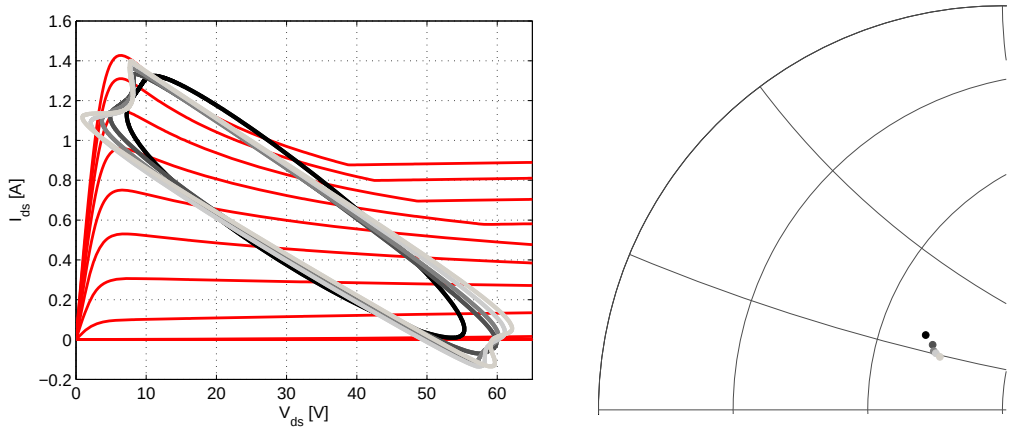
Figure 4.3: Load-pull simulation at 24 dBm input drive. (a), efficiency and delivered power having a step size of 2% and 0.5 dBm respectively, (b), load-line at the impedance point for highest delivered power.

delivered power is 38.5 dBm and the maximum efficiency is 35%. The load-line has a relatively low distortion, mostly being knee-voltage compression.

The distortion of the load-line versus input power is plotted in Figure 4.4, where the input power is varied from 24 dBm to 32 dBm in 2 dB steps. At 32 dBm input power the load-line suffers from serious compression and higher order harmonics are generated. However, the slope and overall shape of the load-line is more or less constant meaning that the optimal load reflection coefficient does not change, which is verified in Figure 4.4b.

The contour lines for efficiency and delivered power at an input power of 32 dBm is plotted in Figure 4.5. The optimal load reflection coefficients for highest delivered power and highest efficiency no longer coincide and has a slightly different behaviour compared to the load-pull at 24 dBm input power. As a result from this, there is now a trade-off between high output power and high efficiency. The load reflection coefficient for highest delivered power is $\Gamma_{L,opt,pdel} = 0.22\underline{/139°}$, and the load reflection coefficient for highest total efficiency is $\Gamma_{L,opt,eff} = 0.30\underline{/122°}$. The device delivers maximally 40.65 dBm of output power, and a highest efficiency of 56%.

Adjusting the bias point of the transistor to a gate-source voltage of -3.15 V, drain-source



(a) *(b)*

Figure 4.4: Load-pull with power sweep. (a), distortion of the load-line due to increased input power, (b), change in optimal load reflection coefficient for highest delivered power.

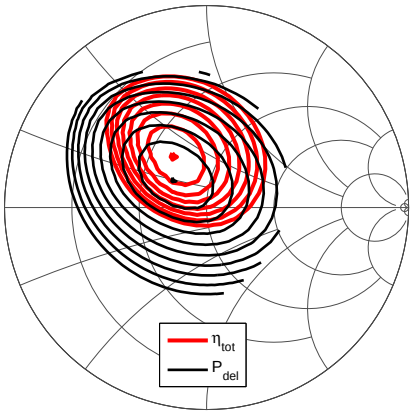
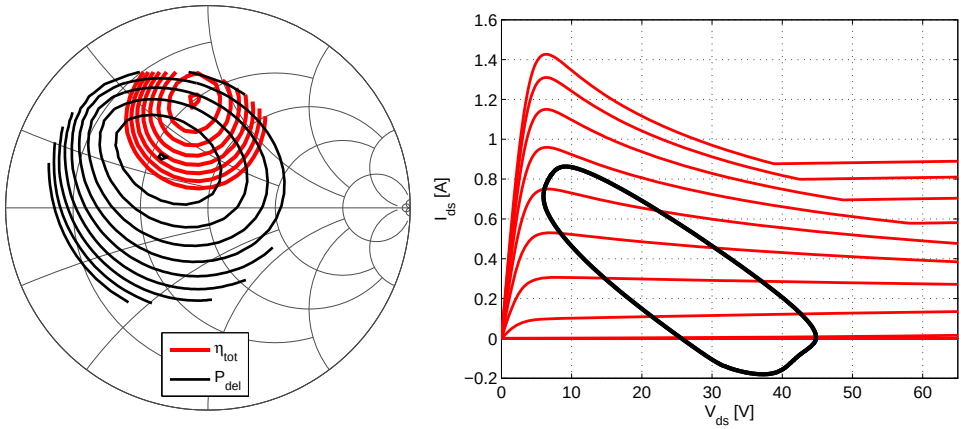
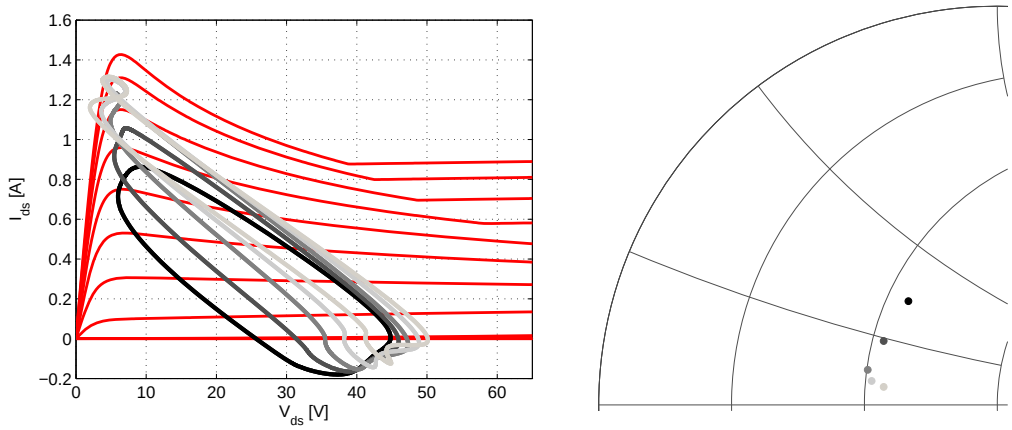


Figure 4.5: Load-pull contour plot, 32 dBm input power, showing efficiency and delivered power. The contour lines have a step size of 0.5 dBm and 2%.



(a) (b)

Figure 4.6: Load-pull simulation at 24 dBm input drive, with new bias point. (a), efficiency and delivered power having a step size of 2% and 0.5 dBm respectively, (b), load-line at the impedance point for highest delivered power.



(a) (b)

Figure 4.7: Load-pull with power sweep and new bias point. (a), distortion of the load-line due to increased input power, (b), change in optimal load reflection coefficient for highest delivered power.

voltage of 25 V and lowering the input power to 24 dBm yields the plots shown in Figure 4.6. Changing the bias point affects the transistor operation. This is shown in the load-line, where a lower gate-source bias voltage and a lower drain-source bias voltage results in a sharper slope of the load-line to maintain full current swing. Therefore, the device requires a lower impedance as seen in Figure 4.6a. Also, the optimal load reflection coefficients for η_{tot} and P_{del} are farther apart and the trade-off is more clear. The device delivers a maximum of 36.4 dBm and the maximum efficiency is increased to 65%. The optimal load reflection coefficients are $\Gamma_{L,opt,pdel} = 0.32\angle 129°$ and $\Gamma_{L,opt,eff} = 0.50\angle 99°$.

Sweeping the input power from 24 dBm to 32 dBm with the new bias point has more apparent effects on the load-line and optimal load reflection coefficient, as shown in Figure 4.7. Compared to before, where the load-line barely changed, increasing input power alters the shape and shifts the load-line significantly.

The contour lines for efficiency and delivered power for 32 dBm input power are shown in Figure 4.8. Compared to Figure 4.6, the two optimal load reflection coefficients are rotated counter clockwise slightly towards the negative real axis. They are now located at $\Gamma_{L,opt,pdel} =$

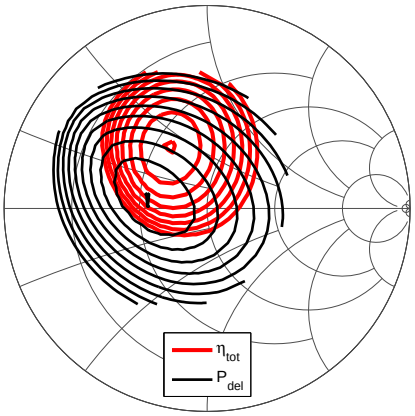


Figure 4.8: Load-pull contour plot with changed bias, 32 dBm input power, showing efficiency and delivered power. The contour lines have a step size of 0.5 dBm and 2%.

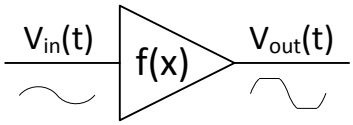


Figure 4.9: Amplifier blackbox with a sinusoidal input signal and a distorted output signal.

$0.29\underline{/166°}$ and $\Gamma_{L,opt,eff} = 0.32\underline{/122°}$, and the device delivers a maximum of 40 dBm output power and the highest possible efficiency is 68%.

The simulations for 2.65 GHz have a similar behaviour, except that it has lower gain and thus require a higher input drive. Simulations for 2.65 GHz are therefore not shown since they do not add much information about the device.

4.1.3 Nonlinear effects theory, intermodulation distortion

Because of non-linearities in the device, the output signal will be distorted in large signal operation. Apart from harmonic distortion, the device will suffer from intermodulation distortion. This phenomenon occurs when the device is excited with two or more tones. Consider the non-linear amplifier illustrated in Figure 4.9. Exciting the device with a two-tone signal and using Taylor expansion, the input and output signal can be expressed as

$$v_{in} = cos(\omega_1 t) + cos(\omega_2 t) \tag{4.6}$$

$$v_{out}(v_{in}) = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \ldots, \tag{4.7}$$

where a_0, a_1, a_2 and a_3 are Taylor coefficients. The expansion is limited to the third order to keep the complexity on a moderate level. Inserting Eq. (4.6) into Eq. (4.7) leads to

$$\begin{aligned} v_{out} = a_0 &+ a_1(cos(\omega_1 t) + cos(\omega_2 t)) + a_2(cos^2(\omega_1 t) + 2cos(\omega_1 t)cos(\omega_2 t) + cos^2(\omega_2 t)) \\ &+ a_3(cos^3(\omega_1 t) + 3cos^2(\omega_1 t)cos(\omega_2 t) + 3cos(\omega_1 t)cos^2(\omega_2 t) + cos^3(\omega_2 t)) \\ &+ \ldots. \end{aligned} \tag{4.8}$$

There are a number of multiplicative terms in the expression above and by using trigonometric identities, the harmonic and intermodulation distortion can be analyzed.

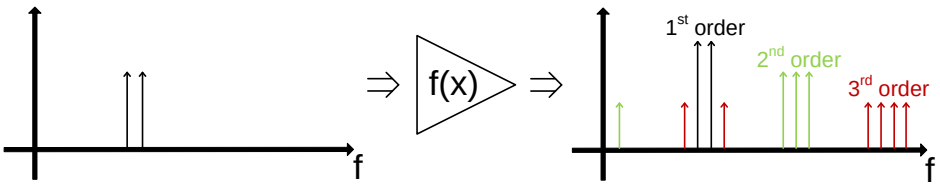


Figure 4.10: Non-linear distortion in an amplifier in frequency domain. First, second and third order terms are shown.

$$cos^2(x) = \frac{cos(2x)+1}{2} \tag{4.9}$$

$$2cos(x)cos(y) = cos(x-y)+cos(x+y) \tag{4.10}$$

$$cos^3(x) = \frac{3cos(x)+cos(3x)}{4} \tag{4.11}$$

$$3cos^2(x)cos(y) = \frac{3}{4}(2cos(y)+cos(2x-y)+cos(2x+y)) \tag{4.12}$$

The frequency components are shown in Figure 4.10. In general, for a multi-tone excitation in a non-linear device:

- If $v_{in} = cos(\omega_1 t) + cos(\omega_2 t) + \ldots + cos(\omega_N t)$
- v_{out} will contain: $k_1\omega_1 + k_2\omega_2 + \ldots + k_N\omega_N$, where $k = \pm 1, \pm 2 \ldots$
- The order is defined as: $O = |k_1| + |k_2| + \ldots + |k_N|$

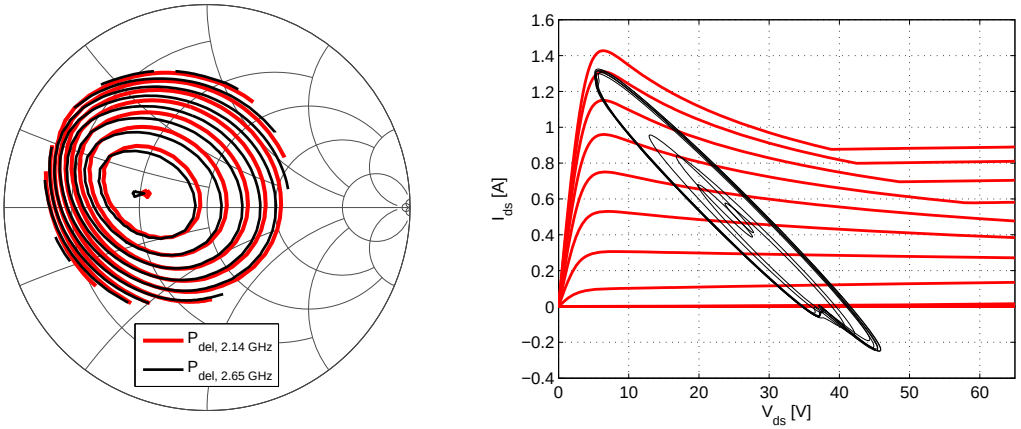
4.1.4 Two tone load-pull simulations

Two tone simulations in ADS were performed in a similar way as the one tone simulations. A second tone was added to the signal source and the input powers at each tone were adjusted to give approximately the same output power at each tone. For simplification, the load impedance presented at the two frequencies were set to be equal. For accurate two tone load-pull simulations, the load reflection coefficients $\Gamma_{L,f1}$ and $\Gamma_{L,f2}$ should be swept independently of each other. The load reflection coefficients are complex numbers which would lead to a four-dimensional sweep. This would give more reliable simulations but at the cost of complexity. The two-tone simulations performed in ADS were mainly used for investigating harmonic generation and intermodulation distortion.

Driving the transistor into saturation, meaning input power levels of 27 dBm at 2.14 GHz and 28 dBm at 2.65 GHz, gave the contour plot and load-line shown in Figure 4.11. As seen in Figure 4.11a, the contour lines are approximately the same for the two frequencies. This might not be an accurate result because of the simplification introduced.

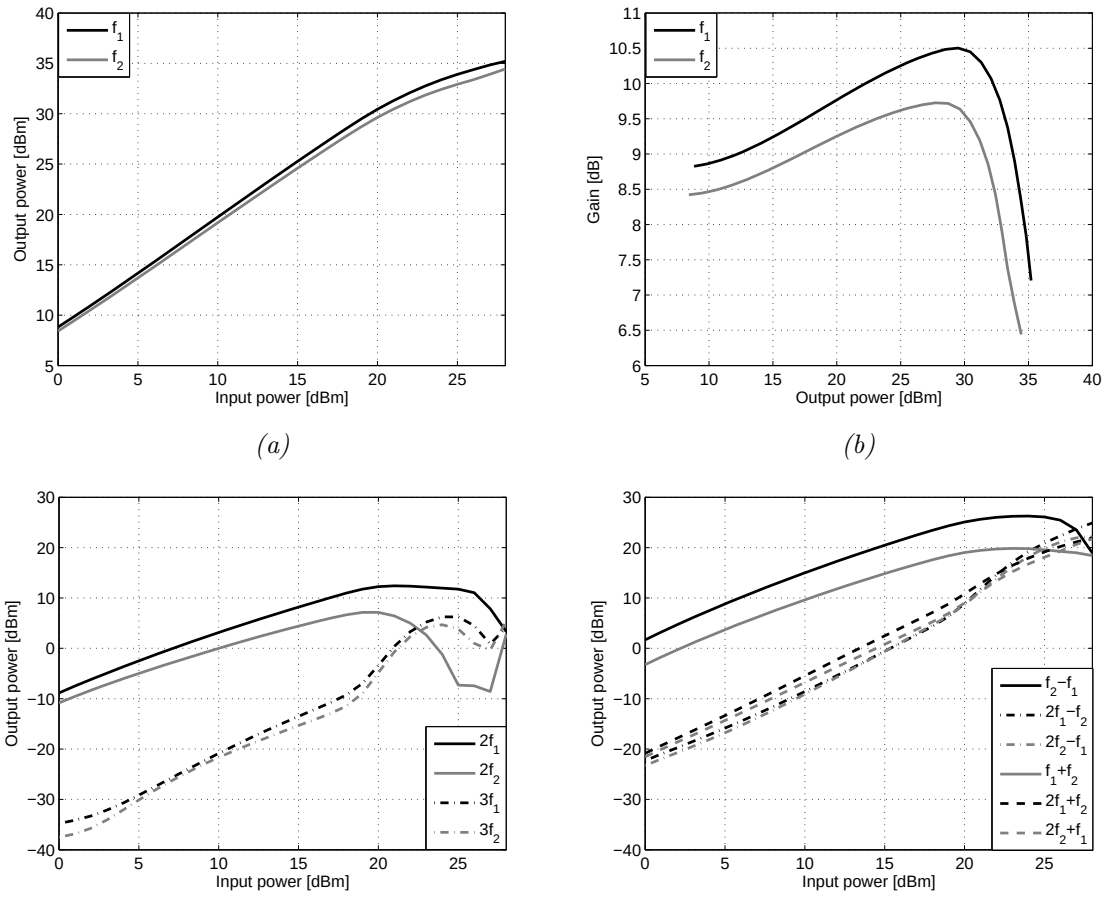
By replacing the load impedance tuner in the simulation setup with a fix load impedance, acquired from the two-tone load-pull simulation in Figure 4.11a, the analysis of harmonic generation and intermodulation distortion can be carried out. Sweeping the input power from -1 dBm to 27 dBm at 2.14 GHz and 0 dBm to 28 dBm at 2.65 GHz, corresponding to transistor saturation, gives the non-linear behaviour of the transistor, shown in Figure 4.12.

A slight gain expansion is noted in Figure 4.12b indicating a Class B/C operation. An important result from these simulations is that there is more energy in the intermodulation products than in the harmonics. A proper termination of the intermodulation products could therefore have a significant impact on the efficiency. The base-band intermodulation product (IM2) is particularly high over the power sweep. The third order intermodulation products have approximately the same power level, as expected from theory.



(a) *(b)*

Figure 4.11: Two tone load-pull simulations. (a), contour plot of the delivered power having a step size 0.5 dBm, (b), load-line at the optimal load reflection coefficient.



(a) *(b)*

(c) *(d)*

Figure 4.12: Two tone power sweep simulation, -1 dBm to 27 dBm at 2.14 GHz (f_1), and 0 dBm to 28 dBm at 2.65 GHz (f_2). (a), output power versus input power, (b), gain versus output power, (c), harmonic power levels versus input power, (d), intermodulation power levels versus input power.

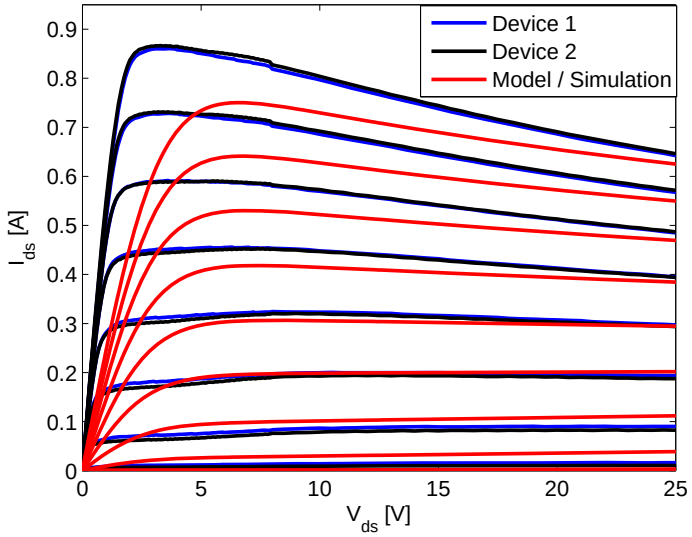


Figure 4.13: DC characteristics of the Cree device, measured on two devices versus simulated.

4.2 Device measurements

A series of measurements were carried out with the multi-band active load-pull system presented in Chapter 3. The transistor was mounted in a high power fixture and connected to the load-pull system. A full two port calibration was made in order to be able to describe the travelling waves with correct magnitude and phase. DC measurements were carried out first, followed by one tone load-pull measurements, two tone load-pull measurements and intermodulation load-pull measurements.

4.2.1 Measured DC characteristics

An IV measurement of the device was carried out, plotted in Figure 4.13. The measurements were limited to a maximum of $V_{gs} = -1$ V and $V_{ds} = 25$ V in order not to stress the device too much. Compared to the simulated DC characteristics in Figure 4.1, the measurements show a discrepancy in the knee voltage. GaN devices suffer from dispersion and by adjusting the IV characteristics in the supplied model, this effect can be compensated for.

The RF power can be estimated from the DC measurements by assuming a maximum current of 1.4 A, a knee voltage of 3 V from Figure 4.13 and biasing the device to a Class A operation, resulting in:

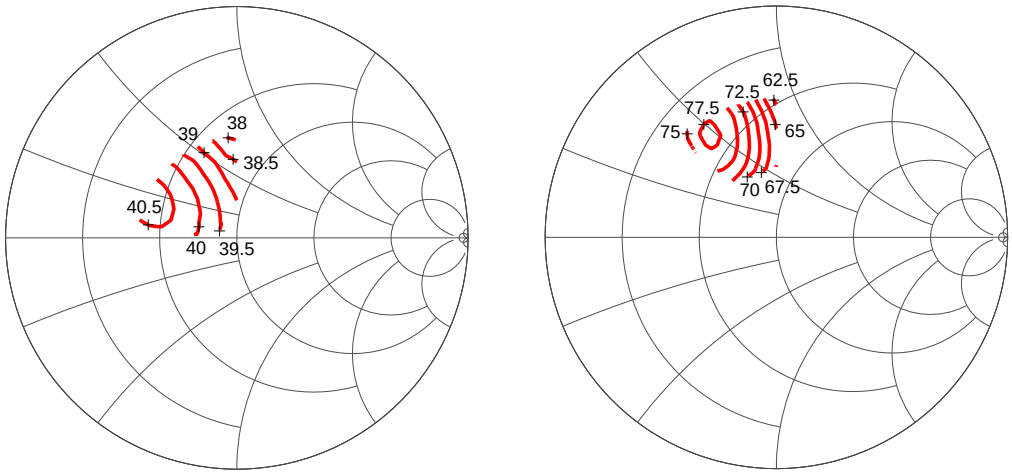
$$P_{fund} = \frac{28-3}{4\pi} \cdot 1.4 \frac{2\pi}{1-(-1)} = 8.75 \text{ W}. \tag{4.13}$$

It is slightly higher than simulated because of the lower knee voltage. The optimal resistive load given by:

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_{dc}} = \frac{28-3}{0.7} = 35.7\Omega. \tag{4.14}$$

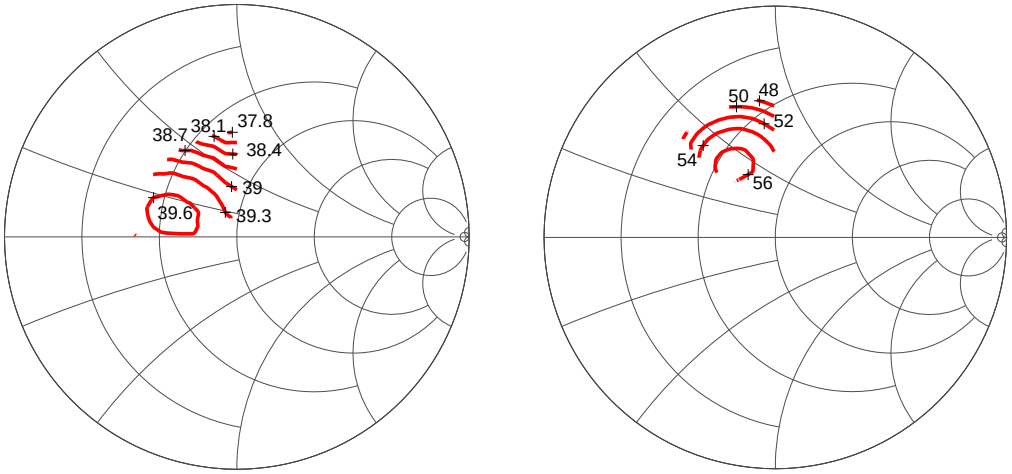
4.2.2 One tone load-pull measurements

An input power sweep was made in order to determine the saturated output power, P_{sat}. Further on, especially for the two tone load-pull measurements, it is much easier to compare results for a well defined measure of performance. For this device and bias point, the 1 dB



(a) (b)

Figure 4.14: One tone load-pull measurements at 2.14 GHz. (a), delivered power load-pull contours, (b), total efficiency.



(a) (b)

Figure 4.15: One tone load-pull measurements at 2.65 GHz. (a), delivered power load-pull contours, (b), total efficiency.

compression point is hard to define due to gain expansion and variation between the two frequencies. Saturated output power is better defined since this is the maximum output power that a device can generate. The input power required to saturate the device occured at around 30 dBm at 2.14 GHz, and around 32 dBm at 2.65 GHz.

Delivered power and total efficiency at 2.14 GHz are shown in Figure 4.14. The load reflection coefficient for maximum delivered power occurs at $\Gamma_{L,opt,Pdel} = 0.40\underline{/160°}$ and the power available at this load impedance is 40.7 dBm. For maximum total efficiency, the optimal load reflection coefficient is $\Gamma_{L,opt,eff} = 0.51\underline{/124°}$ and the corresponding efficiency is 78%.

Delivered power and total efficiency at 2.65 GHz are shown in Figure 4.15. One tone load-pull measurements at 2.65 GHz reveal that both optimal load reflection coefficients move inwards toward origo. The optimal load reflection coefficient for maximal delivered power, 39.7 dBm, occurs at $\Gamma_{L,opt,Pdel} = 0.29\underline{/164°}$ and for maximal total efficiency, 57%, at $\Gamma_{L,opt,eff} = 0.36\underline{/122°}$.

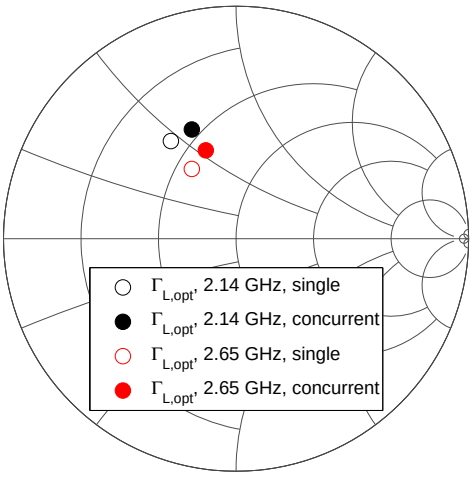


Figure 4.16: Change in optimal load reflection coefficient when the transistor is operated in concurrent transmission mode compared to single transmission mode.

4.2.3 Two tone load-pull measurements

For proper two tone load-pull it is required that a nested sweep is performed. This implies that the load reflection coefficient at one tone is locked and the load reflection coefficient at the other tone is swept over the specified area in the Smith chart. The load reflection coefficient at the first tone is then changed and the sweep at the second frequency starts over. Due to the multi-variable complexity it is in general hard to visualize the results in graphic form.

The input power at 2.14 GHz was set to 27 dBm and at 2.65 GHz it was set to 28 dBm. At these input powers the transistor was saturated and the output power at each tone was approximately the same. This is important since if one tone is dominant it will affect the efficiency. The total efficiency for two tone operation is defined as Eq. (4.15).

$$\eta_{tot} = \frac{P_{RF,out,2.14GHz} + P_{RF,out,2.65GHz}}{P_{DC} + P_{RF,in,2.14GHz} + P_{RF,in,2.65GHz}}. \tag{4.15}$$

At concurrent transmission, a total efficiency of 42% was obtained and the optimal load reflection coefficient rotated clockwise in the Smith chart as plotted in Figure 4.16. Even though the change in optimal load reflection coefficient is not large, it is clearly visible. The new load reflection coefficients are located at $\Gamma^{2.14}_{L,opt,eff} = 0.51\underline{/112°}$ and $\Gamma^{2.65}_{L,opt,eff} = 0.4\underline{/109°}$. This result shows that a measurement system discussed in the previous chapter is important for the analysis of concurrent multi-band power amplifiers.

4.2.4 Intermodulation load-pull measurements

Along with two-tone load-pull measurements, intermodulation load-pull measurements were carried out. The procedure is similar as before; the impedances at the fundamental frequencies were set to the obtained optimum values and the load reflection coefficients at the third order intermodulation products, 1.63 GHz and 3.16 GHz, were set to one in magnitude while the angle was swept from -180 to 180 degrees.

An illustration of the intermodulation load-pull grid is shown in Figure 4.17 and the results are shown in Figure 4.18. The gain variations at the two frequencies have slightly different dependence on the intermodulation termination but both vary about 0.8 dB across the grid. The important result here is the total efficiency which varies from 41.5% to 46%. Optimizing

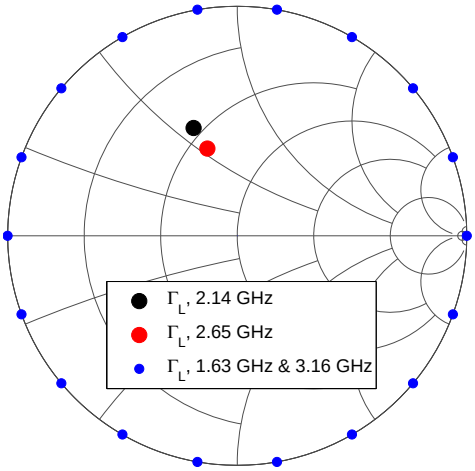


Figure 4.17: Measurement grid of the intermodulation load-pull.

for highest total efficiency results in the load reflection coefficients $\Gamma_{L,opt,eff} = 1\underline{/80°}$ and $\Gamma_{L,opt,eff} = 1\underline{/140°}$ at 1.63 GHz and 3.16 GHz, respectively.

4.2.5 Memory effects

Memory effects in the GaN transistor were visible when performing fast acquisition load-pull. When performing load-pull with short acquisition times for an area in the Smith-chart, as in the one tone load-pull in Figure 4.15, the device had a normal behaviour. However, when sweeping over a larger area in the Smith chart, as in the intermodulation load-pull, the results could vary depending on acquisition times, number of points, etc. For the intermodulation load-pull in Figure 4.18 a CW excitation was used. An example of how the total efficiency can be distorted due to memory effects is shown in Figure 4.19. In comparison to the measurements in Figure 4.18d the optimal load reflection coefficient angles at the IM3 frequencies now seem to be located at around 0 degrees.

4.2.6 Model evaluation, load-pull simulations versus measurements

A model evaluation was performed by comparing simulated and measured load-pull results. Although affecting the simulations very little, the harmonic terminations in ADS were set to the measured terminations in the multi-band load-pull system.

The load-pull contours of delivered power and total efficiency for single tone excitation at 2.14 GHz and 2.65 GHz were compared. 2.14 GHz simulations and measurements are shown in Figure 4.20. The model shows discrepancies in the absolute levels of both delivered power and total efficiency at 2.14 GHz, however the optimal load reflection coefficient for delivered power is comparable to the measured result.

In Figure 4.21 the 2.65 GHz simulations and measurements are plotted. The model is better at predicting the device when operating at 2.65 GHz. Both the absolute values agree better and the optimal load terminations are closer to each other.

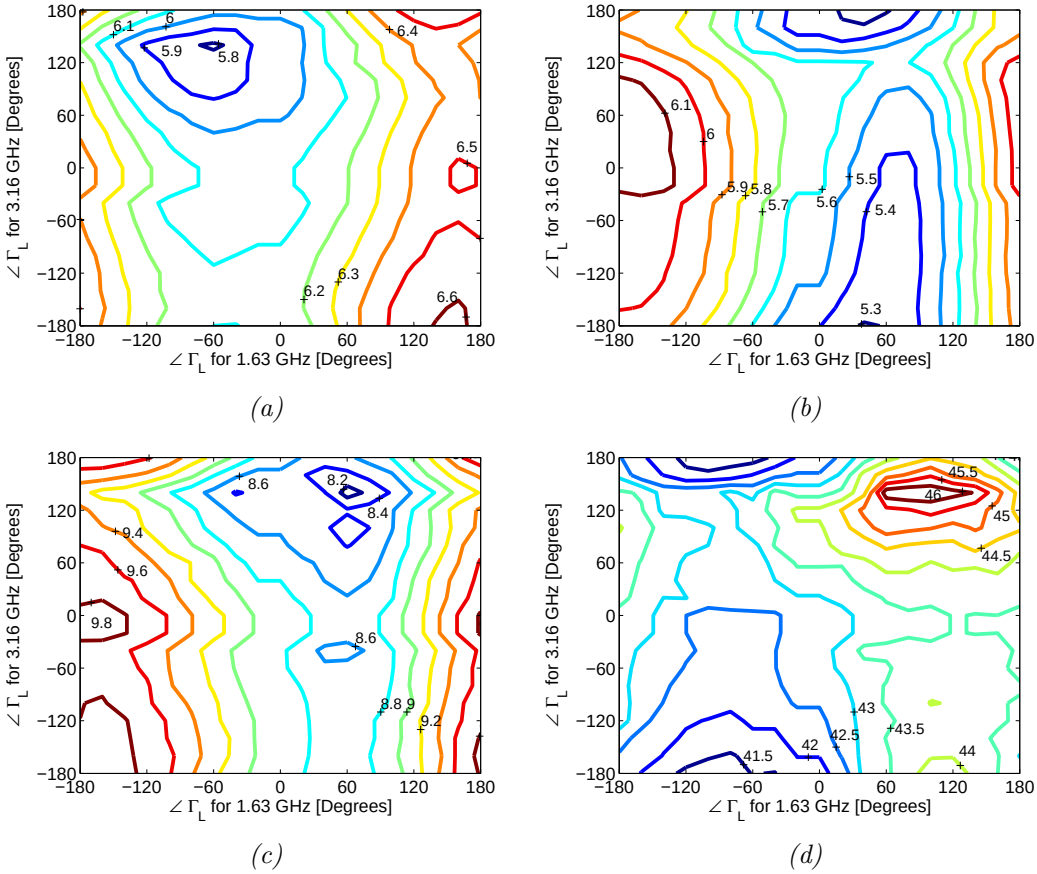


Figure 4.18: Intermodulation load-pull measurements. (a), gain variation at 2.14 GHz, (b), gain variation at 2.65 GHz, (c), DC consumption, (d), total efficiency.

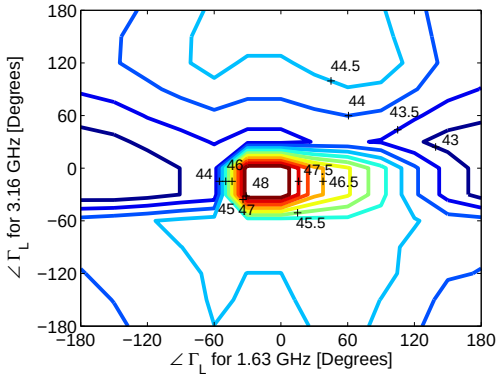
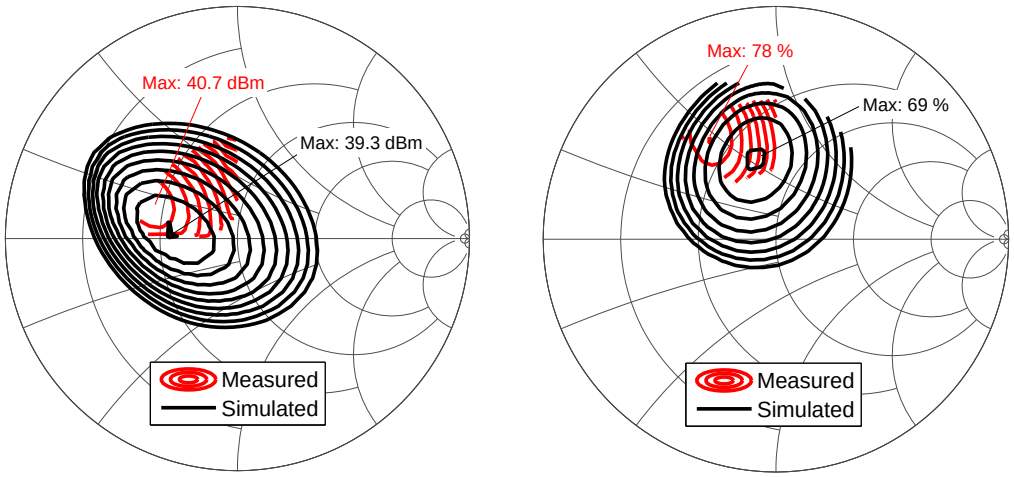
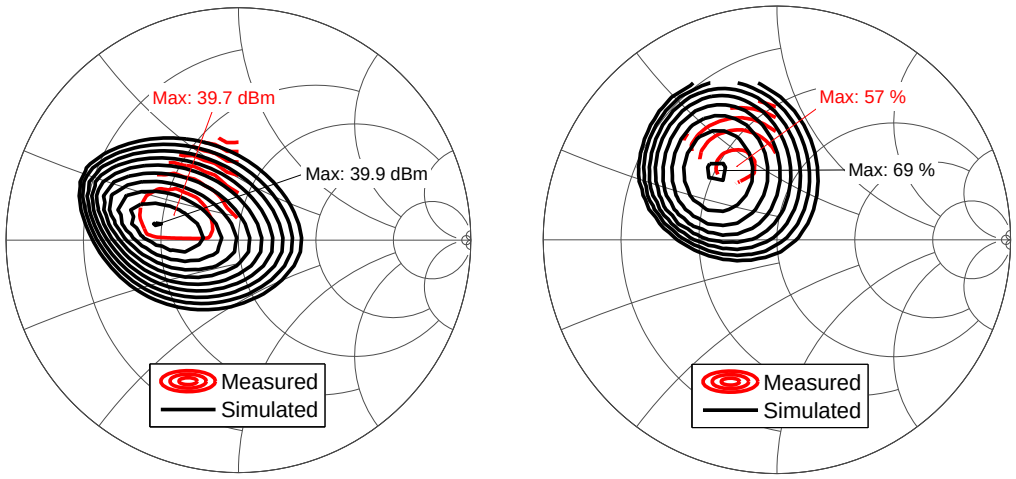


Figure 4.19: Intermodulation load-pull measurement suffering from memory effects in the device, showing total efficiency.



(a) (b)

Figure 4.20: Simulated load-pull versus measured load-pull at 2.14 GHz. (a), delivered power load-pull contours, (b), total efficiency. The contour lines have a step size of 0.5 dBm and 2% respectively.



(a) (b)

Figure 4.21: Simulated load-pull versus measured load-pull at 2.65 GHz. (a), delivered power load-pull contours, (b), total efficiency. The contour lines have a step size of 0.5 dBm and 2% respectively.

Chapter 5

Power amplifier design

This chapter will start out by discussing some common power amplifier topologies. The design process of the power amplifiers will be shown, covering stability network design, input matching network design, output matching network design and biasing of the amplifier. Two amplifiers have been designed in order to compare how proper intermodulation termination affects the efficiency.

5.1 Power amplifier topologies

Power amplifiers are in general classified in two categories; transconductance amplifiers, where the transistor operates as a current source, and switch mode power amplifiers, where the transistor operates as a switch. Transconductance amplifiers are divided into classes, depending on the quiescent current and conduction angle. Class A, AB, B and C amplifiers are all regarded as transconductance amplifiers. Switch mode power amplifiers are also divided into classes, but rather depending on operating conditions and harmonic termination requirements, including Class D, E, etc. In this thesis only transconductance amplifiers have been studied.

5.1.1 Transconductance amplifiers

Transistors operated as voltage controlled current sources are usually regarded as transconductance amplifiers. A configuration of such an amplifier is shown in Figure 5.1a, which incorporates a DC-block capacitor, inductor for blocking RF leaking into the voltage source and a bandpass filter short circuiting harmonics. Since the harmonics are short circuited, the voltage over the load is sinusoidal.

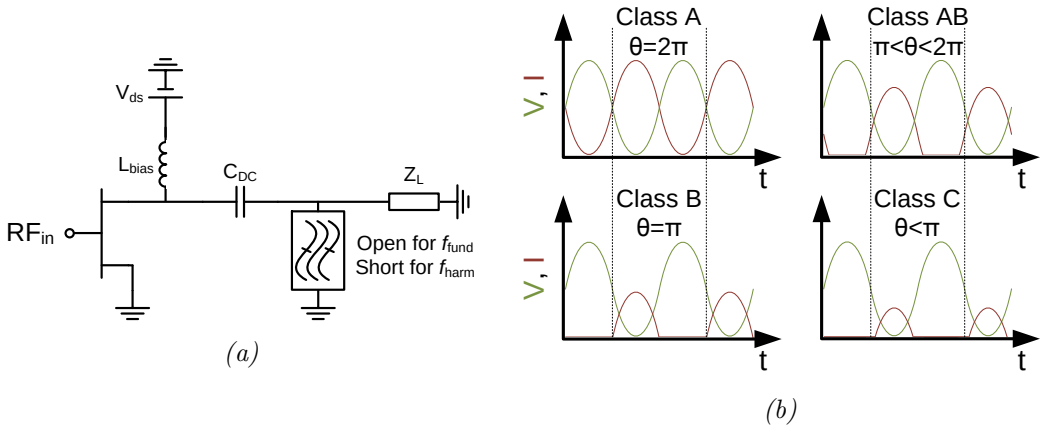


Figure 5.1: Transconductance amplifier. (a), schematic of a typical transconductance amplifier, (b), voltage and current waveforms for Class A, AB, B and C.

The classification of transconductance amplifiers depends on the conduction angle, i.e. the fraction of a wave period the device is conducting current. Depending on the bias voltages, the transistor will conduct differently and thus determining the amplifier class. The most linear mode of operation is called Class A where the device is constantly conducting. There is however a major drawback with a device that conducts 100% of the time, namely lower efficiency. Without any input signal the device still draws current and the maximum theoretical efficiency is 50%. The efficiency can be increased by moving to Class AB operation, where the conduction angle is between half a period and a full period. Increased efficiency comes with a price, the current waveform is clipped at the bottom, generating distortion. At Class AB operation, the quiscent current is usually 10-20% of the maximum current. Reducing the conduction angle further forces the transistor to a pinch-off bias and the conduction angle becomes half a period, known as Class B operation. The theoretical maximum efficiency for a Class B amplifier is $\pi/4$. Up to 100% efficiency can be achieved with Class C operation, where the conduction angle is less than half a period. However, for transconductance amplifiers, increasing the efficiency to 100% would also imply that the conduction angle approaches zero and thus no voltage swing over the load would be possible.

5.2 Design of the power amplifiers

Two amplifiers have been designed in this thesis, incorporating the results from the load-pull measurements in Chapter 4. The design process starts out with the stability network, moving on with input matching network design and harmonic termination, ending with output matching network design and layout. A 0.508 mm thick substrate (Rogers 4350) with 35 µm copper cladding was used in the design and manufacturing, datasheet appended in Appendix D.

5.2.1 Stability network

Determining the stability of an active device is usually done with the K and Δ-values. A device is unconditionally stable when the K-value is above one and the Δ-value is below one. They are calculated from the S-parameters of the device as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{5.1}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{5.2}$$

The transistor was unconditionally stable between 4 and 8 GHz. Outside this band the K factor of the transistor was below one, and a stabilization network was needed. The K- and Δ-values versus frequency are shown in Figure 5.2.

Stabilization of the transistor is possible using only resistive components, but that requires high series resistance or low parallel resistance, which would attenuate the input signal severely. Using reactive components can reduce the losses for higher frequencies and thus achieving unconditional stability without degredation of the gain in the frequency band of interest. The chosen topology is illustrated in Figure 5.3.

At low frequencies the capacitor will be an open circuit and the incoming signal will only see the resistor R_2 in series. The inductor will act as a short circuit and only R_1 will be seen in the parallel branch. At higher frequencies the capacitor will act more and more as a short circuit and the inductor will act as an open circuit. The net result is that the K factor will increase at lower frequencies and slightly less at higher frequencies, and hence unconditional stability and low losses can be achieved.

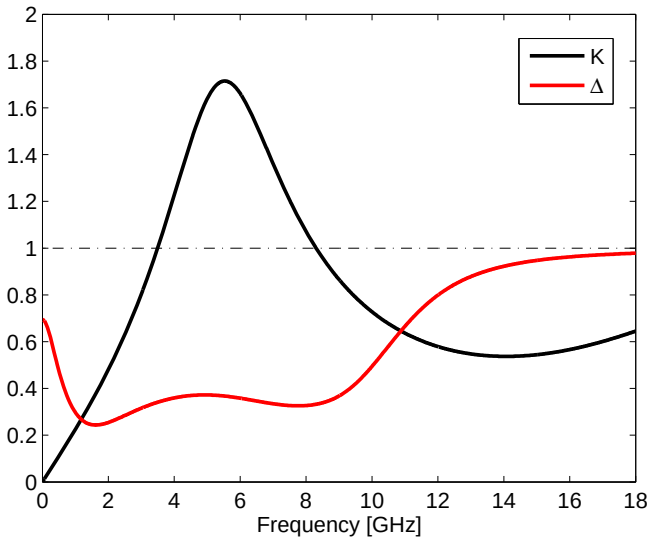


Figure 5.2: K factor and Δ versus frequency. Unconditionally stable between 4 and 8 GHz.

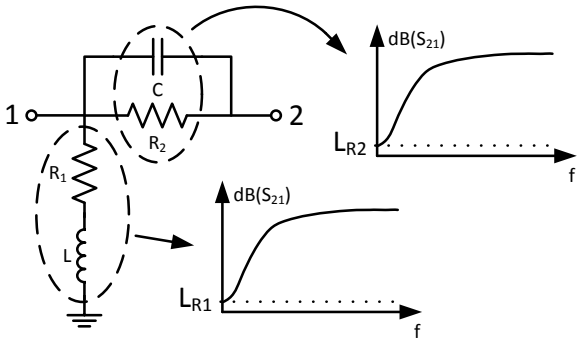


Figure 5.3: Topology of the stability network, two high pass filters.

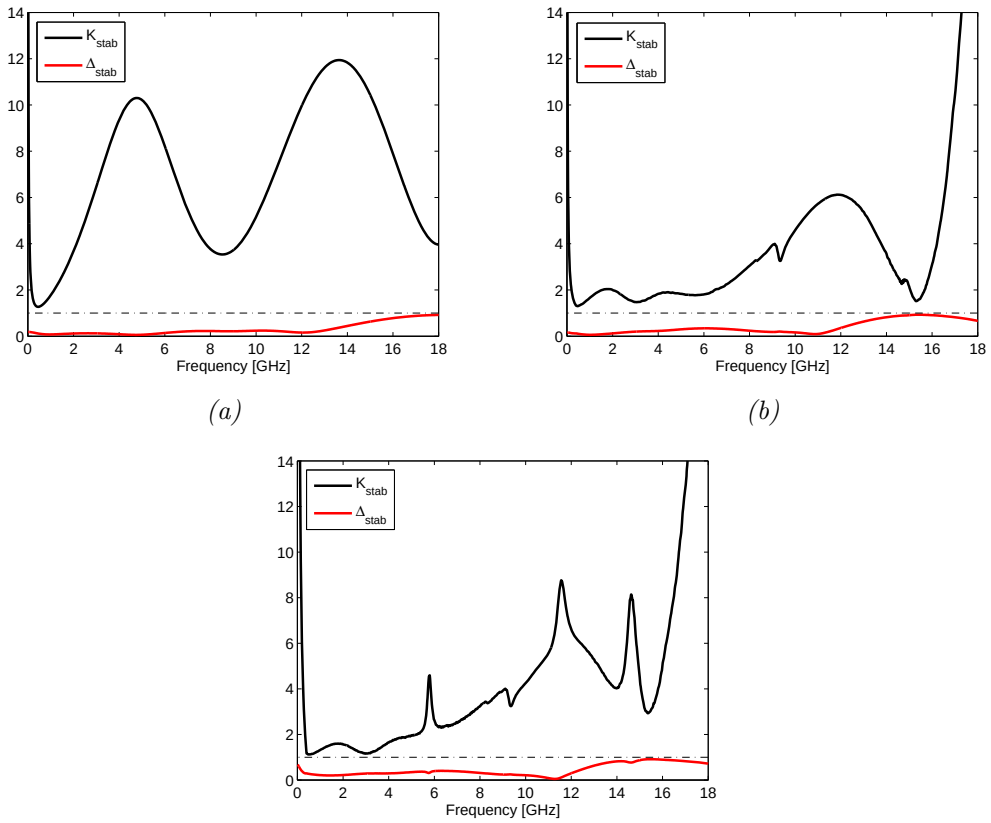


Figure 5.4: K factor and Δ versus frequency for various stability networks. (a), using a series and parallel resistor, (b), using a series and parallel resistor in combination with non-ideal reactive components, (c), using a series and parallel resistor with non-ideal reactive components together with a non-ideal DC-block.

A K factor below 1.6 over the desired frequency band was achieved with the following component values; $R_1 = 100\ \Omega$, $R_2 = 12\ \Omega$, $L = 6.8$ nH and $C = 3.9$ pF. The simulated K and Δ versus frequency are shown in Figure 5.4. The DC block capacitor also plays a role in the stability network, as seen from Figure 5.4c. The K-factor is relatively close to unity at the frequencies of interest; 1.52 at 2.14 GHz and 1.25 at 2.65 GHz.

5.2.2 Input matching network

A good input matching network is necessary to obtain a high power gain of the amplifier. Source-pull is a method to determine what source reflection coefficients are optimal for e.g. high power gain. Using a load-pull system where all of the travelling waves are measured has replaced the need of performing source-pull [27]. From load-pull measurements the travelling waves a_1 and b_1 can be used to calculate Γ_{in}. It is usually enough to conjugate match the input of the transistor.

The input reflection coefficient of the amplifier when performing load-pull measurements was measured to $\Gamma_{in} = 0.87\angle{-154.8°}$ at 2.14 GHz and $\Gamma_{in} = 0.86\angle{-161.4°}$ at 2.65 GHz. The input reflection coefficient of the transistor varied very little between the dual-band output matching condition and the concurrent dual-band output matching condition. The input matching network was therefore designed to be the same in both amplifiers.

Since the stability network contains lossy components, the input reflection coefficient of the transistor had to be transferred to the left side of the stability network, as illustrated

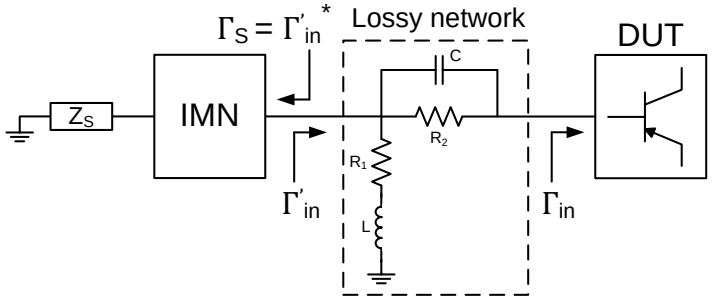


Figure 5.5: Conjugate matching with a lossy network in between.

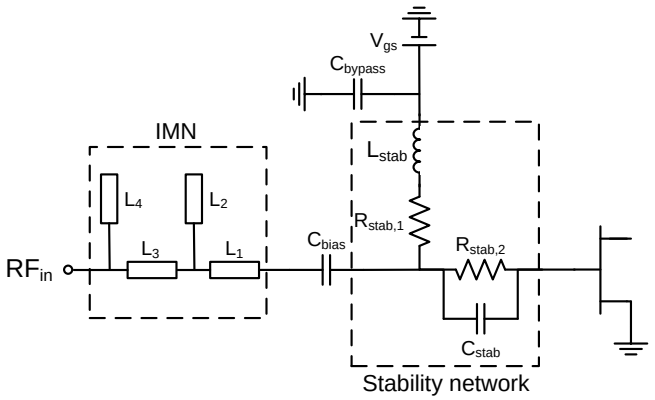


Figure 5.6: Input matching network with stability network.

in Figure 5.5. Having a lossy network in between the transistor and the input matching network voids the conjugate match theorem. Transferring the reflection coefficient to before the stability network results in $\Gamma_{in} = 0.70\angle{-178.6}^\circ$ at 2.14 GHz and $\Gamma_{in} = 0.77\angle{151.9}^\circ$ at 2.65 GHz. The source reflection coefficient needed to match the transistor is then calculated as the conjugate match of Γ'_{in}. Having obtained the source matching condition, the design of the input matching network could proceed.

The topology of the input matching network was a double stub tuner, as shown in Figure 5.6. The lengths of the transmission lines for the input matching network are summarized in Table 5.1.

5.2.3 Harmonic filtering

Designing two different amplifiers with different matching networks poses a risk when comparing the results. The optimal harmonic termination has not been measured and accounted for in this thesis and with different matching networks, the harmonic termination will vary between the two amplifiers. This was solved by placing a low-pass filter at the output of the device, filtering away the harmonics. The harmonic termination will therefore be equal and set by the filter. A fifth order low-pass network consisting of three inductors and two capacitors was chosen.

To bypass the problem with component variations, the lumped filter was converted into

Table 5.1: Transmission line lengths of the input matching network.

	L_1	L_2	L_3	L_4
Length, sim. (mm)	0.50	15.15	4.95	14.07
Length, EM sim. (mm)	0.40	14.93	4.85	13.72

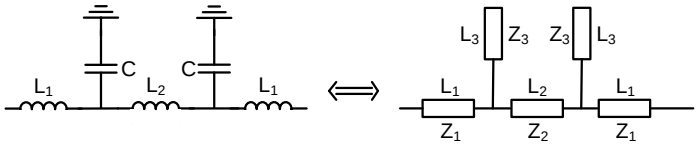


Figure 5.7: Fifth order low pass filter and the transmission line equivalent.

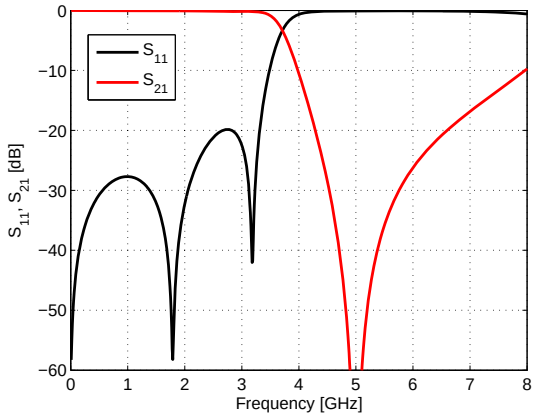


Figure 5.8: The S-parameters of the harmonic filter.

a distributed solution, as shown in Figure 5.7. The component values for the low-pass filter were simulated to be $L_1 = 1$ nH, $L_2 = 3.2$ nH and $C = 1$ pF. This would give a 3 dB cut-off frequency of 3.7 GHz. For the distributed solution, the transmission line impedances were $Z_1 = 110\ \Omega$, $Z_2 = 120\ \Omega$ and $Z_3 = 60\ \Omega$ and the transmission line lengths are summarized in Table 5.2.

The S-parameters of the harmonic filter are plotted in Figure 5.8. A loss higher than 10 dB over the frequency range 4 GHz to 8 GHz will be enough to ensure that the harmonic components are filtered away.

5.2.4 Output matching network

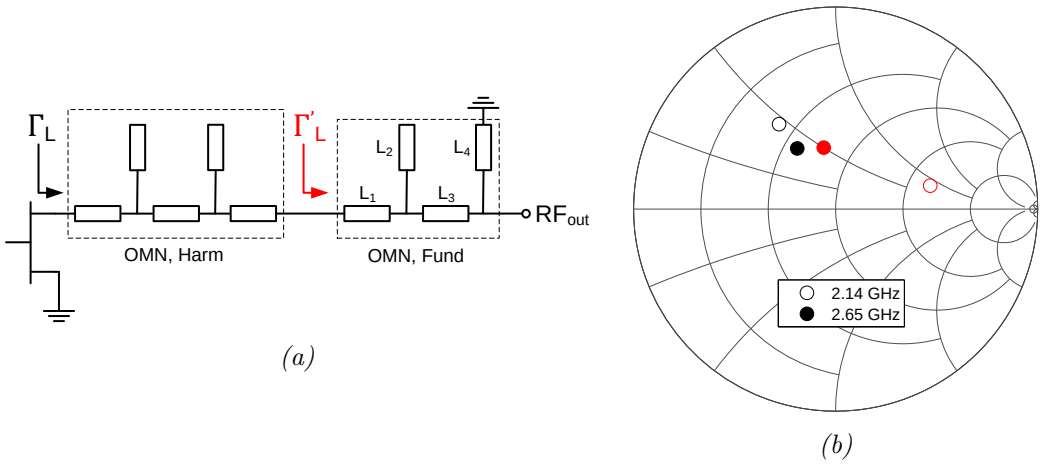
The output matching network of a power amplifier is usually the most crucial design step. Output power and efficiency are dependent on the output matching network, as seen in the load-pull measurements. The design of output matching networks requires a lot of time and consideration in order to utilize the full capacity of the device and thus maximizing the performance.

5.2.4.1 Dual-band power amplifier

For the dual-band power amplifier only two load reflection coefficients had to be designed for, located at $\Gamma_{L,2.14GHz} = 0.51\angle 124°$ and $\Gamma_{L,2.65GHz} = 0.36\angle 122°$. A double stub tuner was implemented as illustrated in Figure 5.9a. Because of the harmonic filter at the output of the transistor, the load reflection coefficients at 2.14 GHz and 2.65 GHz had to be rotated through the filter. This resulted in load reflection coefficients of $\Gamma'_{L,2.14GHz} = 0.49\angle 14°$ and

Table 5.2: Transmission line lengths of the harmonic filter.

	L_1	L_2	L_3
Length, sim. (mm)	2.515	4.844	9.553
Length, EM sim. (mm)	2.515	4.844	9.253



(a) (b)

Figure 5.9: Output matching network for the dual-band power amplifier. (a), topology, (b), rotation of load reflection coefficient through the harmonic filter, red indicating the load reflection coefficients after the harmonic filter.

Table 5.3: Transmission line lengths of the output matching network for the dual-band power amplifier.

	L_1	L_2	L_3	L_4
Length, sim. (mm)	10.52	30.46	34.98	24.83
Length, EM sim. (mm)	7.70	29.48	34.11	25.46

$\Gamma'_{L,2.65GHz} = 0.31\angle 101°$, as shown in Figure 5.9b. Designing the matching network for the two reflection coefficients was done by optimizing in ADS. The transmission line lengths of the output matching network are summarized in Table 5.3. The total loss of the output matching network was simulated to be 0.31 dB at 2.14 GHz and 0.35 dB at 2.65 GHz.

5.2.4.2 Concurrent dual-band power amplifier

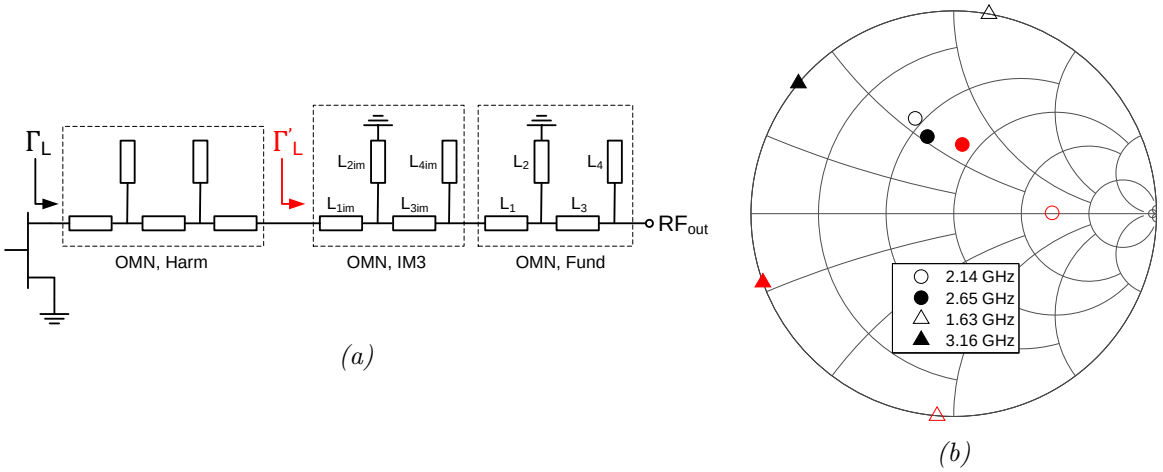
A similar design approach was used for the concurrent dual-band power amplifier (CDBPA), but instead four load reflection coefficients had to be designed for, located at $\Gamma_{L,1.63GHz} = 1\angle 80°$, $\Gamma_{L,2.14GHz} = 0.51\angle 112°$, $\Gamma_{L,2.65GHz} = 0.40\angle 109°$ and $\Gamma_{L,3.16GHz} = 1\angle 140°$. The impedance buffer methodology proposed in [28] was used for designing the matching network for the third order intermodulation products. A double stub tuner served as a matching network for the fundamental frequencies.

The CDBPA output matching network is illustrated in Figure 5.10a. Shifting the reference plane to after the harmonic filter gave the following load reflection coefficients; $\Gamma'_{L,1.63GHz} = 1\angle -95°$, $\Gamma'_{L,2.14GHz} = 0.49\angle 0°$, $\Gamma'_{L,2.65GHz} = 0.34\angle 83°$ and $\Gamma'_{L,3.16GHz} = 1\angle -160°$. The impedance buffer method synthesizes purely imaginary loads for a theoretical unlimited number of uncorrelated frequencies. It creates a short or open circuit at the desired frequency and uses a transmission line to rotate the short or open circuit to the desired imaginary load.

The transmission line lengths of the output matching network are summarized in Table 5.4. The impedance of all stub transmission lines were designed to be 70 Ω, which decreased the length slightly. The total loss of the output matching network was simulated to be 0.59 dB at 2.14 GHz and 1.07 dB at 2.65 GHz.

5.2.5 Layout

The gate of the transistor was biased through the stability network. This is a good solution since the stability network already contains a resistor and inductor in series with the DC



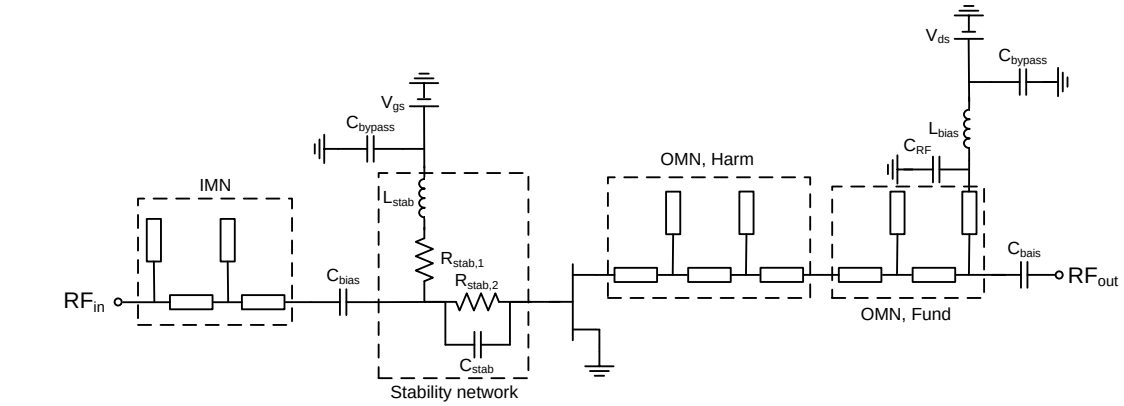
(a) *(b)*

Figure 5.10: Output matching network for the concurrent dual-band power amplifier. (a), topology, (b), rotation of load reflection coefficient through the harmonic filter, red indicating the load reflection coefficients after the harmonic filter.

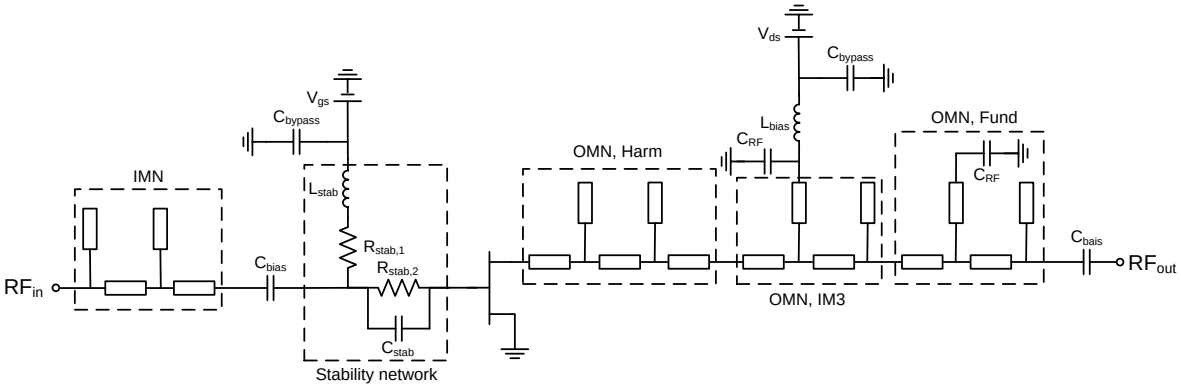
Table 5.4: Transmission line lengths of the output matching network for the concurrent dual-band power amplifier.

	L_{1im}	L_{2im}	L_{3im}	L_{4im}	L_1	L_2	L_3	L_4
Length, sim. (mm)	26.59	28.77	13.71	28.33	28.33	2.29	0.01	15.91
Length, EM sim. (mm)	25.51	27.25	12.75	27.50	28.48	2.11	0.30	15.15

supply, prohibiting high frequency components from leaking into the DC supply. A few bypass capacitors were needed to ensure proper RF ground after the inductor L_{stab}. For the dual-band power amplifier (DBPA), the drain was biased through the last stub, which saved some space in contrast to having a separate bias network. Bypass capacitors were used to ground the RF. For the CDBPA, the drain was biased through the first matching network stub. Bypass capacitors were used on this stub as well as capacitors to ground on the third matching network stub, to provide RF ground and to prevent the DC from short circuiting. The complete schematics for the DBPA and the CDBPA are shown in Figure 5.11a and Figure 5.11b, respectively.



(a)



(b)

Figure 5.11: Amplifier schematic layouts. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.

Chapter 6

Power amplifier measurements

The layout files in Appendix A-C were sent for fabrication and a one centimeter thick aluminum fixture was manufactured. The surface mount technology (SMT) components were soldered on the printed circuit boards (PCBs) and later assembled on the fixtures together with the transistor. The fully assembled dual-band power amplifier is shown in Figure 6.1a and the fully assembled concurrent dual-band power amplifier is shown in Figure 6.1b.

Four different types of measurements were performed; S-parameters, CW power sweep, CW frequency sweep and modulated measurements. The initial measurements looked relatively promising, and showed good performance at single band transmission. However, when driving the amplifiers with a two tone signal the results were not as expected. The difference frequency $2.65 - 2.14 = 0.51$ GHz, from now on referred to as IM2, was not properly terminated, especially not for the concurrent transmission mode power amplifier. An LC network to ground was inserted at the output of the transistor, with a resonance frequency located at 510 MHz, as seen in Figure 6.2.

This changed the output matching network slightly and thus two results are provided for each measurement, one for the PAs without the LC-network and one with the LC-network.

6.1 S-parameter measurements

The S-parameter measurements were performed with a calibrated VNA and compared with the simulated results in ADS. S_{11}, S_{21} and S_{22} for the DBPA is shown in Figure 6.3.

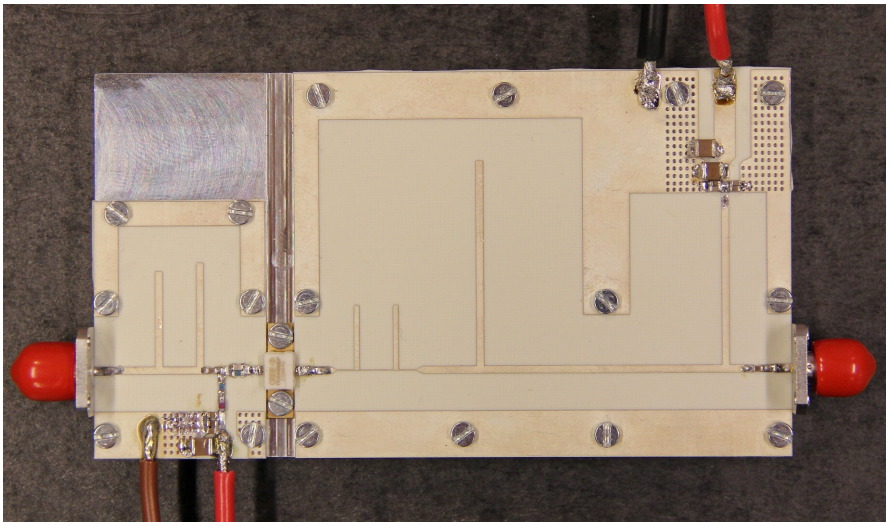
The measurements show a gain of roughly 10 dB at 2.14 GHz and 8.5 dB at 2.65 GHz without the LC-network, and roughly 11 dB at 2.14 GHz and 9 dB at 2.65 GHz with the LC-network. The output of the amplifier is matched, better than -10 dB at both frequencies and both types of the power amplifier. The input is not as well matched but still provides a return loss better than -8 dB at both frequencies and both amplifier types. In overall, the measurements and simulations are in good agreement.

The S-parameters for the CDBPA is shown in Figure 6.4. With a slightly more complicated output matching network, the small signal parameters have a more complex behaviour. A good matching is achieved at the two operating frequencies, similar to the DBPA. The gain at 2.65 GHz is somewhat lower. Again, simulations and measurements are in good agreement.

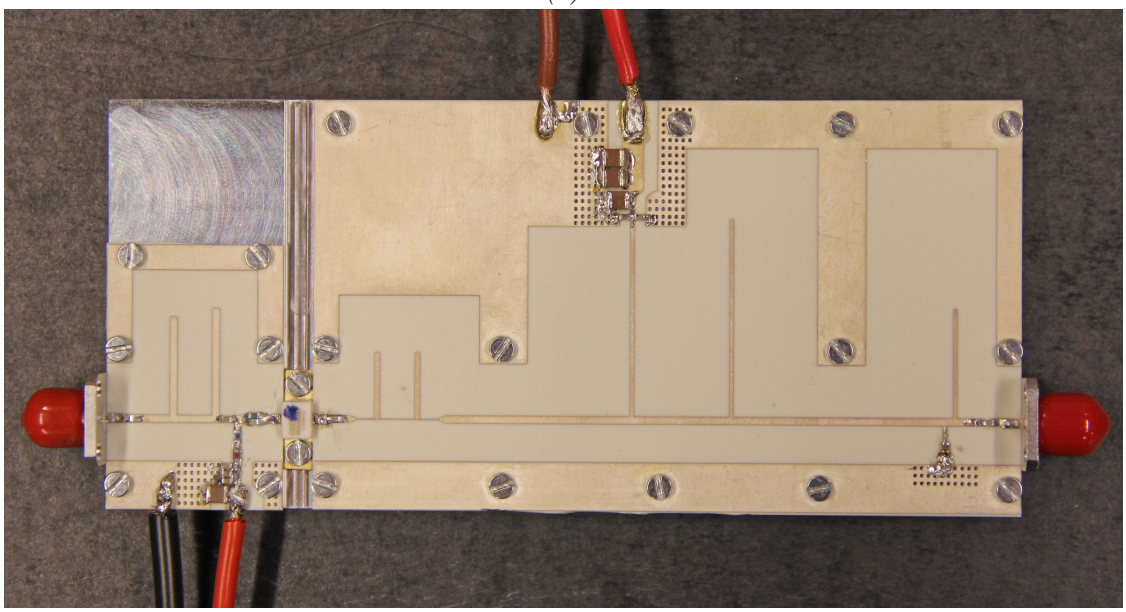
6.2 CW measurements

Power sweep CW measurements were performed with the multi-band measurement system introduced in Chapter 3 and frequency dependent CW measurements were performed with an Anritsu 69087B signal generator together with two power meters and a directional coupler.

First, the power amplifiers without the LC-network were measured. The input power was swept from -10 dBm to 30 dBm at 2.14 GHz and from -10 dBm to 32 dBm at 2.65 GHz, plotted in Figure 6.5. Because of the slightly different matching condition of the CDBPA and



(a)



(b)

Figure 6.1: Assembled amplifiers. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.

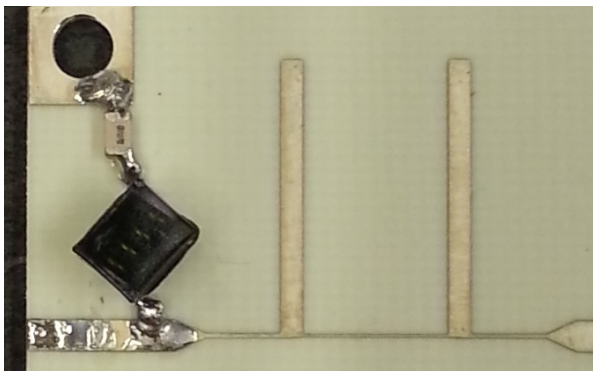
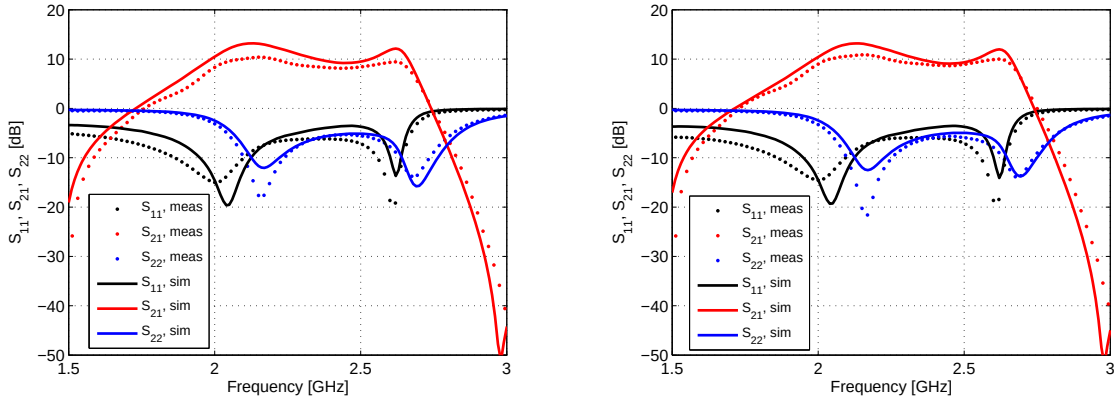
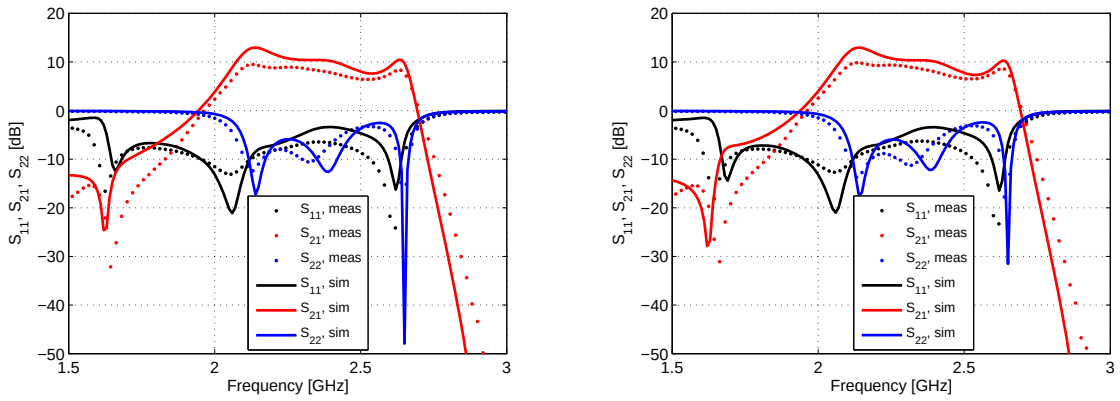


Figure 6.2: IM2 short circuit termination with an LC-network on the output of the transistor.



(a) (b)

Figure 6.3: S-parameters simulations for the dual-band power amplifier. (a), dual-band power amplifier, (b), dual-band power amplifier with IM2 termination.



(a) (b)

Figure 6.4: S-parameters simulations for the concurrent dual-band power amplifier. (a), concurrent dual-band power amplifier, (b), concurrent dual-band power amplifier with IM2 termination.

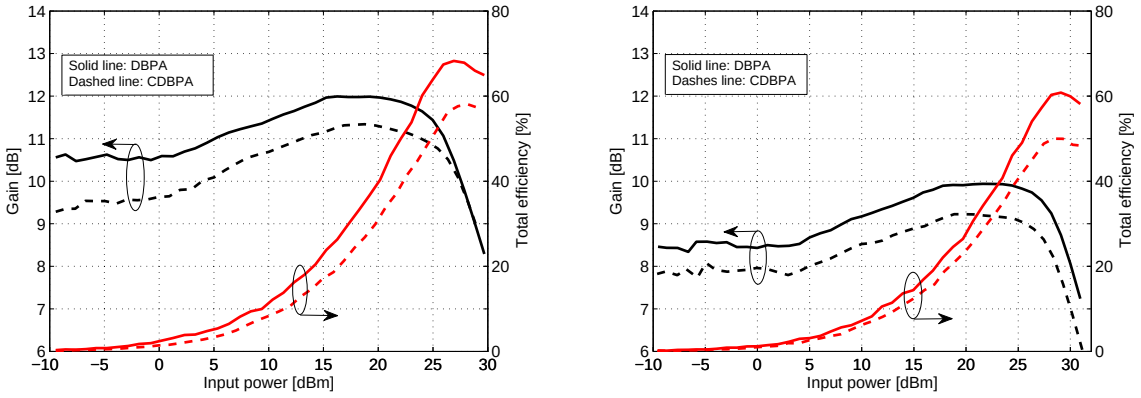


Figure 6.5: Power sweep of the two amplifiers operating in single transmission mode. (a), 2.14 GHz, (b), 2.65 GHz.

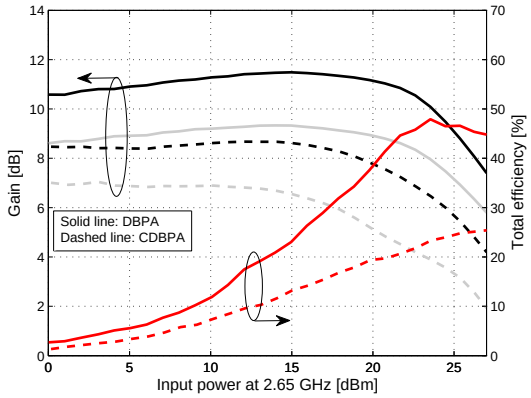


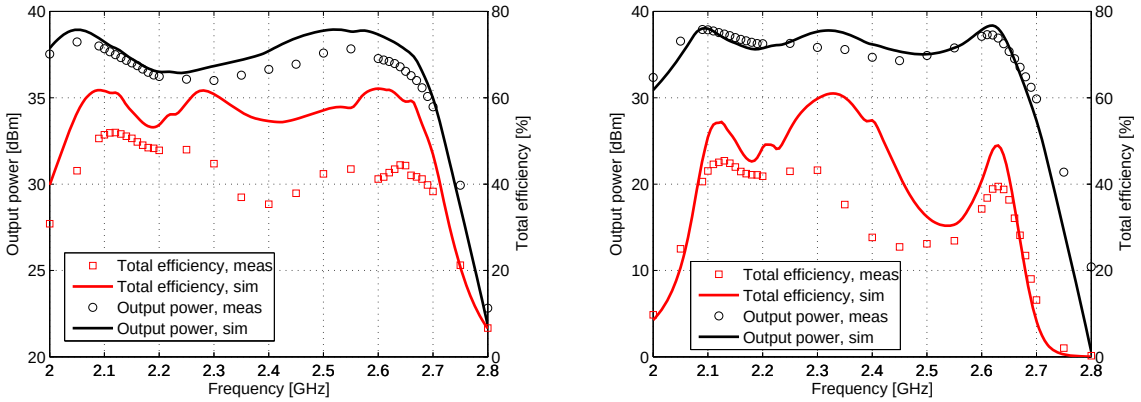
Figure 6.6: Power sweep of the two amplifiers operating in concurrent transmission mode. Black lines are for 2.14 GHz and grey lines are for 2.65 GHz.

slightly higher losses due to a physically longer matching network, the gain was lower at both frequencies giving a lower total efficiency. The efficiency is relatively high taken into account that the harmonics have just been filtered out.

The amplifiers were operated in concurrent transmission mode, where the power at 2.14 GHz was swept from -2 dBm to 26 dBm and the power at 2.65 GHz was swept from 0 dBm to 28 dBm. The result is shown in Figure 6.6. Here the effect of having a bad termination at 510 MHz is seen, the CDBPA saturates too early and has lower gain. The efficiency suffers also due to the earlier saturation.

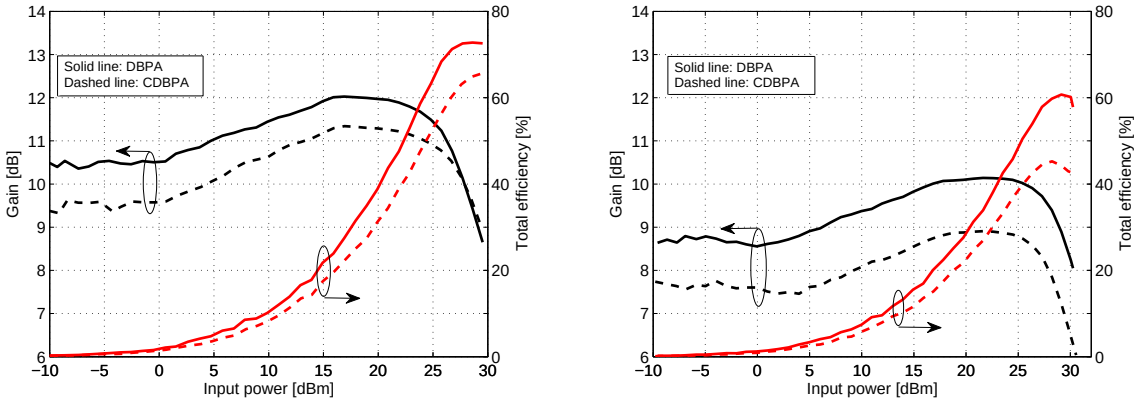
The frequency of the input signal was swept from 2 GHz to 2.8 GHz for both amplifiers and the result is shown in Figure 6.7. The DBPA generated approximately 37.2 dBm with an efficiency of 51% at 2.14 GHz and 36.5 dBm with a efficiency of 44% at 2.65 GHz. The CDBPA generated an output power of 37.2 dBm with 45% efficiency at 2.14 GHz and 35.4 dBm with 36% efficiency at 2.65 GHz. In general, the simulations show a higher output power over the full frequency sweep resulting in a higher efficiency. Besides from the deviation between simulated and measured results, the amplifiers are centered at the design frequencies.

Incorporating the LC-network and measuring the CW input power sweep gives the results shown in Figure 6.8. The gain is similar to results obtained before, a slight increase in efficiency at 2.14 GHz for both amplifiers and a slight decrease in gain and efficiency for the



(a) (b)

Figure 6.7: Frequency sweep and a constant input power of 30 dBm. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.



(a) (b)

Figure 6.8: Power sweep of the the revised amplifiers operating in single transmission mode. (a), 2.14 GHz, (b), 2.65 GHz.

CDBPA at 2.65 GHz.

The output power and efficiency versus input power at concurrent transmission are shown in Figure 6.9. Compared to Figure 6.6, a large increase in gain and efficiency is noted for the CDBPA. The increase in efficiency is about 20 percentage points at saturation. Also an increase in efficiency is noted for the DBPA. This indicates the importance of taking into account the intermodulation product at 510 MHz.

The frequency was swept from 2 GHz to 2.8 GHz and the input power was set to 30 dBm, obtaining the results shown in Figure 6.10. The revised DBPA generated approximately 37.3 dBm with an efficiency of 56% at 2.14 GHz and 36.9 dBm with a efficiency of 45% at 2.65 GHz. For the CDBPA an output power of 37.6 dBm with 51% efficiency at 2.14 GHz and 34.9 dBm with 32% efficiency at 2.65 GHz was obtained.

6.3 Modulated measurements

Modulated measurements were performed with an Agilent E4438C ESG Vector Signal Generator and an Agilent N9030A PXA Signal Analyzer together with a driver amplifier, power meter and a directional coupler. A 5 MHz orthogonal frequency-division multiplexing (OFDM)

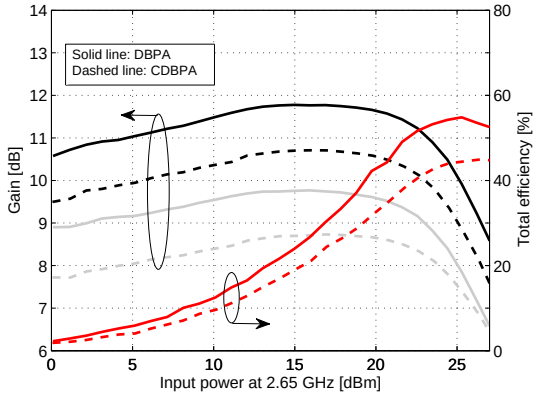
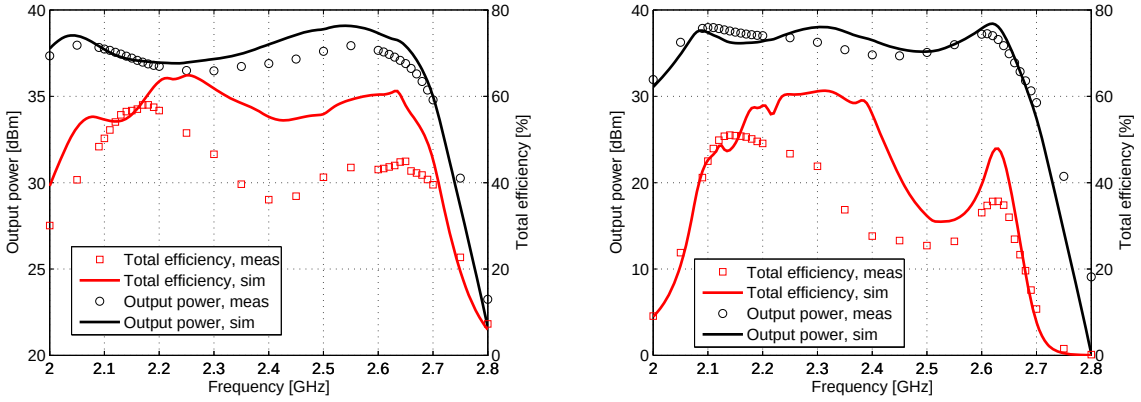


Figure 6.9: Power sweep of the revised amplifiers operating in concurrent transmission mode. Black lines are 2.14 GHz and grey lines are 2.65 GHz.



(a) *(b)*

Figure 6.10: Frequency sweep and a constant input power of 30 dBm for the revised amplifiers. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.

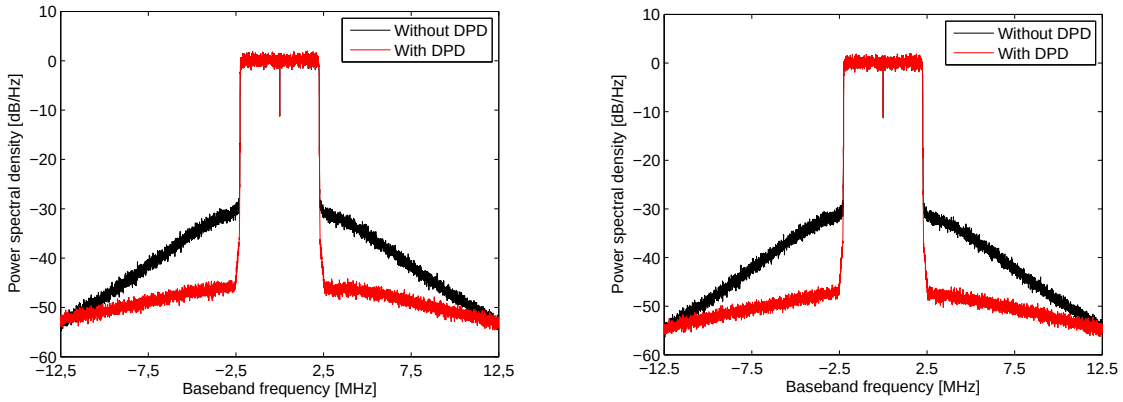


Figure 6.11: Output signal spectrum of a 5 MHz OFDM signal centered at 2.14 GHz. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.

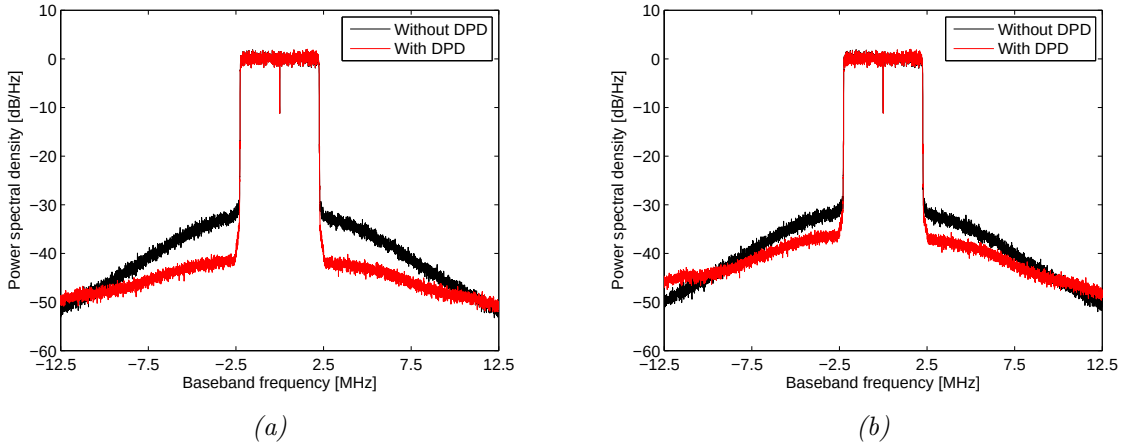


Figure 6.12: Output signal spectrum of a 5 MHz OFDM signal centered at 2.65 GHz. (a), dual-band power amplifier, (b), concurrent dual-band power amplifier.

signal with a crest factor of 8.4 dB was generated by the ESG, and the RMS input power was set to 16 dBm at 2.14 GHz and 18.6 dBm at 2.65 GHz. The amplifiers were linearized with a generalized memory polynomial (GMP) digital pre-distorter (DPD) [29].

Figure 6.11 shows the output power density spectrum of the amplifiers at 2.14 GHz. Without linearization the spectrum is heavily distorted, having adjacent channel leakage ratio (ACLR) of -34.2 dBc and -34.7 dBc for the DBPA and CDBPA, respectively. The DPD is successful in linearizing both amplifiers at 2.14 GHz, achieving ACLR values of -46.3 dBc and -47.4 dBc respectively.

Output spectrum before and after linearization at 2.65 GHz is shown in Figure 6.12. Linearization at 2.65 GHz is generally harder for the DPD mainly because of the fact that the amplifiers are slightly harder driven. The DBPA is fairly well linearized but the CDBPA suffers from spectral regrowth even after linearization. The ACLR before linearization is -35 dBc and -34.4 dBc for the DBPA and CDBPA respectively, compared to -43.2 dBc and -37.4 dBc after linearization. In overall the results for the amplifiers are quite satisfying, proving that they are linearizable. Table 6.1 summarizes the output power, efficiency and achieved ACLR values.

A series of measurements were also carried out on the amplifiers with the LC-network

Table 6.1: Average P_{out}, average efficiency and ACLR for the amplifiers without the LC-network.

	P_{out} (dBm)		η_{tot} (%)		ACLR (dBc)	
	w/o DPD	w DPD	w/o DPD	w DPD	w/o DPD	w DPD
DBPA @ 2.14 GHz	27.7	27.7	26.5	26.0	-34.2	-46.3
CDBPA @ 2.14 GHz	27.2	27.2	21.4	21.0	-34.7	-47.4
DBPA @ 2.65 GHz	28.5	28.6	25.0	25.4	-35.1	-42.5
CDBPA @ 2.65 GHz	27.8	27.8	22.6	22.4	-34.1	-37.9

Table 6.2: Average P_{out}, average efficiency and ACLR for the amplifiers with the LC-network.

	P_{out} (dBm)		η_{tot} (%)		ACLR (dBc)	
	w/o DPD	w DPD	w/o DPD	w DPD	w/o DPD	w DPD
DBPA @ 2.14 GHz	27.8	27.8	27.0	26.3	-33.1	-45.2
CDBPA @ 2.14 GHz	27.3	27.3	21.7	21.4	-35	-48.4
DBPA @ 2.65 GHz	29	29	26.6	26.3	-35	-43.2
CDBPA @ 2.65 GHz	27.3	27.2	20.3	19.7	-34.4	-37.5

implemented. They do not differ much from the previous measurements and thus only a summary of the measured results is presented in Table 6.2.

Chapter 7

Discussion

The importance of proper intermodulation termination cannot be dismissed. As shown in the two tone device simulations in Chapter 4, the intermodulation tone power levels are high throughout the power sweep. This does not only draw power from the fundamental tones, it might also affect the voltage and current swing of the device. It is also shown, in the same chapter, that proper third order intermodulation (IM3) termination improves performance. However, it is important to remember that the benefits of proper IM3 termination is marginal. When designing and fabricating a circuit, the extra losses due to additional matching network might overrule the marginal improvement, and actually result in degraded performance. This is the case in Chapter 6 of this thesis, where two amplifiers with two different matching networks were manufactured. Another contributing factor to the difference between the two amplifiers was that an LC-network was introduced, altering the output matching networks. Simulations in ADS show that the output matching network for the concurrent dual-band power amplifier was affected more than the output matching network for the other amplifier, leading to a degradation in performance for the CDBPA. With a proper termination at the difference frequency, $f_2 - f_1$, the results would have been more comparable between the two amplifiers.

In general, the power amplifier design strategy was successful. Simulated and measured performance agree well for both amplifiers which indicates that the step from simulation to fabrication was accurate. A lot of time was spent on EM simulations, adjusting the transmission lines properly, which explains the good agreement. The circuits were not really affected by component variations and no stability issues were encountered.

The measurements performed in this thesis are slightly more complicated than regular one tone load-pull measurements but still at a manageable level. It would be interesting to perform load-pull measurements including more tones, thus giving a more complete understanding. One could then determine which tones are the most important ones. However, the multi-band load-pull system has restrictions on maximum frequency, and is a limitation of this work.

Chapter 8

Conclusions and future work

8.1 Conclusions

This thesis has analyzed a transistor in large signal operation, conducting one tone load-pull measurements as well as two tone load-pull measurements using an active multi-band load-pull system. Furthermore, two power amplifiers based on two different load-pull measurements have been designed, fabricated and evaluated.

It was shown that exciting a device with a two-tone signal gave a different optimal load termination, compared to exciting the two tones separately. Hence, the design of a transmitter aimed for multi-band operation requires a multi-band simulation and/or measurement. When investigating the effect of proper third order intermodulation product termination, it was found that the efficiency and linearity could be increased.

Two power amplifiers were successfully designed, fabricated and evaluated. The load reflection coefficients for the matching networks were based on the load-pull measurements. The dual-band power amplifier and the concurrent dual-band power amplifier had peak efficiencies of 54% and 45% at concurrent transmission, respectively. It was also proven that linearization is possible with standard DPD models, achieving average efficiencies of approximately 26% for the dual-band power amplifier and approximately 20% for the concurrent dual-band power amplifier.

8.2 Future work

With only touching lightly on the topic of multi-band load-pull measurements there is a lot of future work to be done. A couple of ideas are suggested:

- The measurement methods for multi-band load-pull have to be refined, in particular what kind of signals to be used. Two tone signals might not be the best input signal because of the large variation in signal power. They are however simple to use and the intermodulation products are limited. A tradeoff between signal complexity and signal relevance has to be made.
- A more thorough investigation of how proper load termination at the intermodulation products affects the device performance has to be done. As experienced in the thesis, it is not only the third order intermodulation product that is important.
- Memory effects in GaN devices are present, affecting and limiting the measurements to some extent. A characterization of the memory effect time constants would help when choosing measurement parameters.

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A Appendix 1

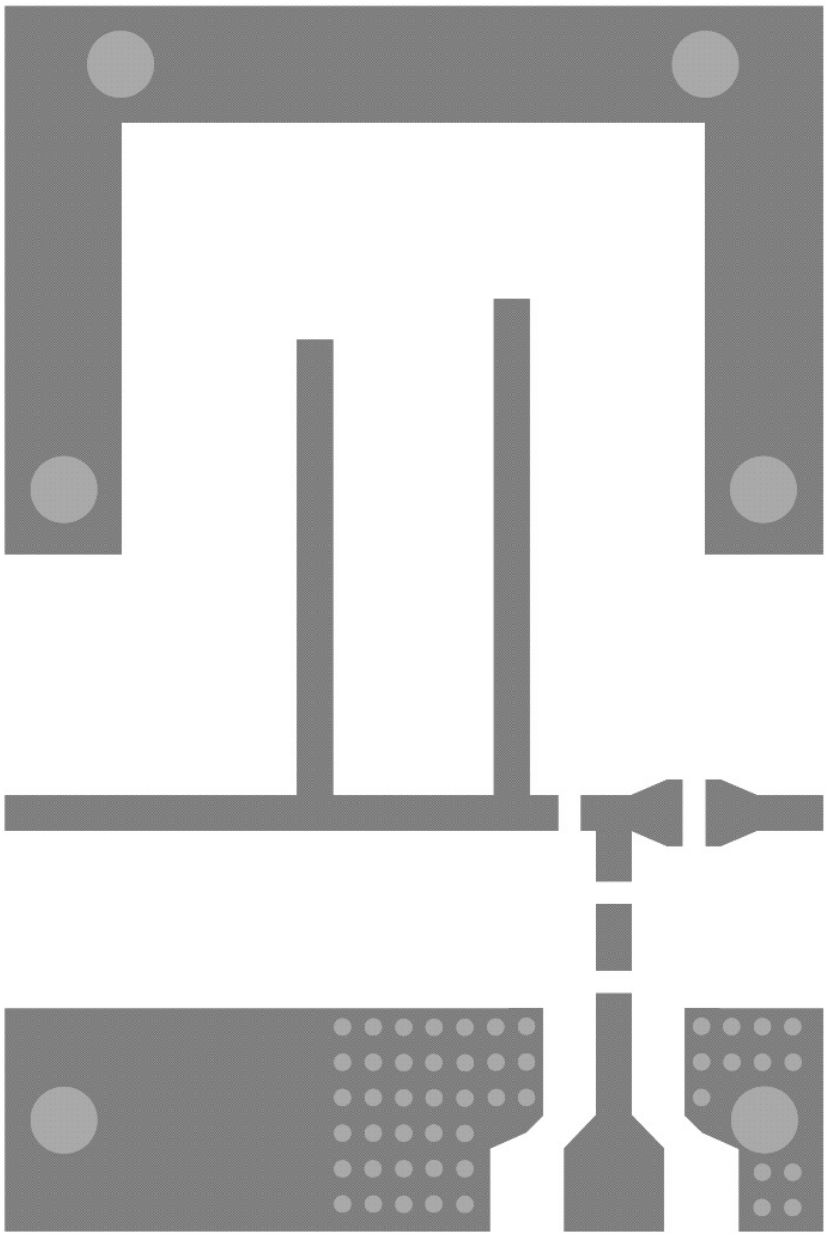

Figure A.1: Layout of the input matching network.

B Appendix 2

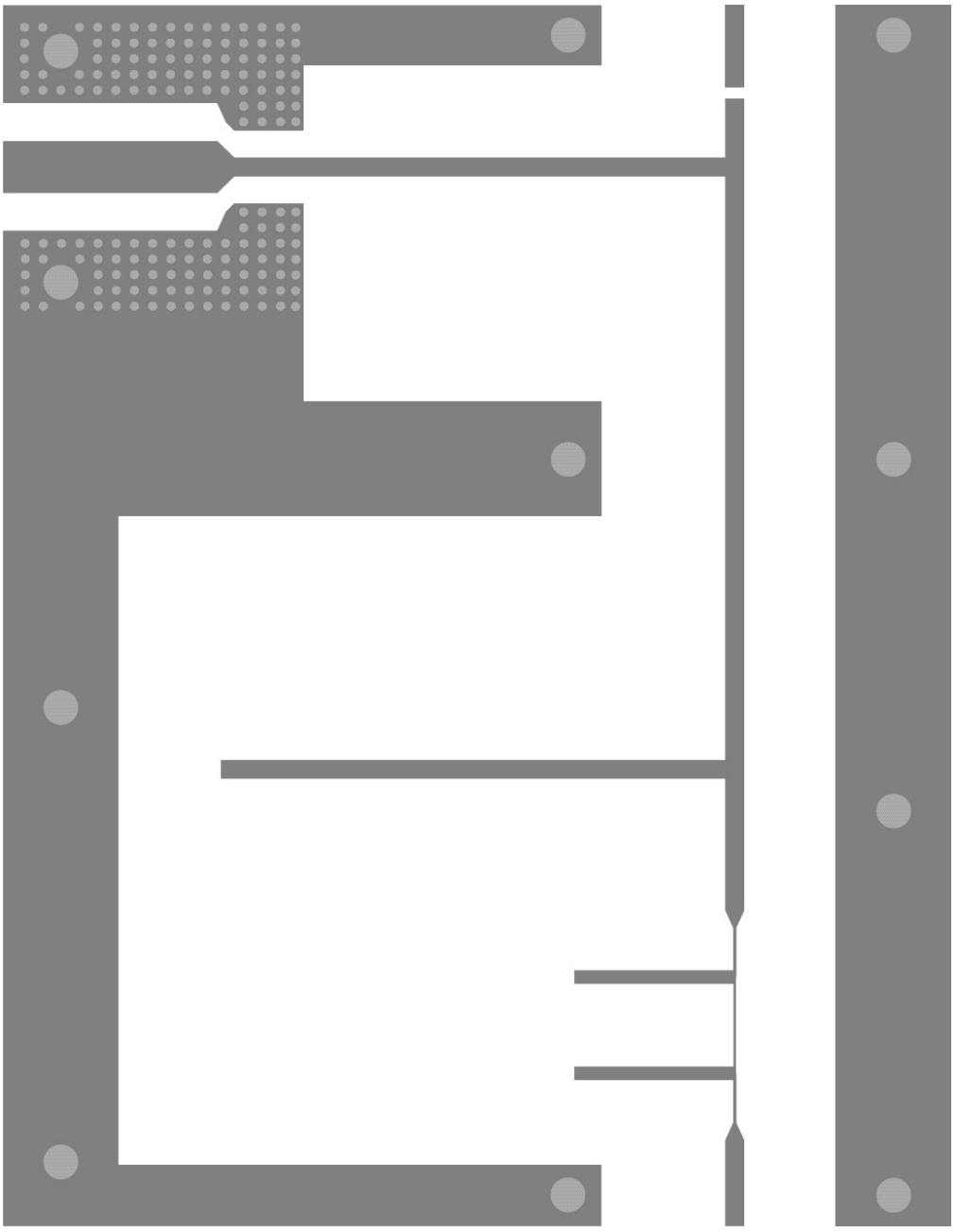

Figure B.1: Layout of the output matching network for the dual band power amplifier.

C Appendix 3

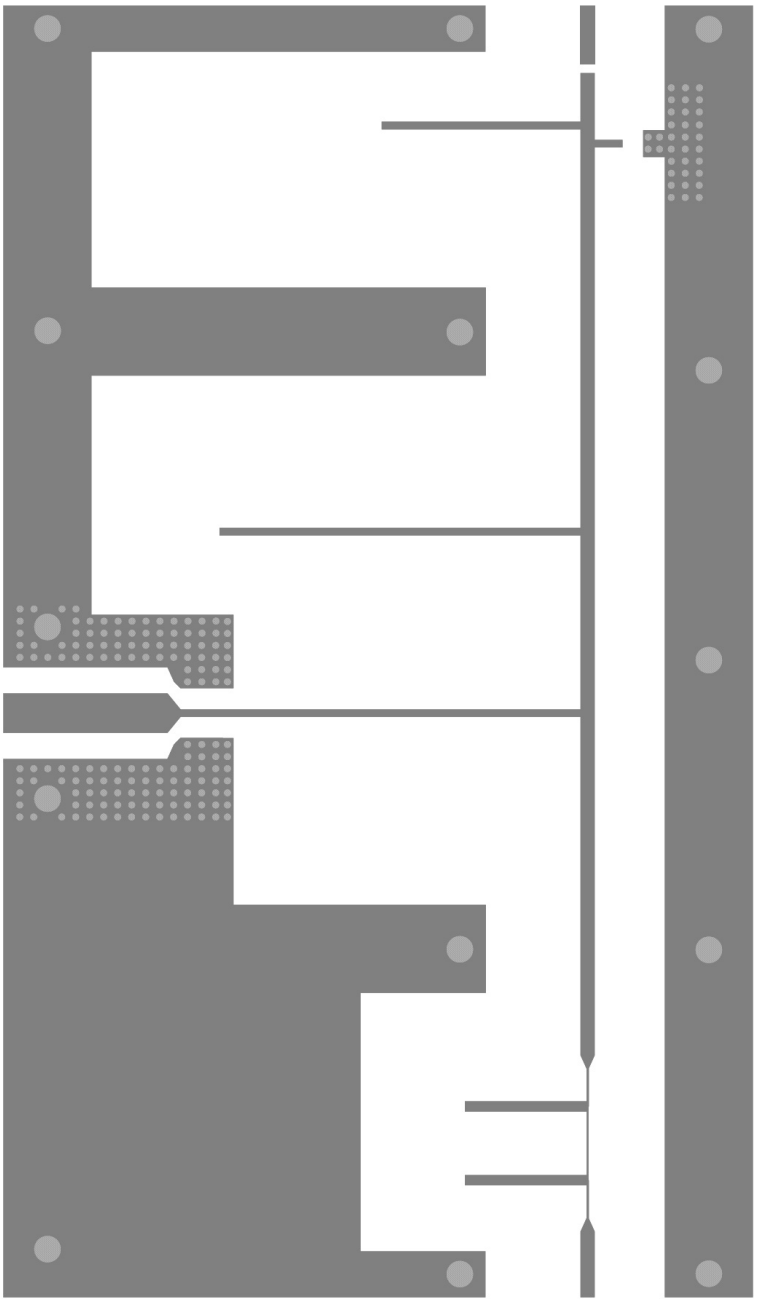

Figure C.1: Layout of the output matching network for the concurrent dual band power amplifier.

D Appendix 4

Rogers 4000 Series High frequency circuit materials

Rogers Corporation

ROGERS CORPORATION

Data Sheet

Property	Typical Value		Direction	Units	Condition	Test Method
	RO4003C	RO4350B				
Dielectric Constant, ε_r Process	3.38 ± 0.05	3.48 ± 0.05	Z	--	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
(1) Dielectric Constant, ε_r Design	3.55	3.66	Z	--	8 to 40 GHz	Differential Phase Length Method
Dissipation Factor tan, δ	0.0027 0.0021	0.0037 0.0031	Z	--	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	+40	+50	Z	ppm/°C	-50°C to 150°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7 X 10^{10}	1.2 X 10^{10}		MΩ•cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2 X 10^{9}	5.7 X 10^{9}		MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	19,650 (2,850) 19,450 (2,821)	16,767 (2,432) 14,153, (2,053)	X Y	MPa (ksi)	RT	ASTM D638
Tensile Strength	139 (20.2) 100 (14.5)	203 (29.5) 130 (18.9)	X Y	MPa (ksi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)		MPa (kpsi)		IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°C	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	14 16 35	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.4.41
Tg	>280	>280		°C DSC	A	IPC-TM-650 2.4.24
Td	425	390		°C TGA		ASTM D3850
Thermal Conductivity	0.71	0.69		W/m/°K	80°C	ASTM C518
Moisture Absorption	0.06	0.06		%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86		gm/cm^3	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)		N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	(2)V-0				UL 94
Lead-Free Process Compatible	Yes	Yes				

NOTES:
(1) The design Dk is an average number from several different tested lots of material and on the most common thickness/s. If more detailed information is required, please contact Rogers Corporation or refer to Rogers' technical papers in the Rogers Technology Support Hub available at http://www.rogerscorp.com/acm/technology.
(2) ** Note on 94V-0 ** RO4350B LoPro™ laminates do not share the same UL designation as standard RO4350B laminates. A separate UL qualification may be necessary.

Typical values are a representation of an average value for the population of the property. For specification values contact Rogers Corporation.

RO4000 LoPro laminate uses a modified version of the RO4000 resin system to bond reverse treated foil. Values shown above are RO4000 laminates without the addition of the LoPro resin. For double-sided boards, the LoPro foil results in a thickness increase of approximately 0.0007" (0.018µm) and the Dk is approximately 2.4. The Dk decreases by about 0.1 as the core thickness decreases from 0.020" to 0.004.

Prolonged exposure in an oxidative environment may cause changes to the dielectric properties of hydrocarbon based materials. The rate of change increases at higher temperatures and is highly dependent on the circuit design. Although Rogers' high frequency materials have been used successfully in innumerable applications and reports of oxidation resulting in performance problems are extremely rare, Rogers recommends that the customer evaluate each material and design combination to determine fitness for use over the entire life of the end product.

Advanced Circuit Materials Division
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ROGERS CORPORATION

Data Sheet

Standard Thickness	Standard Panel Size	Standard Copper Cladding
RO4003C: 0.008" (0.203mm), 0.012 (0.305mm), 0.016"(0.406mm), 0.020" (0.508mm) 0.032" (0.813mm), 0.060" (1.524mm) RO4350B: *0.004" (0.101mm), 0.0066" (0.168mm) 0.010" (0.254mm), 0.0133" (0.338mm), 0.0166" (0.422mm), 0.020"(0.508mm), 0.030" (0.762mm), 0.060"(1.524mm) Note: Material clad with LoPro foil add 0.0007" (0.018mm) to dielectric thickness	12" X 18" (305 X457 mm) 24" X 18" (610 X 457 mm) 24" X 36" (610 X 915 mm) 48" X 36" (1.224 m X 915 mm) *0. 004" (0.101mm) material in not available in panel sizes larger than 24"x18" (610 X 457mm)	½ oz. (17µm) electrodeposited copper foil (.5ED/.5ED) 1 oz. (35µm) electrodeposited copper foil (1ED/1ED) 2 oz. (70µm) electrodeposited copper foil (2ED/2ED) **PIM Sensitive Applications:** ½ oz (17µm) LoPro Reverse Treated EDC (.5TC/.5TC) 1 oz (35µm) LoPro Reverse Treated EDC (1TC/1TC) *LoPro foil is not available on 0.004" (0.101mm)thickness.

E Appendix 5

CGH40006P, 6 W, RF power GaN HEMT

Cree Inc.

CGH40006P

6 W, RF Power GaN HEMT

Package Types: 440109
PN's: CGH40006P

Cree's CGH40006P is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40006P, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40006P ideal for linear and compressed amplifier circuits. The transistor is available in a solder-down, pill package.

FEATURES

- Up to 6 GHz Operation
- 13 dB Small Signal Gain at 2.0 GHz
- 11 dB Small Signal Gain at 6.0 GHz
- 8 W typical at P_{IN} = 32 dBm
- 65 % Efficiency at P_{IN} = 32 dBm
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

PRELIMINARY
Rev 2.1 – April 2012

Large Signal Models Available for SiC & GaN

Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25˚C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	2.1	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	0.75	A	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Thermal Resistance, Junction to Case[3]	$R_{\theta JC}$	9.5	˚C/W	85˚C
Case Operating Temperature[3]	T_C	-40, +150	˚C	30 seconds

Note:
[1] Current limit for long term, reliable operation
[2] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[3] Measured for the CGH40006P at P_{DISS} = 8 W.

Electrical Characteristics (T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 2.1 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DS} = 28 V, I_D = 100 mA
Saturated Drain Current	I_{DS}	1.7	2.1	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 2.1 mA
RF Characteristics[2] (T_C = 25˚C, F_0 = 2.0 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	11.5	13	–	dB	V_{DD} = 28 V, I_{DQ} = 100 mA
Power Output at P_{IN} = 32 dBm	P_{OUT}	7.0	9	–	W	V_{DD} = 28 V, I_{DQ} = 100 mA
Drain Efficiency[3]	η	53	65	–	%	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{IN} = 32 dBm
Output Mismatch Stress	VSWR	–	–	10 : 1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 100 mA, P_{IN} = 32 dBm
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	3.0	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.1	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.1	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40006P-TB.
[3] Drain Efficiency = P_{OUT} / P_{DC}

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