THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Application of Metallic Nanoparticles and Vertically Aligned Carbon Nanofibers as Interconnect Materials for Electronics Packaging

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Contents

Abstract i

List of appended papers iii

Abbreviations v

Chapter 1 Introduction 1

- 1.1 Background 1
- 1.2 Scope 3
- 1.3 Outline 3

Chapter 2 Fabrication of nanostructured materials 5

- 2.1 Spark erosion 5
- 2.2 Chemical vapor deposition 6
- 2.3 Surface coating 7

Chapter 3 Nanocomposite solders 9

- 3.1 Wettability 11
- 3.2 Microstructure 12
- 3.3 Microhardness 13
- 3.4 Thermal fatigue 13
  - 3.4.1 Electrical test 14
  - 3.4.2 Mechanical test 15
  - 3.4.3 Failure analysis 15

Chapter 4 Vertically aligned carbon nanofibers 19

- 4.1 Carbon nanofibers 19
- 4.2 Transfer process 20
- 4.3 Electrical performance 22
- 4.4 Mechanical performance 23
- 4.5 Fracture surface 24

Chapter 5 Summary and outlook 29

Acknowledgements 31

Bibliography 33

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Abstract

In the electronics industry, packaging is responsible to protect chip from atmosphere and provide the path for signal communication as well as thermal dissipation. The realization of these functions in a packaging system depends on the performance of interconnect materials. Any failure on the interconnect materials could make entire system down.

Currently, one of the most popular interconnect materials is lead-free solder, which has been used for two decades instead of toxic Sn-Pb solder. The updates on processes, equipments and standards for lead-free solder have been completed. However, as continuous increase on the chip power and the miniaturization of consumer electronics, lead-free solder is facing big challenges. The disadvantages of traditional lead-free solder, such as high process temperature, grain coarsening and thermal fatigue failure, are gradually exposed. Therefore, one of the urgent needs for packaging is to develop new interconnect materials. In recent years, as the development of nanotechnology, nanostructured materials are gradually applied on the packaging. Following this tendency, two promising nanostructured interconnect materials are presented in this thesis.

The first part of this thesis shows a nanocomposite material. It consists of Sn-3.0Ag-0.5Cu nanoparticles and Sn-58Bi solder matrix. Sn-58Bi solder has the advantage on low process temperature. However the inherent brittleness of Sn-58Bi limits its application. For this reason, the Sn-3.0Ag-0.5Cu nanoparticles are added into the Sn-58Bi in order to improve the mechanical properties. The result of shear test shows that the shear strength of Sn-58Bi increases by two times by the addition of Sn-3.0Ag-0.5Cu nanoparticles. The result also indicates that the nanocomposite solder has excellent thermal fatigue resistance. The demonstrated properties make nanocomposite solder can be a potential candidate for replacing Sn-Ag-Cu in future.

In this thesis, we also present another kind of interconnect material based on vertically aligned carbon nanofibers. High stability and compatibility of carbon nanofibers are always attractive to the packaging industry. By using a series of processes, such as plasma-enhanced chemical vapor deposition, sputtering, transfer and bonding, the vertically aligned carbon nanofibers are successfully assembled in the packaging system. As interconnect material, vertically aligned carbon nanofibers exhibit acceptable electrical resistance and shear strength. The positive preliminary results motivate further research on the aspects of thermal fatigue resistance and stability.

Key words: Electronics packaging, Interconnect materials, Nanocomposite solder, Carbon nanofibers, Electrical resistance, Shear strength, Thermal fatigue, Fracture surface

List of appended papers

The thesis is based on the following papers

Paper A

A Reliability Study of Nanoparticles Reinforced Composite Lead-Free Solder

S. Chen, L. Zhang, J. Liu, Y. Gao, and Q. Zhai

Mater. Trans., vol. 51, no. 10, pp. 1720–1726, 2010.

Paper B

Ultra-Short Vertically Aligned Carbon Nanofibers Transfer and Application as bonding Material

S. Chen, D. Jiang, C. Zandén, Z. Hu, Y. Fu, Y. Zhang, L. Ye and J. Liu

Accepted by Solder. Surf. Mt. Technol.

Other journal papers not included due to being out of the scope of this thesis:

Coffin-Manson equation of Sn-4.0Ag-0.5Cu solder joint

S. Chen, P. Sun, X. C. Wei, Z. N. Cheng, and J. Liu

Solder. Surf. Mt. Technol., vol. 21, no. 2, pp. 48–54, Apr. 2009.

Development and Characterization of Nano-Composite Solder

J. Liu, S. Chen, and L. Ye

Lead-Free Solders: Materials Reliability for Electronics, K. N. Subramanian, Ed. John Wiley & Sons, Ltd, 2012, pp. 161–177.

Selective growth of double-walled carbon nanotubes on gold films

Y. Fu, S. Chen, J. Bielecki, A. Matic, T. Wang, L. Ye, and J. Liu

Mater. Lett., vol. 72, pp. 78–80, 2012.

Through-Silicon Vias Filled With Densified and Transferred Carbon Nanotube Forests

T. Wang, S. Chen, D. Jiang, Y. Fu, K. Jeppson, L. Ye, and J. Liu

IEEE Electron Device Lett., vol. 33, no. 3, pp. 420–422, 2012.

Formation of three-dimensional carbon nanotube structures by controllable vapor densification

T. Wang, D. Jiang, S. Chen, K. Jeppson, L. Ye, and J. Liu

Mater. Lett., vol. 78, pp. 184–187, 2012.

Paper-mediated controlled densification and low temperature transfer of carbon nanotube forests for electronic interconnect application

D. Jiang, T. Wang, S. Chen, L. Ye, and J. Liu

Microelectron. Eng., vol. 103, pp. 177–180, 2013.

A Highly Conductive Bimodal Isotropic Conductive Adhesive and Its Reliability

D. Li, H. Cui, S. Chen, Q. Fan, Z. Yuan, L. Ye, and J. Liu

Ecs Trans., vol. 34, no. 1, pp. 583–588, Mar. 2011.

Study on the Reliability of Fast Curing Isotropic Conductive Adhesive

W. Du, H. Cui, S. Chen, Z. Yuan, L. Ye, and J. Liu

Ecs Trans., vol. 34, no. 1, pp. 805–810, Mar. 2011.

Ultrafast Transfer of Metal-Enhanced Carbon Nanotubes at Low Temperature for Large-Scale Electronics Assembly

Y. Fu, Y. Qin, T. Wang, S. Chen, and J. Liu

Adv. Mater., vol. 22, no. 44, pp. 5039–5042, 2010.

Flip Chip Assembly Using Carbon Nanotube Bumps and Anisotropic Conductive Adhesive Film

X. Zhang, T. Wang, P. Berggren, S. Chen, and J. Liu

Ecs Trans., vol. 27, no. 1, pp. 825–830, Nov. 2010.

Abbreviations

EMC	Epoxy Molding Compound
PCB	Printed Circuit Board
PTH	Pin Through Hole
BGA	Ball Grid Array
IC	Integrated Circuit
I/O	Input/Output
VACNF	Vertically Aligned Carbon Nanofiber
CNF	Carbon Nanofiber
PECVD	Plasma-Enhanced Chemical Vapor Deposition
CVD	Chemical Vapor Deposition
SEM	Scanning Electron Microscopy
VACNT	Vertically Aligned Carbon Nanotube
CNT	Carbon Nanotube
SMT	Surface Mount Technology
IMC	Intermetallic Compound
CTE	Coefficient of Thermal Expansion
TEM	Transmission Electron Microscopy
CA	Conductive Adhesive
EDS	Energy Dispersive Spectroscopy

Chapter 1 Introduction

This introductory chapter provides information on the background of electronics packaging and the motivation of this work. The scope of research on interconnect materials is also illustrated in this chapter. The structure of this thesis is shown in the outline section.

1.1 Background

Packaging is the back-end-of-line of electronics industry and this thesis mentions different interconnect materials in the field of electronics packaging. If chip is described as the brain, the packaging can be the skeleton, nerve and skin. It is responsible for chip protection, signal transmission and heat dissipation.

According to the book written by R. R. Tummala[1], electronics packaging is divided into three levels, namely chip-level packaging, board-level packaging and system-level packaging. Chip-level packaging provides directly protection and communication to the chip. Figure 1(a) and (b) indicate a typical chip-level packaging with wire-bonding structures. The chip is firstly attached on a lead-frame with die attach and then a very thin metallic wire is used for connecting chip pad and frame lead. After wire-bonding, chip and lead-frame are sealed by epoxy molding compound (EMC) and then a common electronics component is formed. The exposed leads from EMC will be connected to the printed circuit board (PCB) by solder with pin-through-hole (PTH) structure as shown in Figure 1(a) or surface mount structure in Figure 1(b). This is called board-level packaging. If we further connect this PCB to a motherboard in a system, it is named system-level packaging. Currently flip-chip and ball-grid-array (BGA) structure as shown in Figure 1(c) is gradually replacing wire-bonding and PTH structure in both chip and board level packaging, because of the need to increase packaging density and decrease packaging size.

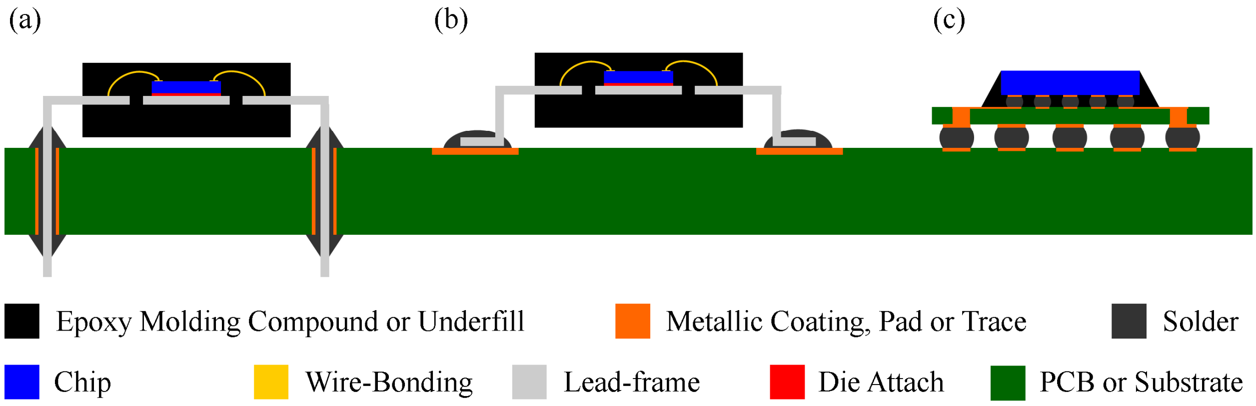


Figure 1. Schematic of packaging structures: (a) Wire-Bonding and Pin-Through-Hole, (b) Wire-Bonding and Surface Mount, (c) Flip-Chip with Ball-Grid-Array.

The development of electronics packaging significantly depends on the integrated circuit (IC) industry. According to Moore´s prediction, the density of transistor on IC will doubles about every two years[2]. This prediction has been proved by industry and significantly stimulated the development of ICs. In fact, the prediction also promoted the development of packaging, as shown in Figure 2. As the number of gates in unit chip increases, the number of input/output (I/O) in unit IC packaging also continuously increases, which obviously decreases the pitch size and increases power and current density. Table 1 summarizes the difference between wire-bonding/PTH packaging and flip-chip/BGA packaging on aspects of pitch, power and current density. It indicates that four times decrease on pitch size leads to twenty times increase on current density, and almost four hundred times increase on power density! This is a big challenge to interconnect materials due to heavier loading on smaller joint. Hence, the issue on the development of novel interconnect materials must be addressed.

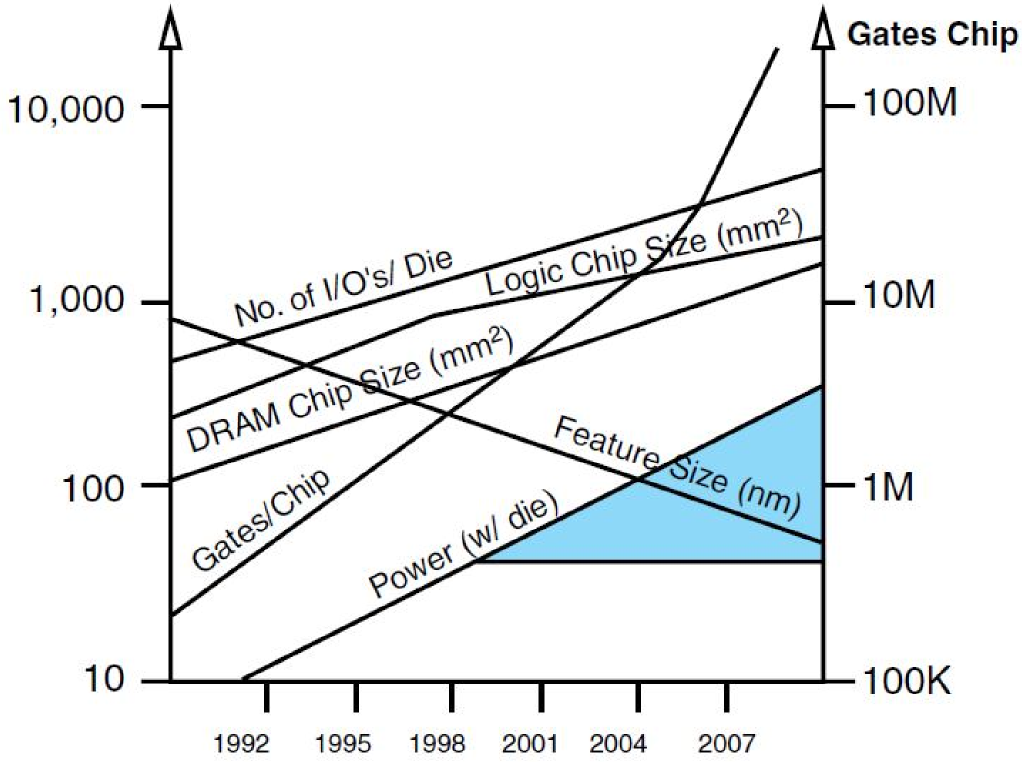


Figure 2. Semi-log Moore's plots of the Road-map data[1].

Table 1. Difference between wire-bonding/PTH packaging and flip-chip/BGA packaging [1].

Packaging	Pitch (mils)	Current density (A/mm^2)	Power density (W/cm^2)
Wire-bonding/PTH	100	1.6	0.024
Flip-chip/BGA	24	31.43	9.8

Besides the development on new materials, traditional processes also require the optimization for high density packaging. For instance, the process temperature for interconnect materials should be decreased to protecting electronics devices from warpage, heat stress and defect.

In addition, the packaging industry should always keep an eye on the environmental issues. For example, twenty years ago, a series of laws were made to limit the application of Pb in the electronics due to it is toxic and harmful to environment and human being health. This situation pushed the packaging industry to give up Sn-Pb solder and develop lead-free solder. This sudden turbulence made a big trouble on soldering process and production quality in the first few years.

1.2 Scope

The research in this thesis covers two types of interconnect material, namely nanocomposite lead-free solder and vertically aligned carbon nanofibers (VACNFs).

Solder normally consists of two or three metallic elements, such as Sn-37Pb and Sn-3.0Ag-0.5Cu, which has low electrical resistivity. Meanwhile, the mechanical property of solder is quite flexible due to it can be adjusted by changing composition or element ratio. However, traditional solders are still far away from the perfect interconnect material. The major shortages of solder are high process temperature, grain coarsening, high cost and toxicity. For solving these problems, one of possible solutions is to develop nanocomposite lead-free solder because nanostructured material is considered as an efficient reinforcement for solder matrix[3]. In this thesis, the work on nanocomposite solder is focused on the Sn-3.0Ag-0.5Cu nanoparticles reinforced Sn-58Bi. Both reinforcement and matrix in this system belong to Sn-based solder, which is capable of decreasing the mismatch.

Carbon nanofiber (CNF) is a low dimensional carbon material. As one of the most attractive materials, it has been researched on aspects of field emission device[4], microscopy[5], nanoelectromechanical switches[6], composite materials[7] and the manufacturing of IC[8]. In this thesis, only application of carbon nanofibers as interconnect materials is studied. Vertically aligned structured CNFs are selected because they are convenient for surface coating.

The process for fabricating nanostructured materials is provided in this thesis. The development on assembly process for new interconnect materials is also addressed. The experimental work is focused on the electrical and mechanical test. The work on microstructural characterization and failure analysis is also carried out for understanding the relationship between microstructure and mechanical properties.

1.3 Outline

This thesis consists of five chapters. Chapter 1 provides a general introduction on the background of electronics packaging and the scope of research. Chapter 2 gives information on the fabrication of nanostructured materials. The detail description on fabrication of Sn-3.0Ag-0.5Cu nanoparticles with spark erosion method and the growth of VACNFs with plasma-enhanced chemical vapor deposition (PECVD) method is presented. A brief introduction on the surface coating for nanostructured materials is also provided in this chapter. Chapter 3 is focused on the nanocomposite solder. The development of nanocomposite solder in last decade is summarized. Some experimental results from our research on Sn-3.0Ag-0.5Cu nanoparticles reinforced Sn-58Bi solder are also included in this chapter. Chapter 4 firstly describes the process for transferring VACNFs and then provides the result of electrical and mechanical test. The problem on current VACNFs joint is also discussed at the end of this chapter. The summary of this thesis is shown in Chapter 5.

Chapter 2 Fabrication of nanostructured materials

Nanostructured materials derive their special properties from having one or more dimension(s) made small compared to a length scale critical to the physics of the process[9]. These special properties drive engineers and researchers to develop the process for fabricating nanostructured materials. Nanostructured materials can be fabricated by top-down or bottom-up techniques. Top-down techniques are those in which the particles are fabricated from bulk material, and bottom-up techniques are those in which the particles are built atom by atom, or molecule by molecule. Typical top-down methods are mechanical milling and spark erosion. Some processes belonging to the bottom-up techniques are chemical vapor deposition (CVD) and chemical reduction. Here it will mainly introduce spark erosion method and CVD method because both methods are closely related to the research topics in this thesis.

2.1 Spark erosion

One method that seems very promising in the manufacturing of nanostructured materials is spark erosion method, also known as consumable-electrode direct current arc or arc discharge. Two major advantages of spark erosion method are the diversity of material selection and the compatibility of large scale production. The pure metals and complex alloy can be efficiently fabricated to the nanoscale by this method. The manufacturing setup, as schematically shown in Figure 3[10]. The spark will be triggered once proper gap and voltage between two electrodes are reached. A plasma channel will be formed during spark. This channel together with large energy and high pressure can increase the surface temperature of electrodes to around 10,000K in a few microseconds[11]. At such high temperature, the electrode will be molten and even evaporated. The molten part will quench in the dielectric to form micron particles. Meanwhile, the evaporated part will form nanosized particles. This method has been successfully used and published[12].

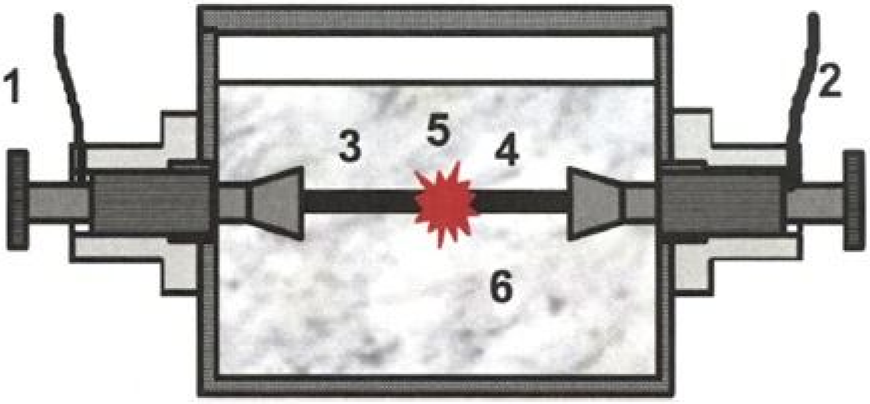


Figure 3. Schematic of spark erosion machine set-up[10]: (1) cathode, (2) anode, (3 and 4) bulk alloy electrodes, (5) spark, (6) dielectric coolant.

The Sn-3.0Ag-0.5Cu nanoparticles were fabricated by spark erosion method with 20A DC current in our research on nanocomposite solder. From scanning electron microscope (SEM) picture[13] in Figure 4, the diameter of spherical nanoparticles is smaller than 100nm.

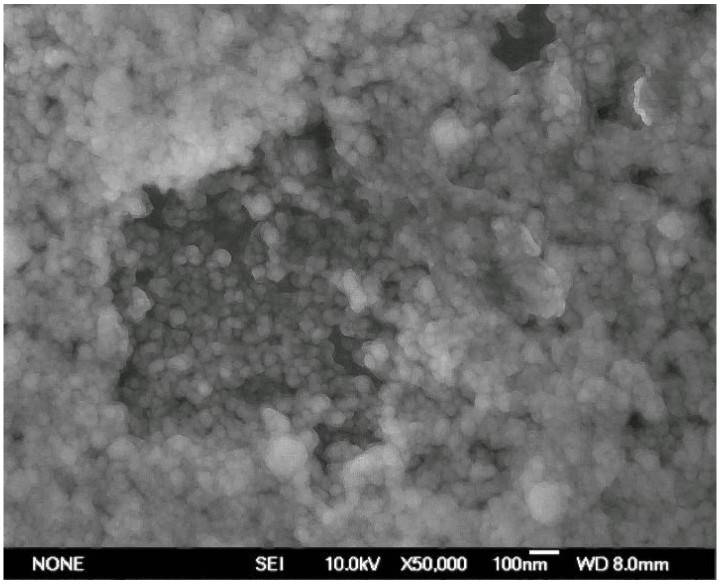


Figure 4. SEM image for Sn-3.0Ag-0.5Cu nanoparticles[13].

The nanoparticles were made in paraffin oil during the spark erosion process in order to prevent nanoparticles oxidation. However, the viscosity of paraffin oil is high. It will make nanoparticles dispersion more difficult. Moreover, sticky paraffin oil could be a barrier layer which can obstacle the contact between nanoparticles and matrix. Therefore, a separation process is needed to carry out before nanocomposite solder mixing process. The chloroform is used to replace paraffin oil from the surface of nanoparticles due to its high solubility to paraffin. After the replacement, the nanoparticles were separated from chloroform by centrifuge. The separated nanoparticles were dried off and then added into solder paste at nitrogen atmosphere. A planetary mixer was employed to mix nanoparticles and solder paste. The revolution and rotation speed is 400rpm and 105rpm, respectively. The mixing time is 30min.

2.2 Chemical vapor deposition

CVD forms thin film on the surface of a substrate by thermal decomposition or reaction of gaseous compounds. The desired materials is deposited directly from the gas phase on to the surface of the substrate[14]. CVD is the main method for producing vertically aligned carbon nanotubes (VACNTs) and VACNFs. The carbon from source gases like C_2H_2 and CH_4 deposits on the catalyst particles for building carbon nanotube (CNT) or CNF. The uniform distributed catalyst particles on the surface are generally formed by annealing several nanometers thick catalyst layer in the process chamber. Thermal CVD is usually used for VACNTs growth. Meanwhile, PECVD can be employed for VACNFs growth. The Figure 5 shows the morphology of as-grown VACNTs and VACNFs.

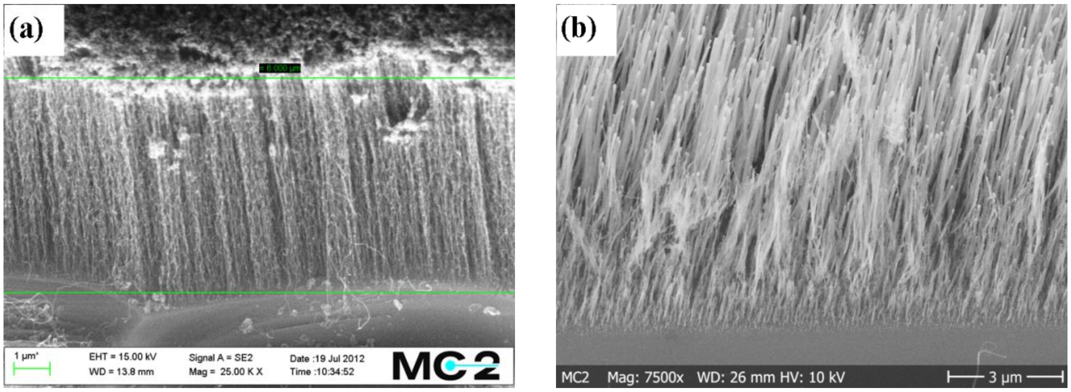


Figure 5. SEM observation on as-grown VACNTs by TCVD (a) and VACNFs by PECVD (b).

The VNCNFs for this thesis were grown on the silicon chip by PECVD method in a commercial machine Black Magic (Aixtron). A 7nm Ni catalyst layer was evaporated on the chip before growth process. At the beginning of growth process, the chip was put on a heater in the process chamber. Then, 5min annealing process was run at 625°C. During annealing process, the ammonia gas was injected into the process chamber with 200sccm flow rate for reducing possible oxidation on catalyst and forming discrete catalyst particles. After the annealing process, the temperature of the heater was risen to 700°C. Once the temperature reached, 40sccm acetylene gas flow was injected as carbon source for CNF growth. Meanwhile, the 600V DC plasma was loaded to promote gas ionization. The duration of growth process is 15min.

2.3 Surface coating

The coating on the surface of nanostructured materials is essential step for further application. If nanostructured materials are metallic materials like pure metal or alloy, polymer coating is generally necessary to prevent nanoparticles oxidation and agglomeration. However, coating thickness should be properly controlled. Thick polymer layer on the surface of nanoparticles will block the contact between nanoparticles and matrix and thus decrease the conductivity of nanocomposite materials. In another case, if non-metallic nanostructured materials, such as ceramic or carbon, need to be used in a metallic matrix, a metallic layer should be covered on the surface of reinforcement in order to merge reinforcement and matrix as one system.

The coating can be done by dry or wet method. The dry coating method is related to certain physical reaction like evaporation and sputtering whereas wet coating usually uses electrical or chemical reaction in certain solution. The coating method will be selected according to the reinforcement structure and type. In general, wet method is favorable to the coating of random distributed nanoparticles because nanoparticles can be dispersed in chemical solution by stirring or ultrasonic. Figure 6 (a) shows the Ag coated SiC nanoparticles as a case of wet coating method. For aligned materials coating, such as VACNTs and VACNFs, dry method is preferred due to alignment is easy to be destroyed by liquid flow during wet coating process. The sputtering method is used for VACNFs coating in our research. Figure 6 (b) shows the SEM observation on Au coated VACNFs.

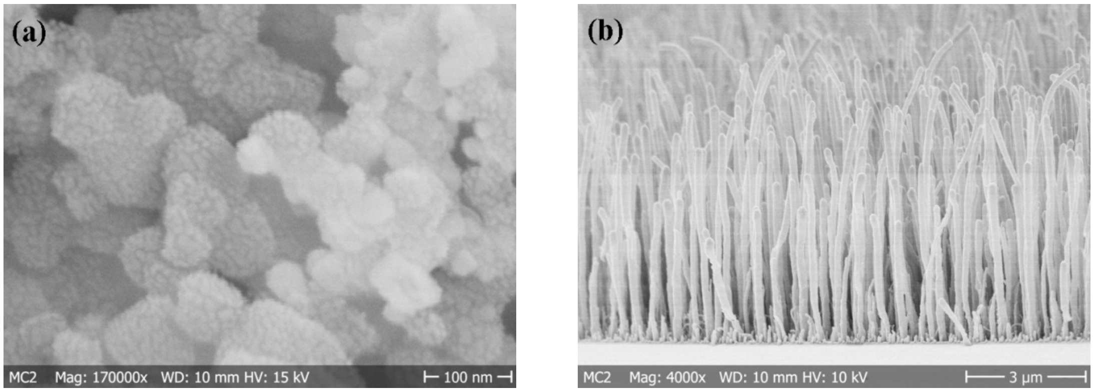


Figure 6. SEM observation on Ag-coated SiC nanoparticles (a) and Au-coated VACNFs (b).

Chapter 3 Nanocomposite solders

About twenty years ago, lead-free solder appeared in the electronics industry as the replacement of Sn-Pb solder. This substitution can be regarded as a revolution of interconnect materials. Although we haven't yet found an ideal lead-free solder to replace Sn-Pb, the processes, components and evaluation system for lead-free solder have been gradually established. For instance, the soldering temperature has been increased by 20% to meet the melting point of Sn-Ag-Cu alloy. Several commercial lead-free solders have been presented in the market. Table 2 lists the main lead-free solders we can find in current market. It shows that most of lead-free solders can demonstrate their qualified performance in one or two aspects. However, it is rare to see a lead-free solder satisfies the decent performance in every item. Thus the market is urgently looking forward to new interconnect materials which have excellent mechanical performance, high stability and low cost.

Table 2. Sn-based lead-free solder alloy systems.

System	Advantage	Disadvantage
Sn-Ag	Mechanical performance	High melting point
Sn-Cu	Economics	High melting point
Sn-Zn	Low melting point	Oxidation[15]
Sn-Bi	Low melting point	Brittleness[16]
Sn-In	Low melting point	High cost

Solders with intentionally incorporated reinforcements are termed composite solders[3]. Composite solder is a possible candidate as the new interconnect material. According to a previous summary work[3], reinforcements can effectively enhance the mechanical strength, increase the creep resistance and stabilize the microstructure of solders.

In recent years, nanotechnology is developing rapidly on the fabrication and characterization. When particle size reaches nanometer, some physical and chemical properties like melting point, conductivity, mechanical strength will be different comparing to microsized particles due to large surface area per unit volume and quantum effect. People have shown great enthusiasm about nanostructured materials and made great efforts to apply the characteristics of nanostructured materials in their fields. In the field of solder, various nanoparticles have been made and added into the traditional solder system attempting to synthesis novel nanocomposite solders. According to our work on literature researching, nanocomposite solder can be roughly divided into four types, namely monolithic-metal-reinforced nanocomposite solder, metallic-oxide-reinforced nanocomposite solder, alloy-reinforced nanocomposite solder and non-metallic-reinforced nanocomposite solder.

Table 3. Literature research on nanocomposite solders.

Nanostructured Reinforcement		Matrix	Form	Year
Monolithic metal	Cu	Sn-37Pb	Paste	2002[17], 2008[18]
		Sn-3.5Ag	Bulk	2009[19]
		Sn-3.5Ag	Paste	2011[20]
		Sn	Bulk	2010[21]
	Ag	Sn-37Pb	Paste	2004[22], 2010[23]
		Sn-0.7Cu	Paste	2008[18]
		Sn-9Zn	Paste	2009[24]
		Sn-3.0Ag-0.5Cu	Paste	2011[25]
	Al	Sn-3.5Ag-0.5Cu	Paste	2010[26]
		Sn-3.0Ag-0.5Cu	Paste	2012[27]
	Zn	Sn-3.8Ag-0.7Cu	Paste	2013[28]
	Mo	Sn-3.8Ag-0.7Cu	Paste	2011[29], 2012[30]
	Co	Sn-3.8Ag-0.7Cu	Paste	2011[31], [32]
	Sb	Sn-9Zn	Bulk	2012[33]
	Ni	Sn-3.8Ag-0.7Cu	Paste	2013[34]
Metallic Oxide	TiO_2	Sn-37Pb	Paste	2003[35], 2008[36]
		Sn-3.5Ag-0.5Cu	Paste	2010[37], 2011[38]
		Sn-3.5Ag-0.5Cu	Bulk	2011[39]
		Sn-3.5Ag-0.25Cu	Bulk	2010[40]
		Sn-0.7Cu	Paste	2012[41]
		Sn-3.0Ag-0.5Cu	Paste	2011[42], 2013[43]
		Sn-3.5Ag	Bulk	2011[44]
	Al_2O_3	Sn-37Pb	Paste	2008[36]
		Sn4In4.1Ag0.5Cu	Bulk	2005[45]
		Sn-0.7Cu	Bulk	2009[46]
		Sn-9Zn	Paste	2010[47]
		Sn-3.5Ag-0.5Cu	Bulk	2010[48]
	SnO_2	Sn-3.5Ag	Bulk	2009[49]
	$SrTiO_3$	Sn-3.0Ag-0.5Cu	Paste	2010[50]
	ZrO_2	Sn-3.0Ag-0.5Cu	Paste	2010[51], 2011[52]
		Sn-8Zn-1Bi	Paste	2013[53]
Alloy	Sn3.0Ag0.5Cu	Sn-58Bi	Paste	2010[54]
Non-metallic	POSS	Sn-3.5Ag	Paste	2005[55], 2010[56]
	SWCNT	Sn-37Pb	Bulk	2008[57]
		Sn-3.8Ag-0.7Cu	Bulk	2008[58]
	MWCNT	Sn-3.5Ag-0.7Cu	Bulk	2010[59]

Table 3 lists the major work on the nanocomposite solder in last decade. The matrix almost covers all of popular lead-free solders as well as Sn-Pb solders. For reinforcement, most of works are related to the pure metal and metallic oxide nanoparticles because they are easy to be purchased from market and convenient for analysis. The problems for metallic nanoparticles are oxidation and grain coarsening. For metallic oxide nanoparticles, the trouble is property mismatch to matrix. Both of them need a proper coating to solve their problems. So far, little work has been done on the alloy-reinforced nanocomposite solder. The Sn-3.0Ag-0.5Cu nanoparticles reinforced Sn-58Bi nanocomposite solder has been developed in our laboratory. Sn-58Bi is a representative of low melting point lead-free solders. The melting point of Sn-58Bi is only 137°C. It is usually used in step soldering process. However, the natural brittleness of Sn-58Bi[60] limits its application in the packaging. Therefore, Sn-3.0Ag-0.5Cu nanoparticles are dispersed into Sn-58Bi solder paste in order to improve the mechanical performance. Advantages of this kind of nanocomposite solder are very obvious. Firstly, nanoparticles and matrix is both Sn-based alloy, which is beneficial for eliminating mismatch. Secondly, the process temperature of nanocomposite solder is low due to the low melting point of Sn-58Bi matrix. Thirdly, the Sn-3.0Ag-0.5Cu nanoparticles can effectively enhance the strength of Sn-58Bi due to dispersion strengthening effect.

Table 3 also provides some information on the form of nanocomposite solder. From presented work, the nanocomposite solder are manufactured to be either paste form or bulk form. For the paste form solder, the reinforcements and matrix powders are blended to be a mixed filler system at first. Then, the proper flux is added and stirred together with filler system to form nanocomposite solder paste. For simplifying process, some researchers also directly add certain volume of reinforcements into commercial solder paste. The paste form nanocomposite solder is more compatible with surface mount technology (SMT) process in electronics industry. However, the critical problem for paste like nanocomposite solder is the separation phenomenon. The nanostructured reinforcements are quite easy to be regarded as impurity in a matrix system and thus taken away by flux. Some studies have shown that[29][30][32] more than half of reinforcements were finally stored in the flux residue but not in the solder system after reflow. Although the separation issue has not been mentioned in literature, we believe it is inevitable for all kinds of nanocomposite solder paste as long as property mismatch between reinforcements and matrix exists in composite system.

For bulk form solder, solder powder with certain volume nanostructured reinforcements are also mixed at first like paste form. Then sinter, extrusion or casting-cooling processes are applied to make bulk form solder. It is possible to keep more nanostructured reinforcements in the bulk form due to flux-free process. However, dispersion and void problem need to be further studied. Currently, most people concentrate their experiments on wettability, microstructure, and microhardness. The variation of microstructure after thermal aging or multi-reflow test is also presented in some literatures. The possible mechanism for enhancement effect of nanoparticles is illustrated. However, thermal fatigue resistance, as one of the most important properties for solder, has not been studied sufficiently.

3.1 Wettability

Wettability is a critical property of solder. Good wettability of solder on substrate is an essential condition for reliable bonding formation. Wettability is generally evaluated by the wetting angle and smaller wetting angle usually means better wettability. From current studies, it seems that different reinforcements bring different effects on wetting angle. For example, wetting angle is increased by adding Co[32], Ni[34] or Zn[28] nanoparticles in the solder system but decreased by Cu[20] and Ag nanoparticles[25]. The reason is still unclear because wettability is extremely sensitive to material properties and atmosphere condition. So far, what we can confirm is that nanostructured reinforcements can actually increase the viscosity as shown in Figure 7[61]. With only 3wt% nanoparticles addition, the viscosity of solder paste increased by 20%. The increase of viscosity may result in the increase of wetting angle. Meanwhile, the improvement effect of nanostructured reinforcements on wetting angle is attributed to the decrease of interfacial tension at the solid/liquid interface[20].

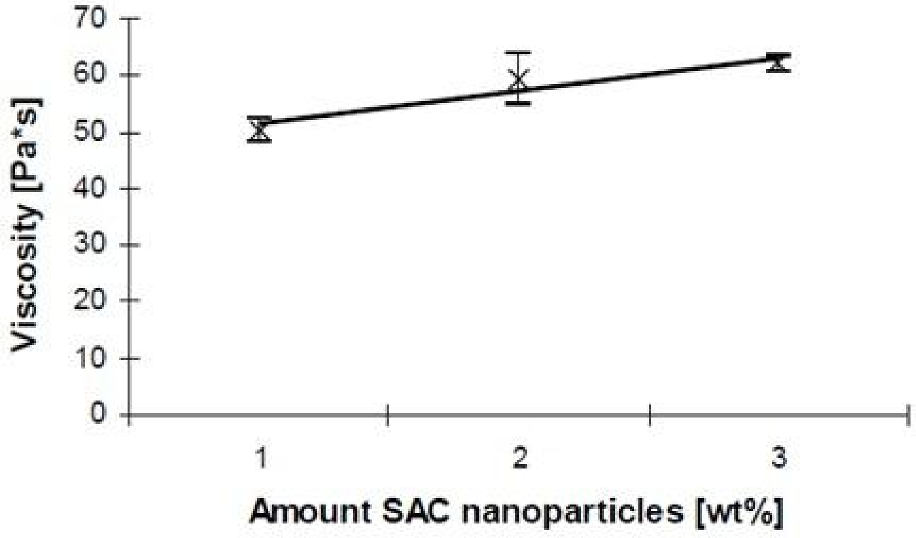


Figure 7. Effect of Sn-3.0Ag-0.5Cu nanoparticles on the viscosity of Sn-58Bi[61].

3.2 Microstructure

In most studies, it is found that the grain size will decrease significantly if nanostructured particles are presented in the structure. The possible explanation is the absorption theory[37]. The nanostructured reinforcements will attach to the surface of grain or embed into grain boundary and then decrease the surface activity, which will delay grain growth and coarsening. Besides the absorption theory, the effect of nanostructured reinforcements on providing more nuclear sites in solder system during solidification was also mentioned in some papers as the explanation for the decrease of grain size[40][50][51].

The refined microstructure was also observed in our nanocomposite solder. The microstructure of pure Sn-58Bi solder and nanocomposite solder with 1wt% nanoparticles are shown in Figure 8. The grain size in the Sn rich phase of nanocomposite solder is finer than that of pure Sn-58Bi solder.

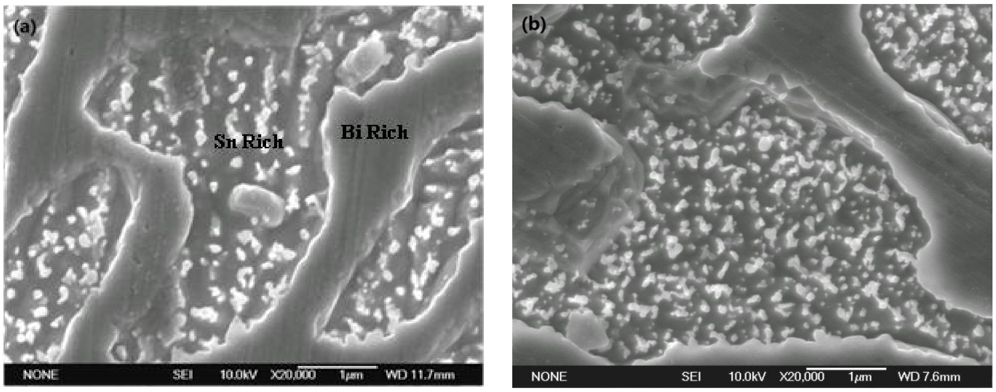


Figure 8. SEM observation on the cross-section of pure Sn-58Bi solder (a) and nanocomposite solder with 1wt% nanoparticles (b).

In addition, the researchers also pay much attention to the thickness variation on intermetallic compound (IMC) layer after the addition of nanostructured reinforcements. The function on suppressing the growth of IMC layer was shown in many kinds of nanostructured reinforcements except Ni, Co and Zn nanoparticles, for that additional IMC layer was generated[34][31][32]. The suppression of nanoparticles on the thickness of IMC layer can be explained by same absorption theory.

3.3 Microhardness

The mechanical properties of metallic materials are usually quantified by its hardness. The value of hardness provides a measure of the resistance of the material to deformation, densification, and cracking[57]. The increase of microhardness was observed after mixing nanostructured reinforcements into the original solder system. The influence of Sn-3.0Ag-0.5Cu nanoparticles on the microhardness of Sn-58Bi solder is shown in Figure 9[61]. It shows that the microhardness of pure Sn-58Bi was increased by 15% by the addition of 5wt% nanoparticles.

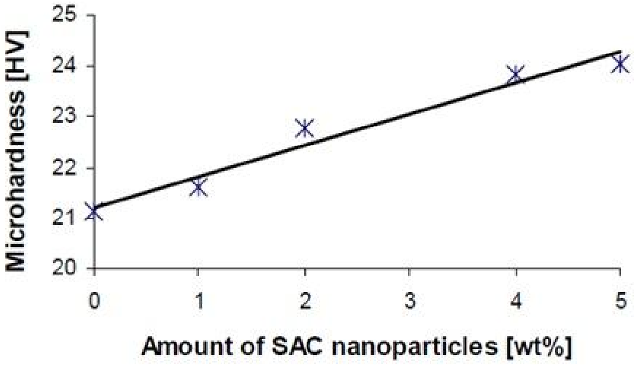


Figure 9. Effect of Sn-3.0Ag-0.5Cu nanoparticles on the microhardness of Sn-58Bi[61].

Theoretically, this phenomenon could be supported by the Hall–Petch mechanism [57][61] and dispersion strengthening theory[48][56]. Because the grain size and spacing between particles are effectively refined by the addition of nanostructured reinforcements as mentioned in section 3.2., more energy is required for grain boundary slide and crack propagation, thus resulting in enhanced microhardness.

3.4 Thermal fatigue

Thermal fatigue is a major failure mode for solder joint. The temperature variation caused by switch on/off or atmosphere change can make stress increased in the solder joint due to the coefficient of thermal expansion (CTE) mismatch between components like chip and substrate. Thermal cycling test is an effective method to evaluate the thermal fatigue resistance of solder joint. Thus our experimental work for nanocomposite solder is focused on measuring the variation of electrical and mechanical performance of solder joint before and after thermal cycling.

As-prepared nanocomposite solder paste was used to make the solder joint in the test sample for thermal cycling. The assembly process followed common SMT process. The solder paste was printed on the (electroless nickel immersion gold) ENIG/Cu pads at first. Then chip resistors were mounted on pads. Finally, reflow process was run according to the Sn-58Bi reflow profile. The assembly test board is shown in Figure 10. Each board includes fifty chip resistors, namely one hundred solder joints. No obvious nanoparticles can be observed around the solder joint, which shows the good compatibility between nanoparticles and matrix.

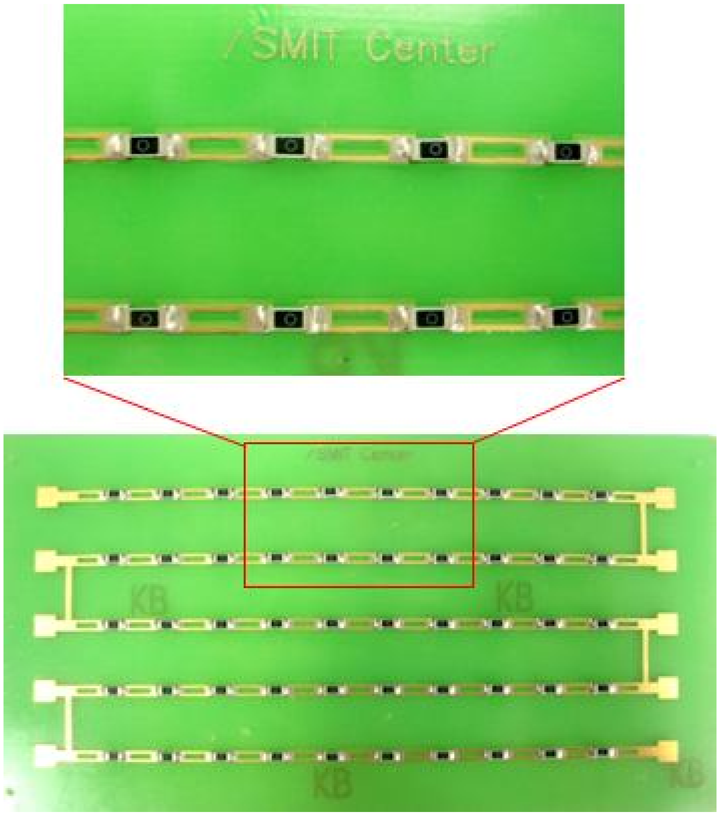


Figure 10. Test board for thermal cycling test.

3.4.1 Electrical test

Figure 11 shows, for all kinds of sample, no obvious difference on the electrical resistance before and after thermal cycling. No large change of electrical resistance in the nano-enhanced composite solder can be observed during thermal cycling. However, it's difficult to know whether crack initiation and growth has occurred or not. If the crack is much smaller than the size of solder joint, it is difficult to detect the change on the electrical resistance at room temperature.

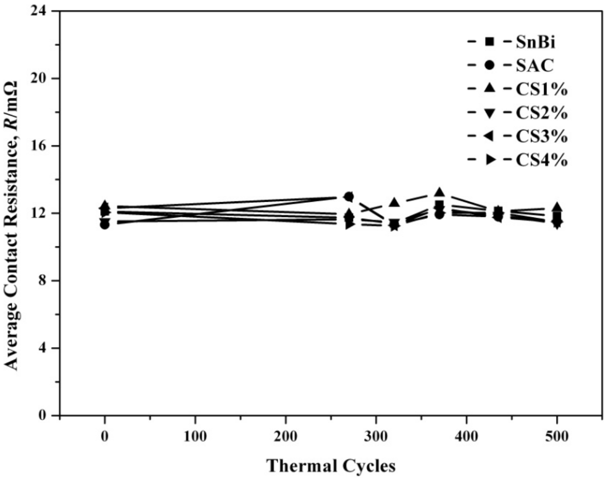


Figure 11. Average contact resistances during thermal cycling.

3.4.2 Mechanical test

The results of shear test are shown in Figure 12. Before thermal cycling, the shear strength of nanocomposite solders are almost two times higher than that of pure Sn-58Bi solder and comparable with the shear strength of Sn-3.0Ag-0.5Cu solder, which maybe results from finer microstructure and the dispersion strengthening effect. After thermal cycling, we observed the obvious degradation of strength in the pure Sn-58Bi and nanocomposite solders with more than 2wt% nanoparticles. The possible reason is described in next section.

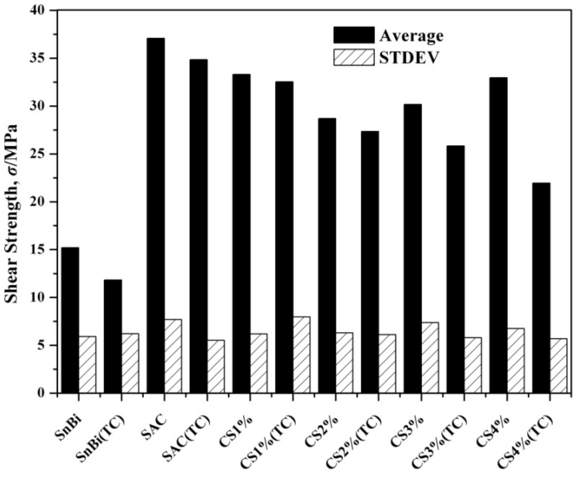


Figure 12. Result of shear test before and after thermal cycling.

3.4.3 Failure analysis

Figure 13 shows optical microscopy observation on the cross-section of pure Sn-58Bi solder and nanocomposite solders after thermal cycling. The visible cracks can be found in pure Sn-58Bi sample and nanocomposite solders with 3wt% nanoparticles and 4wt% nanoparticles. Meanwhile, no similar crack is detected in the nanocomposite solder samples with less than 2wt% nanoparticles, as shown in Figure

13(d) and (e). This phenomenon implicates that the nanoparticle is able to limit crack generation but at the same time too many nanoparticles in the solder joint can inversely promote crack formation.

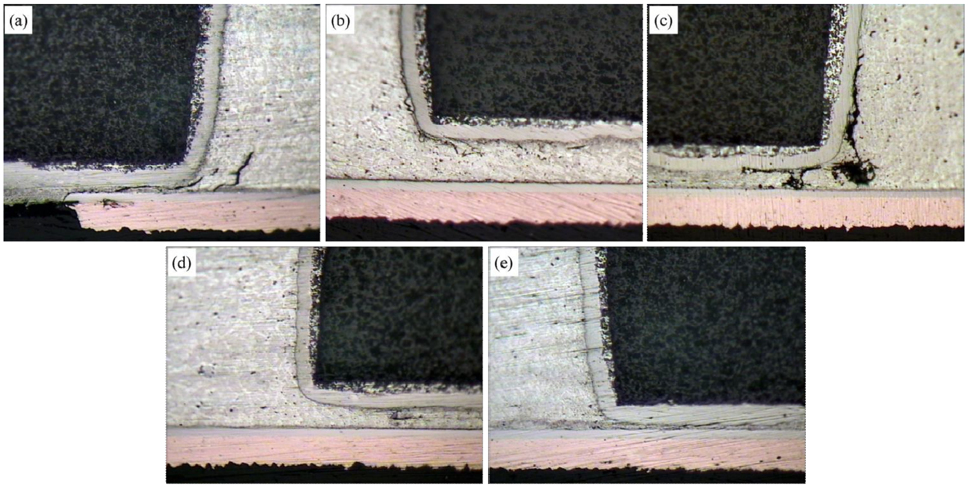


Figure 13. Cross-section observation on pure Sn-58Bi (a) and nanocomposite solder with 3wt% nanoparticles (b), 4wt% nanoparticles (c), 1wt% nanoparticles (d) and 2wt% nanoparticles (e).

As known, crack is one of possible reasons for strength decreasing after thermal cycling. The initial small cracks prefer to generate near defects or in the place where shear strain is largest. These small cracks propagate with thermal cycling progress and finally link each other to form a big crack in solder joint.

For nanocomposite solder, nanoparticles can be uniformly distributed in the solder matrix as shown in Figure 14. These nanoparticles are capable of blocking the crack propagation or changing propagation direction during thermal cycling. In this case, more energy is required for crack propagation. It will effectively retard the cracks linking and thus enhance the thermal fatigue resistance of solder. However, the interface between nanoparticle and matrix is also a potential risk for a reliable bonding because the interface will promote the generation of small cracks during thermal cycling. More interfaces in solder joint maybe result in more small cracks, which will shorten the path for cracks linking and then accelerate the formation of big crack. Therefore, the volume of nanoparticles in the nanocomposite solder must be controlled precisely for maximizing the effect of enhancement.

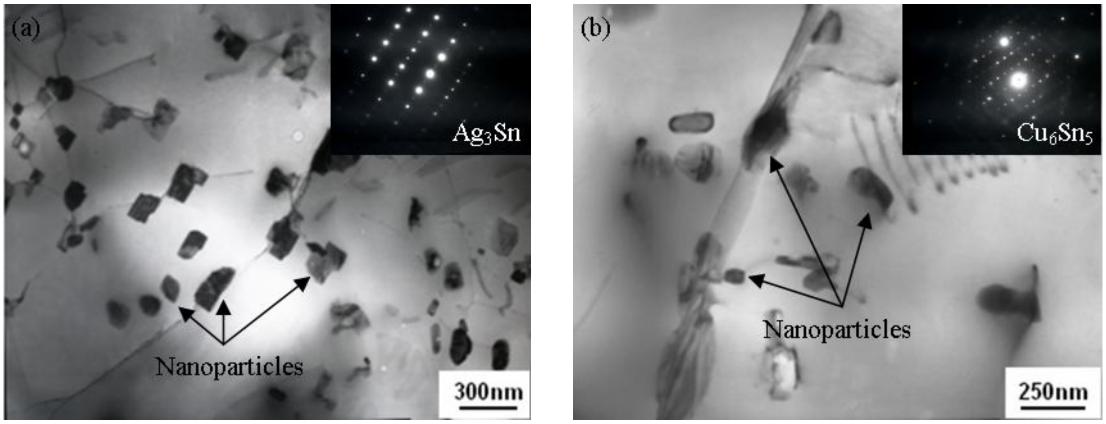


Figure 14. TEM and diffraction pattern analysis on nanocomposite solder with 1wt% nanoparticles.

Besides cross-section observation, the facture surface is also analyzed after the shear test. According to the optical microscopy observation, two kinds of fracture mode are defined. One is named fracture within solder, which means the fracture happened in the solder as shown in Figure 15(a). Another mode named fracture at the interface. In this mode, the fracture is located at the interface between solder and resistor termination, which is shown in Figure 15(b).

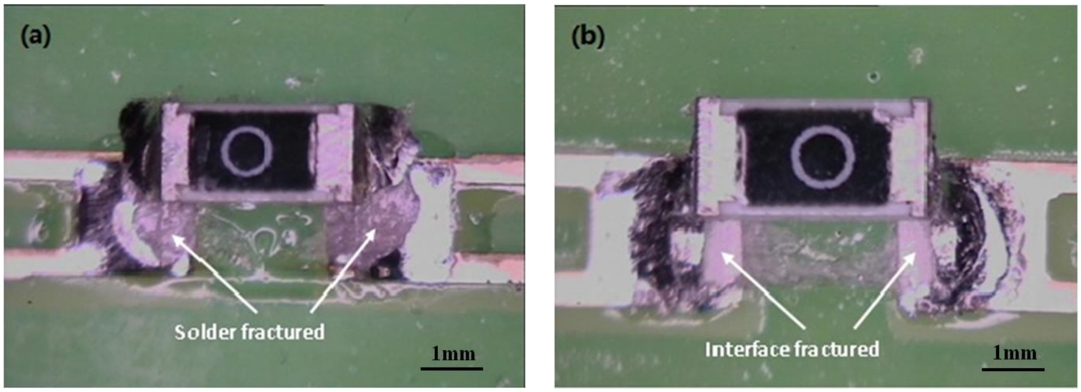


Figure 15. Analysis on fracture surface: (a) Fracture within solder, (b) Fracture at interface.

Figure 16 shows the statistic results of fracture mode. It indicates that most of fracture surfaces belong to fracture at interface mode for all kinds of nanocomposite solder before thermal cycling. Conversely, more than half fracture surfaces are observed in the solder for pure Sn-58Bi samples whatever before or after thermal cycling. It implicates that the addition of nanoparticles make the strength of nanocomposite solder higher than that of interface bonding and then decrease the number of fracture in solder mode. However, once the content of nanoparticles exceeds 2wt%, the case of fracture within solder will increase after thermal cycling. The possible reason can be attributed to the increase of number on void and crack in solder joint after thermal cycling, which make solder weaker than before and interface.

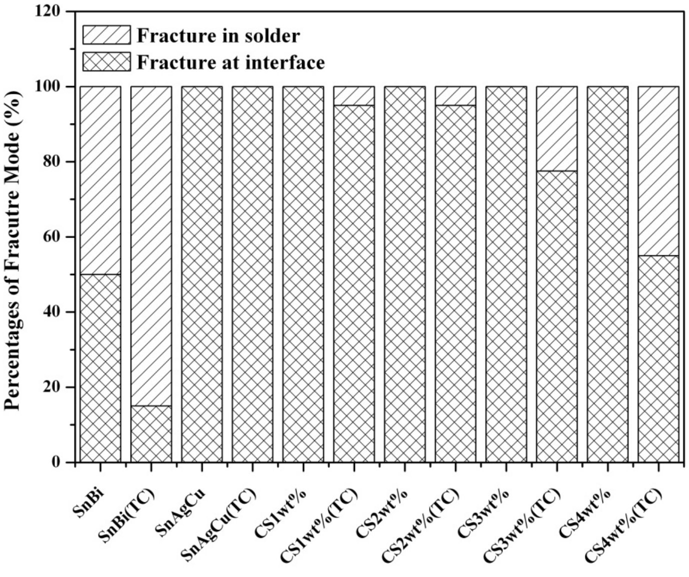


Figure 16. Statistics in percentage of fracture mode (CS1wt%: nanocomposite solder with 1wt% nanoparticles).

Chapter 4 Vertically aligned carbon nanofibers

Low dimensional carbon materials generally include fullerene, CNT and graphene. CNT can be regarded as rolled graphene. Based on the different rolling directions, CNT shows its electrical property as metal or semiconductor[62]. CNT has many excellent properties, such as high current carrying capacity[63], high thermal conductivity[64], high Young's modulus[65] and high flexibility[66]. The study on interconnect materials has covered random distributed CNTs as reinforcement materials in lead-free solder[58][59] and VACNTs as interconnect materials for through silicon via structure[67].

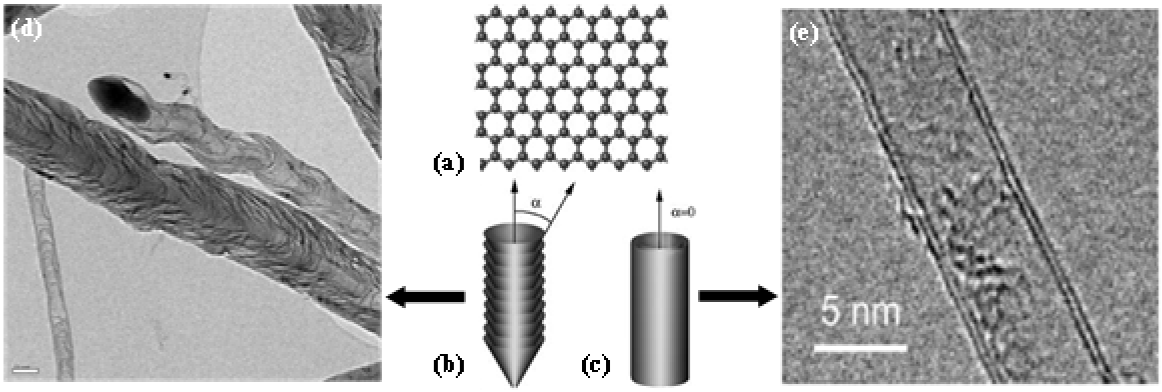


Figure 17. Schematics of graphene (a), carbon nanofiber (b) and carbon nanotube (c)[68]. TEM pictures for carbon nanofiber (d) and carbon nanotube (e)[69].

If we roll graphene layer with certain angle to form a cone and then stack a plenty of such cones in one direction, the structure of CNF will emerge as shown in Figure 17(b)[68]. The transmission electron microscopy (TEM) pictures show the real structure of CNF in Figure 17(d) and CNT in Figure 17(e)[69].

Although low dimensional carbon materials possess many advantages, they still have to face tough challenges from the industry and society. For example, the bonding between carbon and traditional interconnect materials is usually bad if without support from additional coating. However, the high surface stability of carbon materials always makes the coating process hard. In addition, the fabrication condition for low dimensional carbon materials is very harsh. That means that they generally can't be used directly in the packaging. In recent years, a lot of effective processes have been developed aiming to low dimensional carbon materials, such as densification process[70] and transfer process[71].

4.1 Carbon nanofibers

As we have introduced before, CNF is a cone-stack structure material. If we look at the structure of CNF, it is actually not as perfect as CNT's. The angle of cone structure implicates that the charge transport direction wouldn't only be decided by axial direction. The van der Waals bonding between cones also determines the mechanical strength which wouldn’t be as strong as in-plain covalent bonded CNT. Meanwhile, the chemical property of CNF is also not stable due to exposed edges[68]. However, the CNF is still worthwhile as interconnect material owing to special advantages comparing to traditional materials. For example, CNF has high resistance to electrical[72] and chemical corrosion. The electromigration and degradation problems can be resolved. These problems always make a big trouble on solders and conductive adhesive (CA). The excellent thermal stability of CNF also ensures a stable microstructure under high temperature loading or long term thermal aging test. Therefore, the grain coarsening can be avoided by using CNF as interconnect materials. Moreover, the VACNFs, grown by CVD method, can be uniformly dispersed on the surface of substrate. The agglomeration issue of nanostructured materials can be neglected. The reason we choose VACNFs but not VACNTs in this study is the structure of VACNFs is more convenient for coating process than that of VACNTs. As shown in Figure 5 in section 2.2, the spacing between single CNFs in VACNFs is big enough therefore beneficial for sputtering process. It's impossible to coat each carbon nanotube by similar coating method due to the ultra-fine gap between CNTs in VACNTs forest. Therefore, comparing to CNT, CNF is compatible with current packaging processes and possible to be widely accepted by industry. However, one of the challenges for VACNFs is the transfer process. Although the transfer process for VACNTs has been developed by our group[71], it can't be directly used for VACNFs because VACNFs is much shorter than VACNTs and thus is more sensitive to the parameters of transfer process.

4.2 Transfer process

As we have mentioned in section 2.2, the temperature for growing VACNFs can reach 700°C. Nothing can work as normal at such temperature in a packaging system. Therefore, as-grown VACNFs must be transferred to another functional chip. The transfer process is shown in Figure 18. 20nm Ti and 100nm Au was sputtered on the surface of carbon nanofiber at first. After sputtering, the average diameter of CNF increased from 55nm to 147nm, as shown in Figure 19. The 92nm increase in diameter is consistent with the input thickness in sputtering machine. In addition, the catalyst particle on the head of CNF is invisible after sputtering due to the coating layer.

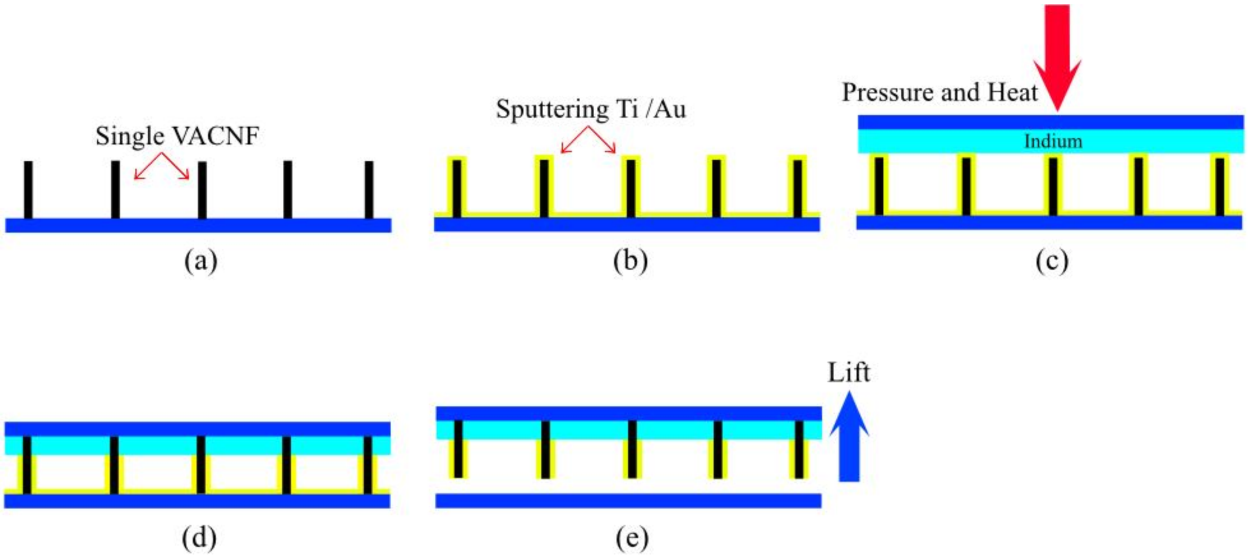


Figure 18. Schematic of VACNFs transfer process: (a) VACNFs were grown on growth chip by PECVD method, (b) 20/100nm Ti/Au metallic layer was coated on VACNFs surface by sputtering, (c) Target chip with 1µm In layer was pressed on growth chip with heating, (d) VACNFs were wetted by In at 160°C, (e) Target chip was separated from growth chip at room temperature.

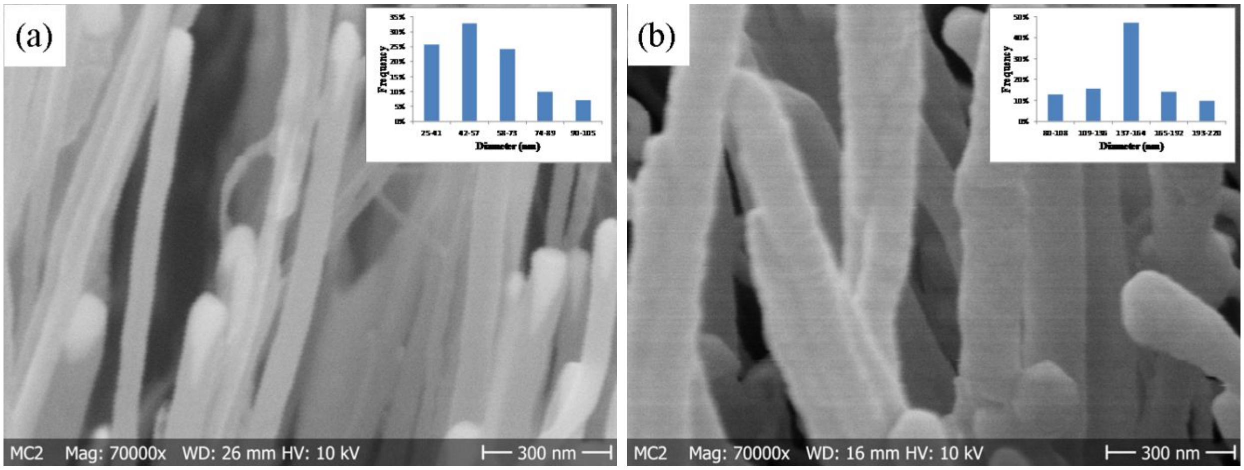


Figure 19. SEM pictures on VACNFs before (a) and after (b) sputtering.

After coating, the transfer process is carried out. Before transfer, an indium coated target chip was prepared, as shown in Figure 18(c). The thickness of indium is 1µm. The transfer process was carried out by a flip-chip bonder which can control heating temperature, time and pressure. The growth chip with VACNFs was pressed on the target chip with 5MPa pressure at 160°C which is just little higher than the melting point of indium. The duration of heating is 20s. In this short time, indium was molten and wetted the head of CNF. The bonding between indium layer and the head of CNF can help pull CNF out from growth chip during separation step. The wetting area on the surface of CNF must be controlled by precisely adjusting process parameters. The whole surface wetting maybe makes indium react with Ti/Au layer and form bonding on the surface of growth chip. It is difficult to achieve entire transfer for VACNFs if comparable bonding force is presented at two sides (growth chip side and target chip side). From SEM pictures in Figure 20, the VACNFs still keep basically straight up after transfer process. Meanwhile, the head of CNF has embedded into the indium layer about 500nm.

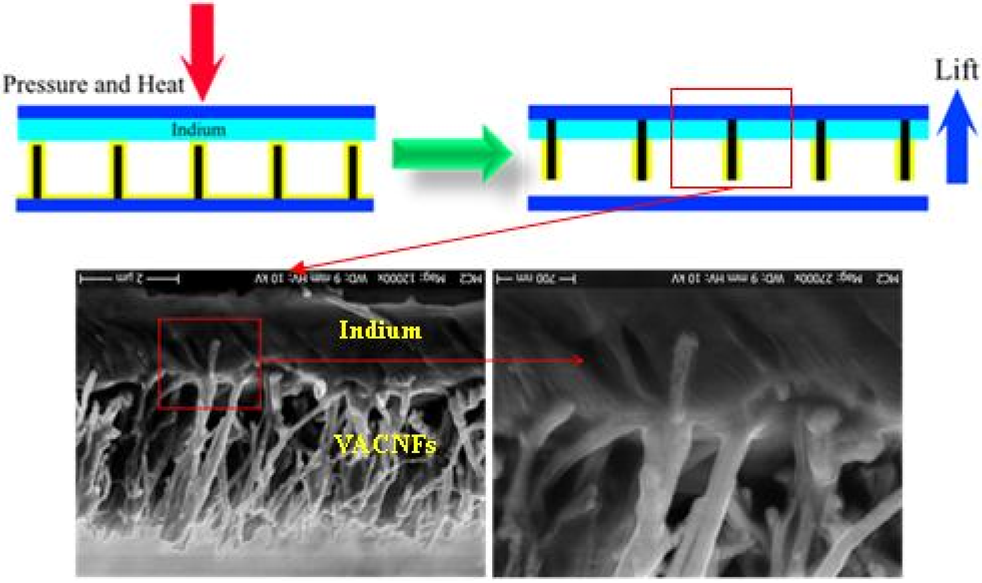


Figure 20. SEM observation on the VACNFs after transfer process.

4.3 Electrical performance

A sample with bridge structure was prepared for electrical test. As Figure 21(a) shown, two VACNFs pads were located at two sides of an indium coated silicon chip by described transfer process. Then Ti/Au was sputtered on transferred VACNFs again in order to enhance the bonding quality. This silicon chip was then mounted on two Au coated silicon chips by flip-chip bonder, as shown in Figure 21(b). Comparing to the transfer process, longer time, higher temperature and bigger pressure were used in bonding process because it's expected that the molten indium is able to cover entire CNF surface and reach the other side to form In-Au bonding. Figure 21(c) and (d) show that the VACNFs are a little leaning in the sandwich structure due to the high pressure in the bonding process.

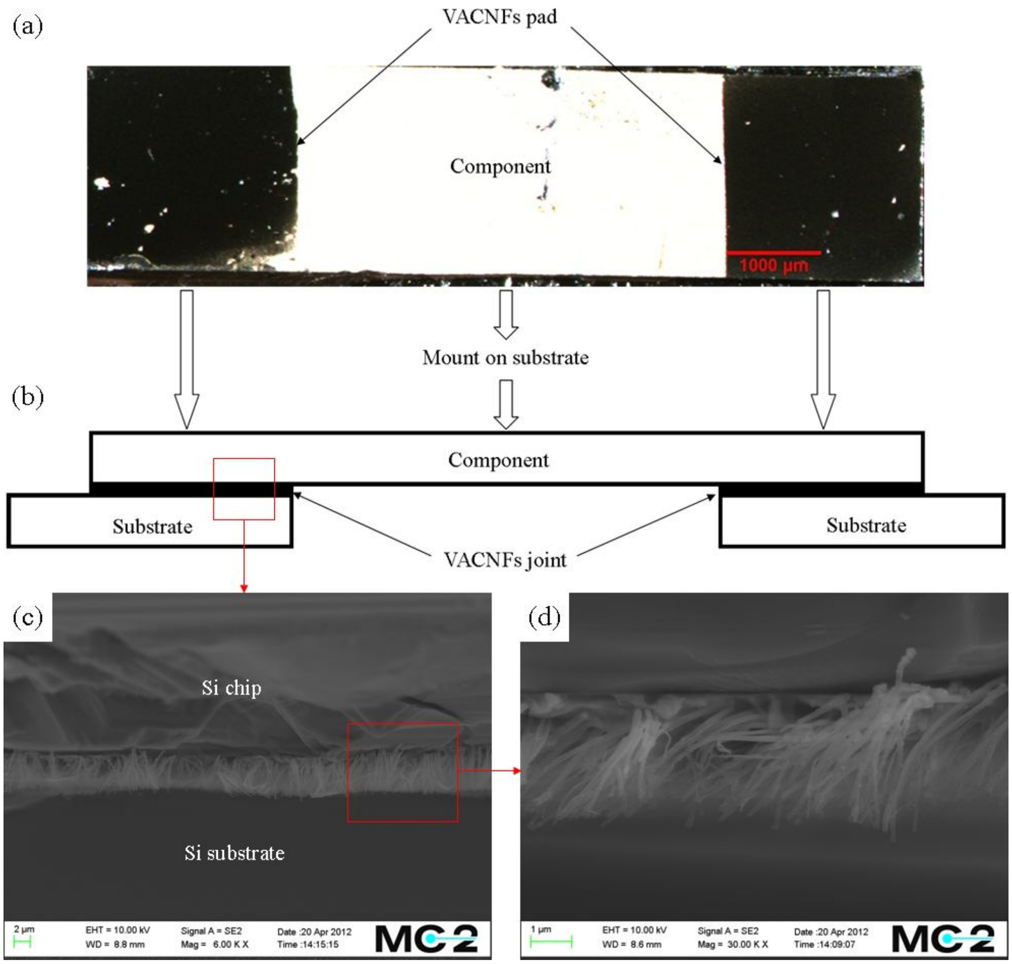
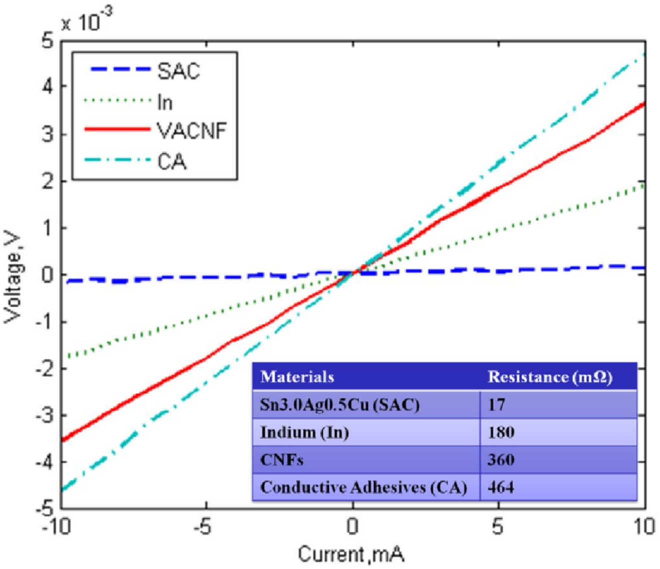


Figure 21. Bridge structure sample for electrical test: (a) indium coated Si chip with two VACNFs pads, (b) schematic for bridge structure sample, (c) SEM observation on cross-section of VACNFs joint, (d) close-up view on the red frame in (c).

For evaluating the electrical performance of VACNFs, three traditional interconnect materials, Sn-3.0Ag-0.5Cu solder, CA and indium piece, were tested with same structure and condition together with VACNFs. The test results are shown in Figure 22. All of I-V curves show a good linear relationship. The table in Figure 22 displays the resistance of four kinds of interconnect materials. It indicates that the electrical performance of VACNFs is comparable with CA and one order of magnitude lower than metallic materials. If we take into account the electrical and chemical advantages of VACNFs, this test result is quite interesting for potential bonding application.



Materials	Resistance (mΩ)
Sn3.0Ag0.5Cu (SAC)	17
Indium (In)	180
CNFs	360
Conductive Adhesives (CA)	464

Figure 22. I-V curves and the result on resistance measurement.

4.4 Mechanical performance

As shown in Figure 23(a), the sample structure of the shear test is a little different from that of the electrical test. The as-grown VACNFs were firstly transferred to an indium coated silicon substrate. Then, a square Au coated chip was mounted on the silicon substrate directly with same bonding process we have described before.

The force-distance relationship was shown in Figure 23(b). All of five VACNFs samples show the similar force-distance relationship. The force will suddenly drop once the shear head has moved a certain distance. It implicates that the fracture mode of VACNFs joint belongs to brittle fracture. In addition, the average shear strength of VACNFs joint is 1.5MPa. Comparing to our previous experiment[54][73], this value is almost one order of magnitude lower than solder and CA. The possible reason is the bond line thickness of VACNFs is only 2~4μm after the bonding process. It's much thinner than that of solder and CA (50~100μm).

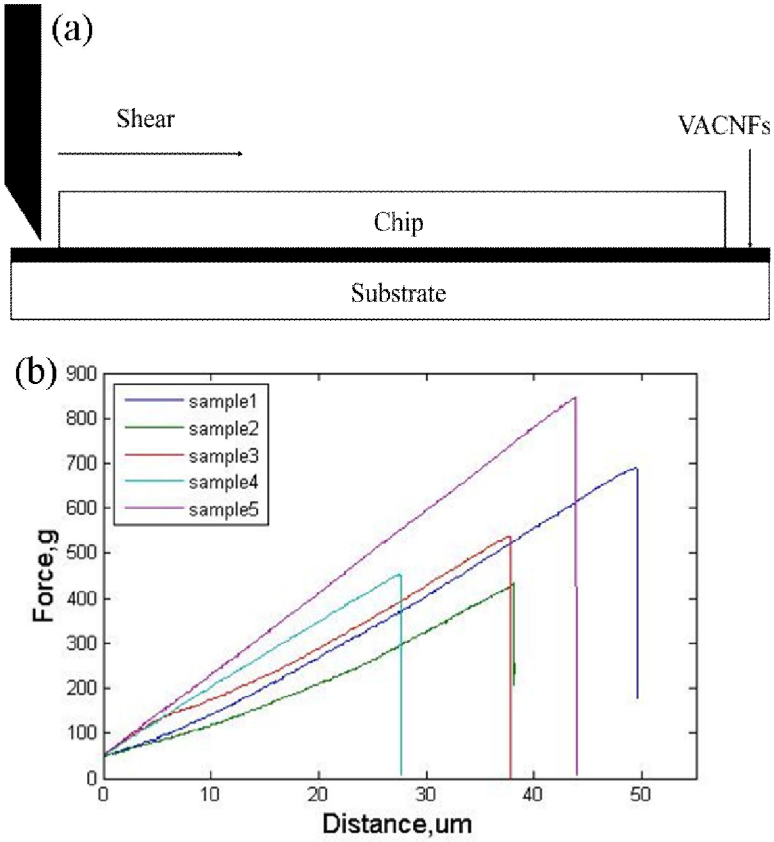


Figure 23. Shear test: (a) Schematic drawing of the shear test set-up, (b) Force-distance relationship during the shear test.

4.5 Fracture surface

The fracture surface was checked by SEM after the shear test. The energy dispersive spectroscopy (EDS) analysis was also carried out on the fracture surface at chip side to confirm composition. Figure 24(a) shows the fracture surface at chip side. It is clearly split to dark area and bright area. Figure 24(b) shows that the dark area is VACNFs and the bright area is the chip surface. Figure 24(c) indicates that, after bonding process, the surface of carbon nanofiber is rougher than the surface of as-coated CNF, as shown in Figure 19(b). It implicates that the surface reaction happened on the Au coated CNF during bonding process. EDS results confirm that the rough surface contains In-Au IMC with atomic ratio about 3:1. It proves that a complete IMC shell was formed on the surface of CNF. Some islands can be also observed on the surface of chip. From EDS analysis, they are also same In-Au IMC. It proves that the IMC layer began to form at the interface. In the VACNFs area, some In-Au IMC pieces were observed at the tips of VACNFs. These IMC pieces should come from the interface at the other side. Figure 24(c) also shows some broken CNFs. The cross-section of broken CNF displays a kind of circular-hollow structure, as shown in Figure 24(d).

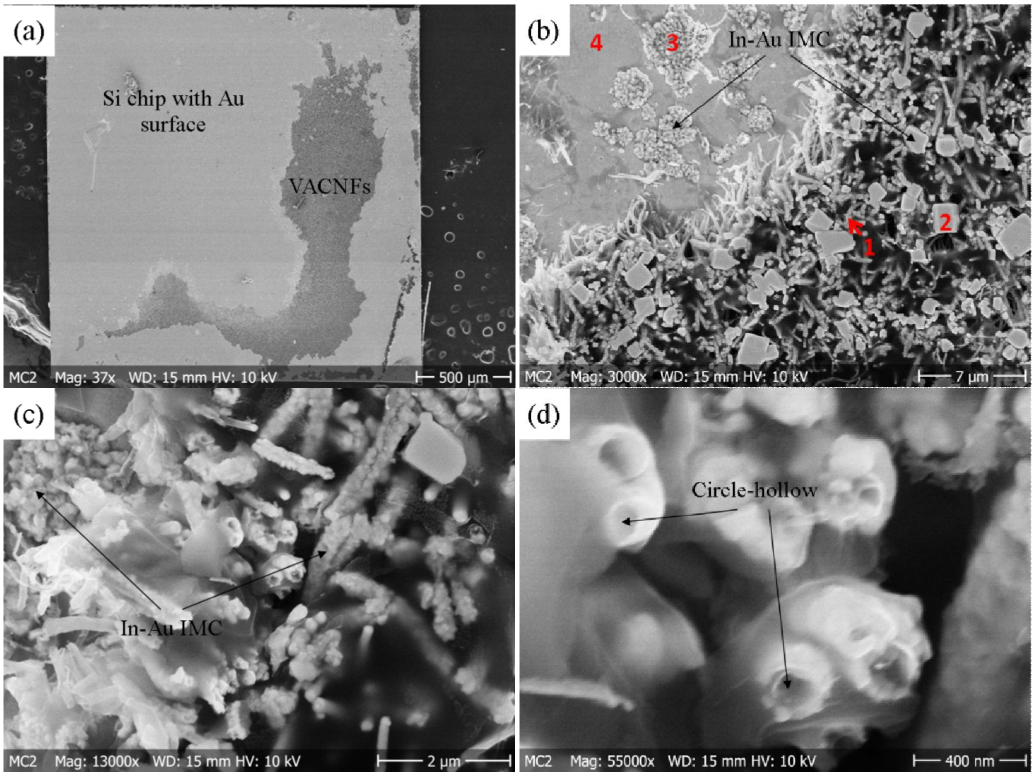
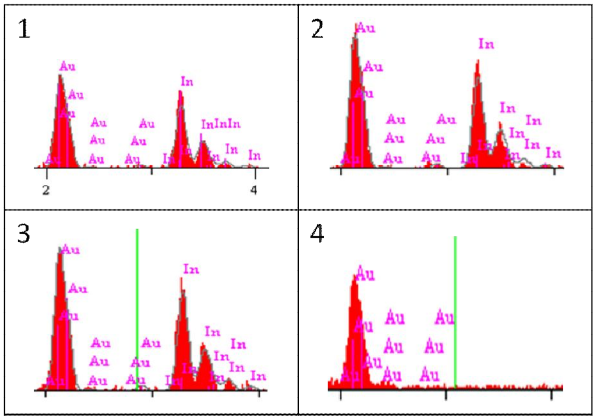


Figure 24. Chip side: (a) Fracture surface at the chip side, (b) Close-up view on the fracture surface, (c) Close-up view on the VACNFs area, (d) Circular-hollow structure on the cross-section of broken CNF.

Table 4. EDS analysis on the fracture surface at chip side based on Figure 24(b).



Point	In (at.%)	Au (at.%)
1	74	26
2	77	23
3	71	29
4	0	100

Figure 25(a) shows the fracture surface at substrate side. It exactly matches to the fracture surface at chip side. Figure 25(b) shows a close-up view on the boundary of dark and bright area. The bright area is VACNFs and the dark area is substrate surface with some small IMC pieces. Some broken CNF residues were found on these pieces. From the close-up view on these broken CNFs, showing in Figure 25(c), the CNFs have been covered by rough In-Au IMC. Figure 25(d) clearly shows the small cone on the cross-section of broken CNF. This conical structure is consistent with the circular-hollow structure at chip side, as shown in Figure 24(d). Combining the cross-sections of broken CNF at two sides, we can conclude the break surface of CNF is easy to be located at the interface between cones. This break structure in CNF was also observed by other researchers[74].

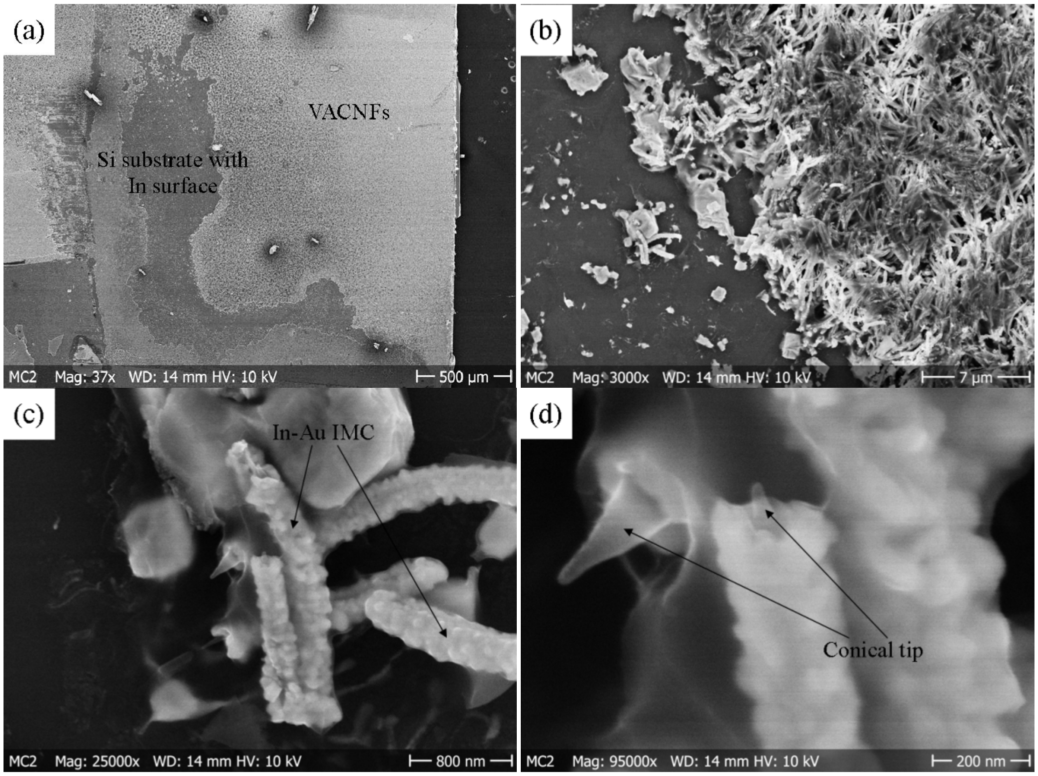


Figure 25. Substrate side: (a) Fracture surface at the substrate side, (b) Close-up view on the fracture surface, (c) Close-up view on broken carbon nanofiber, (d) Conical structure on the cross-section of broken CNF.

From DES results, the point 4 on the surface at chip side only shows Au peaks, without In. It implicates that the IMC layer is discontinuous or not uniform at the interface. The possible reason could be attributed to thin indium layer at the substrate side. During transfer process, the indium will wet the head of CNF as shown in Figure 26(a). A part of indium will be consumed to form In-Au IMC. After that, during the bonding process, indium will be further consumed and wet entire surface of CNF. Finally, the left indium will reach the other side (chip side) to form IMC layer, as shown in Figure 26(b). However, if the volume of indium is not enough, after bonding process, the left indium will be insufficient to form IMC layer with Au at the chip side, see Figure 26(c). In this case, discontinuous IMC layer will be presented at the interface. Therefore, increasing the thickness of indium layer could be a potential way to form continuous and uniform IMC layer at the interface and then improve the electrical and mechanical performance of VACNFs joint.

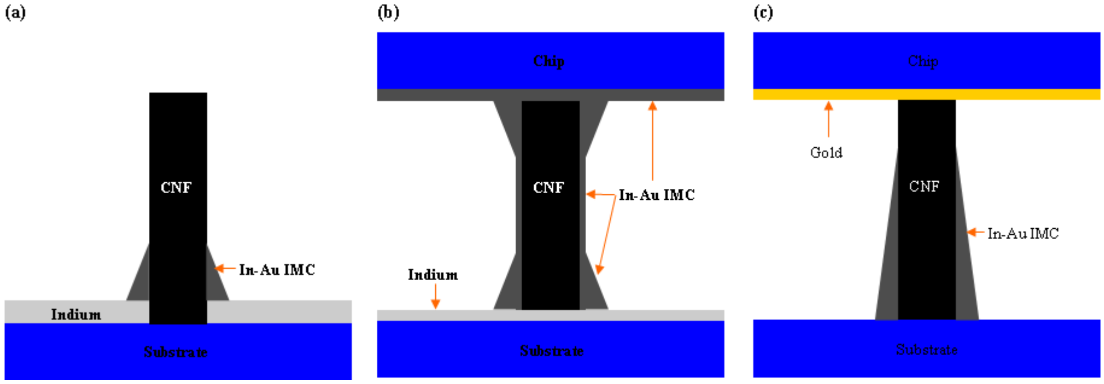


Figure 26. The status of IMC formation during transfer and bonding process: (a) IMC formation at the tip of CNF during transfer process, (b) IMC layer formation at the chip side if sufficient indium presents during bonding process, (c) No IMC formation at the chip side when there is not enough indium supply during the bonding process.

Chapter 5 Summary and outlook

In this thesis, we discussed two novel interconnect materials based on nanotechnology. One is Sn-3.0Ag-0.5Cu nanoparticles reinforced nanocomposite solder. The shear strength of Sn-58Bi increases twice with the addition of Sn-3.0Ag-0.5Cu nanoparticles. The results on thermal cycling test indicate that the thermal fatigue resistance of nanocomposite solder is much better than pure Sn-58Bi and comparable to Sn-3.0Ag-0.5Cu as long as the content of nanoparticles is lower than 2wt%. Besides the improvement on mechanical properties, presented nanocomposite solder also achieves about 60°C decreasing on process temperature. It can decrease thermal stress, defect as well as energy cost. However, the technologies and processes in this thesis are still in the lab level. If we wish to use this nanocomposite solder in the packaging industry, some additional research has to be done. One of the most important tasks is to update processes and equipments. The processes for producing alloyed nanoparticles in large scale must be developed and combined with the traditional production line. The equipment also must be updated to offer high yield to bring down the cost. Otherwise, the high cost of nanoparticles will offset the effort on energy saving.

Another interconnect material is VACNFs, which was fabricated by PECVD method. The common problems on nanostructured materials, such as dispersion and coating, can be solved because CNFs can stand on the surface of growth chip with uniform spacing. The problem on high growth temperature for VACNFs has also been addressed by an optimized transfer process. This transfer process achieved high successful rate in our experiment. The original structure of VACNFs wouldn't be changed after transfer process. From the results of electrical and shear test, the performance of VACNFs is acceptable if we take account of the advantages of VACNFs on stability and flexibility.

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