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Investigation and Design of Low Phase Noise and Wideband Microwave VCOs

Master's Thesis in Wireless and Photonics Engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

This thesis studied the design techniques of low phase noise and wideband microwave voltage controlled oscillators (VCOs) used for point-to-point radio applications. First, basic oscillator theories as well as different technologies were reviewed. Then two C-band MMIC VCOs were designed in a commercial InGaP HBT foundry process with different topologies, namely the balanced Colpitts and the balanced Clapp. The circuits were simulated with a commercial harmonic balance simulator and the designs were optimized for the best phase noise performance by studying the implication of various design parameters, such as tank quality factors, transistor current density, feedback capacitor ratio and etc. Simulation results show over 10% tuning range for both topologies and a phase noise of -122 dBc/Hz at 100 kHz offset for the balanced Clapp, 10 dB superior to that of the balanced Colpitts, owing to a higher current excitation.

Keywords: Voltage Controlled Oscillator, Microwave Monolithic Integrated Circuit, Heterojunction Bipolar Transistor, Phase Noise

Contents

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1. Introduction

Microwave technology has evolved enormously during the 20th century.It has been penetrating into many aspects of our society, e.g., microwave heating, wireless communication systems, military radars and instrumentation. Among the building blocks of a microwave system, the microwave source, or the frequency generation unit, is a vital one, since it provides a stable reference signal for the rest of the system.

Microwave sources used to be bulky and expensive in the early era of the microwave industry, examples are vacuum tubes in the 1940s and reflex klystrons in the 1970s[1]. Late 1970s witnessed more compact versions of microwave oscillator, e.g., Gunn diode and Si transistor hybrid oscillators. Today, thanks to the advancement in semiconductor technology, voltage controlled oscillators (VCOs) are available in the form of monolithic microwave integrated circuit (MMIC), and their sizes and costs have been reduced considerably while still offer excellent performance.

However, the evolution of microwave technology continuously demands higher quality microwave oscillators at lower cost. Taking the microwave backhaul network as an example[2], with the migration to the fourth generation (4G) mobile networks, the point-to-point microwave systems connecting the base stations and the core network are facing enormous challenges in terms of bandwidth efficiency. To this end, modulation scheme up to 1024QAM has been implemented[3]. However, as the modulation order increases, the effects of phase noise will be profound and the oscillator becomes the bottleneck that limits the performance of the system. The high order modulation, in turn, will pose stringent requirements to the oscillators. Meanwhile, the oscillators are always desired to be miniaturized to reduce the costs and possibly to be integrated with other parts of the transceiver.

The specifications of a VCO include oscillation frequency, phase noise, output power, tuning range, harmonic suppression and etc. Phase noise is defined as the ratio between the noise power at a certain offset frequency from the carrier and the carrier power. It is a critical parameter of a VCO for multi-channel communication systems where channels are densely allocated within a limited frequency band. The output power of a VCO should be large enough to drive the following circuits in the transceiver chain, e.g. the mixer. A buffer amplifier is usually utilized in the output stage of the VCO to boost the signal. VCOs are designed to be able to be tuned over a certain frequency band. Broadband VCOs can offer up to an octave tuning bandwidth. In many applications, both low phase noise and wide tuning range are desired. However, trade-offs must be

made between the two parameters. For a typical C-band VCO, used for the point-to-point radio link, over 10% tuning range is expected while the phase noise should be as low as -120 dBc/Hz for the entire frequency band.

This Thesis aims to study design techniques of low phase noise wideband MMIC VCOs intended for microwave point-to-point radio link applications and understand phase noise mechanism and how to make accurate phase noise prediction. Main objectives include literature review on microwave oscillator technologies and topologies, design MMIC VCOs with a commercial foundry process and optimize for the best phase noise performance.

The study will not cover certain technologies such as MEMS. Agilent ADS and a commercial InGaP HBT process are chosen by default when designing the VCOs since they have long been the solution within the company and foundry service is readily accessible as well.

The rest of the thesis is organized as follows. Chapter 2 presents oscillator background including technology, topology, phase noise mechanism, computer simulation, and etc. In Chapter 3, two MMIC VCOs are simulated and optimized for phase noise performance. Chapter 4 summarizes the findings. Finally, Chapter 5 offers some recommendations for the future work.

2. Oscillator Background

2.1. Basics of Oscillating System

A microwave oscillator can be viewed as a feedback circuit, which consists of an active device and a resonator, as shown in Figure 2.1. The active device is essentially an amplifier which amplifies the incoming signal, with its output feed to the input of the resonator, which is further connected to the input of the amplifier and forms a feedback loop. To start oscillation, the loop gain should be larger than unity as well as the loop phase shift should be 0° or a multiple of 360°. The loop gain requirement specifies that the amplifier should at least provide a gain to compensate the loss of the resonator, while the loop phase condition guarantee the feedback signal to add constructively to the original signal [4].

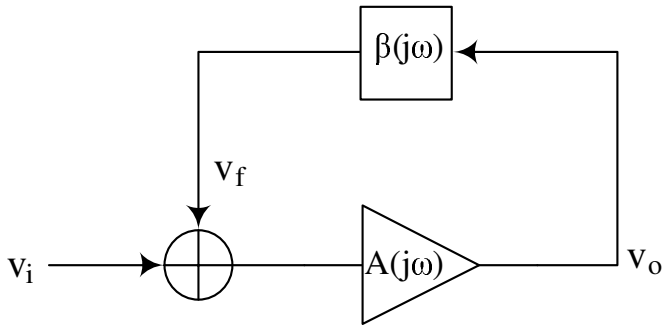


Figure 2.1. Oscillator as a feedback system

Another view of microwave oscillators is the so-called negative resistance concept. The active device generates a negative input resistance which compensates the losses from the resonator tank.

Both the active device and the resonator can be implemented with various types of components. Typical active devices are two terminal diodes, Gunn diode or IMPATT diode, and three terminal transistors, either a bipolar junction transistor (BJT) or a field effect transistor (FET). The resonator is normally realized by a LC network, a dielectric resonator, or an yttrium iron garnet (YIG).

2.2. Resonator Technology

Metallic cavity resonators have historically been the choice for filter and low phase noise oscillator applications, due to their extremely high Q factor. Typical phase noise performance of metallic cavity oscillators can be as low as -180 dBc/Hz at 10 kHz offset for a 10 GHz carrier [5]. However, their bulky size limits them from the most performance critical applications.

Dielectric resonators are based on low loss, temperature stable, high permittivity and high Q ceramic materials with normally a cylindrical shape. They resonate in various modes while the dominate $TE_{01\delta}$ mode is utilized for temperature stability and Q factor optimization reasons. Owing to the high permittivity of dielectric materials, their size can be made much smaller than that of a metallic cavity resonator resonating at the same frequency. Moreover, their miniaturized size allows them to be implemented in a planar hybrid MIC technology. Dielectric resonator oscillators (DROs) are usually housed in a metal enclosure to minimize radiation losses; thereby preventing unwanted Q degradation. The oscillation frequency of a DRO can be tuned either electrically or mechanically. A varactor tuned DRO shows a typical tuning range up to 1% while with a tuning screw the oscillation frequency can be tuned up 5%. An issue of DROs is their sensitivity to microphonic. Unwanted vibrations can cause more than 20 dB deterioration in phase noise [6]. A commercially available DRO [7] shows a phase noise of -122 dBc/Hz at 10 kHz offset and a tuning range from 8 to 8.3 GHz.

Surface acoustic wave (SAW) resonators enable the design of low noise and temperature stable oscillators up to 2 GHz. Their structure consists of an interdigital transducer (IDT) and two reflectors fabricated on a piezoelectric material. The IDT converts acoustic wave to electrical signal. SAW oscillators have been extensively used as very low noise sources in wired applications such as optical communications, Gigabit Ethernet communications, and storage circuits. A 500 MHz SAW resonator with low noise amplifier, showing -140 dBc/Hz phase noise at 10 kHz [8], was used to build an 8 GHz SAW oscillator using frequency multiplication technique.

Bulk acoustic wave (BAW) resonators, also known as film bulk acoustic resonators (FBAR), are a recent introduction to build fixed frequency oscillators. They are normally used in the frequency range between 500 MHz and 5 GHz. Typical phase noise performance of FBAR oscillator is -112dBc/Hz at 10 kHz at 2 GHz carrier [9]. Major foundries are still working hard to bring the FBAR process into mass production.

The most straightforward way to build a resonator is to combine an inductor and a capacitor, i.e. a LC resonator, either in series or in parallel. LC resonators have long been the choice for low frequency oscillators and as the evolution of RFIC/MMIC technology they not long restrict themselves at the low end of the spectrum. Spiral inductors and MIM capacitors are supported by essentially every foundry process while at microwave frequencies transmission lines are sometimes employed to represent high Q inductors.

VCOs can be built by introducing varactor diodes to the LC resonators. It is possible to design fully integrated VCOs with LC resonators. The phase noise of an X-band MMIC LC VCO can be as low as -110 dBc/Hz at 100 kHz offset and the tuning range can be more than 10% [10].

YIG-tuned oscillators (YTO) are widely used in test instruments and military systems requiring octave tuning bandwidth. By using an YTO, low phase noise and wide tuning range can be satisfied simultaneously. The core of the resonator is an yttrium iron garnet ($Y_3Fe_5O_3$) spherical placed between two poles of a cylindrically re-entrant electromagnet. The resonant frequency is controlled by the applied magnetic field strength. YTOs offer a very high Q, around 4000 at 10 GHz. The YTO can operate at frequency up to 50 GHz. Typical YTO shows a tuning range of 3 to 11 GHz and phase noise of -128 dBc/Hz at 100 kHz[11].

2.3. Active Device Technology

The active device generates negative resistance in an oscillator and can be either a two-terminal diode or a three-terminal transistor [1].

2.3.1. Two-terminal diodes

The Gunn diode is named after J. B. Gunn who discovered the Gunn Effect in 1962. It is also known as Transferred Electron Device (TED). Only semiconductor materials with a satellite valley in the conduction band can be made into Gunn diode, such as GaAs and InP. Negative resistance is observed in a region when the electrons transfer from conduction band to the low mobility satellite valley. Despite their relatively low efficiency, normally in the order of 2 to 3 percent, Gunn oscillators can deliver low noise and high power at frequencies up to 100 GHz.

IMPact Ionization Avalanche Transit Time (IMPATT) diodes can offer even greater power than Gunn oscillators with a frequency capability beyond 100 GHz. Moreover, they are more efficient, with a typical efficiency from 10 to 20 percent. However, they show a roughly 10 dB worse performance in terms of phase noise compared to their Gunn counterparts.

2.3.2. Three-terminal transistors

Three-terminal transistors emerged in the RF and microwave generation field in the late 1970s and since then they had been replacing diodes in many applications due to their low cost and high integrability.

Semiconductor transistors can be classified into two categories, i.e, field effect transistors (FETs) and bipolar transistors. The former group comprises mainly metal-oxide-

semiconductor field effect transistors (MOSFETs), metal semiconductor field effect transistors (MESFETs), and High electron mobility transistors (HEMTs) of different materials; while the latter includes Si bipolar junction transistors (BJTs) and heterojunction bipolar junction transistors (HBTs) of different materials.

CMOS technology has long found its applications in digital and analog integrated circuits owing to the low cost silicon process and dense integration. With the continuous scaling of MOSFETs, the RF performance of the Si MOSFETs has been improved considerably and research shows that the state-of-the-art Si RF MOSFETs can have f_T and f_{max} exceeding 300 GHz [12] . In the consumer electronics market today, essentially all products operating in the lower GHz frequencies are based on CMOS technology. With mixed-signal design techniques, RF function is integrated with digital processing and power management units, occupying only a small corner of the entire chip.

As far as VCO applications are concerned, although their notorious high flicker noise corner frequency and low breakdown voltage constrain their appearance in the phase noise critical applications, RF MOSFET can still offer moderate performance given careful design and optimization.

GaAs and InP HEMTs can offer excellent performances in applications such as low noise amplifiers, power amplifiers, and switches up to several hundred GHz. They are, however, seemingly not the best candidate for phase noise critical oscillator applications due to their inherently high 1/f corner frequencies. In spite of this, their superior high frequency performances make it possible to design fundamental oscillators beyond 100 GHz. In addition, GaN HEMT based oscillators can deliver much higher output power, eliminating the need for buffer amplifiers.

Si BJTs are the devices of choice for low phase noise VCO applications at lower GHz frequencies , owing to their low 1/f noise characteristic. They are mainly available in the form of discrete devices and therefore used to design hybrid VCOs together with various resonator technologies.

HBTs differ from conventional BJTs in the use of hetero structure in the base-emitter or/and the base/collector junctions. They maintain the merit of low flicker noise corner frequency as their predecessors while exhibit a much higher f_T and f_{max}, which makes them attractive devices for microwave oscillator applications.

There are, essentially, two categories of HBTs: Si based HBTs and III-V compound HBTs. The former one comprises mainly SiGe/Si HBTs and the latter one can be classified into GaAs and InP HBT depending on the base materials being employed. These technologies can be found in various applications depending on their specific properties, e.g. SiGe HBTs are the best candidate for W-band automotive radar applications due to their high frequency capability and for C-band to X-band MMIC VCO applications, where phase noise is the most critical parameter, InGaP/GaAs based HBTs are dominating due to their high breakdown voltages and superior reliability.

2.4. Oscillator Topologies

Oscillators can have various topologies. Depending on the operation frequency, an oscillator can be built by lumped elements or distribute elements.

At the low end of the microwave frequency range, oscillators are usually implemented by lumped components and based on feedback theory. Common topologies include Colpitts, Hartley, Clapp, and cross-coupled. Taking BJT based oscillators as examples, the schematics of Colpitts, Hartley, and Clapp oscillator are shown in Figure 2.2 [13]. These topologies share the same properties that the elements connected between the emitter-base and emitter-collector terminals have the same signs in terms of reactance while that between the base-collector terminals is the opposite. The choice between the Colpitts and Hartley oscillators is determined by the operating frequency. For relatively low frequency applications, the Colpitts topology is preferred since inductors tend to be large and present low quality factor, so their number should be minimized. However when it comes to high frequency applications, the Q limiting element turns to the capacitor as the inductor Q increases with frequency; therefore Hartley solution seems more efficient. The Clapp topology resembles the Colpitts except that it uses a series LC network at the base-collector terminals and the extra tapping capacitor can further increase the tank swing while keeping the transistor below breakdown. The Colpitts oscillator and its variants are favored for low phase noise applications since the noise current is injected at peaks of the output signal, where the circuit is least sensitive to noise perturbations [14].

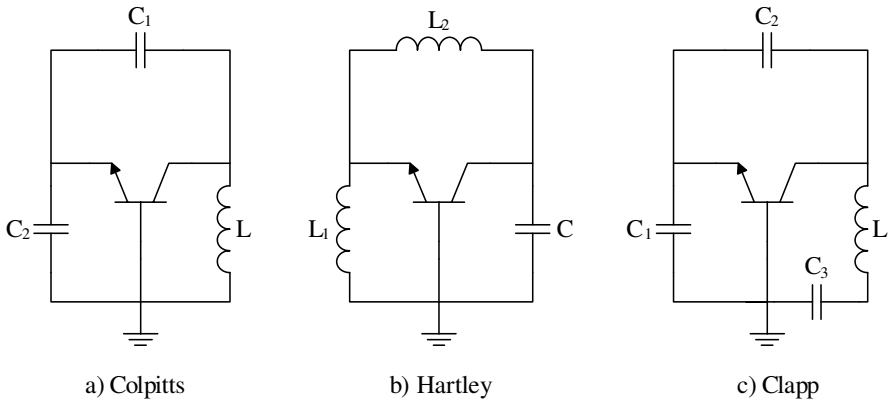


Figure 2.2. The Colpitts oscillator and its variants

The cross coupled topology consists of two transistors providing 360° phase shift for the oscillation condition. It is also known as negative-gm oscillator since the impedance looking into the cross-coupled pair is $-2/g_m$, which compensates for the loss of the tank. The schematic of a cross coupled oscillator is shown in Figure 2.3 [15]. This

topology benefits for relaxed start-up condition and is ubiquitously used in the design of CMOS RFICs.

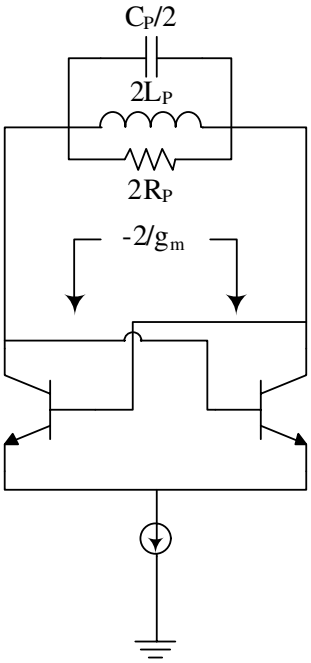


Figure 2.3. The cross-coupled oscillator

When the frequency continues to increase, the negative resistance method is preferred when designing oscillators. For this method, the transistor is viewed as a two-port network and the S-parameter data is obtained. By using a proper terminating network, the transistor enters unstable regions for the desired frequencies, showing a negative resistance at the input. A load network is designed to cancel the reactive part of the input impedance, insuring the circuit oscillates at the desired frequency. A typical negative resistance oscillator with BJT is illustrated in Figure 2.4. As can be seen, it utilized a common base configuration with an inductive feedback at the base terminal. This inductor is used to boost $|\Gamma_{in}|$ and $|\Gamma_{out}|$ [13].

The topologies discussed above are mostly single-ended solutions, and only fundamental output frequency is available. In practical, a balanced configuration is often used in MMIC oscillator design. A push-push structure consists of two symmetric oscillators and can provide output frequency twice of that of the single oscillator, which extend the usable frequency range for a given transistor technology. Another advantage of the push-push configuration is that it can reduce the phase noise by 3 dB.

The theory of push-push operation is illustrated in Figure 2.5 [16]. As can be seen, the two unit oscillators can operate in both odd mode and even mode. However, for

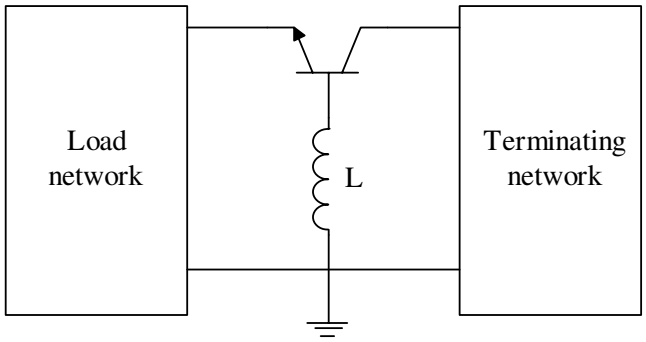


Figure 2.4. The common-base negative resistance configuration

the push-push operation, only the odd mode is desired, which means that the two sub oscillators are oscillating out of phase and a virtual ground is formed in the symmetry plane. The oscillation condition can be written as [16],

$$Re\,(Z_{in}) + R_V < 0 \tag{2.1}$$

$$Re\,(Z_{in}) + R_V + 2R_L > 0 \tag{2.2}$$

2.5. Voltage Controlled Oscillators (VCOs)

In most applications, the oscillators are desired to be tuned electronically over a certain frequency range. The conceptual diagram and the tuning characteristic are shown in Figure 2.6 [15]. The slope of the frequency tuning curve is called the tuning sensitivity and is given by,

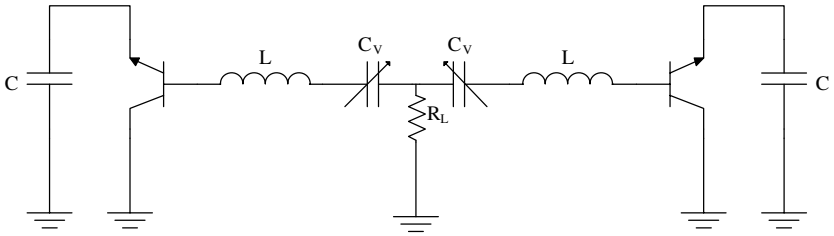
$$K_{VCO} = d\omega_{out}/dV_{cont} \tag{2.3}$$

To design a VCO, either the inductor or the capacitor in the tank of the fixed frequency oscillator can be replaced by a tunable element. Tunable inductors, however, are implemented using active devices and exhibit excess noise. Therefore, most VCOs utilize tunable capacitors, or varactors, in the tank.

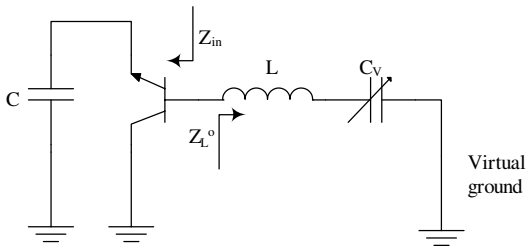
A varactor can be either a p-n junction varactor or a MOS varactor, depending on the technology. For a p-n junction varactor, the diode is operating at reverse bias condition and the junction depletion capacitance is controlled by the tuning voltage. A varactor equivalent circuit is shown in Figure 2.7 [16].

Where C_V is the variable capacitor, R_S is the series resistor, and L_S is the series parasitic inductor [16].

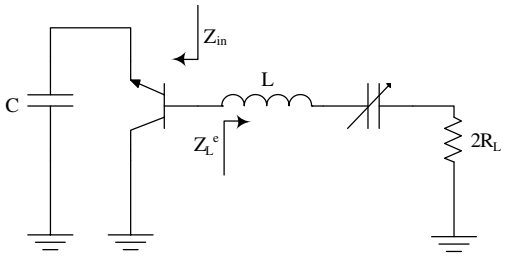
Three main parameters of a varactor are most concerned by VCO designers. They are the reverse breakdown voltage, the capacitance ratio, and the quality factor.



a) A simplified push-push oscillator



b) Odd mode equivalent circuit



c) Even mode equivalent circuit

Figure 2.5. The push-push topology

The reverse breakdown voltage defines the maximum applied tuning voltage and is determined by the technology used and the doping concentration of the junctions.

The capacitance at a given bias voltage is given by [16],

$$C_V\left(V_V\right) = C_{V0}\left(1 + \frac{V_V}{\varphi}\right)^{-\gamma} \tag{2.4}$$

Where C_{V0} is the zero bias junction capacitance, φ is the contact potential (1.3V for GaAs) , and γ is the varactor junction sensitivity which is related to the doping profile. For different γ values, a varactor can be classified as abrupt $(\gamma = 0.5)$ and hyperabrupt $(1 < \gamma < 2)$. The doping concentrations for an abrupt junction and a hyperabrupt junction are plotted in Figure 2.8 [16]. As can be seen, the abrupt varactor has a uniform doping profile in the active region while in the hyperabrupt varactor the active region is nonlinearly doped.

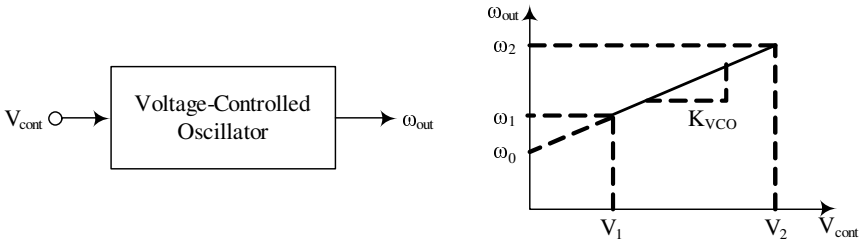


Figure 2.6. VCO characteristic

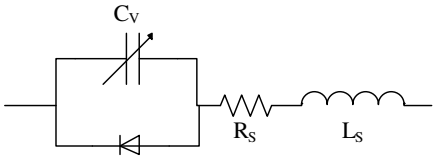


Figure 2.7. Varactor equivalent circuit

The capacitance ratio between the minimum and maximum tuning voltages limits the maximum tuning range of a VCO. It can be shown this ratio is also related to γ, and a hyperabrupt varactor can provide a wider tuning bandwidth.

The quality factor of a varactor is given by [16] ,

$$Q(V_V) = \frac{1}{2\pi f R_S C_V(V_V)} \tag{2.5}$$

The quality factor is inverse proportional to the frequency and is also a function of bias voltage. Most venders provide the quality factor data at 50 MHz for historical reasons, and one can readily extrapolate it to another frequency.

A typical plot of quality factors for the abrupt and hyperabrupt varactors is shown in Figure 2.9 [16]. As can be seen, the hyperabrupt varactor presents a higher Q_V at high reverse voltages and a lower Q_V at low reverse voltages. This is due to the fact that at high voltages, the capacitance of a hyperabrupt varactor decreases more rapidly than that of an abrupt varactor.

The quality factor of the varactor is the most critical parameter for low phase noise VCOs. It is normally much lower comparing with other elements in the resonator circuit and therefore limits the overall tank quality factor.

2.6. Small Signal Loop Gain Analysis

Oscillator small signal loop gain condition can be derived from either the feedback or the negative resistance point of view, and both methods should give the same result.

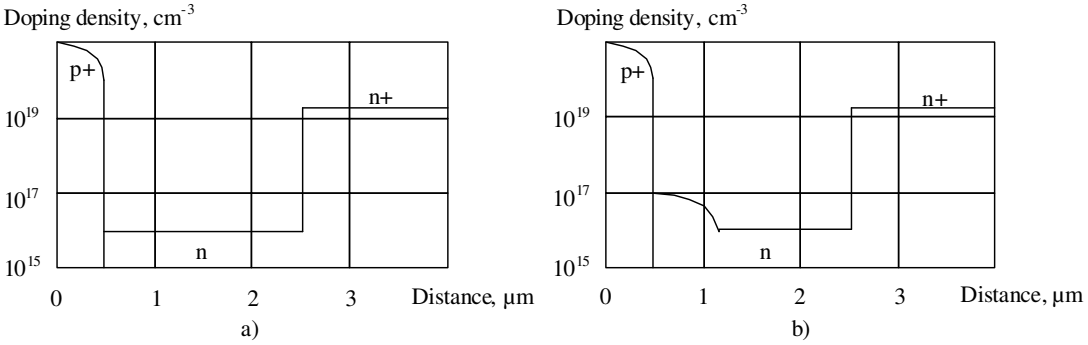


Figure 2.8. Doping profile of a) abrupt junction and b) hyperabrupt junction

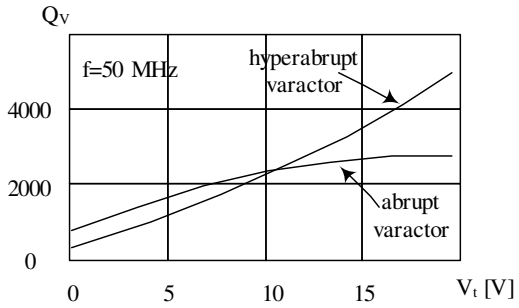


Figure 2.9. Quality factor versus bias voltage for abrupt and hyperabrupt varactors

Here the start-up condition of a single-ended Clapp oscillator is analyzed, using the negative resistance concept. Similar result can be obtained for a Colpitts oscillator.

The circuit of a single-ended Clapp oscillator and its equivanlent circuit are shown in Figure 2.10. We consider the tank to be the series combinition of L and C_3, with the feedback capacitors C_1 and C_2 being included in the active device.

The input impedance looking into the active device can be derived as follows,

$$V_{in} = V_{be} + V_e \tag{2.6}$$

$$V_{be} = \frac{I_{in}}{j\omega C_1} \tag{2.7}$$

$$V_e = \frac{I_{in} + g_m V_{be}}{j\omega C_2} = \frac{I_{in} + g_m \dfrac{I_{in}}{j\omega C_1}}{j\omega C_2} \tag{2.8}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = -\frac{g_m}{\omega^2 C_1 C_2} - j\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2}\right) \tag{2.9}$$

Where V_{be} is the base-emitter voltage and V_e is the emitter voltage.

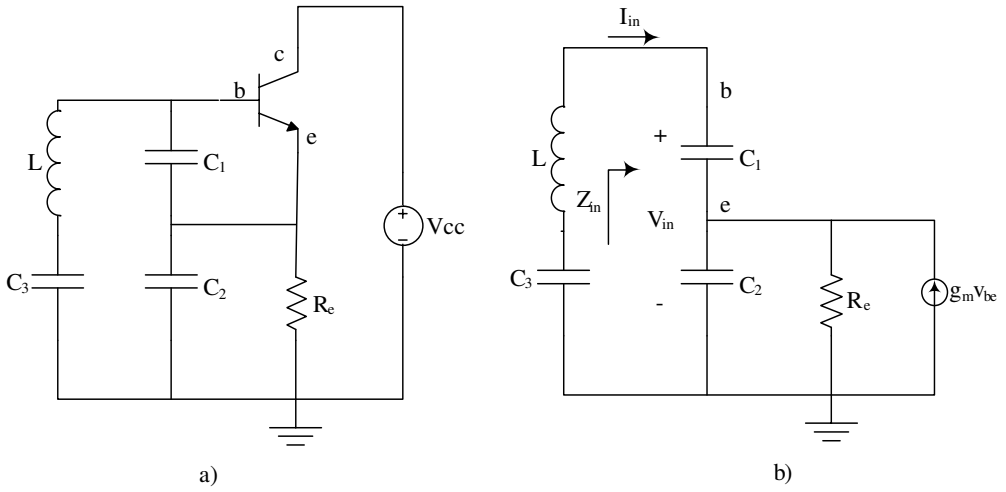


Figure 2.10. The schematics of a) single-ended Clapp oscillator and b) its equivalent circuit

The impedance of the series LC tank is given by,

$$Z_t = R_s + j\left(\omega L - \frac{1}{\omega C_3}\right) \tag{2.10}$$

where Rs accounts for the loss in the tank.

Oscillation will start when the following two conditions are met:

$$R_s < |-\frac{g_m}{\omega^2 C_1 C_2}| \tag{2.11}$$

$$-\left(\frac{1}{\omega C_1 \omega C_2}\right) + \left(\omega L - \frac{1}{\omega C_3}\right) = 0 \tag{2.12}$$

Thus the oscillation frequency can be given by,

$$\omega_{osc} = \frac{1}{\sqrt{LC_{tot}}} \tag{2.13}$$

Where $C_{tot} = 1/(1/C_1 + 1/C_2 + 1/C_3)$.

A Clapp VCO can be constructed by replacing C_3 with a varactor C_V. Normally C_V is chosen to be much smaller than C_1 and C_2. the C_f can be replaced by a tuned varactor C_V. The tuning range can be express as,

$$TR = 2 \cdot \frac{\omega_{osc,high} - \omega_{osc,low}}{\omega_{osc,high} + \omega_{osc,low}} = 2 \cdot \frac{\frac{1}{\sqrt{LC_V(1)}} - \frac{1}{\sqrt{LC_V(0)}}}{\frac{1}{\sqrt{LC_V(1)}} + \frac{1}{\sqrt{LC_V(0)}}} = 2 \cdot \frac{\sqrt{C_V(0)/C_V(1)} - 1}{\sqrt{C_V(0)/C_V(1)} + 1} \tag{2.14}$$

which is largely dependent on C_V.

2.7. Large Signal Analysis

The previous small signal analysis can only guarantee the oscillation to start. As the oscillation amplitude increases, the negative resistance generated by the active device will decrease. The negative resistance will ultimately equal to the tank loss, and the circuit enters steady state. As in the steady state the transistor is usually operating in non-linear regions, traditional linear analysis techniques could not predict the signal amplitude as well as the oscillation frequency and CAD software with harmonic balance simulators need to be employed. An analytical method based on describing function to calculate the final signal amplitude is presented in [4], and is described here briefly.

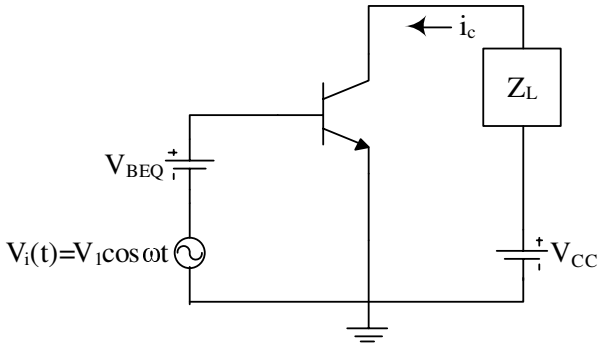


Figure 2.11. Large-signal analysis of a BJT

Consider a BJT under large-signal conditions, as is shown in Figure 2.11 [4], the base-emitter voltage can be represented by a sinusoid signal added on the DC bias voltage,

$$v_{BE} = V_{BEQ} + V_1 \cos \omega t \tag{2.15}$$

And the collector current can be expressed as,

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{V_{BEQ}/V_T} e^{x \cos \omega t} = I_{CQ} e^{x \cos \omega t} \tag{2.16}$$

Where $V_T = kT/q$ is the thermal voltage, I_S is the saturation current, $x(= V_1/V_T)$ represents the signal amplitude.

For large-signals, $e^{x\cos\omega t}$ can be expanded in Fourier series,

$$e^{x\cos\omega t} = I_0(x) + 2\sum_{n=1}^{\infty} I_n(x)\cos n\omega t \tag{2.17}$$

Where $I_n(x)(n = 0, 1, \ldots,)$ are the modified Bessel functions of the first kind. Therefore the fundamental component of i_C is given by $2I_{CQ}I_1(x)\cos\omega t$. The large-signal transconductance $G_m(x)$ is defined as the ratio between the fundamental component of i_C and the voltage V_1, and is given as,

$$G_m(x) = \frac{2I_{CQ}I_1(x)}{V_1} = \frac{2I_{C,dc}I_1(x)}{V_T x I_0(x)} = g_m\frac{2I_1(x)}{xI_0(x)} \tag{2.18}$$

where g_m is the small-signal transconductance.

For large drive level, $G_m(x) \approx 2g_m$, so the fundamental frequency component of the collector current can be approximated by twice the collector DC current.

2.8. Phase Noise Basics

2.8.1. Noise sources

The noise sources in an oscillator system can be classified into three main types: thermal noise, shot noise and flicker noise. They are caused by different mechanisms and are described as follows.

Thermal noise is caused by the random thermal motion of the charge carriers, and can be always found in any conductor or semiconductor device at temperature above absolute zero [16]. It is also known as white noise since its value is independent of frequency. The thermal noise associated with a resistor can be represented by a series voltage source or a parallel current source. In the case of current source, the mean square value of noise current can be written as,

$$\left\langle i_n^2 \right\rangle = 4kT\Delta f/R \tag{2.19}$$

Where k is the Boltzmann constant and equals $1.38 \times 10^{-23} J/K$, T is the temperature in Kelvin, and Δf is the bandwidth in Hz.

Shot noise is originated from the discrete nature of charge carriers that constitute the current flow. In a forward biased p-n junction, the potential barrier can be overcome by the carriers with higher thermal energy. The mean square shot noise current is given by,

$$\langle i_n^2 \rangle = 2qI\Delta f \tag{2.20}$$

where q is the electron charge.

Flicker noise, also called 1/f noise, is a low frequency noise with power spectral density proportional to $f^{-\gamma}$, with γ being close to unity. The mechanism and origin of flicker noise are complicated and it is generally believed that the flicker noise is caused by surface effect of semiconductor materials. The mean square flicker noise current can be expressed as,

$$\langle i_n^2 \rangle = KF \times I^{AF} \frac{\Delta f}{f^{-\gamma}} \tag{2.21}$$

where KF is the flicker noise coefficient, AF is the flicker noise exponent, and I is the DC current. Both KF and AF are device dependent and can be extracted by measurement.

2.8.2. Transistor noise modeling

The challenge in accurate phase noise prediction, especially close-in phase noise, lies in two major aspects: the modeling of the noise sources in the active device, as well as the way in which harmonic balance simulator treats the cyclostationary noise sources.

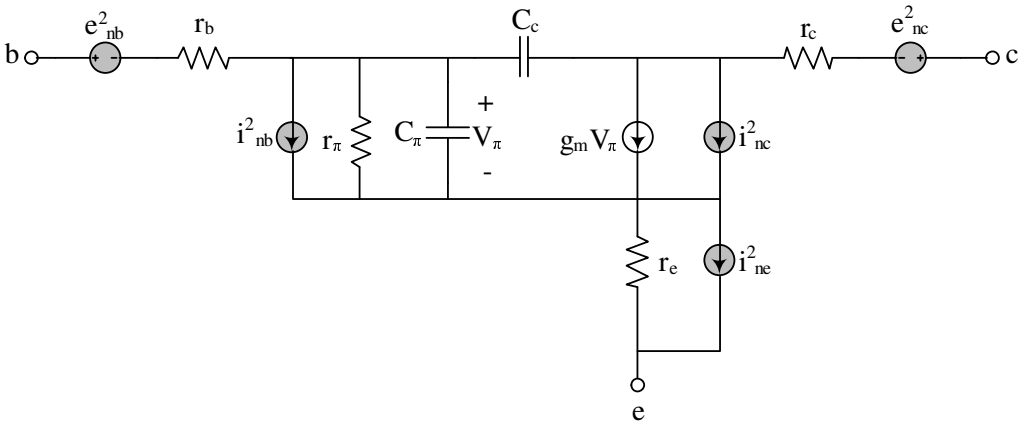


Figure 2.12. HBT model with noise sources

The HBT equivalent circuit with noise sources is shown in Figure 2.12. As can be seen, it consists of three voltage sources representing the thermal noise associated with resistances of the terminals, two current sources representing shot noise from the base-emitter and collector-base junctions respectively. Flicker noise is represented by a current source across the base-emitter junction and is combined with the base shot noise. The mean square values of the voltage and current sources can be given as follows [16],

$$\left\langle e_{nb}^2 \right\rangle = 4kTR_b\Delta f \tag{2.22}$$
$$\left\langle e_{nc}^2 \right\rangle = 4kTR_c\Delta f \tag{2.23}$$
$$\left\langle e_{ne}^2 \right\rangle = 4kTR_e\Delta f \tag{2.24}$$
$$\left\langle i_{nb}^2 \right\rangle = 2qI_b\Delta f + KF \times I_b^{AF}\frac{\Delta f}{f} \tag{2.25}$$
$$\left\langle i_{nc}^2 \right\rangle = 2qI_c\Delta f \tag{2.26}$$

2.8.3. Phase noise modeling

Ideally, the spectrum of an oscillator output shows only one component at the carrier frequency. However, in the real world, phase noise and harmonics can also be observed. The phase noise of an oscillator is a measure of the signal purity and is defined as the ratio between the noise power at offset frequency $\Delta\omega$ and the carrier power. The phase noise is often characterized in 1 Hz bandwidth and expressed in decibel, in other words, it has a unit of dBc/Hz.

There are numerous models analytically expressing the phase noise of an oscillator, among which the Leeson's model and the Lee and Hajimiri's model are most used. The former model is based on linear time invariant (LTI) assumption while the latter assumes a linear time variant (LTV) system.

The renowned Leeson's formula was initially introduced by D.B Leeson in 1966 and can be written as [17],

$$L\left(\Delta\omega\right) = 10 \cdot \log\{\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_c}{|\Delta\omega|}\right)\} \tag{2.27}$$

where F is the device effective noise factor, Ps is the oscillation signal power, ω_0 is the oscillation frequency, Q_L is the tank loaded Q, $\Delta\omega$ is the offset frequency from carrier where phase noise is measured, $\Delta\omega_c$ is the corner frequency between the $1/f^2$ and $1/f^3$ slope region. The typical phase noise spectrum based on Leeson's formula can be seen in Figure 2.13.

Leeson's equation is empirical and thus has certain limitations, for example the factor F is a fitting parameter and has no analytical expression. In spite of that, it gives insights into design techniques to minimize the phase noise in most oscillator applications. These include:

1. Maximize the quality factor of the resonator tank.
2. Maximize the voltage swing in the resonator tank but avoid reaching the saturation region and the breakdown voltage.

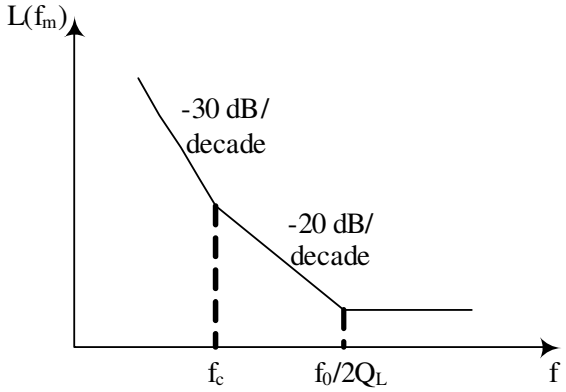


Figure 2.13. Phase noise spectrum from Leeson's equation

3. Choose a transistor with the lowest possible flicker noise corner frequency.

The more recent Lee and Hajimiri's model introduced the concept of impulse sensitivity function (ISF) which encodes information about the sensitivity of the oscillator to an impulse injected at a certain phase. The maximum value of the ISF appears near the zero crossing of the oscillation. The ISF is denoted by $\Gamma(\omega_0\tau)$ and can be expressed as,

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau) \tag{2.28}$$

The phase noise in the 20 dB slope region is given by,

$$L(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right) \tag{2.29}$$

While in the 30 dB slope region, it can be written as,

$$L(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q_{max}^2\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.30}$$

In addition to maximizing tank voltage swing and quality factor, Lee and Hajimiris theory gives other measures to minimize oscillator phase noise. Since the noise is injected into the tank when the transistor is conducting, narrower collector current pulse tends to give better phase noise performance. Colpitts topology and its variants with high drive level have been proved to have to this property and are favorable in low phase noise applications.

2.9. CAD Simulation

The most efficient way to design an MMIC VCO is by introducing commercial CAD software. Today most CAD tools are packaged with common simulators as well as EM solvers which can facilitate the design work to a great extent. Among them Advanced Design System (ADS) from Agilent EEsof and Microwave Office from AWR are most widely used. Essentially every foundry offers process design kit (PDK) and continuous update for these two platforms. In this thesis, ADS2009U1 with a commercial InGaP HBT PDK is employed.

Transient simulator and harmonic balance (HB) simulator are two general-purpose simulators to determine the oscillator steady state solutions. Transient simulator, however, is seldom used especially in complex RF and microwave oscillators with multiple transistors and distributed transmission line elements, since it takes considerably longer time to reach steady state. The HB simulator, on the other hand, is more suitable for these applications. During the HB simulation, the circuit is divided into a linear sub-circuit and a nonlinear sub-circuit, with the same number of ports. The steady-state solution is represented by sinusoidal signal and its harmonics with initial guess. The linear sub-circuit is solved in frequency domain while the nonlinear sub-circuit is modeled and solved in time domain by means of ordinary differential equations (ODEs). The time domain solutions are then Fourier transformed into frequency domain. An error function is given by the sum of the current flowing into the linear sub-circuit and the nonlinear sub-circuit. The error function is checked for each harmonics and the above procedures are iterated until the error function values are within a predefined threshold for each harmonic frequencies. [18]

Oscillator phase noise is simulated by small signal mixing of all noise sources through the transistors nonlinearity characteristic, and therefore the accuracy of phase noise prediction is largely dependent on the modeling of transistor noise sources. However, the HB simulator tends to underestimate phase noise especially for the close-in case even with an accurate noise model. This is due to the flicker noise source in the transistor is cyclostationary under large signal operation, while in commercial CAD tools, e.g., ADS, it is modeled by a current controlled noise source which is only controlled by the DC bias current. In order to make accurate phase noise predictions, the transistor noise sources need to be modified to exhibit cyclostationary characteristic, this can be implemented by using Symbolically Defined Devices (SDDs) in ADS [19] [20].

3. MMIC VCO Design

3.1. Design Specifications

The MMIC VCOs designed in this thesis are intended to be employed in the Mini-Link point-to-point radio links. The major specifications are:

- Center frequency: around 5 GHz (fundamental frequency)
- Second harmonic frequency output: yes
- Relative tuning bandwidth: larger than 10%
- Phase noise: below -110 dBc/Hz at 100 kHz offset frequency for all tuning voltages

Since designing a buffer amplifier is out of the scope of this thesis, there is no specific requirement for the output power but it should still be reasonable. According to [17], the phase noise is inverse proportional to the oscillator signal power and therefore trade-offs need to be made between the phase noise and the power consumption. In this thesis, there is no limitation in terms of power consumption since for the intended application phase noise is more critical and should be given higher priority.

3.2. Design Strategies

Microwave oscillator design has historically been a black magic and still remains a hot topic today. Taking certain strategies when designing an MMIC VCO is of great importance, since tuning is virtually impossible for MMICs after fabrication thus any careless design will result the final circuit not to meet the specifications. Conventional design procedures for hybrid MIC VCOs therefore cannot be applied directly to the monolithic case. In [21], a systematic design approach incorporating dynamic load line wave forming technique was proposed, and it was proved to be very effective for MMIC VCO design aiming for ultra low phase noise, in both HEMT and HBT technologies. The detailed design procedures followed in this thesis are described as follows.

1. Technology selection

Parameter	Value
V_{be}	1.15V
f_t	38GHz
β	115
Breakdown($BV_{cbo,beo,ceo}$)	18,6.5,10V
I_{max}	81mA
Interconnect	3 Metal Layers
NiCr Resistors	50 Ω/sq
MIM Capacitance per Area	0.625 $fF/\mu m^2$

Table 3.1. Process Key Parameters

The process used in this thesis is a commercial InGaP/GaAs HBT. Figure 3.1 shows a generic HBT cross-section [22].

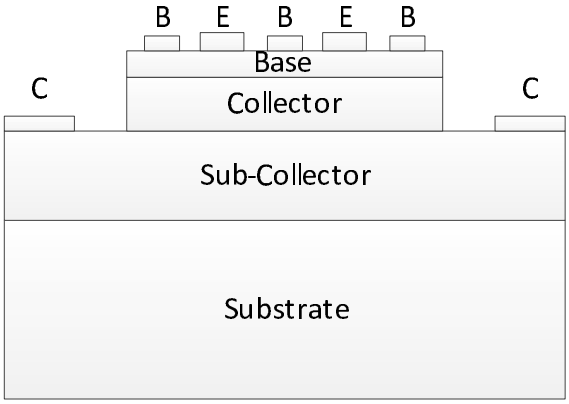


Figure 3.1. Cross-section of a generic InGaP HBT process

Table 3.1 summarizes the key parameters of the commercial foundry process for a $3 \times 3 \times 45\mu m$ Standard Cell. This process has a hyperabrupt BC junction doping profile which exhibits an inverse quadratic C-V curve for the varactor diode and therefore enables a linear tuning characteristic for VCO applications.

2. Topology selection

   Two topologies were implemented in the same InGaP HBT technology: balanced Colpitts and balanced Clapp. Balanced Colpitts oscillator has been studied extensively in previous papers and shows excellent phase noise [21, 23], but it has never been implemented in the commercial foundry process in Ericsson. Balanced Clapp oscillator, on the other hand, is not commonly found in open literature, but its property allows more current be injected into the tank, which is believed to further reduce the phase noise. The simplified schematics of the two topologies

are shown in Figure 3.2.

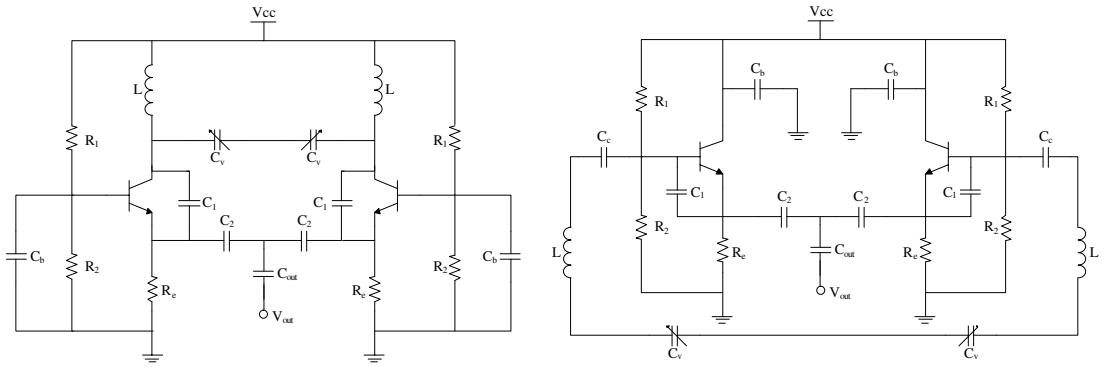


Figure 3.2. Schematics of two topologies implemented

3. Transistor I-V curve simulation

   The I-V curve of the transistor was initially simulated by the DC simulator in ADS. By doing this, one can acquire the basic properties of the transistor and select the optimum DC bias point. The DC characteristic of a default $3 \times 3\mu m \times 30\mu m$ HBT is plotted in Figure 3.3. As can be seen, transistor breakdown behavior could not be simulated, due to the limitation of the Gummel-Poon model, so one must be aware that the collector-emitter voltage should never exceed 10 V, which is the V_{ceo} specified by the foundry. The DC voltage applied to the collector is normally half of the breakdown voltage, or 5 V.

   The DC characteristic slightly varies depending on the transistor size and therefore simulation was performed every time when the transistor size was changed.

4. Initial design parameters calculation

   Initially, the two VCOs were designed with ideal components. Once these ideal VCOs function properly, real components from the foundry PDK library were introduced to better emulate the process. Initial design parameters include the values of tank inductors and feedback capacitors, as well as the sizes of the varactors and transistors.

   To determine these parameters, simple calculations were made based on frequency and tuning range specifications. For both topologies, different combination of tank L and C values can give the same oscillation frequency. As is presented in [21], smaller tank inductor value would result in better phase noise performance for the balanced Colpitts design, so one should design with the smallest possible inductor. As for the balanced Clapp VCO, the relationship between the induc-

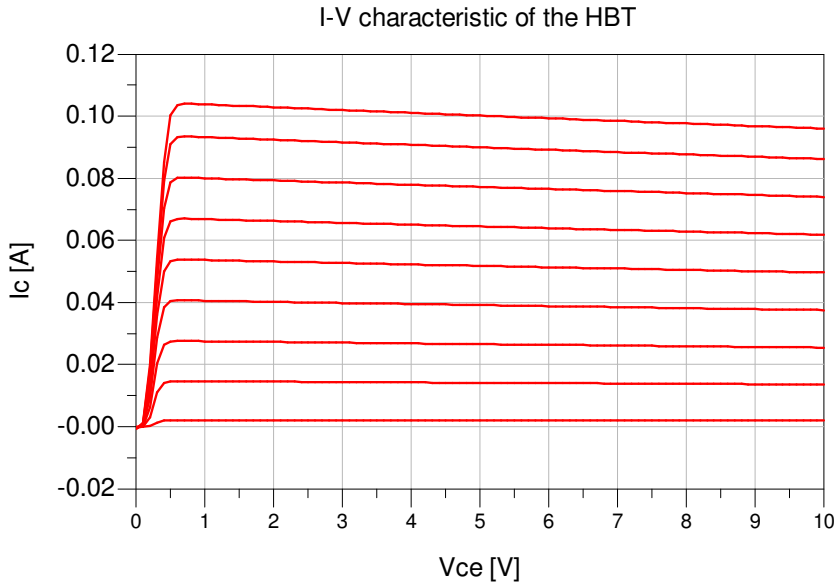


Figure 3.3. DC characteristic of the standard $3 \times 3\mu m \times 30\mu m$ HBT

Parameter	Balanced Colpitts	Balanced Clapp
Tank inductor	250nH	910nH
Feedback capacitor C_1 & C_2	2pF	3.4pF
Varactor size	$100\mu m \times 100\mu m$	$100\mu m \times 100\mu m$
Transistor size	$2 \times 3\mu m \times 20\mu m$	$3 \times 3\mu m \times 30\mu m$

Table 3.2. List of initial design parameters

tor value and phase noise was not clear and therefore the values are from initial guesses and optimized later.

5. Start-up condition analysis

   Start-up condition analysis was performed before detailed designs. This can be done by doing either a small signal loop gain analysis with the 'Ocstest probe' in ADS or an S-parameter simulation for the tank and the active device separately. The latter method was employed during the designs. The simulation result is shown in Figure 3.4. As can be seen, at 5.1 GHz, the negative resistance generated by the active device is more than 10 times of the tank loss, which is sufficient to start the oscillation.

6. Harmonic balance simulation

   The negative resistance provided by the active device is a function of tank voltage amplitude. As the oscillation amplitude grows, the negative resistance will ulti-

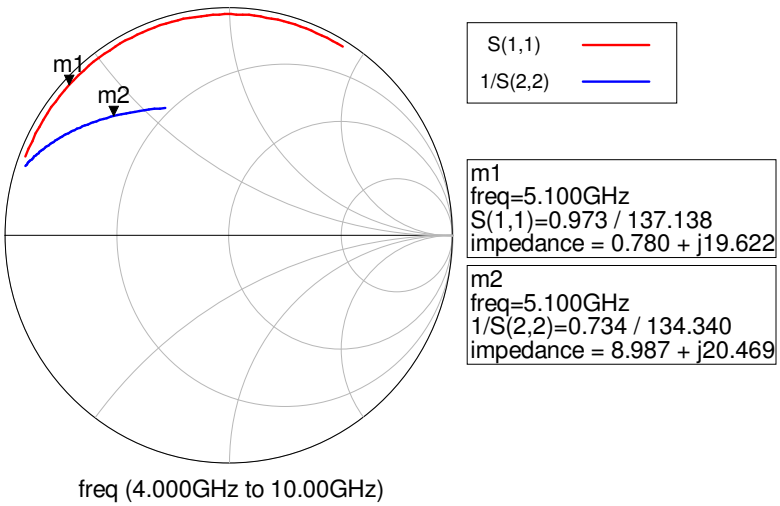


Figure 3.4. Start-up condition analysis

mately reduce to just compensate the tank loss and the oscillator is said to reach steady state. The most efficient way to simulate oscillator large signal behaviors (oscillation power, frequency, and phase noise) is to use a harmonic balance simulator.

The harmonic balance test bench for the balanced Colpitts is shown in Figure 3.5. The tank and the active device were designed in different sub circuits and connected by a differential OscPort2.

The configuration of the harmonic balance simulator needs some special attention to obtain the correct simulation results. As recommended in the ADS manual, the fundamental oversample parameter should be set larger than 4 for phase noise simulation. The order parameter in the harmonic balance defines the maximum harmonic index used for simulation. Larger value of order gives more accurate results but the maximum harmonic frequency should be kept below the limitation of the transistor model to avoid abnormal simulation results.

7. Waveform optimization

   During harmonic balance simulation, the time domain collector current waveform as well as the transistor I_c vs V_{ce} dynamic load line were monitored. The base bias voltage and the emitter degeneration resistor were tuned to control the waveform. The load line was desired to occupy most of the I-V DC curve without reaching the saturation region and exceeding the breakdown limitation.

8. Varactor voltage sweep

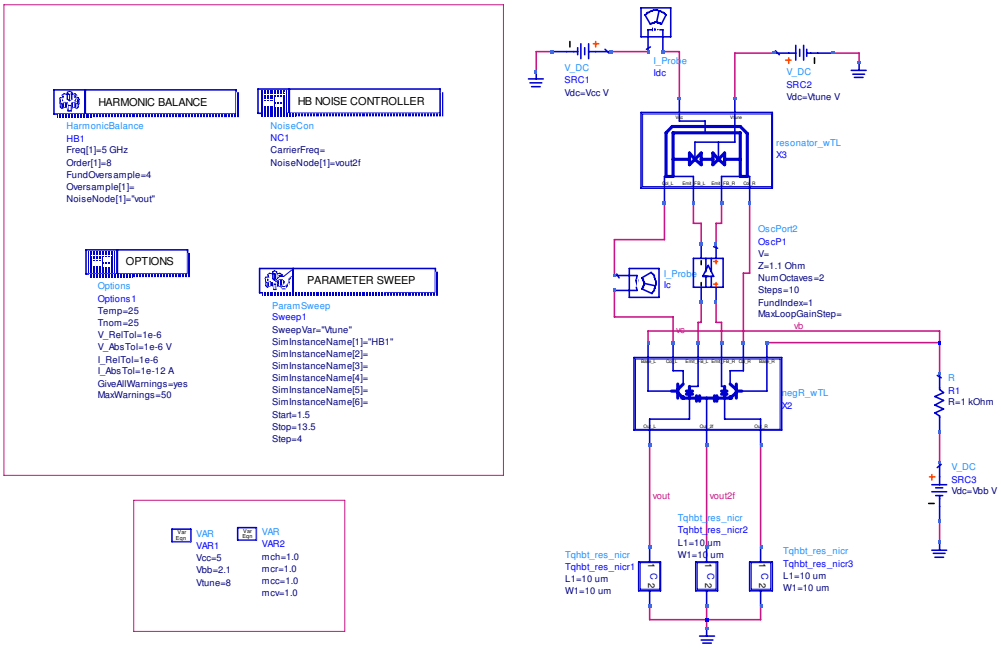


Figure 3.5. Harmonic balance test bench for the balanced Colpitts VCO

The varactor's C-V curve was first simulated by sweeping the reverse bias voltage from 0 V to 14 V. The tuning characteristic of the varactor is presented in Figure 3.6. A capacitance ratio of 2 can be obtained between 1.5 V and 13.5 V tuning voltages. Proper varactor size was chosen depending on the tuning range requirement. The fixed capacitors (the one in parallel with the tank inductor in the Colpitts and the one in series with the tank inductor in the Clapp) ware replaced by the varactors, and harmonic balance simulation was performed for each tuning voltage. If abnormal increase in the phase noise at any tuning voltage was observed, step 5 should be checked for the entire tuning range. Design parameters were tuned to obtain a phase noise performance with flat frequency response.

9. Design parameter optimization

   The effect of various design parameters on phase noise was studied. These include: transistor biasing current density, emitter degeneration inductor value, feedback capacitor ratio and value, varactor arrangement. Details of this section can be found in the following sub chapters.

10. Layout generation and momentum simulation

    The layout was generated in this step, and the schematic with layout parasitic elements was re-simulated. Normally the simulation results will change due to

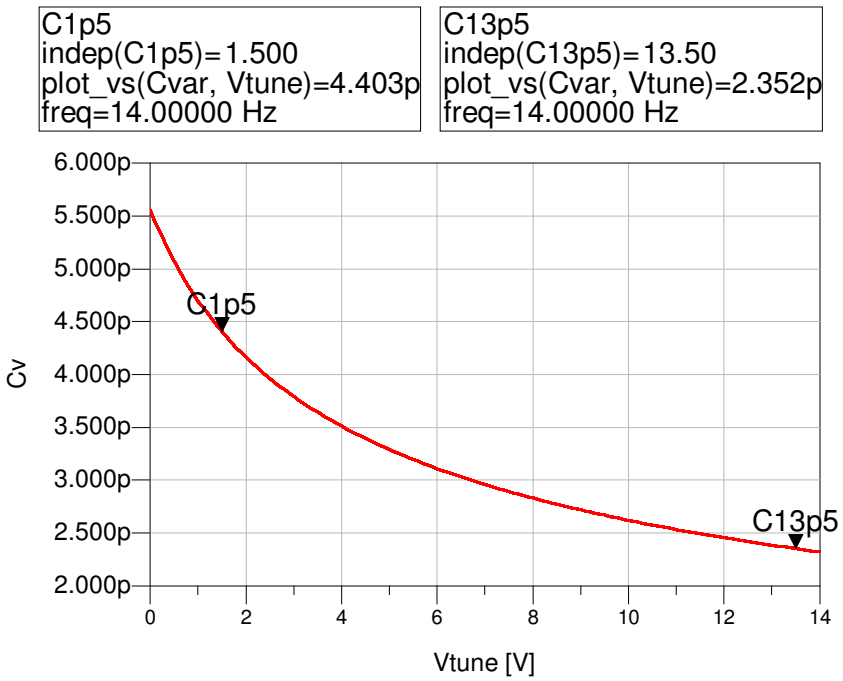


Figure 3.6. The C-V characteristic of a $100\mu m \times 100\mu m$ square varactor

the introduction of the parasitic and one should return to the design procedure from step 3 to 7.

For the critical parts of the circuit, for example the tank inductor, momentum simulator was employed. Momentum is the built-in 2.5D EM simulation engine in ADS and can simulate the passive structures in the planar technology accurately.

The above design procedures were performed in an iterative manner.

3.3. Design Parameters Optimization

3.3.1. Tank quality factor

According to Leesons theory [17], the most obvious way to improve oscillator phase noise is by increasing the signal power and utilizing a high Q resonator. While the former method is straightforward, one can improve the resonator Q considerably by careful design and optimization. In most cases, the total tank Q factor is limited by the inductor and the varactor.

The electrical model of an inductor is presented in Figure 3.6, where R_S and R_P repre-

sent the equivalent series and parallel resistance. The Q factor of an inductor is defined as,

$$Q = \frac{\omega L}{R_S} \tag{3.1}$$

And R_S is given by,

$$R_S = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\tau})} \tag{3.2}$$

Where ρ is the resistivity of the metal, l and w are the length and width of the inductor, respectively, δ is skin depth and t is the metal thickness.

From the above equation, one can observe that the inductor with thicker metal tends to have smaller series resistance and therefore offers a higher Q. In the designs, two-metal-stack microstrip lines with a total thickness of 6 μm were implemented as the tank inductors.

Spiral inductors are normally utilized in RFIC designs since the combination of the self inductance and the mutual inductance makes it possible to obtain an inductance up to several nH at RF frequencies. However, spiral inductors are notorious for their low Q factors. Even with technology evolution and careful optimization, inductor Q is still in the order of 10 at 5 GHz [15].

For microwave applications, transmission lines are preferred since their relatively high Q. A short circuited transmission line has an equivalent inductance given by[24],

$$L = \frac{Z_0}{2\pi f} \tan(\beta l) \tag{3.3}$$

Where Z_0 is the characteristic impedance of the transmission line, f is the operating frequency, β is the phase constant and l is the transmission line length. It should be noted that a transmission can be regarded as an inductor only when its electric length is small.

Transmission lines with widths of 200μm and 100μm were implemented in the Clapp and Colpitts designs respectively.

In a similar way, to increase the Q factor of a varactor, the series resistance should be minimized. This can be accomplished by introducing the finger varactor structure which reduces the sub collector losses [21]. The layouts of a conventional square varactor and a 5-finger varactor are shown in Figure 3.7.

3.3.2. Bias Current Density

The bias current density (J_C) can affect the transistor cutoff frequency and f_t reduces at high current density and the flicker noise is proportional to J_C. For the aim of seeking for the optimum current density, single-ended Clapp oscillator was tested with 9

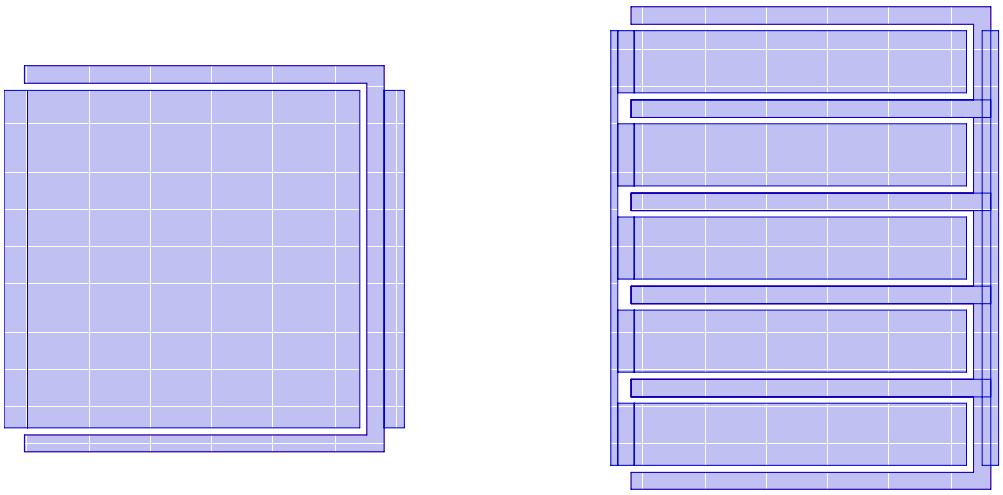


Figure 3.7. The layout of square and finger varactors

different current densities not exceeding $30kA/cm^2$ according to the foundry design manual.

In order to isolate the J_C effect on phase noise, design parameters in Table 3.2 were fixed. At the same time, the ratio of resistors divider R_1 and R_2 and the area of HBT are varied to obtain different J_C.

The simulation results are plotted in Figure 3.8. As can be seen, the phase noise has over 1 dB variation for different current densities and the best phase noise was obtained at J_C around $10kA/cm^2$.

Similar results were observed for a single-ended Colpitts oscillator and one can therefore conclude that the optimum J_C is topology irrelevant.

3.3.3. Transistor Arrangement

The foundry process has unit HBT cell with emitter finger number ranging from 1 to 3. To realize larger total device area, multiple transistor unit cells are connected in parallel, and one can have different combinations of emitter finger number, unit emitter length and width, and transistor number for the same device area. The choice should be made taking into account of layout convenience and thermal stability. Here the effect of transistor arrangement on phase noise was evaluated on transistors with different number of emitter fingers and unit emitter length (UEL). Table 3.3 lists 12 different transistor arrangements employed in the simulation.

To isolate the transistor arrangements effect on phase noise, the optimization was performed on a 5 GHz fixed frequency oscillator with a collector current of 80 mA and a current density of $9kA/cm^2$, in other words, the total emitter area is $900\mu m^2$.

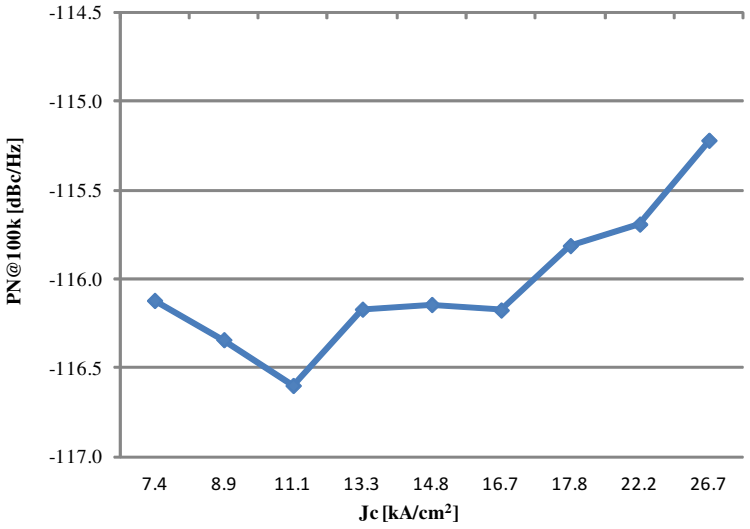


Figure 3.8. Phase noise versus bias current density for single-ended Clapp

No. of fingers	1				2				3			
UEL(μm)	10	15	30	50	10	15	30	50	10	15	30	50
No. of HBTs	30	20	10	6	15	10	5	3	10	6	3	2

Table 3.3. List of different transistor arrangements

The phase noise simulation results are shown in Figure 3.9. As can be seen from the figure, fewer finger transistors with smaller emitter length present superior phase noise and the variation can be more than 1 dB for different configurations. However, 1 finger transistor with small emitter length would be impractical from the layout point of view and should be discarded.

When the transistor is operating under large collector current condition, self heating becomes prominent and the temperatures of all the emitter fingers increase. For the 3-finger case, the center finger becomes hotter than the two outer ones. This results a non-uniform current distribution in which the center finger carries substantial portion of the total current, and will eventually cause stability issues [25]. Therefore, to ensure thermal stability and make the design robust, 2-finger transistors with a UEL of 15μm were employed in the designs.

3.3.4. Feedback Capacitor Ratio and Value

The feedback capacitor ratio is believed to be a vital design parameter in Colpitts-like oscillators. The rule of thumb is a capacitor ratio of 1:4 will result the optimum phase

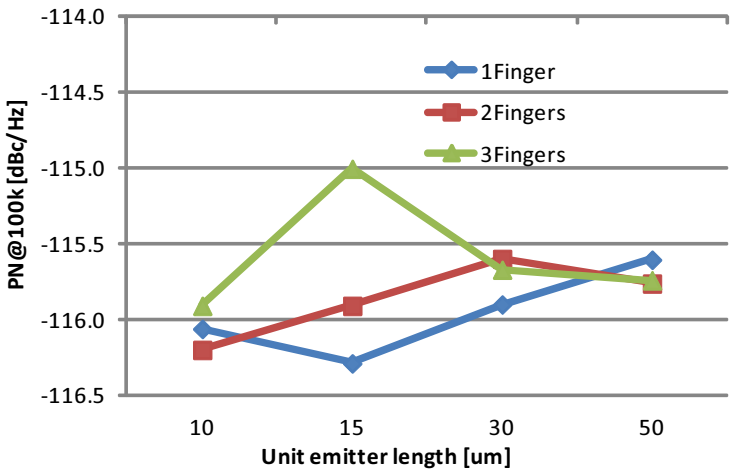


Figure 3.9. Phase noise simulation results for different transistor arrangements

noise and theoretical support was proposed by Lee and Hajimiri with their LTV model [14]. The transistors base-emitter (gate-source) capacitances are generally neglected in most designs; however for microwave frequency oscillators the feedback capacitors become comparable with the intrinsic capacitors of the transistor, a different ratio is expected. Moreover, the optimum capacitive divider ratio is also determined by the technology involved and bipolar transistors generally exhibit a smaller ratio than FETs. It has been shown in [26] that for an InGaP HBT process, the ratio of 1:1.5 provides the best phase noise. Here similar optimization procedures were performed in this commercial HBT process to find the optimum capacitor ratios for both the Colpitts and Clapp designs.

For the Colpitts oscillator, the feedback capacitors are in parallel with the varactors, and therefore the equivalent tank capacitor the sum of them. For this reason, the detailed capacitor value should not be chosen arbitrarily and is given by the tuning range requirement.

Three capacitor ratios were investigated for the Colpitts oscillator, and the simulation results are shown in Figure 3.10. As can be seen, the best phase noise occurs at the capacitor ratio of 1:1.

For the Clapp oscillator, the feedback capacitors are in series with the varactors, and if the capacitance of the varactor is much smaller than that of the feedback capacitors, the equivalent capacitance can be approximated by the varactor. Apart from the capacitor ratio, the effect of feedback capacitor values on phase noise was also investigated.

The capacitor values were swept from $6pF$ to $16pF$ with $2pF$ step, and C_1 and C_2 were assumed to be equal for simplicity. The simulation results are plotted in Figure

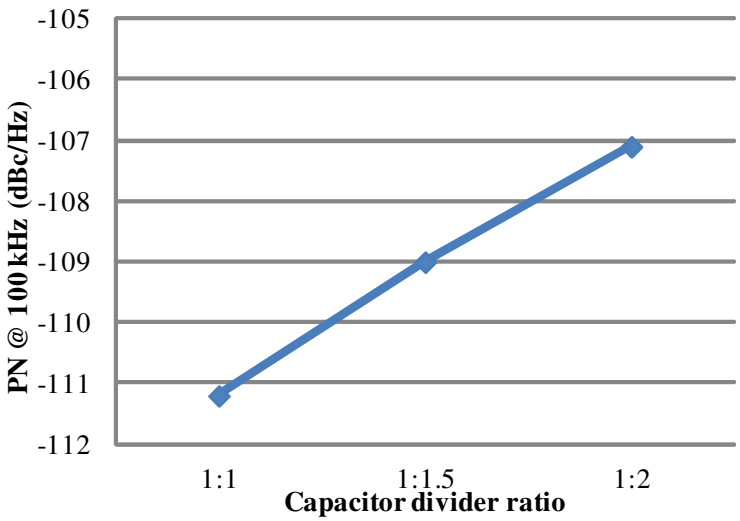


Figure 3.10. Phase noise of the Colpitts oscillator versus feedback capacitor ratio

3.11. As can be seen, the phase noise reduces monotonically until the capacitances reach $14pF$. However, a $14pF$ MIM capacitor is too large to be used in the layout and a large capacitor exhibits lower self resonant frequency which could limit its application at microwave frequencies. Therefore, $12pF$ is considered to be the optimum value for the feedback capacitors, which corresponds to an equivalent capacitance of $6pF$.

Next, the capacitor ratio effect on Clapp topology was investigated. Five ratios were chosen, keeping the equivalent capacitor to be $6pF$. The phase noise simulation results are presented in Figure 3.12. As shown in the plot, best phase noise is observed at the ratio 0.8:1, however, a ratio below 1:1 would make the oscillator hard to startup at low temperature operation. Therefore, a 1:1 capacitor ratio was considered to be optimum, which agrees with the Colpitts topology.

3.3.5. Varactor Bias Choke

The varactor bias choke was utilized to isolate the DC supply and the RF signal on the varactor. It should present sufficient high impedance at the center frequency of the VCO. The RF choke can be implemented by a quarter wavelength transmission line or a large inductor. While quarter wavelength transmission lines are too long to be integrated in the MMIC chip, the spiral inductors were utilized in the designs.

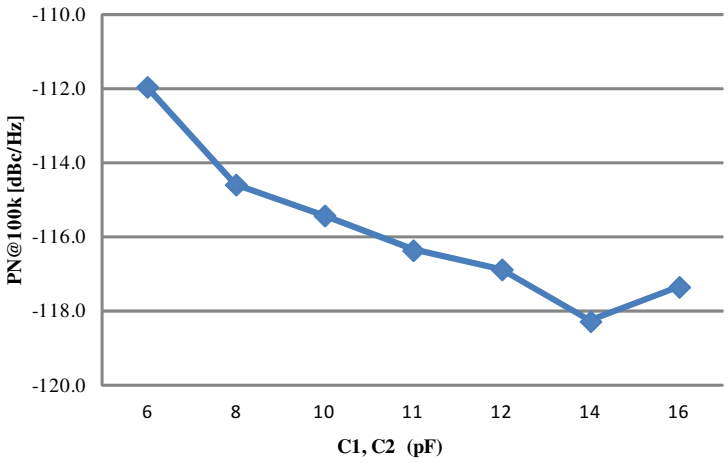


Figure 3.11. Phase noise of the Clapp oscillator versus feedback capacitor values

3.4. Simulation Results

The simulation results for the two designs are illustrated here. These include the frequency tuning characteristic, the output power with respect to tuning voltage, SSB phase noise spectrum and specifically at 100 kHz offset, the I_C vs. V_{CE} loadline and the time domain waveform of I_C and V_{CE}.

3.4.1. Balanced Colpitts VCO

The simulation results of the balanced Colpitts VCO is shown in Figure 3.13. As can been seen, the balanced Colpitts VCO shows oscillation frequencies ranging from 4.8 GHz to 5.4 GHz when the tuning voltage is swept from 1.5 V to 13.5 V. The fundamental output power is larger than 3 dBm throughout the tuning range. The VCO has a phase noise as low as -110 dBc/Hz at 100 kHz offset, exhibiting a 3 dB variation with respect to tuning voltage. The time domain waveform of V_{CE} and I_C together with the dynamic loadline were also plotted and the narrow I_C pulse translates to low phase noise as indicated in [14] [23].

3.4.2. Balanced Clapp VCO

The simulation results of the balanced Clapp VCO is shown in Figure 3.14. The balanced Clapp VCO shows a fundamental oscillation frequency ranging from 4.7 GHz and 5.5 GHz and output power more than 1 dBm for different tuning voltages. Due to the much higher current excitation than the balanced Colpitts VCO, the balanced Clapp VCO is believed to further improve phase noise level according to both LTI[17]

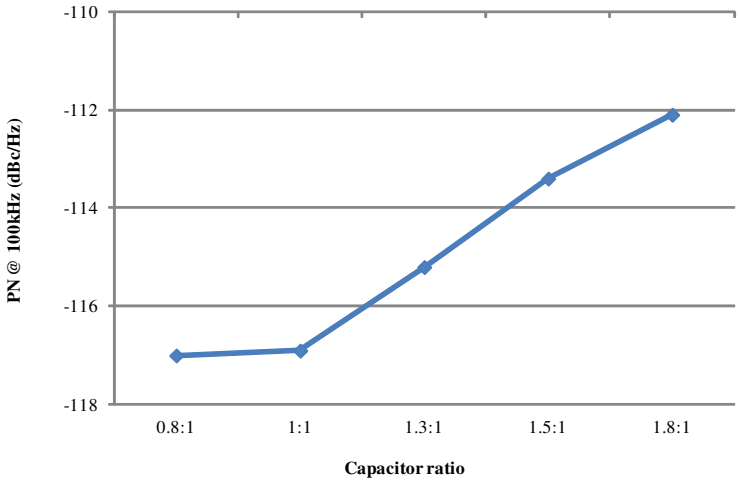


Figure 3.12. Phase noise of the Clapp oscillator versus feedback capacitor ratio

and LTV[14] models. The HB simulation shows a 100 kHz phase noise as low as -122 dBc/Hz, which is more than 10 dB superior to that of the balanced Colpitts. The time domain waveform of V_{CE} and I_C, and the dynamic loadline were plotted as well. However, the loadline is distinct from the balanced Colpitts case and little information can be extracted from it.

3.4.3. Summary and Discussion

To benchmark VCOs with different oscillation frequencies and tuning ranges, the normalized figure of merit with tuning range (FOM_T) is utilized. FOM_T is given by,

$$FOM_T = L(\Delta\omega) - 20 \cdot \log\left(\left(\frac{\omega_0}{\Delta\omega}\right) \cdot \left(\frac{FTR}{10}\right)\right) + 10 \cdot \log\left(\frac{P_{diss}}{1mW}\right) \tag{3.4}$$

Where $L(\Delta\omega)$ is the phase noise at offset frequency $\Delta\omega$, ω_0 is the center oscillation frequency, P_{diss} is the power dissipation, and FTR is the tuning range of the VCO.

The simulation results of these two topologies are summarized in Table 3.4 with FOM_T calculated as well.

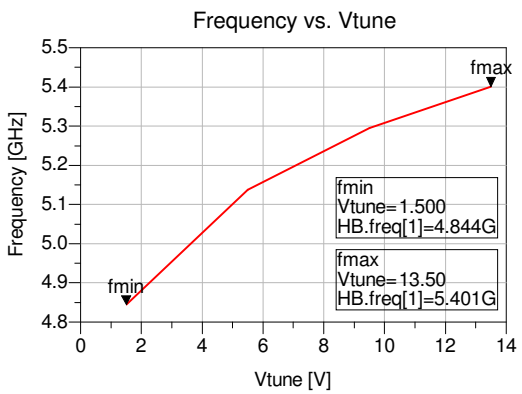
As can be seen from the table, both topologies meet the frequency and tuning range specifications, while the balanced Clapp VCO presents 5% more tuning bandwidth. As far as the phase noise is concerned, the balanced Clapp VCO is roughly 11dB superior for different tuning voltages. The balanced Clapp VCO consumes approximately 4 times DC power of that of the balanced Colpitts VCO. Taking into consideration of all the factors, the balanced Clapp VCO shows 9dB better FOM_T.

	Balanced Clapp	Balanced Colpitts
Frequency	4.71∼5.55GHz	4.84∼5.40GHz
Tuning Range	16.3%	11%
Phase Noise @ 100kHz	-119.6 ∼ -122.2 dBc/Hz	-108.7 ∼ -111.2 dBc/Hz
Output Power	1.1 ∼ 5.5dBm	3.2 ∼ 6.4dBm
Power Dissipation	607 ∼ 755mW	161 ∼ 195mW
FOM_T(averaged)	-191.0 dBc/Hz	-182.5dBc/Hz

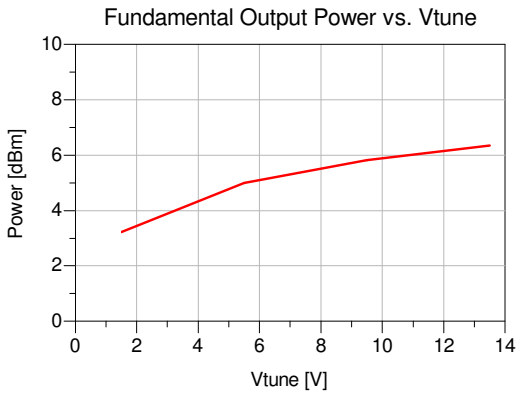
Table 3.4. Summary of simulation results of two VCOs

The superior phase noise obtained from balanced Clapp VCO is partly owing to its high current operation while its Colpitts counterpart can only operates at small current condition. [13], [18] point out that low tank impedance is favorable in low phase noise VCO designs and the solution for balanced Colpitts VCO is to use a tank inductor as small as possible. The Clapp topology, however, can achieve a much smaller equivalent tank impedance than that of the Colpitts; thereby allowing higher current being injected into the tank while still not exceeding the technologys breakdown limitation. The equivalent tank impedance for both topologies is derived in Appendix A.

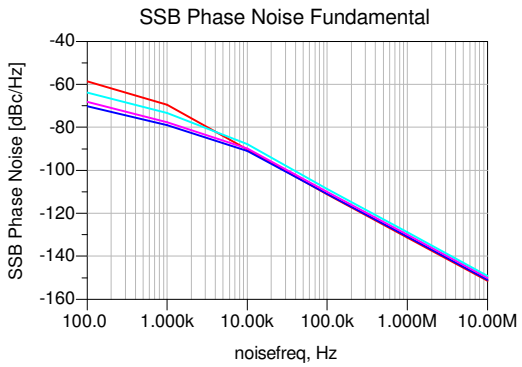
Since the design phase thesis was pure simulation based and no tape-out plan was scheduled. One may easily question the validity of the simulation results, especially the phase noise results. As has been discussed in Chapter 2, the accuracy of phase noise simulation results depends mostly on the accuracy of the transistor noise source modeling and the way in which CAD tools characterize the low frequency noises. However, at 100kHz offset frequency, flicker noise, which is not modeled as cyclostationary in most CAD tools, has little contribution on the phase noise. Therefore small discrepancy between the simulation and measurement results is expected. This assumption has been proved true by tape-outs in the prior version of the current commercial foundry process. The simulation and measured phase noise is plotted in Figure 3.15. As can be seen, the HB simulator generally overestimates the phase noise by 3-5 dB at 100 kHz offset frequency for different tuning voltages while at 10 kHz offset it underestimates the phase noise by up to 10 dB.



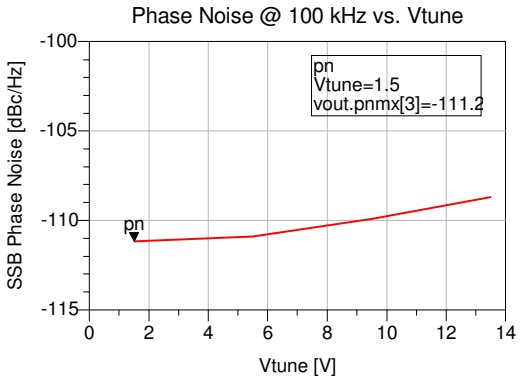
(a) Frequency vs. Vtune



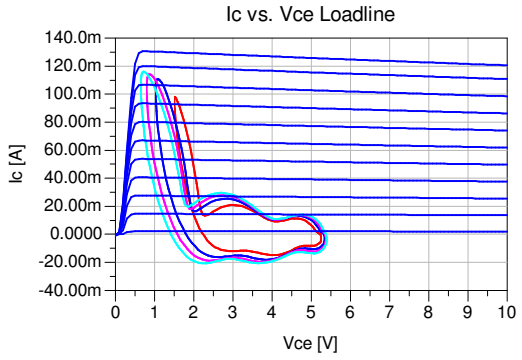
(b) Fundamental Output Power vs. Vtune



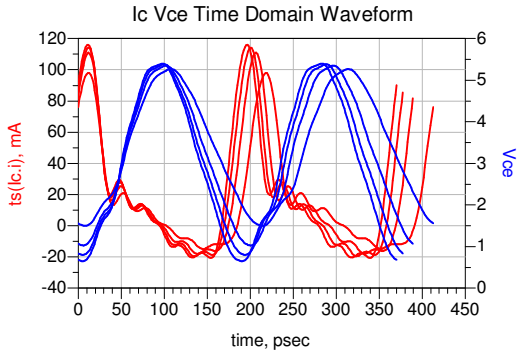
(c) SSB Phase Noise Fundamental Frequency



(d) Phase Noise @ 100 kHz vs. Vtune

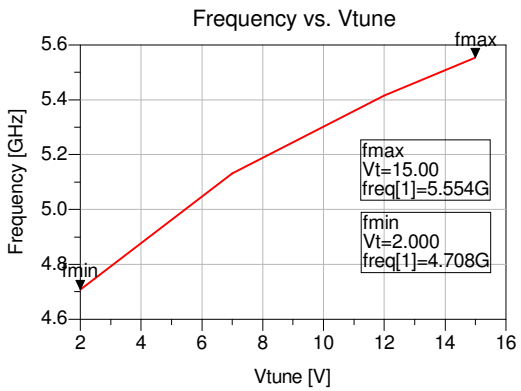


(e) Ic vs. Vce Loadline

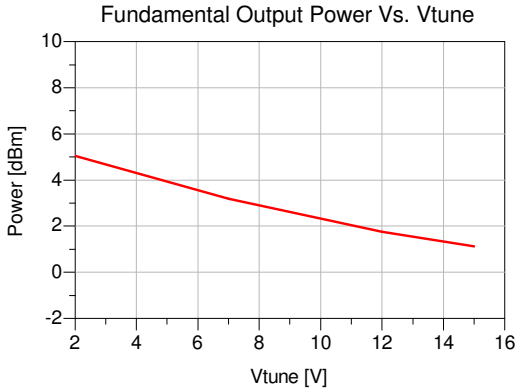


(f) Ic Vce Time Domain Waveform

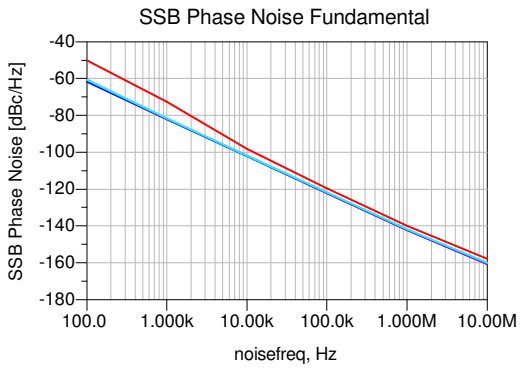
Figure 3.13. Simulation results of the balanced Colpitts VCO.



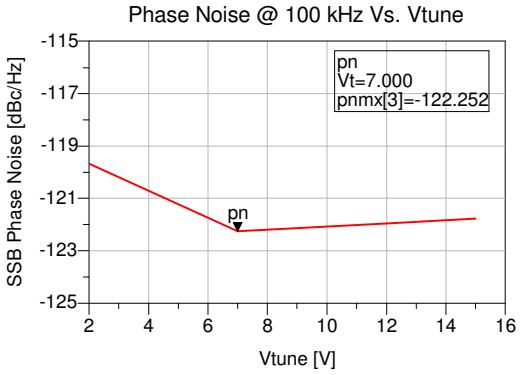
(a) Frequency vs. Vtune



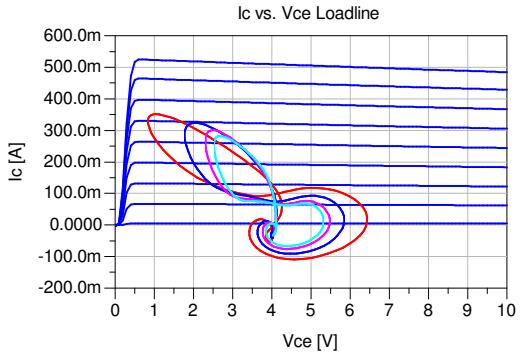
(b) Fundamental Output Power vs. Vtune



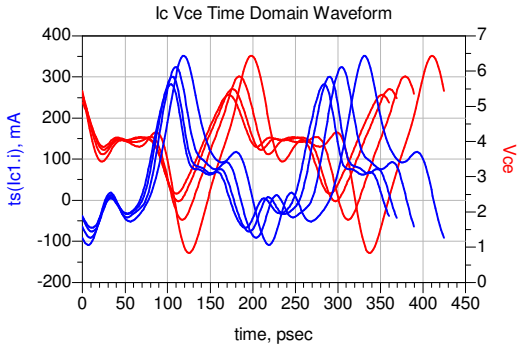
(c) SSB Phase Noise Fundamental Frequency



(d) Phase Noise @ 100 kHz vs. Vtune



(e) Ic vs. Vce Loadline



(f) Ic Vce Time Domain Waveform

Figure 3.14. Simulation results of the balanced Clapp VCO.

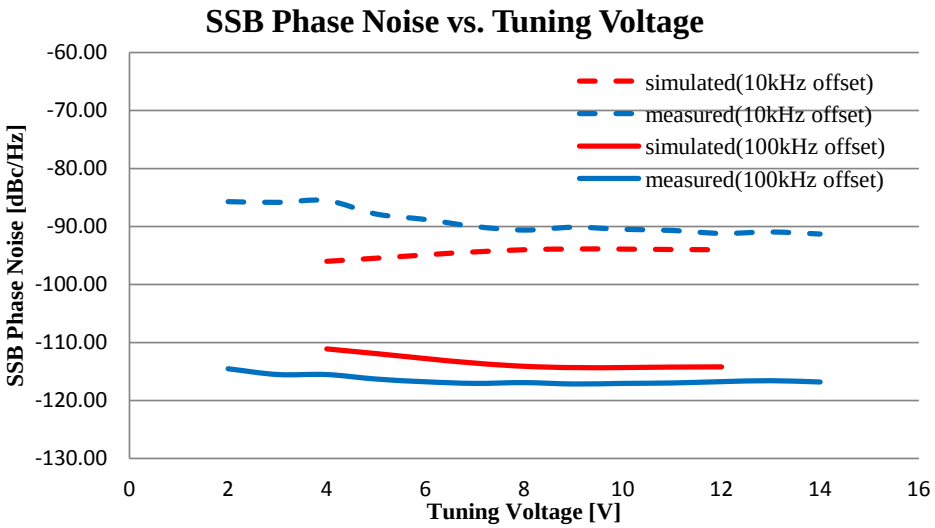


Figure 3.15. Typical phase noise performance of a VCO designed in previous process

4. Conclusion

The evolution of microwave point-to-point radio, towards higher order modulation schemes, is continuously posing more stringent requirement on the signal generating units of the system, the VCOs. Therefore, to design a low-cost and compact MMIC VCO is of great research value.

The study began by reviewing basic theory of oscillator systems, which followed by comparing various resonator and active device technologies, as well as topologies employed in VCO designs. Small signal and large signal analysis of a simple oscillator were carried out for illustrative purpose. Noise modeling of HBT was briefly described and two analytical phase noise models, Leeson's LTI model and Hajimiri's LTV model were presented. CAD tools with HB simulator can facilitate the design of VCOs to a great extent. The principle of HB simulation was introduced and the limitation of the HB simulators in terms of making accurate phase noise prediction was mentioned.

ADS with a commercial InGaP HBT process design kit was employed to design two MMIC VCOs with different topologies, balanced Colpitts and balanced Clapp. The design followed a systematic procedure in an iterative manner. Various design parameters affecting phase noise performance were studied and both VCOs were optimized for the best phase noise performance. Simulation results show that the balanced Clapp VCO is superior in terms of both absolute phase noise value and FOM_T, at an expense of high power consumption. On the other hand, balanced Colpitts VCO can operate under lower current condition while still offering moderate phase noise. The validity of the simulation results was verified by comparing simulation and measured results from a VCO designed with the previous version of this process.

5. Future Work

Despite its inferior phase noise performance, the balanced Colpitts VCO still benefits from its low current operation and thus is more power efficient. Moreover, improvement in phase noise, 3dB in theory, can be achieved by coupling two identical VCOs together using injection locking techniques. Two extra merits are expected from this topology. First the redundancy makes the product more reliable, e.g. once any of the two VCOs fails, the other one still keeps the system running. Second, with proper designed power management circuit, one of the VCO units can be switched off under certain circumstances; thereby reducing the power consumption and making the products more environmentally friendly.

Attempts to include the idea of injection locking were made using the transient simulation. However, due to time constraints, little progress has been achieved. The investigation on injection locking would be a good extension of this work.

Since the design task was based on computer simulations, the results obtained are not totally convincing. Funding permitting, tape-outs and measurements of the two VCOs would further complement this work.

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A. Equivalent Tank Impedance

The tank circuit of a Clapp oscillator is shown in Figure A.1.

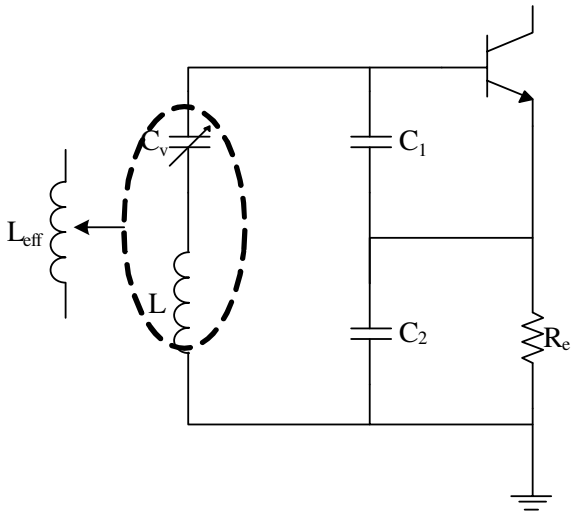

Figure A.1. Equivalent tank inductance of a Clapp oscillator

The oscillation frequency is given by,

$$\omega_{osc} = \frac{1}{\sqrt{LC_{tot}}} \tag{A.1}$$

Where,

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_V} \tag{A.2}$$

For small C_V, Ctot can be approximated by C_V. The series combination of the tank inductor and the varactor is inducive at oscillation frequency, and the effective inductance L_{eff} is given by,

$$j\omega_{osc}L_{eff} = j\omega_{osc}L - \frac{1}{j\omega_{osc}C_V} \tag{A.3}$$

If we define the resonant frequency of the series LC network as ω'_{osc},

$$\omega'_{osc} = \frac{1}{\sqrt{LC_V}} \tag{A.4}$$

So L_{eff} can be expressed as,

$$L_{eff} = L\left(1 - \frac{\omega'^2_{osc}}{\omega^2_{osc}}\right) \tag{A.5}$$

Since C_{tot} can be approximated by C_V, ω'_{osc} is therefore very close to ω_{osc}, this makes that the effective tank impedance much smaller that the impedance of the inductor itself.

In comparison, let us also consider the Colpitts oscillator. The tank circuit of a Colpitts oscillator is shown in Figure A.2.

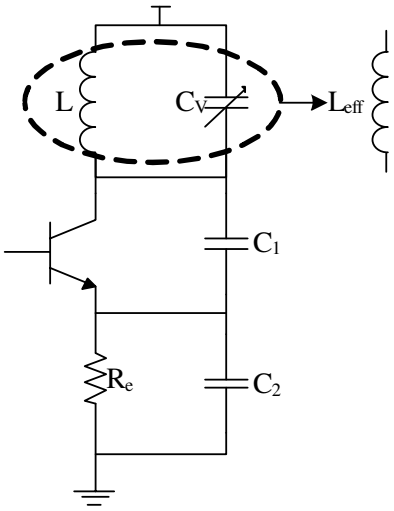

Figure A.2. Equivalent tank inductance of a Colpitts oscillator

The derivation of effective tank impedance is similar as that for the Clapp oscillator. The oscillating frequency is given by,

$$\omega_{osc} = \frac{1}{\sqrt{LC_{tot}}} \tag{A.6}$$

Where C_{tot} can be written as,

$$C_{tot} = \frac{C_1 + C_2}{C_1 C_2} + C_V \tag{A.7}$$

So C_{tot} is larger than C_V, and the effective inductance of the parallel tank is given as,

$$j\omega_{osc} L_{eff} = \frac{1}{j\omega_{osc} C_V + \frac{1}{j\omega_{osc} L}} \tag{A.8}$$

The resonant frequency of the parallel LC network is,

$$\omega'_{osc} = \frac{1}{\sqrt{LC_V}} \tag{A.9}$$

Finally the effective inducatance can be rewrote as,

$$L_{eff} = \frac{L}{1 - \frac{\omega^2_{osc}}{\omega'^2_{osc}}} \tag{A.10}$$

and is larger than the original tank inductance.