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The Design of Boron Epitaxial Emitter for IBC Solar Cells

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Abstract

The efficiency of P-type Cz-Si base solar cells shows a severe degradation of up to 10% relative under illumination (light-induced degradation) or minority carrier injection in the dark, due to the existence of well-known boron-oxygen defect. N-type Silicon substrate as an alternative material has a large potential to be widely developed in industry because of its tolerance to impurities and no boron-oxygen related light-induced degradation even in the presence of a significant amount of oxygen.

In this project n-type substrate silicon solar cells were fabricated and investigated. In previous studying at IMEC, the performance of n-type solar cell, of which emitter was formed by APCVD can obtain an efficiency up to 17.0%. The impact of silicon wafer starting surface before CVD is considered as one of main factor that influences the efficiency. We expect to find out the reasonable thickness of raw substrate to be removed by saw damage removal and chemical polishing. The emitter is going to be applied to interdigitated back contact (IBC). The second purpose is to study the influence of thermal oxidation on emitter doping concentration profile. In the fabrication of bulk crystalline silicon solar cells always involves 2~3 high temperature processes. Thus how much the thermal oxidation will affect the cells is the other goal of this study. In addition, two types of passivation will be investigated. Finally, an IBC solar cells simulation were performed with three types of emitter doping profile, gaussian function, complementary error function and box emitter doping profile.

Keywords: solar cell, IBC solar cell, CVD, boron epitaxy emitter, substrate surface influence, SiO_2 passivation, Al_2O_x ALD

CONTENTS

Abstract I

1 Introduction 1

1.1 Development of Photovoltaic 1

1.2 PV market 1

2 Theory 5

2.1 Standard solar cell and basic working principle 5

2.2 Light absorption 5

2.2.1 Sun radiation spectrum 6

2.2.2 Absorption Efficient 6

2.3 Recombination, Lifetime and Diffusion length 8

2.4 Carrier Separation 9

2.4.1 Drift 10

2.4.2 Diffusion 10

2.5 Solar Cell *I* –*V* Characteristics 11

2.6 Resistance Effect 13

2.7 PV cells 14

2.7.1 Bulk crystalline silicon solar cell 14

2.7.2 Thin film solar cells 15

3 IV Performance optimization 16

3.1. Structure design 16

3.2 Light absorption enhancement and recombination minimization 17

3.2.1Texture 17

3.2.2 Coating 17

4 Experimental 19
4.1 Saw damage removal (SDR) 19
4.2 CP4 Polish 20
4.3 Wafer clean 21
4.4 Emitter formation by CVD 21
4.5 Roughness measurement 22
4.6 Defect density measurement 22
4.7 Passivation 23
4.8 Sheet resistance, SRP measurement 24
4.9 Lifetime measurement 24
5 Result and discussion 26
5.1 Impact of starting substrate surface 26
5.2 Thermal oxidation study 28
5.2.1 Effect of the Oxidation Temperature 28
5.2.2 Effect of the Number of Oxidations 29
5.3 Emitter Performance with AlOx ALD Passivation 30
5.4 Simulation 30
6 Conclusions and outlook 32
Acknowledgements 34
References 35

1 Introduction

1.1 Development of Photovoltaic

With the increasing demand of energy and environmental concern, depletable and contaminative fossil fuels should not be human's main energy source in the long run. Alternative renewable energies have to be explored. One of them is solar energy. The earth approximately absorbs solar energy 3.85E+6 exajoules (EJ) per year [1]. While in 2008 total worldwide energy consumption was 474 EJ [2].

A photovoltaic (PV) cell or solar cell is a device which directly converts sunlight to electricity. This is a clean and sustainable process. If we harvest a tiny fraction of the solar energy using PV cells, it can relieve or even solve the world energy problem. Working as an individual system the PV cells can provide electricity to people in remote areas avoiding transmission. Also it is a non-toxic and no greenhouse emission device. Thus PV electricity is highly appreciated by public. For example, in Japan after the disaster earthquake happened in 2011-03-11 causing nuclear leaking, people become more care safety of new energy. The crisis in Japan has re-opened the debate on the world's future energy mix and security of energy supply. In this context, PV is more than ever part of a global renewable solution [3]. The government is considering a plan that would make it compulsory for all new buildings and houses to come fitted with solar panels by 2030, according to the Nikkei business daily.

Charles Fritts is the person who created the first working solar cell in 1883 with an efficient of 1% [4]. Then in 1950 the photovoltaic cell was developed at Bell Labs primarily initially for space applications. At the end of 1960s PV were used successfully as a power source for satellites. However due to the high cost of PV cells, the terrestrial application development was limited. When it came to 1970s the energy crisis catalyze governments developing the PV technology, and PV industry boosted for a short period. But in the early 1980s oil price began to fall, the growth of PV slowed down again till 1999. When time steps into 21th century PV industrial grows faster than ever.

1.2 PV market

During the past 10 years the photovoltaic (PV) market has experienced unprecedented growth. Entering the 21th not only because of the oil price rising but also the whole world become more and more concerned with the environment problems. At the same time the decreasing raw materials price, developing fabrication technology makes the PV electric price drop

significantly, see in figure 1. With these impetuses, the PV industry has an exponential growth starting at that time, the data shows in figure 2. Especially in 2010, more than 16 GW of PV has been sold worldwide, and the photovoltaic market has reached a cumulative installed capacity of roughly 40 GW and produce approximately 50 TWh of electricity every year [3].

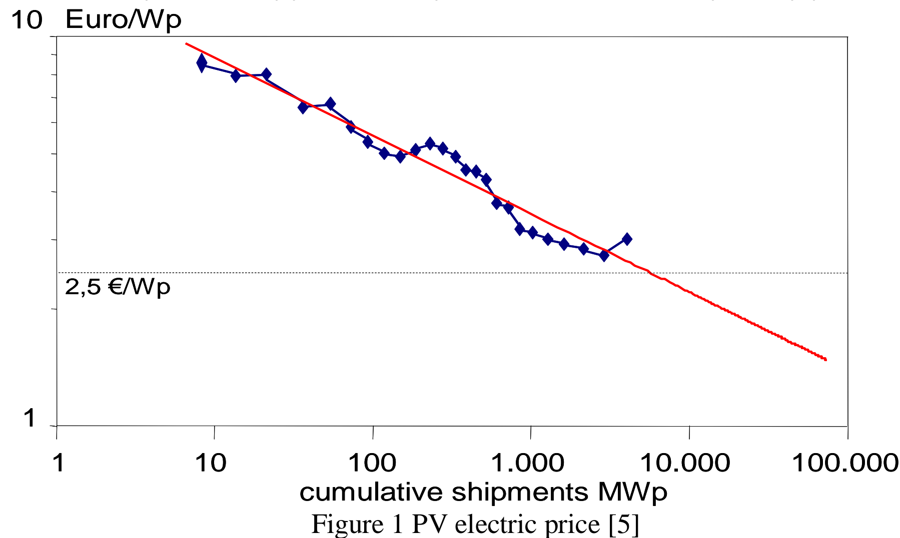


Figure 1 PV electric price [5]

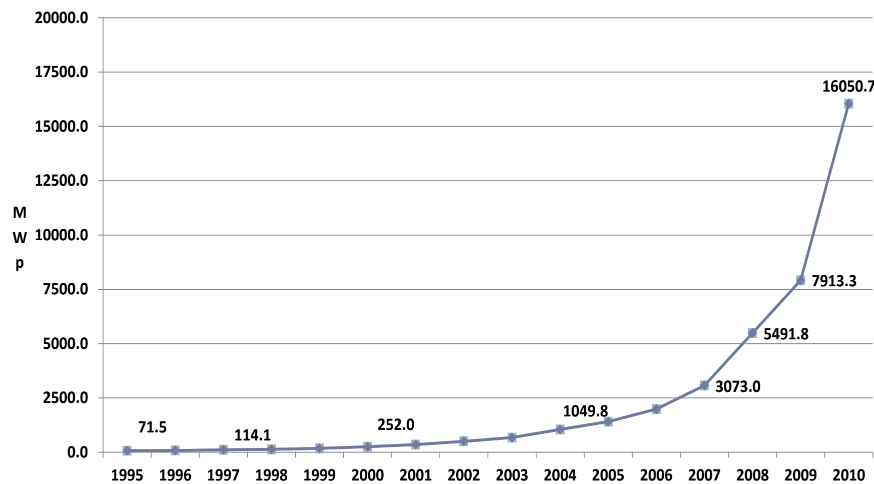


Figure2.PV-market: exponential growth [5]

Despite the significant development of solar cells, the high cost still remains the limiting factor for the implementation of the solar electricity in a large scale. The dominate goal of PV industry is to fabricate solar cell on large scale with high efficiency and cost-effective. To meet this goal different types of PV cells are under research.

There are several types of solar cell produced for terrestrial application in industrial, assorted by materials: crystal silicon solar cell, amorphous Si, cadmium telluride (CdTe), copper indium gallium diselenide(CIGS), dye-sensitized solar cell(DSC) and other organic solar cells. In figure 3 shows the efficiency revolution for these different types of solar cells from 1976 to 2010.

The best efficiency of 41.6% in figure 3, set by Spectrolab a subsidiary of Boeing at the end of 2009, after the Fraunhofer Institute for Solar Energy (ISE) had achieved 41.1% in early 2009. But actually the new record for highest efficiency was broken in October 2010. Spire Semiconductor set a new world record for solar cell efficiency. Working with the US National Renewable Energy Laboratory (NREL) under an 18 month incubator project, the company produced a "triple-junction cell" that has apparently achieved 42.3% conversion efficiency. These records are all in lab. Spectrolab is bringing this kind of efficiency to mass production with the announcement of its C3MJ+ solar cells which boast an average conversion efficiency of 39.2 percent [6]. However this type of multijunction Concentrator solar cell is use in space application in which the energy supply should be independent by the satellite itself so the efficiency is more important than price. The more common PV cells in industrial are the other types

Figure 3 PV cell efficiency research

The most common solar cells are made from Czochralski-grown crystalline silicon (c-Si) or block-cast material in multicrystalline (mc-Si), also called bulk crystalline solar cell. It dominates around 87% of the world market in2010, Figure4 [5]. The others types of solar cells called thin film solar cell with a relatively low efficiency. The driving force to develop these cells is to reduce the cost of materials. They have a thickness from a few nanometers to tens of micrometers. In 2011 although they only hold 13% market all together, their market will grow with the development of technique. They are flexible and also is now available in large module. Expectations are that in the long-term, thin-film solar PV technology would surpass dominating conventional solar PV technology [7]

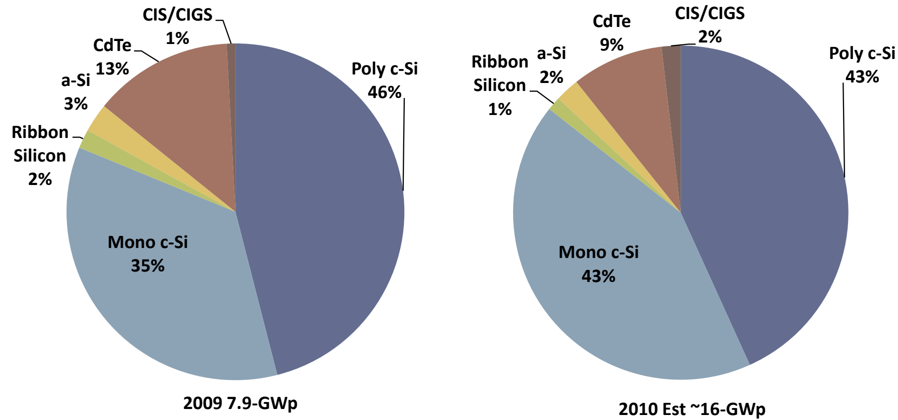


Figure 4 PV market for different types of PV cells

All these types of solar cells are developing simultaneously. Each type has its own merits to charge the market due to different demand. However silicon solar cell is still expected to hold 50 percent market share by 2020. Being a mature participant in the market and having abundance of resources, c-Si cells should ensure its usage throughout this decade. In this project the subject investigated is silicon crystal solar cell.

2 Theory

2.1 Standard solar cell and basic working principle

Solar cells are fundamentally quite simple devices. In most cases they are made from semiconductor materials which can absorb light energy and produce electron-hole pairs. A solar cell is a well designed semiconductor p-n junction that can separate and collect the electron and holes in a specific direction, depicted in figure 5.

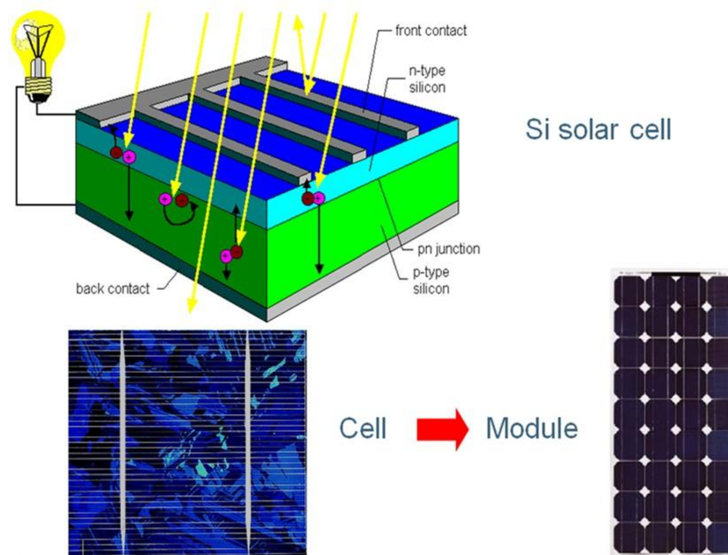


Figure 5 the working principle of solar cell

When the incident sunlight reaches solar cell front side, one of the electrical contacts of the diode at the front formed by a metallic grid allows light to fall on the semiconductor. When the energy of an incident photon hν is larger than the band gap of the semiconductor, the energy will be absorbed and generate one electron-hole pair. There is always a thin antireflective layer deposited under the grid lines which increases the volume of light transmitted to the semiconductor. The p-n junction is formed when an *n*-type semiconductor and a *p*-type semiconductor are brought together with a close contact. This is typically achieved through diffusion or deposition process or implantation of specific dopants. The diode's other electrical contact is on the backside of the solar cell formed by a metallic layer. To understand the detail of how solar cell works, how to characterize its performance and how to improve it, each step of the electricity generation process needs to learn.

2.2 Light absorption

2.2.1 Sun radiation spectrum

The surface of sun called photosphere, is at a temperature of about 6000K and closely approximates a blackbody. The isotropic emission from the Sun when reach to the Earth, however due to the long distance from sun to earth, the light can be considered as parallel streams for practical purpose. The radiation intensity that the sun light incidents on a plane perpendicular to the rays is called Solar constant. It is about 1.353kW/m^2. The air mass (AM) is a value that indicates the influence of sunshine absorbed by air during the penetration through the atmosphere. The definition equation is given by:

$$Air\ Mass = \frac{1}{\cos\theta} \qquad (1)$$

Where $\boldsymbol{\theta}$ is the angle of incidence light($\boldsymbol{\theta = 0}$ means the sun is perpendicular to the surface) . The sun spectrum with different AM shows below. AM=1.5 solar spectral irradiance distribution, a turbidity of 0.27 and a tilt of 37° is a standard reference spectral irradiance for all terrestrial application which representative of average condition **in the 48 contiguous states of the United States**[8].

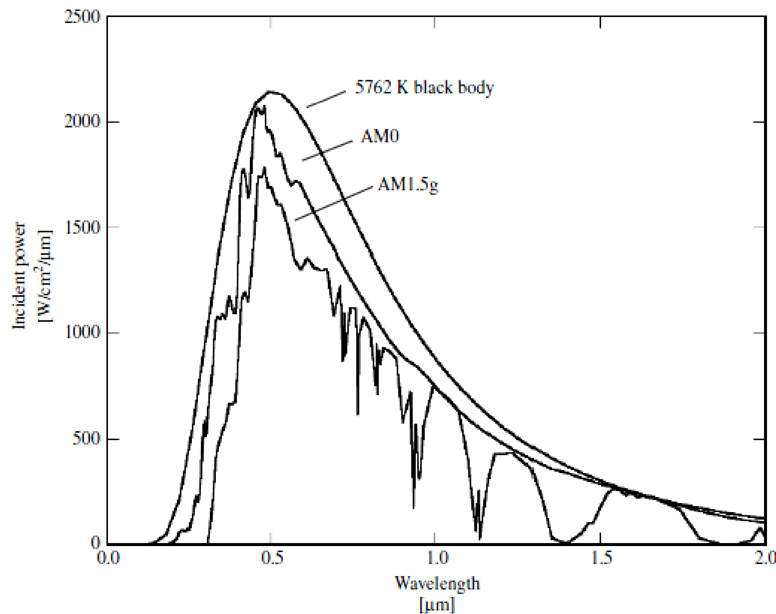


Figure 6 The radiation spectrum for a black body at 5762 K, an AM0 spectrum, and an AM1.5 [8]

2.2.2 Absorption Efficient

The most common solar cells are made of semiconductor materials which have an intermediate property between conductor and insulators. Their energy band has a certain gap between the valence band and conduction band, see picture. This structure is different from conductor and insulator. The conductor has no gap between the bands that allows the electron move freely.

The insulator has a very big band gap which is very hard to let the electron transport in such materials. Semiconductor however has a band gap in between. When the incident light energy $h\nu$ is greater than band gap, it will possibly be absorbed. And an electron from the valence band E_1 will be excited into the conduction band E_2 leaving a hole in the valence band thus forms an electron-hole pair, Figure 7.

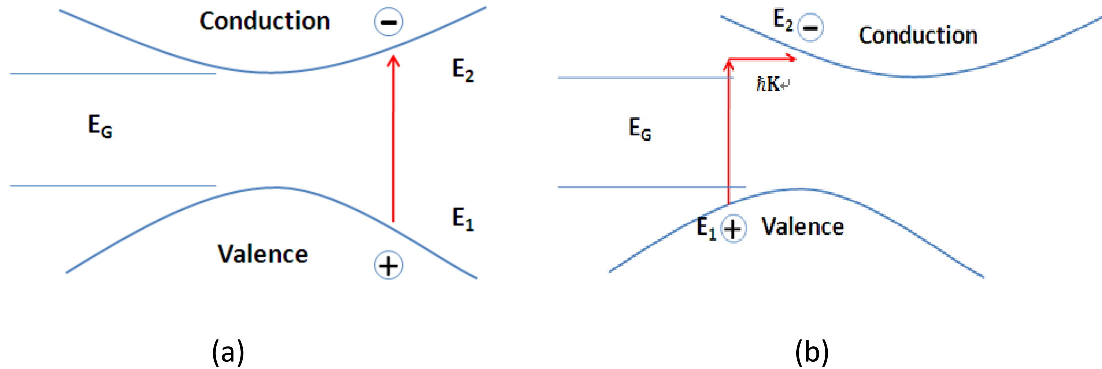


Figure 7 (a) Semiconductor with direct band gap (b) Semiconductor with indirect band gap

In direct band gap semiconductors, such as GaAs, GaInP, CdTe, and Cu(InGa)Se2, the basic photon absorption process is illustrated in Figure 7(a).

However Silicon, the dominate semiconductor materials for PV cell in industry, has an indirect band gap 1.12eV. The excitation of an electron from valence band to conduction band is more difficult in such structure that reduces the absorption possibility. Not only the energy, but also the momentum should be considered.

To measure the absorption possibility absorption coefficient is induced [9]. For direct band gap the absorption coefficient is

$$\alpha(h\nu) \approx A^*(h\nu - E_G)^{1/2}, \quad (2)$$

where A^* is a constant, $h\nu$ is the energy of incident photon and E_G is the band gap energy.
In indirect band gap semiconductors like Si and Ge, the absorption coefficient is

$$\alpha_a(h\nu) = \frac{A(h\nu - E_G + E_{ph})^2}{e^{E_{ph}/kT} - 1} \quad (3)$$

$$\alpha_e(h\nu) = \frac{A(h\nu - E_G - E_{ph})^2}{1 - e^{E_{ph}/kT}} \quad (4)$$

$$\alpha(h\nu) = \alpha_a(h\nu) + \alpha_e(h\nu). \quad (5)$$

Where $\alpha_a(h\nu)$ is the phonon absorption coefficient, $\alpha_e(h\nu)$ a phonon is emitted coefficient. Because both processes are possible

So from the absorption coefficient we can get the rate of creation of electron-hole pairs as a function of position within a solar cell

$$G(x)=(1-s)\int_{\lambda}\big(1-r(\lambda)\big)f(\lambda)\alpha(\lambda)e^{-\alpha x}\,d\lambda \qquad (6)$$

Where s is the grid-shadowing factor, r(λ) is the reflectance, α(λ) is the absorption coefficient, f(λ) is the incident photon flux (number of photons incident per unit area per second per wavelength), and the sunlight is assumed to be incident at x = 0 [10].

2.3 Recombination, Lifetime and Diffusion length

After the electron-hole pair being created, they tend to relax back toward their equilibrium values through a process called recombination in which an electron falls from the conduction band to the valence band, thereby eliminating a valence-band hole. There are several recombination mechanisms important to the operation of solar cells – recombination through traps (defects) in the forbidden gap commonly referred to as Shockley–Read–Hall recombination, radiative (band-to-band) recombination, and Auger recombination

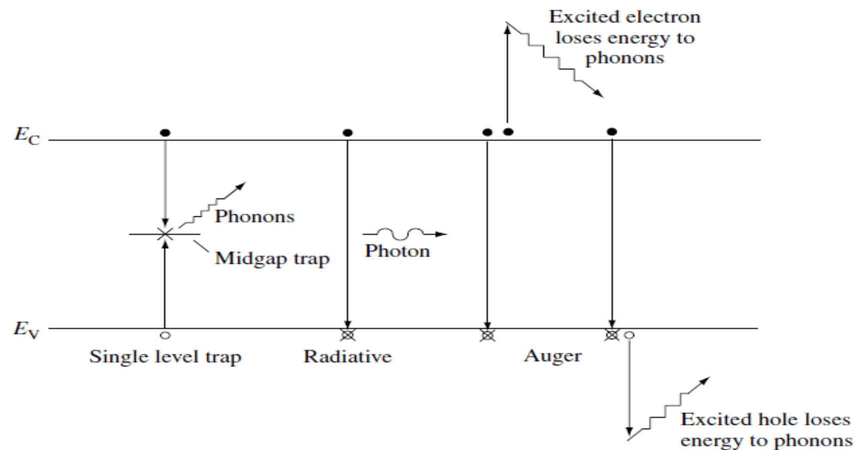


Figure 8 three types of recombination

1. SHR

   Shockely-Read-Hall recombination also known as avoidable recombination which comes from the impurity (defects) of the material. The defect is a recombination center. An electron (or hole) is trap in the forbidden region by the defect, while a hole (or electron) travels to the same energy state before the electron is re-emitted to the conduction band they will recombine in the trap [11]. A high defect density leads to low lifetime of the carries. And the recombination trap center can be imagined as a target present to the travelling carrier with a certain velocity. For a given time, if the velocity is high it will have a higher chance to be captured by the trap .Also the size of the trap affects the recombination possibility. The larger size is more easily to trap the carrier and lower down lifetime. SHR recombination happens more common in bulk crystalline solar cell with a thick substrate. The thick substrate contains the defect can either be unintentionally

introduced or purposely added to the substrate, for example in doping the material. Because of the thick substrate, the carries are more likely to recombine during their diffusion. So for thin film solar cell with very thin layer, this is not the dominant recombination.

2. Radiative

Radiative present the phenomenon that an electron from the conduction band recombines with the hole directly in the valence band and release the energy in the form of a photon. This is also the basic working principle of the light-emitting-diodes (LEDs). The phenomenon happens in the direct band gap semiconductor materials very often like GaAs etc. While in the solar cells which are made from silicon with indirect band gap, this type of recombination is very weak.

3. Auger

Auger recombination is similar to the Radiative. The recombination pass way is the same, however instead of releasing the energy through a photon, auger recombination give the energy to another carrier. This electron (or hole) then relaxes its excess energy and momentum to the phonon, also known as thermally relaxation. So in heavily doped materials auger recombination is very important.

To express how fast the recombination happens, there is a critical parameter called recombination rate. Two parameters that are integral to recombination rate are the minority carrier lifetime and the minority carrier diffusion length. The minority carrier lifetime of a material, denoted by τ_n or τ_p, is the average time which a carrier can spend in an excited state after electron-hole generation before it recombines. Short lifetimes mean that the diffusion length in the base is much less than the base thickness and carriers created deeper than about one diffusion length in the base are unlikely to be collected. Thus the lifetime is a key property for choosing the material for solar cell.

2.4 Carrier Separation

The generated electron and hole behave in the semiconductor now can move like free particles with effective masses m_n^* and m_h^* respectively. To obtain the current we need to separate the electrons and holes and let them move in the opposite direction. There two mechanisms of carrier separation, diffusion and drift.

2.4.1 Drift

Drift is a charged particle's response to an applied electric field. When an electric field is applied across a uniformly doped semiconductor, the bands bend upward in the direction of the applied electric field. Electrons in the conduction band, being negatively charged, move in the opposite direction of the applied field and holes in the valence band, being positively charged, move in the same direction of the applied field. With nothing to impede their motion, the holes and electrons would continue to accelerate without bound. However, the semiconductor crystal is full of objects with which the carriers collide and are scattered. These objects include the component atoms of the crystal, dopant ions, crystal defects, and even other electrons and holes. The net effect is that the carriers appear to move, on a macroscopic scale, at a constant velocity v_d, the drift velocity. The drift velocity is directly proportional to the electric field

$$|\underset{V_d}{\rightarrow}| = |\mu\underset{E}{\rightarrow}| = |\mu\nabla\phi| \quad (7)$$

where μ is the carrier mobility. The carrier mobility is generally independent of the electric field strength unless the field is very strong, a situation not typically encountered in solar cells. At low impurity levels, the mobility is governed by intrinsic lattice scattering, while at high levels the mobility is governed by ionized impurity scattering.

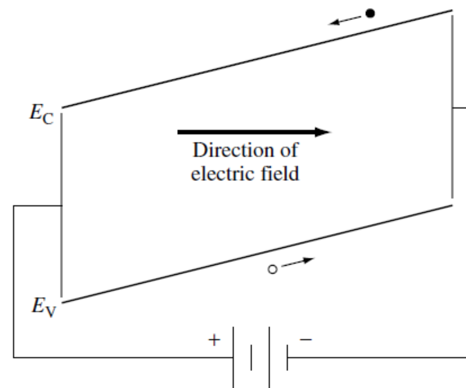


Figure 9 Illustration of the concept of drift in a semiconductor.

The drift current densities for holes and electrons can be written as

$$J_n^{drift} = -qpv_d = -q\mu_n p\nabla\Phi \quad (8)$$

$$J_p^{drift} = qpv_p = q\mu_p p\nabla\Phi \quad (9)$$

2.4.2 Diffusion

Another mechanism is that electrons and holes in semiconductors tend, as a result of their random thermal motion, to move (diffuse) from regions of high concentration to regions of low concentration. Much like how the air in a balloon is distributed evenly within the volume of the balloon, carriers, in the absence of any external forces, will also tend to distribute themselves evenly. This process is called *diffusion* and the diffusion current densities are given by

$$J_p^{diff} = -qD_p\nabla p \quad (10)$$

$$J_n^{diff} = qD_n \nabla n \quad (11)$$

where *Dp* and *Dn* are the hole and electron diffusion coefficients, respectively. Note that they are driven by the gradient of the carrier densities. In thermal equilibrium, there can be no net hole current and no net electron current.

Then the total hole and electron currents (vector quantities) are the sum of their drift and diffusion components [10]:

$$J_{tot} = J^{drift} + J^{diff} = J_n^{drift} + J_p^{drift} + J_p^{diff} + J_n^{diff} \quad (12)$$

2.5 Solar Cell *I* –*V* Characteristics

Solar cell I-V characterization is one of the critical parts from which we can obtain the solar cell efficiency and other electrical properties. From the equation (12) we can get the total current:

$$I = A[J_n + J_p] \quad (13)$$

The general solution of this equation is [10]

$$I = I_{SC} - I_{01}(e^{\frac{qv}{kT}} - 1) - I_{02}(e^{\frac{qv}{2KT}} - 1) \quad (14)$$

where I_{o1} is the dark saturation current due to recombination in the quasi-neutral regions. And I_{o2} is the dark saturation current due to recombination in the space-charge region. I_{sc} is the short-circuit current when the cell is short circuited under illumination, the maximum current. These values depend on the solar cell structure, material properties, and the operating conditions. While under open circuit conditions no current can flow and the voltage is at its maximum, called the open circuit voltage (V_{OC}). From a circuit perspective, it is apparent that a solar cell can be modeled by an ideal current source (I_{SC}) in parallel with two diodes. Diode 1 represents the recombination current in the quasi-neutral regions I_{01}, while diode 2 represents recombination in the depletion region I_{02}.

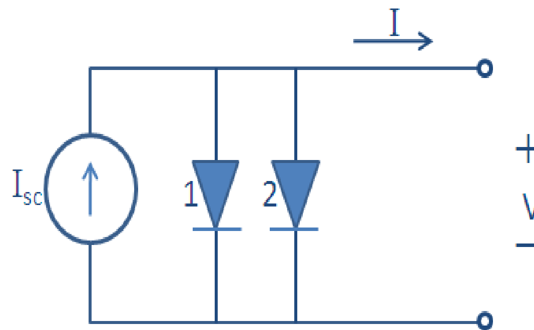


Figure 10 Simple solar cell circuit model

And the I-V curve of a solar cell is plotted in figure 10. There are simply four parameters to characterize the solar cell performance, open circuit voltage (Voc), saturation current (Isc), power conversion efficiency (Eff) and fill factor (FF).

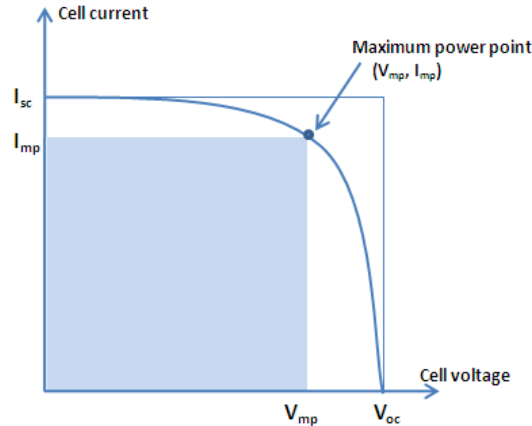


Figure 11 Solar cell's characteristic parameter

The maximum power point P_{mp} is particular interesting which illustrate the power conversion efficiency and fill factor. As seen in Figure 11, this point defines a rectangle whose area, given by $P_{mp} = V_{mp} * I_{mp}$, is the largest rectangle within any point in the I-V curve. So we can get:

$$FF = V_{mp} * I_{mp} / V_{oc} * I_{sc} \tag{15}$$

$$P_{mp} = FF * V_{oc} * I_{sc} \tag{16}$$

$$Eff = P_{mp} / P_{in} = FF * V_{oc} * I_{sc} \tag{17}$$

P_{in} is the power of incident light that is determined by the properties of the light spectrum incident upon the solar cell. From equation (17), it is obvious that a high efficient solar cell will have a high short-circuit current, I_{SC}, a high open-circuit voltage, VOC, and a fill factor, FF, as close as possible to 1.

I_{sc} is proportional to internal current collection efficiency and light-generated current. The internal current collection efficiency related to the recombination velocity and carrier lifetime. For an ideal case the recombination velocity tend to be 0 and lifetime infinite. While the higher light-generated current, equation (6), indicate the solar cell should be least grid shadow, minimum reflectance and the band gap of the semiconductor material can absorb the solar spectrum as much as possible.

V_{OC} is the open circuit voltage (for simplicity the diode 2 that has less effect for a good solar cell is ignored) which can be written as:

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{sc} + I_{01}}{I_{01}}\right) = \frac{kT}{q} \ln\left(\frac{I_{sc}}{I_{01}} + 1\right) \tag{18}$$

From this equation (18), it is clear that V_{oc} depends on saturation current and light-generated current. While I_{sc} typically has a small variation, the key effect is the saturation current.

Therefore through the reducing of I_{o1} can improve the open circuit voltage. I_{o1} can be reduced by minimizing the recombination velocity.

To obtain parameter fill factor (FF) needs extra information, see equation (15). A more commonly used expression for the FF can be determined empirically as [12]:

$$FF = \frac{V_{oc} - \ln(V_{oc} + 0.72)}{V_{oc} + 1} \tag{19}$$

Increasing the V_{oc} can improve the fill factor. To sum up, there are two ways to optimize a solar cell performance:

1. Minimization of recombination rates throughout the device
2. Maximization of the light generated current

The detail methods will be discussed in Chapter IV.

2.6 Resistance Effect

The I-V characterization above neglects the resistance in a real solar cell. A modified model with the series resistance and shunt resistance shows in figure 12

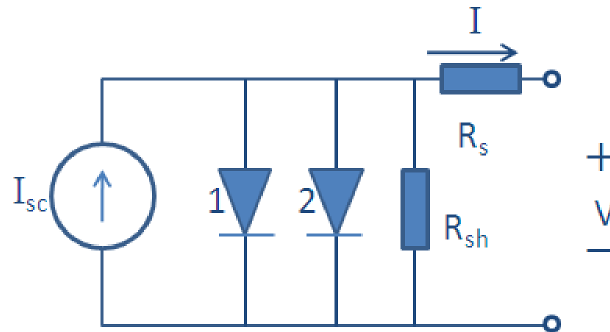


Figure 12 Modified circuit model of solar cell

So the equation (14) becomes like this:

$$I = I_{SC} - I_{01}\left(e^{\frac{qv}{kT}} - 1\right) - I_{02}\left(e^{\frac{qv}{2KT}} - 1\right) - \frac{V + IR_s}{R_{sh}} \tag{20}$$

The shunt resistance does not affect the short circuit current but reduce the open circuit voltage. The series resistance however does not change the open circuit voltage but reduce the open circuit current. Series resistance comes from the metal contact of the grid and transverse flow of the current in emitter to front contact. This can be minimized with innovation design of solar cell. While the shunt resistance typically due to manufacturing defects, rather than the design of solar cell. A low R_{sh} will provide an alternate current path for the light-generated

current that leads to power losses. The effect of R_s and R_{sh} can be illustrated by figure 13 [10]

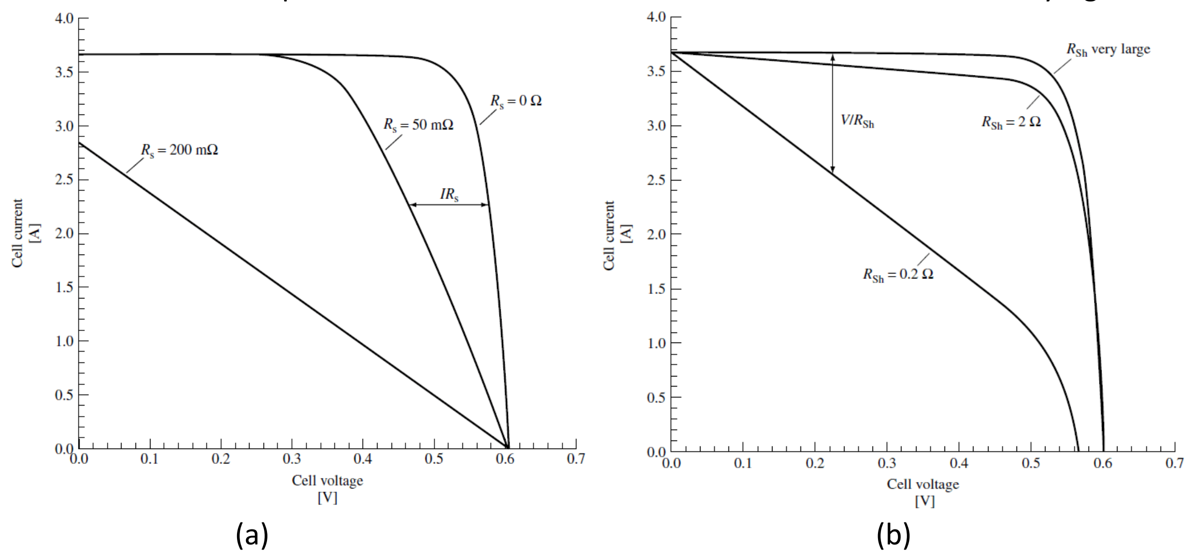


Figure 13 (a) Rs effect of the cell performance (b) R_{sh} effect of the cell performance

2.7 PV cells

2.7.1 Bulk crystalline silicon solar cell

Bulk crystalline silicon solar cells dominate a large market in PV industry as mentioned before. There are many reasons of how this dominance occurs. Firstly, at the starting development of solar cell it was based on Si. From that time most investments of solar cells focused on Si. Now people understand more of the properties and technology of Si, meanwhile tremendous scientific and technical infrastructure for Si have already been built up. Secondly Si is one of the richest elements on Earth. In addition it is non-toxic and stable.

Monocrystalline silicon are mainly made through a technique called Czochralski (Cz)i process in industry. And in laboratory Float-zone silicon is always used for high efficiency but expensive. Poly- or multicrystalline silicon (poly-Si or mc-Si) made from cast square ingots — large blocks of molten silicon carefully cooled and solidified. Poly-Si cells are cheap to produce than single crystal silicon cells and also with a considerable efficiency.

Although the bulk crystalline silicon solar cells keep a high efficiency and technique well developed compare to other types of solar cell, its cost is still high, mainly from the silicon materials, modules. Commercial Si solar cells have a present wafer thickness of 250 to 350 µm for reasons of mechanical stability. A thickness of only 60 to 100 µm has been calculated to be the physical optimum thickness for silicon solar cells [13]. So nowadays the researches for thinner thickness silicon solar cell are undergoing.

2.7.2 Thin film solar cells

When the bulk silicon solar cell technology is well established, scientists however develop another different PV technology---thin film solar cell. The crystalline silicon is often referred to as the first generation photovoltaic technology, while the second generation photovoltaics consists of thin film solar cell materials such as amorphous silicon (a-Si), thin film crystalline silicon, CdTe, CIGS, and DSC. In bulk crystalline solar cell the cost of silicon wafers cost around 40% of the total fabrication cost. Also as direct band gap semiconductors the thin film semiconductor materials have much higher absorption coefficient than silicon. Due to the thinner of materials is required, expensive semiconductor material is thus reduced, or on the other hand, more expensive semiconductors can be used in the thin films. Clearly just reducing the cell thickness will result in reduced absorption because the light will penetrate the substrate without being absorbed. Special structure design is needed to trap light.

Thinner wafers conserve material and also offer a performance advantage by decreasing the bulk-carrier recombination within the solar cell. Hence, for a given material quality of the substrate, a reduction in the cell thickness can result in improving the open-circuit voltage (V_{OC}) and the fill factor (*FF*) of the solar cell. Thus surface recombination becomes an important component of the total recombination.

3 IV Performance optimization

As mentioned in chapter II, there are two ways to optimize a solar cell performance: minimization of recombination rates throughout the device or maximization of the light generated current. Regarding these two fundamental theory result, researchers invented many ways to improve the solar cell efficiency. The traditional solar cells have several drawbacks that reduce efficiency. For example, the traditional solar cell has the emitter on front side, and with the metal grid contact on top from which the generated electrons are collected. However the shadow of the metal grid reduces the amount of light penetrating through the solar cell. Also the flat front surface will reflect the incident sunshine around 30%, a better front surface need to be designed to reduce the reflection.

3.1. Structure design

For a higher light-generated current, it is necessary to minimize the shadow factor. There is a novel structure of solar cell called back contact solar cells: interdigitated back contact (IBC) solar cell, emitter wrap through (EWT) solar cell. This type of solar cell has a back contact emitter, so the metal contact is at the rear side which can avoid the shadow factor comparing to the traditional structure. IBC solar cell was the structure we studied and applied in this project. It is sketched in Fig 14.

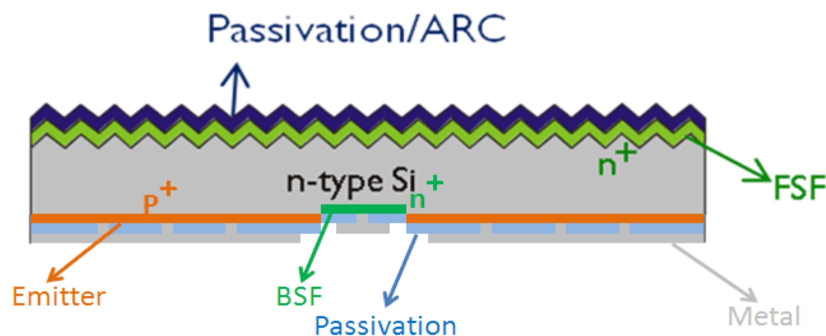


Figure 14 Simple sketch of IBC structure

First designs of IBC solar cells were investigated by Lammert and Schwartz [14]. The development and commercialization on monocrystalline silicon were carried out by Swanson et al. and the SunPower Corporation. Meanwhile back contact solar cells are in production by SunPower in the range of 60MWp/a [15]. The prime reason for the lack of interest thus far is the high material quality required by the device. Diffusion length must be several times the

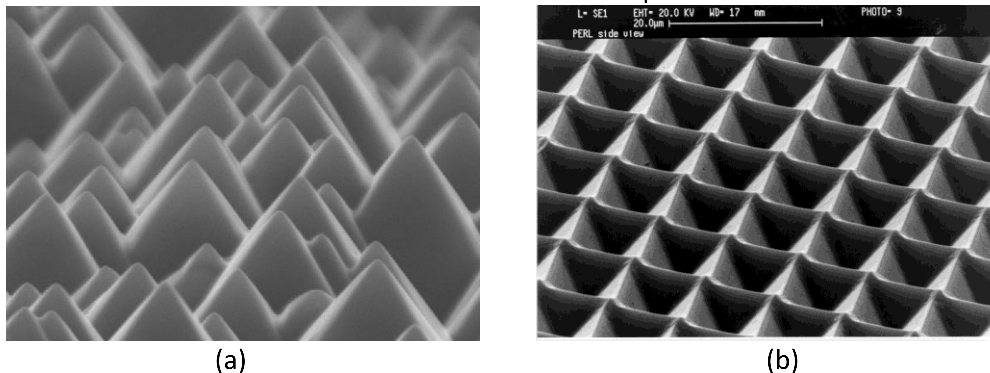
distance of any point in the cell to the nearest collecting junction. Another requirement of the IBC type cell is excellent front surface passivation, since the junction is on the back and most photo generation occurs at the front. This surface passivation must remain stable as well. While the tolerance to common impurities of n-type substrate will potentially increase the minority carrier diffusion lengths compare to p-type crystal Si substrate [16]. In addition n-type substrate avoids the boron-oxygen related light-induced degradation which will happen for p-type based Cz crystal silicon[17]. This is why we use n-type substrate for IBC solar cell.

3.2 Light absorption enhancement and recombination minimization

Other ways to increase the conversion efficiency are to enhance the light absorption and reduce recombination through texture and coating.

3.2.1Texture

The flat surface of silicon will reflect about 30% of the incoming light. The common method of reducing reflection is to build up the random pyramids structure. There are several ways to achieve pyramidal-like surface texture, plasma etching, mechanical engraving and chemical etching. In industrial the anisotropic wet chemical etching of <100> silicon using the solution such as NaOH, KOH, Na_2CO_3 is wildly used as a standard method [18, 19]. In laboratory another type of surface knows as “inverted pyramid” texture is used for better light trapping. Instead of upward pyramid in random pyramid etching, this method etches down into silicon surface. Both are shown in the picture below.



(a) (b)

Figure 15 (a) random pyramid texture (b) inverted pyramid texture

3.2.2 Coating

There are always anti-reflection and passivation layers coated on the solar cell device. Sometimes a back reflecting coating is also needed.

Normally there is anti-reflection coating on the surface of the solar cell which can reduce surface reflection from 30% to 11% [20]. While if it needs to reduce the reflection furthermore,

a three layer coating ($In(P0_3)_3/Al_20_3/MgF_2$)technology is used [21]. It can yield an overall theoretical reflectance of less than 2%.

The grain boundaries and intragrain defects in silicon which is the dominate parameter that reduces the carrier lifetime and diffusion length in the materials. In order to get higher efficiency solar cell the electrically defects have to be passivated both the emitter and bulk of the solar cell. Silicon dioxide grown into silicon surface at high temperature is accepted to a very useful way to passivate the surface [22, 23]. However SiO_2 does not passivate the bulk defects in multicrystalline silicon [24]. In addition, SiO_2 oxidation requires high temperature which will create other defects. For a lower temperature deposition a technology called PECVD with SiN as passivation material is proved to with a good performance by Lauinger et al [25, 26]. Al_2O_3 passivation is an even lower temperature and faster process however has a poor passivation performance compare to the other two methods.

In this project SiO_2 and Al_2O_3 passivation are applied. Thermal oxidation is the process of silicon dioxide creation from pure silicon as a result of a chemical reaction of silicon and oxygen. Two different production techniques can be distinguished; dry and wet oxidation. A thin film of Al_2O_3 for passivation is achieved by atomic layer deposition (ALD). It is known to provide good passivation on lowly doped p-type surface [27]as well as on highly boron doped p+ surface(in this project it is in this condition)[28, 29].

4 Experimental

The experiment goes in the following order shown in figure 19.

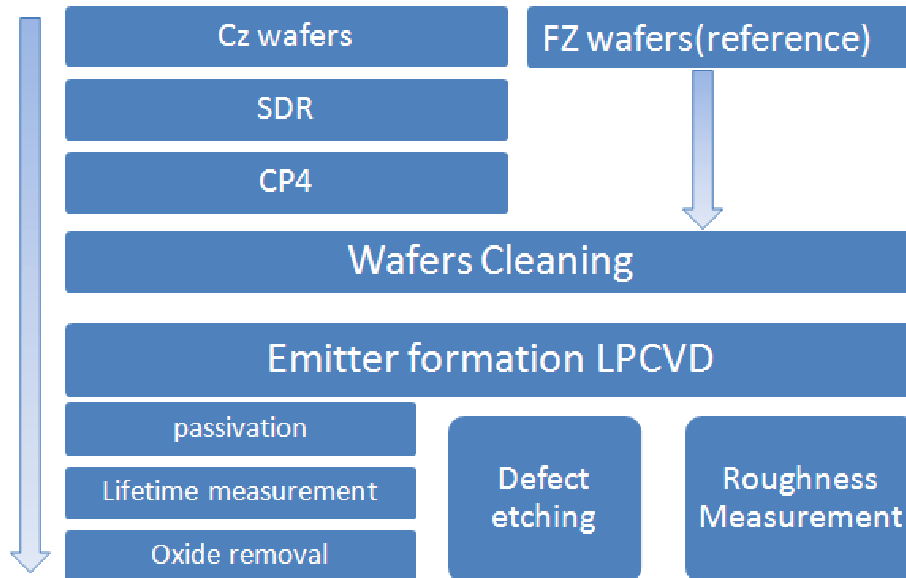


Figure 19 the work flow of the project

4.1 Saw damage removal (SDR)

The Cz wafers coming from the manufactory always have a very rough surface induced by wire saw process that cut ingot to wafers. This thin layer contains many defects which have a negative influence of the solar cell performance. So normally the starting step to fabricate a solar cell in industry is the saw damage removal. There are two commonly methods for SDR wet etch and dry plasma etch. The wet etch is used commonly in industrial. The alkaline etchant is traditionally used for SDR in wet etch which is a 20~30wt.% NaOH or KOH solution with a temperature 80~90 ^{o}C. This process is anisotropic which etches the Si <111> planes more slowly than other orientation [30]. It is an easy control process, but with a higher reflectance after SDR. In the case of acid etchant, it is a mixture of HF and HNO_3. This process involves isotropic chemical etching that is why after SDR it has a lower reflectance. But the concentration of the solute and Si fluctuate the etching rate which needs to be controlled [31]. In addition to reflectance reduction, acid etching reduces the contact resistance of the metallization on a solar cell as well [32]. Dry plasma etching has two substantially chemistries suitable for etching and texturing: Chlorine-based, and fluorine-based [33].The dry plasma etching is more often applied in laboratory because of the high expense.

In this project, traditional alkaline solution was used for SDR. The solution is a mixture of 2kg KOH and 10 liter Di-water, heated to 80-85°C. The beginning step wafers are 12.5×12.5cm^{2} N-type monocrystalline silicon (doping level 2e15 at/cm^{3}) with thickness of 200 µm and <100> orientation. These wafers were placed in cassettes and immersed in the solution for 4 minutes to remove around 10µm per side. After rinsing the wafers were neutralized in 5wt% HCl solution for 10 minutes. After SDR these wafers were divided into 4 groups, A, B, C, D.

4.2 CP4 Polish

After SDR the roughness of the substrate wafers was still not good enough for emitter formation with CVD which needs flatter substrate for better quality. To investigate how much to polish the wafers and the influence of the wafers roughness to solar cell performance is one of the project objects.

To reduce the roughness of the wafers another solution called CP4 acid etchant (HF, CHCOOH, HNO_3) was induced. It is primarily used to polish the silicon wafers with rough surface and edge damage. Also this kind of polishing is anisotropic process and can decrease the reflectance. It is a complex etching reaction, but it can be understood in a simple way that the nitric acid oxidizes the silicon surface and the HF removes this oxide. The acetic acid is working as diluents that improve the polishing effect of the etchant by preventing dissociation of the HNO_3. During the reaction it is normal to see brown gases which comes from the oxidation of one of the products NO. The reaction can be simply written as:

$$4HNO_3+18HF+3Si \rightarrow 3H_2iF_6+4NO+8H_2O \qquad (21)$$

$$2NO+O_2 \rightarrow 2NO_2 \qquad (22)$$

The polishing degree of the four groups shows in table 1

Group	A	B	C	D
Silicon removed(µm/side)	0	5	11	20
Thickness of Si substrate(µm)	180	170	158	140

After the polishing, these four groups of wafers were diced into the size of 10×10cm with label on each wafer. Because one of the following steps called emitter formation was performed in Epsilon2000 in which only a size of 10×10cm can be processed for square wafers.

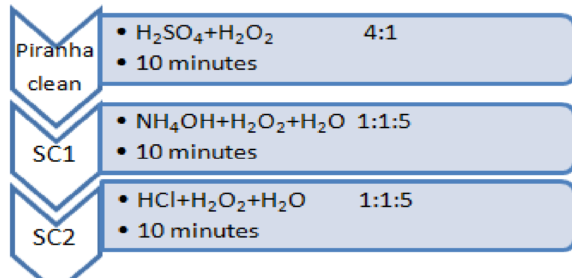


Figure 20 wafer cleaning process

4.3 Wafer clean

The cleanness of the substrate wafer is critically important not only for the PV field but the whole semiconductor devices. There are several types of contamination: particles, metallic impurity, organics, native oxide and other films. It is well known the presence of contamination on the wafer surface will affect the device performance and reliability. Especially in this project, an emitter was formed by CVD which needs extremely clean silicon substrate. So the wafer cleaning is a crucial step. In this experiment the wafers were processed through a standard cleaning called full RCA cleaning. RCA cleaning is often applied for the wafers which are going be performed under high temperature process.

Full RCA mainly contains three parts: piranha cleaning, SC-1 cleaning and SC-2 cleaning. Piranha solution is a mixture of concentrated sulfuric acid and hydrogen peroxide used to remove heave organic (photoresist) on substrate. Here a solution of 4:1 96% concentrated sulfuric acid to 30% hydrogen is used to clean the wafers. The resultant temperature of piranha solution when mixing H_2SO_4 with H_2O can be up to 120°C, while a temperature of 80°C is preferred in this experiment. SC-1 cleaning is to remove the particles and light organics. The solution contains NH_4OH, H_2O_2 and H_2O with a concentration of 1:1:5 which heated up to 75 or 80°C. And heavy metallic removal is the purpose of SC-2 cleaning. This step is performed with a 1:1:5 solution of HCl+H_2O_2+H_2O at 75 or 80°C. All of the three main steps lasted for 10 minutes in the experiment. And actually a process of "rinsing → around 60 seconds 5%HF dip →rinsing" was performed following each of the three main parts. The HF dip is to remove the silicon oxide, native oxide film and polymer before the cleaning of next step. When cleaning finished, it is ready for epitaxy.

4.4 Emitter formation by CVD

The epitaxial of silicon for emitter formation were deposited in Epsilon2000 CVD reactor. The working principle process is shown in figure 21. Process gas is injected from the right side tubes which have screws to control the gas flow speed. There are halogen lamps surround the wafer that are used to control temperature. The wafer is placed on a suspended hold which can rotate in order to get a uniform deposition. The exhaust gases come out from the left side. With the desired 100Ω/cm^2 sheet resistance of the epitaxial emitter, table 2 shows three doping levels of different thicknesses which were the expected results after running in Epsilon2000.

Rsheet Ω/cm^2	Doping level(at/cm^3)	Thickness(μm)
100	5E18	1.454
100	2E19	0.512
100	8E19	0.155

Table 2 The expected emitter doping level and thickness

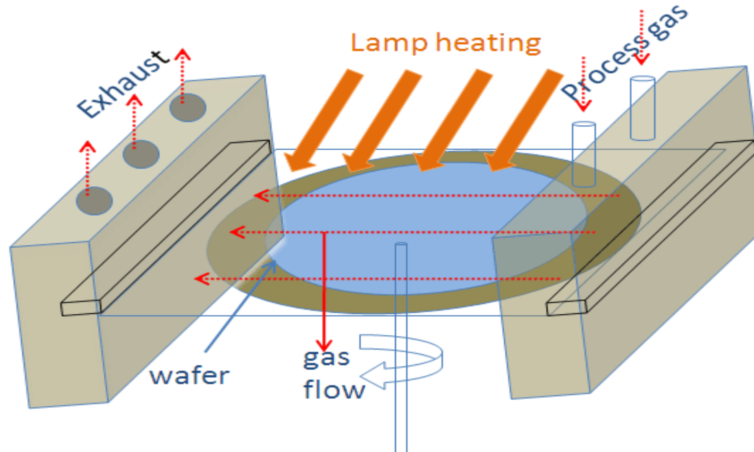


Figure 21 Scheme of Epsilon2000 working process

Desired Emitter		H_2 Bake	Deposition		
Doping level (at/cm^3)	Thickness (μm)	60 slm H_2 5min 950°C 40torr	60 slm H_2 500 sccm DCS 100/100/2 sccm 1% B_2H_6 40 torr	Time (sec)	Temp (°C)
5E18	1.454			138	950
2E19	0.512			45	950
8E19	0.155			50	850

Table 3 The recipes of the boron epitaxy emitter. *. slm-standard liter per minute;DCS-SiH_2Cl_2

The emitters were deposited on both sides which were to form a symmetric structure for the latter lifetime measurement.

4.5 Roughness measurement

Roughness of the wafers is key variable parameter to the experiment. One of project goal is to learn the roughness degree for better cell performance. One piece of each group (not including reference samples which is mirror polished) was sent to measure the roughness by optical profilometer both before and after CVD epitaxy. Optical profilometer has a vertical resolution usually in the nanometer, while lateral resolution is usually poorer that is limited by the wavelength of the light.

4.6 Defect density measurement

The defect in the emitter is the recombination center of the generated hole and electrons mentioned in chapter II which can badly influent the performance of a solar cell. So the defect density of emitter will be one of the parameters that can indicate the quality of the solar cell. There are several types of defects in epitaxial layers, epi stacking fault, growth hillock, dislocation, stacking fault from bulk and epi spike [33,34].Normally four methods can measure the defect density. Transmission electron microscopy, X-Ray topography and small angle neutron scattering, these three methods' working principle are based on the different optical response where the defects exist.   In industrial the last method called chemical preferential etching is substantially used for defect density measurement. It is a fast and cost-effective way. Due to the different etching rate at the defect, the etch pit can be observed after chemical etching which is normally larger than the defect itself.

Depending on the wafer crystal orientation and etching purpose, SECCO, WRIGHT, SIRTL and SCHIMMEL defect etching solution can be chosen [35, 36, 37]. Here we used the WRIGHT etching solution which is ideal for <100> orientation. It is a mixture of 1)45g CrO_3 to 90ml H_2O; 2) 6g $Cu(NO_3)_{5/2}H_2O$ add to 180ml H_2O; 3)90ml HNO_3 and 180ml CH_3COOH&180ml HF [38]. Sample preparation is important for defect etching, because the contamination and rough surface of the sample will cause etching too much or etching the part where no defect exists. So the wafers even after CVD was still not flat enough to perform defect etching. A process of mechanical polishing was involved before defect etching. Depending on the roughness degree of the four groups A, B, C, D, the polishing time is different (the reference samples which were mirror polished wafers didn't have this process). When sample preparation was finished, these samples were all immersed in the Wright solution for 25 seconds. After cleaning the wafers, observed the defect under optical microscope and calculated the defect density.

4.7 Passivation

For high efficiency solar cells low surface recombination and high effective lifetimes are both significantly important. Thermal oxide films grown at high temperatures and silicon nitride layers deposited at low temperatures are generally used for the surface passivation of solar cells. SiO_2 passivation has several advantages. It can suppress the recombination come from the surface defects which is also stable. The passivation can also improve the internal reflection which enhances light trapping. Furthermore it allows for laser fired contacts that could reduce contact resistance. A forming gas annealing can lower the density of interface state which always follows the thermal oxidation. [39]

In the experiment, two methods of passivation were studied, SiO_2 passivation and ALOx oxide passivation. In order to find out the better temperature for passivation, three different

temperatures of 850°C, 950°C, 1050°C were applied to SiO_2 passivation in the furnace system. Usually a forming gas annealing is required to further reduce the recombination velocities at the interface. It is a gases mixture of H_2 and N_2. This process was done at 450°C. AlOx oxide passivation was done with oxide thickness of 15nm/side and 30nm/side using Savannah ALD. This process is a low temperature process at 200°C. Followed by the passivation, lifetime was measured. Then comparison of these 5 different conditions of passivation could find out the better method.

4.8 Sheet resistance, SRP measurement

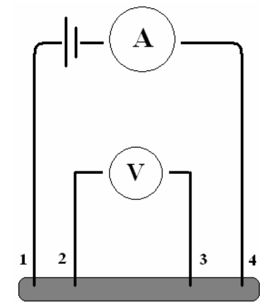


Figure 22 4pp working principle

Sheet resistance is measured by 4-point probes method system. It is an electrical impedance measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements than traditional two-terminal (2T) sensing. The basic principle structure is shown in figure 22 .The accuracy of the technique comes from the fact that almost no current flows in the sense wires, so the voltage drop *U=RI* is extremely low. Wafer sheet resistance were measured several times. For most wafers, Rs were mesaured three times: after epitaxy, after oxide removal and after AlOx removal. In the case of thermal infleunce study, the wafers took 3 times of oxidation. Cz wafers were measured after three different temperature oxidation, 1050°C, 950°C, 850°C. And for the reference FZ wafers Rs were measured after each oxidation at 1050°C, total in three times. Samples after oxidation were sent to spreading resistance profiling measurement which is a technique used to analyze resistivity vs. depth in semiconductors.

4.9 Lifetime measurement

Measurements of minority-carrier lifetime in silicon wafers are extremely valuable for process control and device optimization as well as for material and device physics research. Imaging techniques for measuring lifetime that emerged over the last few years include Infrared Lifetime Mapping (ILM) [40], Carrier Density Imaging (CDI) [41] and Electroluminescence (EL) Imaging [42]. While for ILM/CDI most spatial information is obviously lost. In addition the wafer must be heated to a temperature of ~70 degrees in order to achieve that sensitivity and those techniques are also affected by both minority carrier trapping and by excess carriers in space charge regions. In the case of EL imaging it requires electrical contacts to the device and as such it is only applicable to fully processed solar cells. Secondly, the quantitative interpretation of the images is complicated by series resistance effects [43] Photoluminescence (PL) imaging is demonstrated as a fast characterization tool allowing variations of the minority carrier lifetime within large area silicon wafers to be measured with high spatial resolution and with a data acquisition time of only one second. Injection level dependent quasi-steady-state Photo Conductance (QSS-PC) lifetime measurements on silicon are unaffected by these artifacts [44,

45]. QSS-PC is applied for lifetime measurement in this project. Wafers were measured after the different conditions of passivation.

5 Result and discussion

5.1 Impact of starting substrate surface

The four groups of wafers firstly were viewed by SEM to see the roughness of the surface after SDR and CP4 polishing, shown in figure 23. It is very obvious to see group A which is only processed SDR is the roughest surface wafers, and group D the ones polished longest time is much more flat. While for group B and C it is comparability flatter than group A. In order to know the detail quantity roughness, small pieces from each group were measured by optical profilometer before and after epitaxy. The result shows in figure24 and table 4 and 5. Figure 24 is a 3D picture that shows the surface of wafer from group A. The regions with color from red to blue go to rougher.

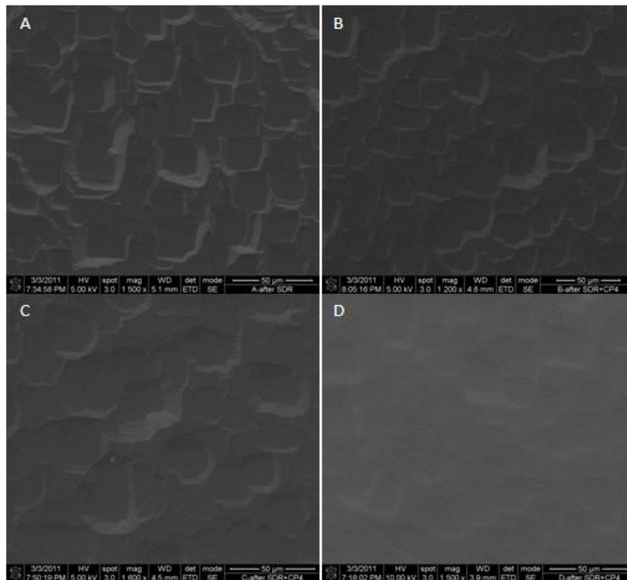


Figure 23 SEM image of roughness of the 4 groups. magnification :A and D 1500×, B and D 1600×

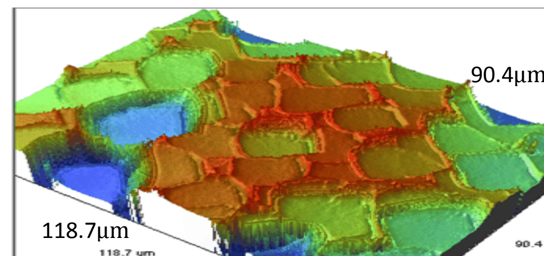


Figure 24 3D picture of surface roughness for the sample from group A

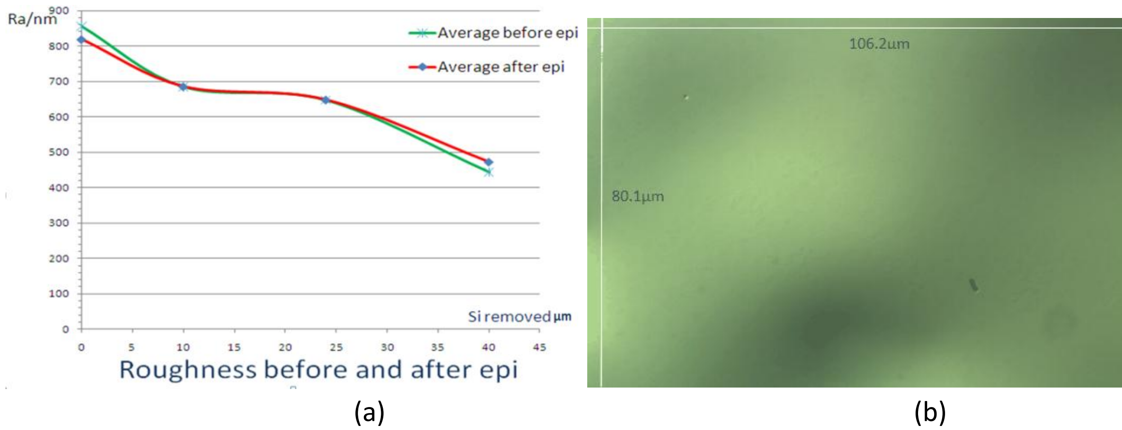
The values of roughness in the table 4 and 5 are an average vertical distance at the center or edge of the sample under different magnification. As expected the results show that the wafers with longer time of chemical polishing will have a flatter surface. The trend of average surface roughness Ra vs Si removal thickness was shown in figure 25(a). We can see that the roughness significantly decrease at the beginning if we process chemical process after SDR. After removing 10µm Si in total by CP4 the roughness reduces more slowly. Compare the value of group D. The roughness degree is already very close to the mirror polished reference wafers (R_1 and R_2). The result also shows that in this case of deposition, the roughness of epitaxial layer is close to the starting substrate roughness.

Substrate	2x Ra[nm]	5x Ra[nm]	10x Ra[nm]	20x Ra[nm]	50x Ra[nm]	Average	Std Devi
A1_centre	807	850	862	832	959		48.59
A1_edge	847	898	891	834	776	855.6	
B1_centre	674	701	674	759	654		51.51
B1_edge	724	727	724	640	572	684.9	
C1_centre	650	654	639	711	506		111.95
C2_centre	751	753	724	702	382	647.2	
D1_centre	455	437	399	394	344		49.05
D2_centre	495	502	472	448	495	444.1	

Table 4 Wafers surface before epitaxy

Substrate	2x Ra[nm]	5x Ra[nm]	10x Ra[nm]	20x Ra[nm]	50x Ra[nm]	Average	Std Devi
A1_centre	837	829	842	857	629		74.15
A1_centre	825	845	837	909	776	818.6	
B1_centre	736	713	736	745	469		112.96
B1_centre	759	770	744	705	480	685.7	
C1_centre	640	645	620	638	596		31.45
C2_centre	628	661	668	705	680	648.1	
D1_centre	508	476	508	465	419		43.97
D2_centre	528	518	456	458	393	472.9	
R1	494	481	474	495	415		46.85
R2	484	470	442	401	355	451.1	

Table 5 Wafers surface after epitaxy



(a) (b)

Figure 25 roughness of wafer surface before and after epitaxy

Table 6 Defect density of the four groups with three different doping levels.

Group \ Ns	5E18 at/cm^3	2E19 at/cm^3	8E19 at/cm^3
A	4.572*10^3/cm^2	2.939*10^3/cm^2	3.527*10^3/cm^2
B	5.878*10^3/cm^2	1.427*10^4/cm^2	7.054*10^3/cm^2
C	3.527*10^3/cm^2	7.481*10^3/cm^2	3.206*10^3/cm^2
D	2.351*10^3/cm^2	2.939*10^3/cm^2	2.351*10^3/cm^2

The samples for defect measurement immersed in WRIGHT solution for 25 seconds. After rinsing defects were observed under optical microscope with a magnification of 100×. The defects in the emitter will increase the surface recombination, thus a low defect density is more preferable. Figure 25(b) shows the defects of the wafer from group B. The picture was taken under the optical microscope at 10 random regions. Defect density is given by:

$$N_d = \frac{Number\ \ of\ defects\ \ in\ total}{Sum\ of\ observed\ \ regioin\ \ area} \qquad (23)$$

Lifetime was measured by QSSPC. The wafers (for roughness study) with different emitter doping levels (R01-5e18 at/cm^3, R02-2e19 at/cm^3, R03-8e19 at/cm^3) were passivated by SiO_2 through thermal oxidation at 950°C and1050^{o}C. The results of emitter saturation current (Jo_e) against roughness were shown in picture .

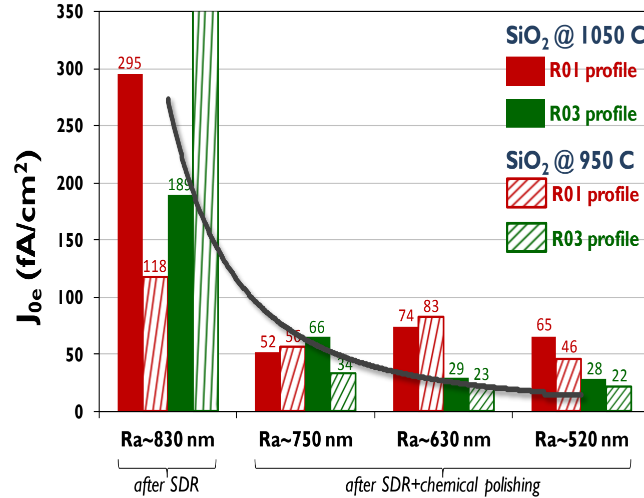


Figure 26 J_{0e} for boron epitaxial emitters passivated with thermal oxide (at 950 C and 1050 C) as a function of substrate roughness

Group A with a average roughness of Ra 830nm. The Joe drops dramatically after polished even wafers were lightly chemical polished of 5µm/side (group B) compare to the wafers of group A which only have SDR. This can indicate that the starting material substrate surface is very important to the solar cell performance.

5.2 Thermal oxidation study

5.2.1 Effect of the Oxidation Temperature

To study the effect of temperature on emitter passivation three different temperatures of 850°C, 950°C, 1050°C were applied to SiO_2 passivation in the furnace system. The results of boron emitter spreading resistance profiling(SRP) after the three temperatures of oxidation were shown in figure 27. Before passivation the emitter after boron epitaxy is Ns $5*10^{19}$ at/cm^3 and R_{sheet} 90Ω/sq. After the SiO_2 passivation the emitter doping level decreased due to the boron diffusion under high temperature, higher temperature get lower doping level. There is also a trend to be detrimental retrograde profile due to boron depletion at boron doped silicon/ silicon dioxide interface [46, 47, 48]. Variations of the boron diffusivity in the oxide due to temperature or ambient effects may have an influence on the boron profile near the silicon/oxide interface. Higher oxide temperature may be the factor of the retrograde profile enhancement [49].

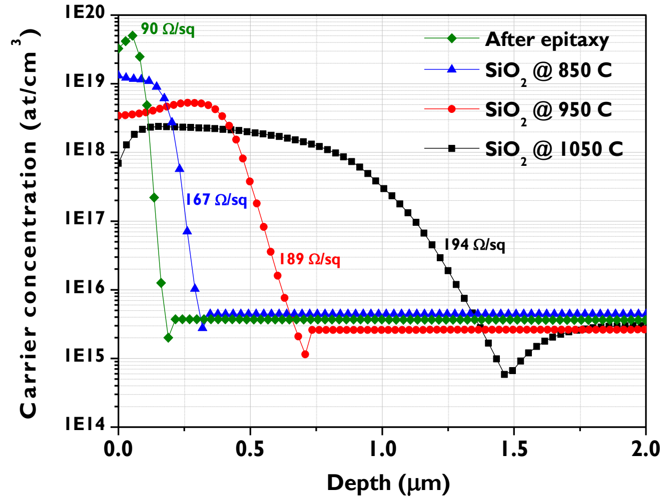


Figure 27 Boron SRP profiles after thermal oxidation at different temperatures

5.2.2 Effect of the Number of Oxidations

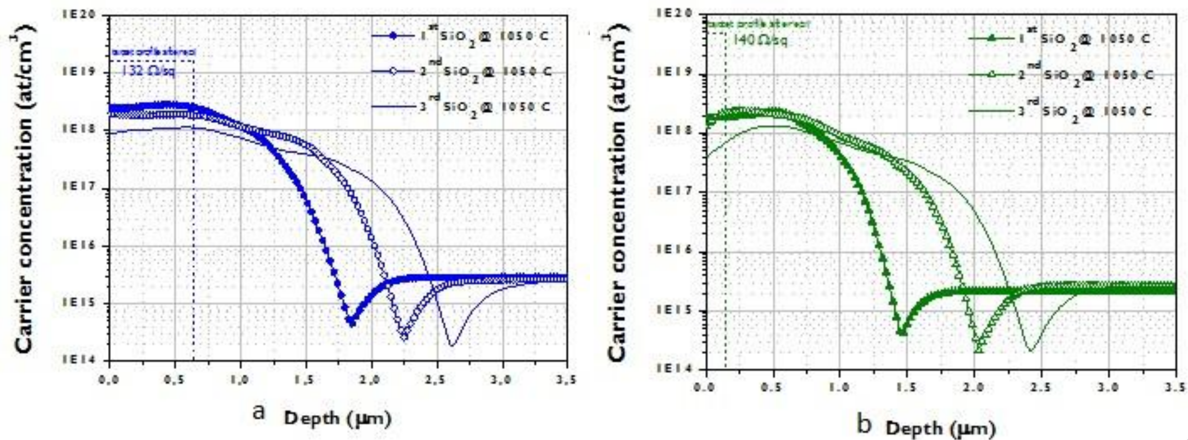


Figure 28 Boron SRP profiles after subsequent oxidations on the same boron emitter after epitaxy: (a) N_s~$1{\cdot}10^{19}$ at/cm^3 and (b) N_s~$5{\cdot}10^{19}$ at/cm^3.

There are several times of oxidation when fabricating a crystal Si solar cell. In this research three times of oxidation (oxide removal in between) for two epitaxial emitters with a box profile and a similar sheet resistance (R_{sheet}~130-140 Ω/sq) but different N_s (~$1{\cdot}10^{19}$ at/cm^3 and ~$5{\cdot}10^{19}$ at/cm^3) were applied to investigate how the boron doping profile changes. SRP profiles (see in Fig.28) after each oxidation show that there is significant boron depletion from silicon at the *silicon/oxide* interface for the higher doping emitter N_s (~$5{\cdot}10^{19}$ at/cm^3), while no depletion is observed for the box profile with lower N_s (~$1{\cdot}10^{19}$ at/cm^3) after epitaxy.

It point out that starting from a box profile with N_s in the range of 10^{19} at/cm^3 after epitaxy, oxidation temperature over 950 ^{0}C can decrease N_s in one order of magnitude. Only low

temperature oxidation (<950 ^{0}C) could keep the target N_s around 10^{19} at/cm^3. Moreover, high temperature oxidation (>950 ^{0}C) suggests a higher trend for retrograde profiles at the emitter surface. The oxidation temperature has also an influence on the junction depth which is more significant at higher temperature.

5.3 Emitter Performance with AlOx ALD Passivation

In part 5.1 it has shown the performance of emitter after SiO_2 passivation under different oxidation temperature. However this is a long time and high temperature process. To avoid these disadvantages, AlO_x ALD passivation is an alternative technology. ALO_x ALD passivation is used for lowly doped p-type surface or highly boron doped p+ surface mentioned in chapter 3.

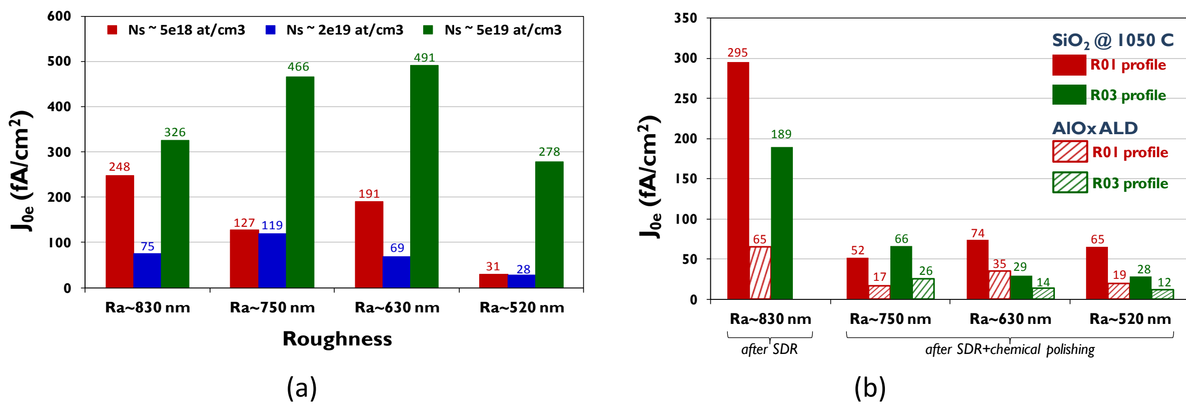


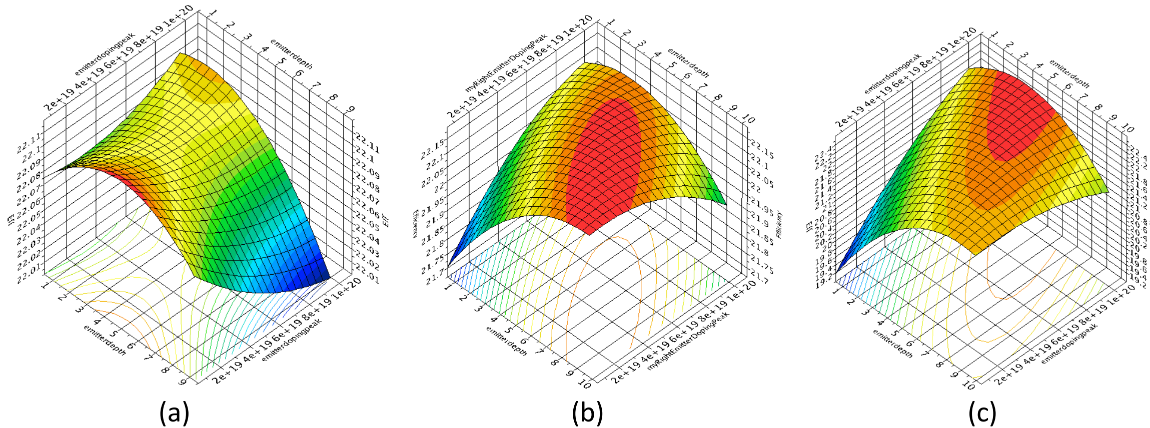
Figure 29 (a) Effect of Ns for AlOx ALD; (b) SiO_2 Passivation vs AlO_x ALD

A thickness of 30 nm was passivated on the samples. The Jo_e results shows the AlOx ALD outstanding performance of passivation for the substrate Ra< 750nm of CZ materials. Figure 29 (a) figure out that although ALO_x ALD passivation can be used for highly boron doped p+ surface but a suitable doping concentration Ns should below $2*10^{19}$ at/cm^3. Picture (b) clear shows ALO_x ALD passivation have a better performance than thermal oxide passivation. These values confirmed for 15 nm thick AlO_x and oxide passivation at 950 ^{0}C, are comparable to the results reported in literature for boron diffused and implanted emitters [28-29, 50].

5.4 Simulation

Both TCAD Sentaurus and Optimus (optimization) software were used to investigate the trend of output efficiency regarding three types of emitter profile: Box, Gaussian, and Complementary Error Function. Depending on the output efficiency, the emitter doping level and depth are investigated to achieve the suitable sheet resistance. Base on an IBC model built with TCAD by IMEC researchers, these three shapes of doping profile were introduced into the model. An experiment with setting parameters can be simulated to get the values of the IBC solar cell IV characterization parameters. However each experiment have to set an exactly value

to run the experiment which cannot run automatically with a certain range that why the Optimus is involved in this simulation work. With the help of Optimus, it can make the Sentaurus run the simulation with the setting range of the parameters. The results show in figure 30.



(a) (b) (c)

Figure 30 Efficiency performance vs emitter depth and peak doping concentration under three doping shape: (a) box profile (b) Gaussian profile (c) ERFC profile

Simulation went under the range of Emitterdepth 0.5~10um; Emitterdopingpeak 5.0E+18~1.0E+20 at/cm^3. The result of maximum efficiency point is shown in table 7.

Profile	Emitterdepth(um)	Dopingpeak at/cm^3	Jsc mA	Voc mV	Eff %	FF %
Box	4.9760	6.74e+18	40.36	0.6864	22.13	79.87
Gauss	9.3466	2.85e+19	40.43	0.6859	22.17	79.95
Erfc	9.7489	1.59e+19	40.47	0.6865	22.19	79.87

Table 7 Maximum Efficiency condition of Emitterdepth and Dopingpeak for the three profile shape

The result shows that at which value of the parameters can get the highest efficiency together with other three performance parameters. However they are under different emitter sheet resistance due to the diverse profile shapes. So the performances of different profile shapes are not comparable. A further simulation should be run to illustrate that under the same emitter sheet resistance how the solar cell performs which is the future work.

6 Conclusions and outlook

The study of the substrate roughness Ra effect on the quality and performance of the boron epitaxial emitters, the results proved that only a slight degree of polishing after SDR, just to reach a substrate Ra≤750 nm, would be enough to achieve good J_{0e} values (<<100 fA/cm^2) for these emitters (N_s~10^{18} at/cm^3 and R_{sheet}~140 Ω/sq) on CZ material with thermal oxide passivation. Nevertheless, much better results for the J_{0e} of these emitters can be measured when using AlO_x ALD passivation. In general, for Ra≤750 nm, J_{0e}≤20 fA/cm^2 can be achieved for boron epitaxial emitters (N_s~10^{18} at/cm^3 and R_{sheet}~140 Ω/sq) on CZ material.

The study of the thermal budget effect on the boron epitaxial emitter profile pointed out the depletion of boron from silicon at the *silicon/oxide* interface at high oxidation temperature (>950 ^{0}C) and for long or subsequent oxidations on the same emitter. These retrograde profiles are detrimental for the solar cell performance. Therefore, a more simple and direct design and integration of the boron emitters would prefer passivation schemes introducing low thermal budget (<950 ^{0}C). Moreover, epitaxy would allow a straightforward formation of the required emitter in a 1-step doping process.

The good performance of our present passivation scheme with AlO_x ALD (including a last FGA) is kept up to N_s~$2\cdot10^{19}$ at/cm^3 (J_{0e}≤20 fA/cm^2 for Ra≤520 nm). For N_s~$5\cdot10^{19}$ at/cm^3, the J_{0e} values go well above 100 fA/cm^2. Hence, further optimization of the present passivation scheme with AlOx ALD would be necessary for boron N_s≥$5\cdot10^{19}$ at/cm^3.

Simulation of IBC cell emitter condition shows the approximately trend how the efficiency changes regarding variable values of emitter depth and doping peak for the three shape of doping profile. To overcome the not comparable data, a method to extract the data that can show the IBC solar cell performance under the same emitter sheet resistance will be one of the future works. Also the IBC model will be update to calculate out more parameter of solar cell, such as Joe, R_{sheet} and R_{sh}.

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