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UVM Based Verification Of 3GPP Chip Rate Processing Unit

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Abstract

Exchange of information in the present world has witnessed a significant progress owing to modern telecommunication technologies, advanced gadgets and powerful computers. Wireless networks are the most popular choice for the obvious reason of connecting people on the move. Cellular technology provides a wide area connectivity and potential of generating higher revenues to the service provider. Universal Mobile Telecommunication System (UMTS) is a 3rd Generation (3G) technology that offers a high speed data access besides conventional voice service. 3rd Generation Partnership Project (3GPP) committee defines the standards for UMTS technology. UMTS uses Wideband Code Division Multiple Access (WCDMA) for radio transmission.

A cellular network infrastructure houses an access point termed as base station to enable radio connectivity to the mobile devices. The base station hardware requires validation to determine its performance and limitation. Specialized hardware is used by Ericsson for testing baseband processing of base station which can emulate multiple mobile terminals. This hardware resembles a Real-time User Equipment (RUE) which is capable of simulating different scenarios of wireless transmission and modes of mobile devices. This test infrastructure encapsulates Digital Signal Processors (DSPs), Field-Programmable Gate Arrays (FPGAs) and other components. One FPGA is used for generating the data needed for transmission to the base station. FPGA performs the physical layer chip rate processing where all the information carrying data and control signals are represented in radio frames. The purpose of this thesis is formal verification of this FPGA based on Hardware Description Language (HDL) simulator.

Specman is a Cadence tool used to create test benches for verifying FPGA and executes the test cases along with a HDL simulator. It provides a standard for defining, compiling and executing a test environment developed in e language. This project uses Specman based verification of the uplink chip rate processing of the FPGA which includes many unit level signal processing blocks. The test bench autonomously generates the necessary inputs, predicts the output using a reference model, monitors the outputs and compares it with predicted output. The sequence of generation of inputs is designed to simulate specific cases defined in 3GPP specification. The device timing, control and configuration information needed is precisely included in test environment. The test results are summarized with coverage information on different combination of inputs tested or occurrence of certain events.

Keywords: UMTS, 3GPP, WCDMA, RUE, Specman, FPGA, Uplink Chip rate processing.

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Abbreviations

1G	1st Generation
2G	2nd Generation
3G	3rd Generation
3GPP	3rd Generation Partnership Project
4PAM	4 Pulse Amplitude Modulation
AICH	Acquisition Indicator Channel
ATIS	Alliance for Telecommunications Industry Solutions
ASIC	Application Specific Integrated Circuits
ARIB	Association for Radio Industries and Businesses
BPSK	Binary Phase Shift Keying
BER	Bit Error Rate
BP	Board Processor
BFM	Bus Functional Module
CCSA	China Communication Standards Association
CRADL	Chip Rate Accelerator Downlink
CRAUL	Chip Rate Accelerator Uplink
CS	Circuit Switched
CCTrCH	Coded Composite Transport Channel
CPRI	Common Public Radio Interface
CN	Core Network
CDV	Coverage Driven functional Verification
CRC	Cyclic Redundancy Check
DCH	Dedicated Channel
DPCH	Dedicated Physical Channel
DPCCH	Dedicated Physical Control Channel
DPDCH	Dedicated Physical Data Channel
DVE	Design Verification Environment
DUT	Device Under Test
DPAD	Digital Processing Adapter board
DSPs	Digital Signal Processors
DUW	Digital Unit WCDMA
DS-CDMA	Direct-Sequence Code Division Multiple Access
DDR	Double Data Rate
DL	Downlink
EDGE	Enhanced Data rates for GSM Evolution
ETSI	European Telecommunications Standards Institute
XHTML	Extensible Hyper Text Markup Language
EMIF	External Memory Interface
FBI	Feedback Information
FPGA	Field-Programmable Gate Array
FIR	Finite Impulse Response

FIFO	First In First Out
FEC	Forward Error Correction
FDD	Frequency Division Duplexing
FDMA	Frequency Division Multiple Access
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile
HDL	Hardware Description Language
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HLR	Home Location Register
HARQ	Hybrid Automatic Repeat Request
HF	Hyper Frame
HTML	Hyper Text Markup Language
ISDN	Integrated Services Digital Network
IMS	Internet Protocol Multimedia Subsystem
MAC	Medium Access Control
MSC	Mobile Switching Centre
MT	Modulation Type
MSB	Most Significant Bit
BFN	Node B Frame Number
OOP	Object Oriented Programming
OVSF	Orthogonal Variable Spreading Factor
PS	Packet Switched
PAR	Peak to Average Ratio
PCH	Physical Channel
PCI	Peripheral Component Interconnect
PRACH	Physical Random Access Channel
PLI	Programming Language Interface
PLMN	Public Land Mobile Network
PSTN	Public Switched Telephone Network
QPSK	Quadrature Phase Shift Keying
QOS	Quality of Service
RAN	Radio Access Network
RNC	Radio Network Controller
RNS	Radio Network Subsystem
RRC	Radio Resource Control
RACH	Random Access Channel
RUE	Real-time User Equipment
RTL	Register Transfer Level
RM	Reuse Methodology
RSS	Rich Site Summary
SAPs	Service Access Points
SGSN	Serving General Packet Radio Service Support Node

SIP	Session Initiation Protocol
SMS	Short Messaging Service
SIR	Signal to Interference Ratio
SF	Spreading Factor
SDRAM	Synchronous Dynamic Random Access Memory
TTC	Telecommunication Technology Committee
TTA	Telecommunications Technology Association
TCM	Time Consuming Methods
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TLM	Transaction Level Modeling
TCP	Transmission Control Protocol
TPC	Transmission Power Control
TTI	Transmission Time Interval
TBS	Transport Block Set
TrCH	Transport channel
TFCI	Transport Format Combination Indicator
TFI	Transport Format Indicator
UTRAN	UMTS Radio Access Network
USIM	UMTS Subscriber Identity Module
UMTS	Universal Mobile Telecommunication System
UTRA	Universal Terrestrial Radio Access
UVC	Universal Verification Components
UVM	Universal Verification Methodology
UL	Uplink
UE	User Equipment
VHSIC	Very High Speed Integrated Circuits
VHDL	VHSIC Hardware Description Language
VHPI	VHDL Procedural Interface
WAP	Wireless Application Protocol

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1 Introduction

The evolution of cellular networks into third generation (3G) system in the last decade has opened up new dimensions in connecting people. There is an ever increasing demand for higher speed in the networking world mainly to cater real time multimedia and large volumes of data traffic. Wideband Code Division Multiple Access (WCDMA) is air interface standard adopted for 3G in Europe, Asia and Africa. Unlike older systems 3G offers variety of services such as web browsing, e-mail, video calls and multimedia streaming. 3rd Generation Partnership Project (3GPP) is the international committee which decides upon standards and architecture for 3G mobile communication system.

3G mobile communication system developed under 3GPP is named Universal Mobile Telecommunication System (UMTS) which consists of three main components – user equipment, base station and core network. Since the first release of 3GPP standards in 1999, WCDMA has developed into High Speed Packet Access (HSPA) networks which can support data rates[1] up to 337.5 Mbps on the downlink [1] and 23 Mbps on uplink [2]. Owing to miniaturized semiconductor devices, advancement in display technology and terminal battery backup has enabled WCDMA to host many applications specifically in packet switched networks.

1.1 Background

Ericsson's WCDMA Radio Access Network development unit located at Gothenburg is responsible for development and maintenance of 3G base stations. This project is carried out at Baseband Processing department in aforementioned unit which undertakes system and software design, integration and verification of baseband processing modules.

These baseband modules are required to be tested to ensure the precise operation and measure the performance during varying conditions. Digital Processing Adapter (DPAD) hardware is used to validate the operation of baseband. This board behaves as Real-time User Equipment (RUE) which can transmit antenna data and decode the messages from baseband component. Antenna data signifies the user data in digital format after various signal processing operations. The infrastructure of the DPAD is capable to simulate different transmission characteristics on air and can be programmed by external host. DPAD comprises of Digital Signal Processors (DSPs), Field-Programmable Gate Arrays (FPGAs) and other controllers. One of the FPGA in DPAD is used for generating the antenna data in uplink[2] based on configuration set by test program. This FPGA is termed as Chip Rate Accelerator Uplink (CRAUL) which has the capability to generate user data for 'X' number of RUE.

[1] These data rates are deduced for a specific case based on modulation, antenna type and number of cells.
[2] UL is direction of transmission from user equipment to base station.

Specman is one of the software tools from Cadence used for functional verification of hardware design. It provides a platform for developing test bench environment in e hardware verification language. The test bench created for block level entities can be reused at higher hierarchies of the system up to chip level. Specman is tightly coupled to a Hardware Description Language (HDL) simulator which simulates the device behavior from the relevant code files.

1.2 Objective

This master thesis aims at verification of the FPGA - CRAUL to validate timing, configuration and data flow. Specman is used for the verification and the necessary test bench is developed for each processing blocks in CRAUL. The block level test benches are later combined to perform system level testing. The purpose of the system level testing is to simulate most of the scenarios possible under 3GPP specification and evaluate the device behavior. The work includes a preliminary study of 3GPP protocols and WCDMA physical layer in UMTS. The different processing blocks of CRAUL are investigated at the beginning and detailed design documentation is prepared before individual test benches are created.

1.3 Scope

The scope of this project is limited to uplink physical layer procedures. Specifically it includes chip rate processing modules and the interaction of the FPGA and DSPs. The verification of the hardware is done in a simulation environment triggered by Specman.

Each physical channel processing includes eight signal processing blocks meant for modulation mapping and spreading combined with one unit for multiplexing, scrambling, gain control, filtering and accumulation of 'X' RUE data. Unit level test benches are designed for modulation mapping, spreading, multiplexing, scrambling and gain control. Unit level test bench is also developed for control modules. At unit level more attention is given to verify the timing accuracy, functionality and data formats of input and output. The test environment for the system encapsulates all these unit level test benches.

1.4 Effort Distribution

The verification effort of the project has been split into two thesis to reach the desired level of verification goal on time. Hence few of the modules have been verified in this thesis and few others in the [17]. The study of design and the discussion of methodology to verify the various modules have remained as common part of both the thesis. The theoretical background in this thesis report has also been written as a common part for both the thesis.

The design constitutes a control path and a data path. The control path consists of frame configuration module, slot configuration module and data generation module. The data path consists of modulator, spreader, IQ mapper, scrambler and transmission power control module (TPC).

Few of the test input sequences of frame configuration module and the verification code for rest of the control path modules has been carried out in this thesis. The verification code for modulator, spreader and the test input generation mechanism for the TPC module has also been developed as a part of this thesis.

1.5 Overview of Report

The report aims at providing enough technical background about the concepts and the design before starting to discuss the verification methodology actually used to verify the design.

- Chapter 2, Gives an overview of UMTS, UMTS services and network architecture, WCDMA protocol and various signal processing operations involved in 3GPP WCDMA protocol.
- Chapter 3, Discusses physical layer in detail, provides an overview of different logical channels that constitutes the physical layer, describes the various physical layer procedures involved before the signals are put out in air.
- Chapter 4 Gives an overview of different verification methodologies (logic simulation, emulation, formal verification) and goes in detail to describe the logic simulation methodology, what is coverage driven verification (CDV) and re-use methodology (RM), Universal verification methodology (UVM) and its structure.
- Chapter 5, Overview of the Ericsson proprietary board and the components on this board that has been verified as a part of this thesis.
- Chapter 6, Architectural description of the test bench design for each of the components , overview of stimuli sequence and the coverage points used, and the hierarchical connection of the unit level test bench components to form the system level test bench.
- Chapter 7, Coverage results and test bench optimizations done to reduce the simulation time.
- Chapter 8, Conclusions and some thoughts on using UVM for verification.
- Chapter 9, some hints on areas which could be further investigated, design modules to which the test bench could be extended.
- Chapter 10, References to the study material used as a part of this thesis.

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2 Universal Mobile Telecommunication System (UMTS)

UMTS is the 3G mobile communication system developed by 3GPP. UMTS encompasses radio access procedures, radio access network and core network. WCDMA is used as the air interface and occupies a 5 MHz bandwidth. This section provides an insight into different UMTS service, UMTS network architecture, WCDMA and power control mechanism. A brief introduction to cellular networks is given below.

2.1 Cellular networks

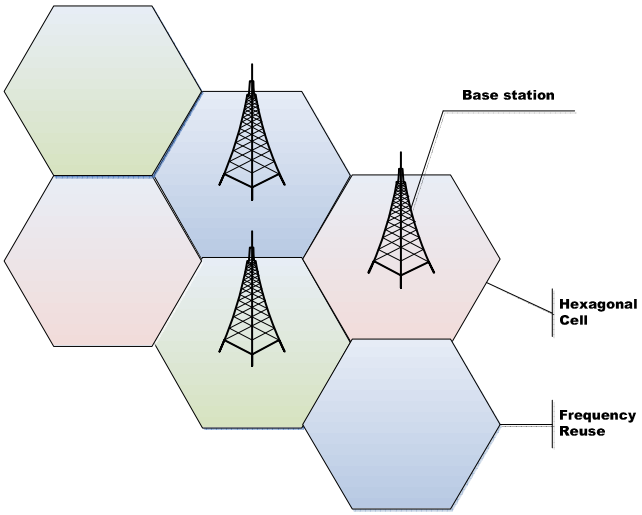

Fig 1. Hexagonal cells and frequency reuse

First generation (1G) mobile radio systems provided services to a larger coverage area with a single high powered base station. This approach had a serious limitation on frequency reuse since it would result in interference and also radio spectrum is a limited resource. To improve the capacity or to support more calls simultaneously cellular concept was proposed [3]. Cellular concept employs relatively low powered base stations serving smaller geographical area as shown in Fig 1. The available frequencies to an operator are divided into groups and each base station is assigned with one set such that the neighboring cells have non overlapping groups. The frequency spectrum is repeated after a sufficiently larger distance so that interference can be kept below acceptable levels. Spectral congestion is resolved for increasing demand in capacity by making the cell size smaller.

Cellular networks have evolved from circuit switched network (1G) to packet switched third generation systems (3G). Global System for Mobile (GSM) is the most popular second generation (2G) mobile communication system launched in 1991 and in 2005 it accounts for more than 75% worldwide cellular market penetration [4]. GSM is a digital, circuit switched network and provides Short Messaging Service

(SMS), voice and fax services. General Packet Radio Service (GPRS) and Enhanced Data rates for GSM Evolution (EDGE) are the packet switched technologies extended for GSM which provide a DL speeds of few hundred kb/s. 3G system was developed to increase the data rates in carrying packet data.

2.2 3GPP

In mid 90s there were efforts to evaluate and develop new cellular technology to support high data rates in different parts of the world. This required a single body to define specification and guidelines for global equipment compatibility in third generation mobile communication systems. This led to establishment of 3GPP in 1998. 3GPP is collaboration between many telecommunication associations worldwide, equipment manufacturers, operators and other telecommunication committees. ARIB (Japan), ETSI (Europe), TTA (Korea), TTC (Japan), ATIS (USA), CCSA (China) are the partners of 3GPP which standardizes the Universal Terrestrial Radio Access (UTRA).

3GPP comprises of four technical specification groups for Radio Access Network (RAN), Core Network (CN), service/system aspects and terminals. 3GPP is also responsible for development and maintenance of GSM and Internet Protocol Multimedia Subsystem (IMS). Release-99 in the year 2000 was the first release for the standardization and defined WCDMA air interface. Subsequent release-5 in 2002 was a breakthrough because of High Speed Downlink Packet Access (HSDPA) and release-6 in 2004 specified High Speed Uplink Packet Access (HSUPA).

2.3 UMTS Services

Along with trivial services such as voice call, SMS and voice mails, UMTS offers a bundle of new services having commercial importance. To name a few are multimedia streaming, mobile broadband, browsing, gaming and content downloading. Some of the key services are explained in brief.

Video Telephony

UMTS has made video telephony commercially viable for the users compared to earlier systems. First release, release-99 supported 64 kbps and release-5 has come up with efficient Session Initiation Protocol (SIP) which gained popularity in netbooks and laptops. Advancement in the smart phone devices with higher resolution cameras has also contributed to the success of video conversation services.

Mobile e-mail

Terminal devices with email clients facilitate push email and competitive approach compared to email access using Extensible Hyper Text Markup Language (XHTML) pages. This is an always-on application and utilizes background Quality of Service (QOS). Supplemented with instant messaging feature makes this service more appealing for real-time chat.

Browsing

Internet access on the move has added advantages in contrast to browsing over a personal computer. Progressive download technique for playing streamed multimedia, easy access to social networking sites and widgets are striking features of UMTS browsing service. High resolution screen, improved battery back-up and memory storage in the mobile handsets makes it equivalent to a computer. Inbuilt Global Positioning System (GPS) receivers promote location based services such as digital maps, city guides, weather and traffic information. Compared to earlier Wireless Application Protocol (WAP) technology, HTML browsing, RSS feeds, blogging and podcasts are feasible in UMTS.

2.4 UMTS network architecture

3GPP standards define elements of the network at different logical levels. The interfaces between different levels are open which implies that it is described to detailed level in order to facilitate equipments from different manufacturers. The high level system architecture (Fig 2) constitutes User Equipment (UE), UMTS Radio Access Network (UTRAN) and Core Network (CN) [5], [6].

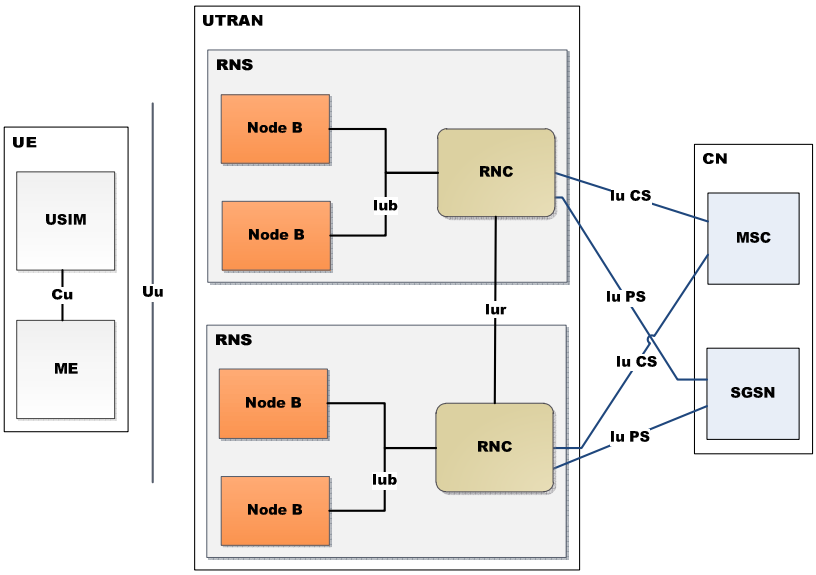

Fig 2. UMTS architecture showing different interfaces

2.4.1 UE

This is the mobile station and houses two logical elements - Mobile equipment or terminal and UMTS Subscriber Identity Module (USIM). USIM stores operator specific information such as authentication and

encryption keys [5]. UE connects to RAN on Uu interface. Terminal, mobile, users all refer to UE in this literature.

2.4.2 UTRAN

The radio functionality is handled in UTRAN including radio access, resource management, paging etc. UTRAN consists of one or more Radio Network Subsystem (RNS) and each RNS includes two logical elements Node B and Radio Network Controller (RNC). There can be more than one Node B in a RNS but only single RNC.

Node B

This is more generically termed as base station and provides the radio infrastructure. Many UEs connect to Node B on the Uu air interface and further routed to RNC on Iub interface. Most of physical layer procedures such as channel encoding/decoding, error handling and modulation/demodulation are carried out by base station. Base stations are physically housed in a cabinet powered by batteries and comprises of DSPs and ASICs. The radio module enables power amplification, mixing, filtering and terminates in an antenna.

Radio Network Controller

Several Node Bs are connected to a single RNC which administers the radio resources. Load and congestion control, code allocation for new links, outer loop power control, soft handovers are major responsibilities of RNC. Iu interface links RNC and CN. RNCs in different RNSs are connected by Iur interface.

2.4.3 Core Network

UMTS CN is adapted from GSM and offers many advantages like global roaming and inter operability with GSM. CN encompasses service and management oriented elements for Circuit Switched (CS) and Packet Switched (PS) networks. CN is the gateway to ISDN, PSTN, PLMN and internet. Home Location Register (HLR) is a database which store user service profile and UE location at Mobile Switching Centre (MSC) and Serving GPRS Support Node (SGSN) level.

2.5 Protocol architecture for Uu Radio interface

Uu air interface bridges UE to the Node B and composed of three logical layers – Layer 1, Layer 2 and Layer 3 as exemplified in Fig 3. The different layers communicate via ports called Service Access Points (SAPs) and the format of the data exchanged between these layers differ [7]. Medium Access Control (MAC) is the lowest sub layer in Layer 2. Layer 1 is the physical layer which is responsible for transmission and reception of bits on air. MAC provides transactions to physical layer as transport blocks which are processed eventually into radio frames. Radio Resource Control (RRC) in Layer 3 co-ordinates the resource management and configures physical layer.

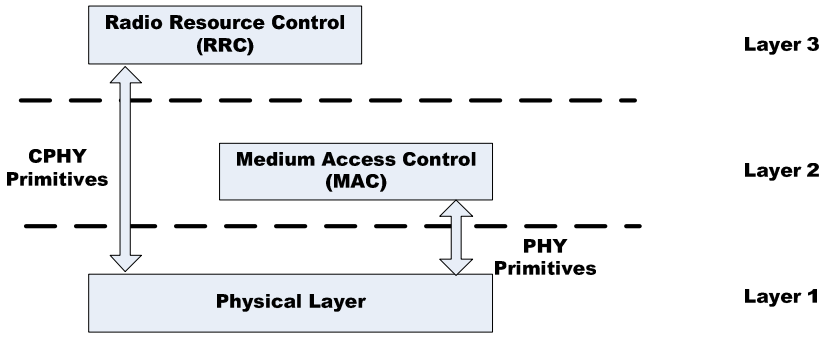

Fig 3. Different interfaces to physical layer

2.6 WCDMA

Different multiple access techniques enable a single channel to be available for different users. Time Division Multiple Access (TDMA) divides the time into specific transmission slots and one slot is dedicated to a user. Frequency Division Multiple Access (FDMA) provides a share of the total available frequency band to each user. 3GPP defines WCDMA as the multiple access technique where all the users occupy the same frequency band and independent in time but separated by orthogonal codes [3]. The multiple access techniques are graphically demonstrated in Fig 4.

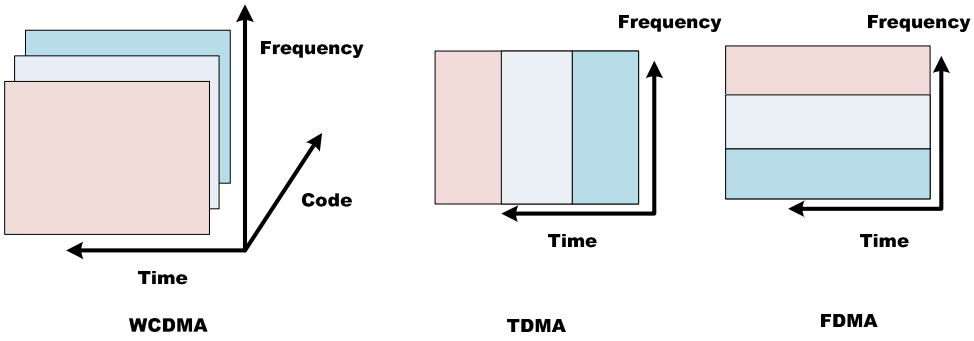

Fig 4. Various multiple access techniques[18]

WCDMA is wideband Direct-Sequence Code Division Multiple Access (DS-CDMA) system which uses high frequency pseudo random bits called chips for spreading the user information [5]. User information is multiplied by chips to spread the data over a wide bandwidth. As shown in Fig 5, the spread signal power is below noise floor by 20 dB for a specific speech case at 12.2 kbps rate [5]. At the receiver the original information is recovered from the product of wideband signal and the original spreading sequence used at the transmitter. Spreading provides higher immunity to narrow band interference, jamming and reduces security threats. Since WCDMA occupies a large bandwidth compared to coherence bandwidth of the channel, multipath fading effect is less [3]. WCDMA also supports multi-rate data, adaptive antenna and multiuser detection.

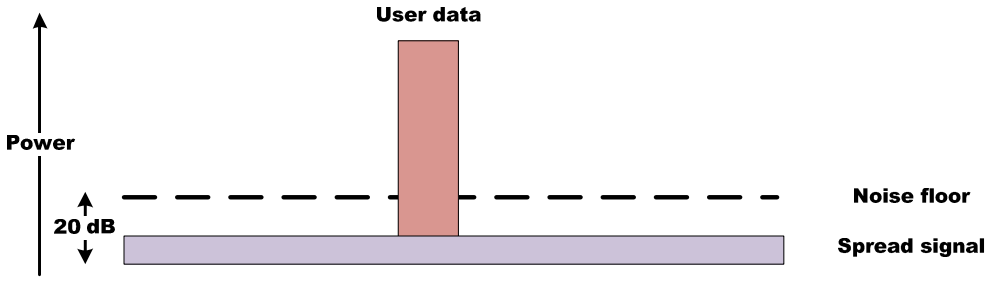

Fig 5. Frequency spectrum of a spread signal

Time Division Duplexing (TDD) and Frequency Division Duplexing (FDD) are the two kinds of duplex modes supported by UMTS for simultaneous transmission in Uplink (UL) and Downlink (DL). UL defines the direction of messages from UE to base station and DL refers to signals from base station to UE. Two 5 MHz bandwidth channels are utilized in FDD for UL and DL. TDD uses a time shared single 5 MHz bandwidth for both directions. Radio frames are transmitted for duration of 10 ms and carries 38400 chips resulting in rate of 3.84 Mcps.

2.6.1 Spreading

The spreading operation is accomplished by multiplying user data with chip sequence bit duration by bit duration as shown in Fig 6a. Number of chips in one symbol duration is termed as Spreading Factor (SF) and higher SF values are used for lower user data rates. SF also signifies the factor by which the spectrum of baseband signal is scaled.

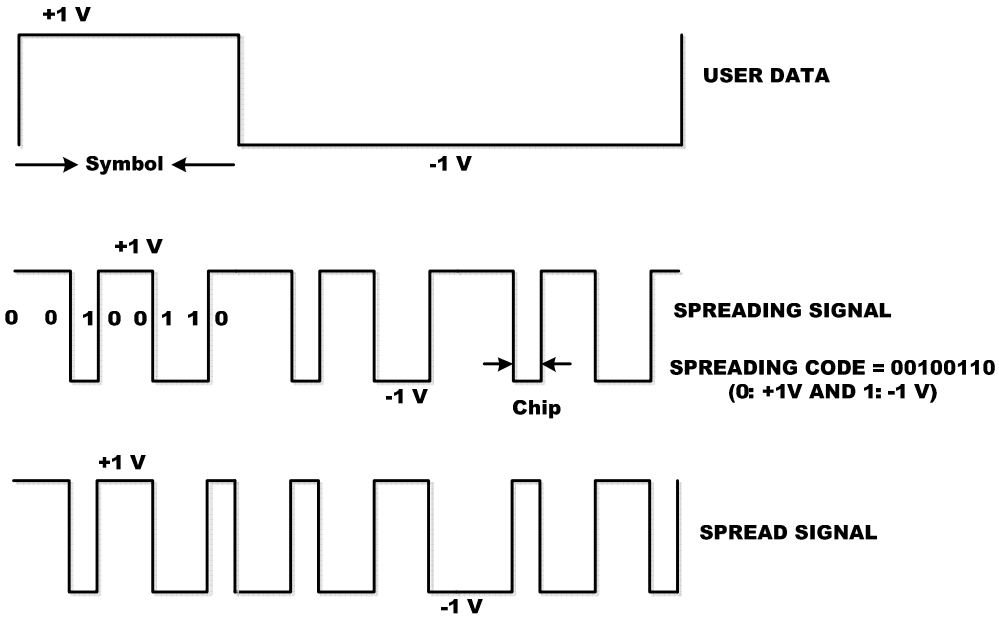

Fig 6a. Spreading of user data

The spread signals are transmitted on air and signal power of different users gets combined. To achieve least interference different users employ spreading codes with zero cross correlation. During despreading a received signal is multiplied by the chip sequence used at the transmitter side to recover the original information. Despreading requires time synchronization between received signal and spreading sequence. This is followed by an integration of the signal envelope over SF chip duration. Interfering signals when despread and integrated, results in a zero value as opposed to a maximum value when the product is integrated for desired user signal. Fig 6b describes despreading of BPSK[3] modulated bit sequence spread with a SF value of 8. Processing gain is the value same as SF and denotes the phenomenon where the desired signal amplitude is increased after integration due to correlation detection. The consequence of integration for other interfering signals after despreading and a processing gain value of 8 for desired signal is shown in Fig 6b.

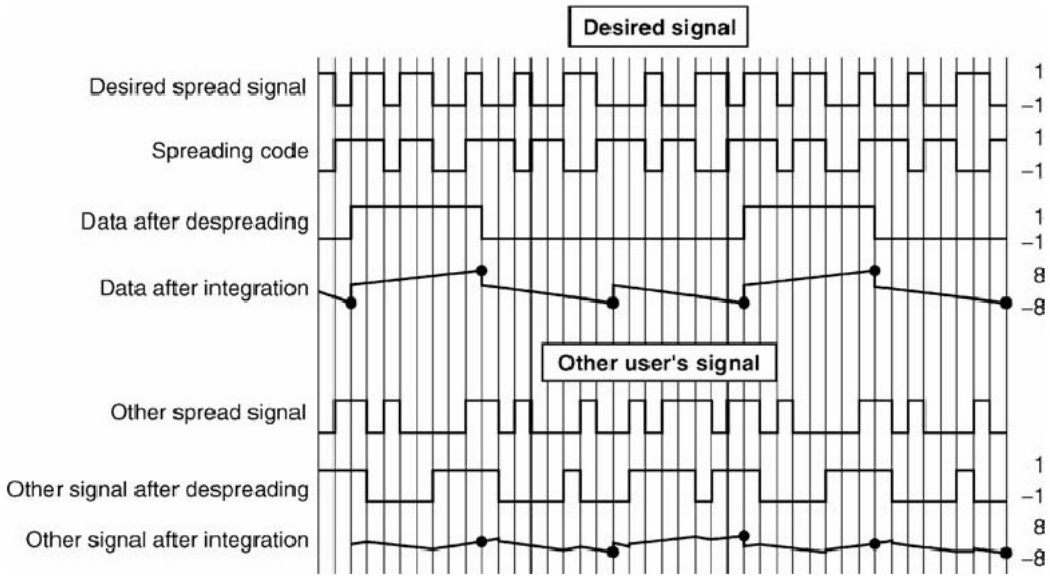

Fig 6b. Despreading of user data [4][5]

[3] BPSK assumes real values of ± 1.

[4] This picture is reproduced from Fig 3.3 Principle of the CDMA correlation receiver, pg 50 in [5].

Orthogonal Variable Spreading Factor (OVSF) codes

To ensure least cross correlation between different spreading codes, OVSF codes are used. OVSF codes can be determined for different values of SF from Walsh tree. Basic pattern in generating the code is described in Fig 7. At each stage the code branches into two with code repeated in one stream and negated code appended to existing code in the other branch. Whenever a code is selected then subsequent sub tree from this code is not used by other channels to ensure that codes are orthogonal.

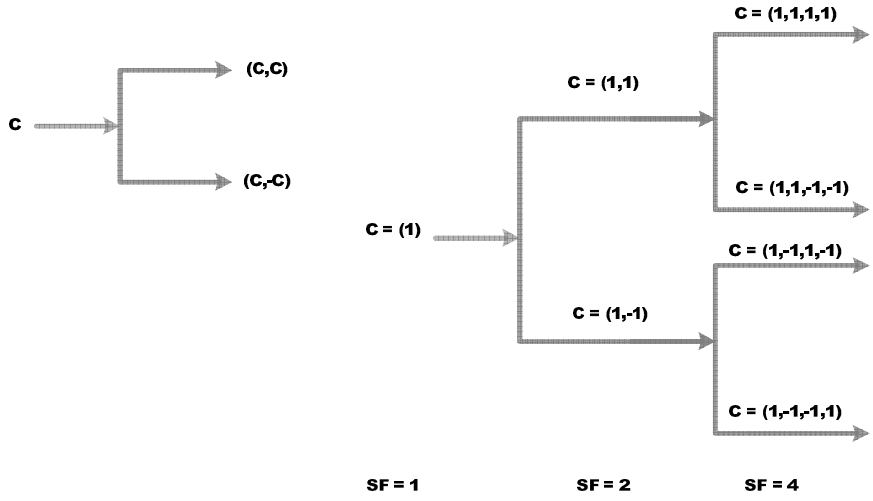

Fig 7. OVSF code generation using Walsh tree

2.6.2 Power control

CDMA systems have an inherent drawback of near far problem [3] where stronger signals from mobile users near to base stations will block weaker signals from distant users. Stronger signals define the noise threshold at base station demodulator circuit and weaker signals are suppressed. A stringent power control of users is managed by the base station in such a way that received power level from all users at base station receiver is equal. Three types of power control mechanism are exercised in UMTS - open loop, closed loop and outer loop control [5]. Fig 8 illustrates open loop and closed loop power control which are described in subsequent section.

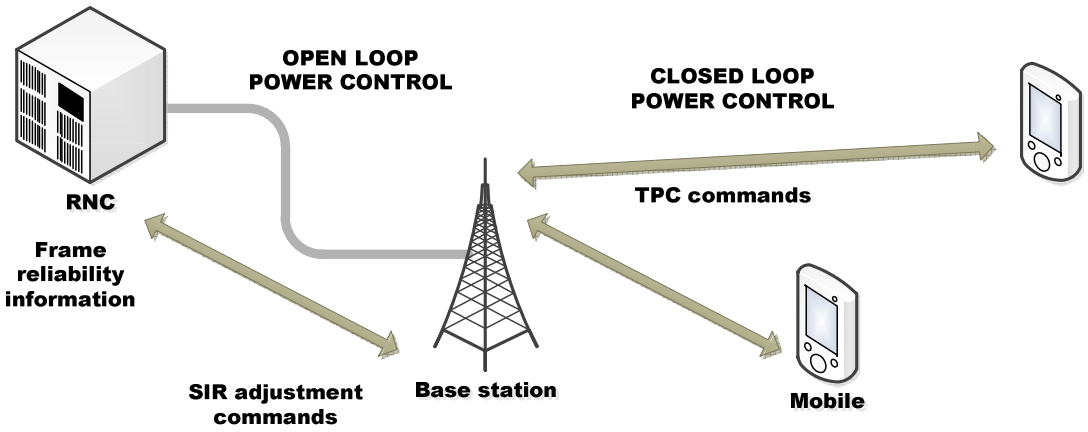

Fig 8. Power control mechanism in UMTS

Open loop control

During a connection set up a UE would measure the beacon frames[5] on the DL and deduce path loss. This estimate is used as initial power setting and usually inaccurate to a large degree.

Fast closed loop control

Signal to Interference Ratio (SIR) measurements for all active[6] mobile users are performed by base station on the UL and compared against a threshold value. Base station sends appropriate commands to each UE on DL to increase or decrease the power based on the result of comparison. The cycle of base station signaling the commands and terminals adapting to these changes occur at a frequency of 1.5 KHz [5]. Hence it is referred as fast closed loop control and is much faster than speed of Rayleigh fading for moderate speeds [5]. On DL there is no near far effect since there is only one base station transmitting to many mobiles. The fast closed loop control on DL provides a mechanism to combat Rayleigh fading and path loss for terminals at the cell edge.

Outer loop power control

The threshold SIR at the base station is set by outer loop power control managed by RNC. The base station indicates RNC the quality of the link between base station and UE by a frame reliability indicator attached to the user data stream. The frame reliability indicator is evaluated from Cyclic Redundancy Check (CRC) results obtained by UL decoded data. RNC ascertains the Bit Error Rate (BER) from frame reliability indicator and directs to change the threshold SIR at the base station to maintain a constant quality.

[5] Beacon frames are broadcast control messages from base station to all terminals in the cell.
[6] Active users have an established connection with base station for voice or data.

2.6.3 Handover

Handover is performed when a mobile moves from one cell or sector to another during an ongoing conversation. A new channel in the target cell is set up after it is released in source cell in hard handover. Soft handover establishes connection in parallel with the two cells. The different types of handovers are explained below.

Inter-system hard handover

The mobile switches between different systems such as between WCDMA FDD and WCDMA TDD or GSM.

Inter-frequency hard handover

Terminal changes the WCDMA carrier frequency when the cell is congested. This handover occurs in hierarchical cells.

Soft handover

It occurs when mobile located in overlapping coverage area of two base stations belonging to one RNC. The mobile can be concurrently connected to both base stations. Received data from two base stations are routed to RNC for combining and data with less BER is selected. Two closed power control loops operate independently.

Softer handover

This occurs when the mobile is in an overlapping coverage area of two sectors of the same base station. The mobile is connected to two sectors distinguished by two scrambling codes on UL. Fast power control is enabled in only one connection. At the base station side a single Rake receiver decodes the information received on both the sectors and uses maximal ratio combining.

3 Physical Layer

Also referred as Layer-1, performs signal processing operation and responsible for radio transmission on air. Different physical layer functions are mentioned below [8].

- Soft handover execution
- Power control and estimates for SIR
- Modulation, spreading, despreading of Physical Channel (PCH)
- Time and frequency synchronization
- Beamforming and Multiple Input Multiple Output (MIMO) transmission
- Multiplexing of transport channels and mapping to different PCH
- Error detection and correction of transport channels and indication to higher layers.

3.1 Transport channel (TrCH)

Transport channel contains information from Layer 2 which is further carried by PCHs. TrCHs are specific to applications like conversation, interactive or internet. The demand for bandwidth may vary over time because of many active applications. Dedicated TrCHs are reserved for conveying user data and determined by a specific code. Common channels are resource shared between all users in a cell and are usually used for control information and small packet data.

Transport Block (TB) is the basic element that is exchanged between L1 and MAC. There may be more than one TB for any channel and the collectively it is defined as Transport Block Set (TBS). The size of a TB is expressed as number of bits and is always fixed for a TrCH. The size of all TBs in a TBS is always equal. Transport format indicates the delivery method of TBS to L1 and contains two distinct parts - dynamic and semi static part [7]. Attributes for a dedicated PCH utilizing FDD are mentioned below.

Dynamic part includes

- TB size
- TBS size

Attributes of the semi static parts

- Transmission Time Interval (TTI)
- Channel coding parameters and type of coding
- Rate matching parameters
- CRC size

3.1.1 Transport channel multiplexing

TBS containing user and higher layer control information on different TrCHs are multiplexed and mapped to PCHs. Each TrCH is associated with Transport Format Indicator (TFI) which signifies the different kind of applications involved and the corresponding data rates. TFIs of different TrCHs are combined to Transport Format Combination Indicator (TFCI) which is essentially mapped to Dedicated Physical Control Channel (DPCCH). The frequency at which TBS is passed by higher layers is called TTI and may be 10 ms, 20 ms, 40 ms or 80 ms. TBS having TTI values larger than 10 ms are distributed evenly in consecutive 10 ms frame. E.g. TBS with TTI 80 ms is contained in eight 10 ms frames after physical layer procedures.

The receiver learns the different TrCHs which are active by decoding TFCI. The reverse operation of determining TFI and bifurcating TrCHs supplemented with error indication are performed by the physical layer, Fig 9. One physical control channel and a physical data channel form a single Coded Composite Transport Channel (CCTrCH).

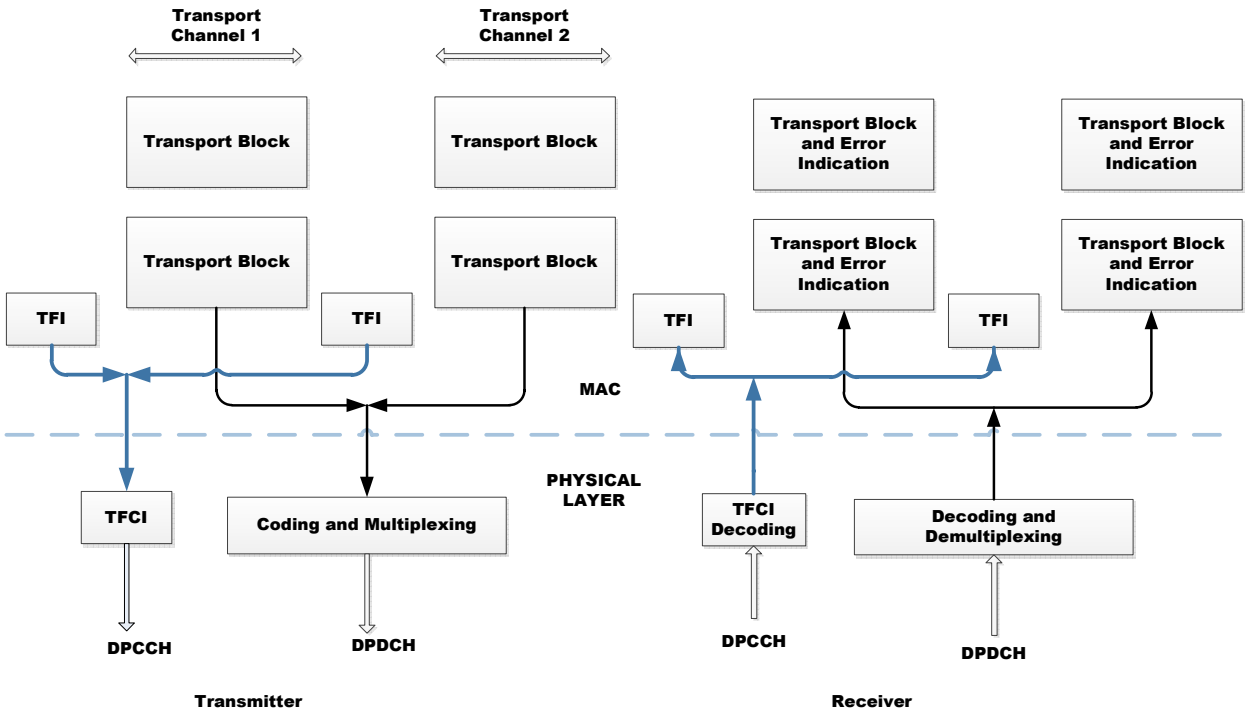

Fig 9. Transport channel multiplexing

3.1.2 Dedicated Channel (DCH)

This is a TrCH which transports user data and there can be several DCHs transmitted in parallel for a UE. It maps directly to Dedicated Physical Data Channel (DPDCH) and Dedicated Physical Control Channel (DPCCH).

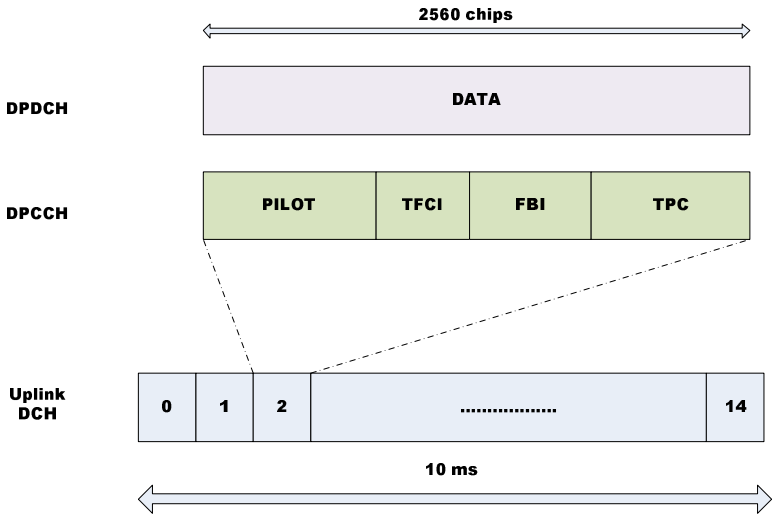

Fig 10. Dedicated physical channels

DPDCH

This carries the user data and higher layer control signaling in a 10 ms frame with a fixed 38400 chips. Logically a frame is divided into 15 slots having 2560 chips (Fig 10). There can be maximum six DPDCH channels IQ multiplexed and spread with SF values from 4 to 256 on UL [9]. Enhanced DPDCH (E-DPDCH) is used by HSUPA characterized by Hybrid Automatic Repeat Request (HARQ) and quick link adaptation.

DPCCH

Single DPCCH carries the L1 control information and SF is fixed to a value of 256 in UL. The data rate of DPDCH is conveyed by TFCI bits in DPCCH. DPCCH is also a 10 ms radio frame with 15 slots and each slot has 2560 chips. Each slot has following parameters (Fig 10)

- Pilot bits used by the receiver for channel estimation
- TFCI includes the data rate of corresponding DPDCH
- Feedback information (FBI) bits are used only for closed loop transmission diversity in DL
- Transmission power control commands to enable fast power control

3.1.3 Random Access Channel (RACH)

Random Access Channel (RACH) is the TrCH which carries signaling information on the uplink in order to setup connections or for transporting small packet data. This is a shared channel with lower data rates and subjected to collisions at higher loads. Physical Random Access Channel (PRACH) carries the RACH information and medium access follows slotted ALOHA protocol with fast acquisition indication [10]. A 20 ms time interval is segmented into 15 access slots of width 5120 chips. The random access transmission can be initiated by any terminal on the beginning of these slots as described in the Fig 11.

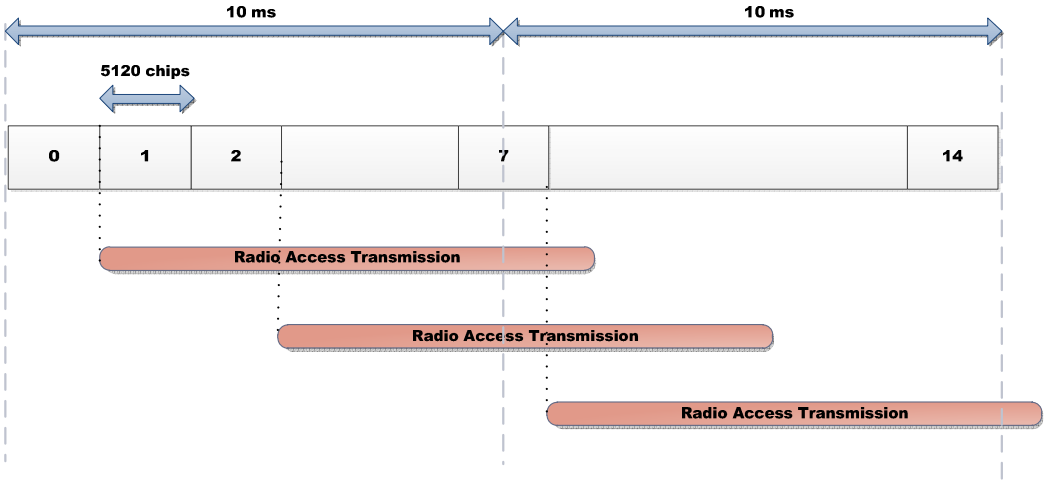

Fig 11. Slot timing for random access transmission

RACH consists of two segments one intended for initial signaling called preamble and upon receipt of an acknowledgment RACH message part is transmitted. A PRACH preamble frame has 4096 chips containing sixteen repetitions of sixteen signature sequences. Node B acknowledges for a preamble on Acquisition Indicator Channel (AICH) in DL. Subsequent to the acknowledgment 10 ms or 20 ms RACH message part is transmitted. RACH message is composed of two PCHs. One PCH represents the data while other channel carries Layer-1 control signaling. Fig 12 illustrates a case where the PRACH preamble is retransmitted because acquisition indication is not received within certain duration after first preamble.

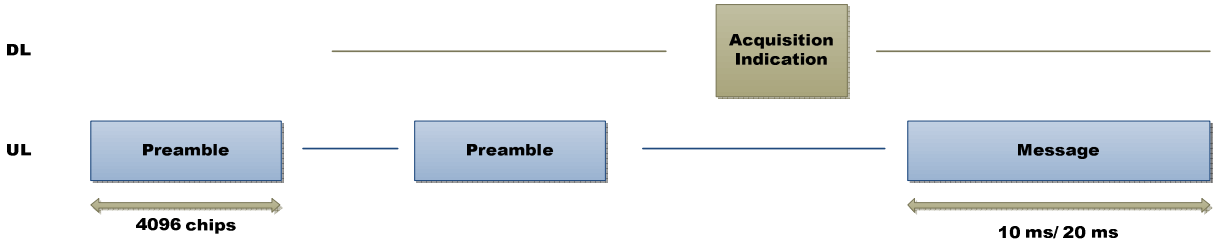

Fig 12. RACH transmission

3.2 Physical layer procedures

3GPP [9], [11] describes TrCH multiplexing, channel coding, modulation and other signal processing for FDD mode on UL. The different signal processing operations are explained in brief and a MATLAB simulation of TrCH multiplexing has been carried out in the project for better understanding. TBS in each TrCH are adapted to PCHs by channel coding, rate matching and interleaving operations at UE which is explained in the following section for UL case (Fig 13).

3.2.1 CRC attachment

To ensure data integrity CRC is attached to every TB in each TrCH. CRC size can assume values 24, 16, 12, 8 or 0 bits. Higher layers signal the size of the CRC depending on the nature of the information. Larger CRC size eases the detection of errors in transport block at the receiver end.

3.2.2 Transport block concatenation and code block segmentation

TBS belonging to same TTI are sequentially concatenated. In case the size of the connected blocks is greater than a threshold value Z bits, it is segmented. Z is determined by the type of channel coding. Value of Z for convolution coding is 504 bits and for turbo coding is 5114 bits. The segmentation divides the concatenated string (X bits) into C equal segments, where C is the number of code blocks. Filler bits of zero value are inserted at the beginning of concatenated string to ensure equal segment length. Filler bits are also added in case of Turbo coding to concatenated string when size is less than 40 and segmented to only one block. Segmentation is expressed mathematically in equation 3.1.

$$C = \left\lceil \frac{X}{Z} \right\rceil \tag{3.1}$$

3.2.3 Channel coding

Error correction is implemented by channel coding for segmented code blocks and belongs to Forward Error Correction (FEC) scheme. The receiver can attempt to correct the errors depending on the redundancy bits added. Higher rate[7] coding provides better immunity to channel distortions and noise effects. Convolution and Turbo coding are the two coding schemes suggested by 3GPP [11] and depends on the TrCH as given in Table 1.

Table 1. Coding scheme for transport channels

Type of TrCH	Coding Scheme	Coding Rate	Redundant bits
Broadcast channel	Convolution coding	1/2	16
Paging channel			
Random access channel		1/3, 1/2	24, 16

[7] Coding rate refers to ratio of size of information bits to total size of information bits and redundancy bits.

Dedicated channel and Forward access channel	Turbo coding	1/3	12

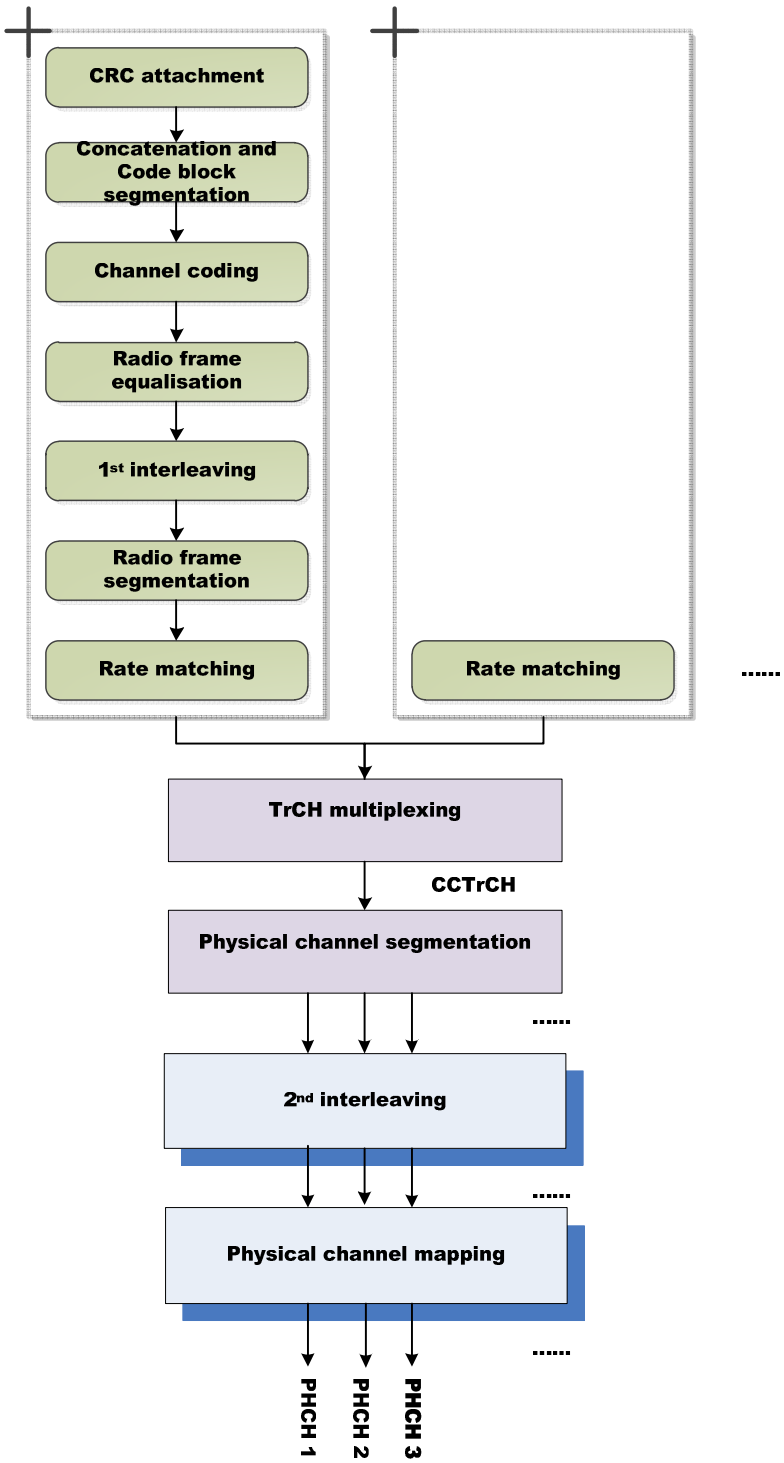

Fig 13. Transport channel multiplexing

3.2.4 Radio frame equalization

After channel coding the code blocks are concatenated serially. This string of bits is appended with 0s or 1s at the end in order to have the number of bits a multiple of TTI.

3.2.5 First interleaving

This is a block interleaving[8] where all the bits are arranged in a two dimensional matrix form. The incoming X bit array is filled up row wise. The number of columns C in the matrix is equal to multiples of 10 ms in TTI duration and the number of rows R is given by the expression 3.2. The interleaving is performed by inter column permutation or replacing the order of column as mentioned in the Table 2. The output bit sequence is read out column after column.

$$R = \frac{X}{C} \tag{3.2}$$

Table 2. Column permutation for first interleaving

TTI	Number of columns C	Inter column permutation pattern
10 ms	1	<0>
20 ms	2	<0,1>
40 ms	4	<0,2,1,3>
80 ms	8	<0,4,2,6,1,5,3,7>

3.2.6 Radio frame segmentation

The output bit sequence of first interleaving is divided into number of fragments if the TTI is larger than 10 ms. Each fragment is included in successive 10 ms radio frame and segmentation distributes input bit sequence received every TTI into N consecutive radio frames, Equation 3.3.

$$N = \frac{TTI}{10} \tag{3.3}$$

3.2.7 Rate matching

A 10 ms radio frame contains 38400 chips and one frame includes bits from different TrCHs. The number of the code blocks passed from the higher layer can change every TTI. This requires a mechanism to repeat the bits if they are few or puncture in case of many, to match channel bit rate supported by the physical layer. Semi static rate matching attribute is also rendered by the higher layer as a part of TFI. If

[8] Interleaving results in a discontinuous sequence of transmission of bits. This reduces the loss of a complete block in case of errors when contiguous transmission is used. With interleaving a loss of one frame due to channel noise minimally impacts several code blocks which could be recovered by error correction.

data bits are in excess few redundant bits[9] are removed. Rate matching depends on SF, number of PCHs and TTI.

3.2.8 Transport channel multiplexing

Each segment[10] from a TrCH is multiplexed sequentially into a CCTrCH every 10 ms.

3.2.9 Physical channel segmentation

Higher data rate requires more than one PCH and physical channel segmentation divides the available bits into different PCHs.

3.2.10 Second interleaving

This stage is also a block interleaving and performs inter column permutation. A 30 column matrix is occupied by the bits on a PCH row by row and padded with zeros to complete the matrix. The permutation pattern is given in the Table 3 and after column replacements the output bits are read column wise pruning away the padded bits.

Table 3. Permutation pattern for second interleaving

Number of columns	Inter column permutation pattern
30	<0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17>

3.2.11 Physical channel mapping

The multiplexed TrCHs are mapped to corresponding PCHs as per Table 4. During normal operation a radio frame is completely occupied by bits. Whereas in compressed mode[11], transmission is switched off intermittently for a very short duration.

Table 4. Transport channel to physical channel mapping

Transport Channels	Physical Channels
Broadcast Channel (BCH)	Primary Common Control Physical Channel (PCCPCH)
Forward Access Channel (FACH) and Paging Channel (PCH)	Secondary Common Control Physical Channel (SCCPCH)

[9] Redundant bits are appended to information bits during channel coding which assist in error correction.
[10] The number of segments is determined at Radio frame segmentation stage.
[11] Compressed mode assists inter-system and inter-frequency handovers by allowing the receiver to measure signals at another frequency during transmission gaps.

Random Access Channel (RCH)	Physical Random Access Channel (PRACH)
Dedicated Channel (DCH)	Dedicated Physical Data Channel (DPDCH) and Dedicated Physical Control Channel (DPCCH)
Downlink Shared Channel (DSCH)	Physical Downlink Shared Channel (PDSCH)
Common Packet Channel (CPCH)	Physical Common Packet Channel (PCPCH)

3.2.12 Modulation

Modulation Mapping

Binary values are converted to real values in order to facilitate mixing with cosine and sine carrier signals. Higher layer signals the type of mapping – Binary Phase Shift Keying (BPSK) or 4 Pulse Amplitude Modulation (4PAM).

BPSK

Binary 0 is represented by +1 V and 1 is mapped to -1 V before modulation is applied.

4PAM

Two consecutive binary symbols are mapped to one real value as per the Table 5 [9].

Table 5. Modulation mapping for 4PAM

Bits	Mapped Real Value (V)
00	0.4472
01	1.3416
10	-0.4472
11	-1.3416

Modulation

Modulation uses dual channel Quadrature Phase Shift Keying (QPSK) scheme. PCHs are mapped to two branches, I and Q differing in relative phase. A pair of IQ value gets mapped to one of four symbols in constellation diagram depicted in Fig 14. Typically the power levels of I and Q branches may vary significantly due to different data rates. This reduces the spacing between the symbols in the constellation diagram making it difficult to decode at the receiver side. To overcome this drawback, branches with lower data rates are multiplied by a β gain factor.

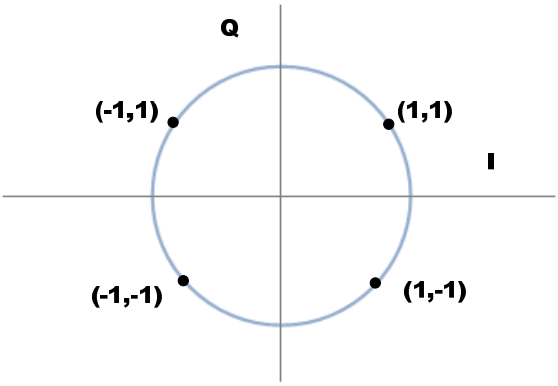

Fig 14. QPSK constellation diagram

3.2.13 Spreading

The baseband signals are spread in the frequency spectrum by multiplying with high data rate chips. Spreading operation involves multiplying data symbols with channelization code followed by complex multiplication of scrambling code for a complete radio frame.

3.2.13.1 Channelization

This operation distinguishes one PCH from the other for a UE. Channelization codes derived from Walsh tree are multiplied with the symbols to convert it to chips. Codes for different channels are orthogonal. The SF can vary from 4 to 256 to enable different data rates in UL. β factor with different weights are multiplied to ensure less power difference between PCHs. Fig 15 shows a DPDCH and DPCCH spread by different channelization codes and DPCCH branch is scaled by β because of the lesser data rate.

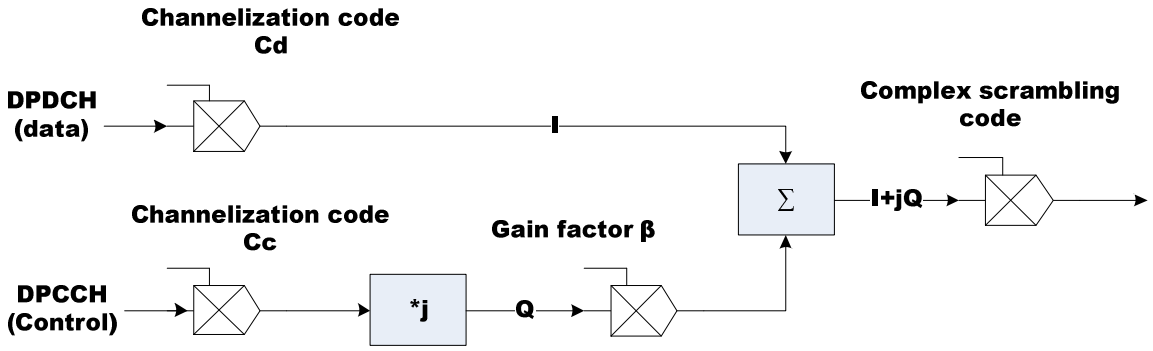

Fig 15. Spreading and multiplexing of physical channels

3.2.13.2 Scrambling

Scrambling codes are complex valued[12] sequences unique for each UE. Scrambling code distinguishes different UEs on UL and different base stations on DL. Scrambling codes are multiplied after applying channelization codes. The time period of chips in scrambling code is same as channelization code and thus scrambling does not alter bandwidth. Long and short scrambling codes are defined in 3GPP specifications [9]. Unique 24 bit scrambling code sequence number for each UE generates scrambling code and 2^{24} scrambling codes are possible.

Linear Feedback Shift Registers (LFSRs) are employed based on the generator polynomials and provide segments of Gold sequences. These sequences exhibit very less cross correlation property. Long scrambling code generates 38400 chips and can be applied to a complete DPDCH frame. Short Scrambling codes are 256 chips in length. Long scrambling codes are relevant to this project. Scrambling procedure restricts the phase transition between consecutive chips in one symbol duration to ± 90° and

[12] Complex value contains real and imaginary parts (a+jb). j represents a phase shift of 90°.

between symbols to ± 180° which reduces Peak to Average Ratio (PAR). Lesser PAR maximizes power conversion efficiency at the amplifier and proportionally enhances the terminal talk time.

3.2.14 IQ mapping

After channelization the spread signals are mapped to an I (In phase) or Q (Quadrature) branch. Two branches differ by a phase of 90° and are combined to provide a complex chip value represented by I+jQ. The multiplexed IQ is forwarded for subsequent scrambling operation. In a time multiplexing mode of control and data channel, there exists an interference with audio equipments [5]. This is observed during silent periods of conversation when only control signaling operates for link maintenance usually at audible frequency range and no user data is transmitted. IQ mode of multiplexing alleviates this audible interference since both data and control channels are multiplexed in parallel which occupies the complete time duration [5]. Fig 15 shows the IQ multiplexing of one DPDCH and DPCCH. A maximum of six DPDCH and one DPCCH channels can be IQ multiplexed in the similar fashion and described in Fig 16.

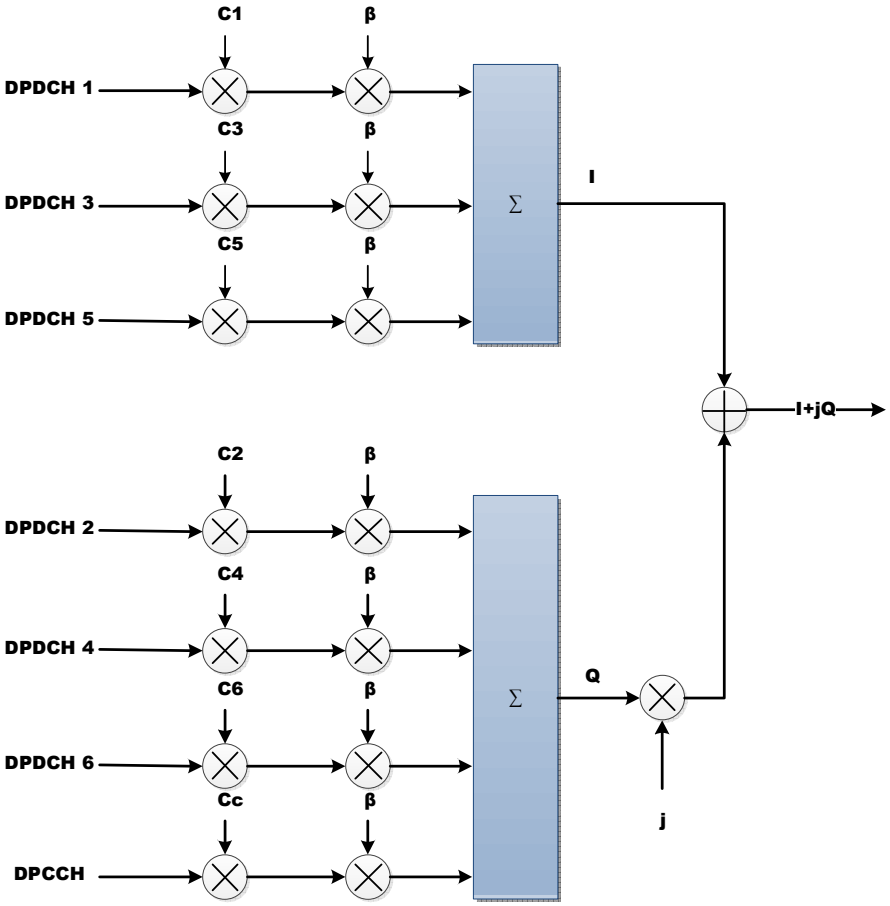

Fig 16. Spreading and IQ multiplexing for DPCH

3.2.15 Mixing

This is the final procedure after scrambling where two branches IQ are split and multiplied by a sinusoidal carrier wave. A raised cosine filter is used to shape the pulse before mixing the two streams by a carrier with appropriate phase, Fig 17. The signals are summed and provided to radio processing for power amplification, filtering and subsequently transmitted on air.

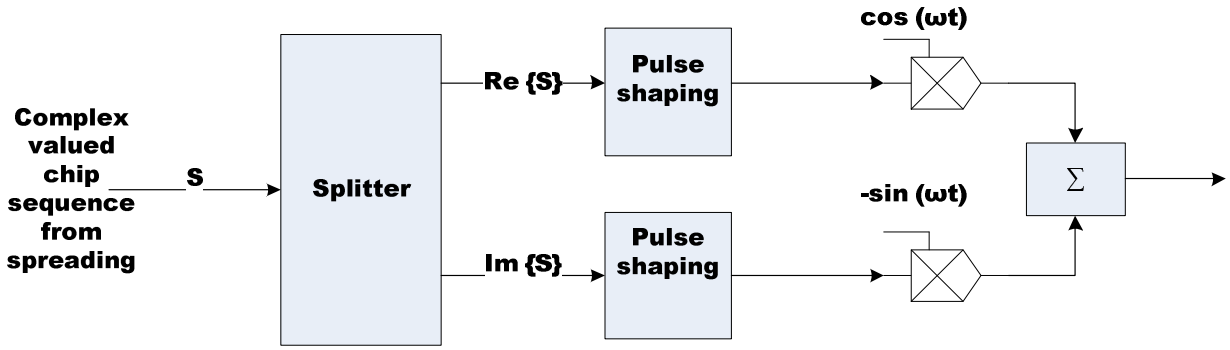

Fig 17. Mixing

4 Functional Verification

Functional verification is the task of verifying whether a given logic design conforms to the specification provided. Due to the increase in complexity of Application Specific Integrated Circuit (ASIC) design, verification has become a huge bottleneck for the chip designers. The verification effort accounts for 70% of the ASIC design life cycle making ASIC verification a major limiting factor for time to market [12], [13].

4.1 Verification methodologies

There are different methods to achieve the functional verification. Few of them have been listed below:

1. **Logic Simulation**: In this method the hardware circuit is simulated by the help of software tools and is subjected to different combinations of input. The inputs are randomized to achieve high distribution over the large input stimuli space.

2. **Emulation**: Using programmable logic, a version of the system could be built to emulate the actual design hardware. This method has the advantage of being much faster than the logic simulation, but it might be difficult to exercise the wide variety of inputs as possible in logic simulation.

3. **Formal Verification**: Here an attempt is made to prove mathematically that certain requirements can be met or assured that undesired behavior would never occur. Formal verification is quite useful for verifying the control logic and interface protocols [12].

The ability to generate wide range of input stimuli makes logic simulation a widely used verification methodology across industries and hence logic simulation is chosen for the verification in this master thesis.

Verification of complex designs consists of hundreds or thousands of deterministic test cases to cover all functionalities of the design. In many cases due to time to market constraints the designs are sent to fabrication with only major functionalities and corner cases verified. However maintaining such huge number of directed test cases is a difficult task and the re-usability for the future projects is small. Hence there was a search for efficient verification methodology to replace the old ones. After a good deal of effort Coverage Driven functional Verification (CDV) along with Reuse Methodology (RM) stood out as a possible solution to enhance verification process by reducing the cost and time to market. Many vendors such as Synopsis, Versity, Cadence etc. came up with advanced verification languages such as Vera, C-

Builder, Specman, System C and System Verilog to solve the verification problem. One of the prominent verification solutions has been from Cadence Specman Elite e-language. Specman Elite e – language is modular, re-usable and based upon randomness and coverage driven functional verification. The language is now an IEEE standard. Specman is the primary tool for developing the test benches in this project.

The functional coverage in CDV and RM is based upon Register Transfer Level (RTL) design specifications. The test plan is derived from these specifications and is written to cover all the functionalities of the design. Four main components of functional verification includes input generation, checking, coverage and debugging. To achieve a very good functional coverage a random input generator is developed and constrained to hit all the desired coverage points. Also for a successful verification a complete verification automation system is necessary which must allow the engineer to efficiently perform the following tasks and graphically represented in Fig 18.

- Defining a test plan
- Writing and maintaining the test bench
- Selecting test vectors (input stimuli)
- Checking results
- Measuring progress against the test plan (coverage)

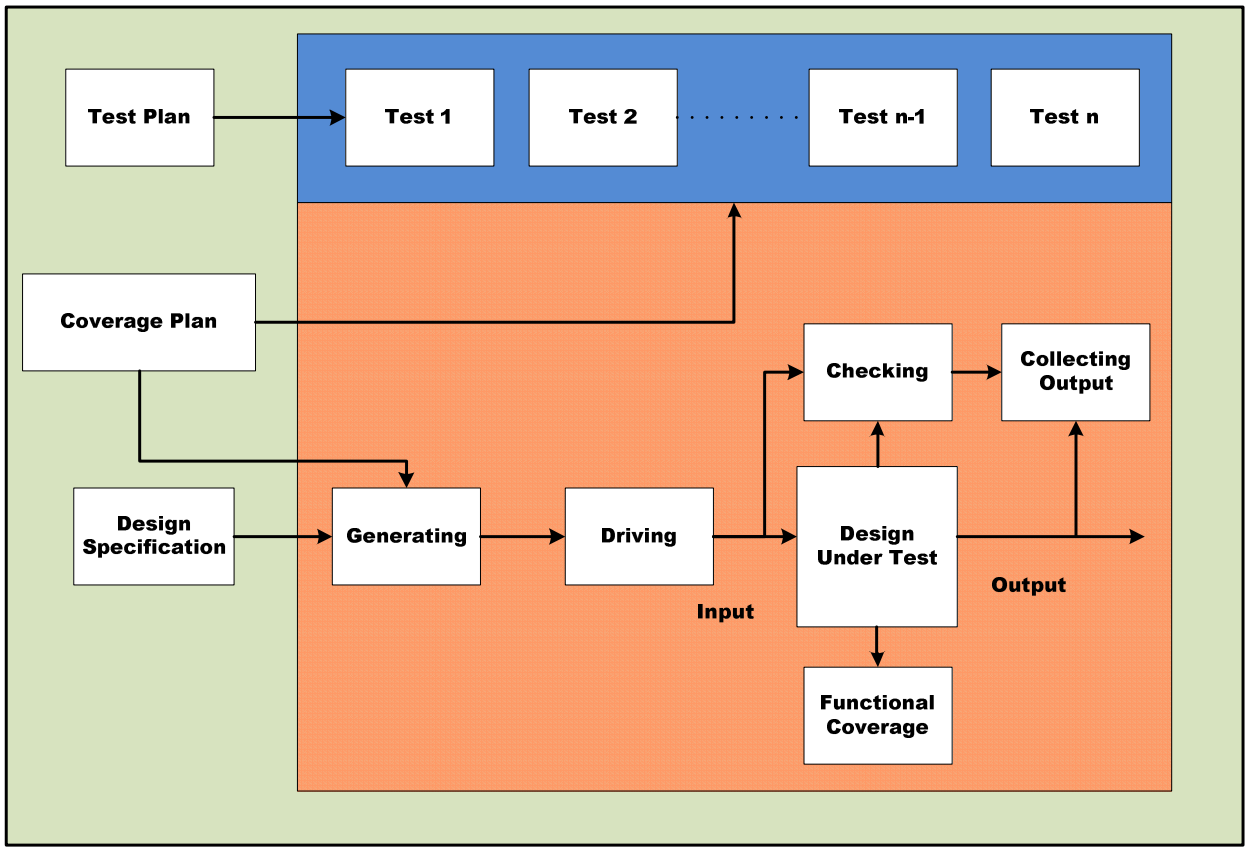

Fig 18. Verification automation system diagram

4.2 Coverage Driven Verification (CDV)

The Design Verification Environment (DVE) in CDV is based upon the functional specification of the design and is implemented by a functional test plan. The test plan points out to all the coverage items to be covered in order to measure the completeness of the verification task. The DVE issues valid transactions onto the Device Under Test (DUT). The functional coverage report indicates the coverage holes which are filled by adding deterministic test cases or by steering the random generator to generate more random input stimuli. The verification is said to be complete if all the coverage holes are covered and 100% coverage is achieved.

The benefits of building the DVE on the concepts of functional coverage includes

- Minimize the number of deterministic test cases required to verify the DUT
- Reduction of simulation time
- Determining the completeness of a verification task
- Adaptability of DVE to accommodate design changes
- Enhancement of overall verification process [13]

The different stage of DVE (Fig 19) and flow chart (Fig 20) gives an overview of the CDV approach.

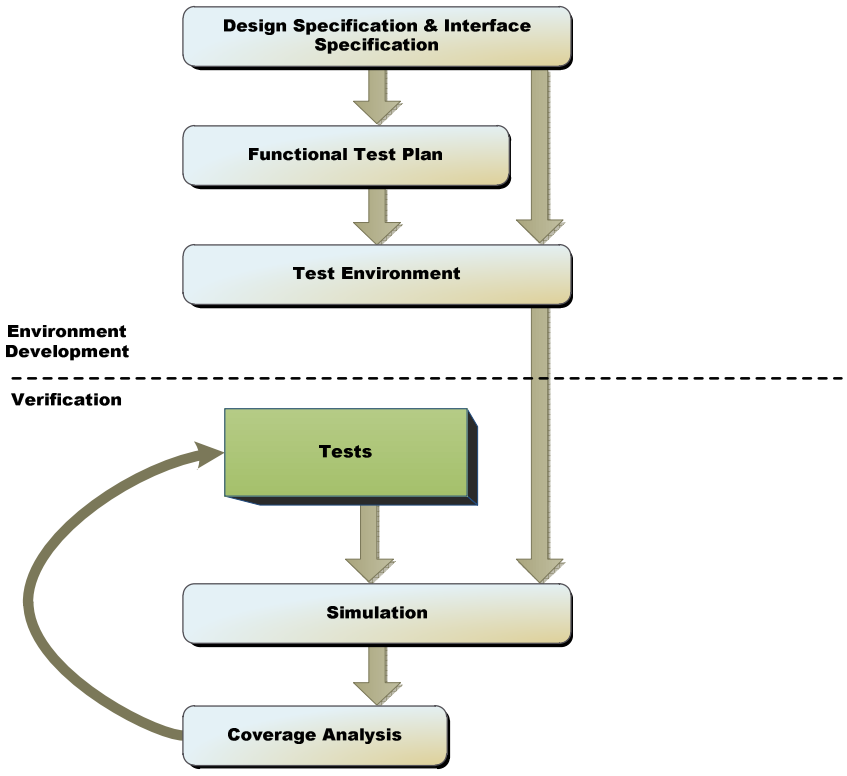

Fig 19. Stages of DVE

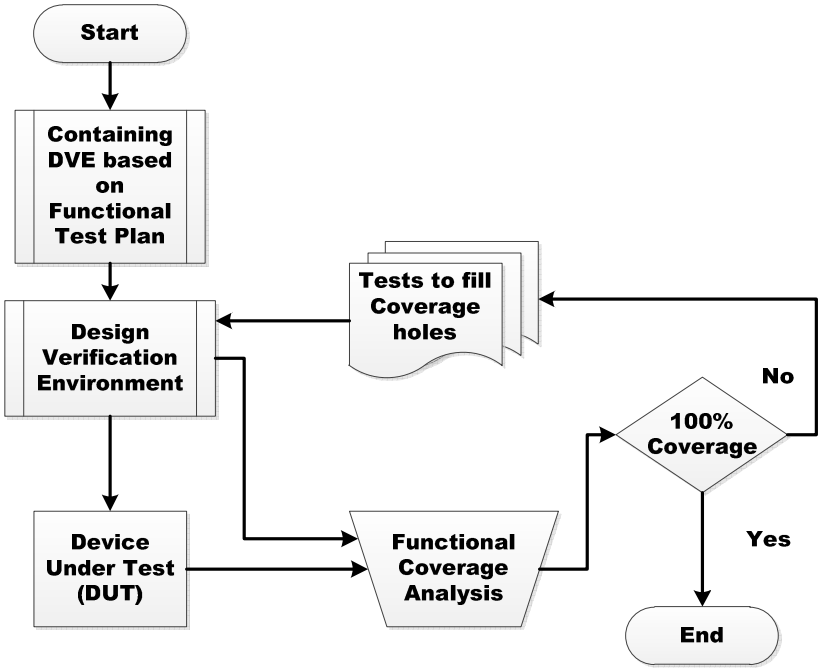

Fig 20. Flow chart for CDV

4.3 Reuse Methodology (RM)

RM is the concept inherited from the Object Oriented Programming (OOP). RM enhances the verification process by enforcing reusability and thereby reducing cost, resources and time to market. It provides a well defined test writing platform for targeting DUT functional scenarios. Test environment in this project follows Universal Verification Methodology (UVM) guidelines. UVM is a scalable, open-source multi-vendor methodology designed for multiple languages. UVM standardizes the following elements [14]

- Packaging and namespace
- Coding style and structure
- Universal Verification Component (UVC) architecture
- Reset and clocking
- Messaging and logging
- Test interface
- Sequences
- Coverage

UVM states that UVC is the basic building block of a UVM verification environment. A UVC is completely encapsulated, ready to use, configurable verification environment for an interface protocol, design module or a full-system. UVC has all the required constructs for stimulating, checking and collecting coverage information for a specific protocol. Since the UVC targets a specific protocol or

design it could be reused across projects which uses the same protocol or design. Thus UVM along with UVC provides a reusable plug and play platform for test bench design [15].

UVCs could be classified into three categories

- Interface UVC
- Module UVC
- System UVC

4.4 Interface UVC

Interface UVC is responsible for driving the input transactions across the DUT. It is aware of the DUT interface protocols and is capable of generating randomized input stimuli to be injected into the DUT. Typically interface UVC focuses on DUT input ports which can be based on bus protocol like Transmission Control Protocol (TCP), Peripheral Component Interconnect (PCI), Ethernet etc.

4.4.1 Interface UVC architecture

Fig 21 shows the block diagram of general architecture of the interface UVC used in thesis project. The various blocks of an interface UVC are discussed below [15].

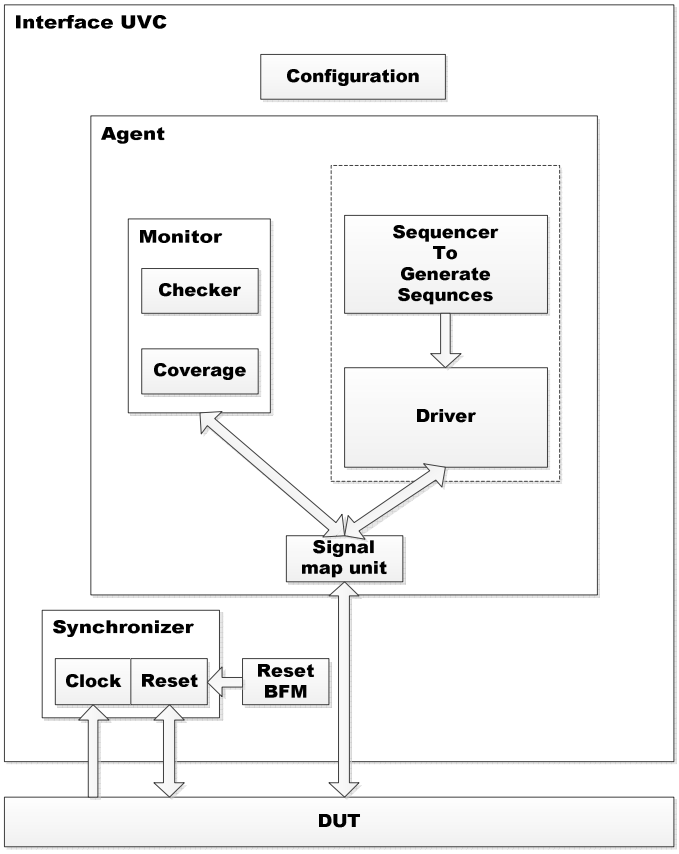

Fig 21. Interface UVC block diagram

Agent

The agent has the necessary components to drive and monitor the interface ports of DUT. The agent could be configured to operate in following modes

- Active: The agent drives and also monitors the ports of the DUT
- Passive: Agent only monitors the ports of DUT
- Protocol specific mode: Agent behavior is dependent on interface protocol

Sequencer

It is a sub-component of agent and forms the heart of the simulation. It generates streams of transaction level stimuli data, passed on to the driver. Transaction level stimuli data means that the sequencer is not protocol aware but generates data at a higher level of abstractions generally as a structure. Sequencer is not aware about the bits and byte level details and mode of transport to DUT port. The stimuli data is also constrained to be within a valid range. A sequence could in-turn call another sequence to form a nested test environment for the DUT. Generally a library of sequences is maintained to generate different kinds of transaction level data to simulate various scenarios.

Driver

The driver also known as Bus Functional Module (BFM) requests and receives the transaction level data from the sequencer. It understands the input protocol of the DUT and converts the transaction level data from the sequencer to bit level as needed by DUT port. It has necessary constructs like Time Consuming Method (TCM) to drive the DUT port with relevant data on every clock edge.

Bus Monitor

Bus monitor extracts signal level information from the DUT and translates it into data structures so as to make the data available to other components as well. It also has the checker and coverage modules.

- **Checker:** It consists of protocol checks and assertions to check for the timing behavior of the DUT.
- **Coverage:** The bus monitor emits events when the signals at the DUT port meet the sampling condition[13]. Upon emission of an appropriate event the monitor collects the required coverage information. Functional coverage tracks the number of times a variable receives a particular value during a simulation run. It provides a mechanism for tracking the unchecked data values in a design. Coverage code in Specman test bench consists of a coverage group with the variables to be tracked defined as coverage items. Cross[14] construct could be defined to track the possible combination of values for many variables together and transition coverage item could be used to track the data change [16].

Signal Map Unit

This unit connects the Specman test bench to the DUT ports and DUT internal signals[15].

[13] Sampling conditions are usually a change in the value.
[14] Cross coverage of two, three bit variable yields a sample space of 64 combinations.
[15] Specman interacts with simulator using Programming Language Interface (PLI) or VHDL Procedural Interface (VHPI).

Synchronizer

The connection of Specman to the DUT clock and reset ports is handled in the synchronizer unit. Generally the clock information is generated from the RTL design and the reset information is driven into the DUT by the interface UVC by reset BFM. The clock and reset event collected in the UVC is distributed to its components, thereby maintaining a single point of DUT contact for the clock and reset pins.

Configuration

The interface UVC has a configuration section where the UVC parameters could be configured to realize the desired behavior. Hence a verification environment could have 'n' instantiations of the same UVC but each configured differently. In other words there can be same test bench setup but with different configuration of interface UVC for each test, to generate interesting set of input stimuli.

The interface UVC could have more than one agent with each agent concerned with different protocols. Specman provides support for constructs like virtual sequences to control the sequence order in an UVC having multiple agents.

4.5 Module UVC

Module UVC models the functionality of the DUT to be verified. Thus the interface UVC has the knowledge of how to drive the input ports of the DUT and the module UVC has the knowledge as to how the DUT actually works.

4.5.1 Architecture of module UVC

Fig 22 represents the block diagram of module UVC. As depicted in the block diagram the module UVC typically consists of following sub-components [15].

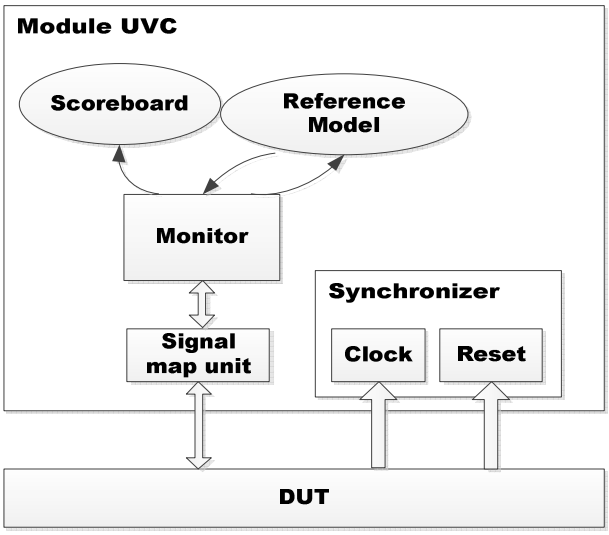

Fig 22. Module UVC block diagram

Monitor

Monitor unit in general acquires the data from the interface UVC monitors. Monitor unit could also collect the data from DUT ports directly and sometimes even from DUT internal signals which are subsequently translated into data structures. As in interface UVC monitors, module UVC monitors may optionally encapsulate checkers and coverage code.

Reference Model

Reference model implements the DUT functionality in a high level language. In the master thesis reference models are developed in C and e-code. The reference model need not be aware of the timing but only relies on the logic of the functionality to be tested. The input stimuli data collected from monitor is provided to reference model which predicts the output of DUT. The output from the reference model is returned back to the monitor which is later stored in a scoreboard.

Scoreboard

Scoreboard is a data comparison unit. It ensures whether the output collected from the DUT and the predicted output from the reference model is the same. In case of mismatch, an error is flagged by the scoreboard. Even scoreboard need not have the intelligence of the DUT timing as the timing behavior of the DUT is monitored by the checkers in the monitor unit.

4.6 System UVC

System UVC makes use of interface and module UVC and connects them to create a complete verification environment. System UVC forms a system verification environment for an entity and could be reused in a larger verification environment.

4.6.1 System UVC test bench structure

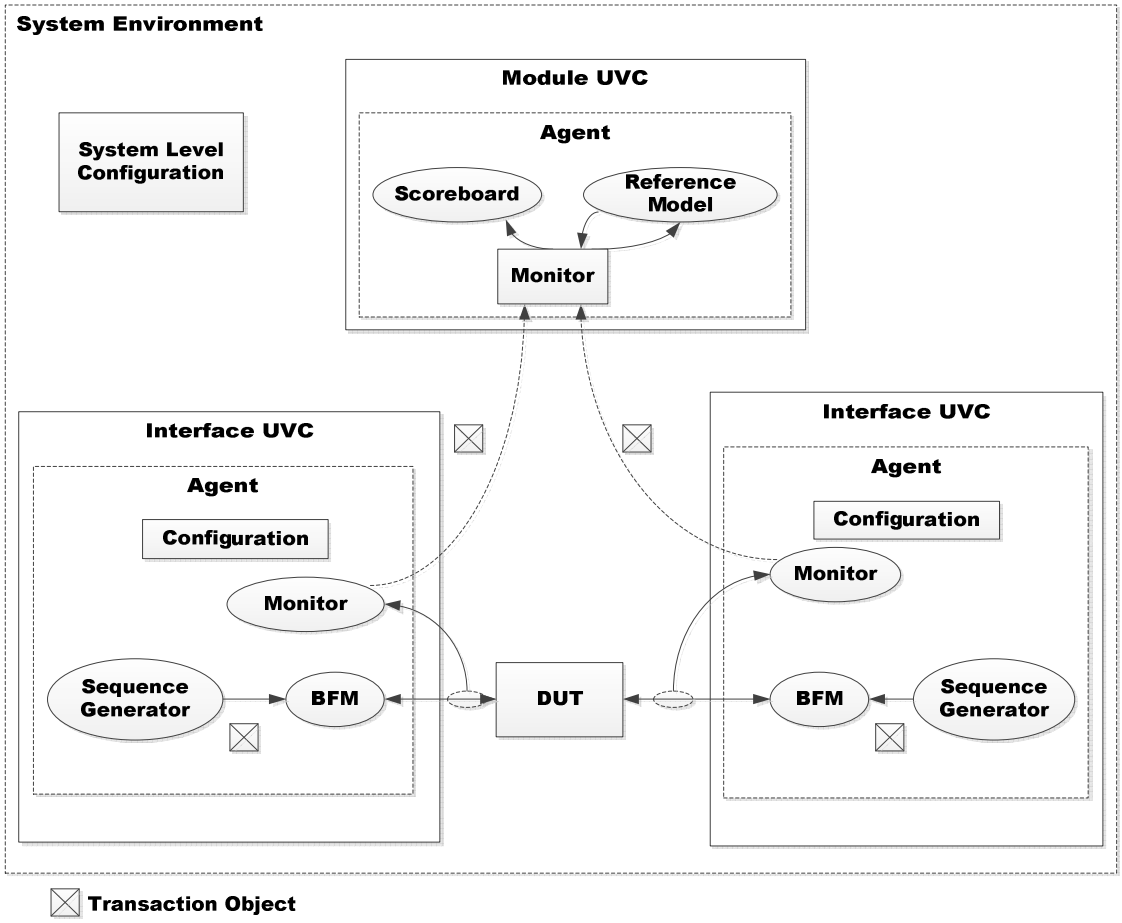

Fig 23. System test bench architecture

The interface UVC and module UVC are interconnected for a single DUT as shown in Fig 23 to form system UVC. It also provides a channel pipe for the transfer of data from interface UVC to module UVC. Verification environment configures system UVC which is specific to test scenarios and these configurations become non reusable[16] when system becomes part of a bigger system. When scaling a unit level test bench to higher level test bench the DUT needs to be driven by another adjoining DUT element and in this case interface UVC agent is configured to be passive.

[16] The configurations for larger test bench including many DUT elements are defined in its system UVC.

5 Test Infrastructure

This chapter introduces the various hardwares which are relevant to this thesis project.

5.1 Digital Unit WCDMA (DUW)

DUW is Ericsson's terminology for digital processing component of a WCDMA Radio Base Station.

5.2 Digital Processing Adapter board (DPAD)

DPAD is an Ericsson proprietary hardware which enables baseband verification of DUW. Internal details of the hardware are not discussed in detail and relevant components for this thesis are described at abstract level. DPAD can emulate many Real-time User equipments (RUE).

DPAD comprises of a Board Processor (BP), DSPs, and FPGAs. DPAD is interfaced to DUW for carrying digital antenna data.

The focus of our thesis was to verify the chip rate processing unit implemented on the FPGA's.

5.3 Chip rate unit components

Chip rate unit performs physical layer frame level processing based on 3GPP specifications [7] – [11]. The various units to be verified are highlighted below.

- Frame configuration unit
  This sets the frame specific static parameters during connection set up or release.

- Slot configuration unit
  Controls the UE behavior on slot basis and this configuration supports variable data rate.

- Data generator
  Closely coupled with slot configuration parameter like SF, the user data is acquired by reading Data generator unit which is updated by DSP at regular intervals.

- Buffer
  The user data is stored into these buffers from Data generator unit before passing through other operations.

- Modulator[17]

[17] Here modulator refers to modulation mapping described in section 3.2.12.

Data symbols in the buffer are modulated into Binary Phase Shift Keying (BPSK) or 4 Pulse Amplitude Modulation (4PAM) format.

- Spreader
  Spreader multiplies modulated value with the channelization code for each PCH. It is also combined with a scaling of the spread signals by beta factors as defined in 3GPP [9].

- IQ mapper
  Maps each PCH after spreading to either I - In phase branch or Q - Quadrature branch. Additionally all I and Q branches are combined to give the composite complex value.

- Scrambler
  Multiplication of combined I + jQ data with complex scrambling code

- Transmission Power Control (TPC)
  To enable fast power control the amplitude of the signals are ramped up or down in discrete steps and TPC behaves essentially as a multiplier.

5.4 Timing Information

The timing is always referred to a 10 ms radio frame and has 38400 chips a. Fifteen slots make up a frame and ten Hyper Frames (HFs) constitute one slot. In one HF duration data corresponding to a HF of all the 'X' number of supported UEs are generated. This is done in a time multiplexed fashion and requires a clock at FPGA which is 'X' times faster than one chip interval. Typically only few UEs are active and processing interval dedicated for other UEs generate idle data which is zero values.

6 Test bench implementation

The scope of the project is the verification of all control modules and signal processing blocks excluding filter and accumulator. Frequently the term DUT is referred and it means the module which is considered for verification. At system level the UL chip rate processing part is designated as DUT and term also implies to individual block when unit test bench is considered. All the test cases were developed using Specman tool in e-language and the associated NCSim tool simulates DUT using relevant VHDL code files.

6.1 Unit level test bench

Each block in the design has a unit level test bench. The unit level test bench comprises of the interface and module UVC for that particular design block. The interface UVC injects stimuli into the design at exact time intervals as per the input protocols of the block.

6.1.1 Frame configuration module

This module generates the UE setup and release conditions. It also sends down the TPC control parameters, scrambler initialization code and the activation time for the UE. These parameters are frame specific and generally remain constant throughout the duration when UE is active. The module can generate frame configuration data for 'X' UE. The test bench generates the frame configuration one frame ahead of the actual intended frame i.e. if an UE is to be activated in Frame 2 then the activation configuration for the UE is sent down in frame 1. Fig 24 highlights the timing diagram followed by the frame configuration module.

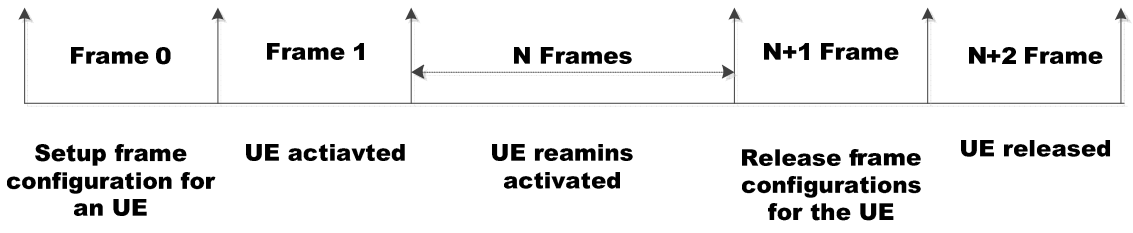

Fig 24. Timing diagram for the frame configuration

The simulation environment generates four basic sequences:

UE_SETUP: This sequence sets up a new UE at a random HFN within the frame.

UE_SETUP_SAME_HF: This sequence sets up a new UE on HFN 1.

UE_RELEASE: Releases an already set up UE.

IDLE: This maintains an idle duration during which no frame configuration is sent down from the test bench. The idle sequence is activated after the UE is setup for a configurable number of frame duration before the UE release sequence is sent down.

IDLE _STOP: This sequence maintains a configurable duration of pause after the UE is released and before an activation sequence is sent down for the same UE.

These base sequences are re-used to create higher level sequences to generate more interesting test stimuli.

Following are the higher level test sequences used by our test bench.

ALL_UE: Here all the 'X' number of UE's are setup on a randomized HFN number in the same frame and is released after running for two frames.

ALL_UE_TWO_FRAMES: Here all the 'X' number of UE is setup on a randomized HFN number in a single frame and is released after running for two frames. Again the UE's are setup and run for two more frames. This sequence creates the test scenario where an UE is setup, run for two frame duration and again the same UE is setup after being released. This sequence was helpful in detecting a bug as the pointers to memory were not getting updated correctly upon release and activation of the same UE.

FEW_UE: Here only few of the supported UE are setup at a time and after releasing these, a new set of supported UE's is setup. This sequence exercises the scenario where in a given HFN duration few UE are setup and few UE's are not (thereby the DUT is idle for this UE duration). Hence in the time multiplexed HFN slot we have an active slot where data is being generated for the active UE followed by an idle slot where no data is generated.

FEW_UE_SAME_HF: This sequence is same as the FEW_UE but the difference being that the UE's are setup on the same HFN number 1. This gives a scenario where in the time multiplexed slot of HFN 1 after some time of simulation run there is a time slot where a UE is being setup followed by a time slot where a UE is being released.

ALTERNATING_UE: In this sequence half of the supported UE's are set up on HFN 1 and the other half of UE's are setup on HFN 2. Thus in the time multiplexed HFN slot for HFN 1 and HFN 2 in the activation frame we have a scenario where an active UE slot is followed by an idle slot.

6.1.1.1 Coverage code for frame configuration module

The coverage code tracks if there was a UE setup event on the following ranges of the HF offset.

Range 1: HF offset 0.

Range 2: HF 1 to HF 40.

Range 3: HF offset 41 to HF offset 148.

Range 4: HF offset 149.

Coverage code is also written to check if the TPC and scrambler bypass options and various TPC control parameter options were indeed exercised onto the DUT.

The interface UVC, module UVC along with basic sequences (UE_SETUP, UE_RELEASE, IDLE) and few of the higher level sequences (ALL_UE, FEW _UE) were developed in [17]. The coverage code and rest of the sequences were developed in this thesis. The study of the module design was common for both the thesis.

6.1.2 Slot configuration and the data generator module

The slot configuration module generates parameters which change from one slot to another. Hence the test bench generates these parameters for every slot for an active UE and as in the frame configuration module the test bench sends the slot configuration for the given slot on the previous slot. The slot configuration parameters include the modulation type(MT) , spreading factor(SF) , channelization code , PRACH mode , number of physical channel(NR_PHCH) and the mapping of the physical channel to I or Q branch. The FPGA has a limited amount of memory thereby setting a limit on the number of UE's that could be configured as high data rate UE. To tackle this problem the test bench was architected to allocate UE's to different user capacity profiles. The test bench user is given the freedom to configure the number of UE's to be allocated to each of these profiles, but which specific UE is allocated to a given profile is randomized. The test environment also flags an error if the given test bench configuration exceeded the available FPGA memory capacity. The data generator module generates a random data such that the data size matches the SF, MT and NR_PHCH parameters of the slot.

Following are the user capacity profiles supported by the test bench:

Heavy rate UE: This profile supports 5, 6 or 7 physical channels and represents an UE utilizing high data bandwidth.

PRACH preamble UE: The UE allocated to this profile are mapped to the PRACH preamble configuration.

PRACH message UE: The UE allocated to this profile are mapped to the PRACH message configuration.

Medium rate UE: The UE allocated to this profile will have two physical channels and one physical channel can have a data rate of 64 bits / slot to 2 bits / slot and the second channel will have a data rate of 1bits/ slot.

Low rate UE: This profile supports two physical channel, both the channels could have a data rate from 1bits/ slot – 2 bits/slot.

Four Channel UE: This profile supports four physical channels and each channel could have a data rate from 4 bits/slot – 2 bits/slot.

The slot configuration module passes on the SF and MT parameters of the UE to the data generator which in-turn generates the required number of data bits for the UE for the given slot. Every 14^{th} slot of the frame the slot configuration module requests for the UE setup/release information for the upcoming next frame. If there is a setup configuration for a UE then slot configuration module generates the required slot parameters(SF,MT,NR_PHCH) one slot before the UE is to be activated on the other hand if it is a release condition for the UE then no slot configuration data is generated for that UE.

Coverage Code:

Coverage buckets were defined to track if all modulation type and spreading factor combinations were exercised onto the DUT. The transition coverage was defined for number of physical channel to check the DUT functionality for all possible physical channel transitions. Transition coverage was also defined for UE in PRACH mode.

Fig 25 on next page shows the flow chart for slot and data configuration module. The design study of this module was common to both [17] and this thesis to understand the flow of data , but the test bench implementation for this module was carried out entirely in this thesis to meet the time deadline.

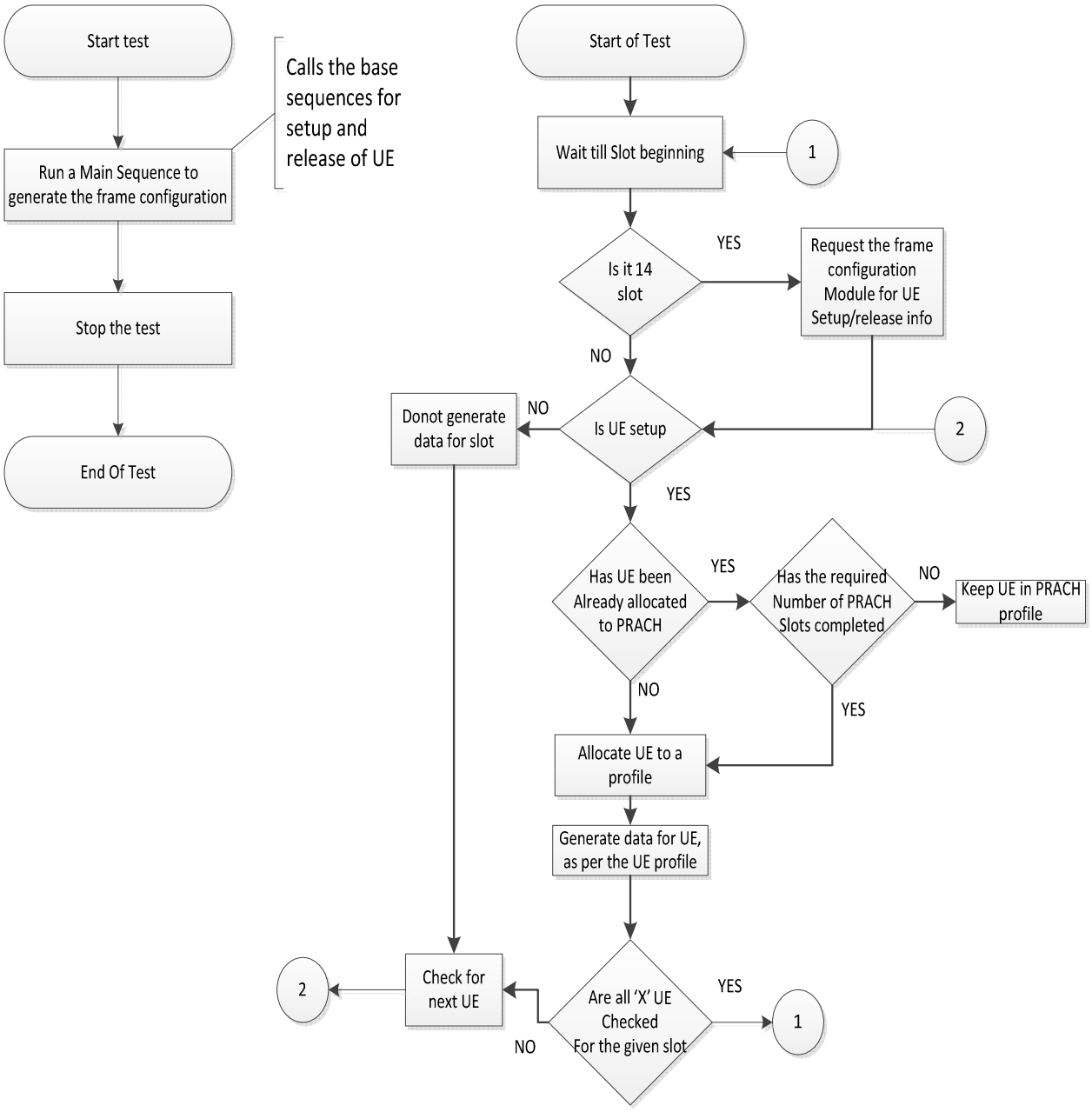

Fig 25. Flow chart of slot and data configuration module

6.1.3 Modulator module

The mapping for modulation type and the PAM configurations are mentioned in the 3GPP [9]. Sequences are developed in the interface UVC to exercise all the bit combinations for both BPSK and PAM modulation onto the DUT and check the DUT behavior. Assertions are used to check for the correct timing of the trigger strobes at the input of the DUT. Assertions are a useful way to check if the test bench is exercising the input stimuli at the right timing instance and is also useful to monitor the timing on the interface ports when the UVC is replaced by an actual DUT block in the system level testing. The module UVC has reference model developed in C to check for the correctness of the DUT.

Coverage code was architected to track if all possible spreading factor and modulation type combinations are exercised onto the DUT.

The design study of the modulator module was common to both [17] and this thesis. But the test bench implementation for this module was carried out in this thesis.

6.1.4 Spreader module

The sequence library in interface UVC is designed to exert all the beta gain configuration and channelization code index ranges for all the physical channels supported by 3GPP[9]. Timing checkers consisting of TCM are used to verify the timing behavior at the input of the DUT. The reference model for OVSF code generation is developed in C and the predicted OVSF code is further multiplied with the spreader input and beta gain factor in the e-reference model. As a part of integrating c-reference model with Specman investigation had to be made to see the Specman equivalent of the c-array types and a wrapper function call was developed for a smooth exchange of data between the Specman and ‘C’ environment.

Coverage code defines the bucket ranges for different spreading factor and channelization code combination. Coverage code also tracks the occurrence of different spreading factor and beta gain combination.

The design study of the spreader module was common to [17] and this thesis. The test bench implementation was carried out in this thesis.

6.1.5 IQ mapper module

3GPP specified different possible combinations for mapping the physical channels onto the I and Q branch [9].

The design study of this module was common to this thesis and [17], the test bench implementation was however done in [17].

6.1.6 Scrambler module

The design study of scrambler module was common to both this thesis and [17]. The test bench implementation is however done completely in [17].

6.1.7 TPC control module

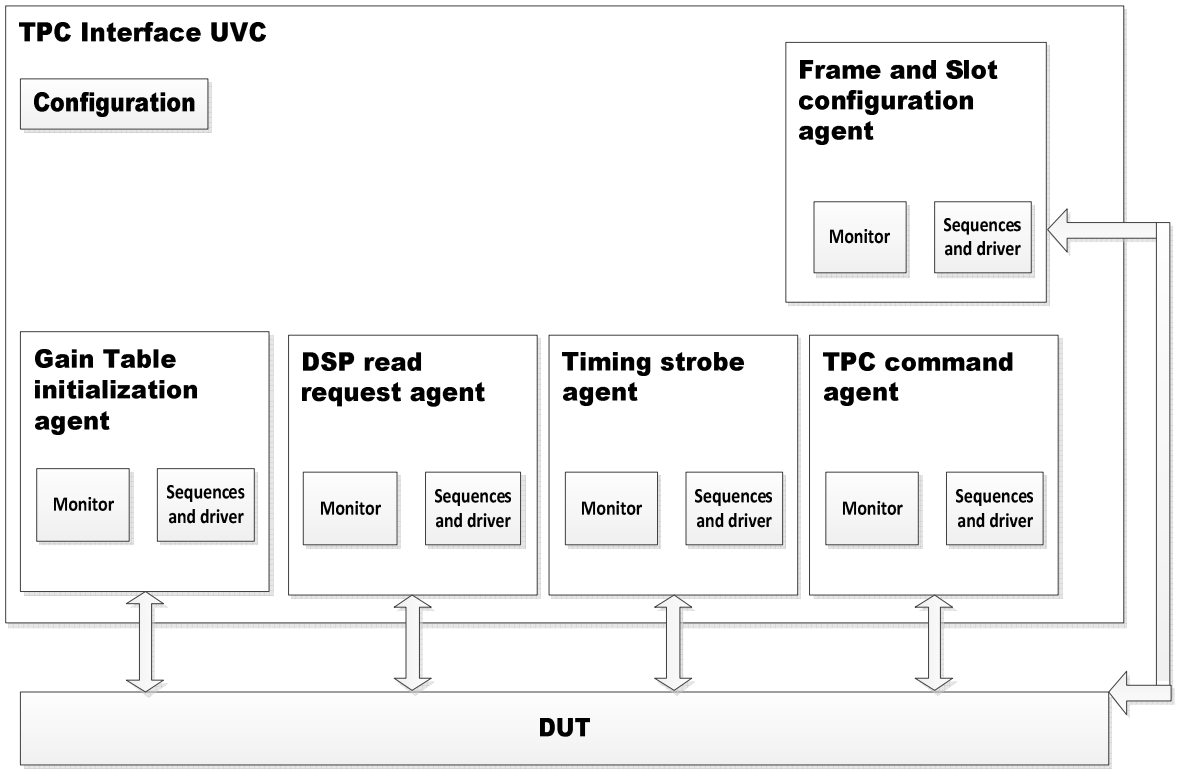

Fig 26 TPC interface UVC test bench structure

The interface UVC is developed with independent agents to handle the gain table initialization, dsp read request, timing strobe generator, tpc command generator, slot and frame configuration generator. Each agent consists of a monitor observing the respective ports. The advantage of having multiple agents for the TPC interface UVC is that it separates the control of stimuli generation for different functionalities of the design making it easier to re-use the interface UVC when testing at system level.

The gain table initialization runs once after reset and initializes the gain table for the TPC. Test bench is architected to run the gain table initialization sequence before running the slot and frame configuration sequence.

Dsp read request agent generates the TPC status requests for the UE. DSP read requests are generated at the slot beginning for a random UE.

TPC command agent keeps track of all the UE that are active and generates TPC command (increase / decrease TPC gain) for all the active UE at the beginning of a slot. The TPC command is randomly generated. If UE is de-activated then the TPC command agent stops generating the TPC commands for that UE.

Timing strobe generator agent generates the timing strobe indicating the beginning of Frame, Slot and HFN.

Slot configuration agent generates the slot specific parameters for each UE (SFNR, MT, NR_PHCH) and the frame configuration agent generates the frame specific configuration for each UE. Frame configuration agent could be configured to activate all the UE on the same HFN number in a frame or on different HFN numbers in a frame. Once UE is activated the number of frames to keep the UE active before de-activation could also be configured. If the frame configuration agent is configured to activate the UE on the same HFN number then once all the UE are released the UE is again activated on the next HFN number i.e. if all the UE are activated on HFN 0 then after de-activation the UE are again activated on the HFN 1. Thus the slot and frame configuration agents activate and de-activate the UE continuously i.e. there is no stopping condition defined in the interface UVC.

It should be noted that each of the agents exert the stimuli onto the DUT independent of others making the test bench capable of exerting parallel input stimuli.

The module UVC has the reference model developed in ‘e’ which models the parallel behavior of the DUT.

The interface UVC for this module was developed in this thesis whereas the module UVC implementation along with coverage metrics was carried out in [17].

6.2 System Level Test Bench Architecture

System level test bench is created using a hierarchical approach by combining few unit level blocks together and then instantiating it in a higher lever system UVC with other blocks.

6.2.1 Hierarchical Instantiation of UVCs

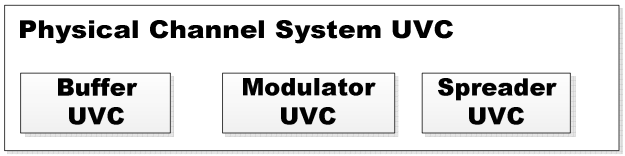

Fig 27. Components of Physical Channel System UVC

Physical Channel System UVC is a fundamental block level UVC for one PCH which comprises of interface and module UVCs for

- Buffer
- Modulator
- Spreader

Each PCH is monitored by above mentioned unit level UVCs (Fig 27) and a pipe encapsulates eight such blocks. The interface UVCs of all the three modules are set to passive and it is expected that stimulus is provided by the upper hierarchy of UVC. Owing to identical architecture of physical channel system UVC, it is reused to construct the Pipe System UVC.

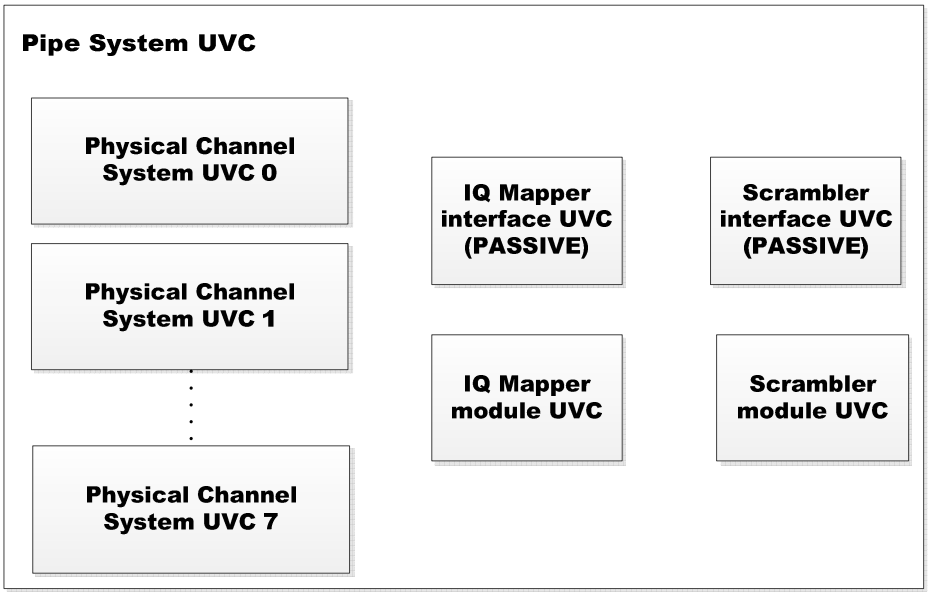

Fig 28. Block Diagram of Pipe System UVC hierarchy

A pipe system UVC is constructed by instantiating the physical channel system UVC eight times, IQ mapper, scrambler as shown in Fig 28. The interface UVCs for IQ mapper and scrambler are set to passive to enable only monitoring and validation of the respective functionality.

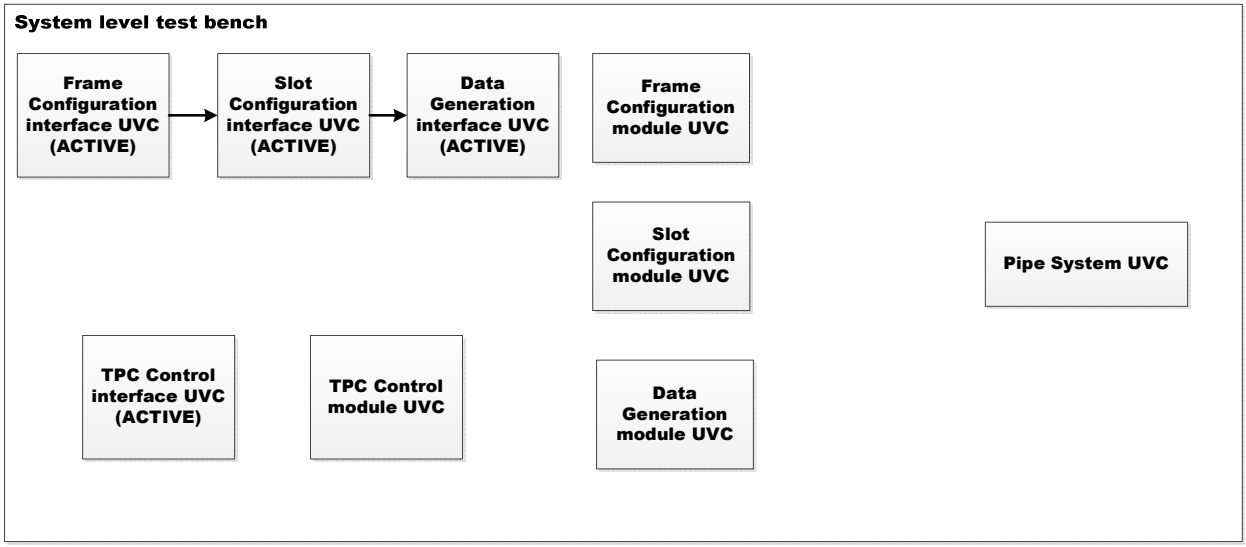

Fig 29. System Level Test Bench

The main system environment (Fig 29) consists of pipe system UVC instantiations, instantiations of interface UVC for frame configuration, slot configuration, data generation and TPC control. The interface UVCs of frame configuration, slot configuration and data generation modules are active and drive the input signals of the DUT. Thus there is a single point of input for the stimuli to be injected into the DUT. These three interface UVCs can generate stimuli for all 'X' supported UE's. The co-ordination of frame configuration, slot configuration and data generation test benches are represented by arrows in Fig 29 which are method ports supported in e-language.

TPC interface UVC independently drives the DUT. TPC command agent, gain table initialization agent and DSP read request agent in the TPC interface UVC are set to active. Whereas timing strobe agent and frame and slot configuration agent are set to passive in TPC interface UVC. The instantiations of module UVCs for frame configuration, slot configuration and data generation modules for the pipe is also included at this level. There is only one TPC control module UVC which verifies TPC control operation of both the pipes. The main system environment has test specific configurations and hence is not a re-usable component. All the test case scenarios discussed for frame configuration and slot configuration modules are re-iterated in the system level test bench.

6.2.2 Timing Diagram for System Level Test Bench

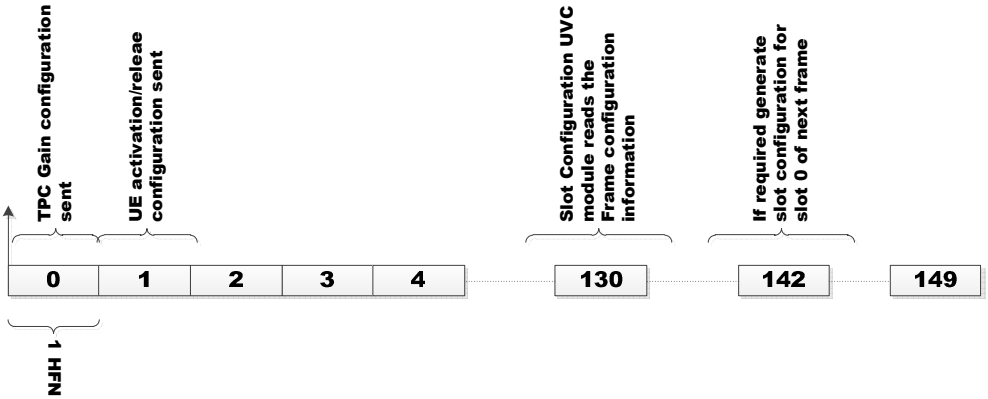

Fig 30. Timing Diagram for Frame 0

Fig 30 and Fig 31 demonstrate the timing of how different configuration sequences are injected into the DUT. As demonstrated in Fig 31 for the very first frame, FRAME-0, the TPC gain table initialization sequence is enabled only on HF0 in FRAME0. The UE setup information for the next frame (FRAME 1) is sent on successive HF 1 for all UEs which need to be activated. The slot configuration interface UVC learns the frame configuration information intended to be valid in next frame in HF 130. If there are UEs to be activated on slot 0 of FRAME 1 then the slot configuration is provided to the DUT in HF 142. From FRAME 1 onwards (Fig 31) on every second HF of each slot, any new slot configuration for the next slot is transmitted to the DUT. Beginning of every slot the TPC specific commands and TPC status DSP read requests arrive at DUT.

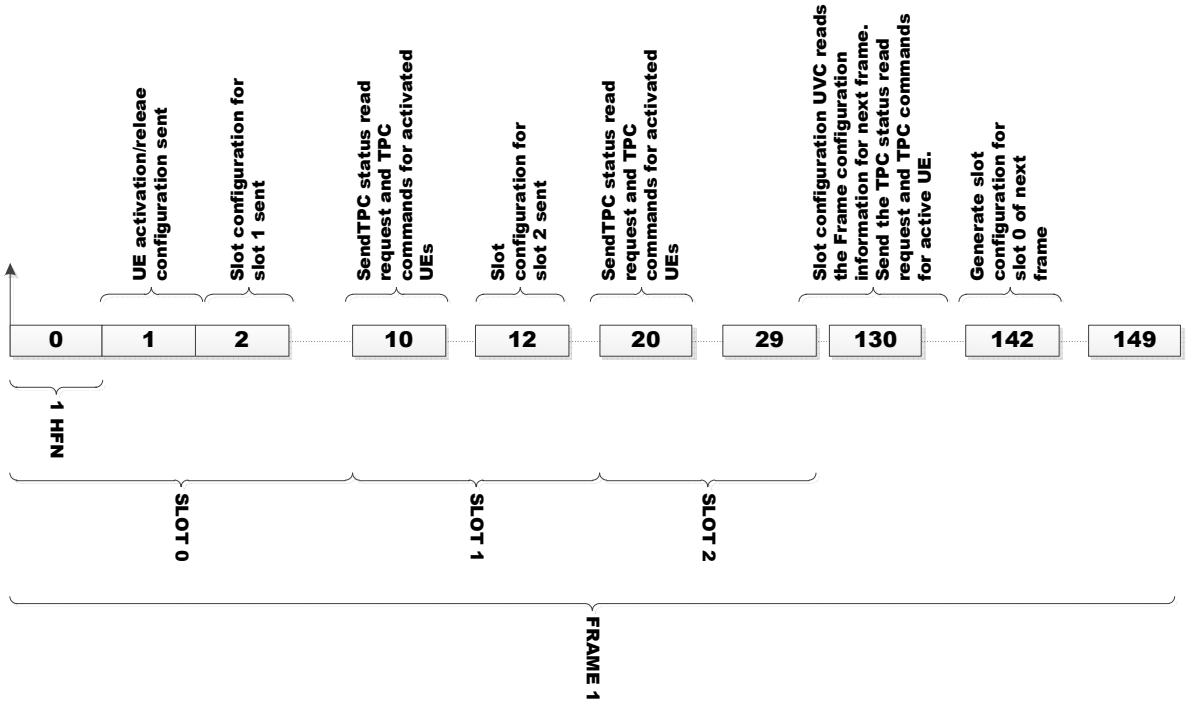

Fig 31. Timing diagram from the onset of Frame 1

7 Result

This section describes the coverage results, errors detected by test bench and conclusion.

7.1 Coverage results

Verification is carried out for the two pipes at both system level and unit level. 94% coverage at system level and close to 100% coverage at unit level is achieved. Also the test bench written for pipe 0 can be reused when simulating pipe 1. The same coverage metrics are applied at both levels of verification to obtain coverage.

Frame Configuration Unit

The coverage code is written for the DUT to track if there was any UE setup event on the following ranges of HF number
Range 1: HF 0
Range 2: HF 1 to HF 40
Range 3: HF offset 41 to 148
Range 4: HF 149

Slot Configuration Unit

Coverage buckets were defined to track if all modulation type and spreading factor combinations were exercised on the DUT. The transition coverage was defined for number of PCH to check the DUT functionality for all possible PCH transitions.

Modulation

Coverage metrics are defined for two modulation types BPSK and 4PAM.

Spreader

Coverage code defines the coverage bucket ranges for different SF and channelization code combination. Cross coverage code also tracks the occurrence of different SF and beta gain combinations.

IQ Mapper

Table 6 provides the different coverage items and the sub range of possible values is given a name [17].

Table 6. Coverage for IQ mapper

Parameter	Coverage labels	Coverage ranges
Spread data	Low Value, Negative Value, Positive Value	[-127 to 127], [-32768 to -1600] and [1600 to 32767]
Number of PCHs	-	1 to 8
Number of I branches (Both in VALID and INVALID)	-	[1 to 4] in VALID and [5 to 8] in INVALID
IQ map	-	[0 to 255]
Range of Output values	Positive and Negative	[0 to 8191], [-8192 to -1]

Scrambler

The coverage metrics for scrambler are defined in Table 7[17].

Table 7. Coverage for Scrambler

Parameter	Coverage labels	Coverage ranges
Type of Frame	DPCH, PRACH preamble and PRACH message	-
Scrambling initialization value	Low, Mid and High	[0 to 512], [513 to 131072] and [131073 to 33554431]
IQ input and outputs	Positive and Negative values	[0 to 8191], [-8192 to -1]

TPC control

TPC coverage metrics include the TPC commands, step size, TPC status request by DSP for different UEs, range of gain values and default TPC pointer values.

7.2 Findings

Errors in the DUT were observed when system level test cases were executed. Detailed background of these conditions cannot be explained because of confidentiality. But in general these bugs could be detected only under scenario of UE activation and hence they had missed the directed test bench developed at Ericsson.

7.3 Optimization

The simulation cycles increase significantly when system UVC combines many unit level test benches. To overcome this drawback optimization procedure was followed and simulation time was reduced from 2.5 minutes per HF to 8 seconds per HF[18]. The steps followed in order to achieve higher performance are listed below.

- Print[19] function is used for displaying messages on the console. Print statements consume more CPU cycles and avoided. Alternate message function is suggested by Cadence which is used to print messages on screen.
- To remove sync or wait functions which are sampled every clock cycle. Some functions predominantly in BFM continuously polls for a signal transition or some event. An event expected to recur after many clock cycles can be sampled at lesser frequency.
- The coverage code is sampled every HF rather than every clock cycle wherever possible. This might reduce the coverage to a small degree but allows the simulation to run for many frames in less time. Also for some parameters with lesser number of bits coverage can be obtained sooner.
- Precompiled e-code can be used if there is no further modification in design and run in batch mode[20].

[18] The time measurements are made by human observation of timing diagram outputs in a graphical mode.
[19] Print is similar to *printf* construct in C language and helpful in debugging.
[20] Batch mode is a non graphical mode which is faster.

8 Conclusion

Both unit level and system level testing was carried out to verify the chip rate processing unit. The design specifications were captured into a VPLAN and were tagged to indicate the specific 3GPP requirements in the specification. The coverage metrics were mapped to these VPLAN and upon running the test a user friendly readable report was generated to track the percentage of coverage for the design goals. The re-use methodology of UVM is a powerful mechanism to build a scalable and configurable test bench. Though it takes a steep learning curve to develop a test bench based on UVM methodology the actual power of the test bench in un-covering the bugs is noticeable. The simulation time could be a bottleneck when verifying complex designs but again the verification automation reduces this impact as the tests could be launched in the evening and the results could be observed for all the test scenarios when starting the work back in the morning. The debugging time duration is also considerably reduced as the test bench could pinpoint to the sub module where the bug was detected.

9 Future Work

This project focused only chip rate accelerator FPGA in DPAD. A test bench to support verification of the complete FPGA can be carried out in future. Further the design of system test bench can be extended to other FPGAs and DSP. This could become a powerful platform to enable a board level verification and evaluate the performance of DPAD. It also becomes a challenge to intelligently reduce the simulation time and improve the co-ordination among different UVCs.

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