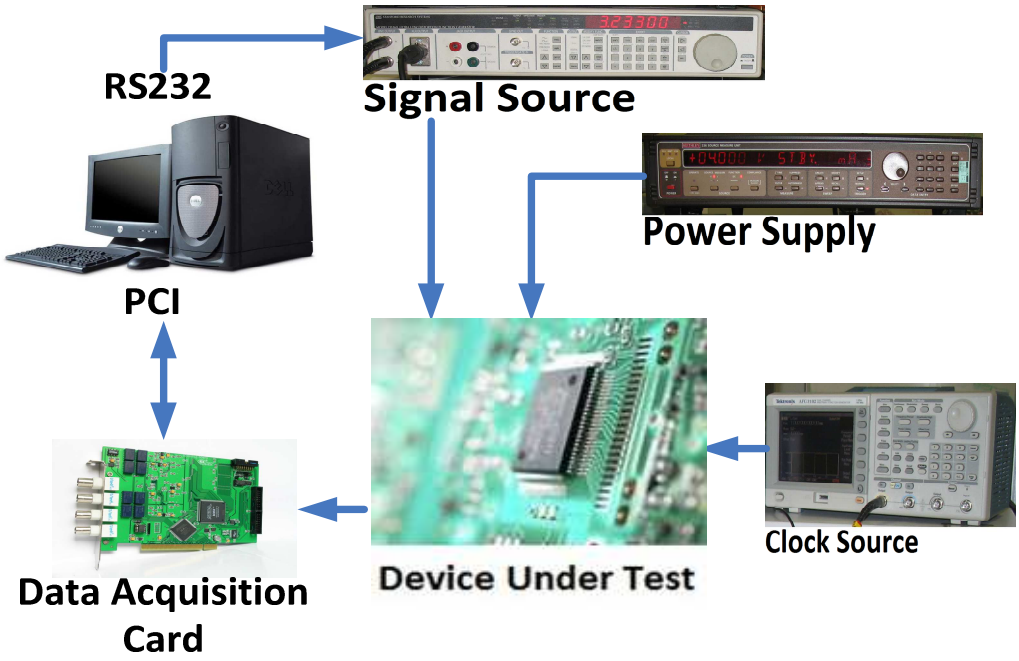
CHALMERS



Software and Hardware Testing Platform for High Resolution ADCs

Master of Science Thesis in Integrated Electronic Systems Design

Ahsan Shehzad

Chalmers University of Technology

Department of Computer Science and Engineering
Göteborg, Sweden, September 2011

Software and Hardware Testing platform for High Resolution ADCs
Ahsan Shehzad

Supervisor: Francesco Cannillo

Interuniversity Microelectronics Centre (IMEC)
Ultra Low Power and Extreme Electronics Group (ULPEXEL)
Kapeldreef 75, 3001
Belgium
Email: cannillo@imec.be

Examiner: Prof. Per Larsson-Edefors

Chalmers University of Technology
Department of Computer Science and Engineering
SE-41296 Goteborg
Sweden
Department of Computer Science and Engineering
Göteborg, Sweden, September 2011

Acknowledgments

- Francesco Cannillo has been an excellent supervisor. He always replied me softly and explained me very well whenever I asked any question. During my time at IMEC, I have learned a lot from him not only technically but also professionally. He cares a lot about student's learning and tries his best to solve his every kind of problem.
- Per Larsson-Edefors has been my examiner. He has reviewed my report at his best. I have learned report writing from him.
- Jan Putzeys helped me very much during PCB design. I have learned PADS Logic software from him. He is very cooperative and explains everything.
- Tom Torfs has solved my problems related to firmware development during my thesis and guided me about working in the LAB.
- I have asked questions several times with many of my colleagues and they always replied me very well. I can never forget the moments that I have spent at IMEC.

Abstract

Performance evaluation of high resolution ADCs is a growing challenge in industry. This report describes a software and hardware testing platform for high resolution ADCs. It explains the requirements of a high resolution ADC under test. Requirements of signal to noise ratio (SNR) of input signal, requirements of allowed jitter on sampling clock and requirements of noise on the power supplies are explored. Noise from different sources like current noise, voltage noise and thermal noise are estimated for components of supply and then verified by implementation results. Signal integrity precautions affecting resolution are also explored and implemented.

Abbreviations

ADC Analog to Digital Converter

DAC Digital to Analog Converter

Op-Amp Operational Amplifier

SNR Signal to Noise Ratio

SNDR Signal to Noise and Distortion Ratio

SFDR Spurious Free Dynamic Range

THD Total Harmonic Distortion

LSB Least Significant Bit

PCB Printed Circuit Board

FFT Fast Fourier Transform

PSRR Power Supply Rejection Ratio

SRS Stanford Research System

HDF Hierarchical Data Format

LDO Low Dropout

RMS Root Mean Square

EMI Electro-Magnetic Interference

Table of Contents

1 Introduction 11

1.1 Software and Hardware Testing Platform for High Resolution ADCs 11

1.2 Motivation 11

1.3 Thesis Organization 11

1.4 Background 12

1.4.1 Nyquist ADC 12

1.4.2 Delta Sigma ($\Delta\Sigma$) ADC 14

1.4.3 Coherent Sampling 15

1.4.4 Windowing 15

1.4.5 Noise Sources 16

1.4.6 Thermal Noise 16

1.4.7 Operational Amplifier Noise (1/f Noise) 17

2 Evaluation of Equipment that Satisfy Requirements of Device under Test 18

2.1 Requirements from the Equipment 18

2.1.1 Power Supply 18

2.1.2 Data Acquisition 18

2.1.3 Signal Source 19

2.1.4 Clock Source 19

2.2 Evaluation Results for Different Equipment 21

3 Evaluation of Components that Satisfy Low Noise Requirement 23

3.1 Requirement on the Noise from the Components 23

3.2 Design of Power Supplies 23

3.2.1 Low Pass RC Filter Design and Implementation 26

3.3 Main Power Supply 28

4 PCB for IMEC Modulator 31

4.1 Architecture of PCB (IMEC's Modulator) 31

4.2 Digital Interface PCB 32

4.3 Signal Integrity Precautions 32

4.4 Measured Values of Noise on the Power Supplies 33

5 PCB for Off-The-Shelf Modulators 36

5.1 Architecture of PCB (Off-The-Shelf Modulators) 36

5.2 Spectrum of Signal Digitized by ADS1203 37
6 Conclusion and Future Enhancements 40
7 References 41
8 APPENDICES 42
8.1 APPENDIX A 42

List of Figures

Figure 1: Quantization 13
Figure 2: Spectrum of Quantized Signal 14
Figure 3: Delta Sigma ADC [9] 15
Figure 4: Operational Amplifier Noise Model 17
Figure 5: Test Setup Block Diagram 18
Figure 6: Effect of Jitter of Clock Source on SNR of Nyquist ADC 20
Figure 7: Effect of Jitter of Clock Source on Effective Number of Bits 21
Figure 8: Schematic of Voltage Tunable Power Source 24
Figure 9: Operational Amplifier Noise Model 24
Figure 10: Voltage and Current Noise Density 25
Figure 11: RC Low Pass Filter 26
Figure 12: RMS Noise Voltage with Different Cut-Off Frequencies of RC Filter 27
Figure 13: Non-Ideal Capacitor Model 27
Figure 14: Non-Ideal Behavior of Capacitor [7] 27
Figure 15: Ultra-Low-Noise LDO 29
Figure 16: Noise Density at the Output of LDO 29
Figure 17: RMS Noise Voltage with Different Cut-Off Frequencies of RC Filter 30
Figure 18: IMEC Modulator Test PCB 31
Figure 19: µ-Controller Interface PCB 32
Figure 20: Spectrum and Integrated Noise of Input Supply 33
Figure 21: Spectrum of Output of Ultra-Low-Noise LDO 34
Figure 22: Spectrum of Analog Supply by LT6233 35
Figure 23: Spectrum of Digital Supply by LT6233 35
Figure 24: ADS1203, ADS1201 and Clock Source PCB 36
Figure 25: Spectrum with 0.0 VP-P Input 37
Figure 26: Spectrum with 0.5 VP-P Input 38
Figure 27: Spectrum with Inputs Shorted to Ground 38
Figure 28: ENOB versus OSR for ADS1203 39
Figure 29: SNR, SNDR versus Input Amplitude (ADS1203) 39

List of Tables

Table 1: Window Types and Bins of Signal Power 16
Table 2: List of Equipment That Satisfy SNR Requirement 21
Table 3: Quantization Error of IMEC Modulator Chip 23
Table 4: RMS Noise of Op-Amp (LT6233) in the Bandwidth of 100 kHz 25

1 Introduction

1.1 Software and Hardware Testing Platform for High Resolution ADCs

The platform in focus of this thesis report is a software and hardware setup on which test of a high resolution 2nd order $\Delta\Sigma$ modulator is performed. This includes application of a high SNR test signal, a low jitter clock and data acquisition from the chip. The software side includes post-processing (Fast Fourier Transform based analysis) to be applied to the $\Delta\Sigma$ ADC. The $\Delta\Sigma$ ADCs consists of two main functional blocks: modulator and decimator. The modulator oversamples the input signal and pushes the quantization noise at high frequency in order to increase the SNR in the signal bandwidth. The decimator filters the modulator output bit stream (at the oversampling frequency) and removes out of band quantization noise. The platform is intended to provide different test setups for device under test and to provide low noise input signal, low jitter sampling clock and low noise power supplies.

1.2 Motivation

Measurement of high resolution $\Delta\Sigma$ ADCs requires components with very low noise and equipment with higher SNR output signal. In order to test a prototype chip, a number of different test configurations are also needed. These test configurations include step by step testing of the chip on different portions. Considering package requirements of chip, requirement of test points on different pins and to accomplish the requirement of noise and different test configurations for the device under test, it was not possible to use a readymade solution. So it was decided to develop a customized platform for testing.

For a 16 bit ADC, the LSB value is equal to the full scale input range divided by the number of levels of the quantizer. The quantization noise is obtained by dividing this LSB value with the square root of 12 [13]. It is targeted that the noise on the power supplies of the test setup should be below the quantization noise in order to get the maximum effective number of bits (ENOB) possible from ADC. This ensures that the test setup does not introduce additional noise. It is also decided to use a test signal with a resolution at least two bits higher than the ADC under test. The targeted resolution for IMECs modulator is 16 bits and the quantization noise is 8 μV_{RMS}. The bandwidth of interest for the input signal is 1 kHz and 256 Hz, so theoretical and measured values of total noise are considered for a bandwidth of 1 kHz.

1.3 Thesis Organization

As the title of the thesis describes that there are two main parts of the project named hardware and software. The software part includes data acquisition and post processing (FFT-based analysis) to be applied to the output of delta sigma modulator. The hardware part includes identification of suitable pieces of equipment and components that satisfy the

high SNR and low distortion requirement. The hardware part also includes signal integrity precautions and implementation of electronics design on PCB.

Chapter one describes the basic information and necessary concepts in order to build up the reader's background and interest in the topic. At first a simple example of Nyquist ADC is taken which explains FFT-based analysis and performance evaluation parameters of ADCs. Then a simple architecture of a 1st order $\Delta\Sigma$ ADC is explained. The factors affecting accuracy in performance evaluation are coherent sampling and windowing. Later on sources of noise are identified and operational amplifier (op-amp) noise calculation is explained.

Chapter two explains the requirements from the equipment. The equipment is used for power supply, data acquisition card, signal source and clock source. Thus, the equipment evaluation and selection, considering sampling rate of data acquisition card, SNR of signal source and jitter of clock source, are explained here.

Chapter three explains the evaluation of low noise components and its electronics design. It also explains how to calculate total wideband noise and how to design and implement an RC filter to reduce it.

Chapter four details the architecture of the main modulator's PCB and its digital interface PCB. Signal integrity precautions are also explained and measured values of noise on the PCB are shown.

Chapter five details the PCB for an off-the-shelf modulator chip and verifies that the electronics design of hardware used for measuring high resolution (16 bits) ADCs is good enough.

Chapter six provides a conclusion and a discussion on the future enhancements that can be done in the project.

1.4 Background

1.4.1 Nyquist ADC

This section will describe a simple Nyquist ADC, the process of quantization and Fast Fourier Transform (FFT) based analysis. Some simulations are performed by implementing a simple quantizer (Nyquist ADC) and then applying a sine wave at the input and estimating SNR at the output by computing a windowed FFT. Some types of windows that can be used are rectangular, Hann and Hann^2[11]. This task helps in developing an understanding of different parameters which represent performance of high resolution ADCs. Figure 1 shows a sine wave signal which was sampled about 26 times higher than its own frequency and it was passed through a 10 bit quantizer(1024 levels of quantization). Figure 2 displays the spectrum of quantized signal. The Hann window is used in computing FFT. Different parameters like signal to noise ratio (SNR), signal to noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) are calculated. Definitions of these parameters are given in Appendix A. The simulation is done with full scale input (1 volt peak to peak). Ideally, a 10 bit Nyquist ADC should give a maximum SNR with equation 1 which is 62 dB.

Since, in this case, the signal has a second harmonic, therefore the value of SNDR is less than SNR.

SFDR measures the harmonic imperfections of the ADC under test. Thus it is crucial that the stimulus to the device under test is as spectrally pure as possible[8]. SFDR can be used to judge the dynamic performance of the signal generator. Hence a good signal source has a maximum SFDR and the SFDR of the device under test describes its dynamic performance. In order to get a maximum value of effective number of bits (ENOB), the SFDR of the function generator used as signal source should be as low as possible.

$$\text{SNR} = \text{ENOB} * 6.02 + 1.76 \qquad (1)$$

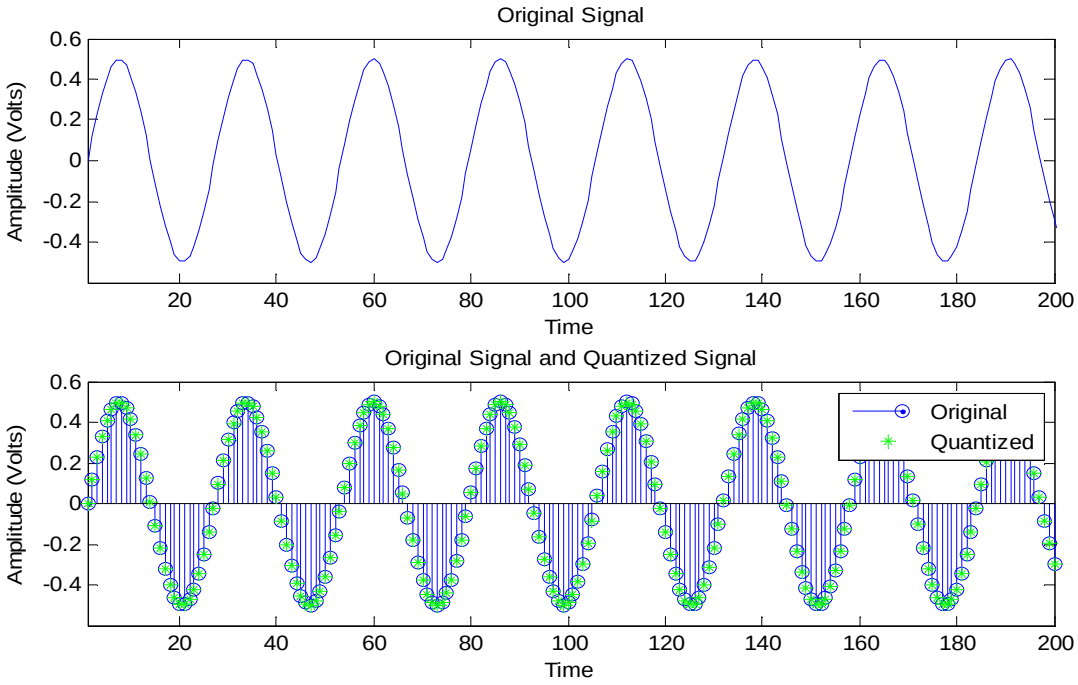


Figure 1: Quantization

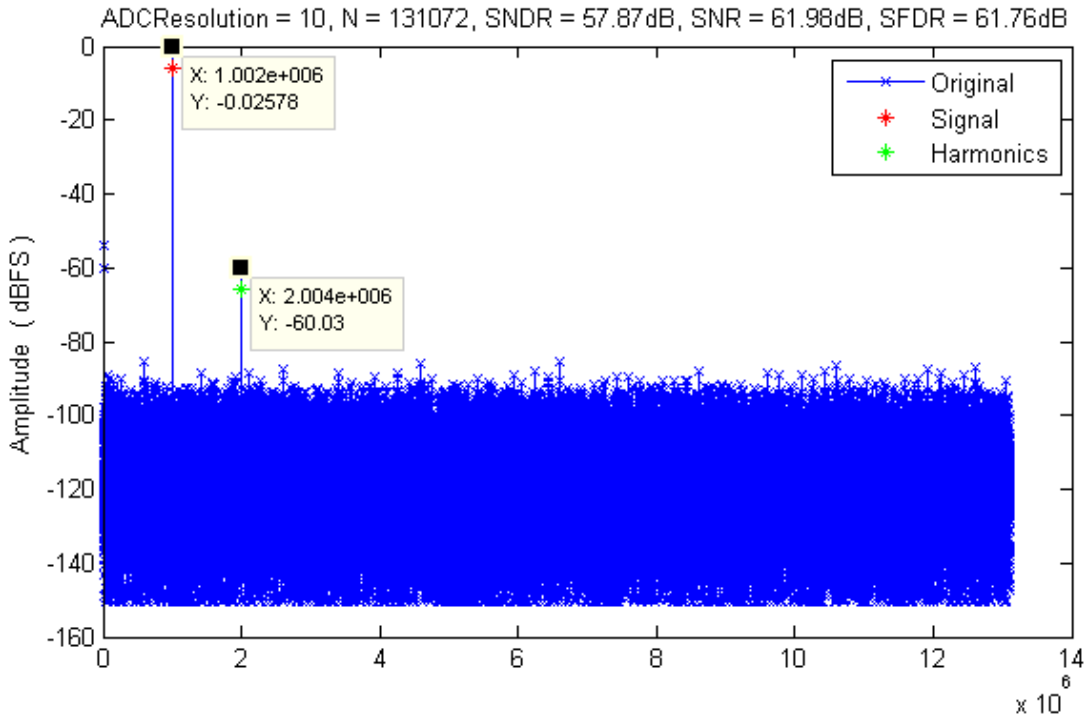


Figure 2: Spectrum of Quantized Signal

1.4.2 Delta Sigma (ΔΣ) ADC

The test platform is designed for a 2nd order ΔΣ modulator and its introduction provides a background for understanding its requirements. The delta sigma (ΔΣ) conversion technique has been in use for many years but recent technological advances made it practical and its use is increasing day by day. Delta sigma conversion is a low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals. In order to understand the delta sigma converter, it is necessary to understand the following terms [9].

Noise Shaping Filter (or Integrator)

The noise shaping filter (or integrator) of a delta sigma converter distributes the converter's quantization error (or noise) in such a way that it is very low in the required bandwidth.

Oversampling

Oversampling is simply the act of sampling the input signal at a frequency much greater than the Nyquist frequency and it decreases the quantization noise in the bandwidth of interest.

Digital Filter

An on-chip digital filter is used to attenuate signals and noise that are outside the band of interest.

Decimation

Decimation is the act of reducing the data rate down from the oversampling rate without losing information.

Figure 3 shows a block diagram of a first order delta sigma ADC. The input signal X enters into the modulator via a summing junction and passes through the integrator. Next, a comparator is being fed by the integrator. The comparator is actually a one bit quantizer and its output is fed back into the summing junction via a one bit digital-to-analog converter (DAC). The comparator output also passes through the digital filter and emerges at the output (Y). The feedback loop forces the average of the signal W to be equal to the input signal X [9].

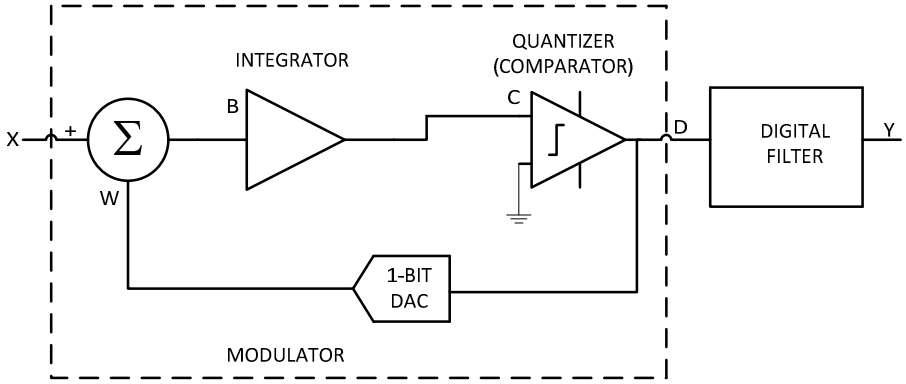


Figure 3: Delta Sigma ADC [9]

The function of the digital filter is to provide a sharp cut-off at the bandwidth of interest which removes out of band quantization noise and signals. So as much as quantization noise is moved towards higher frequencies, the resolution of the converter can be increased [9].

Hence, the comparison among two different types of converters, $\Delta\Sigma$ and Nyquist shows that $\Delta\Sigma$ converters take the advantage of oversampling and increases the resolution of the converter more intelligently. Still it only works with limited bandwidths.

1.4.3 Coherent Sampling

A useful technique for evaluating the dynamic performance of data converters is coherent sampling. This method increases the spectral resolution of an FFT and replaces the need for windowed sampling. With coherent sampling, the power of the signal bins is concentrated in a few known number of bins; without the coherence condition, the signal power bleeds into the neighboring bins which is called leakage. So this technique gives a correct estimate of SNR and other parameters as well. Coherent sampling describes the sampling of a periodic signal, where an integer number of its cycles fit into a predefined sampling window [1].

1.4.4 Windowing

Windowing is the act of multiplying the signal to be analyzed by a window function before subjecting it to an FFT. Since it is not possible to get the spectrum for an infinite-length record of data, windowing is inevitable.

Multiplication in time domain is convolution in frequency domain. So the spectrum of windowed signal is a spectrum of the unwindowed signal convolved with the window. The

number of bins representing power of the signal depends on the type of window that is used. Table 1 shows the number of bins used for representing power of the signal [11].

Type of Window	Number of bins representing signal power
Rectangular	1
Hann	3
Hann^2	5

Table 1: Window Types and Bins of Signal Power

It is decided to use coherent sampling with windowing in order to minimize leakage as much as possible. Mathematically, the coherence condition can be expressed by equation (2) [1].

$$\frac{F_{IN}}{F_{SAMPLE}} = \frac{N_{WINDOW}}{N_{RECORD}} \quad (2)$$

F_{IN}: periodic input signal
F_{SAMPLE}: sampling/clock frequency of the ADC under test
N_{WINDOW}: integer number of cycles within the sampling window
N_{RECORD}: number of data points in the sampling window or FFT

In order to achieve a coherence condition, N_{RECORD} should be a power of 2 and an odd number of N_{WINDOW} should be used. In Figure 2, the coherence condition is achieved with the following parameters.

F_{IN} = 1.0018*10^6 Hz
F_{SAMPLE} = 26.2144*10^6 Hz
N_{RECORD} = 131072
N_{WINDOW} = 5009

A Hann window is used and, therefore, the power of signal bins is concentrated in only three bins.

1.4.5 Noise Sources

It is targeted that the noise on the power supply of modulator should be less than its quantization error. The most common sources of noise are components used in the power supply and they produce thermal noise (current noise and voltage noise) in the circuit.

1.4.6 Thermal Noise

Thermal noise is being generated by random motion of electrons in a conductor and because this motion increases with temperature, so does the magnitude of thermal noise. Thermal noise can be increased as a random variation in the voltage present across the component (e.g. a resistor). The power contained within a thermal noise signal is directly proportional to temperature and bandwidth [2]. Thermal noise is expressed by equation 3.

$$e_n = \sqrt{4 * k * T * R * \Delta f} \quad (3)$$

where "e_n" is the RMS noise voltage.

T = temperature in Kelvin.

R = resistance in Ohms (Ω).

Δf = noise bandwidth frequency (Hz).

k = Boltzmann's constant 1.381E-23 (Joules/Kelvin).

1.4.7 Operational Amplifier Noise (1/f Noise)

Operational amplifier (Op-Amp) noise at its output can be calculated by considering the contribution of different noise sources present in the circuit. The voltage noise spectral density is a measurement of RMS noise voltage (Nano Volt) per square root Hertz (or commonly: $\frac{nV}{\sqrt{Hz}}$). If the noise spectral density is flat, then this noise is called broadband noise. In the case of a resistor, its noise has a flat spectral density so thermal noise can be called broadband noise. But op-amps have a low frequency noise region that does not have a flat spectral density plot. This noise is called 1/f noise, flicker noise or low frequency noise. Because the power spectrum of 1/f noise falls at a rate of 1/f so it means that the voltage spectrum falls at a rate of $\sqrt{1/f}$. The standard operational amplifier noise model is shown in Figure 4.

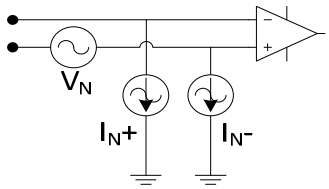


Figure 4: Operational Amplifier Noise Model

At the input of the op-amp, two current noise sources (for biasing currents) and a voltage noise source can be modeled. Then the noise spectral density of current and voltage can be computed from the datasheet of the op-amps. The integration of noise spectral density gives the area under the curve; this is actually the RMS value of noise [2].

2 Evaluation of Equipment that Satisfy Requirements of Device under Test

2.1 Requirements from the Equipment

The evaluation of equipment includes evaluating the quality of signal that is being generated by the equipment. The equipment is used in testing for the purposes explained in figure 5. Figure 5 also explains system level block diagram.

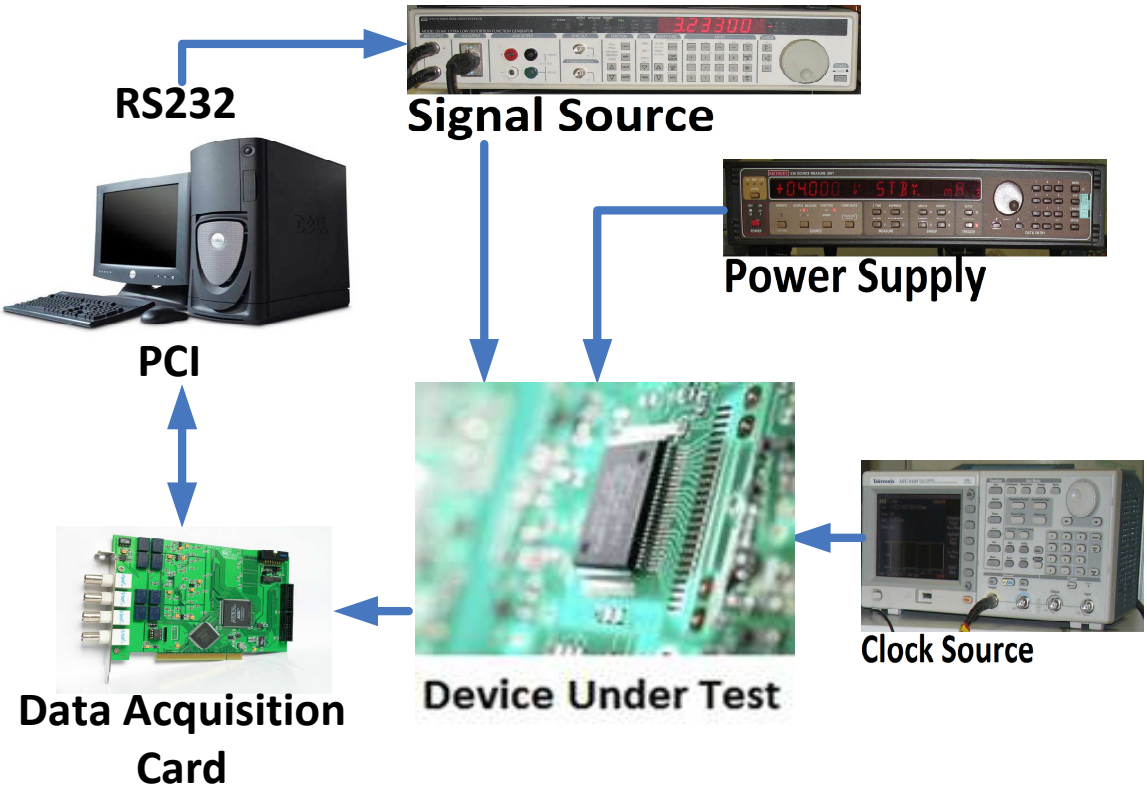


Figure 5: Test Setup Block Diagram

2.1.1 Power Supply

The power supply should have a noise as low as possible so that the estimated calculations (in section 3) of noise can be satisfied. The design of the power supply includes an ultra-low-noise low dropout (LDO) regulator by MAXIM-IC cascaded with several unity gain operational amplifiers to generate lower voltages to power up the chip. The noise on the power supply is targeted to be lower than the quantization noise of ADC.

2.1.2 Data Acquisition

The data acquisition card is being used in order to acquire digitized data for post processing FFT based analysis. This data acquisition card (NI PCI6542 by National Instruments) supports simultaneous sampling of 32 channels with a maximum sampling rate of 100 MHz. IMEC's

modulator chip has four bits of data at the output and the sampling rate is roundabout to 1 mega samples per second.

The data is acquired by a software designed in LabVIEW Signal Express 3.0. This software generates a file in Hierarchical Data Format (HDF) which is being read in MATLAB for further analysis. In order to test the dynamic performance of the modulator chip, data is acquired by applying a signal at the input of the modulator and changing its amplitude from 0 V_{p-p} to full scale. The data is acquired corresponding to each amplitude. Afterwards, the SNR and SNDR are calculated for each different amplitude and then plotted with amplitude to analyze dynamic performance. In order to automate this process, a serial port interface with the function generator (DS360 by Stanford Research System, SRS) is implemented in MATLAB. This software applies a signal with changing amplitude, acquires data corresponding to each amplitude and then generates plots of SNR, SNDR versus amplitude. The dynamic range plot for an off-the-shelf 2nd order $\Delta\Sigma$ modulator (ADS1203) is shown in section 5.2.

2.1.3 Signal Source

High resolution ADCs require very low distortion input signals in order to test full dynamic range. Hence it is compulsory for the equipment to have a higher resolution than the maximum resolution of ADC under test. The total harmonic distortion (THD) and effective number of bits (ENOB) are two important parameters. THD plus noise is the ratio of the RMS value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding dc) and is calculated by the formula given in equation 4.

$$\mathrm{THD + NOISE} = \sqrt{\mathrm{V_{2H} + V_{3H} + \cdots \ldots + V_{NH} + V_{NOISE}}} \Big/ \mathrm{V_{1H}} \qquad (4)$$

This quantity is usually expressed in decibels (dB) or in percentage (%). The quality of the digitized signal can be represented by ENOB of ADC. Based on equation 1, the formula for calculating ENOB is given in equation 5.

$$\mathrm{ENOB} = \left[(\mathrm{SNR} - 1.76) \Big/ 6.02 \right] \qquad (5)$$

As a rule of thumb, the signal delivered by the generator must be 10 dB better than the specification limits of the ADC in order to ensure acceptable test conditions. Hence, it is commonly admitted that the generator resolution should be at least 2 bits higher than the tested ADC resolution [3]. To test IMEC's 16 bits modulator chip, the SRS function generator (DS360) with 18 bits of ENOB (110 dB of SNR) is used. The THD of some function generators is given in Table 2.

2.1.4 Clock Source

The clock source is used as a sampling clock. In order to test high resolution ADCs, the clock source jitter should be as low as possible. There are two types of jitter; deterministic jitter and random jitter. The deterministic jitter is most often caused by the cross coupling from other signals, edges of switching signals, overshoot and ringing. Random jitter is primarily

caused by thermal noise, mostly as a result of electrons bouncing into atoms as they travel through conductors and components. The relationship between analog input frequency, clock jitter and SNR for a Nyquist ADC is given by the equation 6 [4].

$$SNR = 20\log_{10}\left[1/\pi * F_{IN} * T_j\right] \quad (6)$$

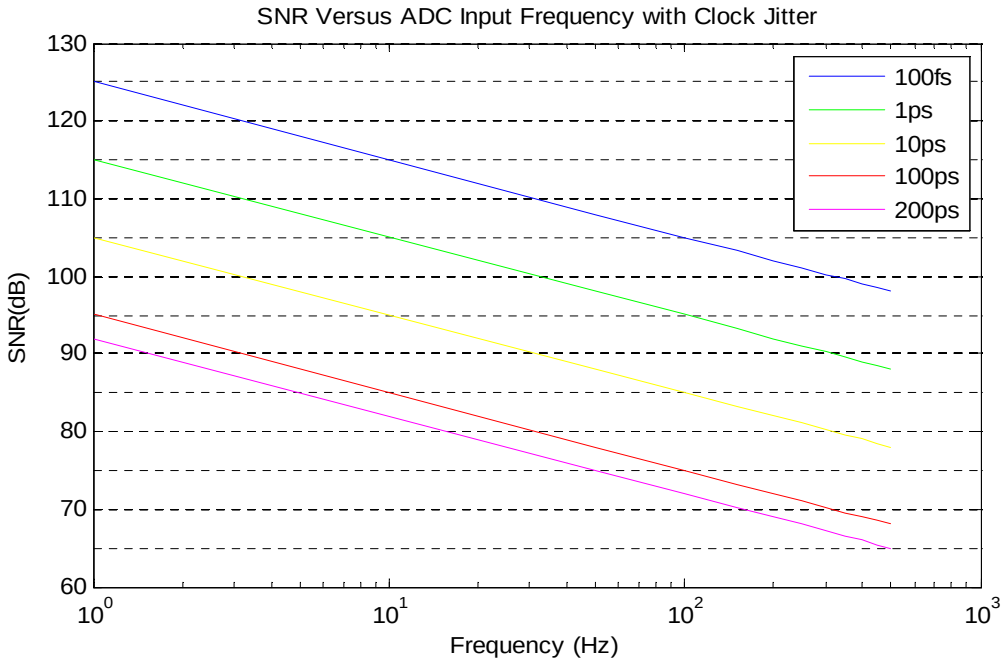


Figure 6: Effect of Jitter of Clock Source on SNR of Nyquist ADC

Where T_j is the jitter time and F_{IN} is the input signal frequency. From Figure 6, it is clear that in order to achieve an SNR of 98 dB from a Nyquist ADC in the range of frequencies shown above; the clock signal jitter should be less than 100 fs.

Figure 7 shows a comparison among Nyquist ADC, continuous time $\Delta\Sigma$ (CT DS) ADC and discrete time $\Delta\Sigma$ (DT DS) ADC. The labels on the plot of Figure 7 show that in order to achieve an ENOB of 16 bits, it is necessary to have a lower value of jitter. To interpret the graph for different values of f_B(input bandwidth), OSR (oversampling ratio) and N (number of bits of ADC), it is useful to consider the relationships given in equations 7, 8 and 9:

$$\sigma_{J\_nyquist} = \frac{1}{\pi * f_B * 2^N} \quad (7)$$

$$\sigma_{J\_DT} = \sqrt{\frac{OSR}{6}}\,\frac{1}{2^N}\,\frac{1}{2*\pi*f_B} \quad (8)$$

$$\sigma_{J\_CT} = \frac{1}{\sqrt{3*OSR}} \cdot \frac{1}{2^N} \cdot \frac{1}{8*f_B} \quad (9)$$

where $\sigma_{J\_nyquist}$, σ_{J_DT}, σ_{J_CT} are the values of jitter for Nyquist ADC, discrete time $\Delta\Sigma$ ADC and continuous time $\Delta\Sigma$ ADC. OSR is the oversampling ratio and f_B is the bandwidth of the signal.

The clock source (clock generator by Tektronix) which was used for testing in the start had an RMS jitter of 200 ps. Because this was not fulfilling the requirement, so another clock source was designed with crystal clock oscillator and its jitter was 1 ps.

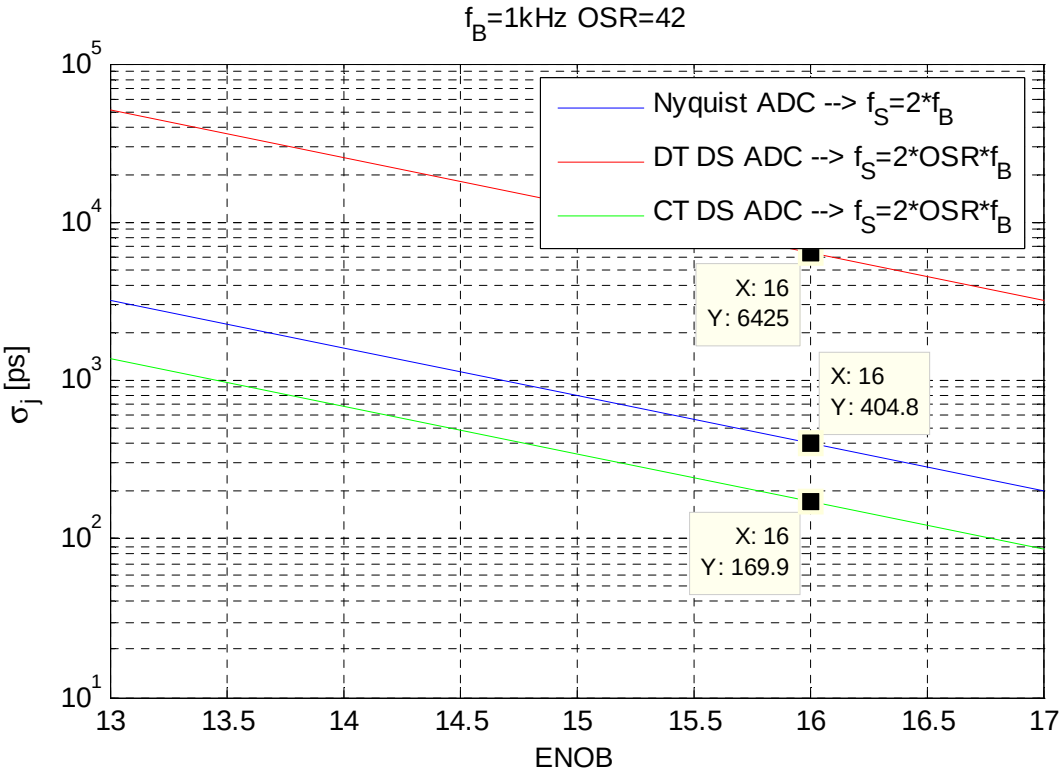


Figure 7: Effect of Jitter of Clock Source on Effective Number of Bits

2.2 Evaluation Results for Different Equipment

Table 2 shows THD of different function generators. The THD plus noise of the audio analyzer by Stanford Research System (SRS) is -112 dB at 22 kHz of bandwidth. This means that this is good enough for testing a 16 bit ADC. The second option is an ultra-low distortion function generator (Model: DS360) by SRS which has a THD of -110 dB in the bandwidth of 5 kHz. The third option is the 2700 series audio analyzer by Audio Precision which has a THD+Noise of -115 dB in 1 kHz and -112 dB in 22 kHz bandwidth.

Company Name	Description	Model	Amplitude	Output Type	THD+Noise	THD	Bandwidth
Stanford Research System	Audio Analyzer	SR1	4 Vrms		-112 dB		22 kHz
Stanford Research System	Function Generator	DS360	1 Vrms	Unbalanced		-110 dB	0.01 Hz to 5 kHz
Stanford Research System	Function Generator	DS360	2 Vrms	Balanced		-110 dB	0.01 Hz to 5 kHz
Audio Precision	Audio Analyzer	2700 Series	2 Vrms		-115 dB		1 kHz
Audio Precision	Audio Analyzer	2700 Series	2 Vrms		-112 dB		22 kHz

Table 2: List of Equipment That Satisfy SNR Requirement

In order to make sure that the function generator has the specified THD performance, the THD of this function generator is obtained using a spectrum analyzer.

The PCB is built up for off-the-shelf 2nd order $\Delta\Sigma$ modulators (ADS1203 and ADS1201 by Texas Instrument, details of this PCB is given in section 5). This PCB also contains a crystal clock oscillator with a clock divider chip on it. The crystal clock oscillator is a 27 MHz (ASFL1) and the clock divider chip is AD9514 and it has available division factors of 1, 2, 3.....32. This clock source is also used to test the IMEC modulator chip. The jitter of this clock source is less than 1 ps (RMS) as written in the datasheet.

3 Evaluation of Components that Satisfy Low Noise Requirement

3.1 Requirement on the Noise from the Components

This section explains requirements on the maximum noise from the components and design of power supplies. It is targeted that the total noise on the power supply should be below the quantization error of the ADC. This noise includes all types of noise sources. The formulas for calculations are described in equations 10 and 11.

$$\mathrm{LSB_{VOLTAGE}} = {}^{F_S}/_{2^N} \quad (10)$$

where

F_S = full scale Input Amplitude

N = number of bits of ADC

The RMS value of the quantization error is given by equation 11.

$$Q_{error} = {}^{\mathrm{LSB_{VOLTAGE}}}\Big/_{\sqrt{12}} \quad (11)$$

IMEC modulator's quantization error is calculated in table 3.

Full Scale Amplitude (V)	1.8
Number of Bits of ADC	16
LSB Value (µV)	27.46
Quantization Error (µVrms)	7.92

Table 3: Quantization Error of IMEC Modulator Chip

This 2nd order $\Delta\Sigma$ modulator has different power supplies which are listed below.

(1) Two for digital to analog converters (DACs) in the feedback path.
(2) Two for reference voltages of these digital to analog converters (DACs).
(3) Two for analog and digital cores of the chip.

3.2 Design of Power Supplies

It is described in section 4 that this 2nd order modulator chip consists of two operational amplifiers and two DACs in the feedback path. Each operational amplifier has a common mode and each DAC has a reference. For the case of op-amps, the noise on the main supply and common mode gets attenuated due to power supply rejection ratio (PSRR) of op-amps

but references of DACs are very sensitive to noise. Thus it is taken care in the placement of decoupling capacitors that these are very close to the reference pins of DACs. In order to power up this chip, it is decided to use a low noise op-amp with a filter at the output. The schematic of this voltage source is shown in Figure 8. The voltage at the output can be tuned with the variable resistor at the input.

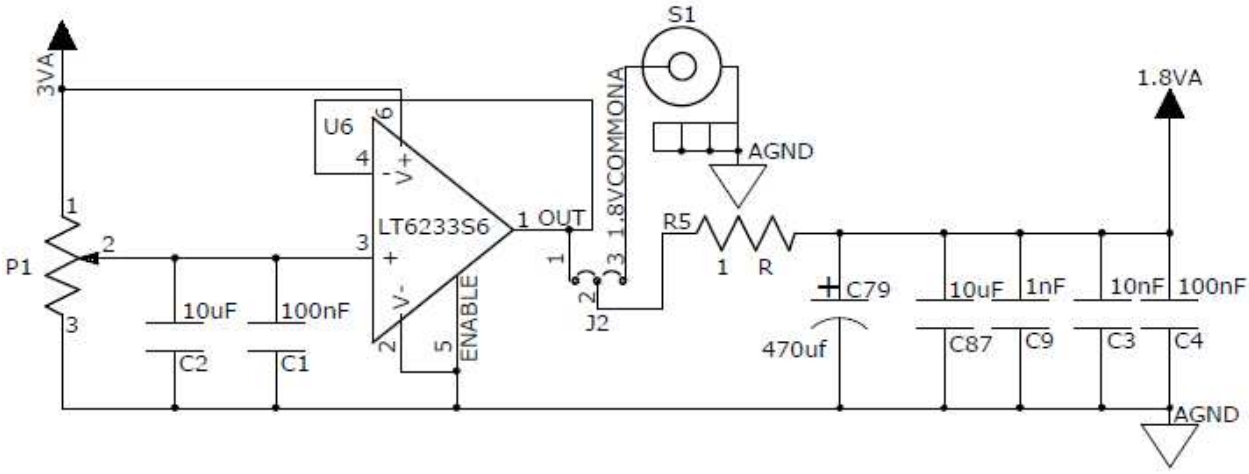


Figure 8: Schematic of Voltage Tunable Power Source

In order to see the contribution of different noises in the op-amp, a noise model is shown in Figure 9. The noise sources outside the op-amp are current noises of the bias currents and thermal noise of the resistor, which are added together in the form of root mean square to give the total equivalent input voltage noise RMS. Equation 12 describes this [5].

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 * R^2 + 4 * k * T * R} \quad (12)$$

where E_{ni} is the total equivalent input voltage noise of the circuit,

e_{ni} is the equivalent input voltage noise density of op-amp, and
I_{ni}*R is the voltage noise generated by the current noise I_{n-} and I_{n+}.
4*k*T*R expresses the thermal noise generated by the external resistor in the circuit where k = 1.38 x 10-23 Joules/Kelvin; T = 300 Kelvin (27^{o}C)

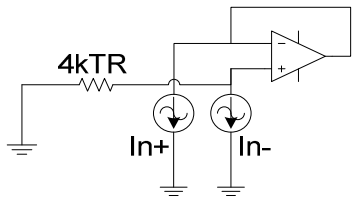


Figure 9: Operational Amplifier Noise Model

The total RMS output noise (E_{no}) of this op-amp with gain equal to G in the bandwidth between f_1 and f_2 is given by equation 13 [5].

$$E_{no} = G * \sqrt[2]{\int_{f_1}^{f_2} E_{ni}^2 \, df} \quad (13)$$

The values of I_{ni} and e_{ni} can be calculated by the noise of op-amp (LT6233) given in the datasheet and a snapshot of it is shown in Figure 10.

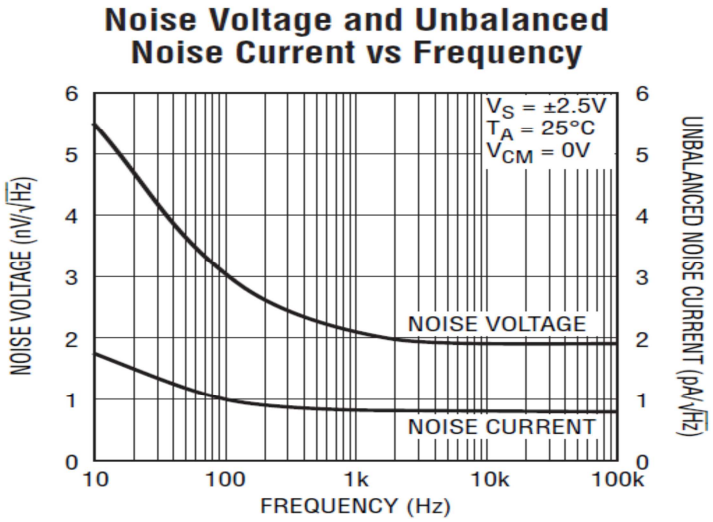


Figure 10: Voltage and Current Noise Density

The area under the curve is calculated by a MATLAB routine which takes values of voltage and current noises on different values of frequencies and with these points, the area under the trapezoidal segments is calculated up to the bandwidth of 100 kHz. Table 4 shows values obtained from the calculations.

LT6233							
Voltage Noise Density, e_{ni} (V/sqrt(Hz))	2.20E-07	2.20E-07	5.50E-09	3.00E-09	2.10E-09	1.90E-09	1.90E-09
Current Noise Density, I_{ni} (A/sqrt(Hz))	2.20E-10	2.20E-10	1.80E-12	1.00E-12	8.00E-13	8.00E-13	8.00E-13
R (Ω)	2.00E+03	2.00E+03	2.00E+03	2.00E+03	2.00E+03	2.00E+03	2.00E+03
e_{ni}^2	4.84E-14	4.84E-14	3.03E-17	9.00E-18	4.41E-18	3.61E-18	3.61E-18
$I_{ni}^2*R^2$	1.94E-13	1.94E-13	1.30E-17	4.00E-18	2.56E-18	2.56E-18	2.56E-18
4kTR	3.31E-17	3.31E-17	3.31E-17	3.31E-17	3.31E-17	3.31E-17	3.31E-17
Eni^2	2.42E-13	2.42E-13	7.63E-17	4.61E-17	4.01E-17	3.93E-17	3.93E-17
Frequency Range (Hz)	0.1	8	10	1.00E+02	1.00E+03	1.00E+04	1.00E+05
Area under Curve (V^2)	4.40E-12						
Voltage Noise (RMS Voltage)	2.10E-06						

Table 4: RMS Noise of Op-Amp (LT6233) in the Bandwidth of 100 kHz

All these calculations are done by considering a noiseless power supply source for the op-amp. Since the quantization error of the modulator in our case is about 8 μV_{rms}, which is a very small value, it is decided to place a filter at the output of op-amp and reduce this noise as much as possible.

3.2.1 Low Pass RC Filter Design and Implementation

This section details the design of the RC low-pass filter and its implementation. First, the theoretical implementation of this filter is evaluated in MATLAB by looking at the reduction on the values of noise and then its practical implementation is discussed. The diagram of the RC filter is shown in Figure 11.

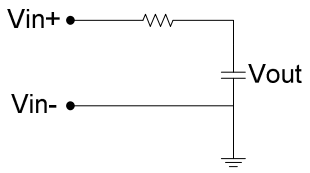


Figure 11: RC Low Pass Filter

The output voltage of this filter is given by equation 14.

$$V_{out} = G_c V_{in} e^{j\emptyset_c} \quad (14)$$

The magnitude of the gain across the two components is given in equation 15,

$$G_c = |H_c(j\omega)| = \left|\frac{V_{out}(j\omega)}{V_{in}(j\omega)}\right| = \frac{1}{\sqrt{1+(\omega RC)^2}} \quad (15)$$

and $\emptyset_c$ is the phase angle.

$$\emptyset_c = \angle H_c(j\omega) = \tan^{-1}(-\omega RC) \quad (16)$$

The attenuation factor for the voltage is calculated with this relation and is implemented in the MATLAB routine which calculates an implementable value of cut-off frequency of the RC filter. A plot showing voltage RMS values for this wideband noise with different cut-off frequencies is shown in Figure 12. It is clear that decreasing the cut-off frequency of this filter more, does not pay off much in terms of reduction in the noise of supply. The cut-off frequency can only be decreased with an increase in the value of the capacitor; increasing the resistance introduces more thermal noise. The RMS value of noise with a capacitor of 470 µF and a resistance of 1 Ohm is 1.197 μV_{rms}. Now if we increase the value of capacitor to 3300 µF, which means a cut off frequency of 48 Hz, the decrease in the RMS noise is not so much and it is also visible in Figure 12. Moreover, the value of capacitor is too large which means a bigger size of capacitor will be needed. Because the IMEC modulator chip requires many supplies and each supply requires a filter so a bigger value of capacitor will result into a larger area of test PCB and very less decrease in noise. Thus it is decided to not reduce the cut-off frequency anymore.

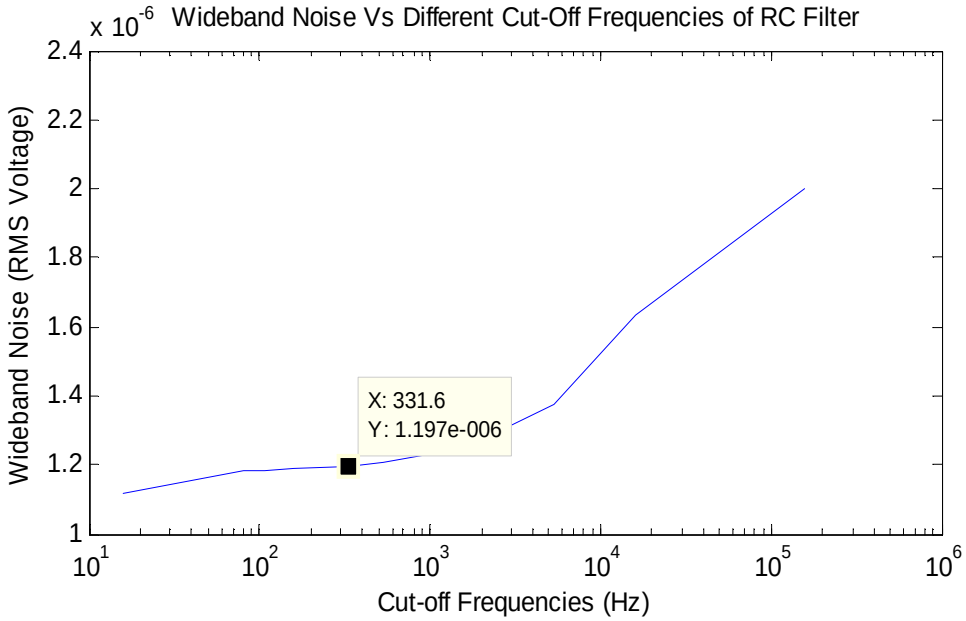


Figure 12: RMS Noise Voltage with Different Cut-Off Frequencies of RC Filter

The calculated values are valid only for an ideal capacitor. The non-ideal behavior of the capacitor is modeled as resistance, capacitance and inductance as shown in Figure 13.

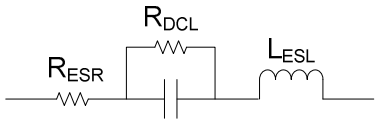


Figure 13: Non-Ideal Capacitor Model

R_{ESR} = equivalent series resistance
R_{DCL} = leakage current
C = capacitance
L_{ESL} = equivalent series inductance ($L = 1/ [(2*\pi*f_o)^2 \times C]$), where f_o is the resonance frequency

So, behavior of the capacitor changes with the frequencies and it becomes open at higher frequencies due to increase in the impedance of the capacitor [7].

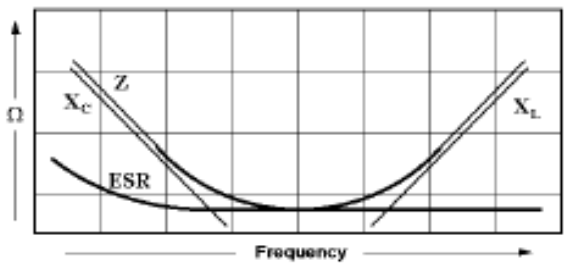


Figure 14: Non-Ideal Behavior of Capacitor [7]

Factors affecting the impedance value are:

1. Capacitive Reactance (Capacitance) - Low
   Frequency Range: $X_C = 1/(2*\pi*f_c)$, where f_c is the frequency in Hz and represent frequencies below the resonance frequency (f_o).
2. ESR (Resistance) - Middle Frequency Range
3. Inductive Reactance (Inductance) – High.
   Frequency Range: $X_L = 2*\pi*f_L$, where f_L is the frequency in Hz and represent frequencies above the resonance frequency (f_o).

The behavior of capacitive reactance (X_C), inductive reactance (X_L) and ESR is shown in Figure 14. So ESR and impedance of the capacitor limits the attenuation factor of filter and after the resonance frequency of capacitor the attenuation factor starts decreasing rapidly. The formula for maximum attenuation is given in equation 17.

$$\text{Attenuation (dB)} = 20\text{Log}_{10}\left[{\text{ESR}}/{(\text{R} + \text{ESR})}\right] \quad (17)$$

The attenuation is low for a lower frequency (which is required for low pass filter) while it starts increasing with an increase in frequency up to the self-resonance frequency of capacitor. After this point, attenuation again starts decreasing but we want more attenuation at higher frequencies and this is the reason due to which capacitors with different resonance frequencies (resonance frequencies are different for different values of capacitors) are used.

In this way the low pass filter is constructed and different values of capacitors are used which are shown in Figure 8 (470 µF, 10 µF, 100 nF, 10 nF and 1nF). The cut-off frequency of RC filter with these values is 331.57 Hz and the resulting RMS voltage noise is 1.19 μV_{rms} which is also shown in Figure 12.

3.3 Main Power Supply

The main power supply which is used to power up the operational amplifiers is chosen as an ultra-low-noise LDO by MAXIM-IC. This LDO combines low-noise components with filtering to achieve an output noise performance of $\frac{6\text{nv}}{\sqrt{\text{HZ}}}$ at 1 kHz [6]. The schematic of the proposed circuit is shown in Figure 15. The output voltage can be adjusted with tuning of resistances at the output and its formula is given in equation 18.

$$\text{R3} = \text{R2}([\frac{\text{V}_{\text{out}}}{2.048\text{V}}] - 1) \quad (18)$$

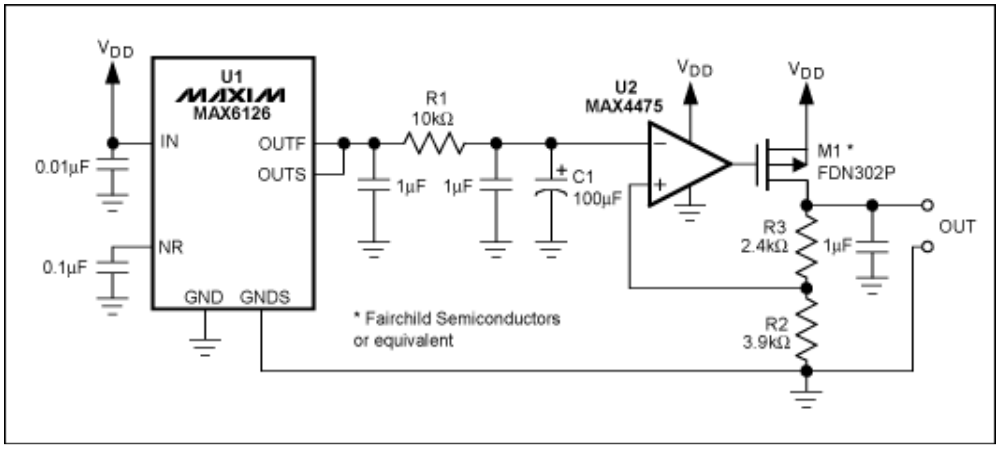


Figure 15: Ultra-Low-Noise LDO

The plot of voltage noise density at the output of this LDO is shown in Figure 16.

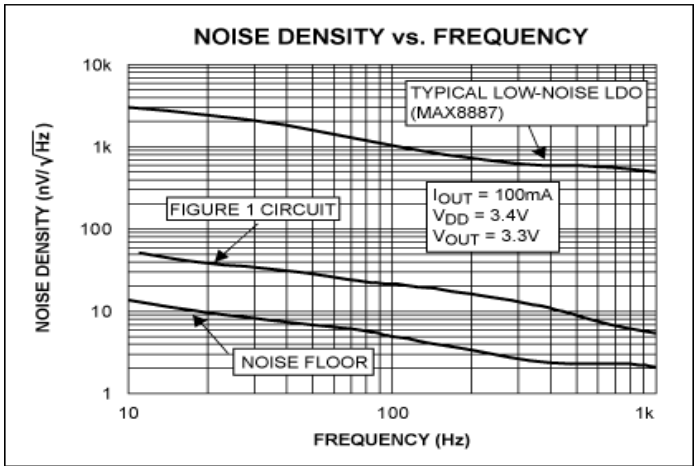


Figure 16: Noise Density at the Output of LDO

The RMS voltage noise of this LDO is calculated by integration and it is 1.78 μV_{rms}. So the effective and implementable value of cut-off frequency is calculated with the MATLAB routine which is 167.5 Hz and this is also shown in Figure 17. A larger capacitance (940 µF) is used to implement this filter. The attenuated RMS value of noise is 0.68 μV_{rms}.

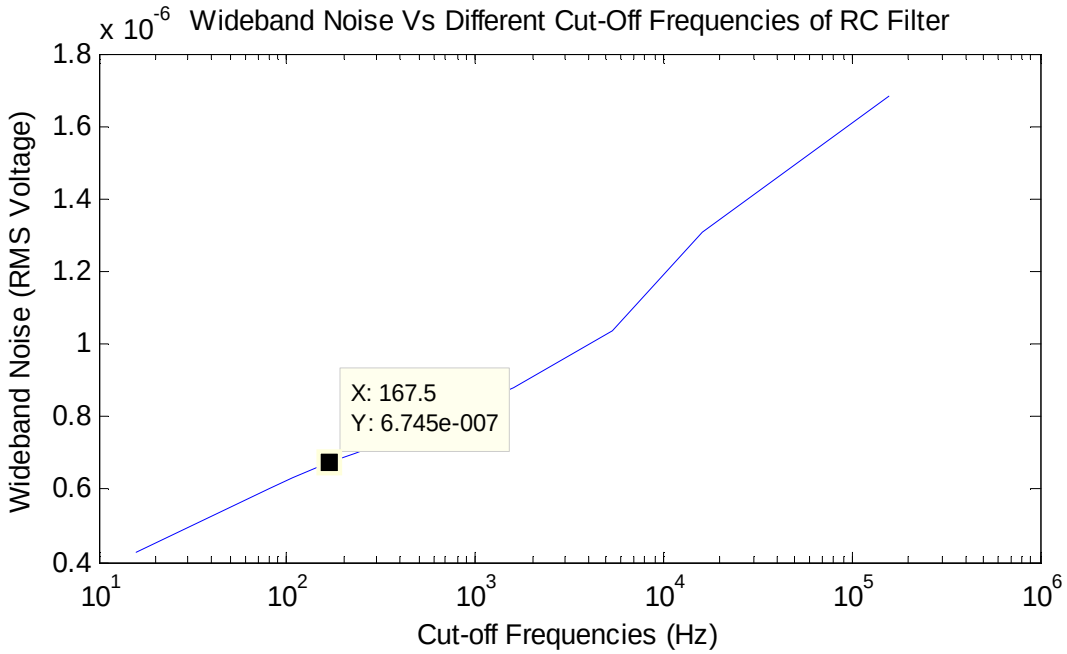


Figure 17: RMS Noise Voltage with Different Cut-Off Frequencies of RC Filter

So the total RMS noise of this LDO and op-amp is calculated in the following way.

$$Noise_{\mathrm{RMS}} = \sqrt{(0.674\mathrm{E}-6)^2 + (1.197\mathrm{E}-6)^2} = 1.37\ \mu\mathrm{Vrms}$$

The theoretical calculated value of noise is 1.37 μV_{rms} and it is less than quantization error (8 μV_{rms}) of modulator.

4 PCB for IMEC Modulator

The purpose of this PCB is to provide different test setups which are required by the IMEC modulator chip for its testing. It is designed using PADS PCB tools (by Mentor Graphics). Its snapshot is shown in Figure 18.

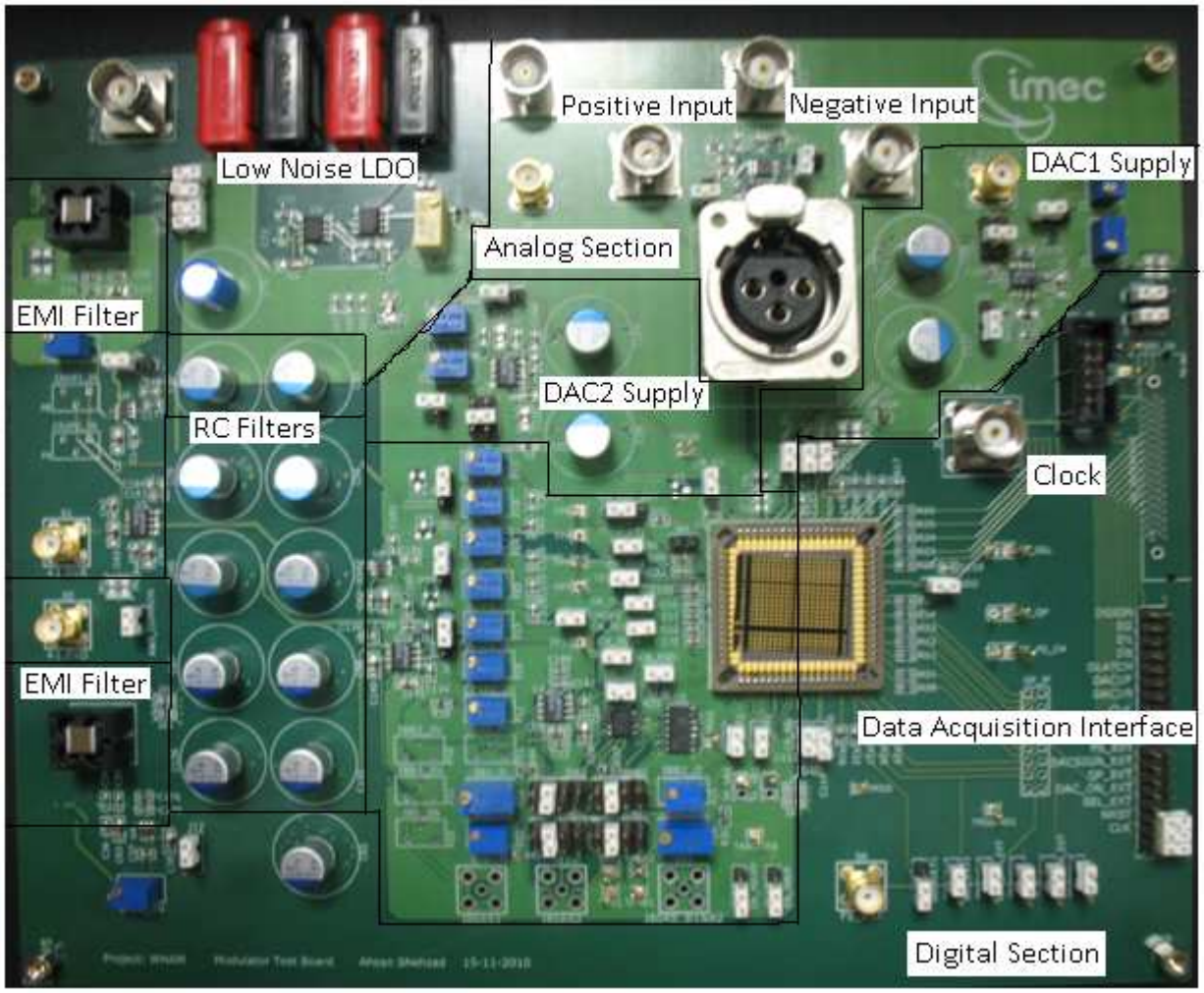


Figure 18: IMEC Modulator Test PCB

4.1 Architecture of PCB (IMEC's Modulator)

The PCB has two partitions of analog and digital domains. It has several options of connections which include shorting analog and digital domains together and powering up the chip with direct supply and bypassing on board op-amp's supplies. This modulator chip has a digital interface which is used to provide a control mechanism in digital part of the chip. This control includes chopping frequency selection, control signals for DACs and change of bandwidths of operational amplifiers. The bandwidths can be changed with a change of capacitance in their feedback paths. The inputs of modulator can be single ended

or unbalanced differential with BNC connectors or balanced differential with XLR connector. This PCB has the option of soldering one of the two differential converter chips which are AD8138 (Analog Devices) and LT6350 (Linear Technology). This low distortion differential converter converts analogue single ended signal to a differential signal. The input bandwidth modes of modulator are 256 Hz and 1 kHz. Clock signal can be applied externally with a function generator and through a data acquisition board.

4.2 Digital Interface PCB

The digital interface is similar to SPI interface and a µ-controller (MSP430F149) is used to program this interface which provides the functionality for different controls. This microcontroller is placed on a separate PCB in order to isolate the noise generated by it and is connectable with the modulator chip designed by IMEC with a ribbon cable. Its snapshot is shown in Figure 19.

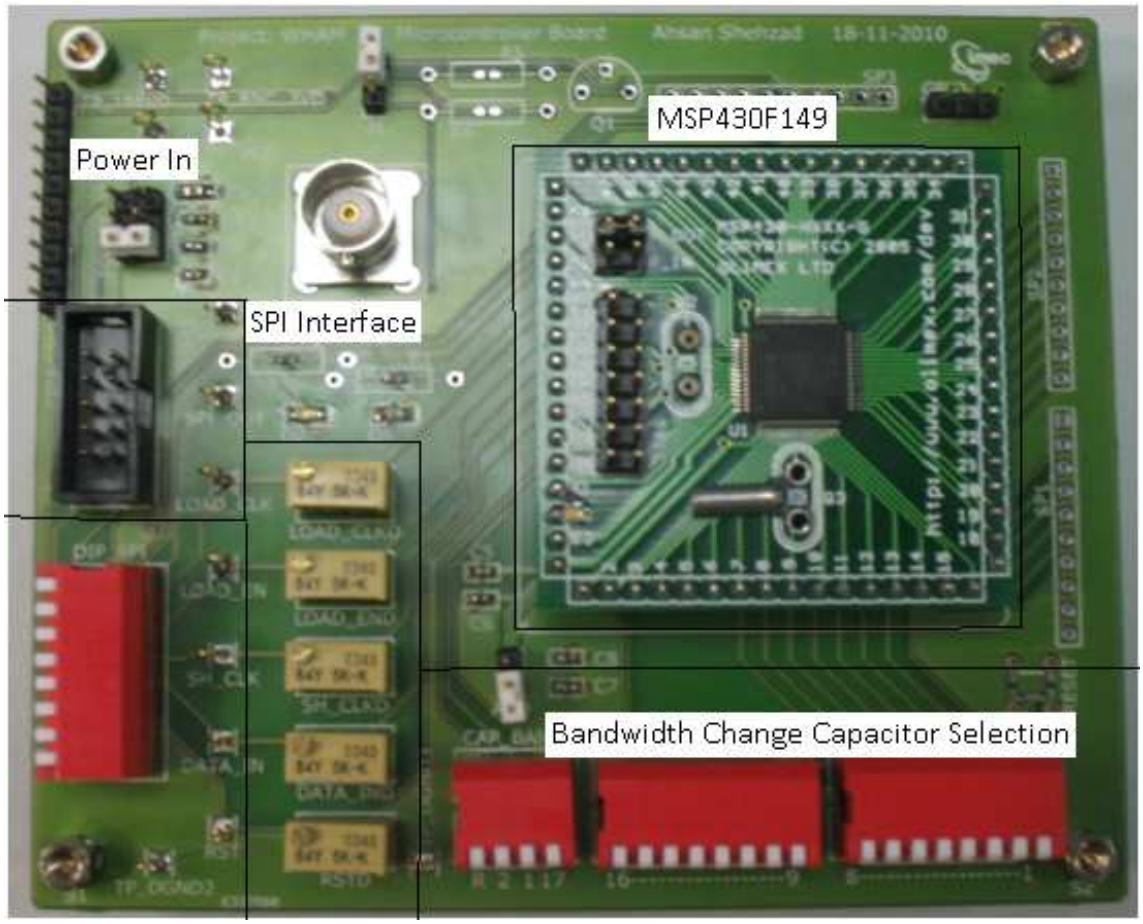


Figure 19: µ-Controller Interface PCB

4.3 Signal Integrity Precautions

Electro-magnetic Interference (EMI) filters are used in the power supply in order to remove electro-magnetic interference. The characteristic impedance of all tracks is matched to 50 Ohm. The PCB has two different analog and digital ground splits which are connectable on

several places. These places include underneath the modulator chip, around the modulator chip and near to power sources etc. These options are provided in order to evaluate the performance with different lengths of return current paths. It is made sure that the return current path is as short as possible and is wide enough. It is also ensured that no analog signal lies in the digital domain and no digital signal lies in the analog domain because these can introduce digital noise coupling in the analog domain. Decoupling capacitors are placed very close to modulator pins.

4.4 Measured Values of Noise on the Power Supplies

All the calculations of noise that are done theoretically were actually done by considering noise free supply at the input. But the IMEC modulator was tested with supplies which have a larger figure of noise at the output. Figure 20 shows the spectrum of noise at the input of the main ultra-low-noise LDO. Considering a bandwidth of 1 kHz, it is observed that the total RMS noise of input supply is 62 μV_{rms} (neglecting "0" Hz). The FFT of supply is taken from spectrum analyzer (SR785 by Stanford Research System). Blank spaces in power spectral density plot are due to removal of 50 Hz and its harmonics.

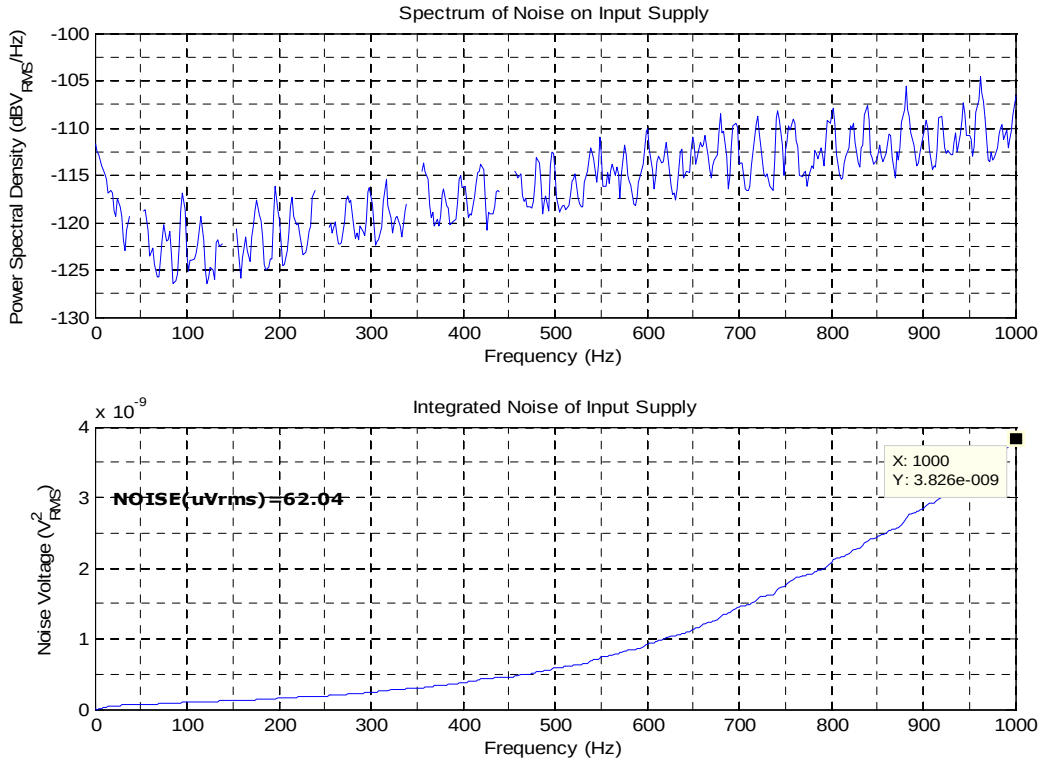


Figure 20: Spectrum and Integrated Noise of Input Supply

Similarly, the spectrum at the output of the ultra-low-noise LDO is shown in Figure 21. Considering a bandwidth of 1 kHz, it is observed that the total RMS noise of input supply is 4.35 μV_{rms} (neglecting zero Hz). It is clear that a lot of noise is being attenuated with this ultra-low-noise LDO but is still larger than theoretically estimated one.

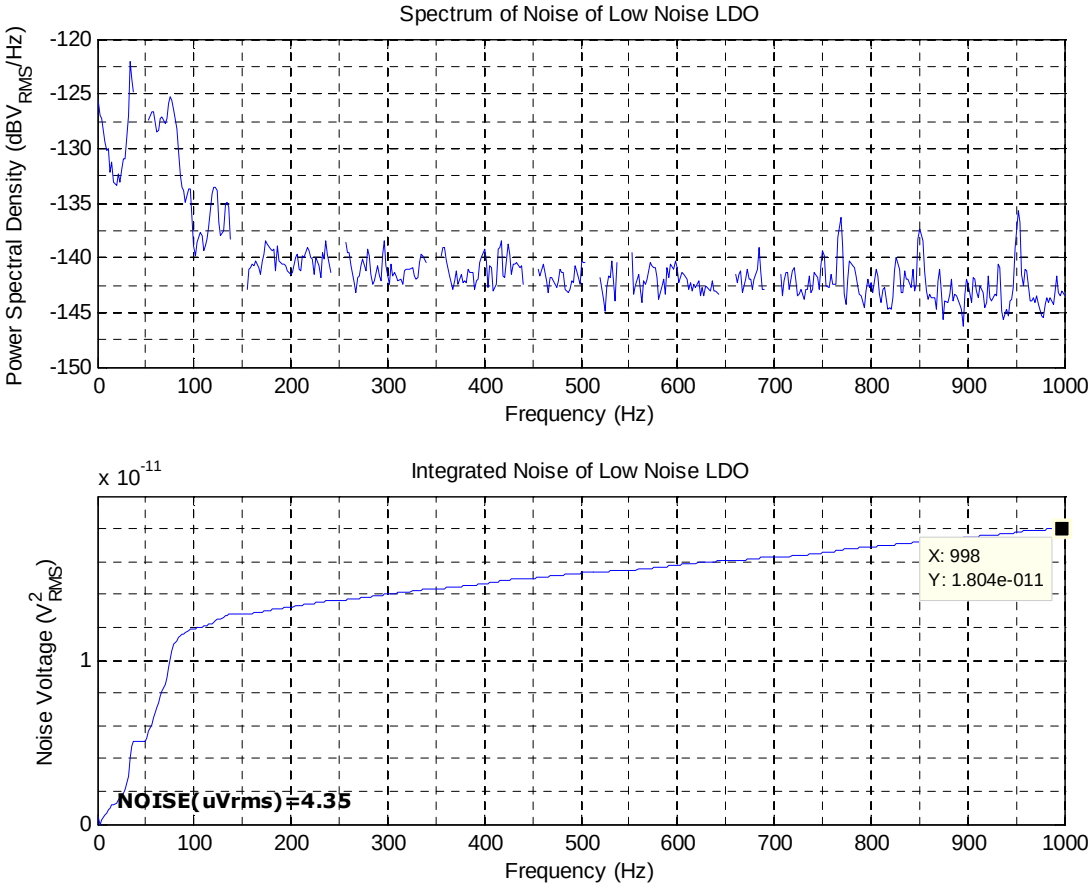


Figure 21: Spectrum of Output of Ultra-Low-Noise LDO

The spectrum at the output of the analog supply and digital supply of the op-amp (LT6233) is shown in Figure 22 and Figure 23 respectively. The RMS value of noise is 4.53 μV_{rms} and 5.12 μV_{rms} respectively.

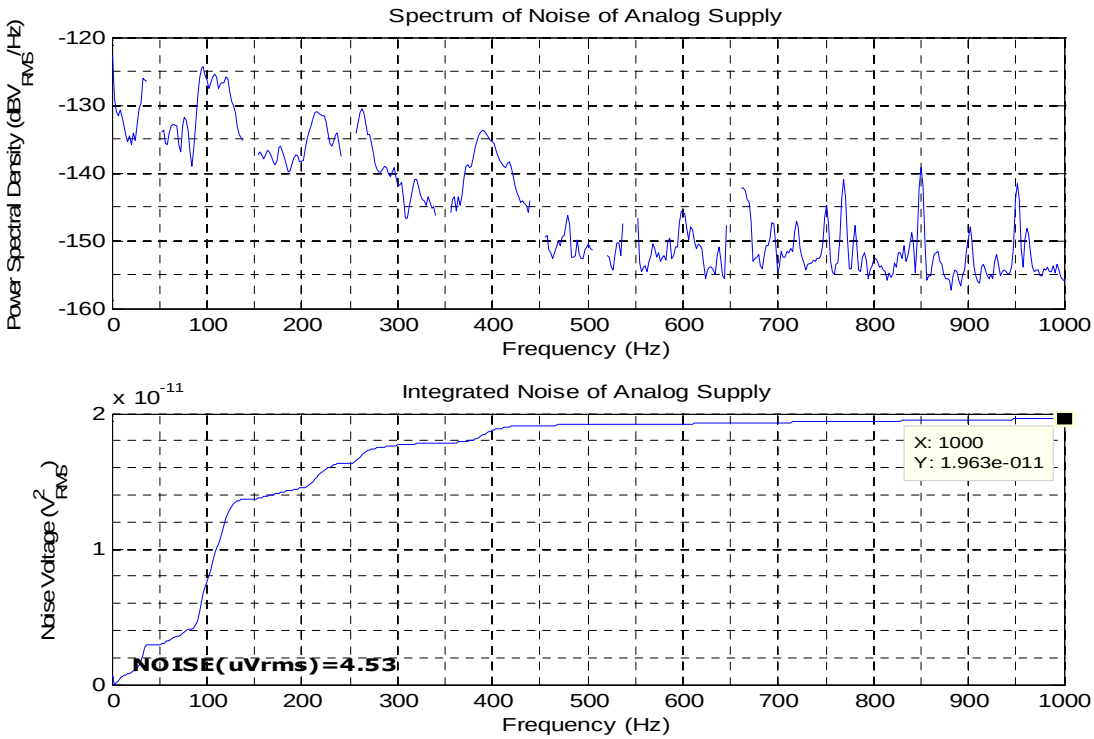


Figure 22: Spectrum of Analog Supply by LT6233

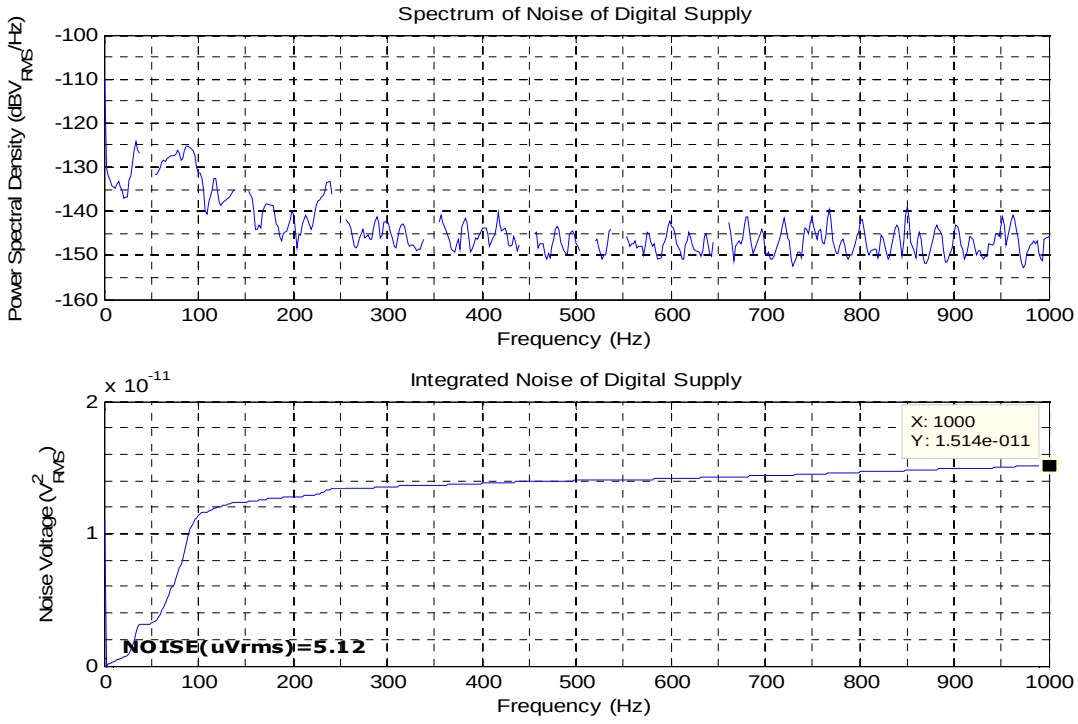


Figure 23: Spectrum of Digital Supply by LT6233

5 PCB for Off-The-Shelf Modulators

The measured value of ENOB from the IMEC modulator was 14 bits while the expected ENOB was 16 bits. Now there were two possibilities of noise sources in the reduction of ENOB. Either the generated noise from the components is causing this reduction or the noise floor of the chip itself is responsible for that. Because the observed values of noise on hardware setup were very large and there was a possibility that these values are actually causing reduction in ENOB, it is decided to check ENOB of an off-the-shelf modulator with the same electronics design and layout whose quantization error value is equal to the IMEC modulator's quantization error (≈ 8 μV_{rms}). Thus another PCB is designed on which two different types of $\Delta\Sigma$ modulators are placed. One of them is ADS1203 whose quantization error is 2.2 μV_{RMS} which is even less than 8 μV_{RMS}. This PCB has the same power supply architecture as the one for IMEC modulator. A snapshot of this PCB is shown in Figure 24.

5.1 Architecture of PCB (Off-The-Shelf Modulators)

This PCB has the option of placing two 2^{nd} order $\Delta\Sigma$ modulators named ADS1203, ADS1201 and crystal clock oscillator (27 MHz, ASFL1) with a clock divider chip (AD9514). It also has a data acquisition interface.

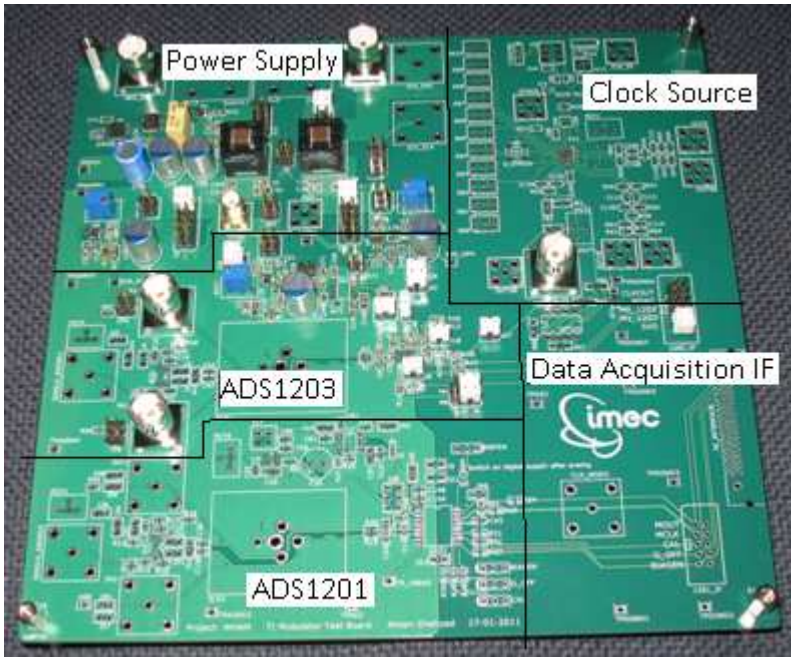


Figure 24: ADS1203, ADS1201 and Clock Source PCB

ADS1203 has single bit output and the datasheet states that an effective resolution of 14 bits (or SNR of 85 dB) can be maintained with a digital filter (decimation filter) bandwidth of 40 kHz at a modulator sampling rate of 10 MHz. It is also stated that a maximum resolution of 16 bits (or SNR of 98 dB) can be achieved in a lower bandwidth or higher oversampling ratio. The full scale input of ADS1203 is 500 mV_{P-P} and hence the LSB value is 7.6 µV and the quantization error is 2.2 μV_{RMS}.

This modulator is tested with the same reference source as was used for the IMEC modulator so that ENOB of the two modulators with the same noise can be compared.

5.2 Spectrum of Signal Digitized by ADS1203

The signal digitized by ADS1203 with 0.00 V_{P-P} and 0.50 V_{P-P} inputs is shown in Figure 25 and Figure 26 respectively. The noise floor with 0 V_{P-P} shown in Figure 25 represents that the maximum amount of SNR that can be achieved is 77.59 dB which is 7 dB less than the specified SNR. This reduction is mainly due to injection of 50 Hz noise from the equipment which is being used as a test signal source. Figure 28 shows the spectrum with acquisition done by shorting inputs with the ground of the PCB in order to observe the effect of removal of 50 Hz. The plot of integrated noise is also shown with values at different bandwidths of 2.6 kHz (OSR = 4k), 10 kHz (OSR = 1k) and 40.1 kHz (OSR = 256). So if a comparison is made among the values of SNR in a specified bandwidth of ADS1203, it can be observed that these values are very close to the specified values and an SNR of 94.68 dB (ENOB equal to 15.43 which was the target) in a bandwidth of 2.6 kHz can be obtained.

SNR and SNDR versus input amplitude plot is shown in Figure 29. This is also called dynamic range of ADC. The dynamic range specifies the range of amplitude which ADC can resolve. It is an important property in many applications where signal strength varies dramatically. If signal is too large, it over ranges the ADC inputs and if it is too small, it gets lost in the converter quantization noise [12].

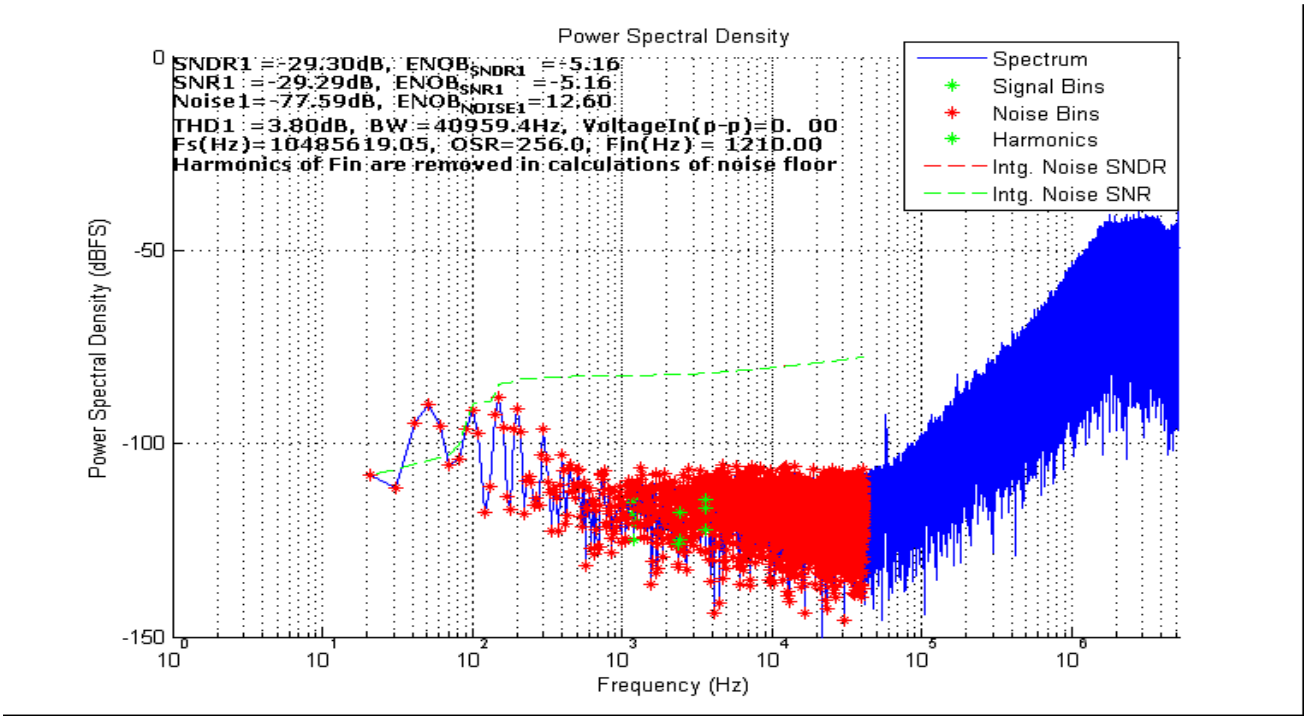


Figure 25: Spectrum with 0.0 VP-P Input

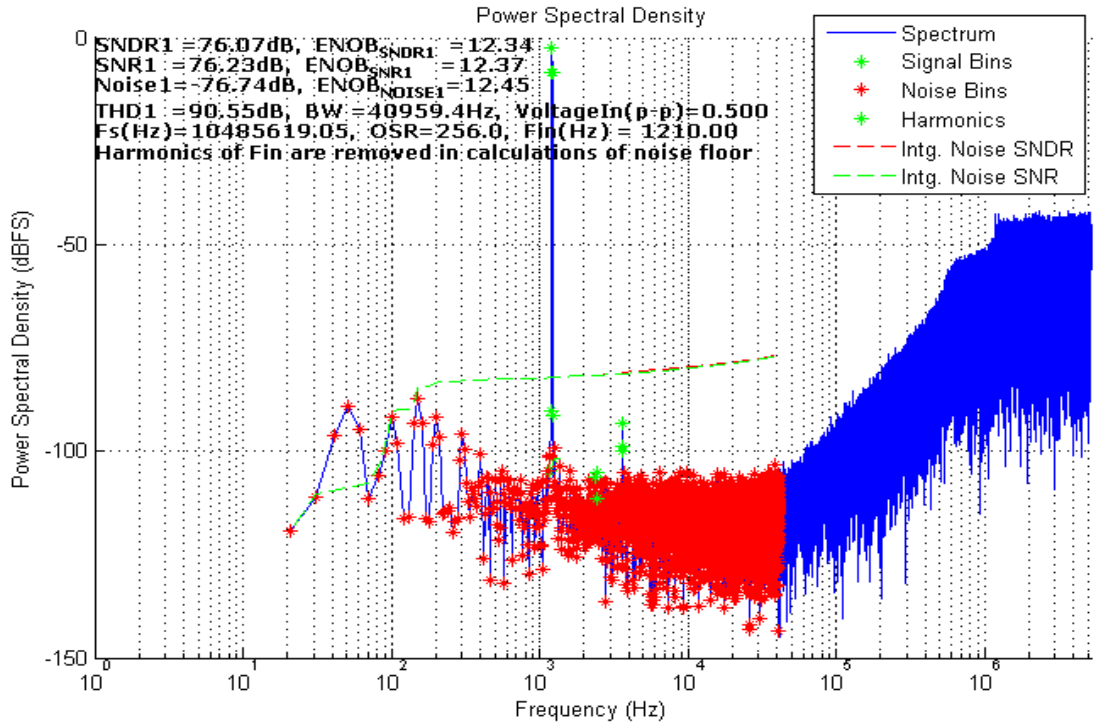


Figure 26: Spectrum with 0.5 VP-P Input

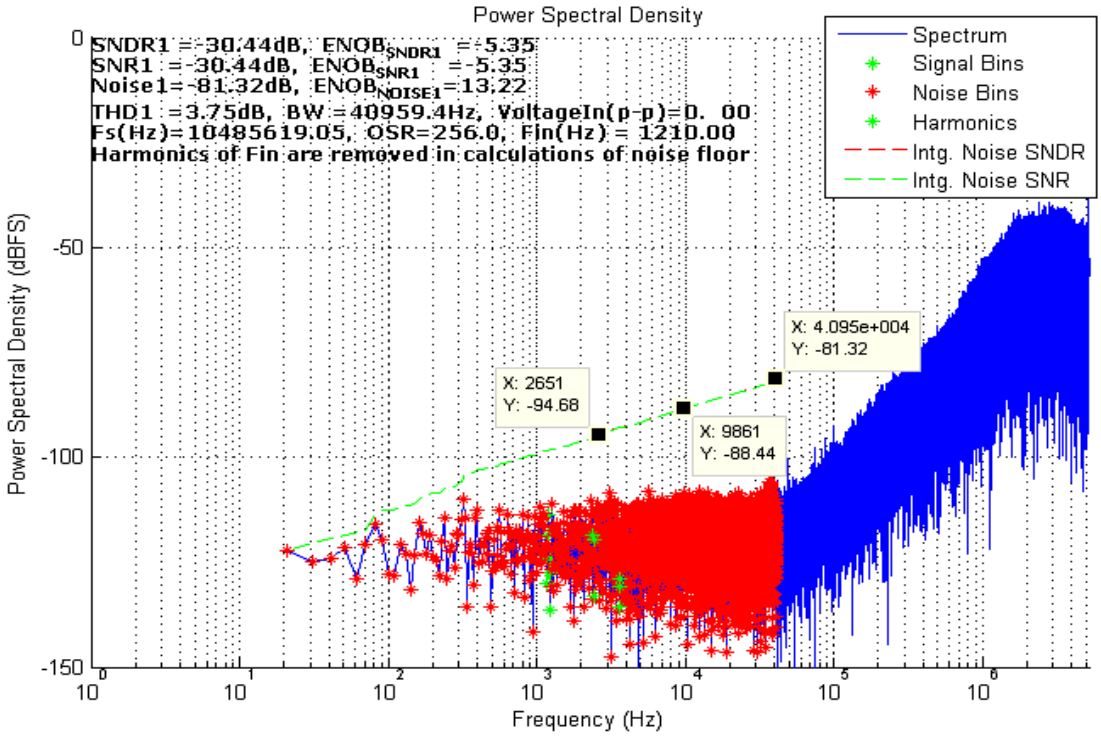


Figure 27: Spectrum with Inputs Shorted to Ground

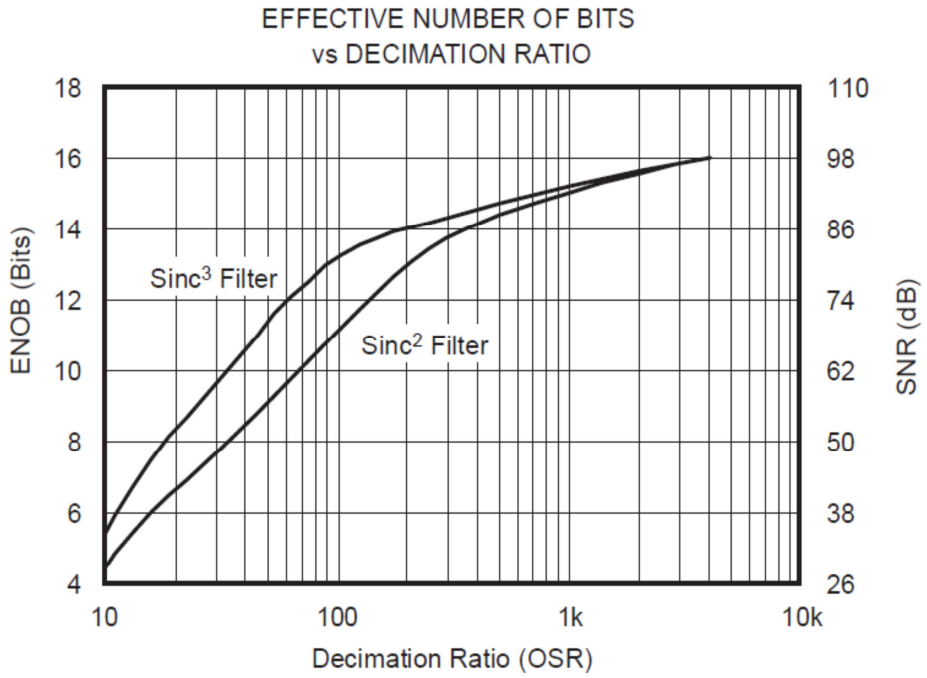


Figure 28: ENOB versus OSR for ADS1203

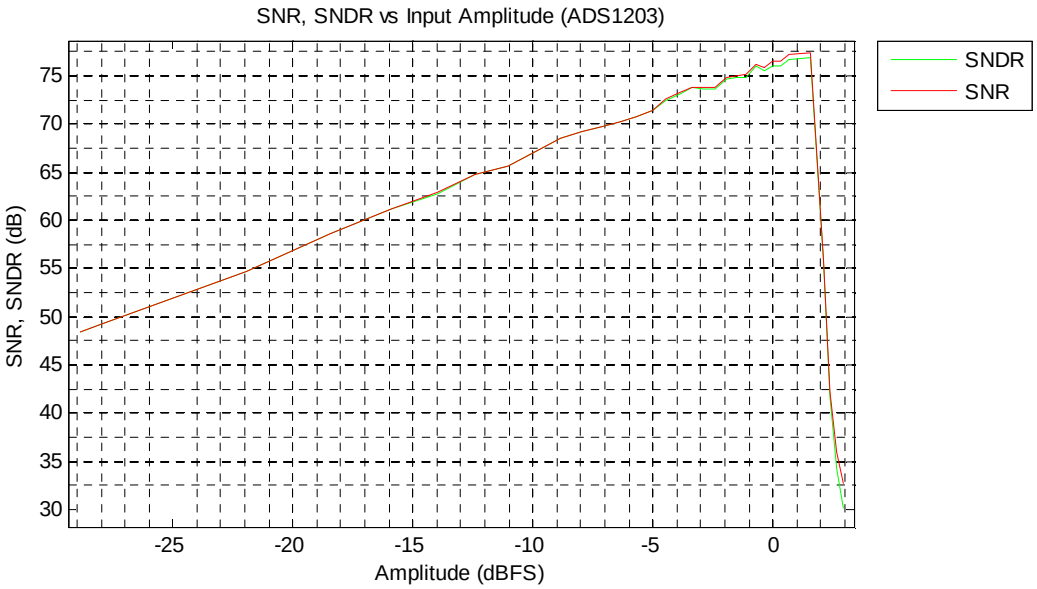


Figure 29: SNR, SNDR versus Input Amplitude (ADS1203)

6 Conclusion and Future Enhancements

A software and hardware testing platform has been designed for a 16 bit 2^{nd} order $\Delta\Sigma$ modulator. In order to test higher ADC resolution, the platform should be targeted for lower values of noise because the quantization error of the ADC will also be smaller. The noise of 50 Hz and its harmonics should be removed in the hardware setup. This can be done by implementing proper grounding of equipment in the lab. The EMI effects should also be removed completely. The hardware setup can be shielded to remove EMI effects. In order to achieve a resolution greater than 16 bits, it is not possible to use the existing signal source. Hence, there is a need to develop a signal source with SNR greater than 110 dB. Some companies provide high resolution DACs and this option can be investigated to design a signal source with SNR greater than 110 dB.

7 References

[1] Application Note by Analog Devices, coherent sampling versus window sampling, March 2002, http://www.maxim-ic.com/app-notes/index.mvp/id/1040.

[2] Art Kay, Analysis and Measurement of Intrinsic Noise in Op Amp Circuits, May 2011, http://www.en-genius.net/site/zones/audiovideoZONE/technical_notes/avt_022508

[3] Vincent Kerzerho, Philippe Cauvet, Serge Bernard, Florence Azaïs, M. Renovell, Mariane Comte, Omar Chakib, "ADC Production Test Technique Using Low-Resolution Arbitrary Waveform Generator", VLSI Design, February 2008.

[4] Bill Odom, "Understand Analog/Digital Converter Clock Jitter and Why You Should Care", December 2007, http://www.eetimes.com/design/analog-design/4010006/Understand-analog-digital-converter-clock-jitter-and-why-you-should-care

[5] Application Note by INTERSIL, "Operational Amplifier Noise Prediction (All Op Amps)" November 1996, http://www.intersil.com/data/an/an519.pdf

[6] Application Note by MAXIM-IC, "Ultra-Low-Noise LDO Achieves $6nV/\sqrt{Hz}$ Noise Performance", May 2011, http://www.maxim-ic.com/app-notes/index.mvp/id/3657

[7] Application Note by United Chemi-Con, "Characteristics of Aluminum Electrolytic Capacitors", May 2011, http://chemi-con.com/u7002/characteristics_ms.php

[8] "What is Spurious-Free Dynamic Range?", October 2010, http://digital.ni.com/public.nsf/allkb/7C77898F35A951E086256BF100686FED

[9] David Jarman, Application Note by INTERSIL, "A Brief Introduction to Sigma Delta Conversion", May 1995, http://www.intersil.com/data/an/an9504.pdf

[10] Power Supply Rejection Ratio, Wikipedia, May 2011, http://en.wikipedia.org/wiki/Power_supply_rejection_ratio

[11] Richard Schreier and Gabor C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press, 2004.

[12] Application Note by MAXIM-IC, "ADC and DAC Glossary", 10th May, 2011, http://www.maxim-ic.com/app-notes/index.mvp/id/641

[13] Richard Lyons, Randy Yates, "Reducing ADC Quantization Noise", June 2005, http://mwrf.com/Articles/Index.cfm?Ad=1&ArticleID=10586

8 APPENDICES

8.1 APPENDIX A

Definitions of some terms that are used are the following.

Signal to Noise Ratio (SNR)

Signal to noise ratio is the ratio of RMS power of signal to the RMS power of all other spectral components excluding harmonics. Its formula is the following.

$$\text{SNR (dB)} = 10\log_{10}\left[\frac{\text{Signal Power}}{\text{Noise Power without Harmonics}}\right]$$

Signal to Noise and Distortion Ratio (SNDR)

Signal to noise and distortion ratio is the ratio of RMS power of signal to the RMS power of all other spectral components including harmonics. Its formula is the following.

$$\text{SNDR (dB)} = 10\log_{10}\left[\frac{\text{Signal Power}}{\text{Noise Power with Harmonics}}\right]$$

Signal to Distortion Ratio (SDR)

Signal to distortion ratio is the ratio of power of signal to the RMS power of harmonics. Its formula is the following.

$$\text{SDR (dB)} = 10\log_{10}\left[\frac{\text{Signal Power}}{\text{Harmonics Power}}\right]$$

Spurious-Free Dynamic Range (SFDR)

Spurious free dynamic range is the ratio of RMS power of signal to the RMS power of spurious signal regardless of where it falls in the frequency spectrum. Its formula is the following.

$$\text{SFDR (dB)} = 10\log_{10}\left[\frac{\text{Signal Power}}{\text{Power of Worsrt Spurious Signal}}\right]$$

Power Supply Rejection Ratio (PSRR)

The PSRR is defined as the ratio of the change in supply voltage to the equivalent (differential) input voltage it produces in the operational amplifier [10].

$$\text{PSRR} = \frac{\Delta V_{\text{supply}}}{\Delta V_{\text{IOS}}}$$