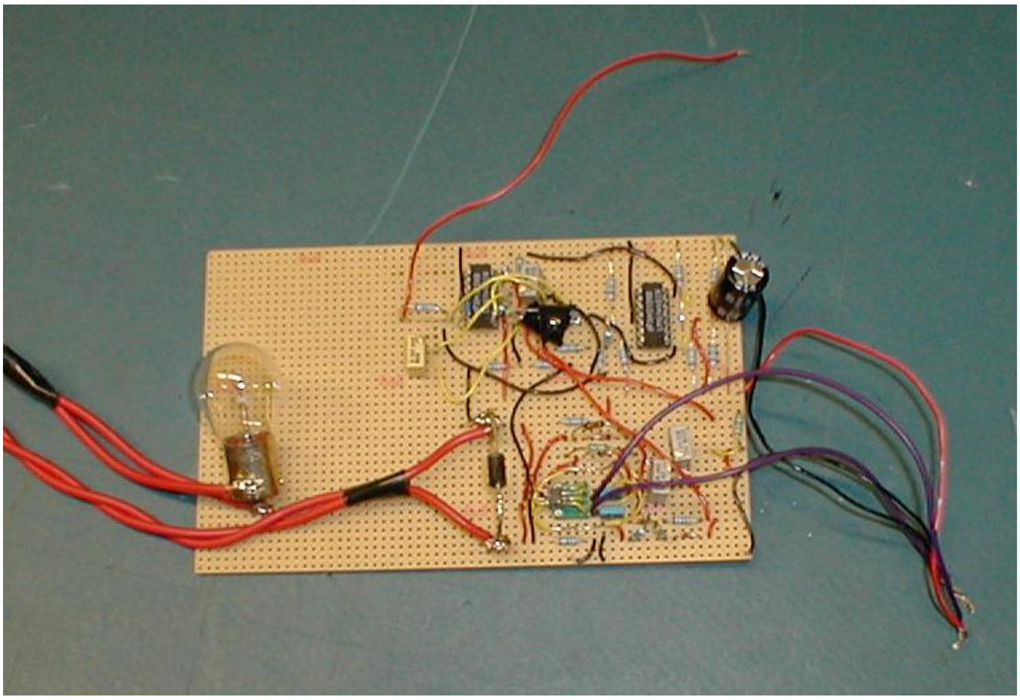
Double MOSFET switching for reducing radiated emissions on the wires to power electronic equipment

Master thesis by

Christian Adolfsson
Pär Madbro



CHALMERS

Department of Electrical Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY,
Gothenburg, Sweden
ISSN 1401-6184
Examensarbete 109E
Examiner: Torbjörn Thiringer

VOLVO
Volvo Car Corporation
Department of Research and Development
Electrical & Electronics Engineering,
VOLVO CAR CORPORATION
Gothenburg, Sweden 2004
Supervisor: Tryggve Tuveson

Titel
Symmetrisk switchning av MOSFET'ar för att minska radiofrekventa störningar.

Title in english
Double MOSFET switching for reducing radiated emission on the wires to power electronic equipment.

Författare/Author
Christian Adolfsson
Pär Madbro

Utgivare/Publisher
Chalmers Tekniska Högskola
Institutionen för elteknik
412 96 Göteborg, Sverige

ISSN
1401-6184

Examensarbete/M.Sc. Thesis No.
109E

Ämne/Subject
Kraftelektronik

Examinator/Examiner
Torbjörn Thiringer

Datum/Date
2004-11-08

Tryckt av/Printed by
Chalmers tekniska högskola
412 96 GÖTEBORG

Abstract

By reducing the RF emission from power electronic equipments, the electromagnetic environment will be improved, which is a big concern when the number of power electronic equipment around us increases, for example in vehicles. In this thesis a circuit made of double MOSFET's have been developed to switch a load in such a manner the RF emissions are reduced.

The designed circuit for switching a load with two MOSFET's is made up of some different major parts. An integrator and an RCD-snubber together with a diode configuration are affecting the rise- and fall-time for the signals to the load so the sum of the two output signals becomes constant. A PD-regulator act as feedback to the MOSFET that acting as a slave in order to ensure that the rise and fall signals are as much as possible in synchronism.

The evaluation of the practical circuit shows that it is possible to lower the RF emission compared to switching with one MOSFET. However, for the case of a load having a low resistance and a substantial inductance, the result was less accurate.

Keywords: double MOSFET, EMI.

Table of contents

List of abbreviation

ALSE	Absorber-lined Shielded Enclosure
AN	Artificial Mains Network
CMRR	Common Mode Rejection Ratio
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
EUT	Equipment Under Test
FFT	Fast Fourier Transformer
LISN	Line Impedance Stabilisation Network
PWM	Pulse Width Modulation
RF	Radio Frequency
RCD-snubber	Resistor Capacitor Diode snubber
V_{bat}	Battery voltage

1 Introduction

The RF emissions in cars are a problem because it leads to interference between different electrical equipment such as radio receivers. Interference in the radio receivers is what the customer immediately will notice, as an irritating noise in the speakers. The frequency range where the disturbances are not desired is from 150 kHz up to 110 MHz where the different locations for radio stations are situated. Various techniques are used today to reduce RF emissions that are generated by switching. Commonly today is to use EMI filters and shielding, EMI filters have some drawbacks such as taking up a lot of space for example and shielding does not eliminate RF emissions from the source itself but do hide so it does not couple with other electronic equipment.

The aim of the thesis is to investigate if it is possible to reduce the RF emissions from switching power electronics equipment by having two MOSFET's that works with 180° phase shift between each other. By having the MOSFET's working in 180° phase shift, the lower MOSFET will work between 0-$V_{bat}/2$ volt and the upper between $V_{bat}/2$ – V_{bat} volt. So, in this way the emitted disturbancs in the supply wire to the load get less dependent on EMI filters or shielding.

To approach the solution to the problem with RF emission from power electronics equipment, the first part of the thesis is an introduction on EMC, EMI and how to measure the radiated emission in a car in a correct way and some theory on the different circuits that will be used. To get a better understanding why the final circuit is designed as it is will be described in the design part and why some ways will not work. The simulation for different parts and the final circuit in PSPICE gives a deeper understanding on how the components work together and separate. By doing the simulations time and money is saved and the simulations gives a hint if something is good or bad which helps the hardware design. In order to utilize PSPICE to evaluate which circuit that works best in reality different circuits have been calibrated and tested which then have been compared with the simulations. With the knowledge of the result of these tests, important conclusions of this project are drawn.

2 EMC/EMI Theory

Because the circuit that is developed with two MOSFET's is planed to be used in vehicles it must full fill the CISPR 25 standard. To better understand the CISPR 25 standard, there is an introduction to EMC and EMI. After this, a concluding part of the CISPR 25 standard appears that's concerning the circuit. This part describes how to measure the disturbances and what the limits are.

2.1 Introduction to EMC

EMC stands for electromagnetic compatibility. A device is electromagnetically compatible if it tolerates the electromagnetic environment and all other devices operating in the same environment tolerate its effects. There exists two broad categories in EMC, electromagnetic emission and electromagnetic susceptibility, these can further be divided into broad categories. For electromagnetic emission these categories are conducted emission and radiated emission, which are significant to this report. The increasing amount of electronic products with power semiconductors the EMI disturbances on the power mains have increased significantly in intensity and frequency of occurrence.

Any electrical equipment, especially semiconductor circuits can be qualified as a potential source of EMI, which will be described later. In general, electrical apparatus can be divided into two principal categories. Equipment whose primary function is to generate and utilize the intentional high frequency signals and those that generate unintentional high frequency electromagnetic signals as a by-product of their primary function. These signals basically appear as electromagnetic noise in the environment. The EMI is originating as a result of quick voltage and current or high amplitude transitions. Classification of the different electromagnetic disturbances can be done on the basis of character frequency content and the transmission mode.

The standard range of radio frequency disturbances starts at 150 kHz. This range is divided in the bands of 0.15 - 30 MHz and 30 – 1000 MHz. The standard limits and procedures for the measurement of radio disturbances are in the frequency range of 150 kHz to 1000 MHz. Figure 2.1 shows the whole usable electromagnetic spectrum to give an overview of where different frequency bands are located and if having disturbances what band they will affect. Because this thesis is concentrated towards radiated disturbances that’s affect radio receivers is the band between 0.15 -30 MHz the most interesting.

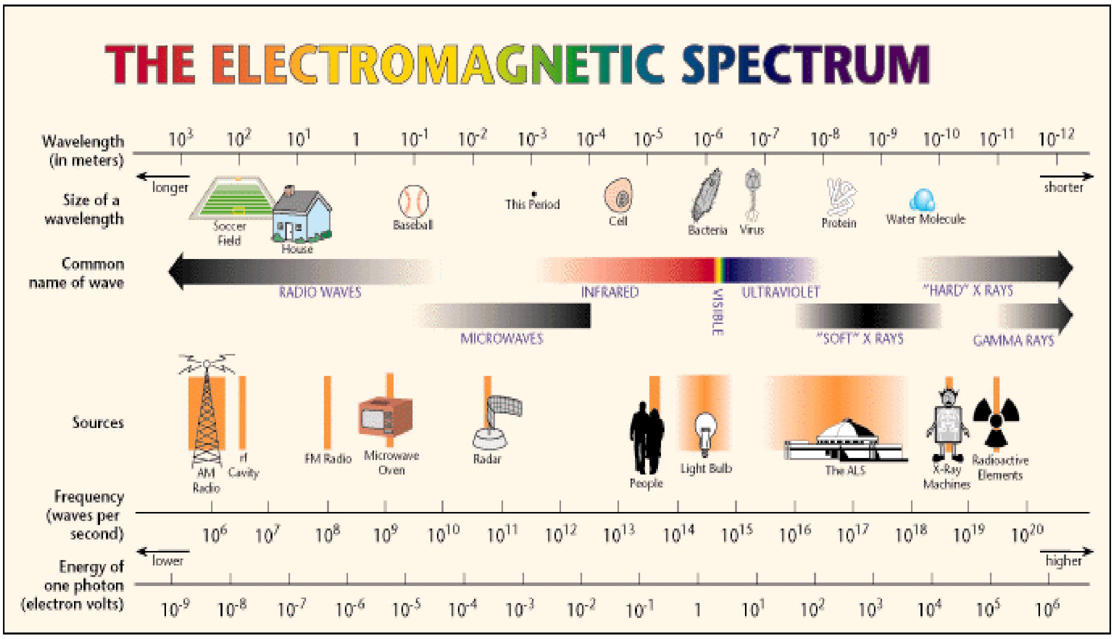


Fig 2.1. Electromagnetic spectrum where the disturbances are not wanted.

2.2 Introduction to EMI [5]

The concepts of the electromagnetic interference situation are quite simple, which basically is divided into two groups, generators and receivers. EMI can only be transmitted in two forms in the environment: conducted and radiated.

Signals having a high frequency that are radiated into the environment qualifies as undesired disturbing signals. Although the levels of these signals are relatively small they are the major cause of EMI. These high-frequency EMI appears as a result of quick voltage and current transitions. Disturbances can be an unwanted signal or electromagnetic noise, which could enter the receiver by the front door or back door. Entry by the front door refers to any undesired signal that enters the receivers input terminal used by desired input signal, whereas the back door refers to any other path, such as radiation directly through the case, see figure 2.2.

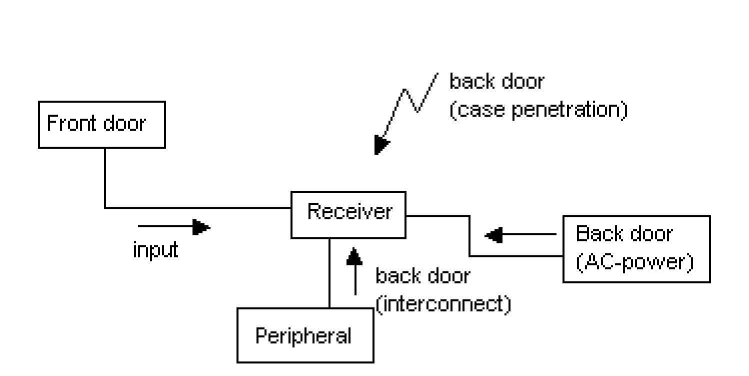


Fig 2.2. Front and back door disturbances entry means to the receiver.

To get a better understanding of what typical EMI generators and receivers are, some are being tabled below.

Some common generators:

- Properly operated transmitter at image frequency
- Properly operated transmitter causing intermodulation or cross-modulation in deficient receivers
- Improperly modulated transmitter
- Receiver local-oscillator or super regenerative emission
- Electrical devices such as motors or relays

Some common receivers:

- Inadequate front-end selectivity resulting in both adjacent-signal reception and image response
- Front-end overload by a strong source, not necessarily on the tuned frequency
- Intermodulation and cross-modulation responses
- Inadequate case shielding

2.2.1 Near field and far field [5]

The emission of a radiating structure has essentially two regions, the near field and the far field. Near fields of radiating structures are considerably more complex than far fields. There exist many definitions of where the transition between the near field and far field begins and end, which is called rayleigh distance, but a roughly criteria is the distance $D= 2*(L_{antenna})^2/\lambda$. Therefore, in the process of measuring the radiated emission for determination of compliance, the measurement antenna is likely to be in the near field of the product from 30 to 200 MHz. This distinction is important because the models that are developed to describe these emissions will need to be considerably more complex to predict near fields accurately. Far fields of radiating structures typically depend on the distance from the radiating structure.

2.3 Comprehensive EMI measurement

Because different types of products produce various kinds of electromagnetic emissions, the emission must be classified and measured in a correct way. Typical emissions for power electronic equipments are broadband and coherent, which are described further on in 2.3.1. Another important classification is in what kind of form the electromagnetic disturbance is generated in, common-mode (asymmetrical) or differential-mode (symmetrical) see fig 2.3 for definition [5].

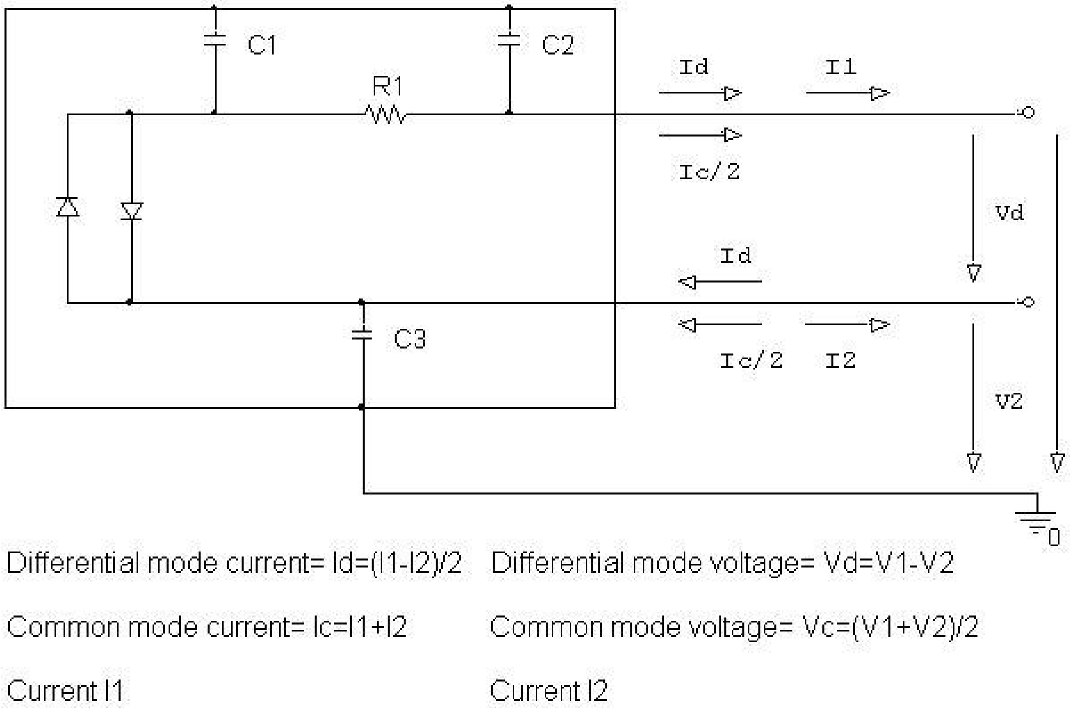


Fig 2.3. Definition for common mode and differential mode EMI voltages and current components in a typical EMI source.

Because of the classifications there exist various kind of detectors for EMI measurement including peak, slide-back, average, effective (RMS), and quasi-peak detectors which are not discussed any further in this thesis but can be read about in reference [6]. For example measurement of common-mode EMI voltage requires an instrument that has an asymmetrical input while differential-mode demands an instrument with a symmetrical input.

2.3.1 Classifying disturbances by frequency content [6]

The frequency spectrum of a broadband electromagnetic disturbance is continuous and covers a relatively wide range. Broadband disturbances are divided into two additional groups, i.e. coherent and non-coherent signals. A signal or emission is coherent when neighboring frequency increments and are related or well defined in both amplitude and phase. For broadband situations, neighbouring amplitudes are approximately equal, while for the non-coherent noise signal the amplitude and phase components are random with no regard to neighboring frequency increments. Classification according to bandwidth means the ratio of the EMI to a reference bandwidth. In EMC practice, this reference bandwidth is the measuring bandwidth, but it can be associated with a potentially susceptible victim receptor too. This ratio can be given in a manner derived from both the measuring bandwidth and the characteristics of the disturbances.

2.4 EMC measurement in vehicles [9]

The limits and the methods of measurement for component on vehicles follow the CISPR 25 standard, which is valid in the frequency range of 150 kHz to 1000 MHz. The standard applies for all electronic/electrical component intended for use in vehicles and large devices. These limits are intended to provide protection for receivers in the vehicle from disturbances produced by components/modules in the same vehicle. Receiver types to be protected by the limits are: sound and television receivers, land mobile radio, radio telephone, amateur and citizens' radio.

2.4.1 Measuring equipment requirements

The equipment shall be calibrated on regular basis to confirm to the required characteristics, the noise floor for the equipment shall be at least 6 dB less than the limit specified in the test plan.

2.4.2 Shielded enclosure

The ambient electromagnetic noise levels shall be at least 6 dB below the limits specified in the test plan for each test to be performed. The shielding effectiveness of the shielded enclosure shall be sufficient to assure that the required ambient electromagnetic noise level requirement is met. The size of the shielded enclosure shall be sufficient to ensure that neither the vehicle/EUT nor the test antenna shall be closer than a) 2 m from the walls or ceiling, and b) 1 m to the nearest surface of the absorber material used.

2.4.3 Measuring instrument bandwidth

The bandwidth of the measuring instrument shall be chosen such that the noise floor is at least 6 dB lower than the limit curve.

2.4.4 Broadcast bands

When measuring the broadcast band shall each band be measured with instrument that have specified characteristic.

2.4.4.1 AM broadcast

The AM broadcast band is divided up in three areas that are:

Long wave 150 – 300 kHz
Medium wave 0,53 – 2,0 MHz
Short wave 5,9 – 6,2 MHz

The measuring system shall have following characteristics:

- output impedance of impedance matching equipment: 50 Ω resistive;
- gain: The gain of the measuring equipment shall be known with the accuracy of ± 0,5 dB. The gain of the equipment shall remain within a 6 dB envelope for each frequency band, see figure 2.4 below.

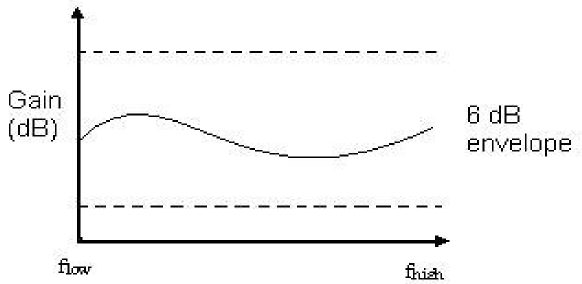


Fig 2.4. Example of gain curve.

- Compression point: The 1 dB compression point shall occur at a sine wave voltage level greater than 60 dB(µV).
- Measurement system noise floor: The noise floor of the combined equipment including measuring instrument, matching amplifier, and preamplifier (if used) shall be at least 6 dB lower than the limit.
- Dynamic range: from the noise floor to the 1 dB compression point.
- Input impedance: The impedance of the measuring system at the input of the matching network shall be at least 10 times larger than the open circuit impedance of the artificial antenna network.

2.4.4.2 FM broadcast (87 MHz to 108 MHz)

Measurement in FM broadcast band shall be done with a measuring instrument that has an input impedance of 50 Ω. If the standing wave ratio is greater than 2:1 an input matching network shall be used. Appropriate correction shall be made for any attenuation/gain of the matching unit.

2.4.4.3 Communication bands (30 MHz to 1000 MHz)

The test procedure assumes a 50 Ω measuring instrument and a 50 Ω antenna in the frequency range 30 MHz to 1000 MHz. If a measuring instrument and an antenna with differing impedance are used, an appropriate network and correction factor shall be used.

2.4.5 Test equipment unique to component/module tests

Following requirements for each device involved in the test equipment are required for a component module test:

- Power supply: The EUT power supply shall have adequate regulation to maintain the supply voltage within the limit specified: 13,5 V ± 0,5 V for 12 V system, 27 V ± 1,0 V for 24 V system, unless otherwise specified in the test plan. The power supply shall also be adequately filtered such that the RF noise produced by the power supply is at least 6 dB lower than the limits specified in the test plan.

- Battery: When specified in the test plan, a vehicle shall be connected in parallel with the power supply.

- Ground plane: The ground plane shall be made of 0,5 mm thick (minimum) copper, brass or galvanized steel for the measurement of conducted or radiated emissions. The ground plane shall be bonded to the shielded enclosure such that the DC resistance shall not exceed 2,5 mΩ. In addition, the bond straps shall be placed at a distance no longer than 0,9 m apart.

2.4.6 Test equipment unique to conducted emission measurements

Following two devices are of importance when measuring conducted emission.

- Artificial mains network (AN) or LISN depending on country: The AN shall have a nominal 5 µH inductance and shall meet the impedance characteristics with a tolerance of ±10 %. The measuring port of all ANs shall be terminated with a 50Ω load. These standards makes the AN to be used up to 108 MHz. For a schematic view of an AN see figure 2.5.

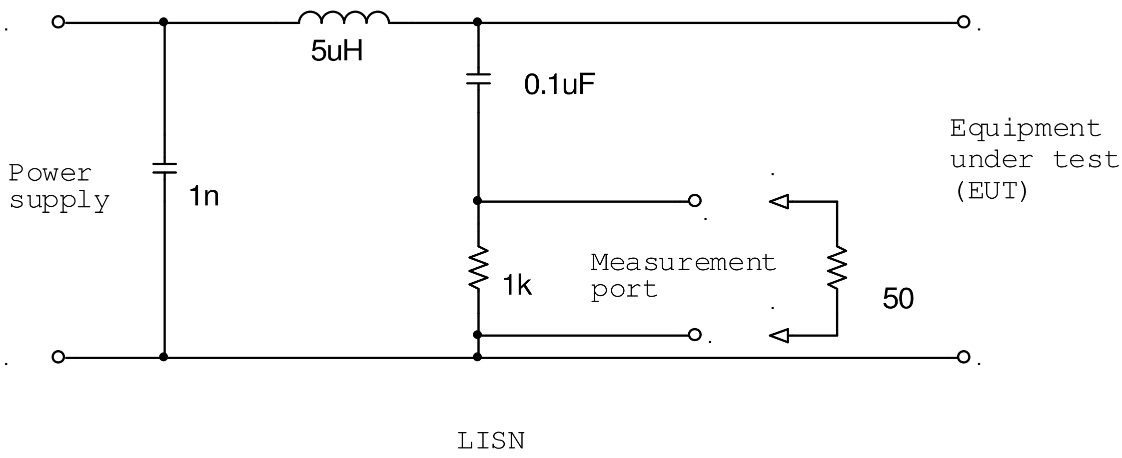


Fig 2.5. Circuit of an AN/LISN.

-Following characteristic shall be taken in consideration when selecting the current probe: the size of the harness to be measured, the frequency range required by the test plan, and the sensitivity of the probe necessary to measure signals at the limit level.

2.4.7 Equipment unique to measurements of component/module radiated emissions

The correction factor for the antenna is applied, and the antenna provides a 50 Ω match to measuring receiver. The standards are based upon following antennas.

- 0,15 to 30 MHz	1 m vertical monopole (where this is not 50 Ω, a suitable antenna matching unit shall be used);
- 30 to 200 MHz	a biconical antenna used in vertical and horizontal polarisation;
- 200 to 1000 MHz	a log-periodic antenna used in horizontal and vertical polarization.

Correct impedance matching between the antenna and measuring receiver of 50 Ω shall be maintained at all frequencies.

2.4.8 Conducted emissions from component/module

In general the emission on power leads shall be measured using an artificial mains network as an isolator. Emission on control/signal leads shall be measured using a current probe.

2.4.8.1 Voltage measurements

Voltage measurements on all power equipments shall be made relative to the case of the EUT (if the case provides a ground return path) or the ground lead as close to the EUT as practical. For the EUT with return line remotely grounded, the voltage measurement shall be made on each lead relative to the ground. The ground plane shall be spaced 50 mm above the test harness.

2.4.8.2 Current probe measurements

Measurements with current probe shall be made on the control/signal leads as a single cable or in sub-groups that is compatible with the physical size of the current probe. The length of the test harness shall be nominally 1,5 m, spaced 50 mm above the ground plane. The test harness wires shall be nominally parallel and adjacent unless otherwise defined in the test plan. Place the current probe 50 mm from the EUT connector and measure the emission, to detect maximum level for frequencies above 30 MHz place the probe in following positions.

- 500 mm from the EUT connector;
- 1000 mm from the EUT connector;
- 50 mm from the AN terminal.

Usually is the position of maximum emission as close to the EUT connector as possible. Where the EUT equipped with a metal shell connector, the probe shall be clamped to the cable immediately adjacent to the connector shell, but not around the connector itself. All parts of the test set-up shall be a minimum of 100 mm from the edge of the ground plane, as illustrated in fig 2.6.

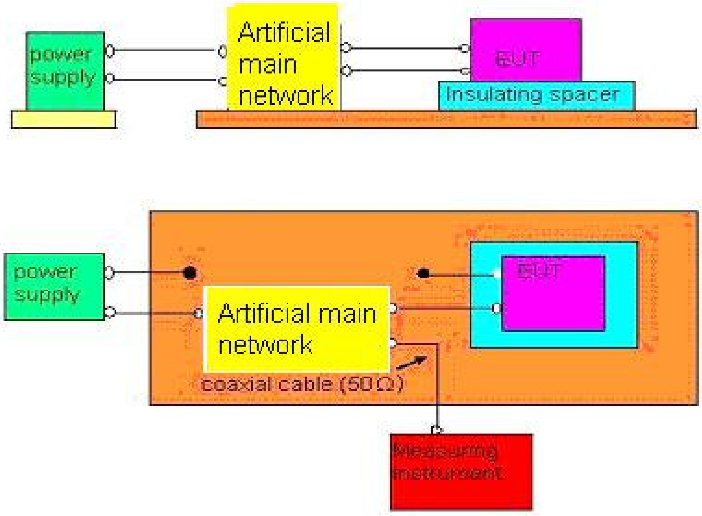


Fig 2.6. Conducting emission test equipment arrangement for 200 mm or shorter power return line.

2.4.8.3 Limits for conducted disturbances from components

Acceptable limits for components conducted disturbances to avoid noise shall not exceed the values in the four tables below, table 1 and 2 concerning power leads and table 3 and 4 concerning control/signal lines. The developed circuit must fulfil class 4 demands to be used in a vehicle.

Class	Levels in dB(µV)									
	0,15 – 0,3 MHz		0,53 – 2,0 MHz		5,9 – 6,2 MHz		30 – 54 MHz		70 – 108 MHz	
	P 1)	QP 2)	P	QP	P	QP	P	QP	P	QP
1	113	100	95	82	77	64	77	64	61	48
2	103	90	87	74	71	58	71	58	55	42
3	93	80	79	66	65	52	65	52	49	36
4	83	70	71	58	59	46	59	46	43	30
5	73	60	63	50	53	40	53	40	37	24

NOTES

For short duration disturbances, add 6 dB to the level shown in the table.

All values listed in this table are valid for the bandwidths in table 3.

1) Peak

2) Quasi-peak

Table 1. Limit for broadband conducted disturbances on power input terminals.

Class	Levels in dB(µV)				
	0,15 – 0,3 MHz	0,53 – 2,0 MHz	5,9 – 6,2 MHz	30 – 54 MHz	70 – 108 MHz
1	90	66	57	52	42
2	80	58	51	46	36
3	70	50	45	40	30
4	60	42	39	34	24
5	50	34	33	28	18
NOTE – For 87 MHz to 108 MHz, add 6 dB to the level shown in table.					

Table 2. Limit for narrowband conducted disturbances on power input terminals.

Class	Levels in dB(µA)									
	0,15 – 0,3 MHz		0,53 – 2,0 MHz		5,9 – 6,2 MHz		30 – 54 MHz		70 – 108 MHz	
	P [1)]	QP [2)]	P	QP	P	QP	P	QP	P	QP
1	100	87	92	79	74	61	74	61	68	55
2	90	77	84	71	68	55	68	55	62	49
3	80	67	76	63	62	49	62	49	56	43
4	70	57	68	55	56	43	56	43	50	37
5	60	47	60	47	50	37	50	37	44	31
NOTES For short duration disturbances, add 6 dB to the level shown in the table. All values listed in this table are valid for the bandwidths specified in table 3.										
1) Peak 2) Quasi-peak										

Table 3. Limit for broadband conducted current disturbances on control/signal lines.

Class	Levels in dB(µA)				
	0,15 – 0,3 MHz	0,53 – 2,0 MHz	5,9 – 6,2 MHz	30 – 54 MHz	70 – 108 MHz
1	80	66	57	52	52
2	70	58	51	46	46
3	60	50	45	40	40
4	50	42	39	34	34
5	40	34	33	28	28
NOTE – For 87 MHz to 108 MHz, add 6 dB to the level shown in the table.					

Table 4. Limit for narrowband conducted current disturbances on control/signal lines.

2.4.9 Radiated emissions from component/module

Conducted emissions will contribute to the radiated emissions measurements because of radiations from the wiring in the test set-up. Therefore, it is advisable to establish conformance with the conducted emissions requirements before performing the radiated emissions test. To eliminate the high levels of extraneous disturbance from electrical equipment and broadcasting stations the measurements of radiated field strength shall be made in an ALSE. The reflection characteristics of the shielded enclosure shall be checked by performing comparative measurements in an open field test site and in the ALSE.

2.4.9.1 Test procedure

The general arrangement of the disturbance source and connecting harnesses etc. represents a standardized test condition. Any deviations from the standard test harness length etc. shall be agreed upon prior to testing and recorded in the test report. The harness (power and control/signal lines) shall be supported 50 mm above the ground plane by non-conductive material, and arranged in a straight line. Maximum emission state shall be made to occur when the EUT is operating under typical loading and other conditions. These operating conditions must be clearly defined in the test plan to ensure supplier and customer are performing identical tests. Depending on the intended EUT installation in the vehicle.

- EUT with power return line remotely grounded: two artificial networks are required, one for the positive supply line and one for the power line;
- EUT with power return line locally grounded: one artificial network is required for the positive supply line.

The EUT shall be wired as in the vehicle and the measuring port of the artificial mains network shall be terminated with a 50Ω load. The face of the disturbance source causing the greatest RF emissions shall be closest to the antenna. Where this face change with frequency, measurements shall be made in three orthogonal planes and the highest level at each frequency shall be noted in the test report. For frequencies above 30 MHz the antenna shall be oriented in horizontal and vertical polarization to receive maximum indication of the RF noise level at the measuring receiver. The distance between the wiring harness and the antenna shall be 1000 ± 10 mm. This distance is measured from the centre of the wiring harness to:

- the vertical monopole element; or
- the midpoint of the biconical antenna; or
- the nearest part of the log-periodic antenna.

Finally the EUT shall be mounted 100 ± 10 mm from the edge of the test bench. To see how the test layout should be see figure 2.7 below.

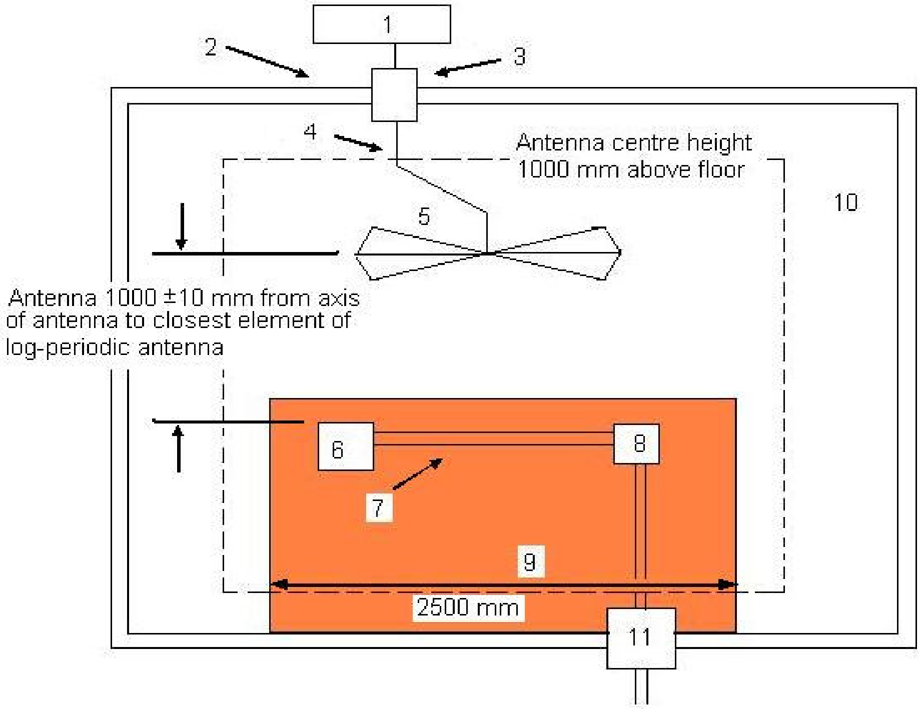


Fig 2.7. Example of a test layout for radiated emission test where the numbers refer to equipment 1) Measuring receiver 2) ALSE 3) Bulkhead connector 4) Double-shielded coaxial cable 5) Antenna 6) EUT 7) Test harness 1500±75 mm long, 50±5 mm above ground plane 8) Artificial mains network 9) Test bench 10) Typical RF absorber material 11) Filter to power supply.

2.4.9.2 Limits for radiated disturbances from components

Because there is difference between the disturbance sources are continuous emitters and require a more stringent limit than disturbance source that is only on periodically or for a short time. The limits in tables 5 and 6 have been adjusted to take account of this fact and measurements need only be performed with one detection type.

Class	Levels in dB(µV/m)									
	0,15 – 0,3 MHz		0,53 – 2,0 MHz		5,9 – 6,2 MHz		30 – 54 MHz		70 – 108 MHz 144 – 172 MHz 420 – 512 MHz 820 – 960 MHz	
	P[1)]	QP[2)]	P	QP	P	QP	P	QP	P	QP
1	96	83	83	70	60	47	60	47	49	36
2	86	73	75	62	54	41	54	41	43	30
3	76	63	67	54	48	35	48	35	37	24
4	66	53	59	46	42	29	42	29	31	18
5	56	43	51	38	36	23	36	23	25	12

1) Peak

2) Quasi-peak

NOTES

1 For short duration disturbances, add 6 dB to the level shown in the table.

2 All values listed in this table are valid for the bandwidths specified in table 3.

Table 5. Limits for broadband radiated disturbances from components.

Class	Levels in dB(µV/m)				
	0,15 – 0,3 MHz	0,53 – 2,0 MHz	5,9 – 6,2 MHz	30 – 54 MHz	70 – 108 MHz 144 – 172 MHz 420 – 512 MHz 820 – 960 MHz
1	61	50	46	46	36
2	51	42	40	40	30
3	41	34	34	34	24
4	31	26	28	28	18
5	21	18	22	22	12
NOTE – For 87 MHz to 108 MHz, add 6 dB to the level shown in the table.					

Table 6. Limit for narrowband radiated disturbances from components.

The circuit which is developed belongs to class 4 but Volvo car corporation limit for narrowband radiated disturbances shall be lower than 30 dB(µV/m).

3 Switching idea and theory on shaping of signals for MOSFET´s

The idea is to have two MOSFET's that are switching against each other to cancel out the radiated emissions from the wires. This is done by letting the upper voltage (V_{upper}) go between V_{bat} and $V_{bat}/2$ and the lower voltage (V_{lower}) go between zero and $V_{bat}/2$, which mean that the sum of the upper and lower voltage shall be V_{bat} at all times, this is shown in figure 3.1. When the sum is equal to V_{bat} at all time it will only be a DC signal seen from the outside and there will not occur any high frequency disturbances.

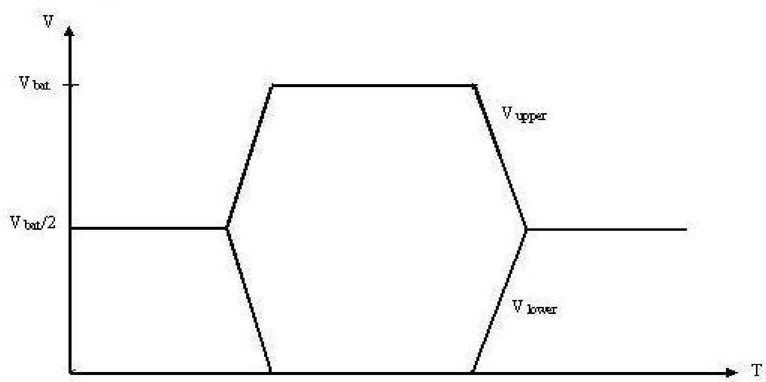


Fig 3.1. Ideal shape of the upper and lower output voltages.

To accomplish that the sum of the upper and lower voltage equals V_{bat} one MOSFET will be master and the other one will be slave. The MOSFET that is acting as the slave shall have the non inverted switching signal added with a regulated feedback signal from the load as it input.

3.1 Theoretical calculations on differences from ideal that can occur with double switching

Because the components are not ideal and that it is hard to have the two signals switching equal against each other, there will exist a differential from an ideal DC level, an acceptable deviation from the ideal vaule is ±1V. The following section describes how much disturbance these deviations from the ideal creates, these disturbances can be compared with a normal switching with one MOSFET between V_{bat} and ground and the result can be seen in fig 3.2.

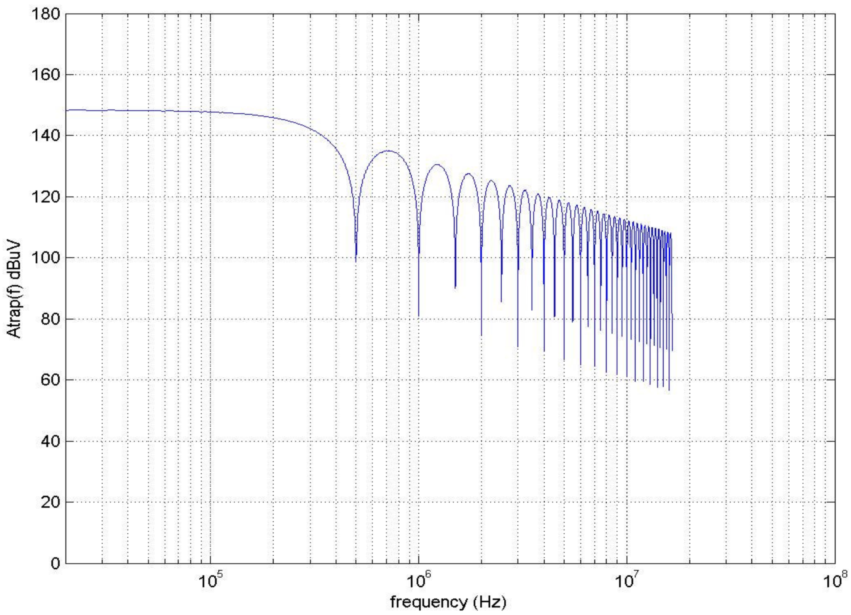


Fig 3.2. FFT of a square wave between 12V and ground.

As can be seen in figure 3.2 there is high amplitude all over the frequency range.

3.1.1 Beginning and end of the pulse

In the beginning and at the end of a new pulse there may occur four important inaccuracies with the switching that will create an increasing EMI. The four inaccuracy aspects are time shift, positive transient, negative transient and oscillation.

The EMI disturbance from a positive- and negative transient is the same if they have the same shape and time duration due to that the energy content is the same in both transients. The graphs are made in matlab with the code from appendix 1.

3.1.2 Time shift

When there is a time shift between the two switches, the result is that on the summation of the two signals and will have a trapezoidal look. When the time shift is equal to the rise time, the result will be a triangle shape instead. As the time shift, difference between fall and rise time increases the resulting deviation gets bigger leading to a larger disturbance in the AM broadcasting band. See figure 3.3 for how a time shift between the two switches can look like and in fig 3.4 is the FFT on a trapezoid made.

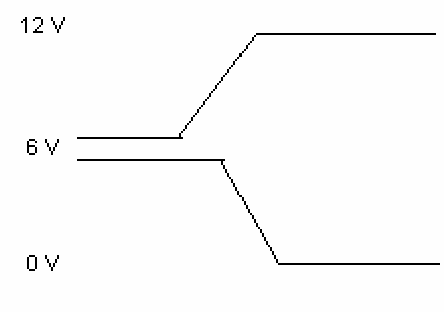


Fig 3.3. Example of how a time shift can look like.

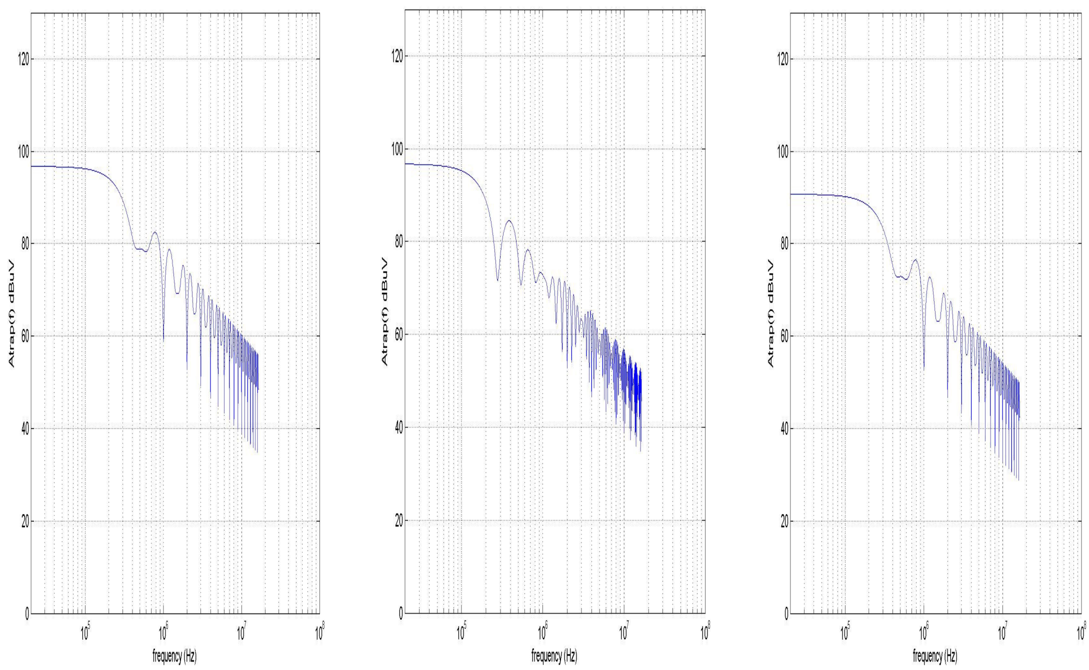


Fig 3.4. FFT of a trapezoid with a) A=1V, t_{rise}=1µs, t_{fall}=1µs, $t_{duration}$=2µs b) A=1V, t_{rise}=2µs, t_{fall}=2µs, $t_{duration}$=1,5µs c) A=0.5V, t_{rise}=1µs, t_{fall}=1µs, $t_{duration}$=2µs.

As can be seen from FFT graph a recurrent time shift occur which will create a trapezoid shape on the DC signal which arise big disturbances in the whole frequency band, if there only would be a DC signal there should not exist any FFT signal in the frequency spectra above.

3.1.3 Positive transient

If there exist a triangle shaped transient in the beginning of the pulse on one of the switches the disturbances will increase. The amount of disturbance depends on the amplitude of the duration. Higher amplitude and longer time duration of the transient leads to more disturbances in the AM broadcasting band. See fig 3.5 for how a positive triangle shaped transient can look like and in fig 3.6 is the FFT calculated for the transient.

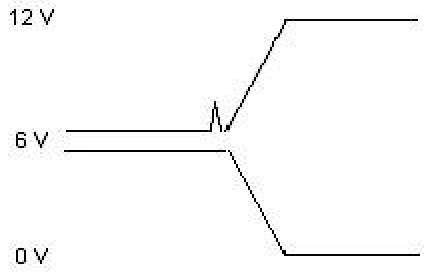


Fig 3.5. A positive transient shaped like a triangle.

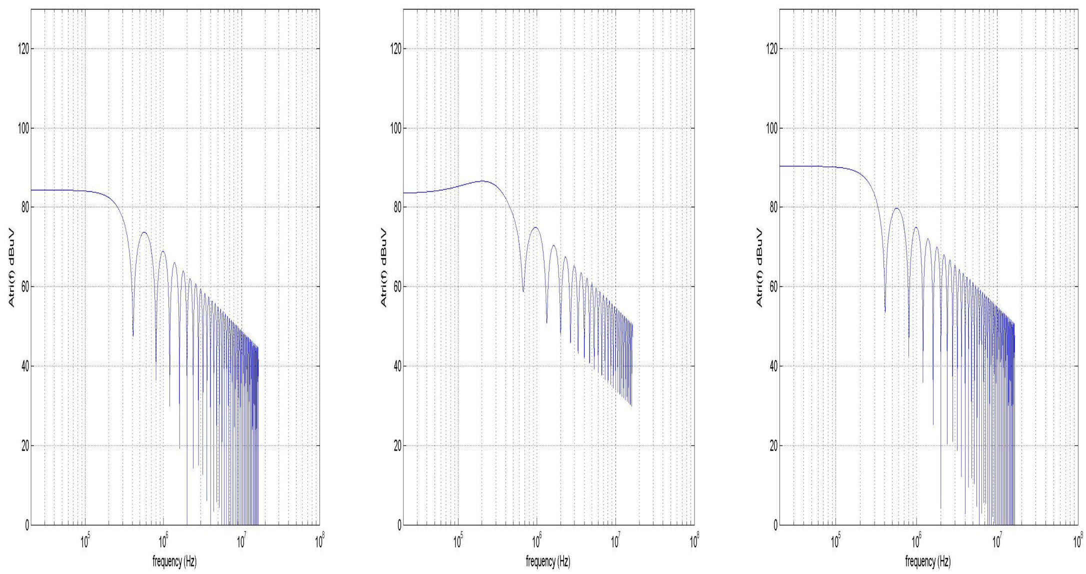


Fig 3.6. FFT of unsymmetrical triangle pulse with a) A=1, t_{rise}=1.5µs, t_{fall}=2.5µs b) A=1, t_{rise} =2.5µs, t_{fall}=3.5µs c) A=0.5, t_{rise} =1.5µs, t_{fall}=2.5µs.

When there is a triangle shaped pulse on the DC signal which is small and fast and recurrent the disturbance does make large distortion as seen in the FFT graphs. As can be seen above in fig 3.6 the disturbances are well above the desired values of the ideal case which should be zero.

3.1.4 Negative transient

Figure 3.7 shows how a negative transient is defined, the calculated spectrum is the same as for positive transient when having the same dimensions.

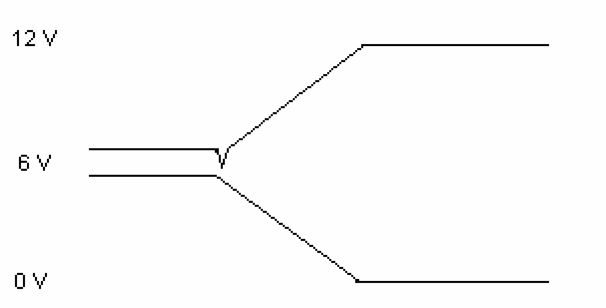


Fig 3.7. A negative shaped triangle transient.

3.1.5 Positive sinus transient

For a positive sinus transient with negative offset, the disturbances will increase with higher amplitude and they decrease with lower amplitude. When the frequency change for the sinus wave arc, the disturbance changes too, lower frequency leads to more disturbance in AM broadcasting band due to the transient duration time gets longer, which is opposite to what happens for higher frequencies. See figure 3.8 for how a sinus transient can appear and in fig 3.9 is the FFT calculated for a sinus transient with an offset to shape the signal to an arc.

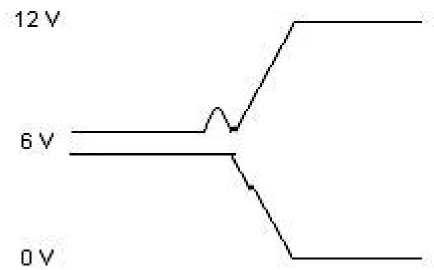


Fig 3.8. A positive transient shaped like a sinus wave arc.

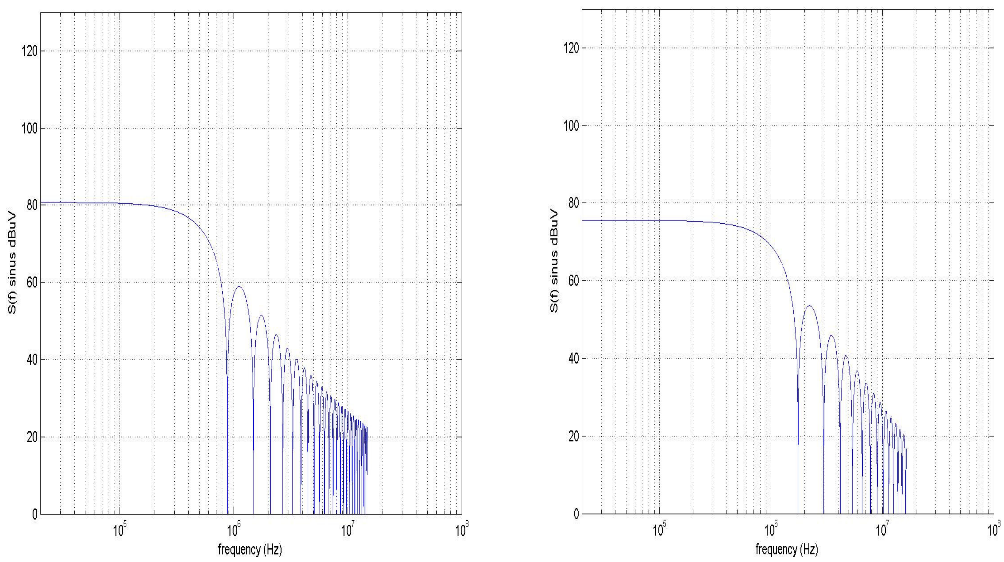


Fig 3.9. FFT of a sinus arched transient with negative offset. First FFT has A=2V, offset=-1V, f=0.2MHz => $t_{duration}$=1.72µs. Second FFT has A=2V, offset=-1V, f=0.4MHz => $t_{duration}$=0.84µs.

When there is a sinus arched transient on the lower or upper voltage as in fig 3.8 it will also occur in the same shape on the sum of the lower and upper voltage. This sinus arc transient disturbance makes large disturbances over the whole frequency spectra in the FFT although it has no sharp edges. It is also seen that if increasing the frequency, the disturbances decreases.

3.1.6 Oscillations

When the pulse turns on/off some oscillation may arise. Such an oscillation will have a great disturbance impact if they are not damped fast. Higher amplitude and higher frequency results in more disturbance. See figure 3.10 for how an oscillation may look when the lower and upper voltage meet at $V_{bat}/2$, in figure 3.11 is the FFT calculated for an oscillation.

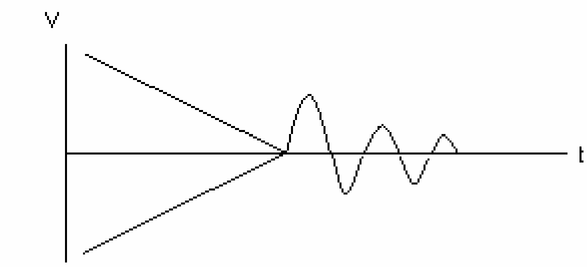


Fig 3.10. Look of oscillation when the pulse turn off.

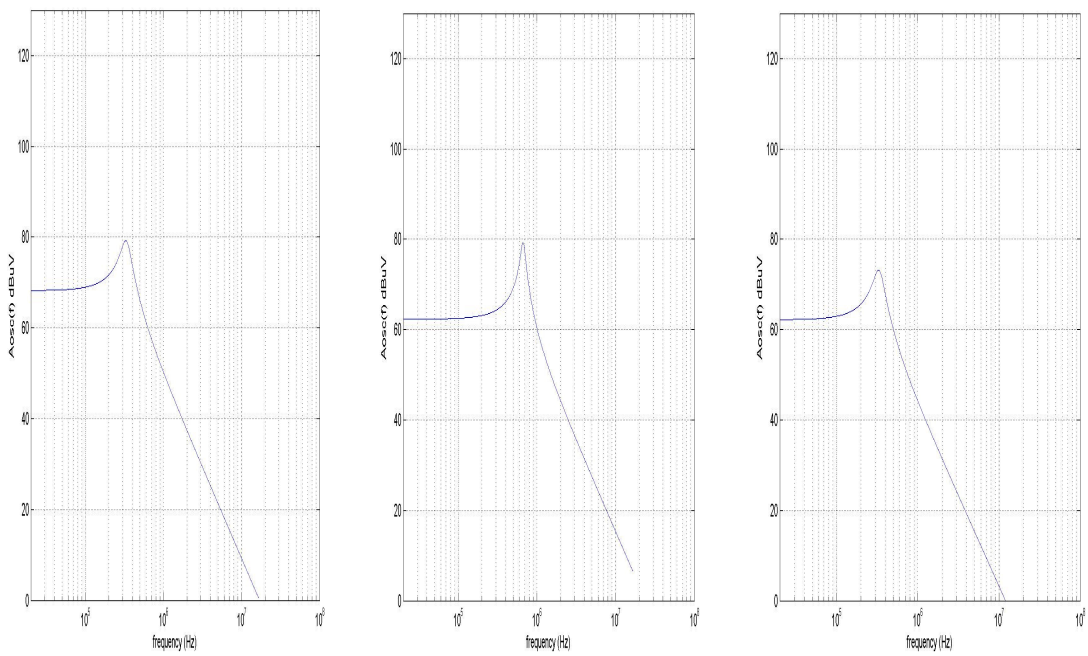


Fig 3.11. FFT of an oscillation with a damping factor=$3*10^5$ and a) A=1V, f_{osc}=333kHz b) A=1V, f_{osc}=666kHz c) A=0.5V, f_{osc}=333kHz.

As can be seen in the FFT graphs the spectrum of the disturbance is high until its eigenfrequency is reached which appears with the self oscillated frequency and then the magnitude decreases rapidly. That's why oscillated disturbances with high frequency must be avoided.

3.1.7 Problems during the on period

The idea with two switches that goes in opposite direction is to cancel out each other's emission the whole time. In order to make this possible they must have the same amplitude seen from $V_{bat}/2$, and equal fall and rise time. During the on time the problem is to keep them at same amplitude otherwise an amplitude difference appears and that leads to emitted disturbance.

3.1.7.1 Amplitude difference

When the amplitude difference gets larger, the disturbance will increase, so it's important to keep the difference as small as possible. In figure 3.12 an amplitude difference can be seen from the outside of the twisted wires. In fig 3.13 the resulting FFT calculated for an amplitude difference is presented.

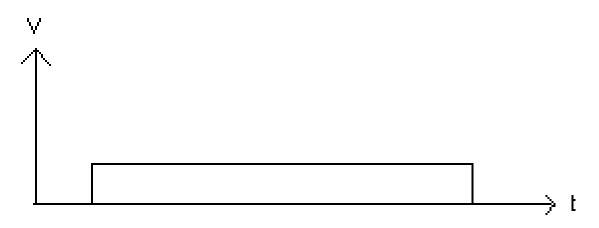


Fig 3.12. A voltage amplitude difference between the two switches.

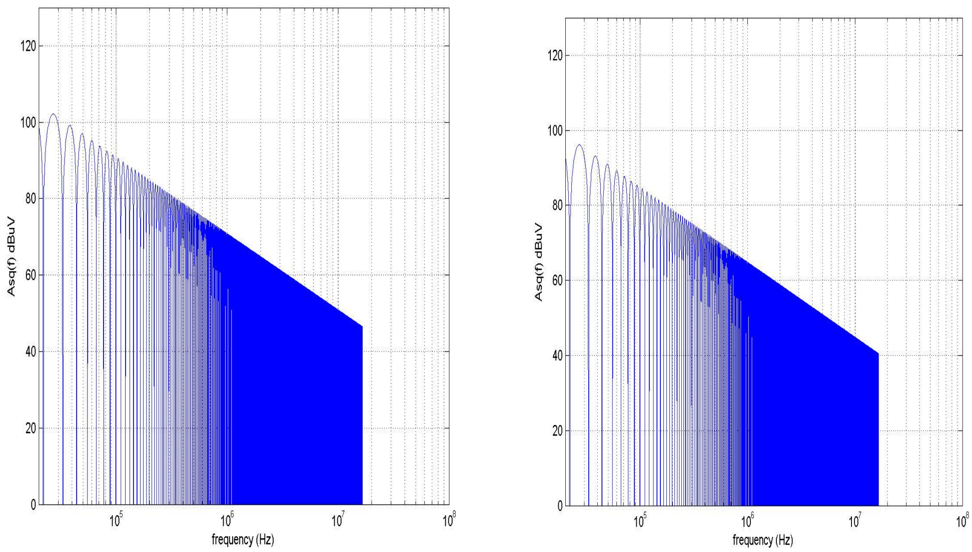


Fig 3.13. FFT of a square wave with a). amplitude=1V and time duration=20µs. b). amplitude=0.5V and time duration=20µs.

Because a square formed disturbance is built up of the whole frequency spectra, the disturbances decrease slowly for higher frequencies in the FFT when it appears on a DC signal as is shown in fig 3.12.

3.2 Miller capacitance [7]

MOSFET devices have a considerable miller capacitance between their gate and drain terminal which affect the time constant of fall and rise time. This is rarely no concerns for low voltage or slow switching applications, but this can cause problem when high voltages are switched quickly. One problem that occurs when using a circuit with MOSFET is to have the same result in the circuit when it is massproduced. This is due to that the miller capacitance in the MOSFET that affects the upper frequency limit. The miller capacitance is different as an unavoidable feature of the manufacturing, every MOSFET have different miller capacitance, even in the same series that becomes a problem when equal result is demanded for every circuit that is produced. When a producer stop producing a particular series it should be possible to replace the MOSFET without changing the whole circuit. This problem can be solved in theory by inserting a compensating capacitor of approximately 1-100nF between the gate and the drain, see figure 3.14, that is a factor 10-100 times bigger than the miller capacitance that often have a value between 10-1000pF.

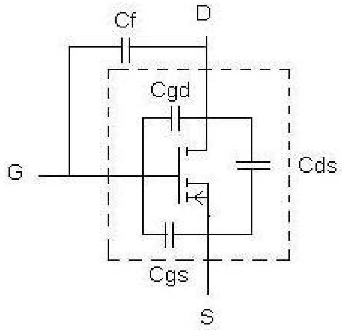


Fig 3.14. C_f is the compensating capacitor and C_{gd} is the miller capacitance.

Since the external capacitance will be added to the internal, the small value of the internal capacitance can be neglected making the capacitances more equal to each other. This makes the time constant $t=R_G(C_{gd}+C_f+C_{gs})$, and as above, C_{gd} and C_{gs} are very small making $t=R_G*C_f$.

3.3 Snubber circuits, design and theory [1]

The function of snubber circuits is to limit the electric stress to safe levels on the components during the switching. The switching stresses are limited to safe levels by:

1. Limiting voltage applied to devices during turn-off transients
2. Limiting device current during turn-on transient
3. Limiting the rate of rise (*di/dt*) of current through devices at devices turn-on
4. Limiting the rate of rise (*dv/dt*) of voltage across devices during devices turn-off or during reapplied forward blocking voltages
5. Shaping of the switching trajectory of the device as it turns on and off

There are three broad classes of snubber circuits, these are:

1. Unpolarized series R-C snubbers used to protect diodes and thyristors by limiting the maximum voltage and *dv/dt* at recovery, characteristic and the circuit can be seen in fig 3.15.

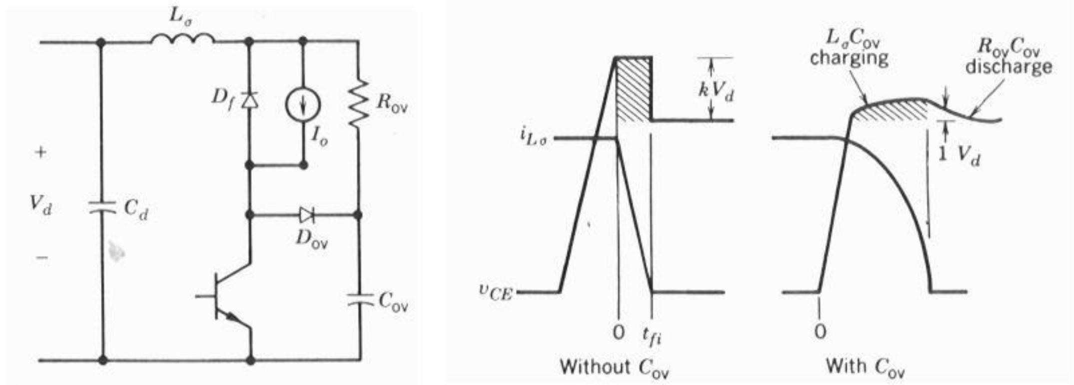


Fig 3.15. Circuit for over voltage snubber and its characteristic.

2. Polarized R-C snubbers. These snubbers are used to shape the turn-off portion of the switching trajectory of controllable switches, to clamp voltages applied to the devices to safe levels, or to limit *dv/dt* during devices turn-off. In fig 3.16 is the circuit and characteristic shown.

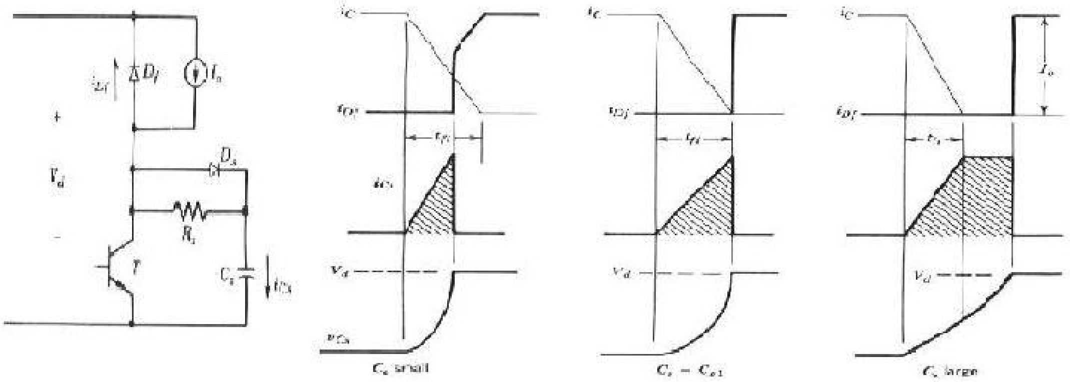


Fig 3.16. Circuit for turn-off snubber and its characteristic.

3. Polarized L-R snubbers. These snubbers are used to shape the turn-on switching trajectory of controllable switches and/or to limit *di/dt* during devices turn-on. In fig 3.17 is the circuit and characteristic shown.

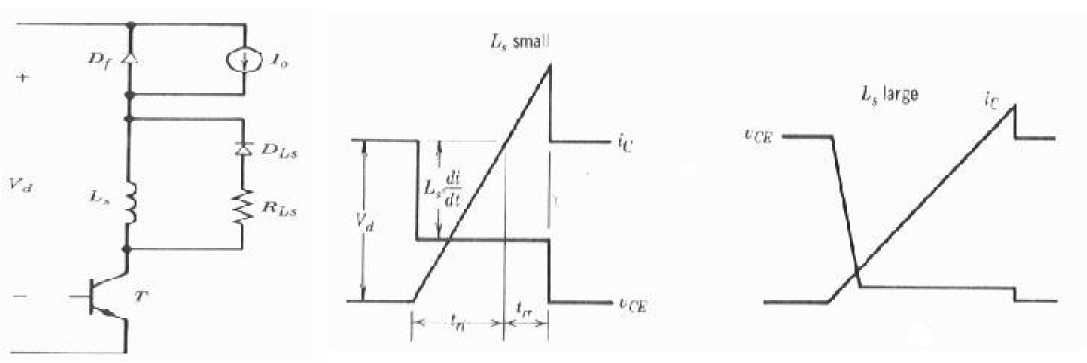


Fig 3.17. Circuit for turn-on snubber and its characteristic

These three classes of snubber circuits can be combined into one circuit called Undeland snubber that regulates over voltage, turn-on and turn-off, which circuit is shown in fig. 3.18.

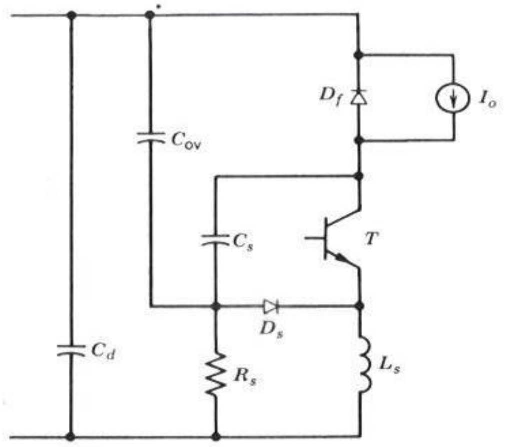


Fig 3.18. Undeland snubber circuit for step-down converters

3.3.1 RCD-snubber

The RCD-snubber that will be further discussed in this part is shown in figure 3.16. The capacitance value in an RCD-snubber is decided to either minimize switching loss or to minimize total loss. The capacitance can be decided for three different cases. If the value of C_s are chose to C_s=$C_{s,normal}$, then capacitor voltage rises to V_s at the current fall time t_s (normal snubbering). When $C_s < C_{s,normal}$ then the capacitor voltage reaches V_s before the current fall time is reached (undersnubbering). And for large C_s, $C_s > C_{s,normal}$, the capacitor voltage rises slowly and takes longer than t_s to reach V_s (oversnubbering). The capacitor current is equal to the load current. To minimize the total losses the capacitor is chosen for the undersnubbered case and to minimize switching losses the capacitor is chosen for the oversnubbered case. Snubber resistance are chosen so that the peak-current through it is less than the reverse-recovery current of the freewheeling diode. The minimum snubber resistance are $R_{s,min}=V_s/(k_{rr}*I_L)$ where k_{rr} is the reverse-recovery factor ($0<k_{rr}<=0.2$).

4 Design of circuit

The design is built upon two MOSFET´s. The first idea was two have two N-MOS's but there were several disadvantages with a configuration like that. Main disadvantage is that with a configuration like that there has to be a buck converter to have an output signal level that is needed for the end product, because the N-MOS had troubles with reaching the supply voltage. The idea with two N-MOS's was abandoned and instead a configuration built upon one N-MOS and one P-MOS was used.

The P-MOS is going to work as a master switch in the circuit. This means that the component values around this switch will be kept constant. Then the N-MOS will act as a slave where there is going to be a couple of circuits working for eliminating the differences between the two MOSFET´s outputs.

4.1 MOSFET setup

The design is built up around two MOSFET´s. One P-MOS and one N-MOS where the P-MOS will act as a switch for the upper level between $V_{bat}/2$ and V_{bat}. The N-MOS is working in the area between ground and $V_{bat}/2$. In figure 4.1 the setup is shown for how the load is attached to the MOSFET´s and how the MOSFET´s are located to each other.

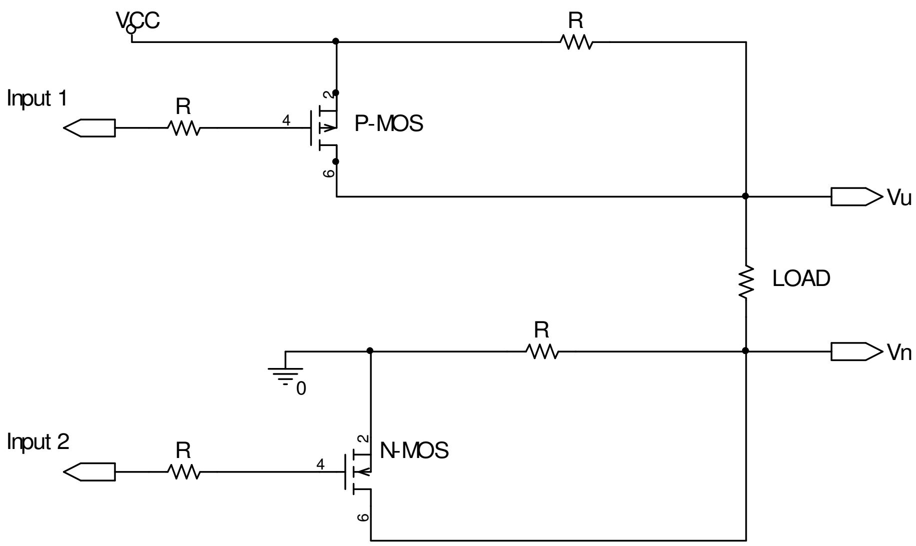


Fig 4.1. Setup of the two MOSFET´s.

In figure 4.1 the setup of the two MOSFET´s can be seen. This is the basic configuration that will be examined with different circuit solution.

4.2 Input signal to MOSFET

There is a need of two input signals, one for each MOSFET where one is inverted to the other. The idea is to have the two input signals as equal as possible to minimize the difference between the outputs of the MOSFET, but for the difference between the two outputs, a regulated signal will be added up to the N-MOS.

The requirements of the input signals are that they have to have a slew rate that are not too fast, so the MOSFET have time to switch before the input have reached its maximum/minimum level. This is because it should be possible to change the input signal while the output signal switches, if then changing the input signal when the output is switching the speed of the slope can be altered. The idea is to have a square wave input that will be integrated over time. If integrating, it is easy to choose a desired slew rate with one capacitor or resistor value.

The output from the integrator is supposed to be the source of input for both MOSFET´s. Then the output from the integrator has to be inverted for one of the inputs to the MOSFET. The signal intended for the master, P-MOS, will get its input from the inverter. This choice fell out since the input signal for the slave, N-MOS, have to go through at least one more stage than the master. And because of that, there will be less time delay between the two input signals.

The hardware integrator is built up with an operational amplifier with an input resistor and a feedback capacitor. There is a need of a rail-to-rail and single supply operational amplifier because of the MOSFET and that it is a battery application. Rail to rail so that it is sure that the MOSFET is running in either saturated or off mode and single supply since the battery gives ground and approximately +12V, or V_{bat}. The circuit for making the input signals is shown in figure 4.2.

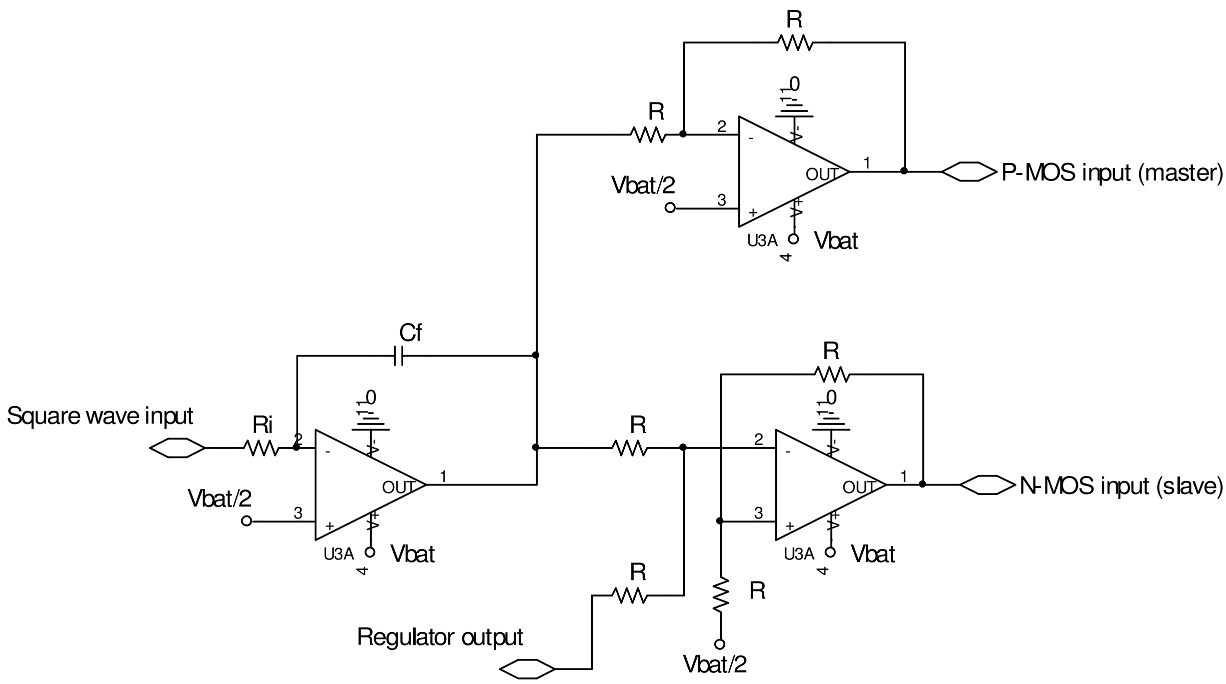


Fig 4.2. Design of input circuit.

If the integrator has a constant input then it produces a constant rate of change of voltage at the output. The time constant may be set by the term 1/RC and since the output slew rate of the MOSFET should be at least 20us, the output from the integrator needs to be larger than that. From the integrator there are two branches, one for the P-MOS input where the signal goes through an inverter with the gain –1. The second branch is for the N-MOS input where the signal goes through a non-inverting summation where the signal is added up with the signal coming from the regulator output. This one has a gain of +1.

4.3 Internal capacitances of MOSFET

Because of that the design are built up around two MOSFET´s, then the characteristics of the two MOSFET´s have to be taken care off. One issue that is different from MOSFET to MOSFET is its internal capacitances.

Charges in a MOSFET that have to be moved on are those in stray capacitances and depletion layer capacitances. These capacitances can be modeled when the MOSFET is in the active or cut-off region with an equivalent circuit shown in fig. 4.3. The drain-source capacitance is not included in the equivalent circuit since it will not affect the switching characteristics of the MOSFET, but for example in a snubber design it has to be included since it can be a part of a total capacitance requirement.

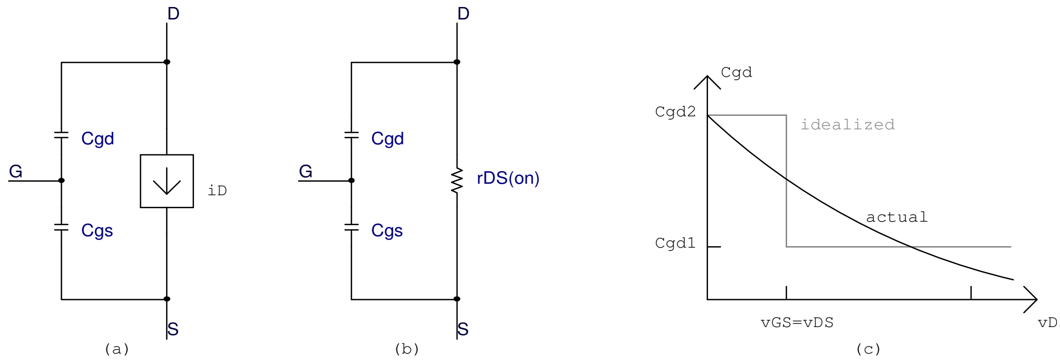


Fig 4.3. (a): MOSFET in active and cutoff region; (b): MOSFET in ohmic region; (c): Variation in C_{gd} with v_{DS}

The current source in the equivalent circuit above is equal to zero when $v_{GS}<V_{GS(th)}$, and when device is in active region it is equal to $g_m(v_{GS}-V_{GS(th)})$. The drain current is linear over most of its range in the active region and the slope of the transfer characteristics is the transconductance g_m. When v_{DS} is less or equal to $v_{GS}-V_{GS(th)}$ the MOSFET enters the ohmic region. When the device is on, $v_{GS} >> V_{GS(th)}$, making the criteria for entering the ohmic region simplified to $v_{DS} < v_{GS}$. In the ohmic region the current source is no longer valid because of that the inversion layer shorts the drain to the source, so the drain end of C_{gd} in the ohmic region equivalent circuit is shown as grounded. On-state resistance $r_{DS(on)}$ is added to the equivalent circuit for the ohmic losses. The capacitances C_{gd} and C_{gs} vary with the voltage across them, C_{gs} is a combination of the electrostatic capacitance of the oxide layer in series with the capacitance of the depletion layer. The change in C_{gd} occurs because of the voltage change across it, v_{DS}, is much larger than the voltage change across C_{gs}. As seen in fig. 4.3 the change in C_{gd} with v_{DS} can be as much as a factor between 10 to 100. For calculations C_{gd} is set to the two discrete values C_{gd1} and C_{gd2} with the change in value occurring at $v_{GS}=v_{DS}$, where the MOSFET is either leaving or entering the ohmic region. The capacitance C_{gs} is assumed to be constant.

The switching behavior of a MOSFET with the gate driven from a voltage source with an external gate resistance R_G needs to be taken care of since there are no MOSFET´s that have equal specifications, and the configuration needs two MOSFET´s that switch equal. The changes in specifications lead to differences in values of C_{gs} and C_{gd}.

When turning on a MOSFET, v_{GS} will rise from 0 to $V_{GS(th)}$ because of currents going through C_{gs} and C_{gd}. The rise in this region is approximately linear with a time constant of $t_1=R_G(C_{gs}+C_{gd1})$. When v_{GS} reaches $V_{GS(th)}$, the drain current increases and when the drain current equals the load current (I_0), v_{GS} will be clamped at the gate-source voltage needed to keep $i_D=I_0$. In this case, the entire gate current flows through C_{gd} causing v_{DS} to decrease in two intervals. In the first interval $C_{gd}=C_{gd1}$ and in the second $C_{gd}=C_{gd2}$. When v_{DS} have completed its decrease, the gate-source voltage will become unclamped and continue its way up to V_{bat} with a time constant of $t_2=R_G(C_{gs}+C_{gd2})$, at the same time the gate current will decrease at the same pace. When turning off the MOSFET, the same behavior will arise and the same time constants can be used to determine its behavior.

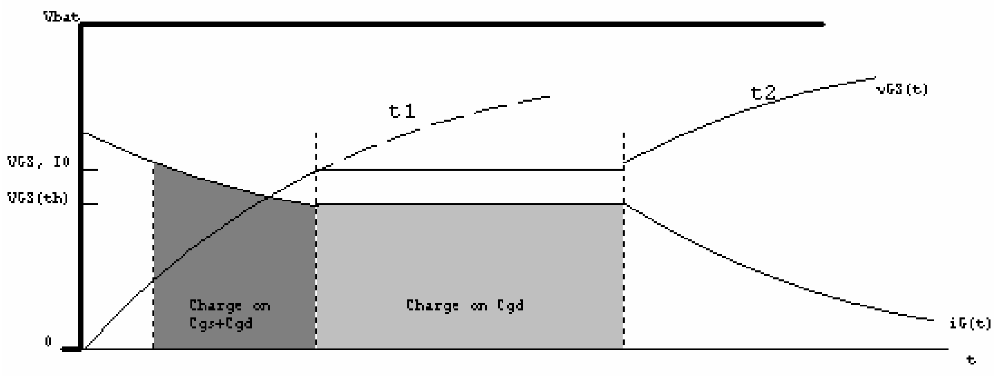


Fig 4.4. Turn-on voltage waveform.

As can be seen in fig. 4.4, the rise and fall times of the MOSFET when switching are dependent on the gate-source capacitance, the gate-drain capacitance and the gate resistance. Since the capacitances in a MOSFET can vary, causing MOSFET´s to switch with different time-constants, it is good to choose the gate resistance for each MOSFET to compensate for each time-constant.

4.3.1 Compensation of time constants with diode configuration

Because of the scheme that the two MOSFET´s are switching at, one is in turn-on mode when the other one is in turn-off mode. There is a need of a solution where both turn-on and turn-off can be specified so the MOSFET´s can be adjusted to each other. As seen earlier, the time constants are depending on the gate resistance, the gate-source capacitance and the gate-drain capacitance. An easy solution would then be to regulate the gate resistance of one MOSFET until the time constant is equal to the second MOSFET´s time constant.

$$t_{1(m1)} = R_{G(m1)}(C_{gd1(m1)} + C_{gs(m1)}),\ \ Eq.\ 4.1 \qquad t_{2(m1)} = R_{G(m1)}(C_{gd2(m1)} + C_{gs(m1)}),\ \ Eq.\ 4.3$$
$$t_{1(m2)} = R_{G(m2)}(C_{gd1(m2)} + C_{gs(m2)}),\ \ Eq.\ 4.2 \qquad t_{2(m2)} = R_{G(m2)}(C_{gd2(m2)} + C_{gs(m2)}),\ \ Eq.\ 4.4$$

Regulating only R_G will reduce the error between the different time constants of the two MOSFET´s but it cannot be perfect since it is two time constants and three capacitor levels per MOSFET. If setting $R_{G(m2)}$ to regulate for the error between the time constants, then we could have $R_{G(m1)}(C_{gd1(m1)}+C_{gs(m1)})=R_{G(m2)}(C_{gd1(m2)}+C_{gs(m2)})$, but then there is one case that is not taken care of. To fill in the error of the second time constant, there is a need of a gate resistance that is having one value when it is in on-state and one value when it is in turn off-state. This is accomplished by using two different R_G per MOSFET in parallel with each other. In series with each R_G there is a diode that should conduct at either turn on or turn off-state. It works according to the following: When in turn on-state there is a diode coupled that is to be reverse biased, making that path the gate resistance. When in turn-off state there is a forward biased diode making that path to the gate resistance. It works in the same way for both N-MOS and P-MOS. The idea is presented in figure 4.5.

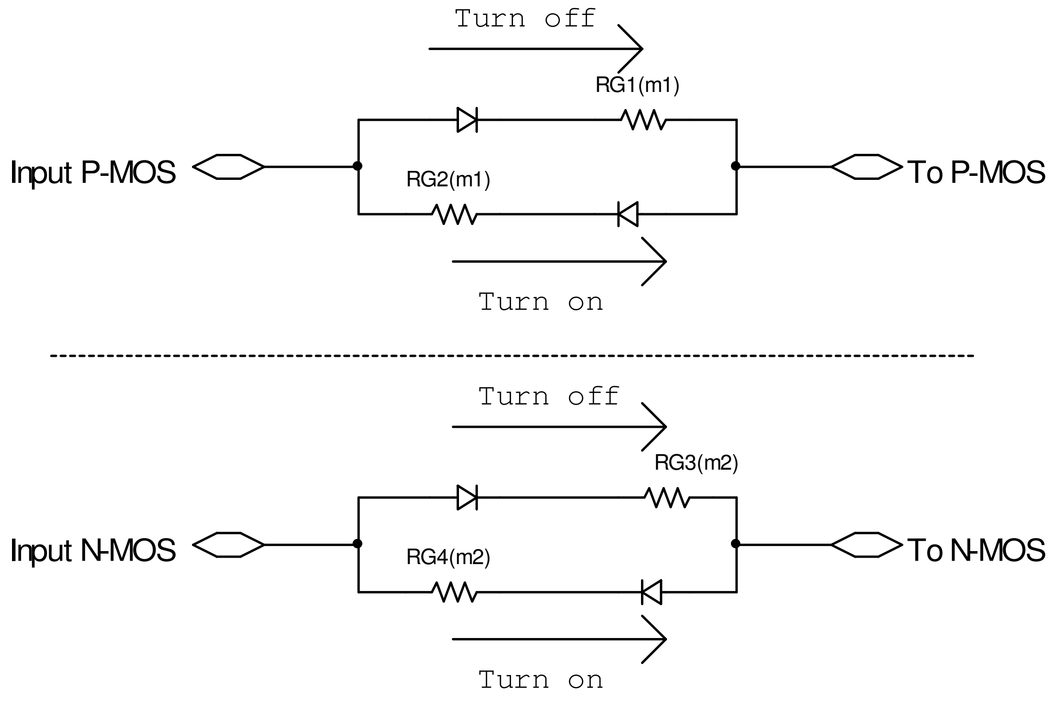


Fig 4.5. Circuit for setting time constants equal to each other.

The adjustment works in the following way: Let the gate resistors to the P-MOS ($R_{G1(m1)}$, $R_{G2(m1)}$) be fixed, then vary $R_{G3(m2)}$ to compensate for the difference in time constants when turning off the N-MOS and on the P-MOS. Vary $R_{G4(m2)}$ to compensate for time differences when turning on the N-MOS and turning off the P-MOS. Since the gate resistance are governing the rise/fall time of the MOSFET, it is important to choose a value that keeps the signal in a range that suits the input frequency.

4.3.2 Shape signal with snubber network

The snubber that has been used is a so-called turn off snubber. The turn off snubber have a function that should provide a zero voltage across the MOSFET while the current turns off. The design of the snubber consists of a RCD-network that is placed between the MOSFET´s drain and source, as can be seen in fig. 4.6.

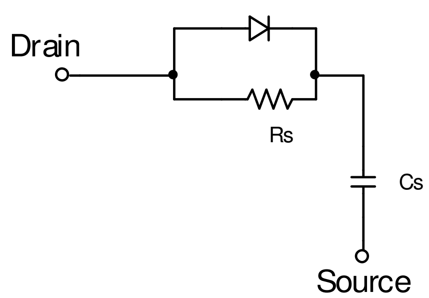


Fig 4.6. RCD-network acting as a snubber

The function of a snubber network is to limit the rate of change of the voltage across the output terminal. In a RCD-snubber the rate of change of the voltage on the output is dominated by the capacitor while the resistor is used primarily to limit the peak current flowing through the MOSFET. The resistor is sized so the maximum load current will produce a voltage less than the minimum power supply voltage. The maximum resistance for the snubber is given by [11]:

$$R_{\max} = \frac{V_d}{0.2I_0} = \frac{12}{0.2 \cdot I_0} = \frac{60}{I_0}\Omega, \quad Eq.\ 4.5$$

The capacitance is calculated from the peak current and the target rise time, the capacitance is given by [11]:

$$C = I_{peak} \cdot \frac{dt}{dv} = I_{peak} \cdot \frac{6\mu s}{12V} = \frac{I_{peak}}{2}\mu F, \quad Eq.\ 4.6$$

These results have been optimized during the simulation and hardware testing to be able to get a snubber that is optimized for the total circuit. Depending on how the output signals are looking, there is a possibility to change the values to change the limit of peak current and the rate of change of the voltage.

4.4 Feedback

The fault that is remaining after adding the gate resistors and external capacitances has to be eliminated in some way. The idea is by using a feedback circuit to cancel the remaining fault in the sum of the two output signals. This is done by adding up the two output switch signals to each other, amplify the result and add it up to the input signal of the lower MOSFET.

When calculating the fault of the signal, it will show a result of below $V_{bat}/2$ if the lower switch is too fast and a result of above $V_{bat}/2$ if it is too slow. This result is supposed to make the rise/fall time of the input go faster or slower to steer the input of the MOSFET. To make an adder for the two output signals from the MOSFET´s that will show the result around a reference of half the battery voltage, approximately 6 volt, one can simply use an operational amplifier configured as a non inverting summer, figure 4.8, with a unity gain buffer for holding the voltage reference. The non-inverting summer have an output of

$$V_O = V_{i1}\left(\frac{R_{i2}}{R_{i1}+R_{i2}}\right)\left(1+\frac{R_f}{R_i}\right) + V_{i2}\left(\frac{R_{i1}}{R_{i1}+R_{i2}}\right)\left(1+\frac{R_f}{R_i}\right), \quad Eq.\ 4.7$$

Where if R_{i1} and R_{i2} are equal there will be an addition of the two signals that are proportional to each other. The resistors R_f and R_i will set the amplification of the output signal and since the negative input of the operational amplifier have a potential of $V_{bat}/2$, the result of the output signal will vary around that potential.

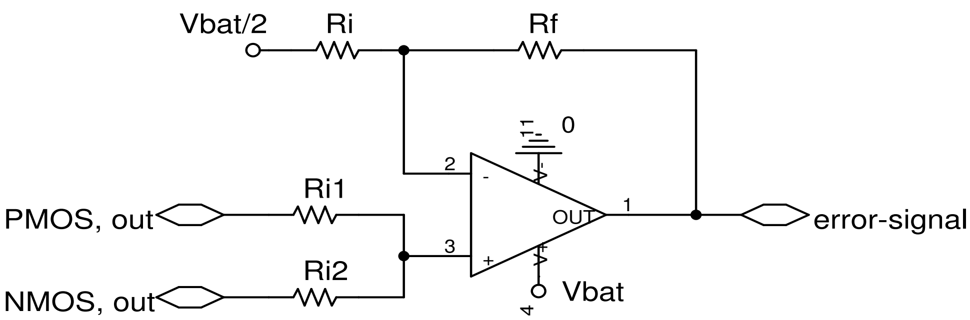


Fig 4.8. Non-inverting summer for the fault between the two outputs

The non-inverting summer in figure 4.8 is supposed to add up the two output signals from the two MOSFET´s. The resistors R_{i1} and R_{i2} are set to be equal and by increasing or decreasing R_f the gain of the difference may be set.

4.4.1 Detection of the error between MOSFET´s output

To be able to get a circuit that have two MOSFET´s that switches equally inverted to each other, it is good to have an error detection to know how to steer the MOSFET´s to minimize the discrepancy. The errors will not occur when the MOSFET´s are stable, e.g. when in saturated or in cut off mode. The errors will occur when going from saturated mode to cut off mode. Errors because of different rise/fall times and that one MOSFET are switched before/after the other MOSFET. The idea is to detect the error and then change one of the input signals to minimize it.

If summing the two output signals to each other, the result should be V_{bat}. If there is a difference between the two signals the sum will be greater or less than V_{bat}. Since there is problem to handle a signal that is above V_{bat}, the summing application has a reference signal putting the result around Vbat/2. This summing application is done with an operational amplifier coupled as a non-inverted summer.

The advantage of having the result of the error around $V_{bat}/2$ is that it is enough by having one calculation of the error. There are four kinds of fault that can occur and following text explains how all four errors are taken care of when it is around $V_{bat}/2$.

4.4.1.1 Upper level faster than lower

When the P-MOS switches earlier than the N-MOS or if the slew rate is faster for the P-MOS, then there will be two different faults depending on if the P-MOS is turning on or off.

4.4.1.1.1 When upper turns on

In this case where the P-MOS if faster than the N-MOS and is turning on, going from $V_{bat}/2$ to V_{bat}, the input to the N-MOS are going from 0 to V_{bat}. Though the N-MOS output is going from $V_{bat}/2$ to ground and then have to be quicker switched leads to that the input to the N-MOS has to be quicker as well. This error-signal has to be larger than $V_{bat}/2$ so when adding the fault signal to the input, it will make it faster. Figure 4.9 shows the principle.

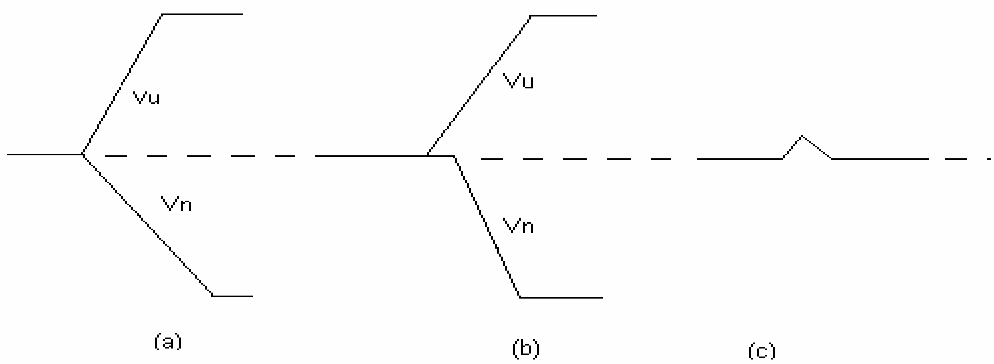


Fig 4.9. (a) P-MOS have faster slew rate (b) P-MOS switches earlier (c) arised fault.

The arised error that can be seen in figure 4.9c is to speed up the slew rate of the input signal to the N-MOS. The error occurs when the upper output signal is switched before the lower or if it has a faster slew rate.

4.4.1.1.2 When upper turns off

P-MOS turns off and is quicker than the N-MOS which is going from 0 to $V_{bat}/2$. N-MOS input signal have a falling edge leading to that the fault have to be less than $V_{bat}/2$ to be able to speed up the lower output level. The result is showed in figure 4.10.

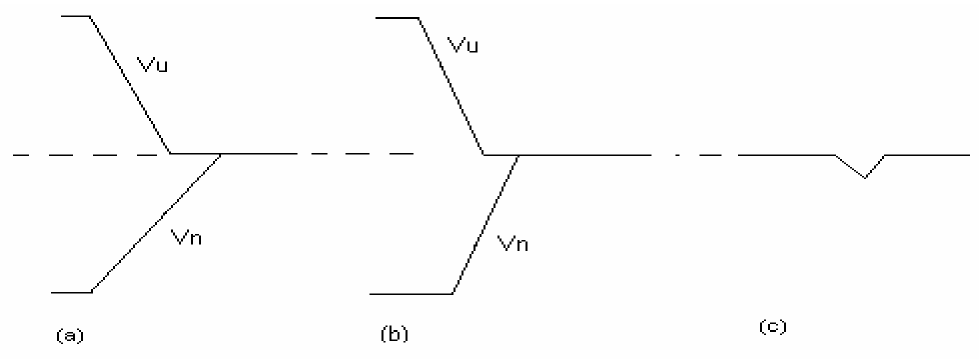


Fig 4.10. (a) P-MOS have faster slew rate (b) P-MOS switches earlier (c) arised fault.

The fault signal in figure 4.10c does occur when the upper output signal switches earlier or has a faster slew rate than the lower output. The fault will speed up the input signal to the N-MOS to minimize the fault.

4.4.1.2 Lower level faster than upper

If P-MOS switches after or have less slew rate than the N-MOS, it will be two different results from the result signal depending on if P-MOS is turning on or turning off.

4.4.1.2.1 When upper turns on

If P-MOS is slower than the N-MOS when it turns on, then the input to the MOSFET have to be speeded up, which is the same as the error-signal have to go below $V_{bat}/2$. The fault that will occur can be seen in figure 4.11.

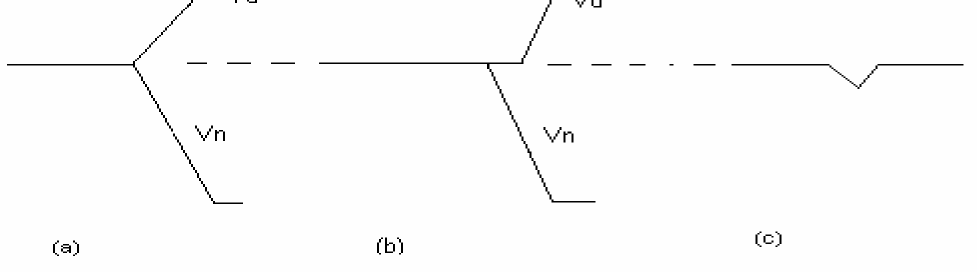


Fig 4.11. (a) P-MOS have slower slew rate (b) P-MOS switches later (c) arised fault.

In figure 4.11c it is shown how the fault signal will look if the upper output signal is switching after the lower or if it has a slower slew rate. The resulting discrepancy will slow down the input signal to the N-MOS.

4.4.1.2.2 When upper turns off

When the P-MOS is slower when it turns off compared to the N-MOS, then the input to the N-MOS have to be speeded up, to make sure it does that with help from the error-signal, the fault signal have to be higher than $V_{bat}/2$. The resulting error can be seen in figure 4.12.

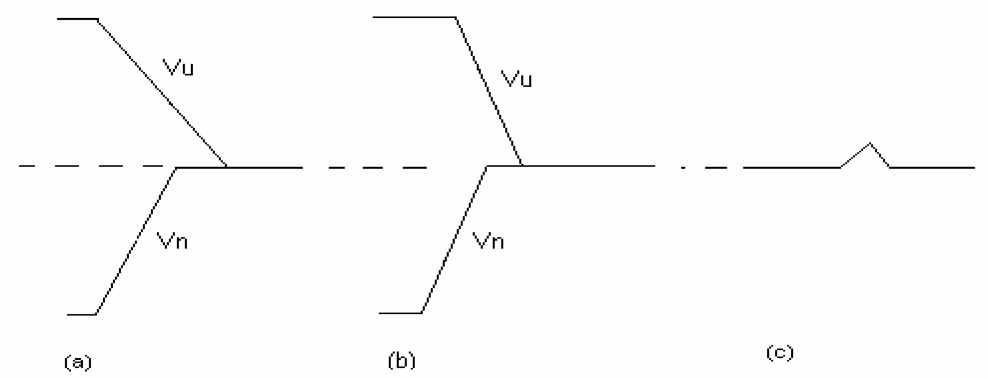


Fig 4.12. (a) P-MOS have slower slew rate (b) P-MOS switches later (c) arised fault.

The arised error in figure 4.12c is supposed to slow down the input signal to the N-MOS. The error occurs when the upper output signal has a slower slew rate than the lower or if it is switched later.

4.4.1.3 Function of error-signal

The error-signal is over $V_{bat}/2$ for two of the statements above and below $V_{bat}/2$ for the two others. Two states for the error-signal do manage to correct the four possible errors because of that one state corrects the N-MOS input for one fault per slope, if the error-signal is above $V_{bat}/2$ then it will speed up the N-MOS input signal at rising edge, and slow down if falling edge. When the error-signal is below $V_{bat}/2$ it will slow down the input signal at rising edge and speed up at falling edge.

The $V_{bat}/2$ in figure 4.8 is created with a voltage divider and a voltage follower, this is because a voltage follower have a low output resistance, able to keep it steady. The fault-signal is then added to the input signal of the N-MOS with another non-inverting summer. This will end up in a signal that have the right rise and fall time and are speeding up/slowing down the rise/fall time depending on the N-MOS, if it is following the P-MOS exactly or not. This configuration has the function of a P-regulator, a proportional regulator that has a signal that is proportional to the error-signal via an amplification factor. A large error will result in a larger control signal. Tests will be done to see if adding an I-regulator, D-regulator and ID-regulator will improve the result even more.

So the main task for the feedback is to amplify the error and add it to the input signal to minimize the error by regulation. A negative thing about only amplifying the error-signal is that if there is a large amplification, it is very easy for the system to start to oscillate. Because of this, there can also be a need of adding an I-regulator and also maybe a D-regulator.

4.4.2 Hardware configuration

In choosing operational amplifier, there are certain needs that have to be fulfilled. The design need to have operational amplifiers with rail to rail since the input need to get as low as possible to make sure that the MOSFET is turned off. The operational amplifier needs to have single supply because of battery operation between ground and approximately 12 volt, V_{bat}. There are not several amplifiers that have these two features, but national semiconductors have one, LM6144, that were chosen for this project.

In choosing the MOSFET there are some properties that are extra important. The MOSFET´s have to have similar characteristics so they work as similar as possible to each other to minimize the problem from the beginning. Because of the large currents that have to go through the load, it has to be a device that can manage at least 10 ampere. Looking through the alternatives the choice fell on IRF7307 from International Rectifier. A surface mount package with a dual N and P channel MOSFET that gives a device with two MOSFET´s that are complementary to each other. This power MOSFET can handle a pulsed drain current of 21A in N-channel and –17A in P-channel. This should be enough for the loads that this device is supposed to work for [10].

4.4.2.1 Adding fault signal to input signal

To be able to add up the fault signal that is created out of the circuit in figure 4.8, an equal circuit is used. A non-inverting summer with the fault signal added up with the ordinary input signal. In the configuration it is important to keep a gain of 1 to not amplify the signal that may lead to that the slew rate is changed of the input signal. Instead there is a possibility to change the scaling factor between R_{i1} and R_{i2}, to be able to decide how much the fault signal is going to affect the input signal.

4.4.2.2 P-regulator

For the P-regulator, the non-inverting summer in figure 4.8 have been used where R_i and R_f sets the gain of $A_0=1+R_f/R_i$. The two resistors Ri1 and Ri2 sets a scaling factor between the two input signals and these are picked to be equal, so the scaling factor between the input signals are 1:1. The output will be equated as:

$$V_{fault} = V_{PMOS}\left(\frac{R_{i2}}{R_{i1}+R_{i2}}\right)\left(1+\frac{R_f}{R_i}\right) + V_{NMOS}\left(\frac{R_{i1}}{R_{i1}+R_{i2}}\right)\left(1+\frac{R_f}{R_i}\right), \quad Eq.\ 4.8$$

4.4.2.3 PI-regulator

For the PI-regulator there are two solutions. One where the I-regulator have been built in to the non-inverting summer by placing a capacitor in series with the feedback resistor, R_f. And the other solution is a stand alone PI-regulator [2], where there is a need of two extra operational amplifiers, compared to the first solution. One inverting amplifier with a resistor and a capacitor in series at the feedback where the resistor sets the proportional gain and the capacitor sets the amplification for the integration. The second operational amplifier is to invert the signal so it is suitable for the summing amplifier. The two solutions can be viewed in figure 4.13.

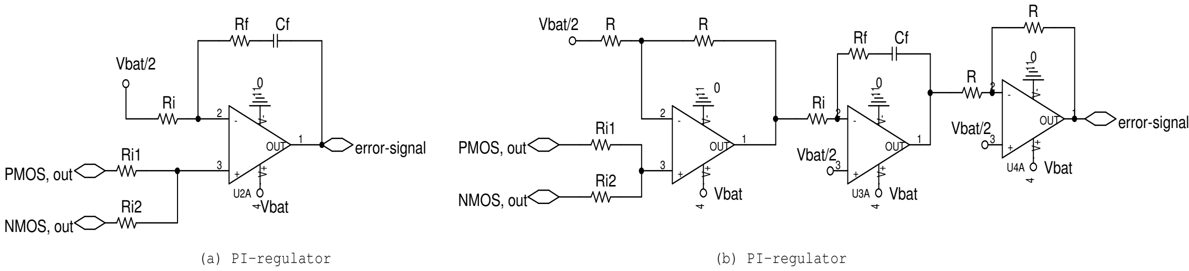


Fig 4.13. Two different circuits where both is acting as a PI-regulator.

The first regulator has an output of:

$$Z_{out} = R_f + \frac{1}{sC_f}, \quad Eq.\ 4.9$$

$$\frac{1}{Z_{in}} = \frac{1}{R_i}, \quad Eq.\ 4.10$$

$$\frac{Z_{out}}{Z_{in}} = \frac{R_f + \frac{1}{sC_f}}{R_i}, \quad Eq.\ 4.11$$

$$A_0 = 1 + \frac{Z_{out}}{Z_{in}} = 1 + \frac{R_f}{R_i} + \frac{1}{sR_iC_f}, \quad Eq.\ 4.12$$

$$V_{fault} = V_{PMOS}\left(\frac{R_{i2}}{R_{i1}+R_{i2}}\right)\left(1 + \frac{R_f}{R_i} + \frac{1}{sR_iC_f}\right) + V_{NMOS}\left(\frac{R_{i1}}{R_{i1}+R_{i2}}\right)\left(1 + \frac{R_f}{R_i} + \frac{1}{sR_iC_f}\right), \quad Eq.\ 4.13$$

This gives:

$$K_p = 1 + \frac{R_f}{R_i}, \quad Eq.\ 4.14$$

$$K_i = \frac{1}{R_iC_f}, \quad Eq.\ 4.15$$

And the second is [2]:

$$A_0 = \left(1 + \frac{R}{R}\right)\left(-R_f - \frac{\frac{1}{R_iC_f}}{s}\right)\left(-\frac{R}{R}\right) = 2\left(\frac{R_f}{R_i} + \frac{\frac{1}{R_iC_f}}{s}\right) = \frac{2R_f}{R_i} + \frac{2}{sR_iC_f}, \quad Eq.\ 4.16$$

$$V_{fault} = V_{PMOS}\left(\frac{R_{i2}}{R_{i1}+R_{i2}}\right)\left(\frac{2R_f}{R_i} + \frac{2}{sR_iC_f}\right) + V_{NMOS}\left(\frac{R_{i1}}{R_{i1}+R_{i2}}\right)\left(\frac{2R_f}{R_i} + \frac{2}{sR_iC_f}\right), \quad Eq.\ 4.17$$

This gives:

$$K_p = \frac{2R_f}{R_i}, \quad Eq.\ 4.18$$

$$K_I = \frac{2}{R_i C_f}, \quad Eq.\ 4.19$$

Which shows that both circuits will act as a PI-regulator since the equation for a PI-regulator is:

$$F_{PI}(s) = K_p + \frac{K_i}{s}, \quad Eq.\ 4.20$$

The benefit for the first solution is that it does not need any extra operational amplifiers and that there will be less time delay for the signal since it does not have to pass as many states as in the second solution.

4.4.2.4 PD-regulator

One feature of a PD-regulator is that it can be used to increase the stability of the feedback of a system. The derivative D is introduced to increase the speed of the feedback. When increasing the proportional gain, the speed will be increased but at the same time the damping and the stability are reduced. The deterioration is counteracted by the derivative. By combining the P and D, the speed can be increased without getting an unstable feedback. Negative for this regulator is that the increased speed will increase the gain of high frequencies [2].

Two PD-regulators have been designed to see if both do act as a PD-regulator. The first regulator is built up on a non-inverting summer where a parallel circuit is added up to R_i. The parallel circuit consists of one resistor and one capacitor. The second solution [2] is built up on three operational amplifiers where there is one feature per amplifier instead of having all in one. The two circuits are presented in figure 4.14.

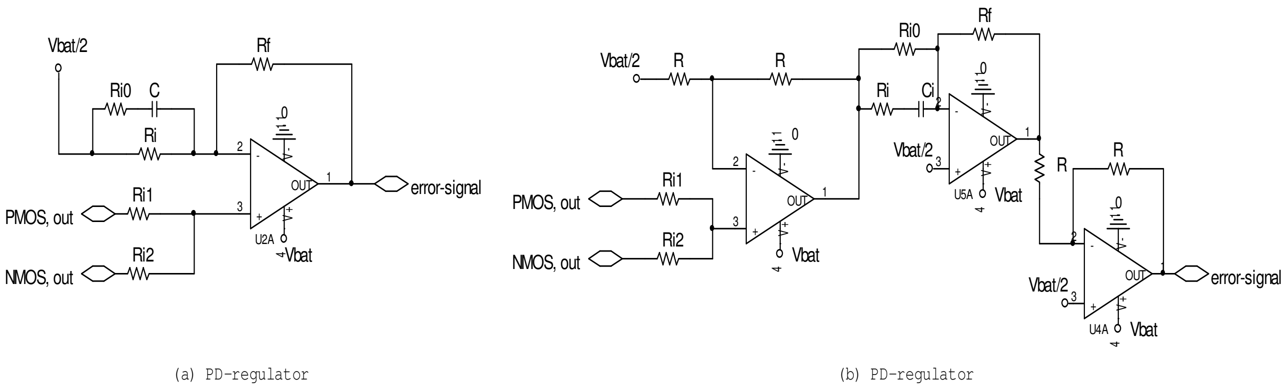


Fig 4.14. Two different configurations of a PD-regulator.

The amplification of the first circuit is equated as:

$$\frac{1}{Z_{in}} = \frac{1}{R_i} + \frac{1}{R_{i0} + \frac{1}{sC}} = \frac{1}{R_i} + \frac{sC}{sR_{i0}C + 1}, \quad Eq.\ 4.21$$

$$\frac{Z_{out}}{Z_{in}} = \frac{R_f}{R_i} + \frac{sR_f C}{sR_{i0}C + 1}, \quad Eq.\ 4.22$$

$$A_0 = 1 + \frac{Z_{out}}{Z_{in}} = 1 + \frac{R_f}{R_i} + \frac{sR_f C}{sR_{i0}C + 1}, \quad Eq.\ 4.23$$

This gives:

$$K_p = 1 + \frac{R_f}{R_i}, \quad Eq.\ 4.24$$

$$K_d = R_f C, \quad Eq.\ 4.25$$

$$T_f = R_{i0} C, \quad Eq.\ 4.26$$

The second PD-regulator is formulated as [2]:

$$\frac{Z_{out}}{Z_{in}} = (1 + \frac{R}{R})(\frac{R_f}{R_i} + \frac{sR_f C}{1 + sR_{i0}C} = \frac{2R_f}{R_i} + \frac{2sR_f C}{1 + sR_{i0}C}, \quad Eq.\ 4.27$$

This gives:

$$K_p = \frac{2R_f}{R_i}, \quad Eq.\ 4.28$$

$$K_d = 2R_f C, \quad Eq.\ 4.29$$

$$T_f = R_{i0} C, \quad Eq.\ 4.30$$

And a PD-regulator is formulated as follows:

$$F_{PD}(s) = K_p + \frac{sK_d}{1 + sT_f}, \quad Eq.\ 4.31$$

This gives:

$$K_p = 1 + \frac{R_f}{R_i}, \quad Eq.\ 4.32$$

$$K_d = R_f C, \quad Eq.\ 4.33$$

$$T_f = RC, \quad Eq.\ 4.34$$

With these equations it is possible to dimension the regulator, and when comparing the two circuit's solutions, both should act as a PD-regulator.

The same benefits are found here as for the PI-regulator.

4.4.2.5 PID-regulator

One way of solving a PID-regulator is to use an operational amplifier with a derivative in parallel with the PI-regulator, figure 4.15b. When designing the PID-regulator, the aim was to rebuild the PI-regulator so there still only is one operational amplifier for the regulator. This was done by adding a capacitor and a resistor to be in parallel with the input resistor for the PI-regulator, figure 4.15a. This configuration will be compared with a PID-regulator [2] that uses three operational amplifiers to see if it works correctly. The differences in output are due to that the first PID-regulator has a gain that is A+1 and the second have a gain of A. For the proportional gain this is not a problem but the integral gain will be higher for the first circuit if equal values are chosen. The proportional gain is equal since there is a non-inverting summer that has the gain of A+1 at the second PID-regulator.

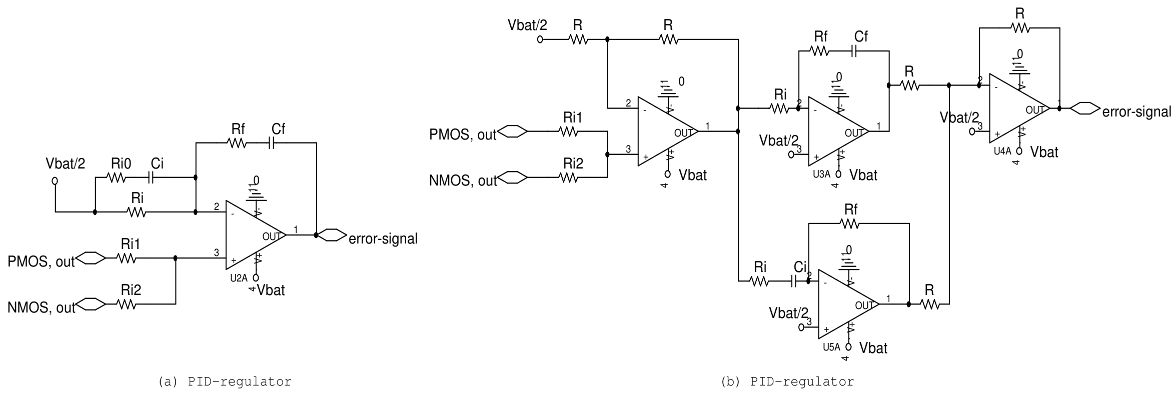


Fig 4.15. Two configurations of PID-regulators

The output from the first PID is equated as:

$$\frac{1}{Z_{in}} = \frac{1}{R_i} + \frac{1}{R_{i0} + \frac{1}{sC_i}} = \frac{1}{R_i} + \frac{sC_i}{sR_{i0}C_i + 1}, \quad Eq.\ 4.35$$

$$Z_{out} = R_f + \frac{1}{sC_f}, \quad Eq.\ 4.36$$

$$\frac{Z_{out}}{Z_{in}} = \frac{R_f + \frac{1}{sC_f}}{\frac{1}{R_i} + \frac{sC_i}{sR_{i0}C_i + 1}} = \frac{1 + s(C_i(R+R_i) + C_f R_f) + s^2 R_f C_f C_i (R + R_i)}{sR_i C_f (sRC_i + 1)}, \quad Eq.\ 4.37$$

Where:

$$A_0 = 1 + \frac{Z_{out}}{Z_{in}} = \frac{1 + s(C_i(R+R_i) + C_f(R_f + R_i)) + s^2 C_f C_i (R_f R + R_i R + R_f R_i)}{sR_i C_f (sRC_i + 1)}, \quad Eq.\ 4.38$$

And a PID-regulator is equated as:

$$F_{PID}(s) = \frac{K_p}{T_i} \cdot \frac{1 + s(T_i + T_f) + s^2 T_i (T_d + T_f)}{s(1 + sT_f)}, \quad Eq.\ 4.39$$

Output from the second [2]:

$$A_0 = \frac{Z_{out}}{Z_{in}} = (1 + \frac{R}{R})(\frac{R_f}{R_i} + \frac{\frac{1}{R_i C_f}}{s} + \frac{sR_f C_i}{1 + sRC_i}), \quad Eq.\ 4.40$$

As can be found from the equations above, the first PID-design is supposed to work as a PID-regulator if comparing the equations, despite it has some differences in the constants.

4.4.2.6 P-regulator with LP-filter

The last choice of feedback is to use a P-regulator with a low pass filter placed before it is added to the input signal. The low-pass filter will then cancel high frequency oscillations when having too high gain, this is to see if the output error reduces when canceling out the oscillation created by the amplification. Figure 4.16 shows the circuit for this configuration, which is a plain non-inverting summer with a low pass filter connected at the output of the operational amplifier.

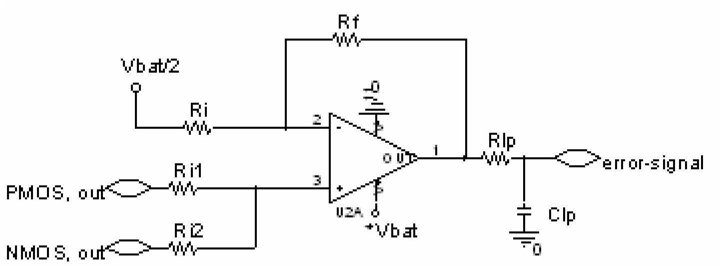


Fig 4.16. Circuit for P-regulator with added LP-filter.

The aim of this circuit is to see if it is possible to cancel out oscillation if there is an over steering at only one of the slopes.

5 Simulation

The design has been put into OrCad Capture, where the different solutions have been simulated with the program Spice core. The circuit has been simulated as a complete circuit and also parts of the circuit have been simulated. Simulation of regulators have been performed to see that the function is correct, the circuit have been simulated with and without feedback to see what configuration that gives best result.

5.1 Simulation of parts of total circuit

The total circuit has a couple of features that have been simulated stand alone from the total circuit. The results are shown below.

5.1.1 Simulation of diode configuration without feedback

The aim of the test is to see that the diode configuration does work as it is intended. It is done with a configuration of the total circuit from appendix 2 but without any feedback. By having the gate resistors to the P-MOS constant and then change the gate resistors to the N-MOS would then show that the time constant of the MOSFET is changed. But after testing it, it showed that when changing the turn on time constant for the N-MOS, it affected the total result by changing the level where the two outputs are met. If lowering the N-MOS turn on time constant then the P-MOS output would have time to go below Vbat/2, if increasing turn on time the P-MOS output would not have time to go below Vbat/2. This means that there is a need of changing the P-MOS turn off time constant when changing the N-MOS turn on time constant. This is not the case when changing the N-MOS turn off time constant. In figure 5.1 the result of just changing the N-MOS can be viewed.

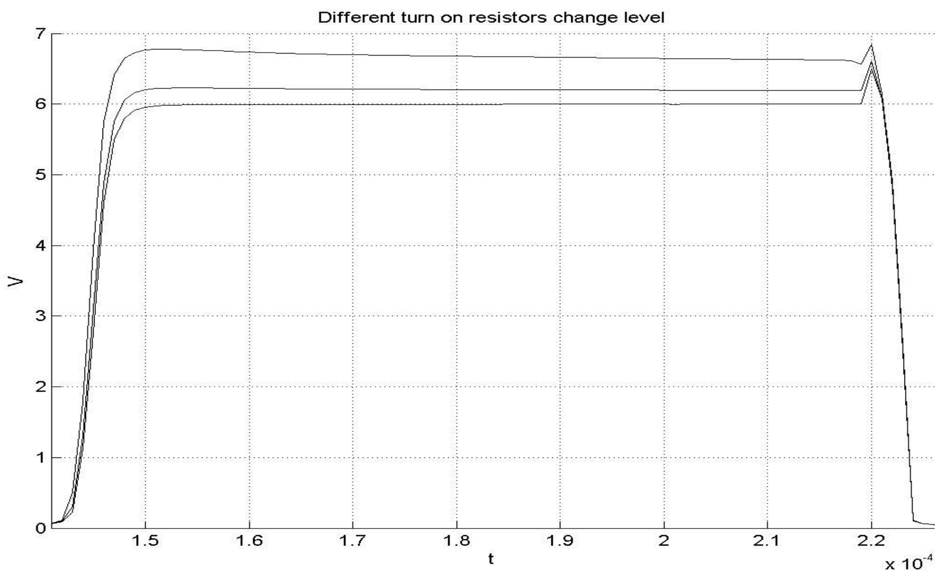


Fig 5.1. When changing the turn on resistor for N-MOS, the amplitude changes. Small resistances give fast rise/fall time and higher amplitude.

The result shows that there is a change in time constant when changing the gate resistance but it is not good to have two outputs that meet at different values. This behavior was found that when not using any feedback, there is not a stable level where the two outputs are met. The next aim of the test is to see if it is possible to change the N-MOS turn on time constant to a desired value and then by changing the P-MOS gate resistance to make the result end up at the right level. The result can be seen in figure 5.2.

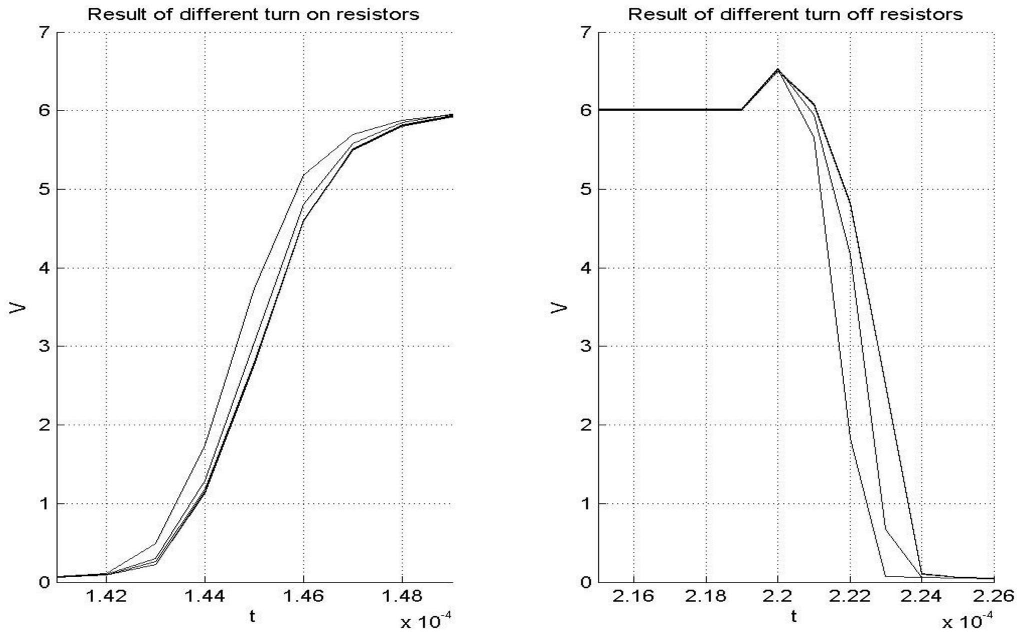


Fig 5.2. Result of different gate resistances, fast rise/fall time for big gate resistance and slow rise/fall time if small gate resistance.

The result shows that the slope can be changed by changing gate resistances and that a desired slope can be tuned in so that the level ends up at Vbat/2. The result of changing the gate resistances is that it is possible to speed up or slow down the rise/fall time. In figure 5.2 it is shown that when a large resistor is used, the rise/fall time is slower and the opposite occurs if a small resistor is used. The curve does start at the same point and does end at the same point when rising, when falling the start point is the same and depending on speed it will end at different times.

5.1.2 Simulation of diode configuration with feedback

Out of the output result from the MOSFET´s, the gate resistances were set so the two MOSFET´s switch as equal as possible. In figure 5.3 there is a simulation showing three different cases. In the first the gate resistance of the N-MOS is chosen too small, showing that the upper curve goes much slower than the lower causing a big fault if summing the two signals together. In the second, the gate resistances have been matched to give an output that keeps rise and fall times equal for the P-MOS and the N-MOS. In the third, the gate resistances have been chosen too large and which causes the P-MOS to switch much faster than the N-MOS. From the results of the simulation, there seems to be a possibility to optimize the values of the gate resistances to get a result of equal time constants for the two MOSFET´s.

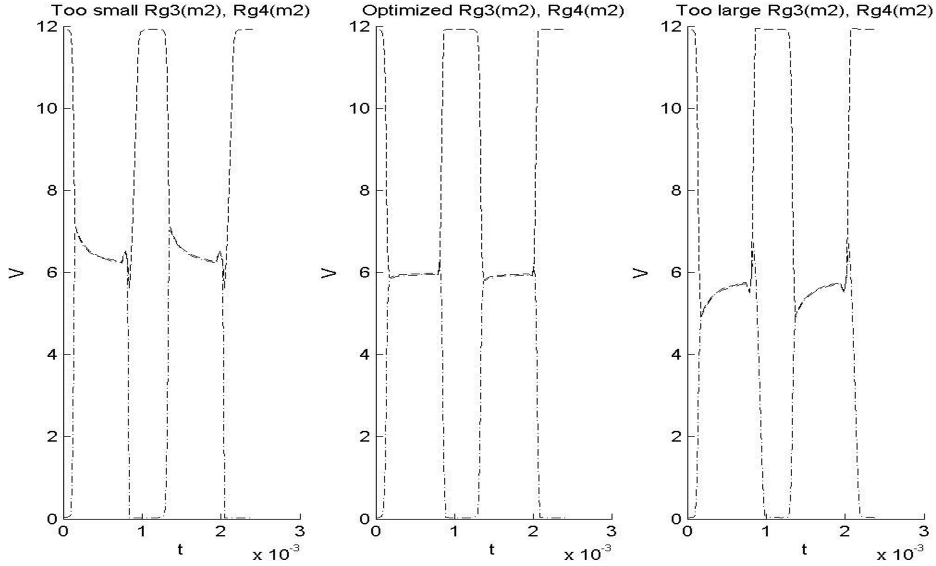


Fig 5.3. Differences when changing gate resistances

As can be seen in figure 5.3 there have been a severe decrease of the error by tuning the gate resistances. By simulations, there seems not to be a zero level for the fault but by tuning it as good as possible there have been results at approximately ±0.5V. Figure 5.4 shows the sum of outputs from figure 5.3.

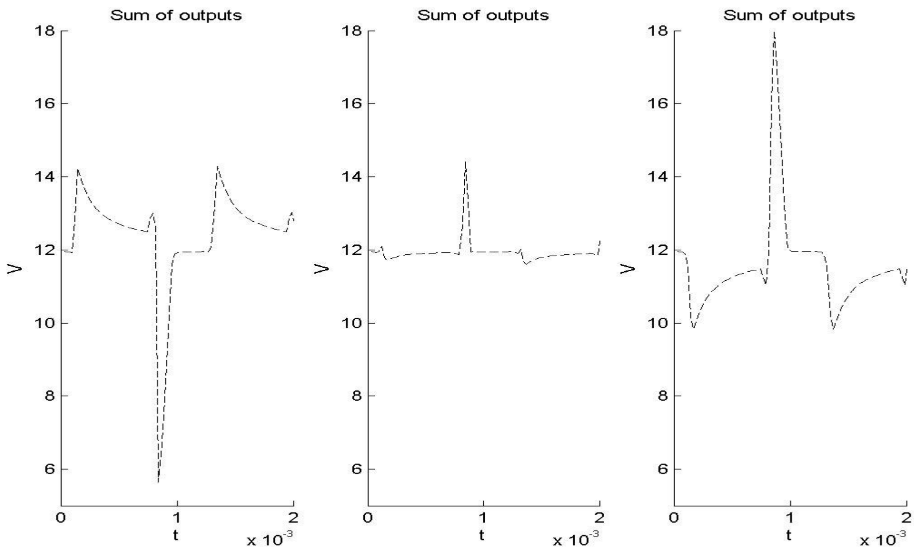


Fig 5.4. Sum of outputs when simulating with different gate resistances

The result in figure 5.4 shows that by only using the diode configuration, the fault between the two outputs signals can be eliminated pretty good.

5.1.3 Simulation of added gate drain capacitance without feedback

When simulating the effect of adding an external capacitance in parallel with the MOSFET´s internal capacitances, the desired result was to have the two outputs more equal to each other than if not using an external capacitance. The simulation was performed with the diode configuration optimized and the first test was done with equally sized capacitances at both MOSFET´s. The result showed that the capacitance change the level for the input where the MOSFET goes in to its active region. This is not a wanted feature since if the input signal almost is at its top or bottom value then it will be harder to regulate the fault. Figure 5.5 shows the difference between input and output signal when there is an external capacitance and when it is not.

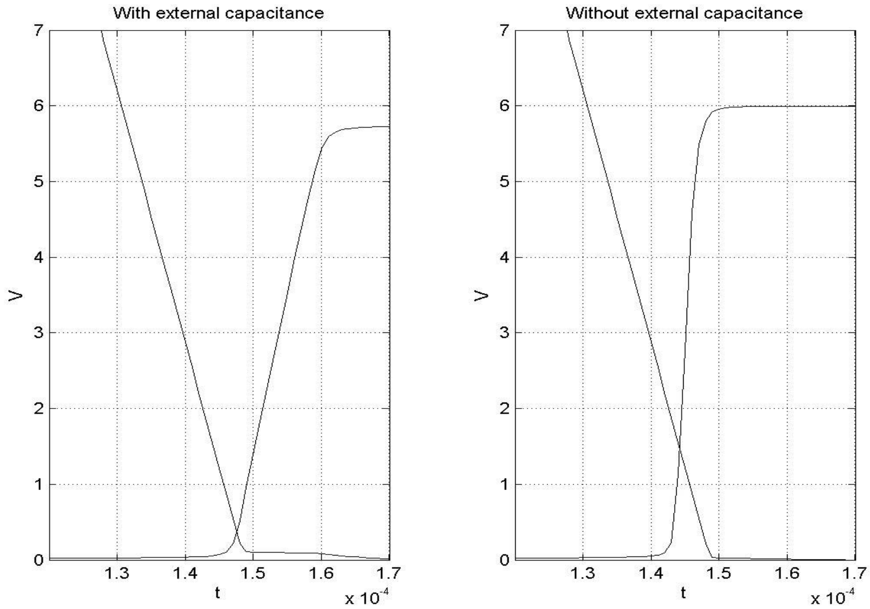


Fig 5.5. Showing differences of added capacitance. Falling edge is input, rising is output.

In figure 5.5 it can be seen that when using an external capacitance, the output goes into its active region when the input is at approximately 1 volt, which means that there is 1 volt left to adjust for faults between the P-MOS and the N-MOS. It can also be seen that the output have only reached 1 volt when the input is at approximately zero leading to that the output can not be regulated in the rest of the interval. The idea of that the time constant should be changed does correspond to what was investigated earlier in the report. In figure 5.5 it can be seen that there is a big difference in rise time if comparing with and without an external capacitance.

5.1.4 Simulation of snubber circuit without feedback

There have been done a simulation series on the circuit to test how the snubber acts. Four different cases with different values of the resistor and of the capacitor. The result fell out as in the case when the resistor is small, there is a small overshoot on the N-MOS when it turns off. This is because of that the P-MOS is a bit slower in its turn on moment. If the capacitor is changed, it will steer the differences on the other slope. When a large capacitor is used the N-MOS will be slower when it is turned on and the P-MOS will be slower when it is turned off.

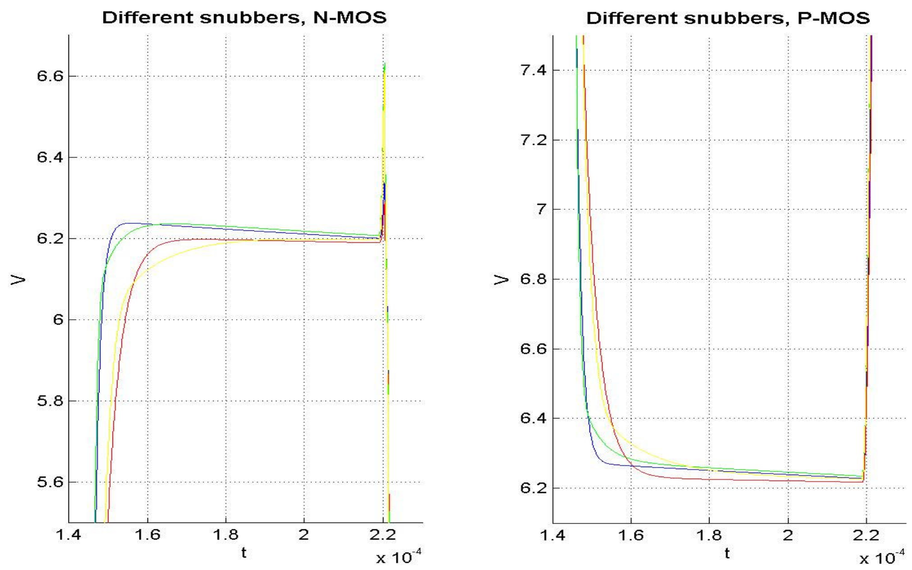


Fig 5.6. Different values on snubber components.

In figure 5.6 the result of different snubber components can be viewed. Blue line shows when there is a small resistor and a small capacitor that leads to that it is fast on one slope and has a small overshoot on the other. The red line shows when the resistor is kept small and the capacitor is enlarged. Then there is a slow rise time for the N-MOS and a small overshoot when turning off. Green line is for a large resistor and a small capacitor, the result shows one fast slope and one slope with a substantial overshoot for the N-MOS, this is because of that the P-MOS is turning on earlier. Finally the yellow line is when both the resistor and capacitor is large. Then there is a slow rise time for the N-MOS and a substantial overshoot when turning it off.

5.2 Simulation of different regulators

When simulating to see if the different regulators are working as they are intended to do, the outputs were simply compared when having same inputs for the different regulators.

5.2.1 Test of PI-regulators

When testing the PI-regulators, there was two inputs where one is switching between 6 – 12 volt and one that have a slight time shift between 0 – 6 volt. The result can be observed in figure 5.7.

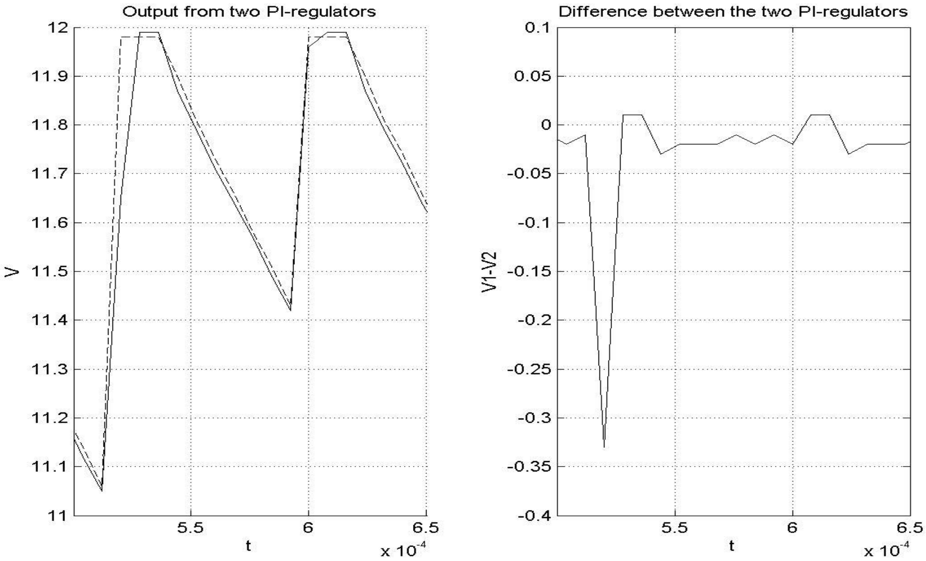


Fig 5.7. Differences of the two PI-regulators. Full line is PI-regulator based upon one OP, and dashed line is the second PI-regulator.

It can be seen that the solid line, first PI-regulator, are slight different from the dashed line, second PI-regulator, and in the figure to the right the difference have been printed which shows that there is a very small difference between them. Because of the small differences between the two circuits simulation results, the first PI-regulator is used in the design to save components.

5.2.2 Test of PD-regulator

The two PD-regulators from figure 4.14 were tested in the same way as for the PI-regulators.

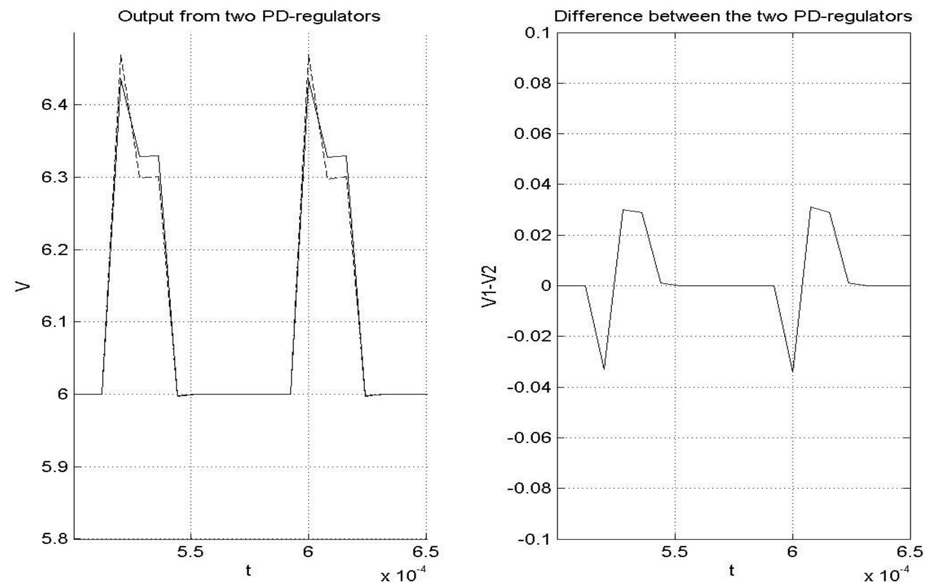


Fig 5.8. Result from testing the two PD-regulator designs. Full line is the first PD-regulator and dashed line is the second.

In figure 5.8 the result of the two PD-regulators can be seen. The solid line is for the first regulator and the dashed line for the second. In the figure to the right the difference between the two is shown which shows that the two PD-regulators does work very similar, why the first design will be used to save the number of components that is needed for the design.

5.2.3 Test of PID-regulators

The two configurations of PID-regulators from figure 4.15 were used and same test as for the PI-regulators were used, with same input signal. Results show that there is a slight difference between the two signals. The first solution is not as fast as the second but there are so small differences that the first will be chosen because it only needs one operational amplifier.

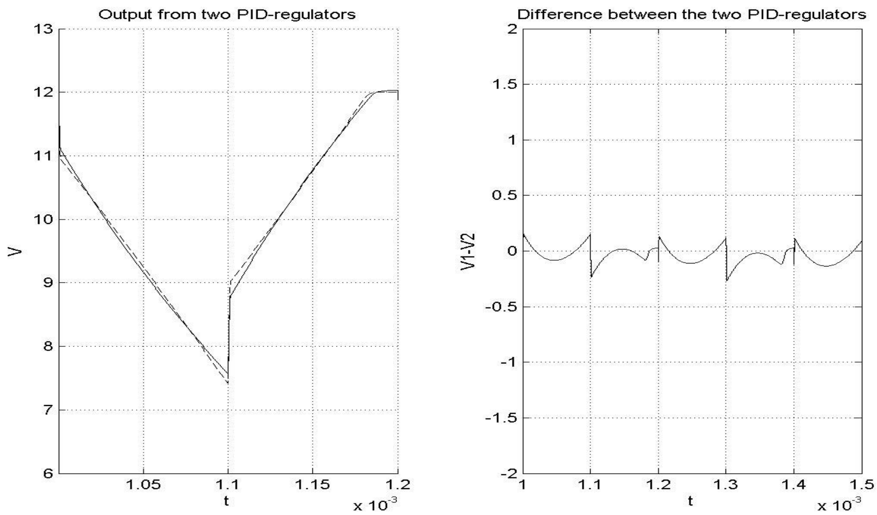


Fig 5.9. Differences between the two PID-regulators. Solid line is the first circuit and dashed line is the second. In figure to the right the difference between the two results can be seen.

Figure 5.9 show that the two PID-regulators give almost the same result, where the solid line is for the first PID-regulator and the second PID-regulator is the dashed line. The differences that can be seen are that the second one has a larger amplification.

5.3 Simulation of feedback

To simulate the behavior of a feedback, the diode-configuration has been used to get a most accurate simulation as possible. There have been a couple of different feedbacks to test to find the most suitable design as possible. The result of the feedback is input signal added with fault signal, where input signal are running between 0 and V_{bat} with a rise/fall time at 1/RC us. Fault signal are at its best $V_{bat}/2$ and the worse the fault gets, it will get closer to 0 or V_{bat}.

5.3.1 Simulation with pure P-regulator

With a pure P-regulator there is only one variable to adjust to see how the circuit will react on the feedback. That is the amplification of the fault signal. This type of feedback is good in the matter of that there will not be a major time delay of the fault signal. The fault signal will pass through one operational amplifier before added to the input signal. Negative is that it is easy to set too high amplification that will cause oscillations. The result shows that when the two outputs are switching towards each other there is a large improvement when increasing the amplification, though with to high amplification the system will start to oscillate. A suitable gain for this one seems to be between two and three. When switching in the reverse direction we have a pretty good result but the upper output is going slight too fast. The P-regulator makes the slave go faster and the bigger the amplification is the better the result gets, but the same here is that too much amplification will create an oscillation. The results can be seen in figure 5.10.

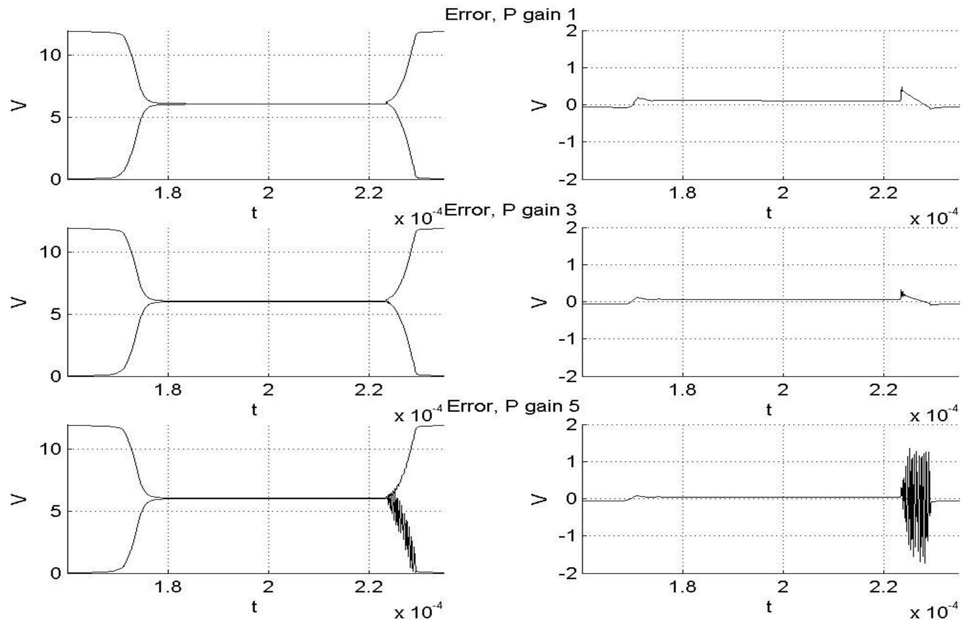


Fig 5.10. Simulation of total circuit with P-regulator.

The simulation results in figure 5.10 shows a great improvement when increasing the gain for one of the slopes. Though the other slope starts to oscillate when having too high amplification, why one has to be careful when setting the gain.

5.3.2 Simulation with PI-regulator

For PI-regulators there are some issues to think about when configuring it. If the integral amplification is too high there will be problems with instability. The same thing happens when the proportional amplification is too low, which gives too high I-regulation which leads to reduced stability. In figure 5.11 three different results can be seen from the regulation with the first PI-regulator. When comparing with the P-regulator, it can be seen that a PI-regulator would improve the total result of the circuit.

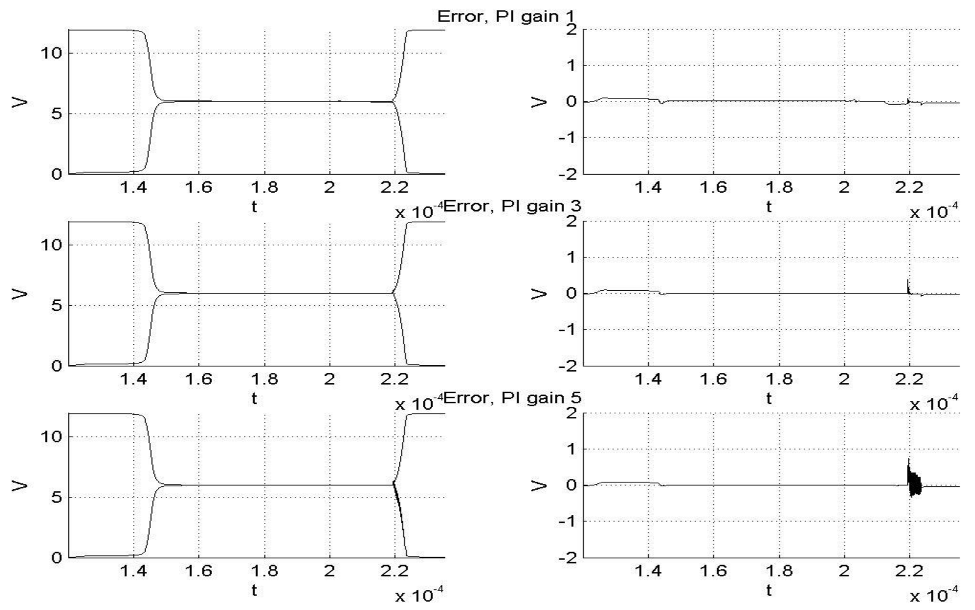


Fig 5.11. Result of switching with different gain with PI-regulator.

The result shows that when the two signals are leaving each other it is preferable with a low gain, or else the regulator will make the signal oscillate. For the case when the two signals are switching towards each other, the results are pretty much the same but there is a slight improvement when having a larger gain.

When changing the integrator of the regulator, the result shows that it is important to choose a correct capacitor, if too small capacitor it will start to oscillate and if too big the capacitor will charge up and give a rise in the resulting signal before it is switching. Result can be seen in figure 5.12 where the gain is set to three and then there are three different cases with different capacitors.

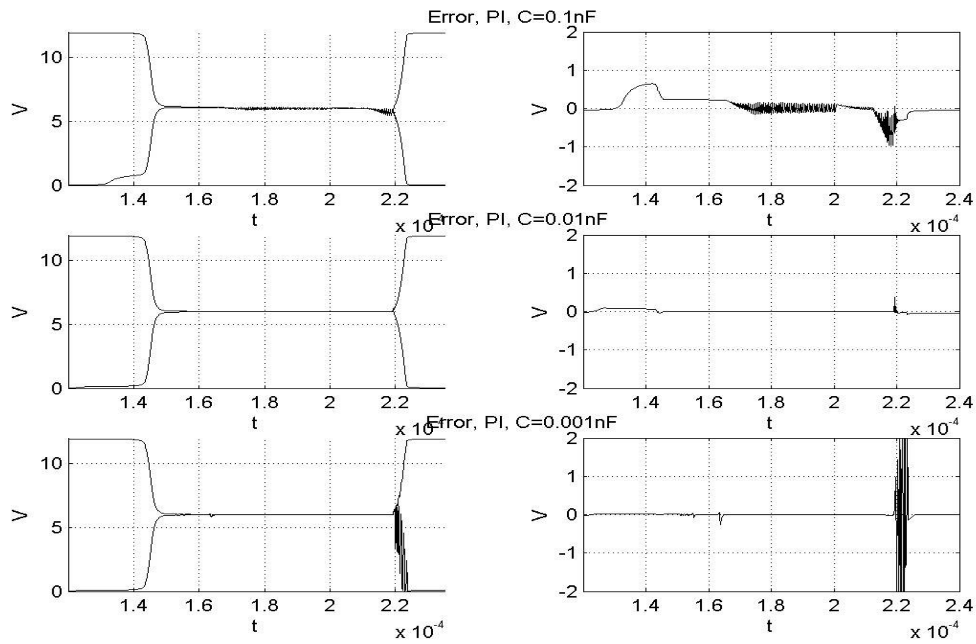


Fig 5.12. PI-regulator with three different capacitor values.

The result in figure 5.12 shows that the value of the capacitor is changing the sum of the outputs pretty much. If the capacitor size is decreased, there can be a cancellation of the error at one of the slopes, but at the other one there will be a lot of oscillations. This shows that it is important to choose the correct value of the capacitor, since there have to be a result that is as good as possible for both slopes.

5.3.3 Simulation with PD-regulator

There have been two simulations done on circuit with PD-regulator in the feedback. One simulation when adjusting the amplification and one when changing the capacitance for the derivative of the regulator.

When increasing the amplification, there is a decrease of the fault between the two output signals. But if increasing the amplification too much then the system will be unstable and start to oscillate.

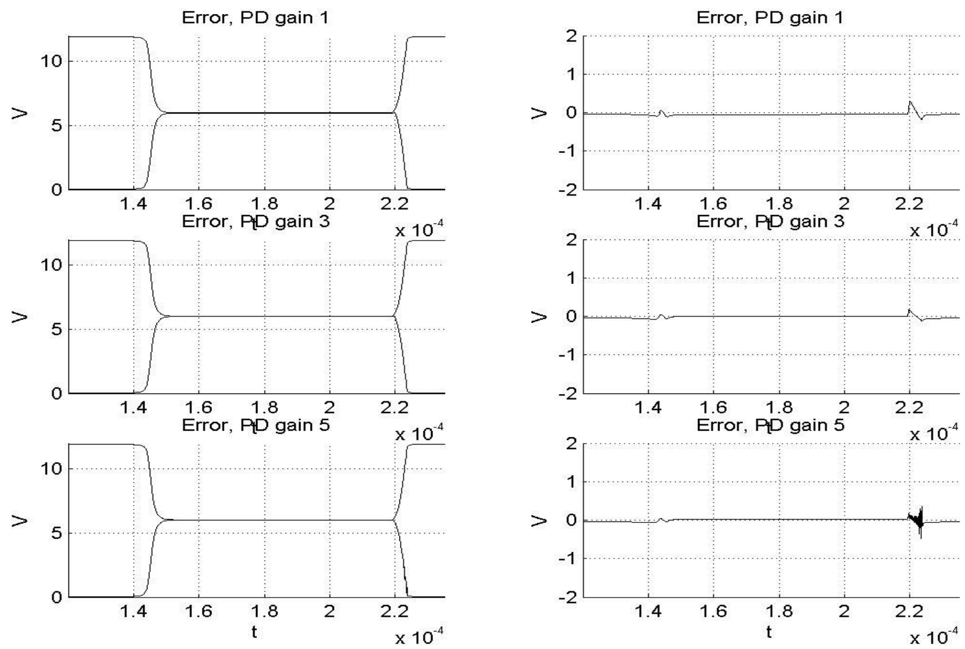


Fig 5.13. Simulation of PD-regulator with different R_f.

As can be seen in figure 5.13, the sum of the two outputs decreases when increasing the gain, but when the gain is too high there will be an oscillation.

For the second simulation the gain is set to three and then the capacitance is changed to show how the output is changed. The result is shown in figure 5.14 for three different capacitances. If using a large capacitance, the sum of the outputs does decrease but a slight oscillation will appear. When the capacitance is decreased there is a very small change in the sum of the outputs.

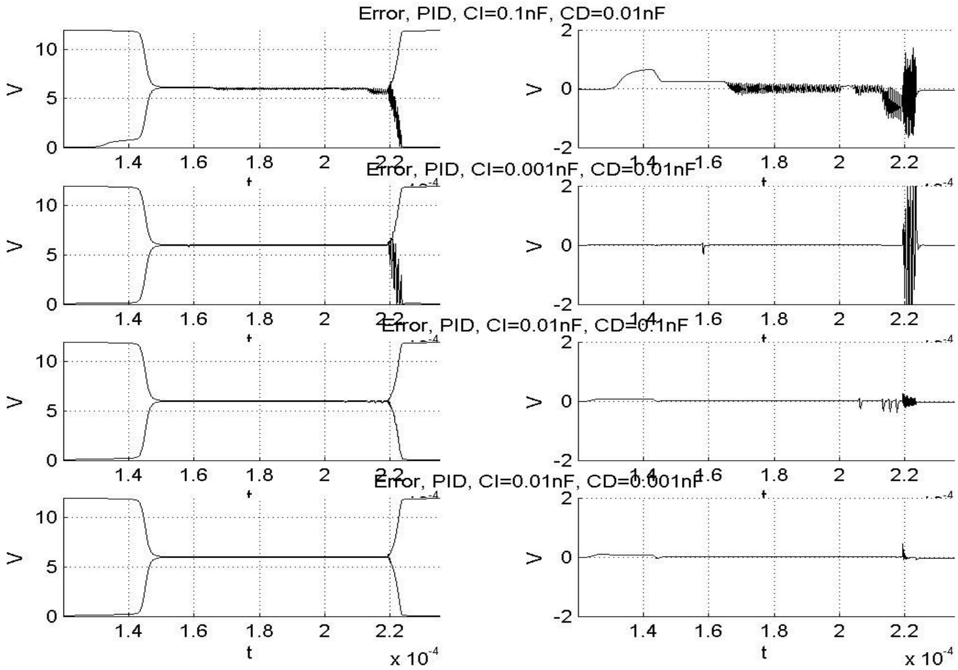


Fig 5.14. PD-regulator, simulation of different capacitor values.

In figure 5.14 it can be seen that when keeping the gain constant and changing the capacitor value there is almost no change at all. It can be seen that some small oscillations are decreased but despite that it is almost the same result.

5.3.4 Simulation with PID-regulator

The simulation was done by only changing the feedback resistor for the regulator. The result that is wanted is that by only changing one component, it is possible to control the regulator.

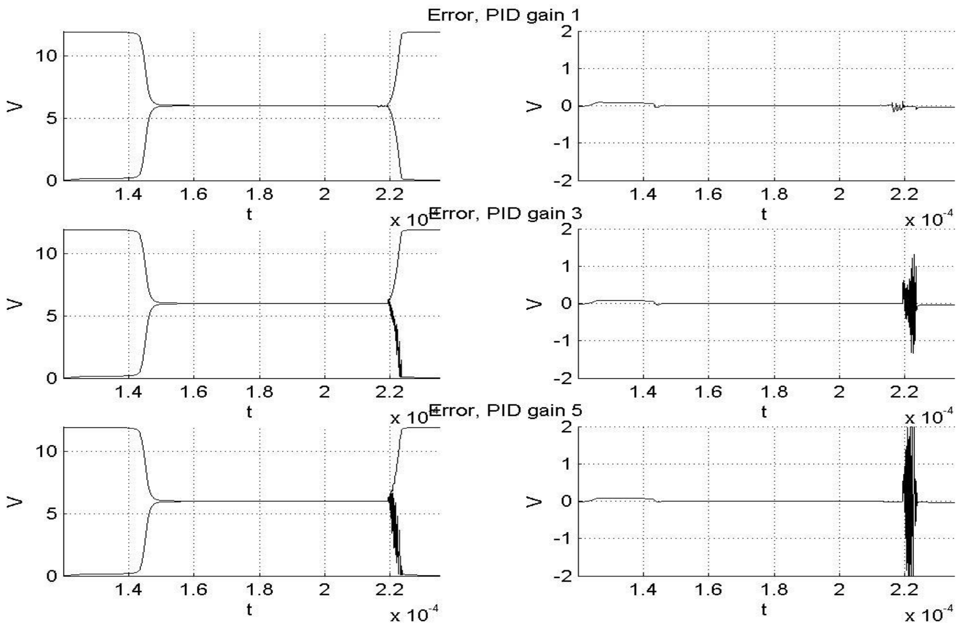


Fig 5.15. Result when simulating circuit with a PID-regulator.

It can be seen in figure 5.15 that when the gain of the regulator is increased, one slope is almost unchanged while the other slope starts to oscillate due to over steering when having quite a small gain. Using this result it is found that it is not enough to only change the gain to get an acceptable regulation since one slope is not changed at all, while there is a big difference on the other. In order to investigate this further a simulation was performed with the gain kept constant at three, and by changing the capacitors in order to see which slope that is changing.

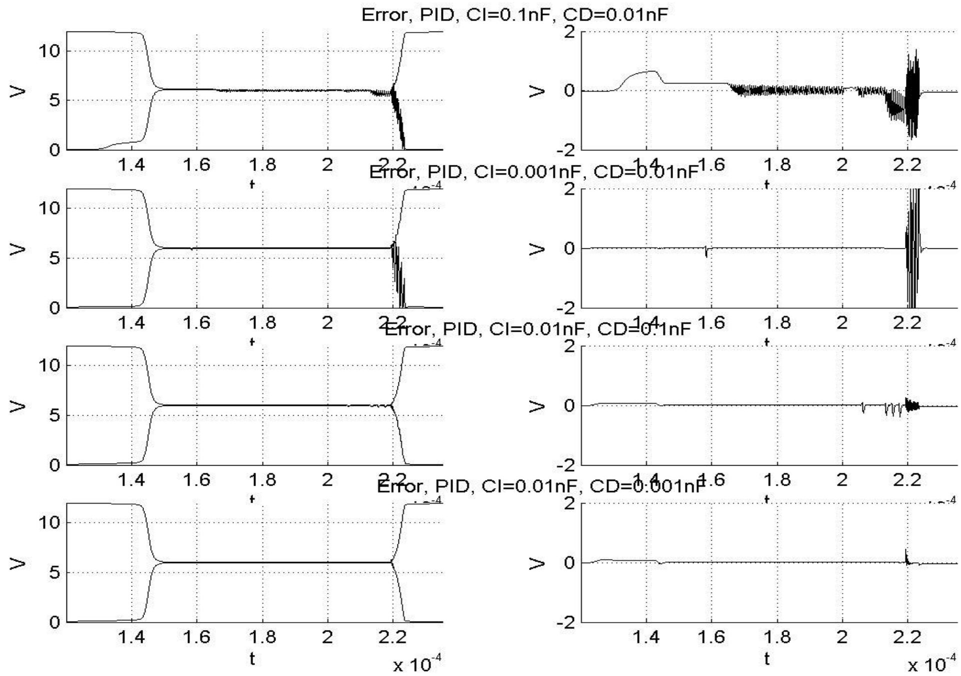


Fig 5.16. Circuit with PID regulator when C_I and C_D are changed.

Figure 5.16 shows that when the integrating part of the regulator is changed, there are a lot of oscillations, despite from that when changing the capacitor of the derivating part. At one slope there is a very good result when the capacitor for the integrating part is decreased but at the other slope there are a lot of oscillations. For the derivating capacitor there is no change at one of the slopes but a big difference at the other.

The conclusion of this is that the integrating part regulates one slope better than the other and the same thing is for the derivating part.

5.3.5 Simulation with P-regulator plus low pass filter

As could be seen in section 5.3.1 where there was only a P-regulator in the feedback, the sum of the outputs showed that when using a high gain it started to oscillate. This is a test based on the regulator circuit in figure 4.16 to see if filtering out the high frequencies of the sum of the outputs will make better result since the feedback will not add up the oscillations to the input signal of the N-MOS input.

The frequency that the oscillation is at when the P-regulator has a gain of 5 is at approximately 2.4 MHz. So the low pass filters that will be tested are for frequencies below that.

The resistor for the low pass filter is set to 10 kOhm which leads to that R_{i2} of the non inverting summer have to be set to 20 kOhm so there is a factor of 1:1 between the two input resistors. The capacitance for the filter is:

$$C = \frac{1}{R \cdot f}, \quad Eq.\ 5.1$$

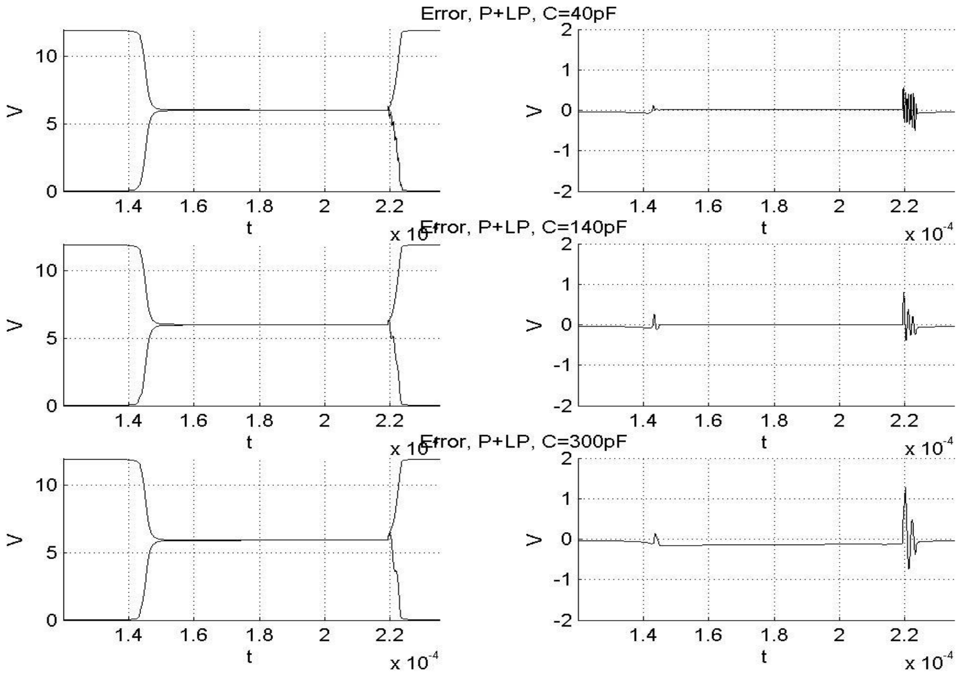


Fig 5.17. Simulation of different low pass filters in feedback.

In figure 5.17 there have been a test of three different low pass filters when the gain is set to a factor of five. As can be seen when lowering the cut off frequency of the filter, the frequency of oscillation is decreasing. The amplitude is though slight increased when the cut off frequency is lowered. This solution can be a good complement if knowing that there are disturbances at a special frequency. It is not possible to cancel out the oscillation, but it is possible to move it in the frequency spectrum if knowing that it is disturbing at a certain frequency.

5.3.6 Conclusion of the different feedbacks

The different feedbacks that have been tested seem to give a result that is almost equal to each other. When the system is stable there is a fault between the two outputs of approximately ±0.3 volts. If the sum has an oscillation, the oscillation occurs at approximately 2.5 MHz and as can be seen in the simulation results, when there is an oscillation, the other slope is better configured.

5.3.7 FFT for different feedbacks

Since the results from the transient analysis were not that different from each other, there is only presented two FFT's, where one is for a steady output and one is when there is an oscillation in the sum of the two outputs.

When looking for radiated disturbances, the frequencies according to the standard are from 150 kHz and up to 2GHz. For the band between 150 kHz – 25 MHz, there is a maximum limit of 30 dBμV/m and for the band 25 MHz – 200 MHz there is a maximum limit of 10 dBμV/m. These limits are put into the figure 5.18, to see so the calculated FFT of simulated circuit is below the range of maximum limits.

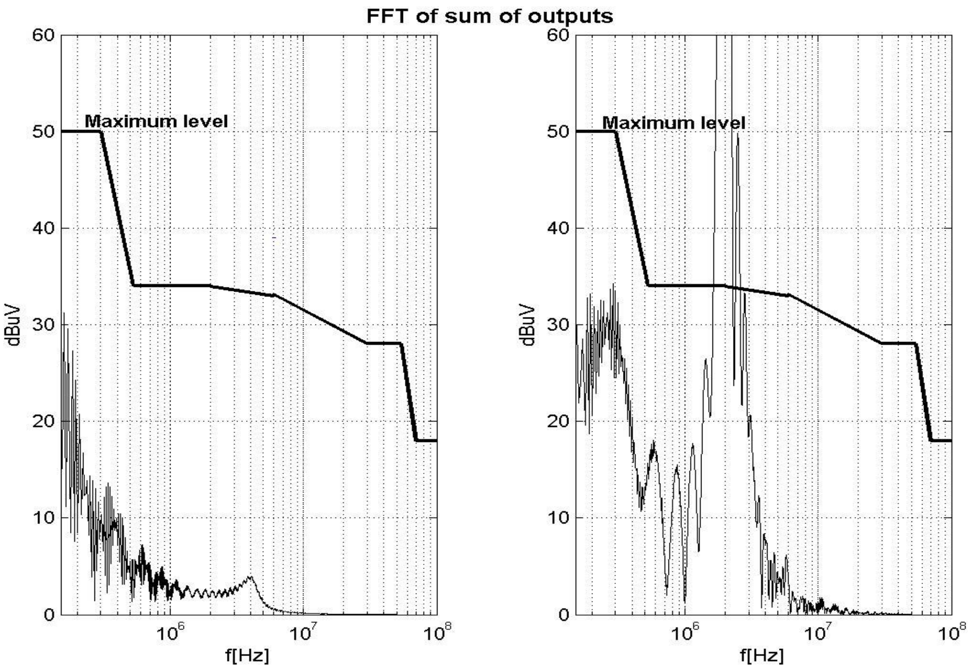


Fig 5.18. FFT of two different outputs. a) Steady output. b) Oscillating output.

In figure 5.18 it can be seen when over steering so the sum is oscillating makes the result go above the maximum values for radiated disturbances. This means that it is a better result to have a sum that is slow rather than having one that is fast.

5.3.8 Simulation of different loads

The design is supposed to work for different loads, such as purely resistive or inductive. Simulation has been done on different loads to see what loads the design has the ability to work with.

The simulations that have been done on the circuit this far, have been with a load that is pure resistive. This has been done because of that the behavior of a resistive load is easier to handle than an inductive load. The circuit is supposed to work for other loads than pure resistive and in figure 5.19 – 5.21 there can be seen the behavior of the circuit when using different loads.

The circuit for this test has been that one with a PD-regulator in its feedback.

The first test is to see if the circuit manages to handle a resistive load that is smaller than the one used in earlier simulations. In the simulations for testing the circuit, a resistive load of 47 Ohm has been used. The first test was performed in order to investigate what the result will be when lowering the resistance of the load, which is presented in figure 5.19.

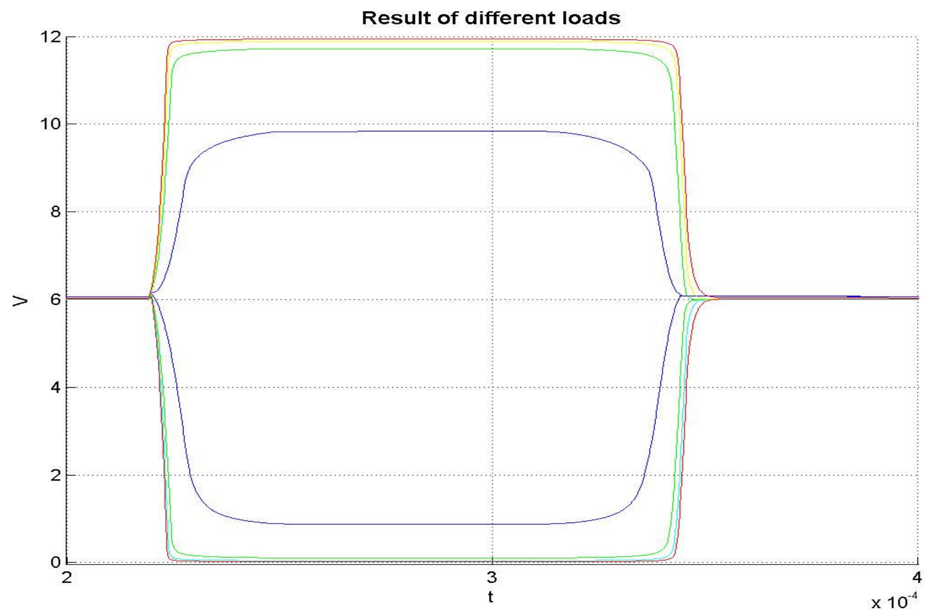


Fig 5.19. Result when testing different resistive loads. Red is 47 Ohm, yellow 25 Ohm, green 10 Ohm and blue is 1 ohm.

The result of lowering the resistance of the load is that the output signal will not reach its wanted final value. The decrease in output value starts already when the resistance is decreased just a couple of Ohm's. When a resistive load of 1 Ohm is used, the P-MOS only reaches approximately 10 volt and the N-MOS reaches down to 1 volt.

When adding up with an inductive load with a freewheeling diode, the snubber will be more important than when only a resistive load was used. The snubber network has to be set to minimize peak currents. Figure 5.20 shows how the circuit is responding when putting an inductive load in parallel with a resistor of 47 Ohm.

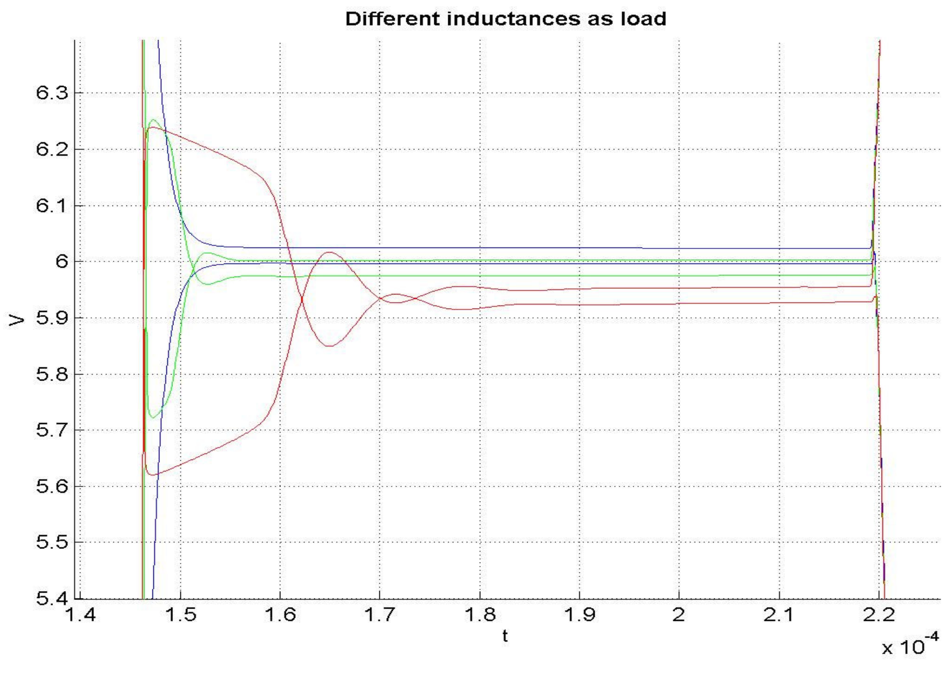


Fig 5.20. Result when signals are meeting at $V_{bat}/2$. Blue line shows an inductance of 10 µH, green line 50 µH and red line 200 µH. Resistance is 47 Ohm.

In figure 5.20 it can be seen that when a small inductance is added, the circuit is equal to the result when only using a resistive load. When increasing the inductance, there will be some overshooting in both output signals, if adjusting snubbers, this behaviour can be eliminated if the inductance is not too big. If there is an inductance that is too big and the snubbers are adjusted to minimize the overshooting, the rise and fall times will be too slow. This has been done for a load with an inductance of 50 µH and a resistance of 47 Ohm that can be seen in figure 5.21.

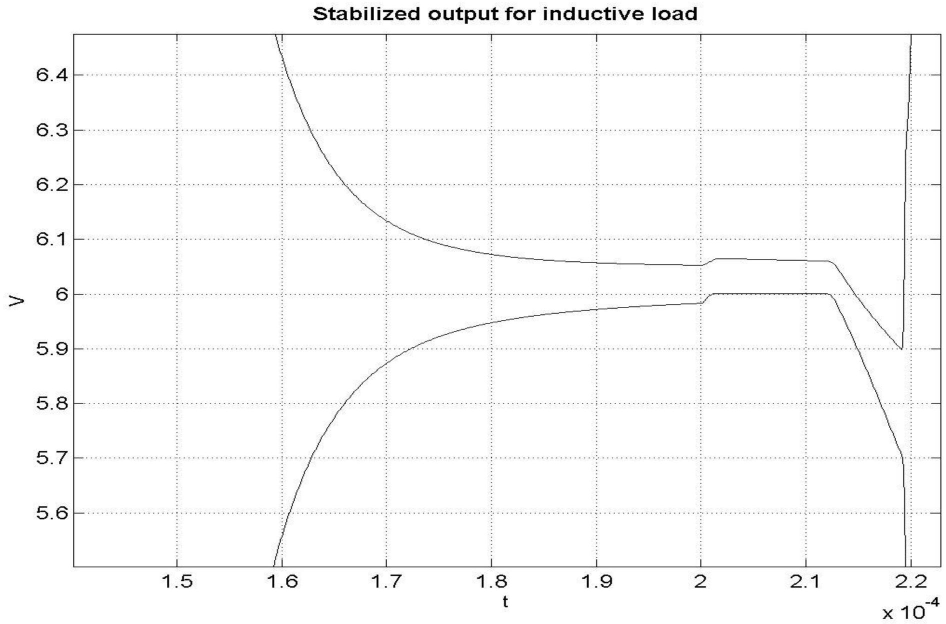


Fig 5.21. Stabilized output for inductive load at 50 µH, resistance of 47 Ohm.

As can be seen in figure 5.21, the overshooting is eliminated and that the rise time respective fall time of the two MOSFET´s have been slowed down dramatically. Because of this, there is not a possibility to use an inductance as load if it is too big.

5.4 Conclusion of simulations

During the simulations it has been found that it is difficult to get a result that is of a constant DC-level. Problems during regulations of input signal have shown that it can easily be steered in wanted direction, but since the fault signal will follow the created input signal it is very easy for it to start oscillating.

It has also been found that if having one slope at its optimum, will give a worse result on the other slope. Often with an oscillation as result, which is not good because it is placed in a frequency range where it is unwanted to have disturbances.

Best result is achieved by using a PID-regulator in the feedback. By first adjusting the resistors in the diode configuration, and then adjusting the values of the PID-regulator in the feedback an acceptable result is given.

By the different solutions that have been investigated, there does not seem to be any that can achieve a result of a plain DC-level between the two outputs.

To be able to optimize the result, one may need to use a smaller input signal for the slave, which would be easier to regulate. In this circuit an input between 0 and V_{bat} have been used, but using a signal that works between the MOSFET´s active region levels would be smaller in amplitude and make the regulation easier since it does not have to swing that many volts per second causing more ease of oscillation.

6. Hardware test results

In order to find the best result when calibrating the hardware cicruit there were a power supply used to keep V_{bat} at 12 volt and a frequency generator as switch signal with a frequency of 5.4 kHz, the arrangement for the equipment during the calibrating tests can be seen in figure 6.1. The resistors that could be changed so the circuit could get calibrated to wanted result were R_{g3}, R_{g4}, R_f and the proportional resistor between switching signal and feedback signal. During the test of the hardware it were found that there is a problem with the switching, the N-MOSFET and the P-MOSFET don't switch at the same time. This gives the same error for all different circuits but the problem is especially visual when the load is small.

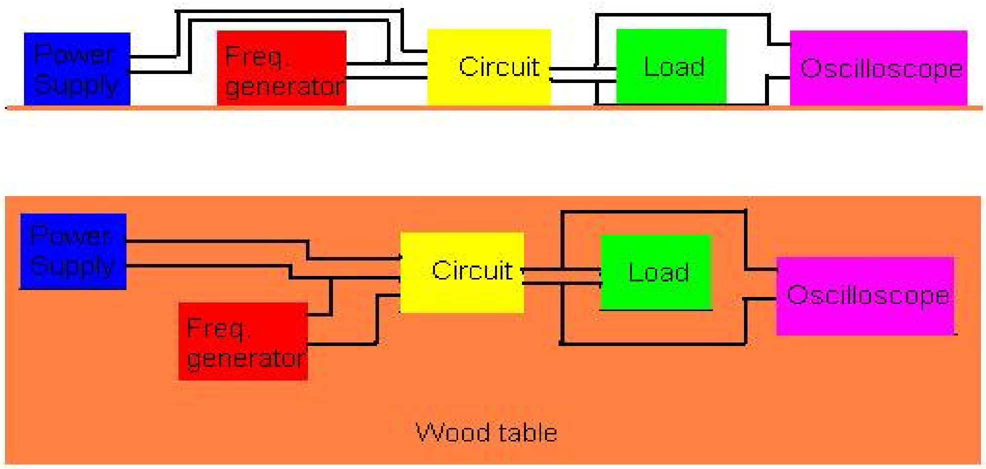


Fig 6.1. Arrangement for the equipment used during the calibration tests.

6.1 Test without feedback

This is the simplest circuit that only has an integrator and an inverter before the MOSFET's. The test without feedback had to be done to see how big the deviation is from the ideal and to have a comparison to the regulated circuits to see if they are better or worse. The best thing about this solution is that it needs few components and it is quite stable to ±5% resistance changes. Because the circuit is missing regulation it can't compensate for differences so the result isn't that good as can be seen in fig. 6.2.

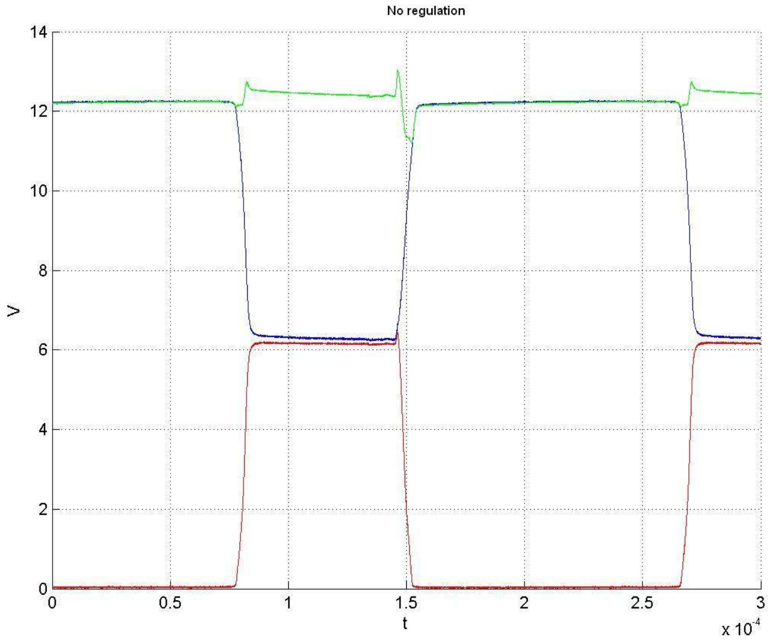


Fig 6.2. Voltage over load for the hardware circuit with no regulation, red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

6.2 Test with P-regulated circuit

This is the simplest form of feedback and the result is among the best, close to the ideal case for resistive load (47 Ω), as can be seen in figure 6.3. This circuit can be compared with the PD-regulated further down, they give almost the same result but this P-regulated circuit is a little bit more sensitive to small resistance changes. If a low-pass filter is added to the circuit, the result will be almost the same. To study where the disturbances in the frequency band occur an FFT is done on the sum of the lower and upper voltage which is shown in figure 6.4 where it is also added a reference for the limitations of narrowband conducted disturbances from table 2, class 5.

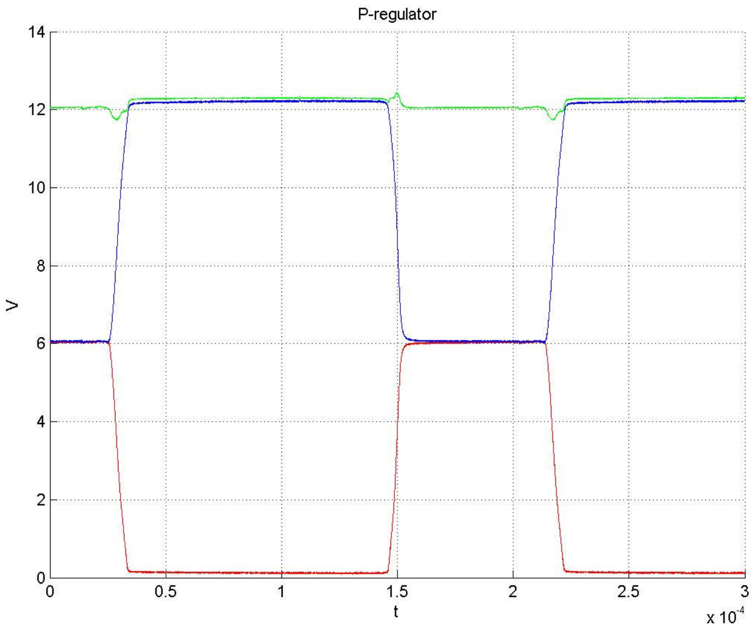


Fig 6.3. Voltage over the load for p-regulated hardware circuit, red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

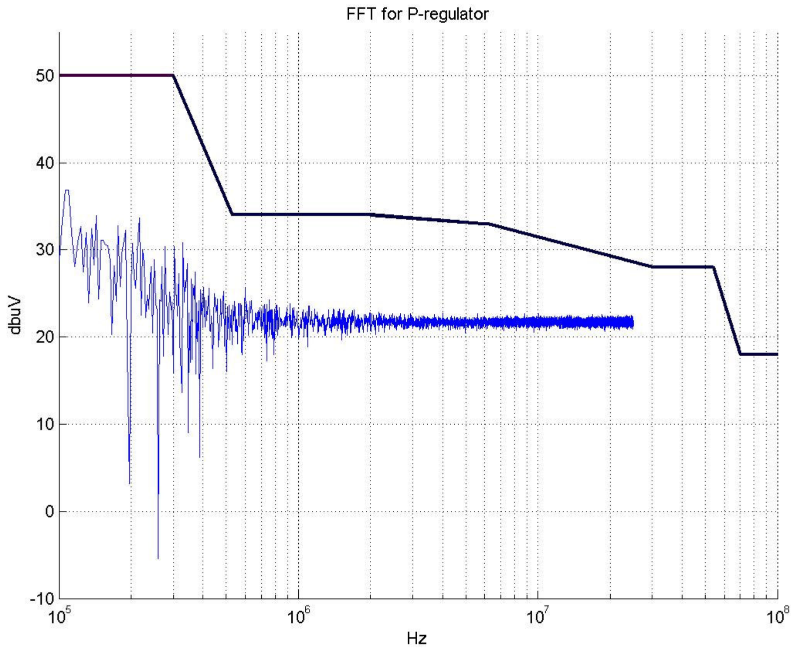


Fig 6.4. FFT for the sum of the lower and upper voltage over the load for the P-regulated hardware circuit, black line is showing the limit for narrowband conducted disturbances, class 5 from table 2.

From figure 6.3 the result shows that there is a slight difference between the two output signals. The lower output seems to be faster than the upper at both slopes. As seen in figure 6.4 there is a result that is below the limit with only a P-regulated feedback. The amplitude decreases with a factor of approximately 20 dB/decade in the region between 100kHz and 1MHz and after that it is a constant value of 22dBμV ±1dBμV.

6.3 Test with PID-regulator circuit

This circuit with PID-regulator and no low-pass filter is similar to the one with low-pass filter see chapter 6.4 below, but it's a little more stable and the result is still bad compared with the ideal case and P-regulator. One factor that affect the stability is the gain factor, higher gain will cause more instability, but sometimes will the gain factor not affect the result that’s depending on how the resistance that steers in the fault to the switching signal is set. Figure 6.5 below shows the best result for voltages over the load for the PID-regulator hardware circuit and figure 6.6 showing FFT for the sum of the lower and upper voltage.

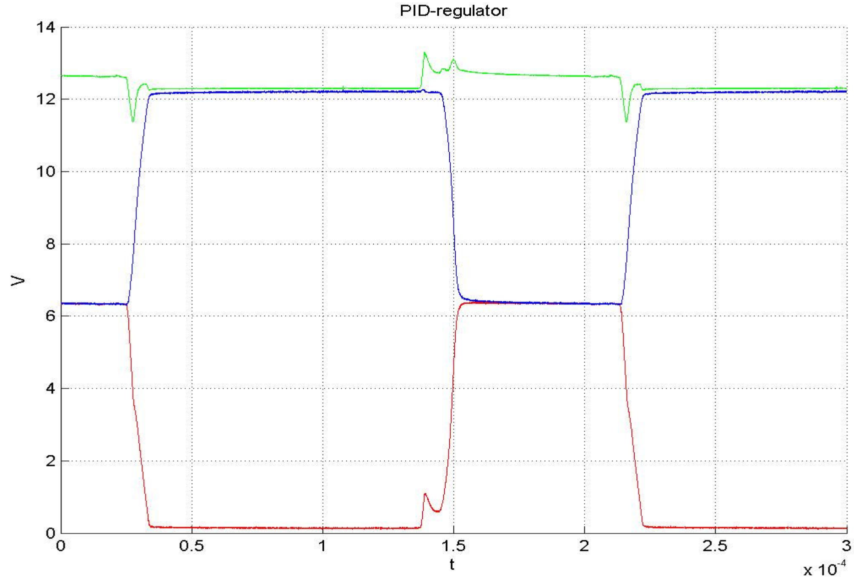


Fig 6.5. Voltages over the load for the PID-regulated hardware circuit, where the red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

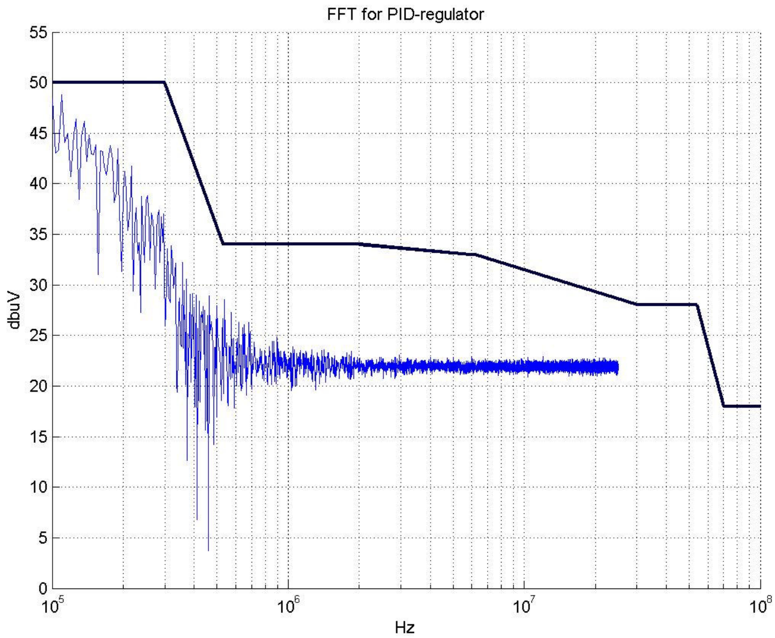


Fig 6.6. FFT for the sum of the lower and upper voltage for the PID-regulated hardware circuit, black line showing maximum allowed value.

The FFT in figure 6.6 shows that there is more disturbances with a PID-regulated than for a P-regulated circuit in lower frequencies. Though there is a fast decrease of the amplitude with almost 35dBμV/decade before it stabilises at the same level as for the P-regulated circuit as seen in figure 6.4.

6.4 Test with PID-regulated hardware circuit with low-pass filter

Common for the different PID-regulated circuits with low-pass filter is that they are volatile, the circuits where the derivation capacitor is equal or bigger than the integrating capacitor are more stable and the result is better. But if the derivation capacitor gets too big compared with the integrating capacitor it gets worse. The result gets a little better if there is a small external miller capacitor on the P-MOSFET because the internal miller capacitor is about 50pF smaller than the N-MOSFET capacitor. Sometimes there are quite good result but there would be problems to mass-produce this circuit, since if a resistor or capacitor is changed a few percent the result gets very bad, causing oscillations and bad regulation. Figure 6.7 shows how the result for the voltages over the load usually looks and fig. 6.8 shows the FFT for the sum of the lower and upper voltage over the load.

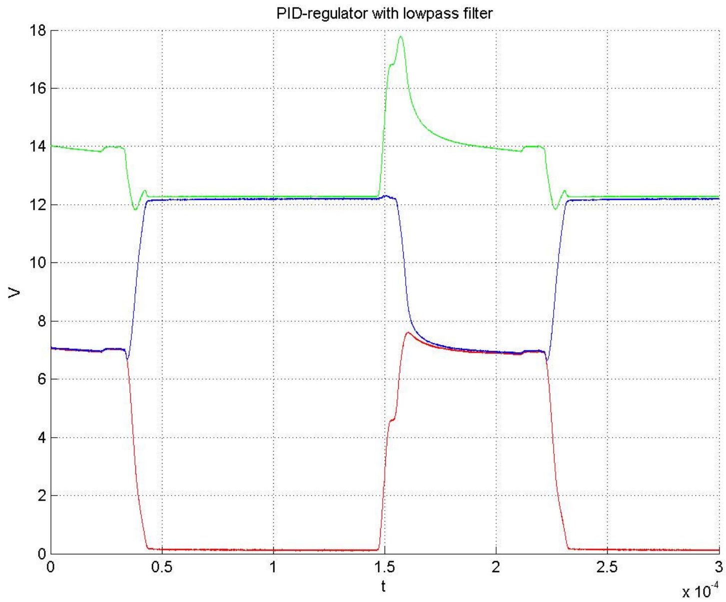


Fig 6.7. Voltages over the load for the hardware circuit with PID-regulator and a low pass filter where the red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

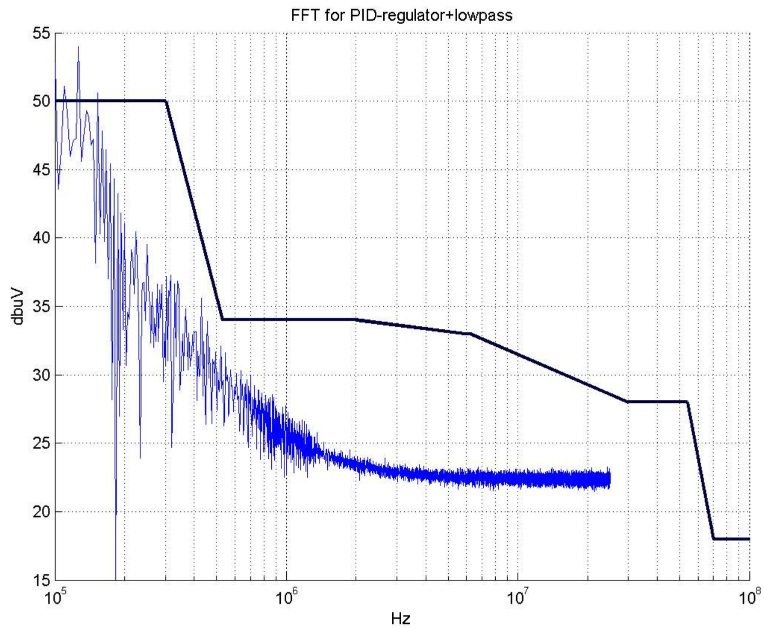


Fig 6.8. FFT for the sum of the lower and upper voltages for the PID-regulated with low pass filter hardware circuit, black line showing the maximum allowed value.

Comparing the result between a PID-regulated circuit and a PID-regulated circuit with a low pass filter shows that there is a big difference in result. The FFT in figure 6.8 shows that there is a lot of disturbances and that the result does not pass the limit for narrowband conducted disturbances.

6.5 Test with PI-regulator circuit

The circuit with a PI-regulator is the most sensitive of them all. With that is meant if a resistor value would be changed just 1-2 % the result will be changed drastic. When a small external capacitance is connected in parallel with the miller capacitor to the P-MOSFET the result gets a little better. Although a small external capacitance improves the result for PI-regulating this is a bad solution that is not recommended to use. Result on the best PI-regulator can be seen in figure 6.9 below.

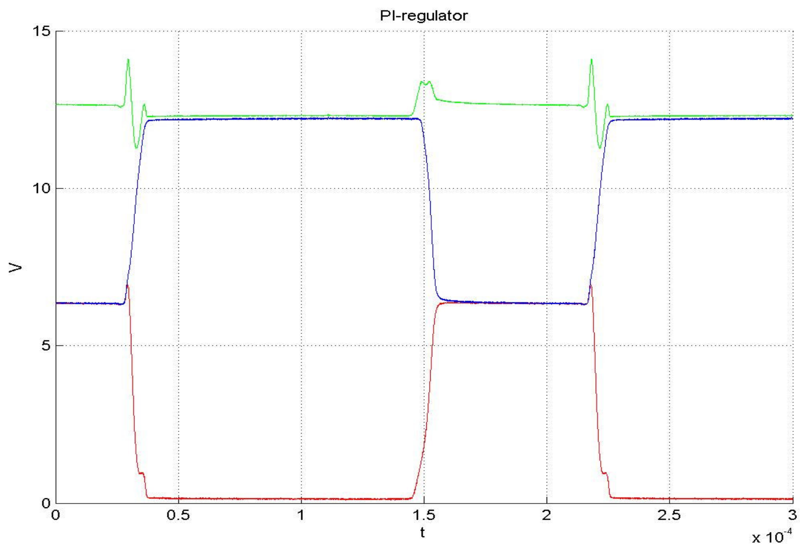


Fig 6.9. Voltages over the load for the PI-regulated hardware circuit where the red line is the lower voltages, blue upper and the green is the sum of the lower and upper.

6.6 Test with PD-regulator circuit with a big external capacitance

Although in theory it seems all right to compensate for difference in miller capacitors between N-MOSFET and P-MOSFET through an external parallel capacitor that is about 10 times bigger than the inner to avoid the difference between them, the hardware test showed the opposite. There exist oscillations and the rise and fall time is different, that can be compensated but not the oscillations. The hardware circuit result where very bad as can be seen in figure 6.10.

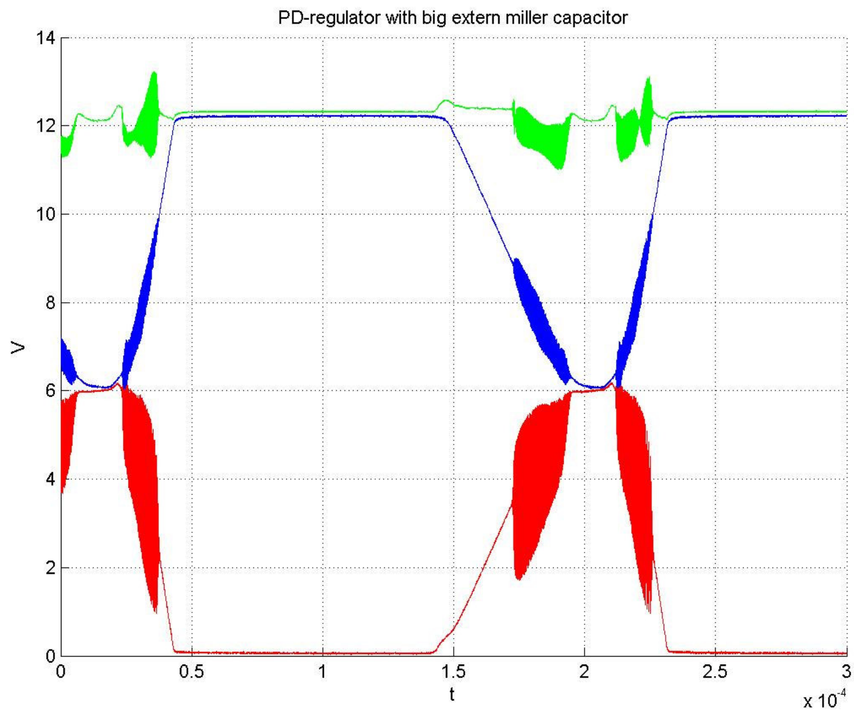


Fig 6.10. Voltages over the load for the PI-regulated hardware circuit where the red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

The oscillation that's appear during the switching gives rise to large disturbances high up in the frequency band which would be very dominant in a FFT graph, which hasn't been done because of the bad result it would give and the solution is not recommended to be used.

6.7 Test with PD-regulator

When testing the different circuits it were found that the circuits that where PD-regulated where the best, more stabile for changes and closest to the ideal look and the derivation resistor was chosen to be 10.0 kΩ and the gain resistance (R_i) 9.1 kΩ. Because this was the best circuit several more tests have been performed on it to get good understanding on what the different components do and how they should be changed to improve the result.

6.7.1 Changing the derivation capacitor

When increasing the derivation capacitor the gain has to be lower to get a stable result over the load. For PD-regulator the oscillations doesn't get that big, and if decreasing the gain they will disappear. The best result where from the circuit with a derivation capacitor with the size of 10 pF. Figure 6.11 shows the voltages over the load for the PD-regulated circuit with the snubber resistors equal and no external capacitor on the P-MOS, this result is used as a reference to the other PD regulated circuits that is tested below to see if they are better or worse. Figure 6.12 shows the FFT of the sum of the lower and upper voltages for the PD-regulated circuit with equal snubber resistors and no external capacitor.

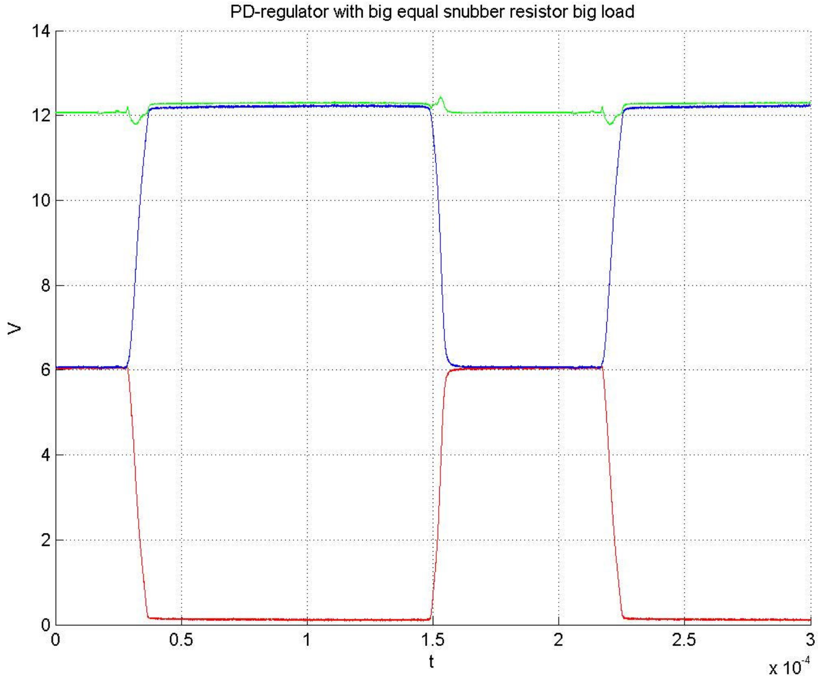


Fig 6.11. Voltage over the load for a PD-regulated hardware circuit where the red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

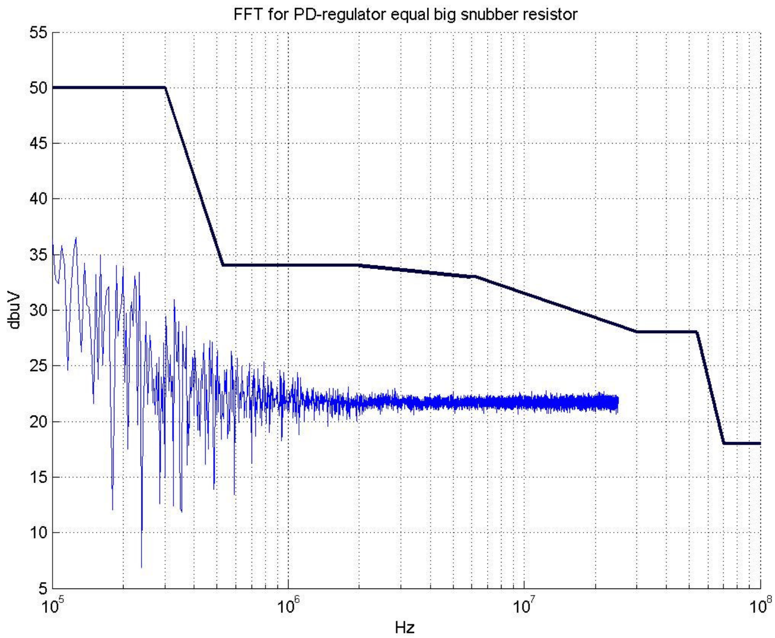


Fig 6.12. FFT of the sum of the lower and upper voltage for the PD-regulated circuit with equal snubber resistors, where the black line showing maximum allowed value.

The FFT result for the PD-regulated circuit when having equal snubber resistors shows a pretty good result with a decrease of 15dBμV/decade between 100kHz and 1Mhz and then a stable result for frequencies above that. It is far below the limit for the narrowband conducted disturbances even for low frequencies which is good.

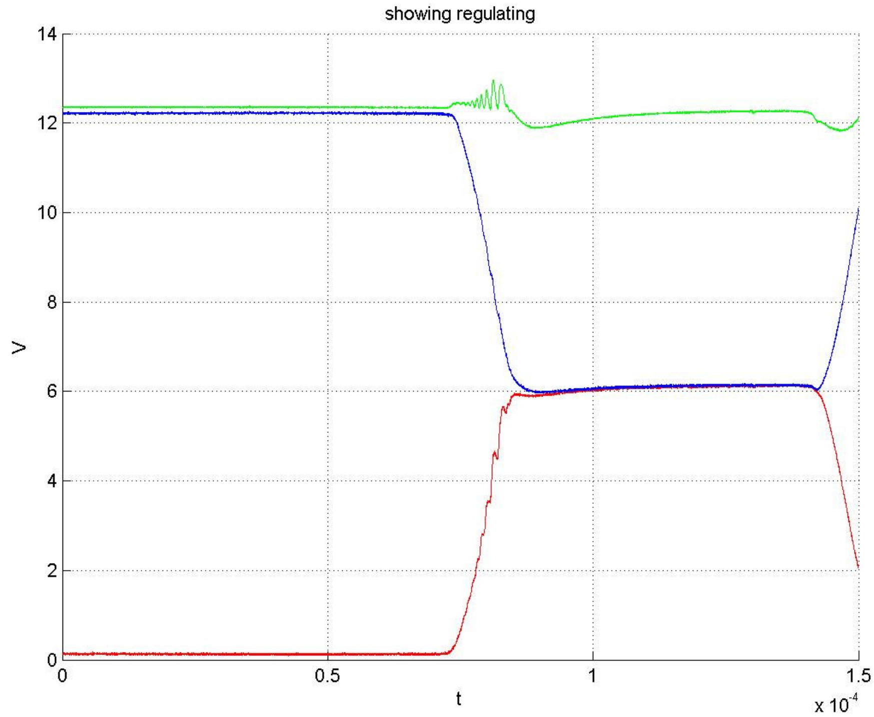


Fig 6.13. Result if gain is set too high, same thing happens for all the circuits, red line is the lower voltage, blue upper and the green is the sum of the lower and upper voltages.

The result gets better if the gain is high but fig 6.13 above shows what happens if the gain is set too high which is bad for the result, this result appears for all the circuits when the gain gets too high.

6.7.2 Varying the snubber resistors

To see how the snubber resistor would be best dimensioned, the hardware testing was made without a small external capacitor on the P-MOS. To get the best result the snubber resistors should be optimized for the size of the load. But this test was made to find out if the snubber resistors would be of different or same size, when they were not dimensioned for any special load. The result was showing that if we have a quite big load and the resistors were dimensioned larger than necessary, they should be of the same size for best result. But when the load resistance is small it's necessary to calculate the both resistors for the best result according to the design chapter for the snubber se section 4.3.2. The result in figure 6.14 is showing the result for a big load and the resistors different to each other, the snubber resistor for the P-MOS is about two times bigger than the snubber resistor for the N-MOS. In figure 6.15 shows the FFT for the sum of the lower and upper voltages so the disturbances amplitude and where in the frequency spectrum they appear.

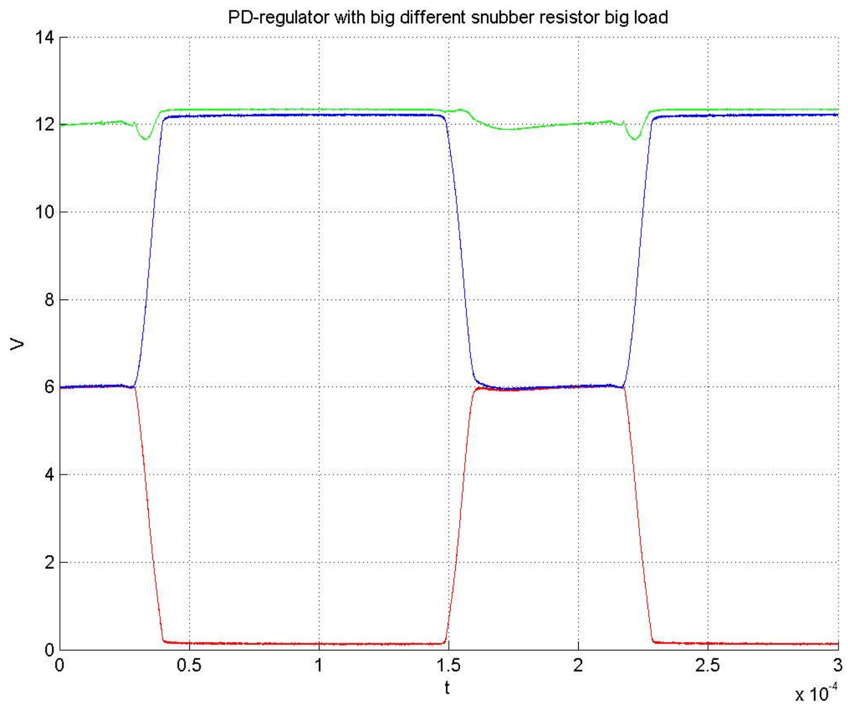


Fig 6.14. Voltages over the load for the PD-regulated circuit with different snubber resistors, red line is the lower voltage, blue upper and the green is the sum of the lower and upper.

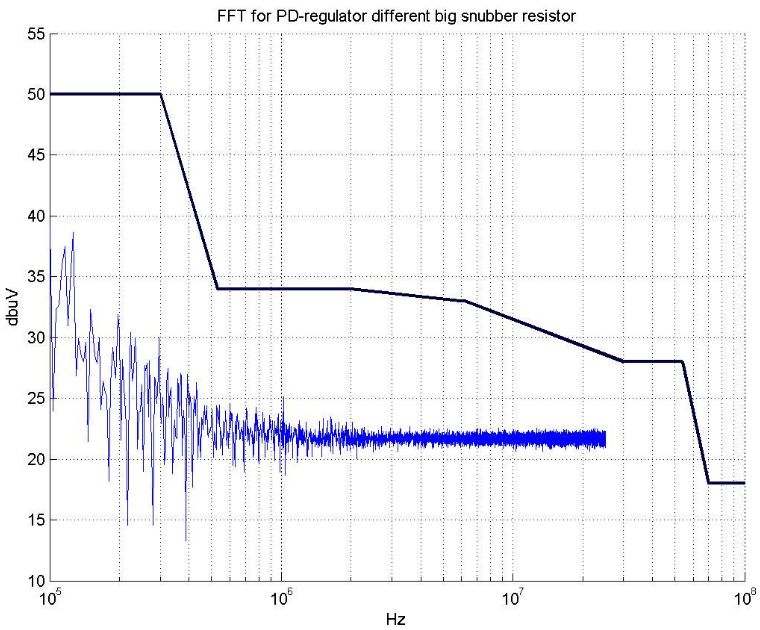


Fig 6.15. FFT signal for the sum of the lower and upper voltages for the PD-regulated signal with different snubber resistors, black line showing maximum allowed value.

If comparing the FFT in figure 6.15 with the FFT result in 6.12, one can see that there is a slight difference between the two. The result in figure 6.15 have bigger disturbances in the intervall of 100 – 200kHz which is not wanted because of that is a frequency band for AM-radio. The result is though below the limit for narrowband conducted distrubances.

6.7.3 Varying the external capacitor for the P-MOS

Because of that the integrated N- and P-MOSFET have different internal capacitor values, an external one were connected in parallel with the P-MOSFET because it had the smallest capacitance. The results were showing an improvement on all the tests but the best result were when the external capacitor were a little bigger, 1-4 times, than the difference between N and P miller capacitor. The improvements gave a more stable signal and were easier to calibrate. The result for the circuit with an external capacitor of 560 pF is presented in fig. 6.16. The FFT signal for the sum of the lower and upper voltages is shown in figure 6.19.

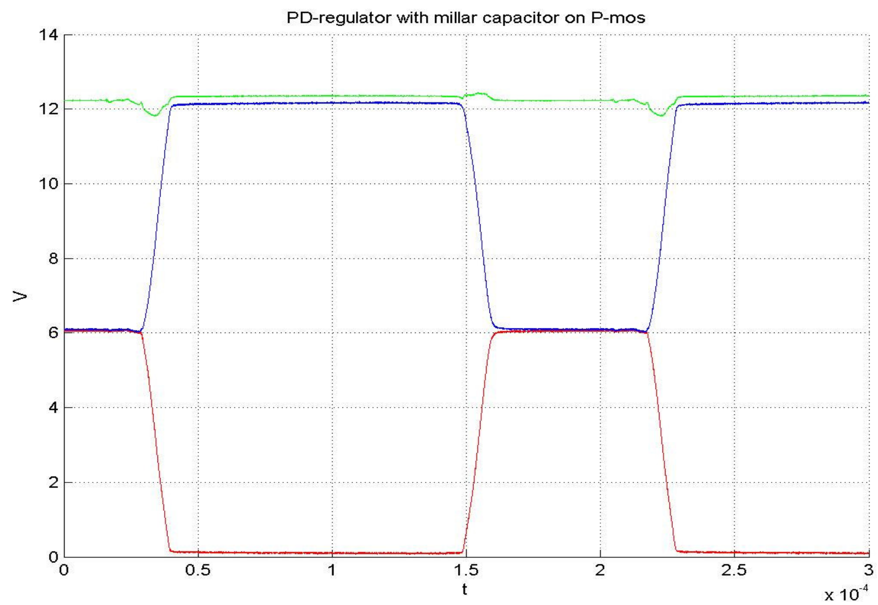


Fig 6.16. Voltages over the load for a PD-regulated circuit with a small external capacitor on the P-MOS, the red line is the lower voltage, blue upper and the green line is the sum of the lower and upper voltage.

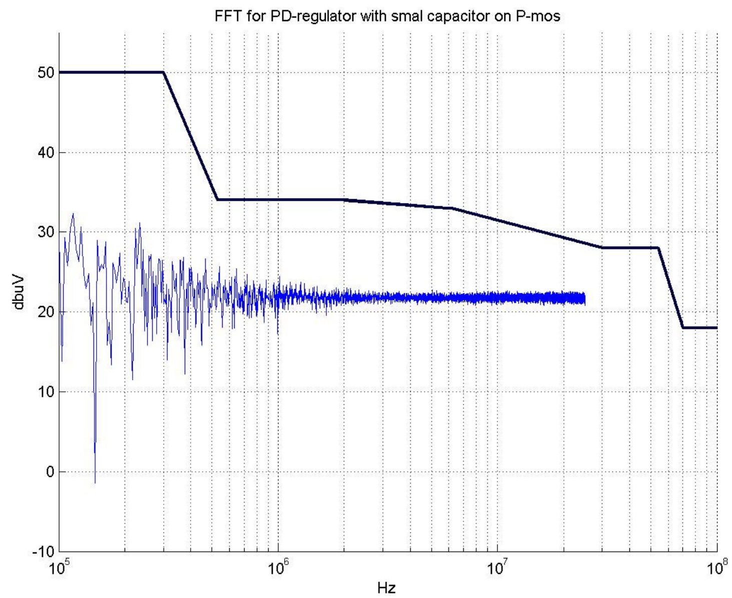


Fig 6.17. FFT for the sum of the lower and upper voltages for the PD-regulated circuit with a small external capacitor on the P-MOS, black line showing maximum allowed value.

The result shown in figure 6.17 is the best result achieved for the different configurations that have been tested. It is far below the limit for narrowband conducted disturbances and there is almost no spikes in the lower frequencies that have been an issue in the earlier FFT's.

6.8 Test of different loads

During the test of different loads it was found that the resistors in the diode configuration must be changed for different loads to keep the rise and fall-time equal to each other and not slower than 20µs. When the load and the diode resistors decrease it becomes harder to regulate, when the load is small and inductive it becomes even harder for the regulator to keep the result as close as possible to the ideal result. Keeping the switching moment equal for both the MOSFET's becomes more important when the load is decreased, because the regulator can't compensate for an error that is too big.

All this problems with smaller and inductive load becomes visual in figure 6.18 where the load is an OSRAM lamp 12V55W where the voltage source is only 6V to avoid too big currents. In figure 6.19 is voltages over an OSRAM 12V21W shown for a PD-regulated circuit with different snubber resistors and a small external capacitor, but the voltage source is not stabilized with a big capacitor between $+V_{bat}$ and ground as in the final circuit which result is shown in figure 6.20.

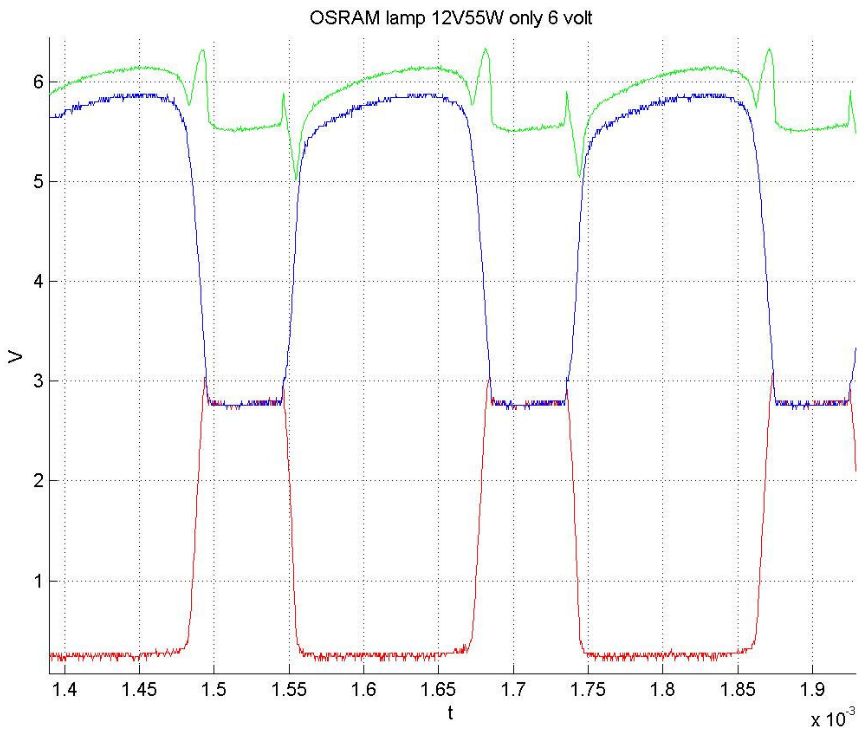


Fig 6.18. Voltage over the load for a PD-regulator with different snubber resistors and a small external capacitor on the P-MOS, red line is the lower voltage, blue upper and the green is the sum of the lower and upper voltages.

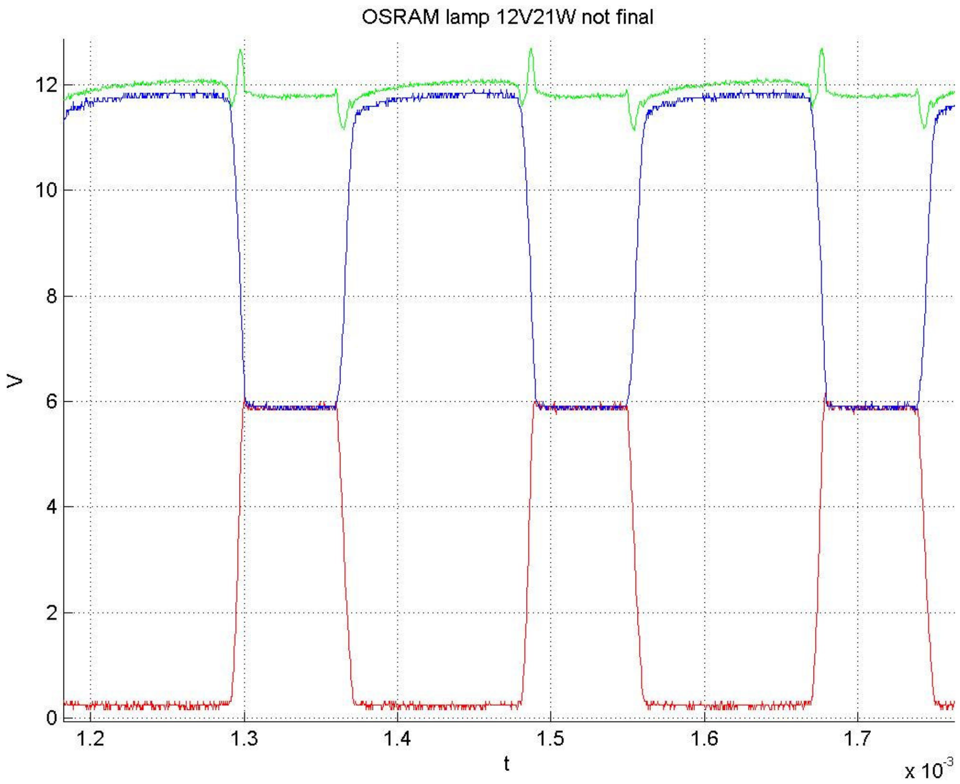


Fig 6.19. Voltages over the load (OSRAM lamp 12V21W) for a PD-regulated circuit with different snubber resistors and a small external capacitor on the P-MOS, red line is the lower voltage, blue upper and the green is the sum of the lower and upper voltages.

The spikes that can be seen above in the figures when the MOSFET's are switching, are lower than ±1 V which is a demand, but these spikes will give disturbances in a FFT graph that is above the limit which is not good. The spikes in fig 6.18 will not get that much bigger when the DC level is 12 volt, these arise because there is different between when the N-MOS and P-MOS switch that will be kept almost at the same level until the both MOSFET's done with rise/fall time.

6.9 Radiated emission test for hardware circuit

The test for radiated emission from the twisted wire were made in a ALSE close to standardized test condition according to CISPR 25, and the circuit itself were screened as much as possible. The PD-regulated circuit with adapted snubber resistors and a small external capacitor on the P-MOS with no stabilisation capacitor between $+V_{bat}$ and ground were not good enough because of the LISN. The error is much bigger with a LISN between the circuit and the power generator, because the LISN can not hold the voltage level stable when the circuit is switching. When transients occur on the DC voltage the reference voltage will be affected and the discrepancy gets larger. Figure 6.20 shows the radiated emission from the twisted wire when the DC level is stabilized on the circuit with a capacitor between +Vbat and ground and the load is an OSRAM lamp12V21W. In figure 6.21 the radiated emission is shown from a circuit with one MOSFET that is switching the OSRAM lamp 12V21W with no snubber, normal switching circuit. Comparing these two results, it is easy to see that switching the load with two MOSFET's against each other lowers the radiated emission.

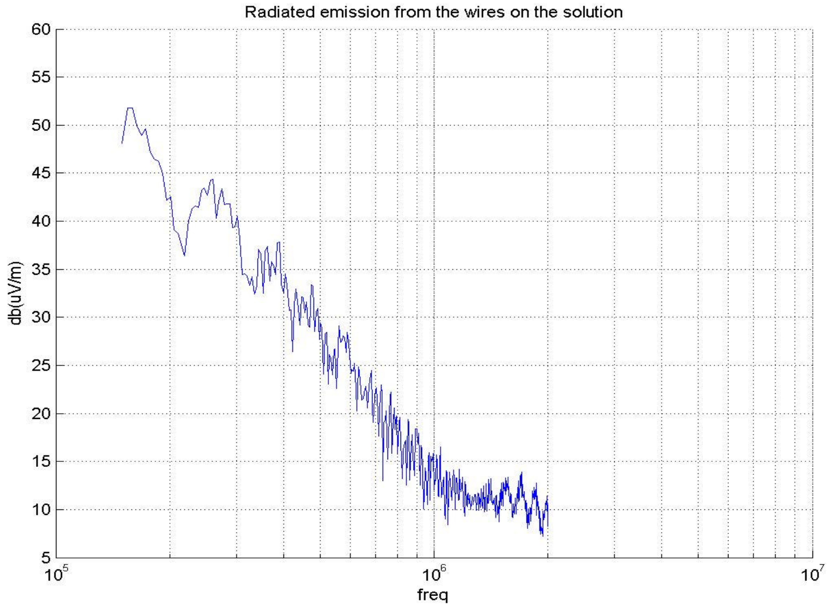


Fig 6.20. Radiated emission from the wires for final solution which is PD-regulated with different snubber resistors, a small capacitor on the P-MOS and between +V_{bat} and ground is big stabilizing capacitor.

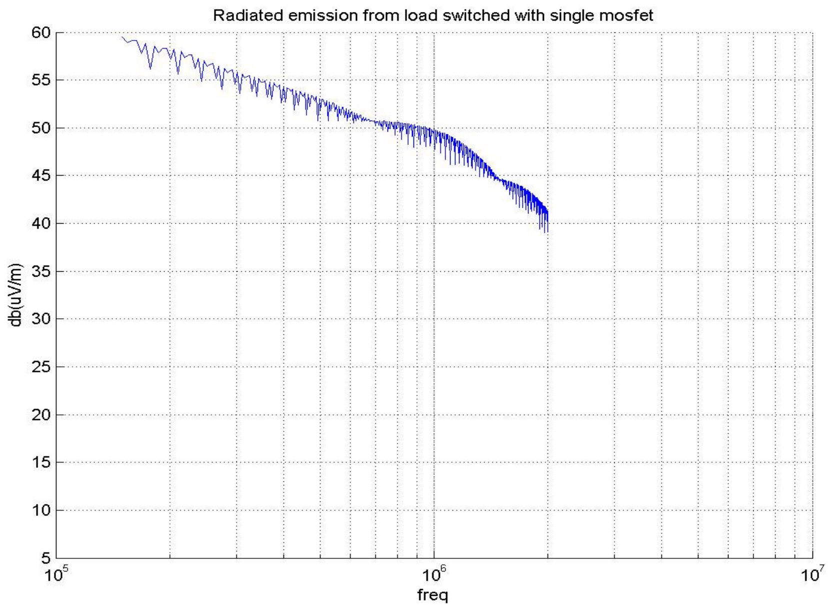


Fig 6.21. Radiated emission from the same load (OSRAM lamp 12V21W) but only switched with one MOSFET.

The FFT in figure 6.20 shows a test from an ALSE where the radiated emissions from cable between circuit and load have been under investigation. The result shows that there is a decrease of 45(dBµV/m)/decade which is a very good result. And if comparing the result in figure 6.21 where only one MOSFET were used there is a very large difference in both amplitude and how fast it decreases.

6.10 Rise- and fall-time for hardware circuit

Because there are different rise- and fall-time between the MOSFET's, the faster times must be adapted to the slowest time. The reason for adapting the rise and fall times to be same is to cancel out RF emission and to have symmetrical pulses. Depending on the load there is a different slowest time for the MOSFET's in the circuit. Setting the rise- and fall-time to be equal is done with the diode configuration and an external capacitor. The fastest equal rise- and fall-time occurs when the load is small which give a time about 2µs. But when the rise and fall time is fast and a switching problem occurs, the error will be bigger than for a slower time. The rise and fall-time can at its most be 10% of the total pulse duration, this gives the highest allowed switching frequency of 25 kHz.

6.11 Conclusions on the hardware circuit

During the hardware test some important improvements and conclusion have been made that has to be summarised. The most important improvement of the circuit that has been done is the stabilising of the DC voltage during switching with a capacitor between V_{bat} and ground on the circuit. This capacitor improves the result considerable because the dc signal gets stabilized when there is a switching. If the circuit would not have this stabilizing capacitor the error will be feedbacked to V_{bat}, which is not good since the reference signal $V_{bat}/2$ will be affected because it is created with a simple voltage divider. $V_{bat}/2$ is affecting the switching point and if there exist a time shift between the two MOSFET's switching point would this time shift be bigger if not the DC level is stabilized.

This improvement was not done until the test of the radiating emission, where it became most visible, which was the last thing that was tested. But this improvement didn't affect the other hardware test that much so they had not to be done again. During the other hardware tests were the DC level stable enough, which not affected the result during the switching. In figure 6.22 the result of the improvement can be seen when the load is an OSRAM lamp 12V21W, when the circuit is PD-regulated with a small external capacitor on the P-MOS see Appendix 2. The shape of the sum of lower and upper voltage is about the same as in figure 6.3 so the FFT gets about the same as for that circuit which is shown in figure 6.4.

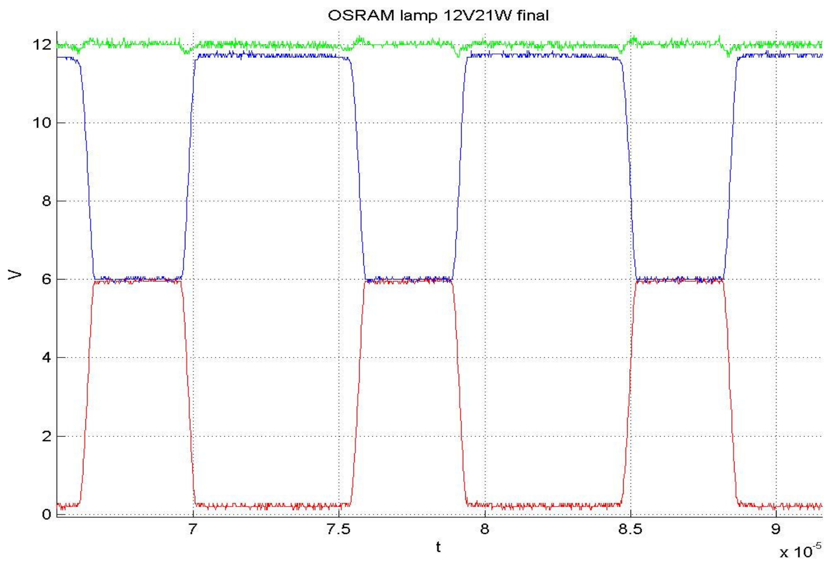


Fig 6.22. Voltage over the load for the final solution, where the red line is the lower voltage, blue upper and the green is sum of the lower and upper voltage.

The problem that gives the largest error on the result after stabilization is the problem with different switching point for the N-MOS and P-MOS. To make this error decrease the integrator, which slows down the switched signal, and the inverter must be improved, moreover if the regulated feedback signal would be faster the error would decrease even further. As long as these parts are not improved the circuit can not be used for all loads. If the load have too small resistance and too big inductance can not the differency be within the wanted limits and the circuit can't be switched with too high frequency.

The final conclusion of the hardware circuit is that the idea with two MOSFET's that are switching against each other to lower the RF emission compared with the normal way of switching with one MOSFET works, but there exist some problems.

7 Conclusions

The idea of having two MOSFET's switching a load by letting one MOSFET be switched between 0 – $V_{bat}/2$ and the other MOSFET between $V_{bat}/2$ – V_{bat} and in this way cancel out the radiated emissions works, which can be seen when comparing fig 6.20 and 6.21. The voltage variation on the sum of the lower and upper voltages in the solution is below ±1V which was a demand but the radiated emission from the wires without EMI filter or shielding were a little bit over the demand when switching with a frequency of about 5.4 kHz.

The simulation program OrCad was used as an aid when the circuit was constructed to get to the final solution and to get a deeper understanding of the circuit. But there are some differences between the best hardware circuit and the best circuit in the simulation program. The circuit that gave the best result in the simulation was PID-regulated, same hardware circuit was really bad with lots of oscillations and hard too calibrate to get a decent result. The best result on the hardware circuit was PD-regulated which gave good result in the simulations too. This circuit was stabile and easy to calibrate to get the desired result and stable to small resistance and capacitance changes that can arise during manufacturing process. Although there is a difference between simulation and hardware circuit, the simulation did give a good hint on how the result looked in reality.

Because the circuit is not optimal, some limitations do exist. The limitations are mainly that the circuit is load dependent, which gives limitations in the choice of operational amplifiers and the availability of complementary MOSFET´s for the desired currents and voltages. The limitations that exist on the present design are rise/fall time that can be too fast, which limits the switching frequency to about 25 kHz. The circuit also has some problem with loads that have too small resistance or too big inductance, which creates transient on the upper and lower voltage and amplitude difference between the upper and lower voltages. These two errors lead to that the radiated emission increase because the cancellation is less effective.

As the hardware tests show, this circuit can be used for switching lamps with a frequency below 5.4 kHz and get an environment with low emission, almost without using an EMI filter or shielding. The circuit can be used for other loads as long as the load is not having too low resistance or/and too big inductance and need to be switched with high frequency. If the circuit will be used for any kind of load it is recommended to improve the integrator, inverter, speed of the regulator. Moreover work with the stability on the DC signal is also needed. If those parts of the circuit would be improved in future, this will be a good circuit for reducing the radiated emission from the wire between the circuit and the load.

Acknowledgements

This examination thesis work was carried out at Research and Development department for Electrical and Electronics Engineering 94800 at Volvo Cars Corporation Gothenburg autumn 2004, Sweden. The work is a compulsory part of the Electrical Engineering degree at Chalmers University of Technology.

We would like to express our highest gratitude towards our supervisor Tryggve Tuveson at Volvo Cars Corporation for initiating this idea and guiding us through the thesis in terms of technical discussions and buttress us in providing requisite facilities to accomplish this task. We would also thank our examiner Assoc. Prof Torbjörn Thiringer at Chalmers University of technology for invaluable contribution in participating in discussions and providing his suggestions for improvement of work.

We would also like to convey thanks to Göran Petersson, Robert Karlsson, Thomas Törnvall who were lending their time for discussion and supporting with technical devices. We are also sending our deepest thanks to Volvo Car Corporation for letting us utilise lab facilities, test sites and equipment whenever we were in need of carrying out experimental studies.

References

[1] Mohan, Undeland, Robbins (2003) *Power Electronics Converters, Applications, and Design*, USA: Wiley, ISBN 0-471-42908-2

[2] Lennartson, Bengt (2002) *Reglerteknikens grunder*, Sweden: Studentlitteratur, ISBN 91-44-02416-9

[3] Nelson, John C.C (1995) *Operational Amplifier Circuits: Analysis and Design*, Boston: Butterworth-Heinemann, ISBN 0-7506-9468-8

[4] Emanuelsson, Alf (1993) *Signaler och kretsar*, Sweden: Studentlitteratur, ISBN 91-44-39211-7

[5] Perez, Reinaldo (1995) *Handbook of Electromagnetic Compatibility*. California: Academic press, ISBN 0-12-550710-0.

[6] Tihanyi, Laszlo (1995) *Electromagnetic Compatibility in Power Electronics*. N.J, IEEE Press, ISBN 0-7803-0416-0

[7] Sedra, Adel S. (1998) *Microelectronic Circuits*, New York: Oxford Univ. Press, ISBN 0-19-511690-9

[8] Floyd, Thomas L (1996) *Electronic devices*, New Jersey: Prentice Hall, ISBN 0-13-362963-5

[9] International Electrotechnical Commision (1995) CISPR-25, *Limits and methods of measurement of radio disturbance characteristics for the protection of receivers used on board vehicles*. Geneva: IEC Press. CISPR25 © IEC 1995

[10] ELFA AB. 1998. Retrieved august 2004. <http://www.elfa.com>.

[11] Snubber Networks. 2000. Retrieved august 2004. <http://homepages.which.net/~paul.hills/Emc/Snubbers.html>.

Appendix 1: Matlab code for calculating theoretical differences from the ideal

Following code is made for calculating and plotting the difference from the ideal

```
clc;
clear;
close all;

%-----Triangle-----
Amptri=0.4; %amplitude of triangle disturbance
tr=1.5*10^(-6); %rise time triangel
tf=2.5*10^(-6); %fall time triangel
ts=4*10^(-6); %time duration of triangle puls ts=tr+tf

%----Trapezoid----
Amptrap=1; %amplitude of trapezoid disturbance
tr2=1*10^(-6); %rise time trapezoid
tf2=1*10^(-6); %fall time trapezoid
ts2=4*10^(-6); %time duration of trapezoid puls ts=tr2+tf2+td2
td2=2*10^(-6); %duration flat time trapezoid td=ts2-tr2-tf2

%----Square----
Ampsq=0.6; %amplitude symmetrical square wave max 1.2 allowd

%----Oscillation----
Amposc=2; %amplitude oscillation
Tper=30*10^(-7); %time/freq for the oscillation

A=0.4; % amplitude
fsw=5.5*10^3 %switching frequency
R=1.5*10^(-6); %rise time and fall time
Td=1/fsw;
 %R=0.08; % rise time/period
 %F=0.01 % fall time/period
d=0.2; % duty ratio


%----unsymmetric square wave will not to be used only reference

S2=120+20*log10((A./(2*pi.*k)).*abs(3.*sin(pi*d.*k)-sin(pi*(2-d).*k)));
figure(2)
semilogx(fS,S2,'b-'), grid on

xlabel('frequency (Hz)')
ylabel('SquareUn(f) dBuV')
axis([20e3 100e6 ymin ymax])

%------ triangle wave unsymmetric, symmetric if tf=tr

Atri=120+20*log10(abs((((Amptri*Td)./(tr*4*(pi)^2.*k.*k)).*((exp(-
j*2*pi*tr.*k/Td)).*((-j*2*pi*tr.*k/Td)-1)+1))...
    +(Amptri./(j*2*pi.*k)).*((exp(-j*2*pi*tr.*k/Td))-(exp(-
j*2*pi*ts.*k./Td)))...
    -((Amptri*Td)./(tf*4*(pi)^2.*k.*k)).*((exp(-j*2*pi*ts.*k./Td)).*((-
j*2*pi*ts.*k./Td)-1)...
    -(exp(-j*2*pi*tr.*k./Td)).*((-j*2*pi*tr.*k./Td)-1))...
    +((Amptri*tr)./(j*tf*2*pi.*k)).*((exp(-j*2*pi*tr.*k./Td))-(exp(-
j*2*pi*ts.*k./Td)))));

figure(3)
semilogx(fS,Atri,'b-'), grid on
```

```
xlabel('frequency (Hz)')
ylabel('Atri(f) dBuV')
axis([20e3 100e6 ymin ymax])

%---- trapezoid ----
% symmetric trapezoid should work for unsymmetrical to depending on
rise
% and fall time

Atrap=120+20*log10(abs((((Amptrap*Td)./(tr2*4*(pi)^2.*k.*k)).*((exp(-
j*2*pi*tr2.*k/Td)).*((-j*2*pi*tr2.*k/Td)-1)+1))...
    +(Amptrap./(j*2*pi.*k)).*((exp(-j*2*pi*td2.*k/Td))-(exp(-
j*2*pi*ts2.*k./Td)))...
    -((Amptrap*Td)./(tf2*4*(pi)^2.*k.*k)).*((exp(-
j*2*pi*ts2.*k./Td)).*((-j*2*pi*ts2.*k./Td)-1)...
    -(exp(-j*2*pi*td2.*k./Td)).*((-j*2*pi*td2.*k./Td)-1))...
    +((Amptrap*td2)./(j*tf2*2*pi.*k)).*((exp(-j*2*pi*td2.*k./Td))-
(exp(-j*2*pi*ts2.*k./Td)))...
    -(Amptrap./(j*2*pi.*k)).*((exp(-j*2*pi*td2.*k/Td))-(exp(-
j*2*pi*tr2.*k/Td)))));

figure(4)
semilogx(fS,Atrap,'b-'), grid on

xlabel('frequency (Hz)')
ylabel('Atrap(f) dBuV')
axis([20e3 100e6 ymin ymax])


%---- symmetrical square wave ----

Asq=120+20*log10(abs((2*Ampsq/pi)*(sin(pi*0.5.*k)./k)));

figure(5)
semilogx(fS,Asq,'b-'), grid on

xlabel('frequency (Hz)')
ylabel('Asq(f) dBuV')
axis([20e3 100e6 ymin ymax])

%---- oscillation ----

Co2=(2*pi/Tper);
damping=300000; %damping variable depending on the curve
Co1=damping+j*2*pi.*k/Td;

Aosc=120+20*log10(abs((Amposc/Td)*((exp(-
(Td/2).*Co1)./(Co1.*Co1+Co2.*Co2)).*(-Co1.*sin(Co2*Td/2)-
Co2*cos(Co2*Td/2))...
    +Co2./(Co1.*Co1+Co2.*Co2))));

figure(6)
semilogx(fS,Aosc,'b-'), grid on

xlabel('frequency (Hz)')
ylabel('Aosc(f) dBuV')
axis([20e3 100e6 ymin ymax])

figure(7)
timeosc=0:10*10^(-9):20*10^(-6);
signalosc=Amposc*(exp(-damping.*timeosc)).*sin(Co2.*timeosc);
plot(timeosc,signalosc);

%===============================================================
```

```
clc;
clear;
close all;


A=2; % amplitude for sinuswave
fsw=5.5*10^3 %switching frequency
Td=1/fsw;
t1=1.7*10^(-6); %half the length of sinus lookalike puls
offset=1; %offset
tau=5*10^(-6)/4; %time of hole sinus

step=.05;
initk=1;
finalk=3000;

k=initk:step:finalk;
fS=fsw*k;
ymin=0;
ymax=130;



% sinus lookalike puls with negative offset
S=120+20*log10(abs((4/Td).*((A*((sin((2*pi/(4*tau)-
2*pi.*k/Td).*t1))./(2.*(2*pi/(4*tau)-2*pi.*k/Td))...

+(sin((2*pi/(4*tau)+2*pi.*k/Td).*t1))./(2*(2*pi/(4*tau)+2*pi.*k/Td)))).
..
    -(offset*Td./(2*pi.*k)).*sin(2*pi*t1.*k/Td))));

figure(1);
semilogx(fS,S,'b-'), grid on

xlabel('frequency (Hz)');
ylabel('S(f) sinus dBuV');
axis([20e3 100e6 ymin ymax]);

% sinus lookalike puls with positive offset
S2=120+20*log10(abs((4/Td).*((A*((sin((2*pi/(4*tau)-
2*pi.*k/Td).*t1))./(2.*(2*pi/(4*tau)-2*pi.*k/Td))...

+(sin((2*pi/(4*tau)+2*pi.*k/Td).*t1))./(2*(2*pi/(4*tau)+2*pi.*k/Td)))).
..
    +(offset*Td./(2*pi.*k)).*sin(2*pi*t1.*k/Td))));

figure(2);
semilogx(fS,S2,'b-'), grid on

xlabel('frequency (Hz)');
ylabel('S(f) sinus dBuV');
axis([20e3 100e6 ymin ymax]);

%======================================================================
```

Appendix 2: Hardware circuit