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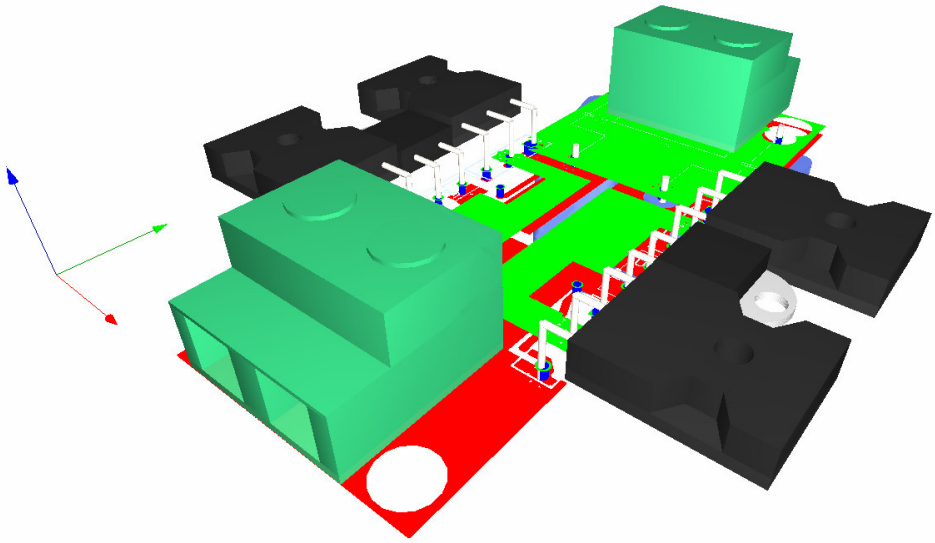

Evaluation of a Halfbridge Configuration Using CoolMOS transistors and Silicon Carbide Schottky Diodes

Master of Science Thesis *of Electric Power Engineering*

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Abstract

In power electronics, MOSFET transistors are continuously being important due to their low switching losses at high frequencies. However, a regular power MOSFET suffers from a relatively low breakdown voltage. In the late 1990's the super junction MOSFET transistor was launched. It combines the low on state losses of an IGBT and the low switching losses of a MOSFET. In this project CoolMOS transistors from Infineon Technologies has been used. These are based on the super junction topology.

The purpose of this project was to design, build and evaluate a two quadrant step down DC/DC converter with CoolMOS transistors and silicon -carbide Schottky diodes as free wheeling diodes. Based on the results, conclusions will be made about the transistor topology's suitability for a high power application, for instance in a hybrid vehicle.

Because of the structure of the CoolMOS, a diode has been put in series to prevent the current to flow in the negative direction through the transistors during its off state. From the simulation and measurements, the basic function of the two quadrant step down converter circuit is verified.

The main problem with the circuit is the stray inductance in the wires and the capacitance in the series diode and transistors. These phenomena result in transients of the current through the transistors and in the voltage across the transistors.

To prevent the transients, tighter design to minimize the stray inductance and capacitance must be achieved. An alternative is to construct a snubber to minimize the transients.

The features of the CoolMOS are suitable for high power application due to its low losses. In such an application the bridge should be built as a single chip for optimal design and usability.

Preface

The rapid development in hybrid electric vehicles of today, has opened the automotive industries eyes for power electronics. In automotive applications, properties such as size and efficiency are more important than in many other applications. With a direct influence on aspects like effective range and driving economy, improvements of power electronic inverters are indeed an interesting area of investigation.

The CoolMOS is a relatively new type of semiconductor switch, combining the low on state losses of an IGBT with the low switching losses of a traditional power MOSFET. In this report the suitability for CoolMOS transistors in bridge configurations, such as inverters, is investigated.

The work has been performed on request by the group of automotive hybrid technology at Caran AB in Göteborg. We would like to express our gratitude to the company and especially our tutor Karin Davidsson for feedback and the opportunity to work with her.

This report is a master of science thesis at the department of energy and environment, Chalmers university of technology. The work has been carried out from September 2006 until February 2007 and represents 20 weeks of full time studies. The authors would like to thank the examiner Torbjörn Thiringer, professor in applied power electronics at the department of energy and environment, for technical support and quick feedback. Another acknowledgement goes to research engineer Robert Karlsson at the department of energy and environment for his help with the PCB design and result analysis.

One special thanks goes to Richard Möller at Infineon Technologies for providing the samples of CoolMOS transistors and SiC schottky diodes.

Göteborg, February 2007

Björn Öhnell and Mats-Åke Isaksson

Symbol and Acronym Dictionary

AC	Alternating Current
D	Duty ratio
DC	Direct Current
EMI	Electro Magnetic Interference
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PWB	Printed Wiring Board
PWM	Pulse Width Modulation
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis

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1 Introduction

1.1 Background

MOSFET transistors are continuously being an essential part of power electronic components due to the low switching losses at high switching frequencies. However, the traditional power MOSFET suffers from a relatively low source to drain breakdown voltage. In 1998, the CoolMOS transistor was launched by Infineon Technologies. These devices are capable of blocking a considerably higher source to drain voltage, and virtually combine the low on-state resistance of the IGBT with the low switching losses of the MOSFET. Today these devices are available in different versions rated up to a breakdown voltage of 800V with very low on-state losses and capable of handling high switching frequencies because of their low gate capacitance.

In 2004 it was declared that the CoolMOS technology in combination with silicon carbide Schottky diodes will be a crucial milestone in the development of high frequency power conversion. The two components extremely fast switching and quick reverse recovery make way for high switching frequencies (Lorenz, 2006).

The efficiency of the drive system for a hybrid electric vehicle is of great importance for the overall energy consumption in the vehicle; therefore, it is vital to minimize the losses in the inverter supplying the electric motors with power. Traditionally, MOSFET transistors have been used in applications where there is a need for high switching frequencies because of their low switching losses. When moving towards higher voltage, the on state losses become too high in traditional power MOSFET design.

Now, when the system voltage has passed the limit for the traditional MOSFET, the CoolMOS could be a suitable choice.

1.2 Purpose and Goal

The purpose of this report is to design, build and evaluate a two quadrant step down converter with CoolMOS technology and to identify problems in the different parts. Based on these results the problems are to be explained and if possible solved. Some of the different aspects that are to be evaluated are efficiency, electro magnetic interference, possible switching frequency and the use of snubber circuits.

Eventually a goal is to simulate and evaluate a full scale model of the motor drive for a hybrid vehicle system using CoolMOS transistors. In this application, a full bridge DC to AC inverter is to be used in simulations.

1.3 Previous Work

Since the CoolMOS transistor was introduced in 1998 a lot of work has been done to investigate this transistor. Several papers have been presented about the construction of the device (Lorenz, 1999) and its features. A key issue in these articles has been the difference between the CoolMOS transistor and a common MOSFET transistor for high-voltage applications (Claudio).

Due to the structure of the CoolMOS transistor, work has been done in minimizing the recovery effect (Hongrae). The poor recovery effect in hard switched inverters of the

CoolMOS transistor are studied and also how to minimize these effects.

By combining a fast CoolMOS transistor with a SiC Schottky diode several advantages can be reached for power electric devices (Lorenz, 2006).

2 Background Needed

This report is to be comprehendible also for people without substantial knowledge about power electronics. In this chapter, a thorough introduction to the concept is presented to give the reader some amount of understanding of the problems involved.

2.1 Hard Switching and Power Electronics Fundamentals

There are three major advantages in using a switch mode voltage source compared to a linear version. First, and most important, is that the efficiency is higher. Due to that the losses are lower; there is less need for cooling and heat resistant components. This means that the size of a heat sink can be smaller. The third advantage is that by designing different topologies of converters, an output voltage that are both higher and with reversed polarity compared to the input voltage can be created.

In the switched mode power supply the transistor is operated as a switch. By switching either on or off a primary voltage at a high frequency, and filter the output through an inductance, an output voltage of a different amplitude than the input voltage can be achieved. The typical way to control the on and off time for the transistor is by using pulse width modulation, PWM. PWM patterns are generated typically by comparing a reference voltage with a saw tooth wave and, depending on whether it is higher or lower, the PWM wave is set high or low as seen in Figure 1. Depending on the frequency of the switching, different kinds of EMI, electro magnetic interference is created. Normally, it is desired to keep the frequency above 20 kHz in order to make it inaudible for humans.

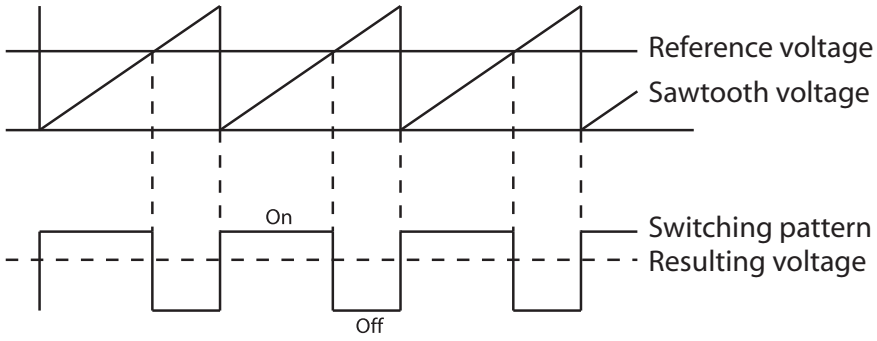

Figure 1 ***Creating PWM switching pattern***

When using switches to form and transfer energy, the electronic devices are required to operate as close to ideal switches as possible, acting as a short circuit when conducting and an open circuit when turned off. It is also important that the turn on and turn off time are as short as possible to minimize losses. The simplest form of converter is the step down or “Buck” converter. This can be seen in Figure 2.

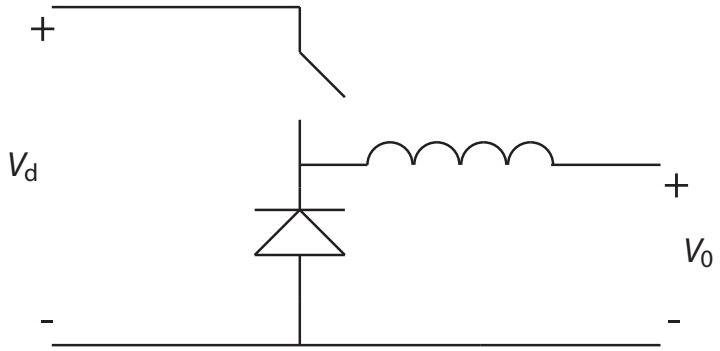

Figure 2 ***Buck converter***

2.2 The Two Quadrant DC/DC Converter Topology

The two quadrant DC/DC step down converter makes it possible, unlike the Buck converter, to have power flowing in both directions. This is a useful feature when supplying active components, such as DC motors and batteries (battery chargers). Since the converter is designed like one phase leg in a three phase motor inverter, it is also possible to investigate the switching properties for the inverter by using this topology. The setup can be seen in Figure 3.

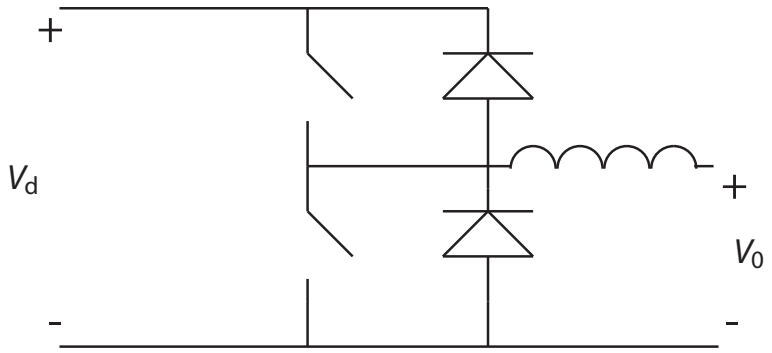

Figure 3 ***Two-quadrant DC/DC converter***

When operating the converter in the first quadrant, with positive power flow and positive voltage, only the upper transistor and the lower diode are conducting, exactly as in a normal step down converter. When, on the other hand, the voltage on the secondary side grows larger than the supposed output voltage, the current will change direction and reverse the power flow. Now the lower transistor and the upper diode will be acting as a step up converter in the opposite direction, pushing the current towards the higher input voltage.

There are a number of new features that need to be implemented in the two quadrant design. Most important is maybe the blanking time. Since the two transistors in series are the only object blocking the input voltage and preventing a short circuit, it is of vital importance that they never are conducting at the same time. To prevent this, there is a short time when none of the transistors are conducting. This time period is called dead band or blanking time and is typically in the length of a few micro seconds.

The output voltage from a two quadrant DC/DC converter is calculated by using the fact that the sum of the voltage across an inductor must be zero over one period. In (1) the output voltage as a function of the input voltage and duty cycle is derived.

$$\int_0^{DT}(V_d - V_0)dt + \int_{DT}^{T} -V_0 dt = 0 \Rightarrow V_d D = V_0 \quad (1)$$

2.3 Full Bridge Switch-Mode DC/AC Inverter

Unlike the two quadrant DC/DC converter, where the output voltage is positive, the full bridge inverter can operate in all four quadrants. This means that the output voltage and current can be both positive and negative. In a hybrid electric vehicle an AC motor is used for propulsion, so the DC voltage from the batteries needs to be converted into AC voltages and currents. The full bridge DC/AC inverter converts the DC voltage to a controllable AC voltage and current with variable frequency. A single phase full bridge inverter topology can be seen in Figure 4.

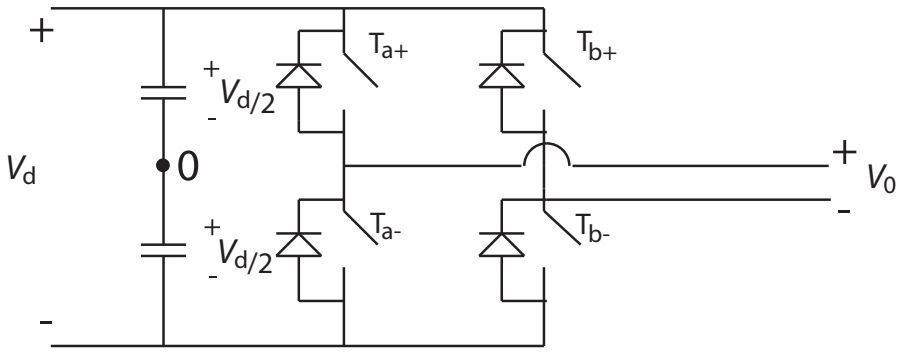

Figure 4 ***Single phase full bridge inverter***

As seen in Figure 4, two equally sized capacitors are placed at the voltage source giving half input voltage across each capacitor. The transistors are then switched in pairs, (Ta+ and Tb-) and (Ta- and Tb+), giving either a voltage the input voltage or minus the input voltage.

In order to create an AC voltage, the switching pattern must be created in a different way than with the DC/DC converter. Instead of having a constant control voltage the control voltage is sinusoidal with the desired output frequency. As a result the output voltage varies with the sinusoidal control voltage. The PWM switching and the output voltage can be seen in Figure 5.

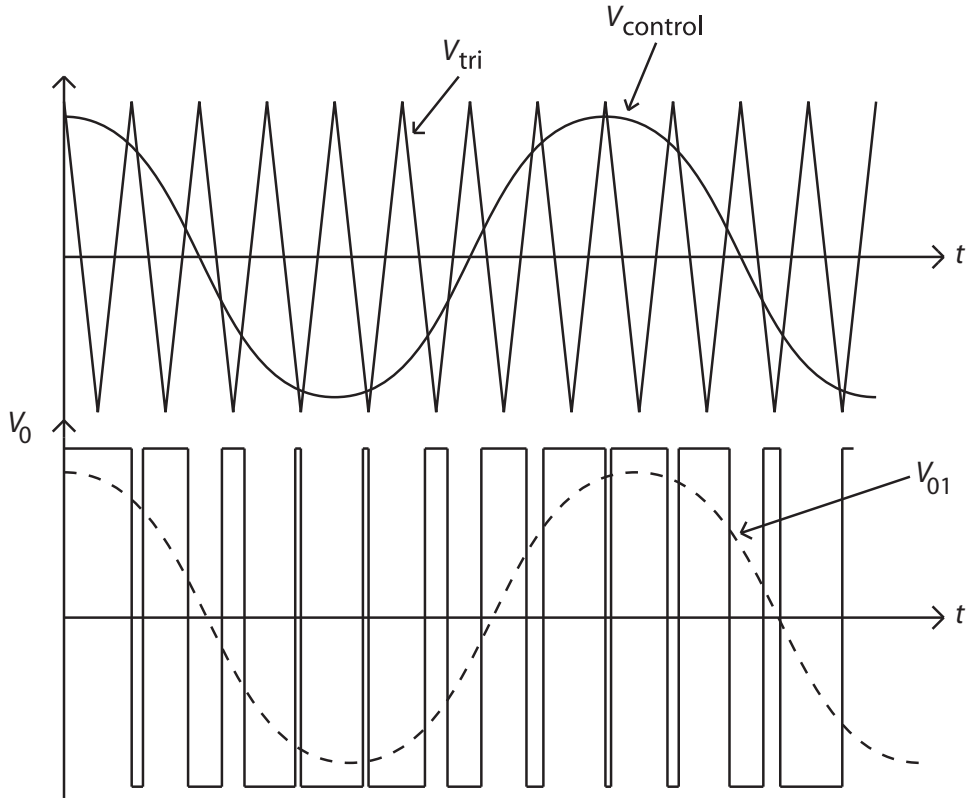

Figure 5 ***PWM switching with sinus control voltage and output voltage***

As can be seen in the lower part of Figure 5, a fundamental voltage can be extracted from the output voltage. A filter is then used to demodulate the switching pattern into the fundamental voltage.

Since an AC motor often runs on three phases, a three phase inverter is needed. One basic setup can be seen in Figure 6.

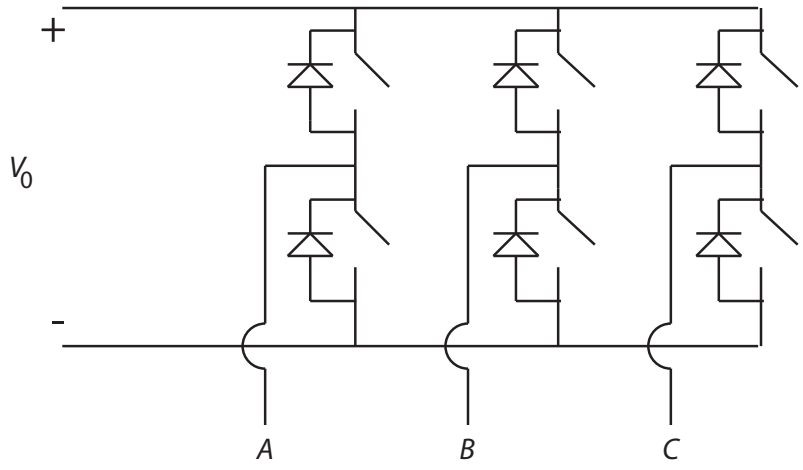

Figure 6 ***Three phase inverter***

The control voltages then consist of three sinusoidal voltages 120 degrees displaced in time in steady state. The output voltages between A-B, B-C and C-A then acts like single phase

voltages, only displaced 120 degrees in time.

2.4 Snubbers

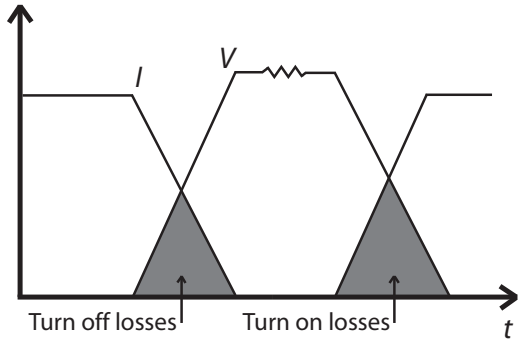

Figure 7 ***Switching losses***

In theory a switch or a transistor is turned on and off instantaneously. This means that the current is turned on and off immediately and no switching losses occur. In reality this is not true; the switch needs some time to turn off and on. The overlapping periods can be seen in Figure 7. In order to move these losses away from the transistor, a snubber circuit can be used.

Snubber circuits are used to improve the shape of the switching waveforms around the transistor or switch in power electric devices. There are a number of different types, all with their specific purpose and design aspects.

2.4.1 Overvoltage Snubber

One phenomenon that results in the need for a snubber is the stray inductance in the conductors. The inductance cause over voltage transients acoss the transistor when the switch is turned off. The inductance pushes extra current into the switch, resulting in voltage spikes when the switch is turned off. To solve this problem a snubber circuit called an overvoltage snubber can be implemented. The overvoltage snubber design can be seen in Figure 8.

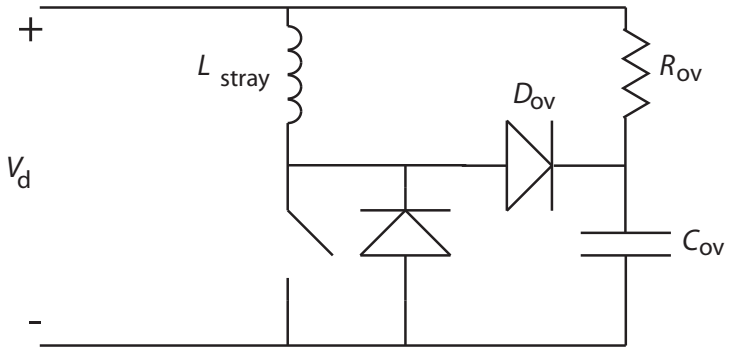

Figure 8 ***Overvoltage snubber***

Initially the voltage across the capacitor is V_d. Then the transistor is turned off. Now the energy in the stray inductor is transferred through the diode to the capacitor. The voltage across the capacitor will then increase. When the current from the stray inductance is zero, the capacitor will discharge down to V_d through the resistance. By having an overvoltage snubber

the extra voltage will be much lower than without one, and therefore cause less stress to the switch.

2.4.2 Turn Off Snubber

During turn-off the current must decay to zero and the voltage must rise up to its full value. This process is not instantaneous which leads to losses in the transistor. Because of the losses the temperature of the transistor is increased which deteriorates its performance.

The goal of the turn-off snubber is to provide a zero voltage across the switch while the current turns off and thereby minimizing the switching losses. This is easily done with a RCD network seen in Figure 9.

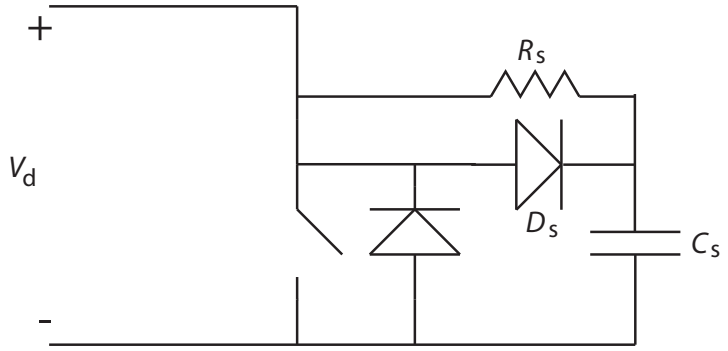

Figure 9 ***Turn-off snubber***

At turn-off the transistor current decreases with a constant *di/dt* and the remaining current flows into the capacitor through the diode. The capacitor voltage, which is the same as the voltage across the transistor as long as the current flows through the diode, is being built up at a slow and controlled rate. With an appropriate value of the capacitor, the full voltage is reached at the same time as the current has decayed to zero. During turn-on the voltage drop across the transistor takes more time due to the turn off capacitor. To prevent that the transistor takes up all the losses, the turn-off resistor dissipates all the energy from the capacitor. The resistor has the following beneficial effects:

- In theory, all the energy in the capacitor is dissipated in the resistor, which is much easier to cool than the transistor.
- No additional energy dissipation occurs in the transistor due to the turn-off snubber.
- The peak current the transistor must conduct is not increased due to the turn-off snubber.

Both the overvoltage snubber and the turn-off snubber should be used simultaneously (Mohan).

2.4.3 Turn on Snubber

The turn-on snubber is only used to reduce turn-on switching losses at high frequencies and to reduce the reverse recovery current in the free wheeling diode because of the large forward bias safe operating area in transistors. Turn-on snubbers work by reducing the voltage across the transistor as the current is being built up. The turn-on snubber circuit can be seen in Figure

10.

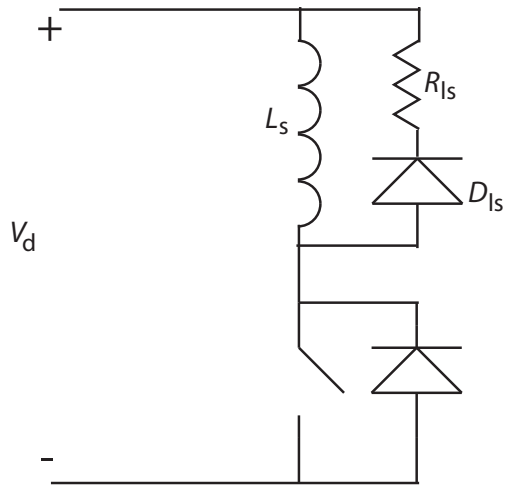

Figure 10 ***Turn-on snubber***

The reduction of the voltage across the transistor during turn-on is due to the voltage drop across the inductor. If the minimization of the reverse recovery current is important a large value of the inductor is necessary. Thus the voltage across the transistor is almost zero during the current rise time. During on-state, the inductor conducts the full load current. When the transistor turns off, the energy in the inductor will be dissipated in the snubber resistor. A large inductor value will result in lower turn-on voltages and lower turn-on losses, but will also result in higher over voltages during turn-off, lengthen the minimum off-state interval and result in higher losses in the snubber. Therefore the inductor and resistor must be selected with great precautions. Since the inductor must carry the full load current, the turn-on snubber will be expensive and large.

2.4.4 Snubbers for Bridge Configurations

The overvoltage, turn on and turn off snubbers are not only to be used separately but can be implemented simultaneously. Especially for bridge configuration it is good to use them for reducing the losses in the transistors. A full scheme for a half bridge converter with all three snubbers is shown in Figure 11.

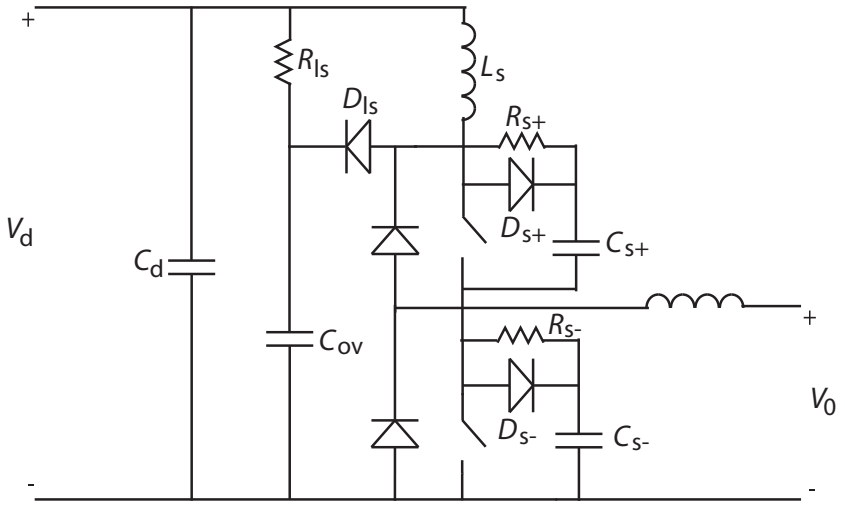

Figure 11 ***Half bridge with snubber configuration***

In this configuration there are many components and the circuit design becomes complex. A reduction to a simpler arrangement can be made, the Undeland snubber for bridge configurations, which can be seen in Figure 12.

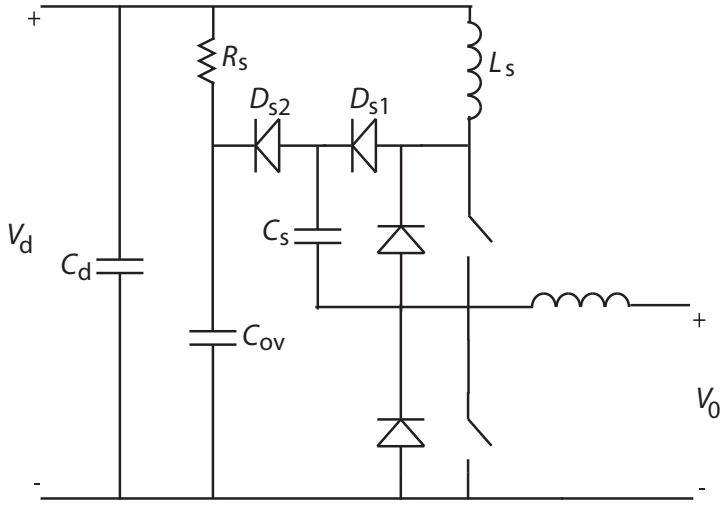

Figure 12 ***Undeland snubber for half bridge configuration***

2.5 MOSFET/CoolMOS

2.5.1 Traditional MOS Technology

Ever since Shockley and Bell Labs invented the metal-oxide-semiconductor field-effect transistor (MOSFET), it has been the most common field-effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material depending on doping level of electrons or holes.

A MOSFET is based on the modulation of charge caused by a MOS capacitance. It contains two terminals (drain and source) which are connected to a highly doped region. The region can be of N-type or P-type depending on which transistor that is used, but the drain and the source must be of the same type. The two highly doped regions are separated by a lower

doped region of opposite type, which is called the body. A third electrode, the gate, is located above the body with an oxide insulating the gate from all other regions. This oxide provides the MOS capacitance. The cross section of a MOSFET can be seen in Figure 13.

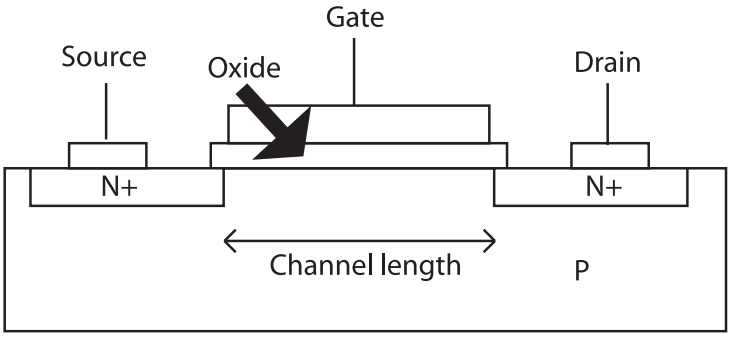

Figure 13 ***Cross section of MOSFET***

When a voltage is applied to the gate, positive if the MOSFET is an N-channel or nMOSFET, electrons from the body creates a channel between the source and the drain just under the oxide. The channel stretches from the source to the drain providing conductivity to the transistor. This allow current to flow between the source and the drain. When the gate voltage is set to zero or negative the channel closes and no current can flow. For a pMOSFET a negative voltage should be applied to the gate and the channel consists of holes. In an nMOSFET, the drain and source are doped to have an excess of electrons (N^+) with a less doped body of holes (P). The opposite should yield if the transistor is a pMOSFET.

2.5.1.1 Operation of the MOSFET Transistor

In order to create a channel, a certain gate voltage must be applied. This voltage is called the threshold voltage (V_{TH}). If the gate voltage is lower than the threshold voltage, the transistor is turned off. Although, there is always a small leakage current that depends on an exponential function of the gate-source voltage (V_{GS}). This phenomenon is sometimes called the sub threshold leakage.

If $V_{GS} > V_{TH}$ the transistor turns on. Now, if the drain-source voltage (V_{DS}) < V_{GS} - V_{TH} a channel has opened and current can flow through the transistor. The MOSFET now operates as a resistor and is controlled by V_{GS}. The transistor is now in the ohmic region. The current depends on V_{GS} and V_{DS}. A cross section of the MOSFET transistor in the ohmic region is shown in Figure 14.

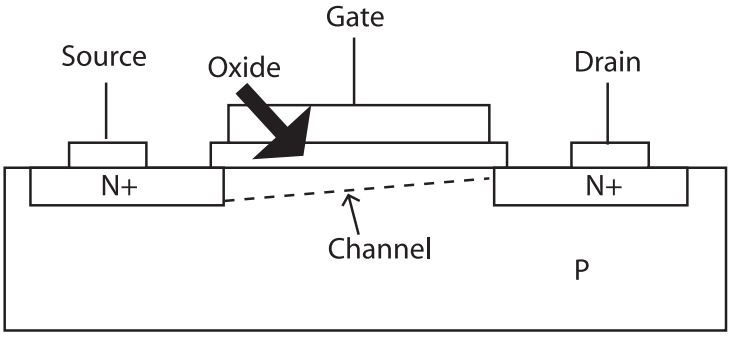

Figure 14 ***MOSFET in the linear region***

When $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS}$-V_{TH}, the transistor goes into the active region. Since the drain-source voltage is higher than the gate voltage a bit of the channel is removed. The current through the transistor is now only depending on the gate voltage. A cross section of the transistor in saturation is shown in Figure 15.

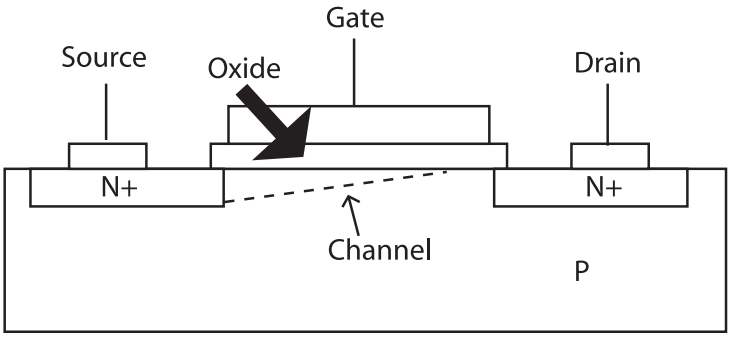

Figure 15 ***MOSFET in saturation***

Figure 16 shows the drain current with the drain-source voltage for several gate voltages.

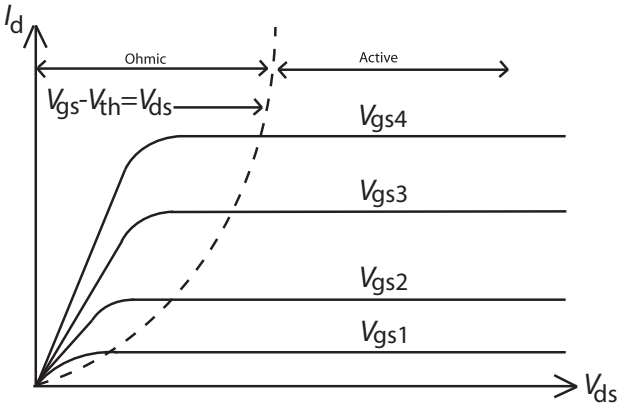

Figure 16 ***Vgs vs. Vds of the MOSFET***

2.5.2 POWER MOSFETs

A power MOSFET has a different structure compared to a regular MOSFET. The structure of a power device is vertical and not planar as a common semiconductor device. This can be seen in Figure 17 where the drain is placed under the drift region.

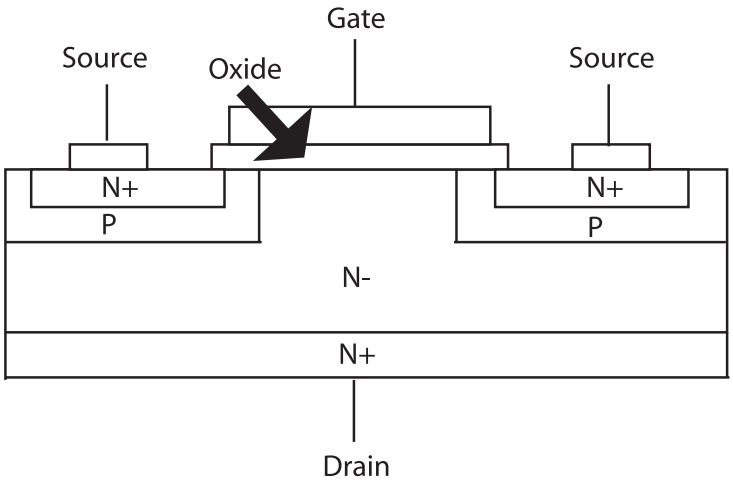

Figure 17 ***Cross section of a power MOSFET***

By using a vertical structure it is possible for the transistor to have a high blocking voltage and a high current flowing through it. In a planar structure the current and the breakdown voltage is a function of the channel size. In a vertical structure the breakdown voltage is proportional to the thickness and doping of the drift region. In order to get a higher breakdown voltage, the layer must be thicker and the doping reduced. This results in a higher on state resistance for the device causing higher losses.

2.5.2.1 On State Losses

When the power MOSFET is turned on it behaves as a resistor between the drain and the source, R_{DSON} . In Figure 18 the different resistances that adds up to R_{DSON} can be seen.

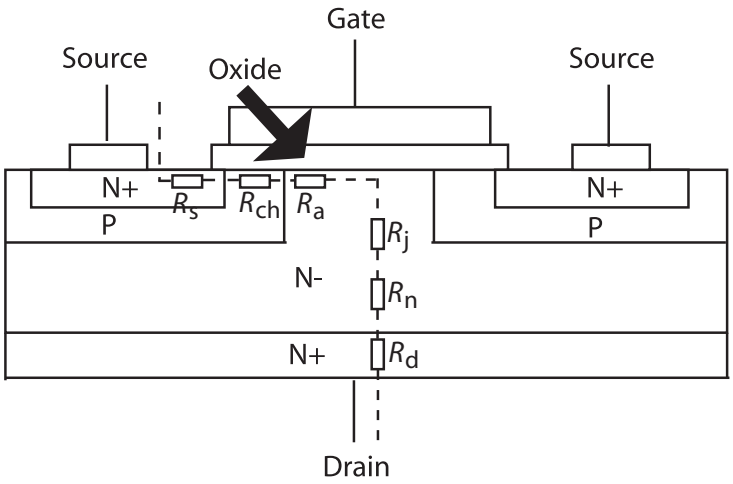

Figure 18 ***On state losses of the power MOSFET***

As can be seen in Figure 18, R_{DSON} consists of several components. R_S is the source region resistance, R_{CH} is the channel resistance, R_A the accumulation layer resistance, R_J the JFET component-resistance of the region between the two body regions, R_N the drift layer resistance and R_D the drain region resistance.

When the power MOSFET is in off-state it is equivalent to a diode. The lightly doped drift

region results in a high breakdown voltage. When the power MOSFET is in on-state, the low doping of the substrate gives a high resistivity and high on-state losses. A thicker and lower doping level of the layer results is a higher breakdown voltage. But at the same time, a thinner layer and a higher doping level means a smaller $R_{DSON.}$ This leads to lower on-state losses. So, a trade-off between breakdown voltage and on-state losses has to be made.

2.5.3 CoolMOS

The super-junction MOSFET or CoolMOS was introduced in the late nineties. A huge drawback of the power MOSFET has been the large on-state resistance. The drift region with a low doping was necessary to have a large breakdown voltage, but at the same time led to low conductivity. In a CoolMOS the drift region is smaller and the doping is higher but still the component has the same breakdown voltage. The conduction losses in a CoolMOS can be as low as one fifth that of the regular power MOSFET for the same voltage level.

The basic structure of the CoolMOS is the same as the regular power MOSFET. The main difference is that a CoolMOS has n^- or p^- strips parallel with the drift region. The different structures of a CoolMOS and a MOSFET can be seen in Figure 19.

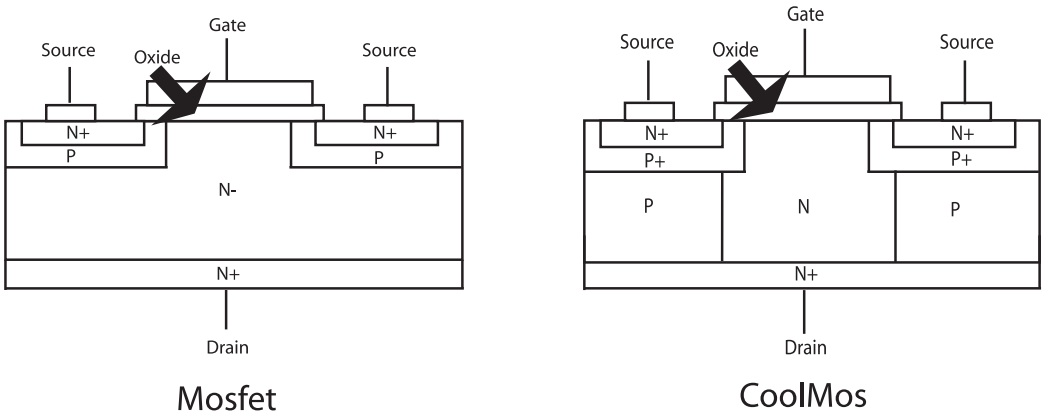

Figure 19 ***Cross section of power MOSFET (left) and CoolMOS (right)***

The strips in parallel with the drift region does not contribute during the on state, but are essential for achieving high breakdown voltage of the transistor despite the higher doping of n and p regions. When the transistor is reversed biased, a large p-n junction builds the electrical fields in both vertical and horizontal direction allowing the breakdown voltage to be high. It is although necessary that the net charge is in balance between the doping of the strips and the drift region. A higher doping in any of the regions leads to a decrease of the breakdown voltage. With this kind of structure the doping of the drift region can be higher and the drift region smaller leading to higher conductivity and a lower on-state resistance.

2.5.3.1 Advantages/Disadvantages

The main advantage of the CoolMOS compared to a regular power MOSFET is the lower on state resistance (R_{DSON}). The on-state resistance can be as low as one fifth of a MOSFET. Another advantage is that the gate charge can be reduced by a factor of three versus a MOSFET with the same on-state resistance. This major advantage allows a much higher switching frequency and lower overall losses.

A disadvantage of the CoolMOS compared with a MOSFET is the reverse recovery current.

Due to the structure, the inserted plasma in on-state must be removed before the p-n junction can support a substantial amount of blocking voltage. This leads to a high reverse recovery current. A low drain source voltage V_{DS} also leads to high capacitances between drain source C_{DS} and drain gate C_{DG}. At higher V_{DS} these capacitances are lower than in a MOSFET which leads to lower switching losses.

A low gate charge is very critical when it comes to switching losses. A lower gate charge means lower switching losses and faster switching.

As a result, CoolMOS transistors can be operated with the lowest control power, the cheapest driver circuits and the highest frequencies.

2.6 Schottky Diode

The schottky diode is a semiconductor device with relatively low voltage drop and very fast switching action. These properties make it suitable for power switching applications, allowing both low conduction losses and good switching performance.

The function of the diode is based on one Schottky barrier, a certain type of metal semiconductor junction as seen in Figure 20. The rectifying properties of the junction depend on the metals function, the band gap of the intrinsic semiconductor, the type and concentration of dopants in the semiconductor. In case no rectifying properties are desired, the junction is called ohmic, meaning that the voltage drop across the junction is proportional to the flowing current.

The Schottky barrier is formed by applying one thin film of metal upon a semiconductor. When being this close together, electrons will move from the metal into the semiconductor and vice versa. However, since the energy needed for the electrons to escape the metal is significantly higher than for the semiconductor, more electrons will flow into the metal. This results in a negative charge in the metal and a positive charge in the semiconductor, causing a dipole like the one found in a p^+n-junction. This dipole will cause electrons to drift in the opposite directions at a rate depending on the difference in potential and eventually the drift and diffusion will come to a steady state. The potential difference achieved in this process will behave similar to the p^+n –junction in a normal semiconductor diode.

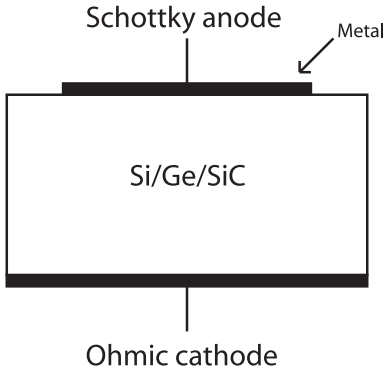

Figure 20 ***Cross section of the Schottky diode***

2.6.1 Forward and Reverse Bias

When a positive bias is applied to the metal –semiconductor junction, the Fermi energy of the

metal is lowered compared to the semiconductor. This will cause more electrons to diffuse towards the metal than the number drifting towards the semiconductor. This means that when the forward bias is higher than the built in potential, there will be a resulting current flowing through the junction.

When a reverse voltage is applied, the Fermi energy of the metal side will increase. The potential across the barrier will now increase, causing a larger depletion region and a stronger electric field in the device. Because of this, regardless of the magnitude of the applied reverse voltage, the current flow through the junction is limited, resulting in a rectifying behavior.

In this report a normal silicon schottky diode will be compared to one silicon carbide schottky diode. The silicon carbide diode is with the latest thinQ 2G technology from Infineon Technologies.

2.7 Drive Circuit

The basic function of a drive circuit is to switch the power semiconductor device between the on- and off-states. The drive must also be able to keep the switch on or off. In the case with a MOSFET switch, this means that the gate voltage must be kept constant. To optimize the use of a switch, it is of vital importance that it can be controlled properly. Several important aspects, such as switching speed and on-state losses, depends on proper control. The drive circuits basic task is to convert the logical control signal into enough electrical power to turn the switch on or off properly. The current needed to switch is proportional to the switching frequency because the gate capacitor needs to be charged and discharged once for each switching period.

There are three basic functional considerations for drive circuits. First, it is a big difference whether a unipolar or bipolar drive is needed. The unipolar version benefits from a simple design and few components, but sometimes a bipolar drive is needed for high switching speeds. The second consideration is if there can be an electrical connection between the logic level and the power switch or if they must be electrically isolated. Third, decision has to be made whether the drive will be connected in series or parallel with the switch. These are of course basic considerations and when the requirements for the switch increase, so will the complexity of the drive.

More complex switch setups such as bridge circuits require some additional features in the drive circuit, such as blanking time to make sure that only one switch in each pair is conducting at a time. Also, since it is the gate-source voltage that controls the gate, it will require an offset off approximately the DC source voltage when the upper transistor is conducting. Most drive circuit ICs for bridge operation have built in functions to boost the output control voltage to an appropriate level.

Today there are many power switches with built in drive circuits, making it possible to connect the switch directly to a logic circuit or a micro processor.

2.8 SPICE

2.8.1 Simulation

The main circuit described in this report have a very comprehendible main purpose. It is designed to convert one level of voltage to a lower one. During its operation, there will be a

lot of secondary phenomena taking place in the circuit. To be aware of these phenomena and to avoid serious issues at an early state, a program for simulating the circuit is a valuable tool.

When simulating a circuit, there is a good chance of identifying design errors and mistakes before the circuit have been completely manufactured and ready for testing. Many of the currents on a board might be difficult to measure, while adding another probe to the simulation model presents no problem.

Depending on the level of complexity in the used models, the results from the simulations can be very accurate. By replacing the more complex models with ideal components one by one, it is possible to identify the part responsible for a certain event.

2.8.2 History

Simulation Program with Integrated Circuit Emphasis, SPICE, has its origin in the University of California, Berkeley. It was mostly a derivative of the CANCER program presented by Ronald A. Rohrer in a paper from 1971. Today SPICE with graphical interfaces for circuit design is available in many commercial versions for most platforms. One of them is PSpice which was originally designed by MicroSim, later on by Orcad and today it is a product by Cadence Design Systems.

2.8.3 Orcad

Orcad PSpice is a powerful package of tools for both simulating and modelling but also for designing PCB circuit boards. There is an evaluation version available which can be freely distributed. The free version is however limited regarding circuit board design and size of the schematics. The possibility to go from simple ideal circuits and then improve the complexity to observe new phenomena is truly a great advantage when designing and optimizing circuits.

The circuit for the simulation is created as a netlist file in which all of the components and connections are listed. The program then takes input from the file and sets up equations to be solved. The general equations produced are nonlinear differential algebraic equations which are solved by the program. The result is then presented as graphs showing voltage and current in selected nodes.

For the simulations, OrCad Pspice lite version 9.2. and OrCad Pspice 10.5 have been used.

2.9 PCB

A PCB, or printed circuit board, is used to mechanically and electrically connect electric components using conductive pathways, usually copper on a non-conductive substrate. Alternative names are printed wiring boards or etched wiring boards.

PCBs are inexpensive and highly reliable, although they require much more work with the layout of the board and a higher initial cost than both wire-wrapped and point-to-point constructed boards. In the two latter cases wires are drawn from the components to the next point. This means that a lot of wires must de drawn across the board creating a lot of stray inductance. In switched applications it is crucial to keep the inductance low, so a wire-wrapped or point-to-point construction will lead to poor results. Another advantage by using a PCB is the possibility to have a ground layer all over the board to further reduce the number of conductive traces and lower the inductance.

A PCB is composed of one or many conductive layers. The layers are separated and supported by an insulating non-conductive substrate. In this project a two layer PCB is used. The layers can be connected together with a drilled hole called a via. These vias can be connected on both sides, one side, called blind vias, and on neither side, called buried vias.

The common modes of manufacturing a PCB is by gluing a copper layer on the substrate, sometimes both sides, and then remove the unwanted copper, leaving the desired copper traces.

Because bare copper oxidizes quickly and are therefore not easily solderable, via holes are often plated with silver, gold or gold over nickel. Around the plated via, a solder resist is places to prevent short circuits to nearby component leads.

Text or line art can also be printed on the board. This is called the silkscreen layer. It can be used to print components on the board so it is easy to know where to put them.

2.10 CADint PCB

To go from circuit schematic to PCB layout, a software called CADint PCB was used. This programs main feature is to create cad drawings of the PCB board, either by starting from a schematic or by designing the PCB layout directly. The software is provided by a company called Cadint Sweden and was first released in 1983.

The idea of the program is to create the parts needed, both as schematic blocks and as actual size connections. Thereafter, the circuit schematic is drawn using the created symbols. From the schematic, the parts and connections can be exported to a PCB layout. Here, the user has to put the components in position and connect them through conductive copper layers. The connections needed are imported from the schematic and shown as yellow lines when they are unconnected. In this way it is fairly simple to get a good overview and make sure that everything is connected even in large and complex designs.

When the design is completed and ready for manufacturing, it is exported to a manufacturing standard file format. Often there will be one file for each layer and another one for each type of holes to be drilled. A common format is the Gerber and Gerber extended which is more or less standard in the PCB manufacturing business.

Besides from creating a PCB layout suitable for manufacturing, there is a feature that allows the user to examine the layout in 3D. By creating the components in special package layers, the circuit can be seen in its final form. This is useful both for verifying that there is enough space, but also for getting a good overview when presenting or explaining the circuit.

2.11 CoolMOS Transistors in an Electric Drive Train

All electric drive trains, regardless the type of electric machine involved have one thing in common. There must be some way to control the produced mechanical power. In traditional electric vehicles, such as trams and subways, the power was controlled with large resistors. This is a very inefficient way to control the vehicle, similar to controlling the speed of a car using only the brakes at full throttle.

In modern electric drive trains the outdated DC machines have been replaced by AC machines. These machines benefit both from their higher efficiency, but also as they need less

or none maintenance. Typically these machines are permanent magnet synchronous machines, asynchronous machines or brushless DC machines.

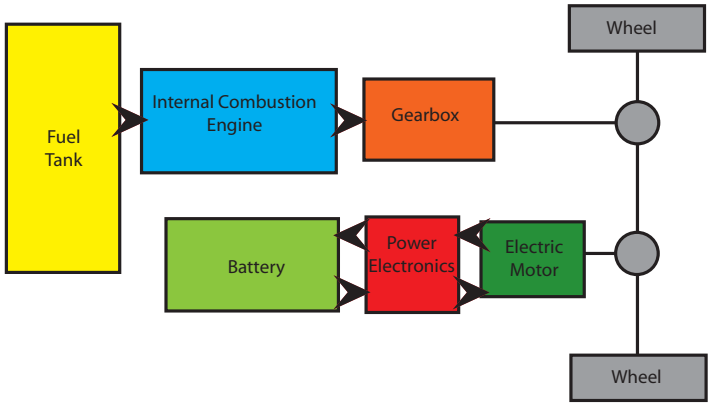

Figure 21 ***Parallel hybrid electric drive train***

The way to use and control these machines is through power electronic inverters. In this device the DC from the battery is converted into AC with a suitable frequency, amplitude and number of phases. With this type of equipment the electric motors behaviour can be controlled with high accuracy. The basic setup for a parallel hybrid electric drive train can be seen in Figure 21.

The most essential component in an inverter is the transistor, or switch. Properties such as overall efficiency and maximum power depend directly on the type of component used. With this in mind, the low losses of the CoolMOS seem like a favourable choice, and will be further investigated in this report.

3 Simulation, Measurements and Results

3.1 PCB Design

The size of the board where decided at an early stage due to limits set by the first manufacturer. Later on, when another board manufacturer where selected, there were no reason to change the size. The size where selected to 160 by 100 mm on which two different main boards and one drive circuit where fitted. On one of the main boards, connections were made for a possible implementation of an Undeland snubber as seen in chapter 2.4.4. The final PCB design can be seen in Figure 22 and the manufactured PCB can be seen in Figure 23.

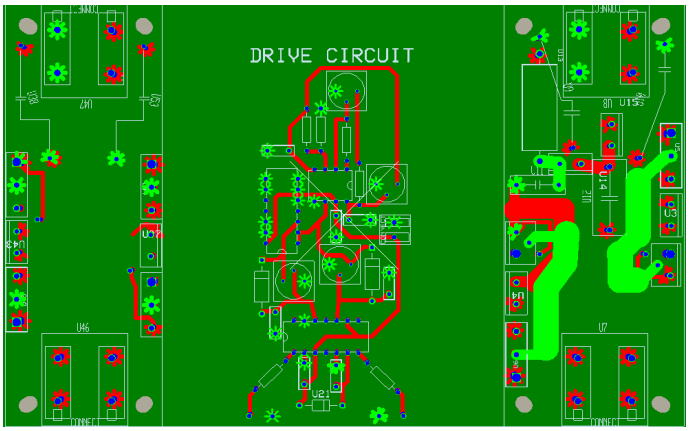

Figure 22 ***PCB layout with both side copper layers and silk screen as seen in CADint PCB***

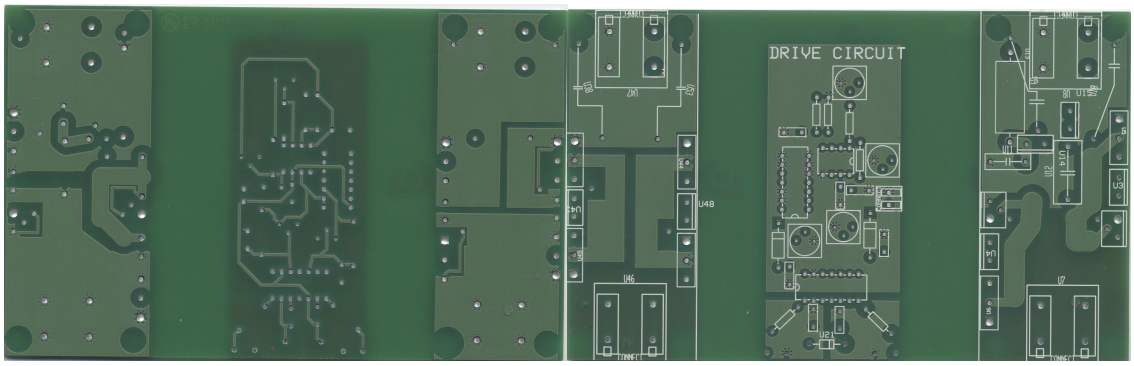

Figure 23 ***The PCB card as received from the manufacturer. Bottom layer (left) and top layer (right)***

3.1.1 Main Board

The board was divided into two main parts. One main board with the actual half bridge, and one drive circuit board with the control signal logics.

3.1.1.1 Requirements for the main board

- Voltage 300V
- Current 30A

- Switching frequency >100kHz

3.1.1.2 Minimizing Inductance

In switching applications it is very important to minimize inductance in the conductors around the switches. Since inductance will give a "momentum" to the current, the switches will experience problems when trying to break the current. The result of these difficulties can be observed as overvoltage transients across the switch, caused by the current trying to force its way through.

Inductance appears in every electric conductor according to Lenz's law, which is defined as "the induced current produced in the conductor, will always flow in such a direction that the magnetic field it produces will oppose the change that produces it". This means that any change in the current will be opposed by the induced magnetic field. A result from Lenz's law is that if a current is returned in a parallel conductor, the induced magnetic fields will cancel out each other, resulting in a zero inductance.

When designing actual applications, it is not realistic to cancel out all inductance. However, there are a number of things to keep in mind to improve the performance of the circuit. Most important is to keep the design tight. A wire results in approximately 5nH/cm, so a tight design and short component legs will lead to better results.

Another way to remove inductance is to have a ground plane on one side of the board. This will improve performance both by acting as a capacitor with metal plates on each side of a dielectric material, but also by cancelling out the magnetic fields.

3.1.1.3 Component Placing on the main board

The components in the circuit that require cooling are the transistors, the free wheeling diodes and the Schottky diodes in series with the transistors. To be sure that there is enough room for all the heat sinks, these components have been placed lying down along the side of the board. In this way, the heat sinks and fans can be placed downwards and away from the other components. Because there can be up to 300V difference between the different packages, only the component that requires the most cooling must electrically connected to the heat sink. To avoid having a high voltage on the heat sink, all of the components were mounted with galvanic isolation.

3.1.2 Main Board Specifications

The requirements on the board are due to the specifications of the switching transistors and the free wheeling diodes used. However, in order to have a DC supply with enough current available, the maximum testing voltage has been set to 300 V instead of 650 V, which is the specified voltage for the components. In most designs, components are selected to operate at no more than half the rated voltage. With 300 V, the minimum distance between conducting traces must be at least 1.2 mm. Since there is a risk for over voltage spikes, a clearance of 2 mm is used in this design.

The semiconductor components used on the board are in either the TO220 or TO247 packages. To ensure that the voltage can not jump between the legs of the smaller TO220 package, the drain is extracted a few millimetres. This causes the mounting holes to be in a triangle rather than in a line.

The maximum current in the circuit is set to 30A, which is close to the maximum rating of the smallest transistors used.

3.1.2.1 Selecting Copper Traces

With help from tables, the size of the copper traces where calculated. To keep the traces at a reasonable temperature the copper layer thickness must be at least 105µm with traces no less than 6mm wide. These traces will have a resistivity of 0,028 Ω/m.

3.1.3 Drive Circuit

The main task for the drive circuit is to generate a PWM signal and feed this to the transistor gates. The transistors require a gate voltage of at least 10V. For this, a supply voltage of 12V for the drive circuit is suitable, since it can be used both for the logic circuits and the gate voltage. Since the source of the upper transistors oscillates between ground and the DC-link voltage, the ground layer has to be divided into separate parts.

The PWM pattern is created with a PWM generator, where the output varies between either zero or twelve volts. To have full control of the circuit, the frequency and the duty-cycle of the PWM wave must be able to be changed. One potentiometer is used to control the reference voltage which changes the duty-cycle and another potentiometer is used to tune the frequency.

The PWM wave consist of one signal, but since the drive circuit controls two transistors, the signal is split into two parts. One of these signal is then inverted through a NAND circuit so the transistors is switched on and off separately. Since it is crucial that the transistors are not turned on at the same time, a dead-time during which none of the switches conduct is required. This is achieved via a circuit that generates a small delay of the signal at turn on, so the transistors can turn off and on without creating a short circuit. These two signals are then sent to the gate driver to control the switching of the two transistors. The schematic for the entire drive circuit PCB can be seen in Figure 24.

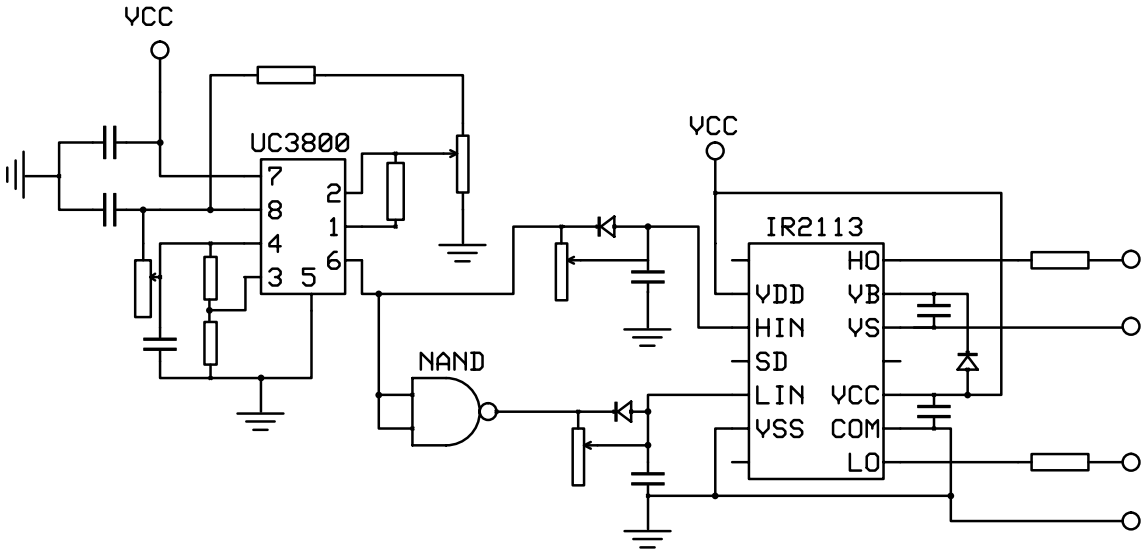

Figure 24 ***Drive circuit schematic***

3.1.3.1 Requirements for the drive circuit board

- Voltage 12V/300V
- Switching frequency >100kHz

3.1.3.2 Component Placing on the drive circuit board

Since the drive circuit is supposed to stand perpendicular to the main board, it is important that the board is kept small. The components need to be close together, but at the same time it must be possible to draw the copper traces. Another aspect is to make the board foreseeable so it is easy to see where the different parts of the circuit are placed. An important layout matter is to separate the low side voltage with the high side. This is done by dividing the ground layer into two separate parts. One for the twelve volts ground, and one for the high side ground.

3.1.3.3 High Side/Low Side/Interface

The drive circuit is connected to the main circuit through four connection pins, two for each transistor. The lower transistor have the source pin connected to ground so it requires no more than 12V to be operated. When the upper transistor is conducting, the source pin will be connected to the DC source voltage. This means that in order to keep the transistor open, the gate voltage must be equal to the high DC voltage plus the required gate voltage. To do this, our gate drive IC uses a boot strap configuration to deliver the high voltage output. The boot strap works by charging a capacitor with the gate turn on voltage during the transistors off time. Then, when the transistor is turned on, the capacitor keeps the gate voltage at the required level.

The four connection pins are put in a line across the main circuit respectively along the short side of the drive circuit. The idea is to put the drive circuit perpendicular to the main board, keeping the gate conductors as short as possible. Because there are separate boards for the drive and main circuits, the high voltage can be well separated from the low voltage logic

parts.

3.2 Simulation

To investigate the dynamic circuit behaviour and function, a circuit simulation program is a valuable tool. In this project Orcad were used for the simulations. It is a great advantage to be able to verify a design before the actual manufacturing of the board. In chapter 3.3.2 the simulated results will be compared with the actual measured values. Throughout all simulations a duty ratio of 50% has been selected. From (1) it can be seen that the output voltage should be half the input voltage.

3.2.1 Initial Simulations

The circuit to be simulated are based on the two quadrant DC/DC converter described in chapter 2.2. The main difference is that extra diodes are put in series with the transistors. To avoid difficult problems setting up the complete circuit in the simulation program and to learn more about the program and its behaviour, the initial tests were performed on an ideal circuit. With ideal switches and no losses in the cables the efficiency was almost 100 percent. As work progressed, more realistic component models were put into the circuit.

Most manufacturers offer free PSPICE models of their components, so these were used in the simulations. These models are more or less simplified, but can still be used for valuable results as long as their limitations are known.

3.2.2 Simulating with Semiconductor Models

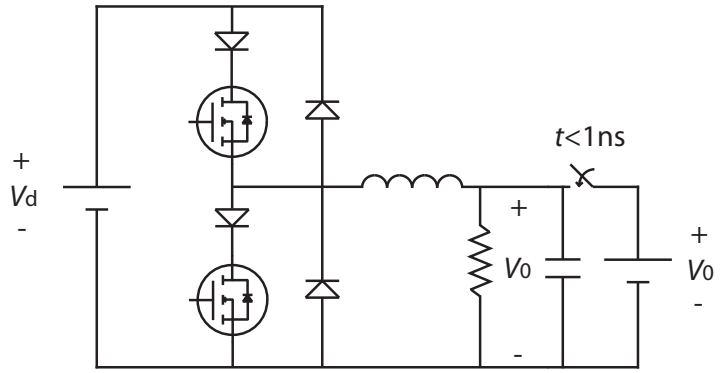

Figure 25 ***Simulation schematics with semiconductor models***

With actual models of the transistors and the SiC Schottky diodes implemented, the main circuit was completed. The schematic as seen in Orcad can be seen in Figure 25. Note the diodes connected in series with the transistors. It could now be tested in the simulation program to see its dynamic behaviour. The goal for the simulation was not to investigate the start up behaviour, but the different voltages and currents in steady state. To shorten the time until the circuit is stabilized the smoothing capacitor on the output is charged with the output voltage instantly. The duration of the simulation is set to 30ms and data is only collected from the last millisecond. In all simulations a maximum step time of 5ns has been used. Due to this limitation some of the quickest transients and oscillations will be somewhat distorted. In Figure 26 the voltage across both transistors can be seen while feeding the circuit with 300V and a load of 50 ohm.

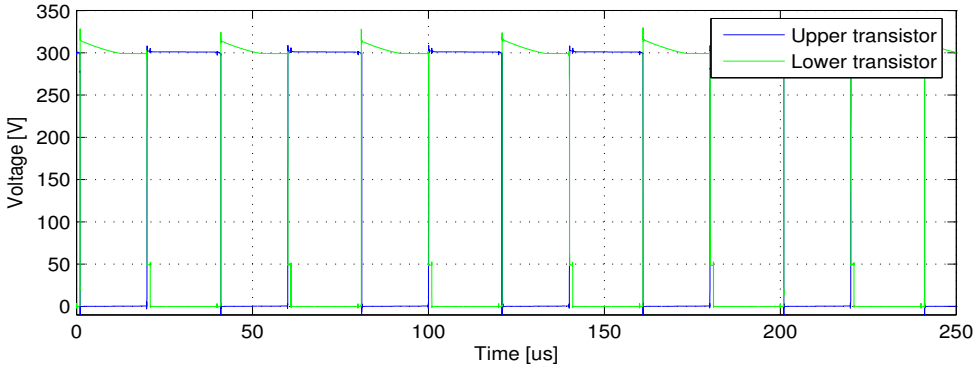

Figure 26 ***Simulated transistor voltages***

It can be seen in Figure 26 that the voltages across the transistors switch between the input voltage and zero. There is also some over voltage when the lower transistor turns off.

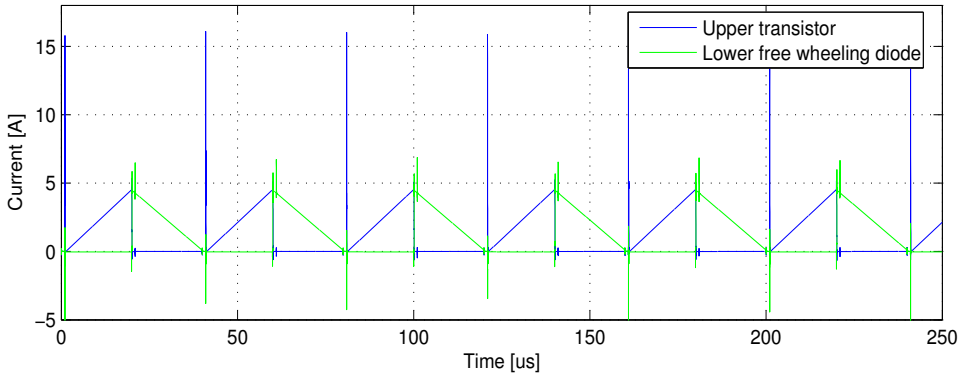

Figure 27 ***Simulated current through the upper transistor and the lower free wheeling diode***

In Figure 27 the current through the upper transistor and the lower free wheeling diode is shown. The current waveforms in the two components behave as predicted. The circuit is working and is producing a DC voltage. A current transient can be seen when the upper transistor is turned on.

3.2.3 Improving the Circuit Model

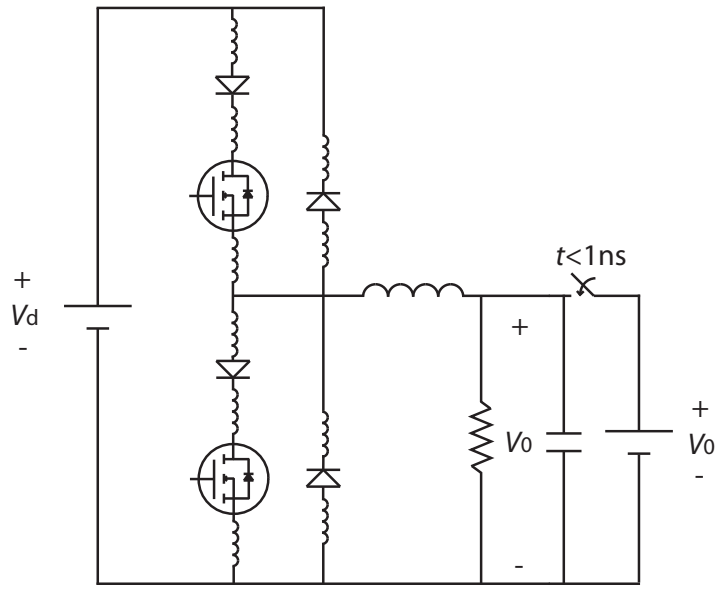

Figure 28 ***Circuit model improved with inductive wires and copper traces***

In the circuit layout described inchapter 3.2.2, there where no losses implemented in traces or cables. Although the PCB card is designed to minimize the inductance, some inductance appear in the component legs. A guideline for calculating inductance in a conductor is approximately 5nH/cm. Based on this assumption; an inductance of 5nH was connected to every leg of the components models resulting in a more realistic circuit as seen in Figure 28. In Figure 29 the voltages across the two transistors is shown.

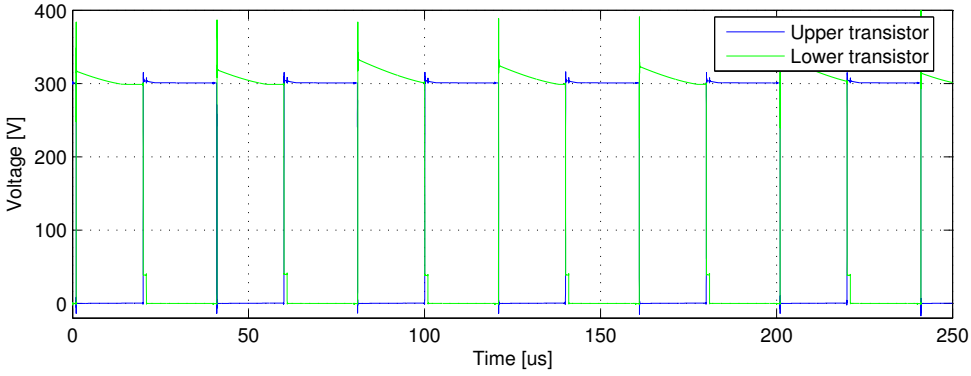

Figure 29 ***Simulated voltage across the two transistors***

It can be seen in Figure 29, that the voltage transients across the lower transistor is significantly higher than without the added inductance. This is because the inductance pushes the current forward when the switch is opened. The transistor currents can be seen in Figure 30.

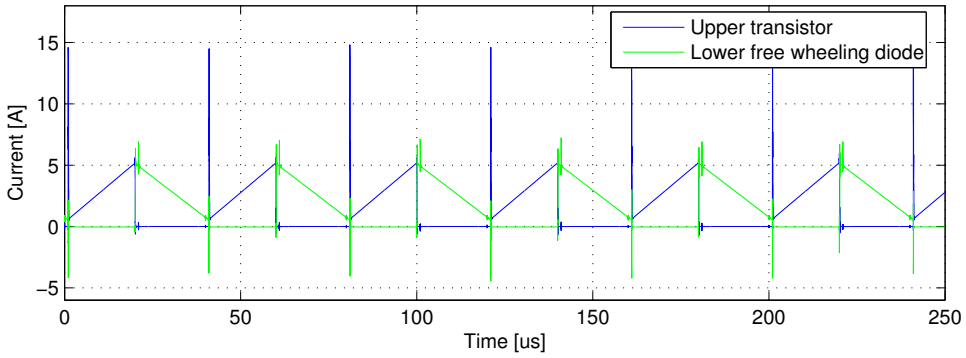

Figure 30 ***Simulated current through the upper transistor and the lower free wheeling diode***

3.2.4 Tuning the Simulation Model Using Measured Data

After verifying that the circuit model worked, the actual circuit was designed and constructed. In chapter 3.2.3 an ideal voltage source was used so the DC link voltage was totally stable. Neither were losses in the input cables implemented. To improve the simulation model, more elements were needed. On the physical circuit a large capacitor was mounted near the input to the card. In the measured current and voltage curves from the physical circuit, losses in form of cable resistance and inductance were seen. From the observations, a more complex model of the DC link where implemented. The new model included both cable inductance and resistance. The model improvement can be seen implemented in Figure 31.

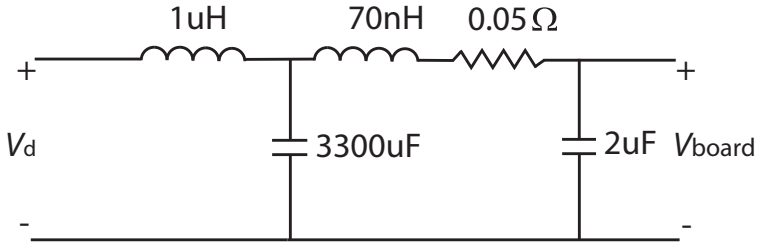

Figure 31 ***Input oscillating circuit***

After implementing the input oscillation circuit the total simulation model looked like Figure 32.

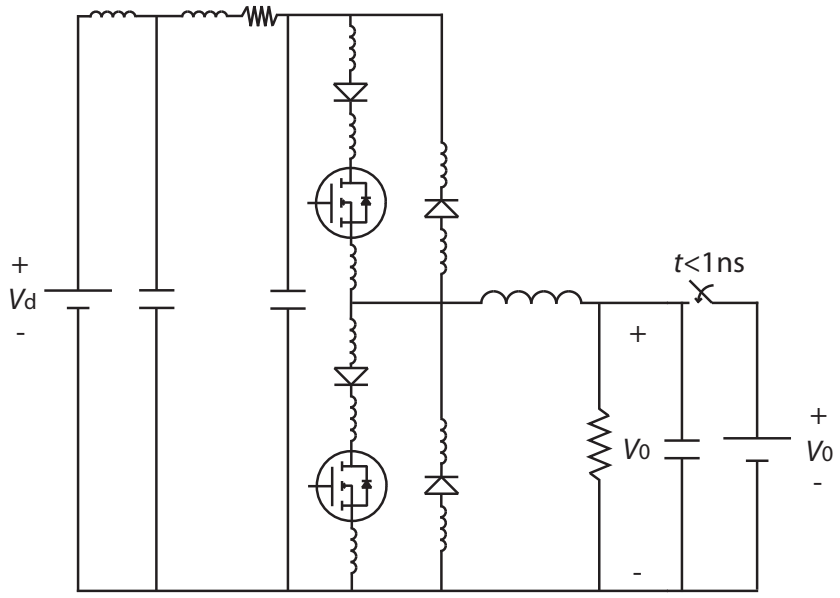

Figure 32 ***Circuit model with connected input oscillation circuit***

The voltages across the components are now more realistic than in chapter 3.2.3. The voltage from the improved model simulations can be seen in Figure 33.

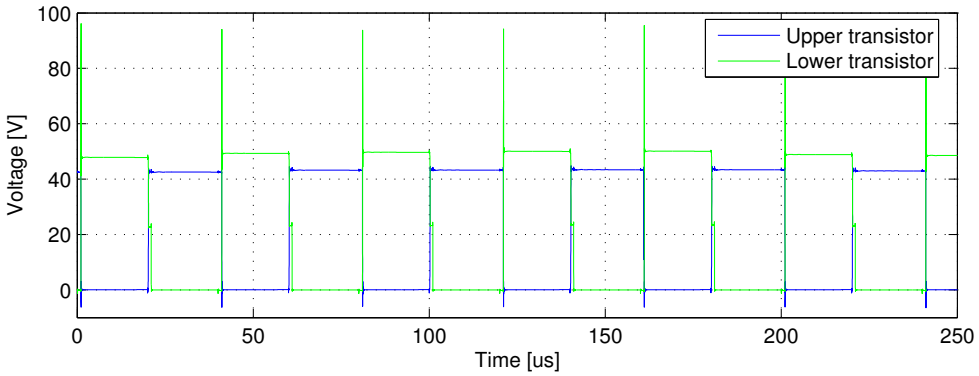

Figure 33 ***Simulated voltage across the two transistors***

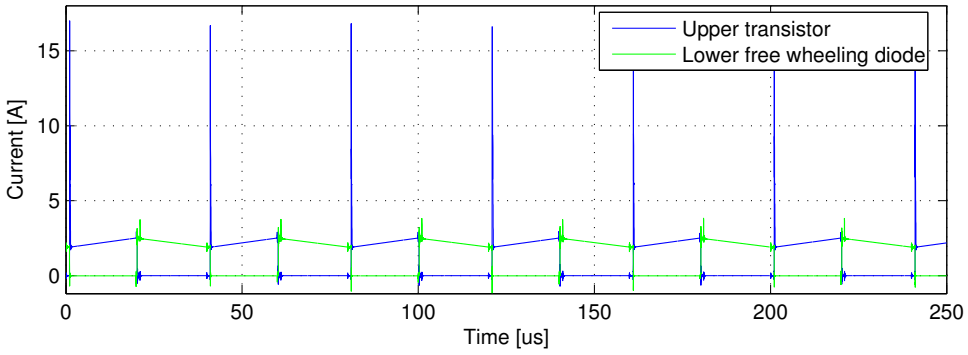

Figure 34 ***Simulated current through the upper transistor and the lower free wheeling diode***

As can be seen in Figure 34 a high current transient occurs when the upper transistor switches on. This is because of the lower series diode and transistor that acts as a parasite capacitor. When the capacitor is charged, the current is stabilized. The output current is not affected by this phenomenon since most of the transient it pushed down to the lower transistor. This also contributes to the high voltage transient across the lower transistor seen in Figure 33. When the transistors are turned off, the voltage across them is higher than the input voltage. This is because the current transient boosts the voltage, which is then kept by the series diode. The series diodes have a relatively low breakdown voltage, forcing them to conduct if the negative voltage is too high. When they break down, the voltage across them decreases down to almost zero, but this will not result in a short circuit since the transistor is turned off.

3.2.5 Using Switching Diodes for Free Wheeling Diodes

To test the suitability of the SiC free wheeling diodes, a simulation was made with these replaced by normal silicon switching diodes. The main advantage with the SiC diodes is that they have virtually no reverse recovery effect compared to normal switching diodes. The voltage when using silicon switching diodes can be seen in Figure 35.

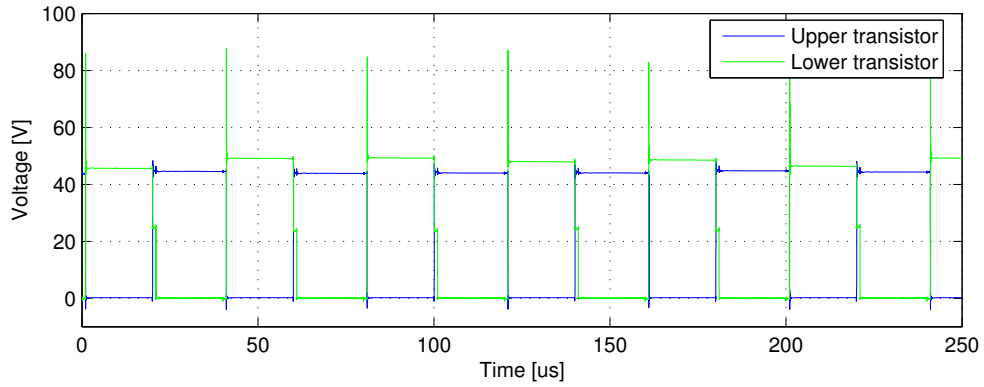

Figure 35 ***Simulated voltage across the transistors***

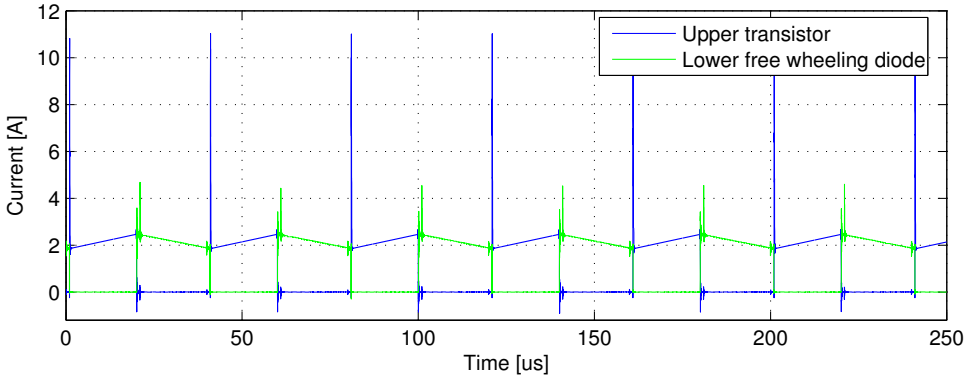

Figure 36 ***Simulated current through the upper transistor and the lower free wheeling diode***

Figure 35 and Figure 36 show that the voltage transients across the lower transistor and the

current are a little bit lower than with the SiC Schottky diode. This is due to the reverse recovery effect in the switching diode. During the reverse recovery time the current transient can pass the diode and go down to ground.

3.2.6 Simulations with Clamping Diode

To minimize the voltage transients at the lower transistor a simple clamping diode where connected between the lower transistor drain and the DC link voltage. The clamping diode is used as a simplified version of the over voltage snubber seen in chapter 2.4.1. The setup can be seen in Figure 37.

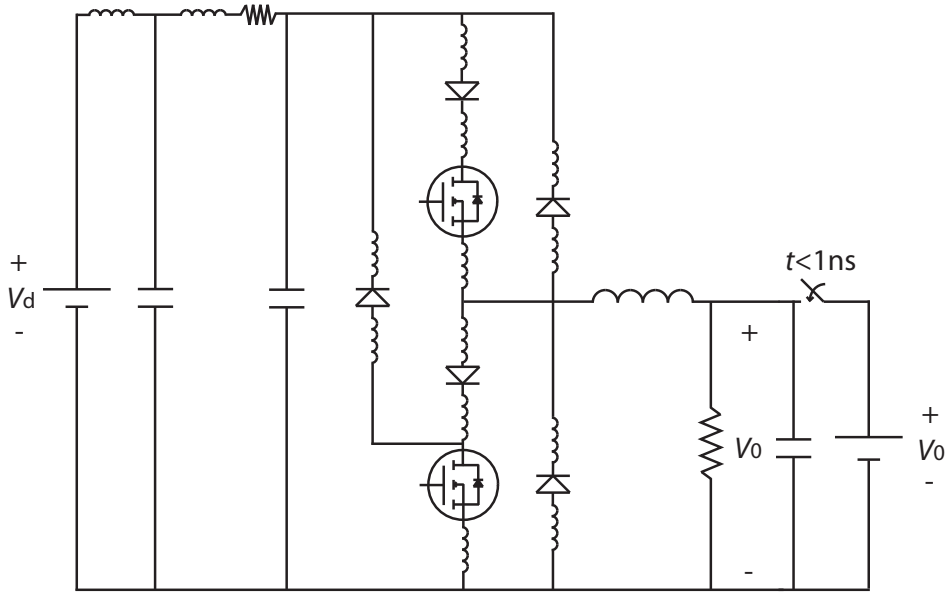

Figure 37 ***Circuit model with a clamping diode as snubber***

With this design, the over voltage will be fed back to the source. The results from the simulation can be seen in Figure 38 and Figure 39.

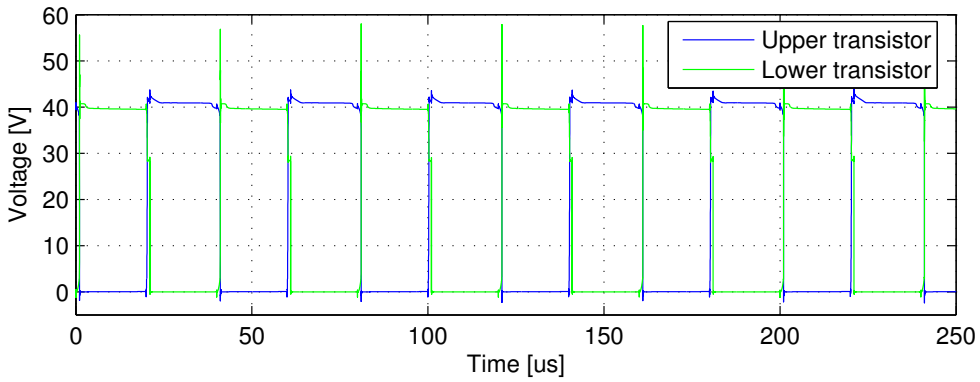

Figure 38 ***Simulated voltage across the two transistors***

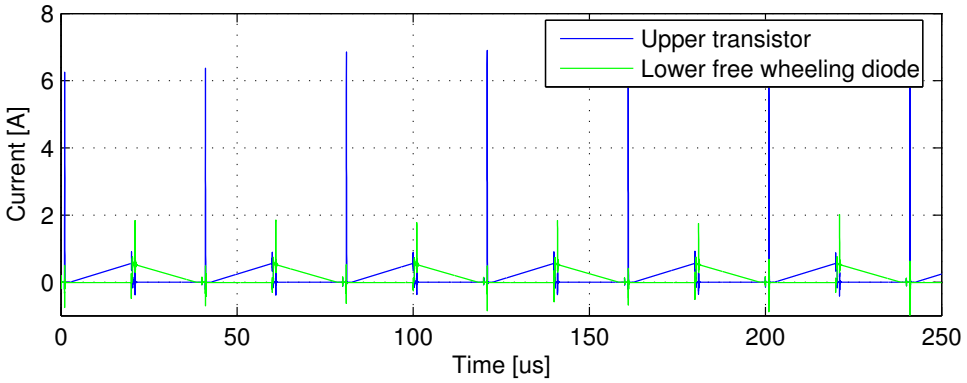

Figure 39 ***Simulated current through the upper transistor and the lower free wheeling diode***

Although in theory this should work perfectly it can be seen that the voltage and current transients still occurs. This is because of the stray inductance in the clamping diode connection. A tighter snubber design would improve the performance even more.

3.2.7 Simulating with 300V DC Link Voltage

In the initial simulations an input voltage of 40V where used. The low voltage level is the same as used in the initial measurements on the physical circuit to keep the measurements safe. In Figure 40 and Figure 41 voltage and current when running 300V where simulated to verify that the overall behaviour is similar to that with the lower voltage.

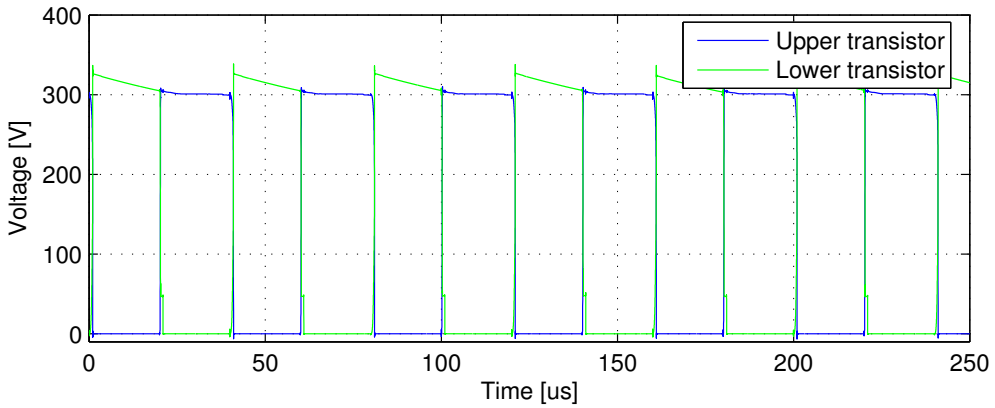

Figure 40 ***Simulated voltage across the two transistors***

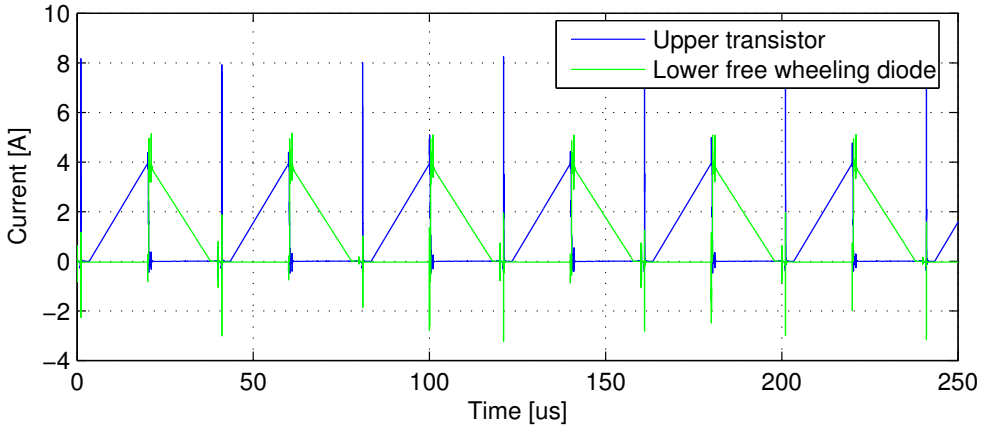

Figure 41 ***Simulated current through the upper transistor and the lower free wheeling diode***

From Figure 40 and Figure 41 the high voltage performance could be verified. The voltage and current show similar properties to that of the low voltage simulations.

3.2.8 Using the Transistors Parasite Diode as Free Wheeling Diode

Since the physical properties of the CoolMOS transistor results in a slow parasite diode, one idea is to remove the free wheeling diodes and use the parasitic effect instead. This also means that the diodes connected in series with the transistors had to be removed. The two transistors are now the only components in the circuit. The minimized half bridge can be seen in Figure 42.

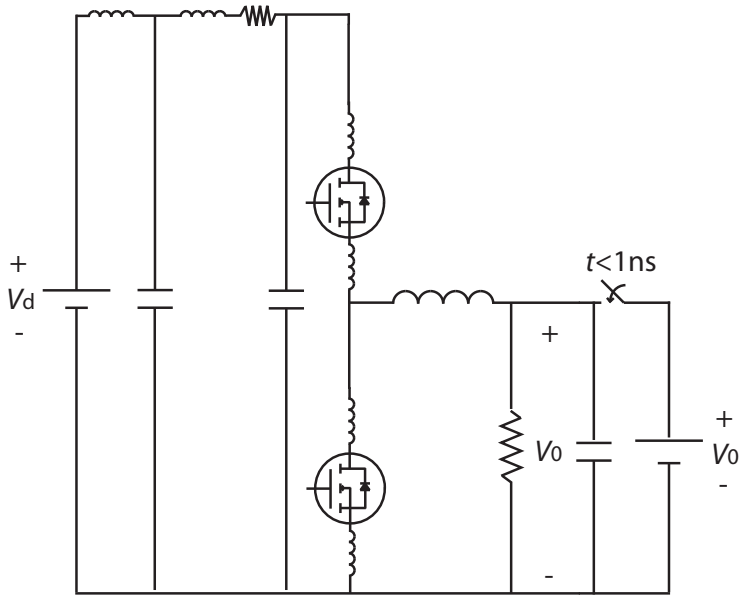

Figure 42 ***Circuit model without external free wheeling diodes***

The circuit was simulated with an input voltage of 40 volts and an eight ohm load. The voltages across the transistors and the currents through them can be seen in Figure 43 and Figure 44.

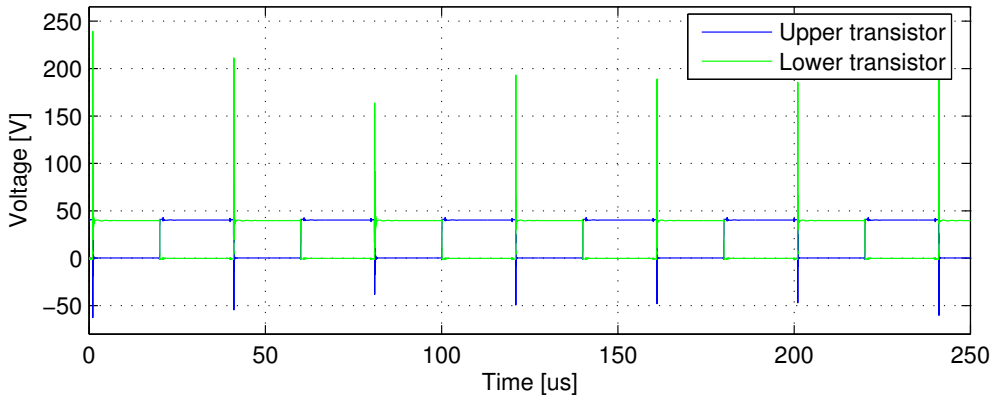

Figure 43 ***Simulated voltage across the two transistors***

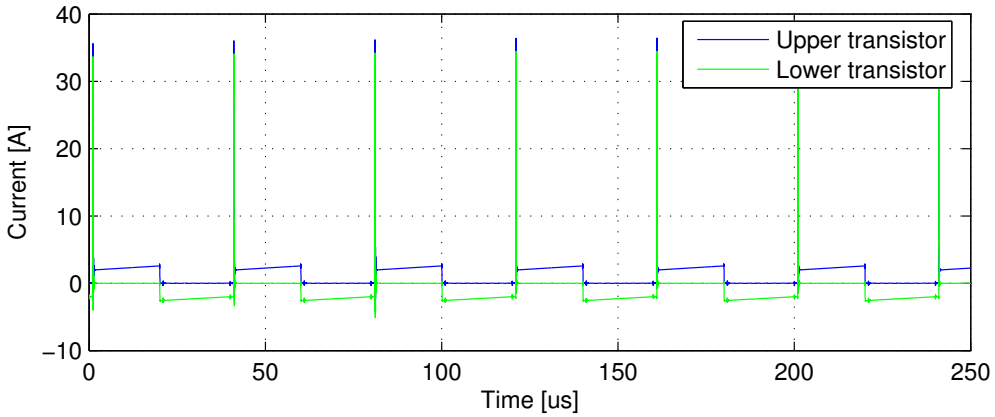

Figure 44 ***Simulated current through the transistors***

When the upper transistor is turned on, the current is still flowing through the lower transistor. Since the parasite diode in the lower transistor is very slow, the bridge will be short circuited for a short while. The short circuit current transients can be seen in Figure 44. When the parasite diode stops conducting, the stray inductance creates a voltage transient. These voltage transients can be seen in Figure 43.

One way to minimize this effect is to have a slower turn on for the upper transistor by charging the gate with less current. In this way, the transients will be lost as heat, while the upper transistor operates in the linear region.

3.3 Measurements

3.3.1 Drive circuit

The PWM IC generates a saw tooth signal with the frequency according to the values of the resistor and the capacitor controlling the signal. The saw tooth signal is then compared with a control reference voltage and results in a PWM signal. In Figure 45 the saw tooth voltage and the reference voltage measurements from the drive circuit can be seen. The circuit appears to operate as predicted when compared to Figure 1.

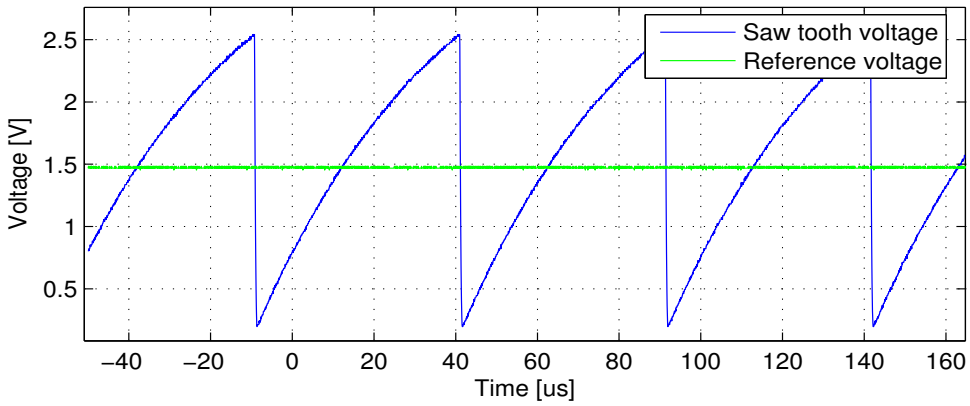

Figure 45 ***Saw tooth voltage and reference voltage***

These two signals, the saw tooth and the control reference, are both controlled by two potentiometers. One for changing the frequency of the saw tooth, and one for changing the value of the control voltage. The value of the control signal determines the duty-cycle of the PWM signal.

Since the PWM generator only has one output, one more signal is needed. The second one should be the inverse of the first one to prevent that both switches are open and cause a short circuit. To invert the signal a NAND circuit is used. By splitting the signal in two and feeding it to the NAND, an inverting effect if produced. The NAND is connected this way to the PWM circuit to produce the second PWM voltage. The PWM voltage, both before and after the inverting circuit, can be seen in Figure 46. It is worth noticing that the inverted voltage is slightly delayed by the logic NAND.

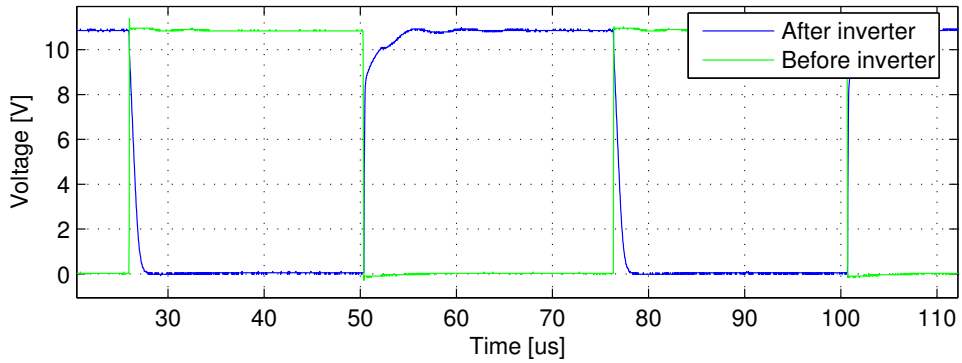

Figure 46 ***PWM voltage before and after inverting circuit***

It is very important that the two transistors are not turned on at the same time. To prevent this, a blanking time circuit is put between the PWM IC and the gate driver. The blanking time circuit increase the rise time of the signal voltage. The gate driver circuit has Schmitt triggers on the inputs, which mean that the input doesn't get high until the input voltage has a certain value. Now there is a small delay between the two PWM signals and the transistors can operate without causing a short circuit. The simple asymmetric RC network used to create the delay can be seen in Figure 47.

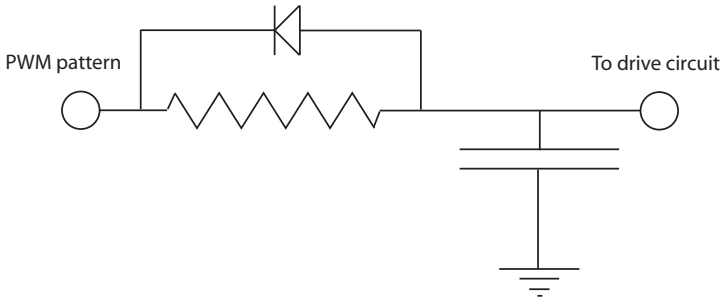

Figure 47 ***Asymmetric RC network for blanking time***

The blanking time is produced by limiting the current to the capacitor with a resistor. Now it takes time before it is fully charged, and the rise time increases. By changing the value of the resistance the time to charge the capacitor can be controlled. When the signal should go down to zero, The capacitor can discharge through the diode without any current limiting resistor. The effect of the blanking time can be seen in Figure 48.

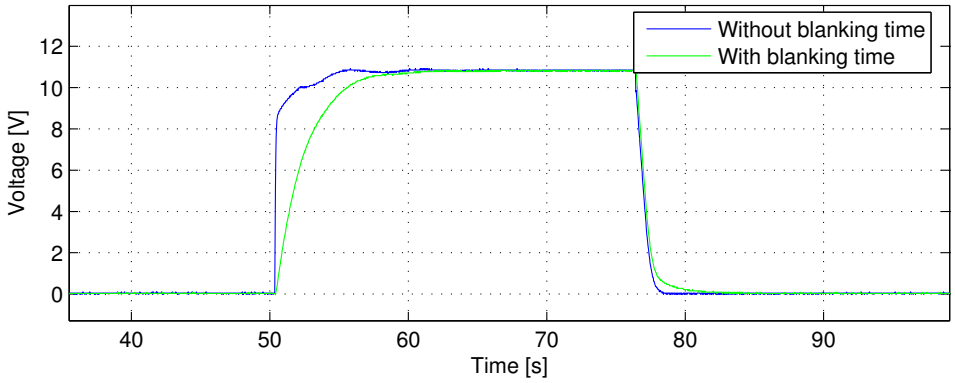

Figure 48 ***Voltage before and after time delay***

After the blanking time circuit, the voltage signals are fed to a gate driver. There are two reasons that a gate driver IC is used. First, the transistor gate requires more current than the PWM IC can deliver. The selected gate driver can deliver up to two amperes which should be enough for at least 100 kHz. Second and most important is the ability to add an offset to the driver for the upper transistor of the bridge. This is possible because of the bootstrap capacitors and diode connected to the high voltage side of the driver.

The output voltage from the gate driver can be seen in Figure 49. In this figure, the slow rise time from the delay circuit has turned into a blanking time between the pulses. This is due to the Schmitt trigger of the gate driver input. The driver is not connected to any load in Figure 49.

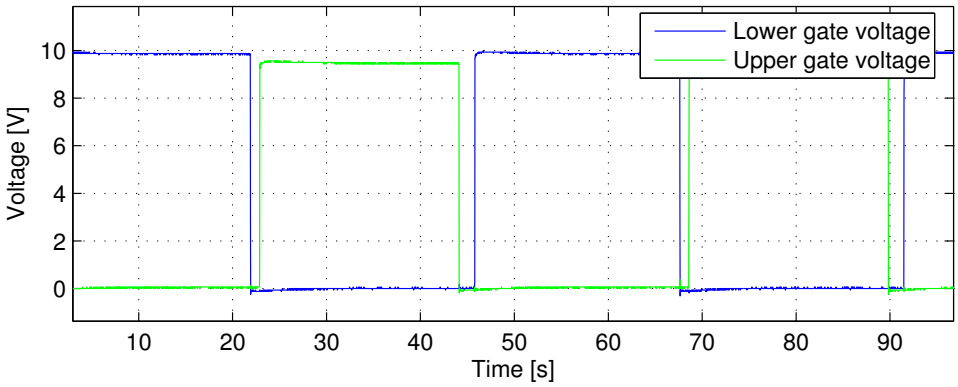

Figure 49 ***Gate voltages with no load***

The small voltage drop at the upper transistor seen in Figure 49 is because of the voltage drop across the bootstrap diode.

When connected to the gate, the gate charge requires current to increase in voltage. The gate charge can be approximated by a capacitor of similar size. Since the current is limited to two amperes, the voltage will take some time to reach its final value. In Figure 50 the gate voltage with load can be seen.

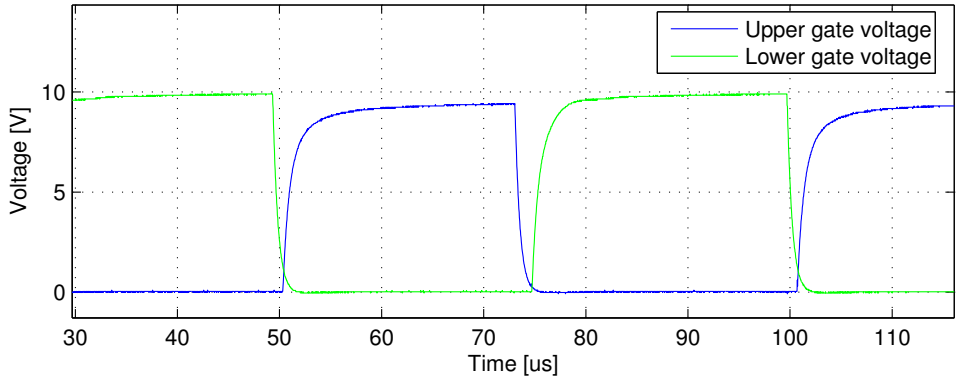

Figure 50 ***Gate voltages with load***

3.3.2 Main Circuit Dynamics

To make all the tests as equal as possible, all measurements except the high voltage test, were done with the same setup. After investigating the DC link current, a large capacitor of 3300µF was connected as close to the board as possible. To smooth the DC voltage across the load, a large long life electrolytic capacitor of 6800µF was connected in parallel with the load. This might be an unnecessary high value, but the capacitor must be able to handle a high current ripple. The used long life electrolytic capacitor is able to handle a current ripple of a few amperes. Another important aspect is that the load inductor doesn't go into saturation. After a few tests with different inductors, a 650µH toroid inductor where chosen. The input voltage was set to 40 V and the load resistance to eight ohm. The frequency of the drive circuit was set to approximately 25 kHz which is the same as used in the simulations. The duty ratio was

set to approximately 50% which means that the output voltage should be half the input voltage according to (1).

The tests were performed and evaluated in the following order:

1. Main circuit
2. Main circuit with switching diodes
3. Without free wheeling diodes
4. Main circuit with snubber
5. High voltage test

3.3.2.1 Main Circuit

For testing the main circuit the IPP60R099CP CoolMOS transistor was used. The free wheeling diode was an IDT16S60C SiC Schottky diode and the series diode was a 30CPQ045/IR Schottky diode.

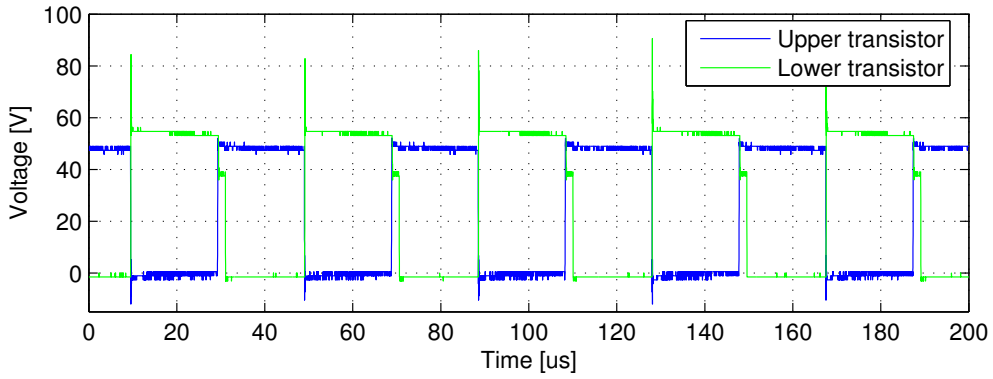

Figure 51 ***Measured voltage across the transistors***

As seen in Figure 51 the voltage across the transistors appears to have a similar behaviour as in the simulation. A comparison between the simulated and the measured voltage across the lower transistor can be seen in Figure 52.

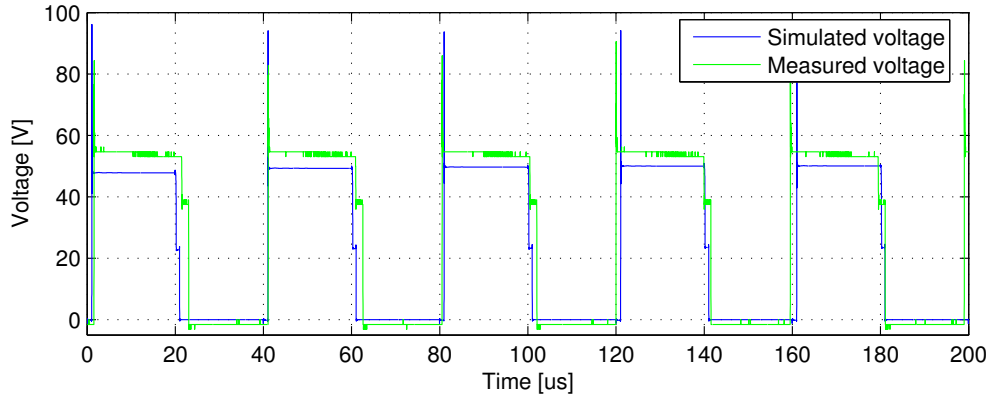

Figure 52 ***Simulated and measured voltage across the lower transistor***

As seen in Figure 52, the measured voltage across the transistor at turn off is a bit higher than the simulated value. This is probably due to a difference in the simulated schematic compared to the actual circuit regarding stray inductances and capacitances. When the upper transistor turns on, a current transient will boost the voltage between then lower series diode and the lower transistor. Next, the upper transistor will turn off and the current commutate to the lower free wheeling diode. Now the boosted voltage will be across the lower series diode. Since this diode has a reverse blocking voltage of 40 V, it will act as a Zener diode and the boosted voltage will drop to 40 V. As the lower transistor turns on, the voltage across the lower series diode will drop to almost zero. This can be seen as a step down to 40 V in the measured voltage in Figure 52. The reason why the step in the simulated voltage appears to be lower is because a diode with a lower reverse blocking voltage was used in the simulations. This phenomenon can be seen throughout all simulations and measurements. In Figure 53 the voltage breakdown and boosting across the series diode can be observed.

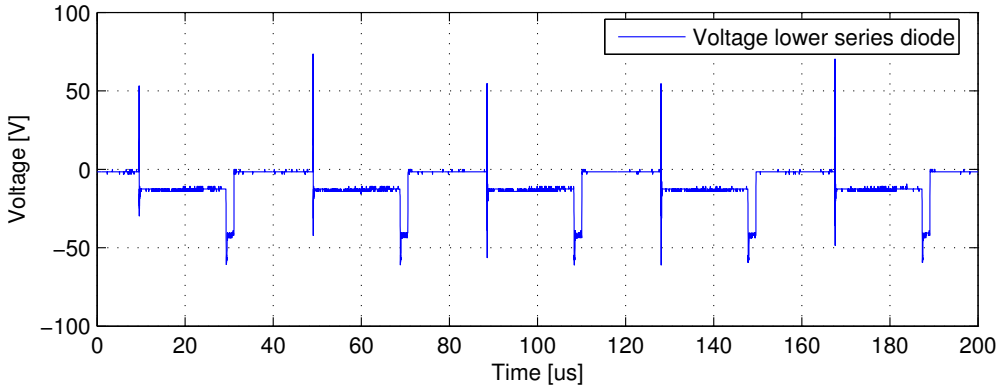

Figure 53 ***Measured voltage across the lower series diode***

The negative voltage is built up by a current transient when the upper transistor is turned on. The voltage is then kept negative by the reverse biased series diode. As the upper transistor turns off, then voltage across the series diode falls down to minus 40 volts until the lower transistor turns on and then diode is connected to ground.

According to (1) the output voltage should be half the input voltage which can be verified in Figure 54.

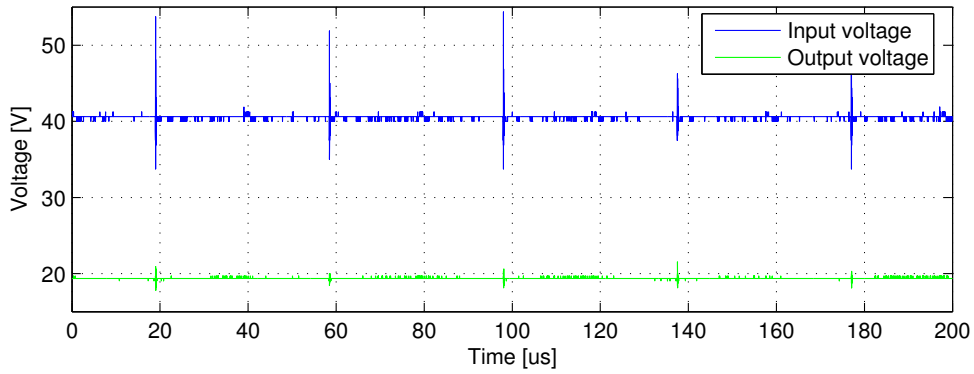

Figure 54 ***Measured input and output voltage***

In Figure 54 it can be seen that the transients from the upper transistor turn on affect the input and output voltages. The power source in the tests is not ideal like the source in the simulations. If the circuit was fed with a more stabile voltage source, like a battery, these transients would be heavily reduced. In Figure 55 the simulated input current is compared to the measured.

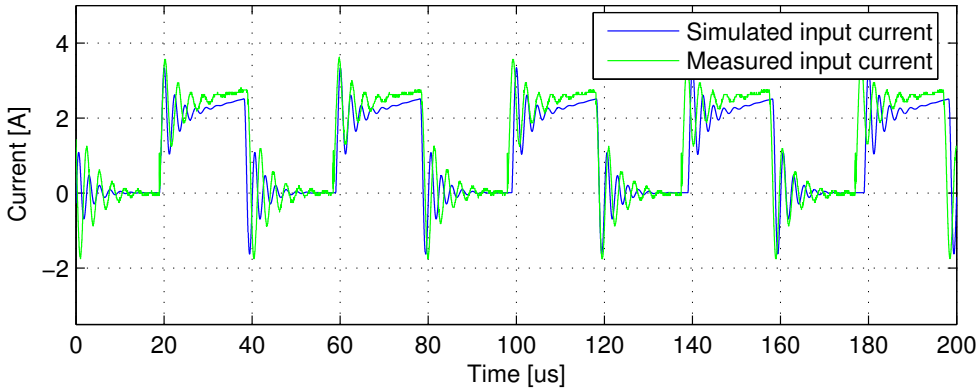

Figure 55 ***Simulated and measured input current***

In Figure 55 the measured current is a bit higher than the simulated, but the oscillations have the same frequency which from Figure 55 was calculated to approximately 330 kHz. This frequency where then used to calculate the stray inductance between the two input capacitors. This result was then used in the simulations as seen in chapter 3.2.4.

Since it is impossible to measure the current through the upper transistor, the input current is measured between the two capacitances at the input. From the simulations it can be seen that the current into the upper transistor should look like Figure 34.

3.3.2.2 With Switching Diodes

For testing the circuit with regular switching diodes instead of the SiC Schottky diode the 20ETF04/IR diode was used. From the simulation, it seemed that the voltage transients across the lower transistor were a little bit lower than with the SiC diode. The voltages across the two transistors with the switch diode can be seen in Figure 56.

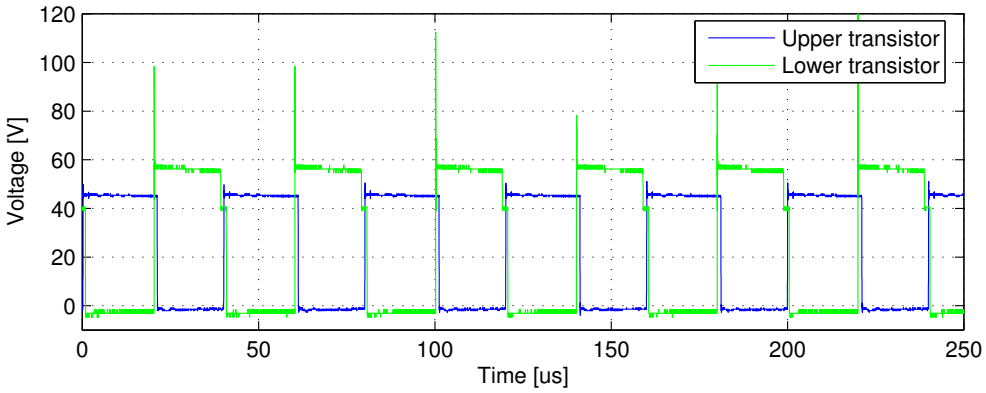

Figure 56 ***Measured voltages across the transistors with switching diodes***

In Figure 56 the voltage transients appears to be higher than with the SiC diode seen in Figure 51. The voltage across the lower transistor also seems a bit high. This can be seen in Figure 57 when comparing the simulated value to the measured.

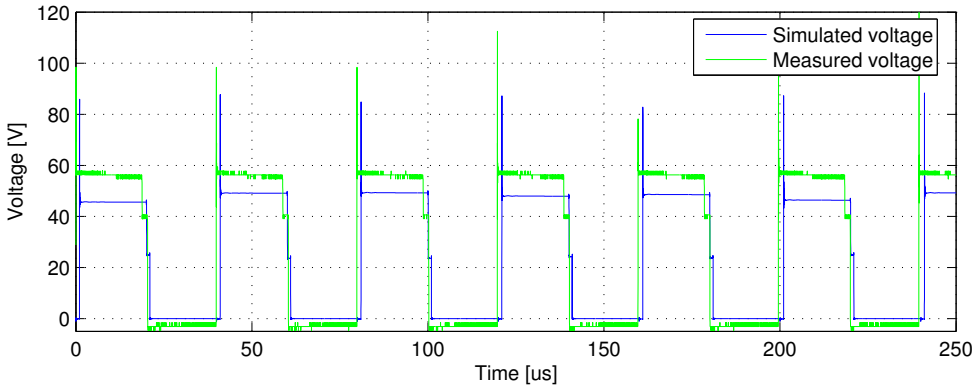

Figure 57 ***Simulated and measured voltage across the lower transistor with switching diodes***

In Figure 57 the measured voltage is compared to the simulated. As in the test with the SiC diodes, the voltage across the two transistors is a little bit higher than in the simulation.

The input and output voltage can be seen in Figure 58.

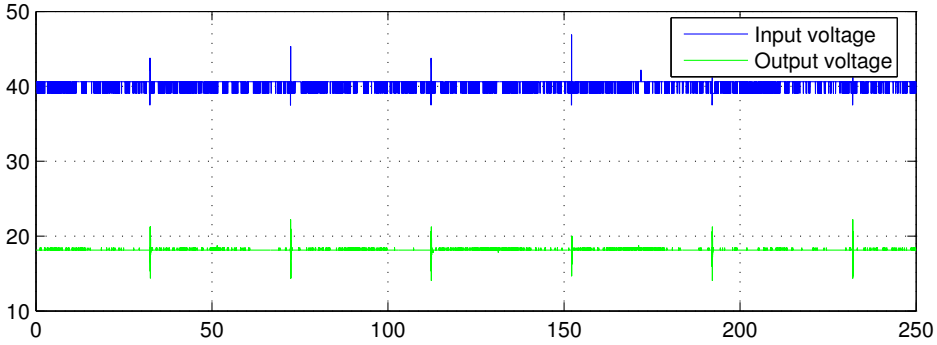

Figure 58 ***Measured input and output voltage with switching diodes***

It can be seen in Figure 58 that the transients from the transistor voltage and current also affect the input and output voltages.

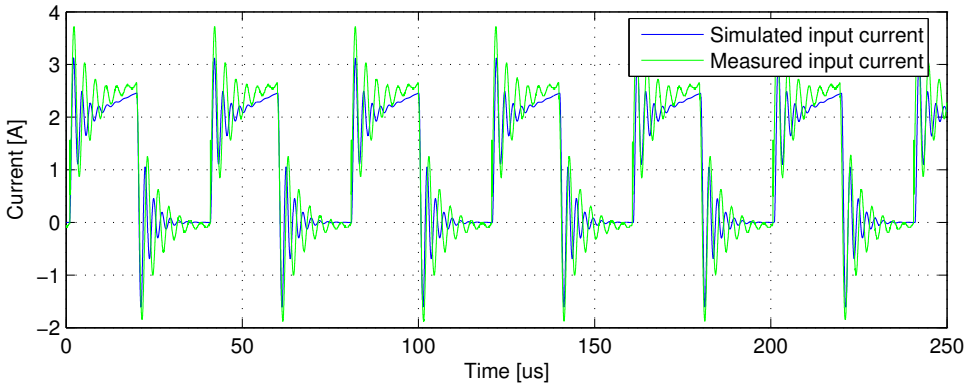

Figure 59 ***Simulated and measured input current with switching diodes***

It can be seen in Figure 59 that currents from the simulations and the measurements match each other very well. The measured current is in this case a bit higher than the simulated, and has more oscillations but with the same frequency as in the measurement with the SiC free wheeling diode. The different magnitude of the oscillations is the result of a small difference in cable resistance between the simulation model and the real circuit.

3.3.2.3 Without Free Wheeling Diode

To test the circuit without free wheeling diodes great precaution has to be taken into account. Since the current is free wheeling through the lower transistor the circuit is going to be short circuited from a small period of time, during the transistors reverse recovery. In this test the power source was set to a current limited level. The voltage was then slowly increased from zero to a suitable level. The most interesting thing to measure was the voltage across the lower transistor as can be seen in Figure 60.

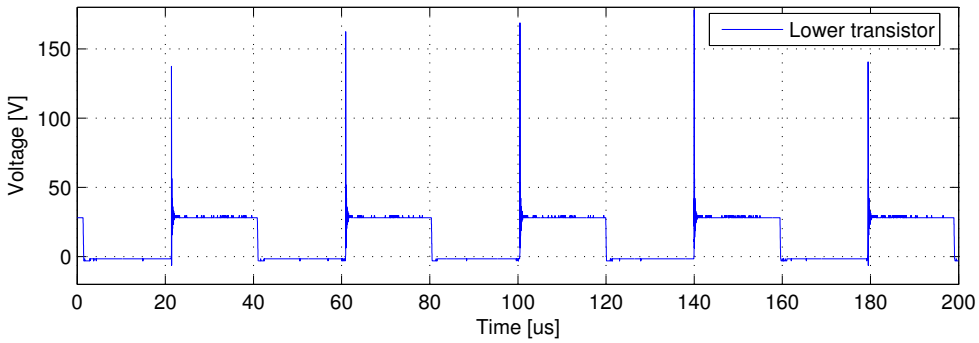

Figure 60 ***Measured voltage across the lower transistor without free wheeling diodes***

As can be seen in Figure 60, there are huge voltage transients. This could be seen in the simulation and was not surprising, but the transients are unacceptably high considering that the DC link voltage is about 30 V. The voltage transients are due to the large current running through the lower transistor during the reverse recovery time.

In Figure 61 it can be seen how the drive circuit missed some of its turn on pulse as the DC

link voltage passed 40 V.

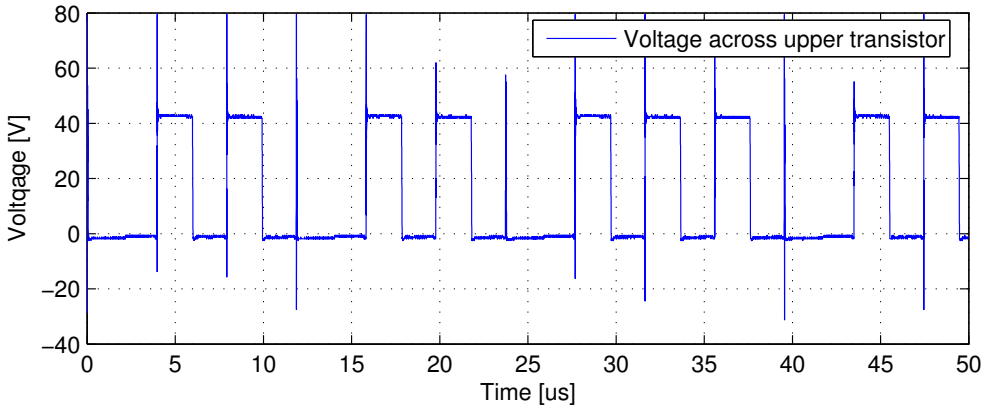

Figure 61 ***Measured voltage across the lower transistor when the gate drive misfires***

There are a number of different theories why the gate driver shut down. Most likely it is EMI from the switching that interferes with either the shut down pin of the driver IC or the logic signals. The assumption is based on the fact that the higher voltage will cause more EMI.

Another interesting measurement is to see the current flow through the lower transistor as seen in Figure 62. For the measurements a small wire loop was added.

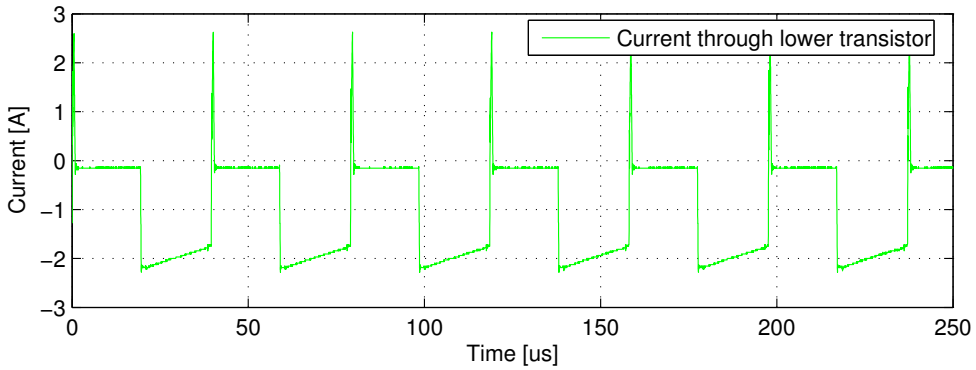

Figure 62 ***Measured current through the lower transistor***

In Figure 62 the current through the lower transistor can be seen. The current transients in the measurement are low compared with the simulation seen in Figure 44. This is due to the current limit reached in the power source. When the drawn current goes above the limit the power source reduce its voltage until the current is within its limit again.

The circuit with no free wheeling diodes and no series diodes works although the transients become very high because the reverse recovery of the lower transistor. Some improved control of the transistors could be implemented, but is left out in this report.

3.3.2.4 With Clamping Diode

For the test with a clamping diode an 8ETH03 switch diode was used. The voltages across the two transistors can be seen in Figure 63.

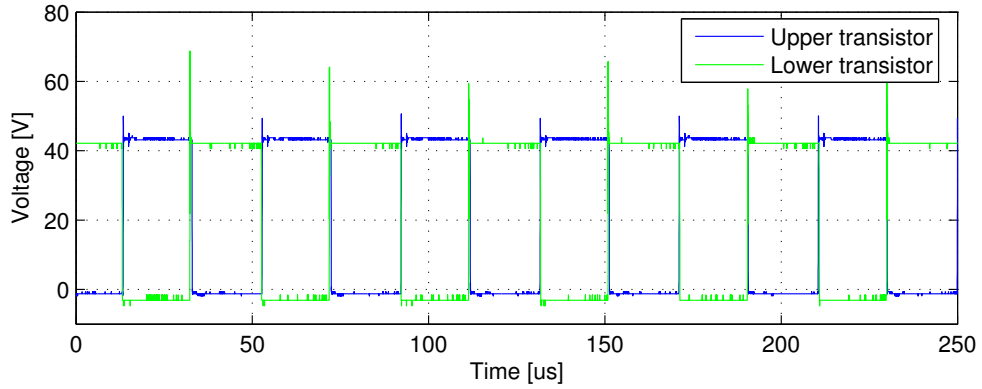

Figure 63 ***Measured voltage across the transistors with clamping diode***

As can be seen in Figure 63 the transients still occur as in the simulation, see Figure 38. The inductive properties of the wires that connect the clamping diode will not allow too fast current transients. The voltage across the transistors is however somewhat lower than without the clamping diode. In Figure 64 the voltage across the lower series diode is shown.

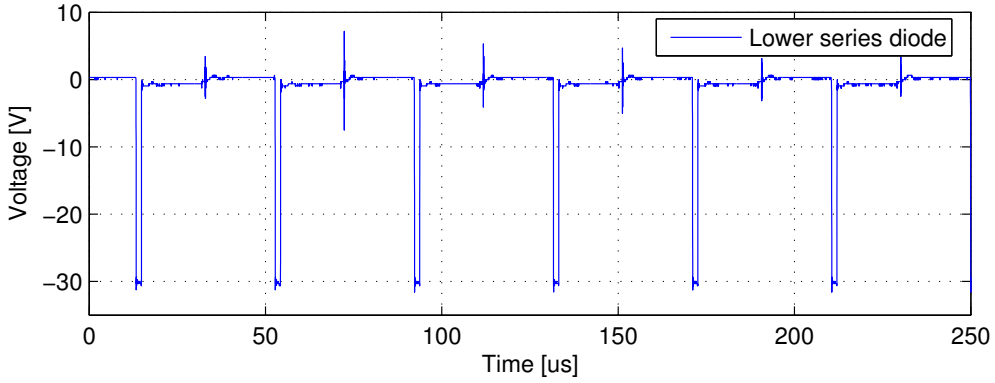

Figure 64 ***Measured voltage across the lower series diode with snubber***

The clamping diode starts to conduct when the transistor voltage reaches just over the input voltage. Because of this, the transients are lower across the lower transistor.

In Figure 65 the difference between simulated and measured values of the voltage across the lower transistor can be seen.

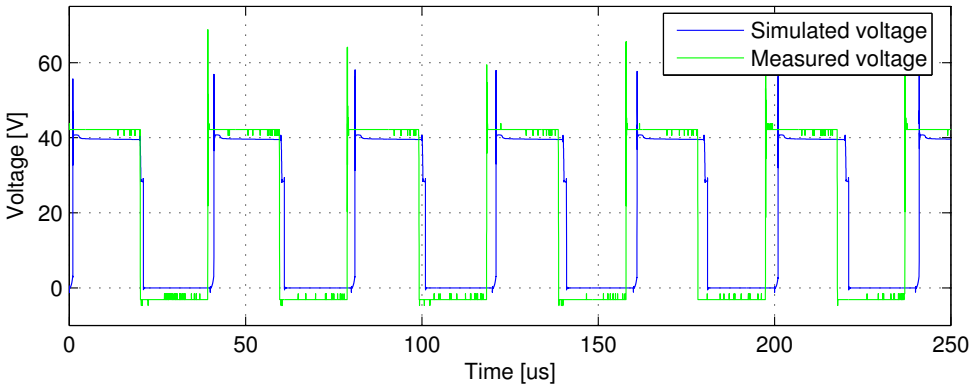

Figure 65 ***Simulated and measured voltage across the lower transistor with snubber***

The voltages are very similar. The small difference can be that the clamping diode has a smaller voltage drop in the simulation program than in reality.

To implement a snubber circuit can lower the voltage across the transistors and reduce the transients. This can be a good idea to reduce the stress to the switch.

3.3.2.5 High Voltage Test

For the high voltage test the second board with wider copper traces was used. The transistors were changed to the IPW60R045CP transistor for lower on state losses and higher current capability. Since the DC link voltage was going to be about 300 volts, the load had to be changed. The 8 Ω load were too small and could not handle that much power so it had to be replaced. A load of 50 Ω that could handle a continuous power of more than one kilowatt was connected to the output of the board. With the DC link voltage at 300 volts and a duty cycle of 50% the load power would be approximately 450 W. The load capacitor was also changed, since it had a maximum voltage of 70 V. A smaller capacitor of 3600µF that could handle a voltage of 360 V replaced the 70 V capacitor. When applying a high voltage across the load inductor the ferrite core went into saturation, so a new coreless inductor with approximately the same inductance was constructed. The power source used in the other tests was not able to deliver enough voltage so the circuit were connected to a variable transformer via a diode rectifier. The connection can be seen in Figure 66.

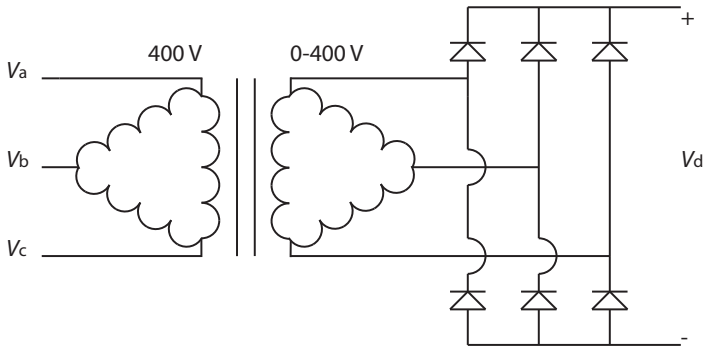

Figure 66 ***Transformer and diode rectifier bridge***

The voltage across the transistors when running from the diode rectifier can be seen in Figure 67.

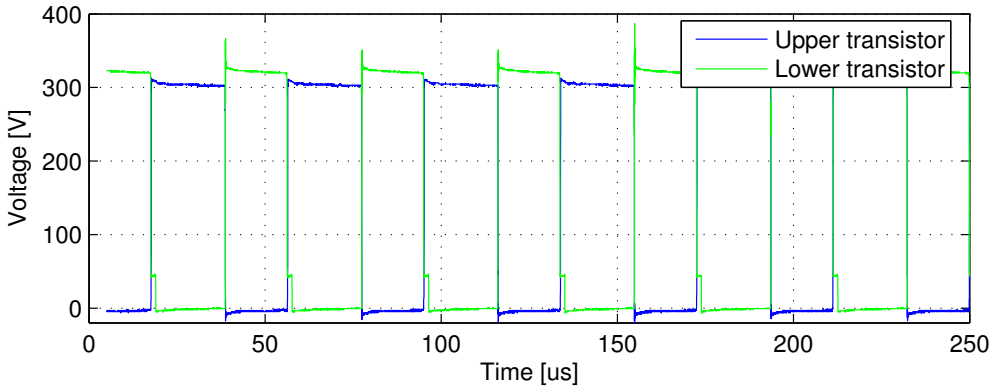

Figure 67 ***Measured voltage across the transistors at high voltage***

The transients have about the same magnitude or maybe a bit lower than with a lower voltage. This is possibly due to that the higher DC link voltage with about the same current will make it harder for transients to appear.

In Figure 68 a comparison of the voltage from the simulation and the measured values across the lower transistor can be seen.

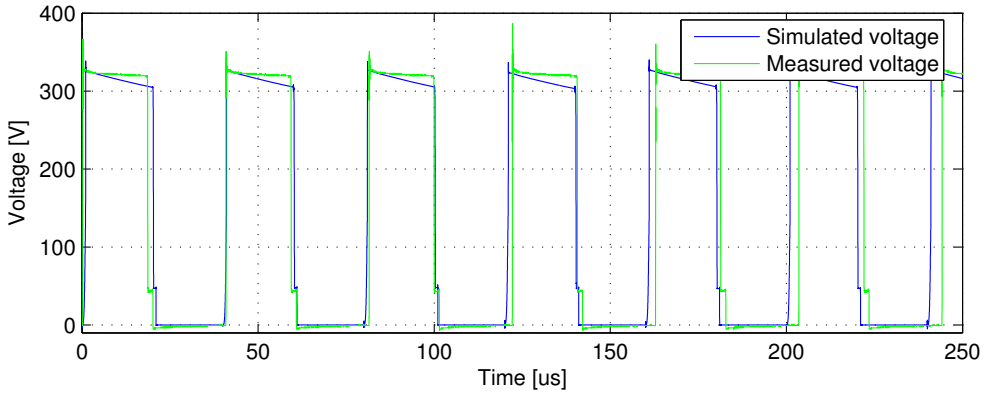

Figure 68 ***Simulated and measured voltage across the lower transistor at high voltage***

As seen in Figure 68 the simulated voltage reaches the same level as the measured, but then it decreases.

It can also be seen in Figure 68 that the switching frequencies differ a bit. The physical drive circuit switching frequency is control with a variable resistor, so it is practically impossible to set an exact frequency.

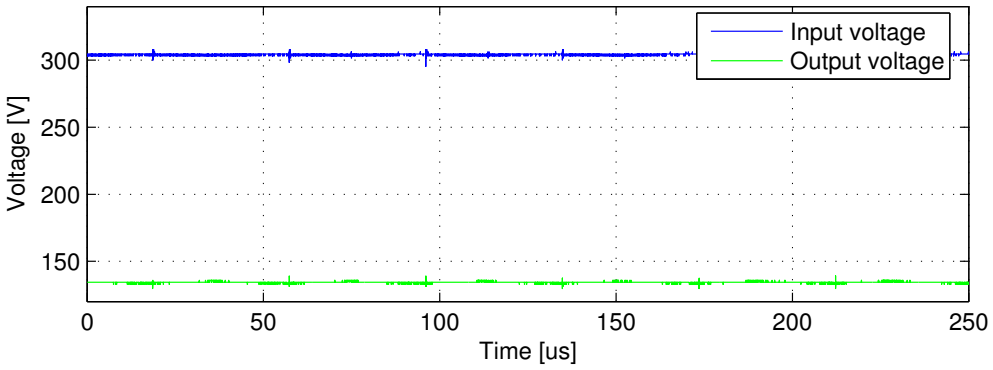

Figure 69 ***Measured input and output voltage at high voltage***

The input and output voltage seen in Figure 69 are stabile although some transients from the switching of the upper transistor can be seen.

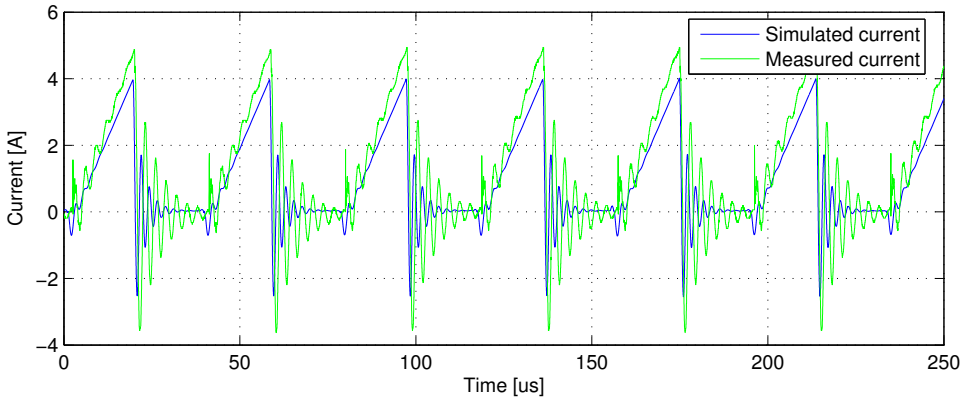

Figure 70 ***Simulated and measured input current at high voltage***

It can be verified in Figure 70 that the input current from the simulation and the measurement have almost the same waveform and oscillation frequency.

3.3.2.6 Investigating the DC-link

To minimize stress on the power source, the current and voltage drawn should be kept as constant as possible. Fluctuations in the power drawn can both damage the source and disturb other components connected to the source. The following chapter presents a number of problems and solutions regarding the DC-link.

3.3.2.6.1 Shaping the Current Wave Form

In the design phase of the project it was believed that the two metal film capacitors connected to the power source would be able to keep the power flow stable. This could have been true if the board could be connected with very short wires to a stable power source, but not in a normal setup. The longer cables cause more inductance and will result in fluctuations that are too large current for the capacitors to handle. Figure 71 shows what the current looked like during simulation with an ideal voltage source and no cable inductance.

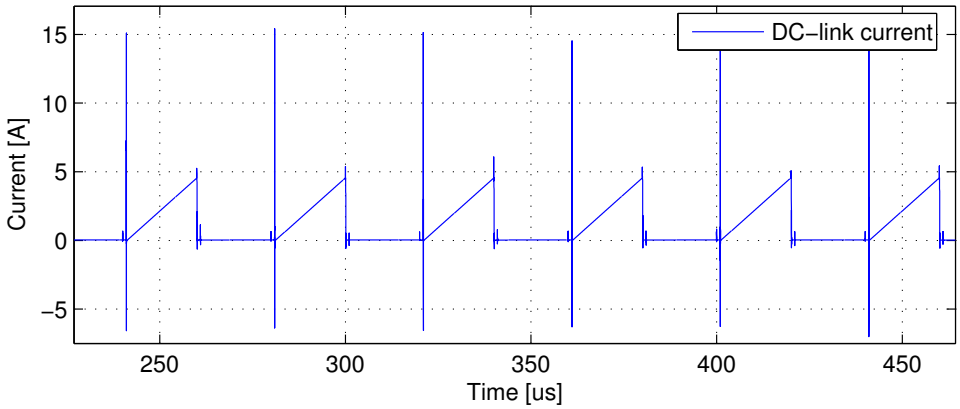

Figure 71 ***DC link current as seen in the simulations***

During the first test run the input current had a fluctuating waveform due to large inductive effects. This can be seen in Figure 72.

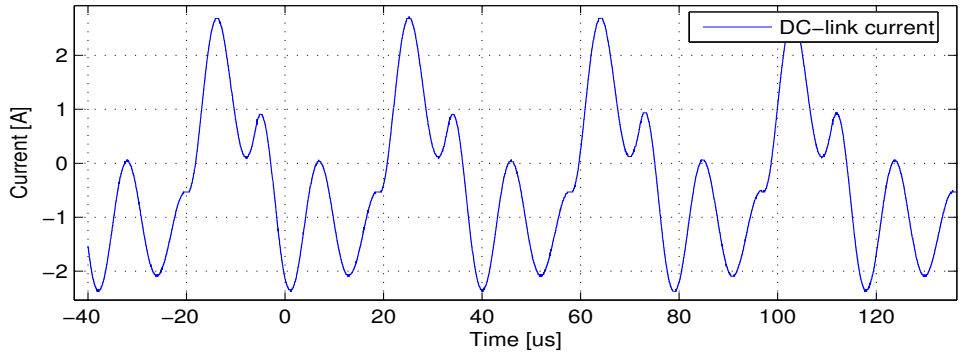

Figure 72 ***Measured DC link current without electrolytic capacitor***

To limit the influence of the cable inductance and stabilize the DC-link, an electrolytic capacitor of 3300 µF was connected to the input. Now, the current from the source to the capacitor had a nice triangular wave form that will cause less stress to the source. The current from the source can be seen in Figure 73.

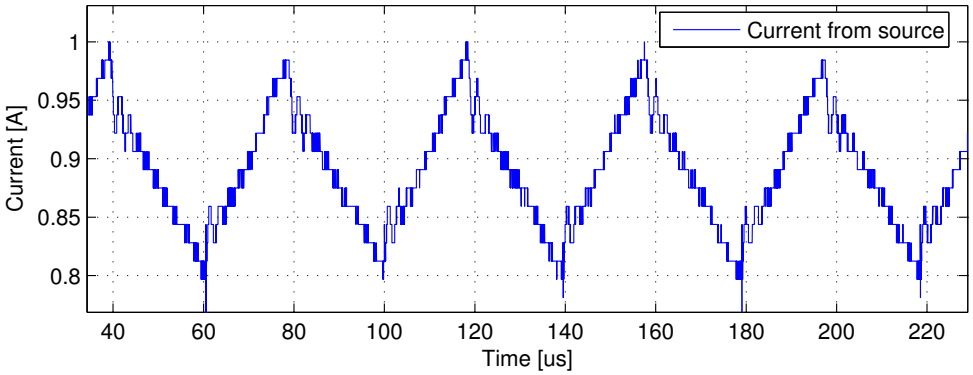

Figure 73 ***Measured current from voltage source***

Although the current from the source has a nicer wave form, a new problem in the form of oscillations between the capacitors occurred. This is due to the inductance in the wires used to connect the electrolytic capacitor to the board, forming a resonant circuit with a frequency depending on inductor and capacitor values. A simple LC oscillating circuit can be seen in Figure 74.

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \qquad (1)$$

The oscillating frequency for such a circuit is described in (1). From the current waveforms seen in Figure 75, the resonant frequency was calculated to be about 300 kHz.

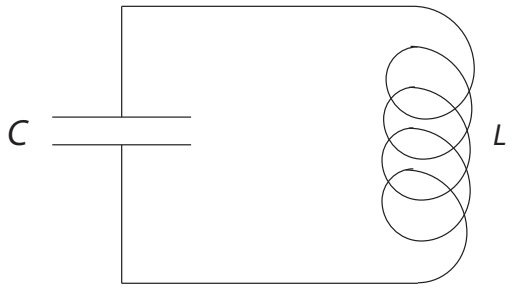

Figure 74 ***The basic LC oscillating circuit***

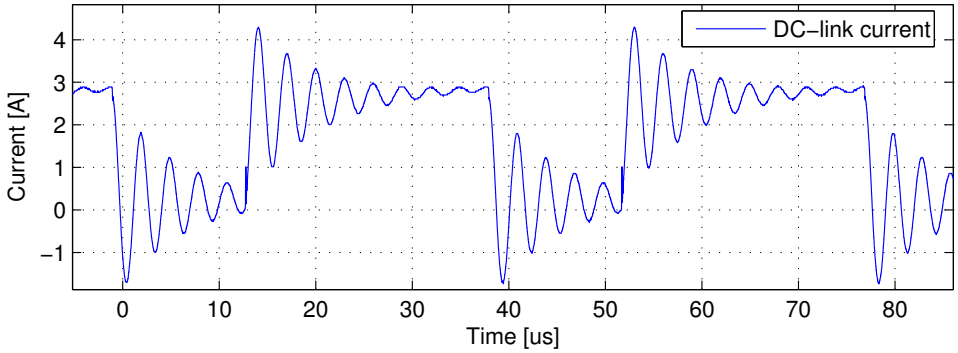

Figure 75 ***Measured oscillating DC link current***

3.3.2.6.2 Problems with Oscillating DC-Link Currents

To be able to get rid of these oscillations four different solutions were investigated.

The first and obvious solution is to minimize the inductance but since the PCB board already has been fabricated, the electrolytic capacitor can't be placed directly on the board. Instead it has to be connected through wires. With the high frequency switching, the design does not allow much inductance in the wires from so the connection to the electrolytic capacitor has to be as short as possible.

Another theory was that the electrolytic capacitor couldn't handle very quick current transients. If this was the problem, the solution could be to connect a quick capacitor directly to the electrolytic capacitor. An extra metal film capacitor were connected directly to the electrolytic capacitor with the purpose of taking care of quick current transients. These

transients proved not to be the reason to why the oscillations occur, and therefore the extra capacitor didn't lead to any improvement. The resulting current can be seen in Figure 76.

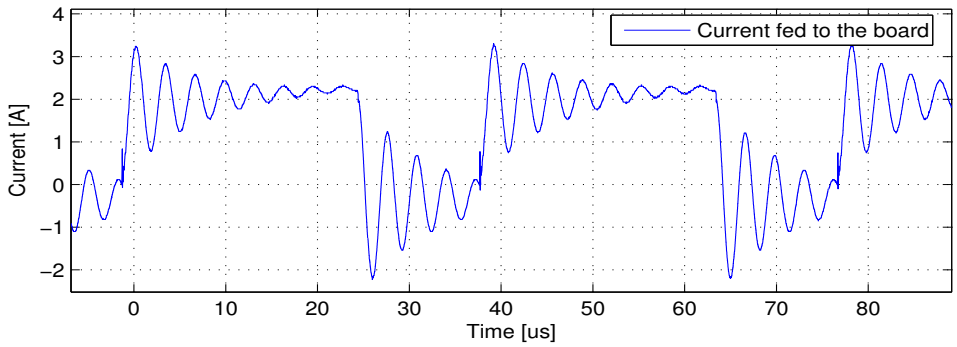

Figure 76 ***Measured DC link current with extra capacitor***

A third approach to the problem was to make the input inductance larger and thereby creating a current stiff source. An extra inductor was placed between the capacitors and the result was a resonant circuit with a much lower frequency, leading to an almost sinusoidal input current. Unfortunately, the stiffened current resulted in larger over voltage transients across the transistor, and an overall decrease of performance for the circuit.

Last, a first order low pass filter was designed and connected to the current feed. Since the oscillation had a frequency of about 300 kHz, a cut off frequency of 200 kHz was chosen. This is done in order to dampen only the oscillation, not the switching frequency current which can go up to over 100 kHz.

With the low pass filter the current oscillations showed to be considerably damped, having only a single overshoot as can be seen in Figure 77.

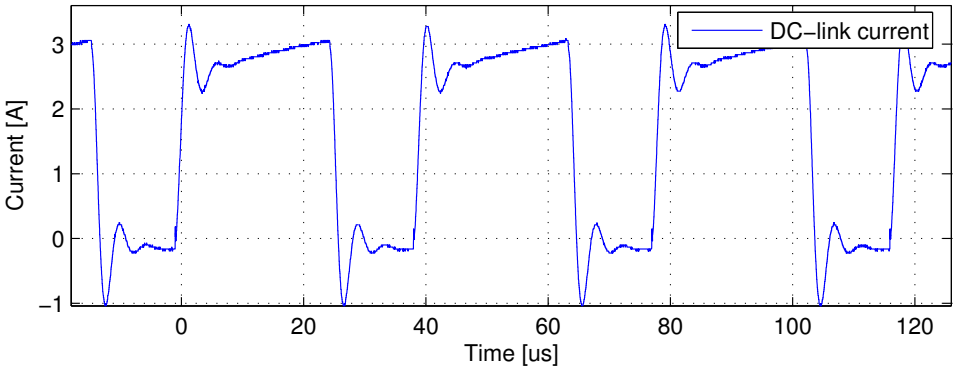

Figure 77 ***Measured DC link current with filter***

The low pass filter requires a resistance in series with the board causing high power loss. Even with a small resistance the power loss would be large when a high current runs through it. For instance, with a 0.1Ω resistance, the power loss would be 90W with a current of 30 amperes. This power loss is considered too high compared to the improvement of current wave forms.

From these results the best solution is to minimize the inductance. Although the low pass

filter gives a smoother current into the circuit, it leads to high power losses.

3.3.2.7 Circuit Oscillations

Because the stray inductances in the wires and copper traces form oscillating circuits with the capacitive properties of the components, many different oscillations can be observed in the current and voltage waveforms. By calculating the frequency of these oscillations, this data can be used to tune the simulation model to a higher level of accuracy.

3.3.3 Component Currents

A problem when measuring real life situations is that the current through various components and copper traces are almost impossible to measure without disturbing the circuit. Since current probes must enclose only the wire in which the current are to be measured, this is not possible to perform on a circuit board. If the current is flowing through a well defined resistor it is possible to measure the voltage drop and calculate the current from this. Unfortunately, when measuring the current through the switches and diodes, no known resistor is available. Another way is to add an extra wire loop out from the board and measure the current through it with a current probe. The wire will add extra inductance to the circuit but can be a way to get approximate values of the current. This method where used to mainly to locate the origin of the over voltage spikes that appear in the measurements. To verify that the wire loop didn't render the circuit unusable, the voltage drop across the component where measured both before and after the loop was connected. The measurement setup can be seen in Figure 78.

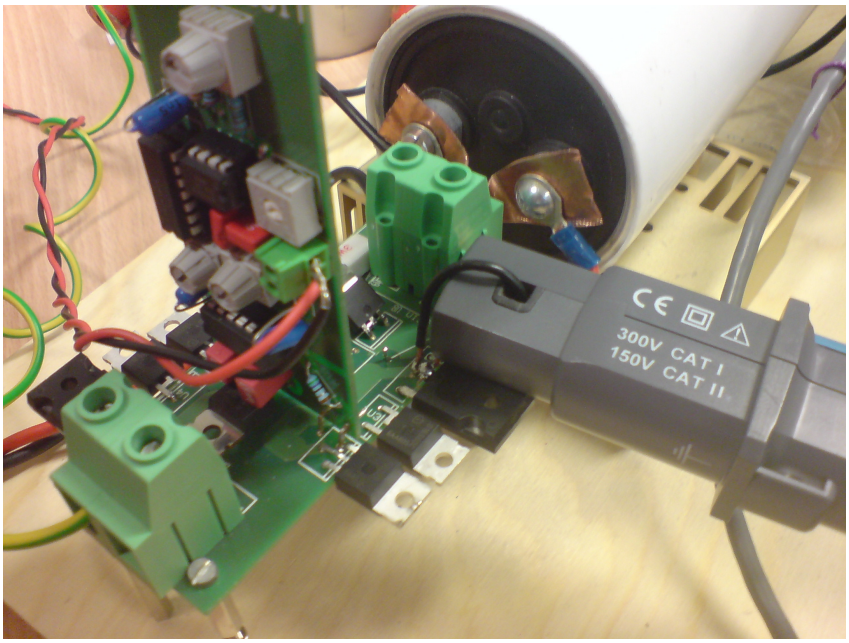

Figure 78 ***Measuring current through a series diode***

3.3.3.1 Component Losses

One attempt to calculate the component losses during operation was to measure the temperature of the component casing. The values for all the thermal resistances were given in each components specifications sheet, but since these values are a worst case, the actual components are much likely better. In an attempt to calculate a more accurate thermal

resistance, each component was tested with a known DC voltage and current. From this the exact power was calculated while the temperature was measured using a wireless temperature meter. The current where kept constant while the power and temperature where measured. Since most of the components have higher losses at higher temperatures, it was very important that the power and temperature where measured at exactly the same time. The calibration setup can be seen in Figure 79.

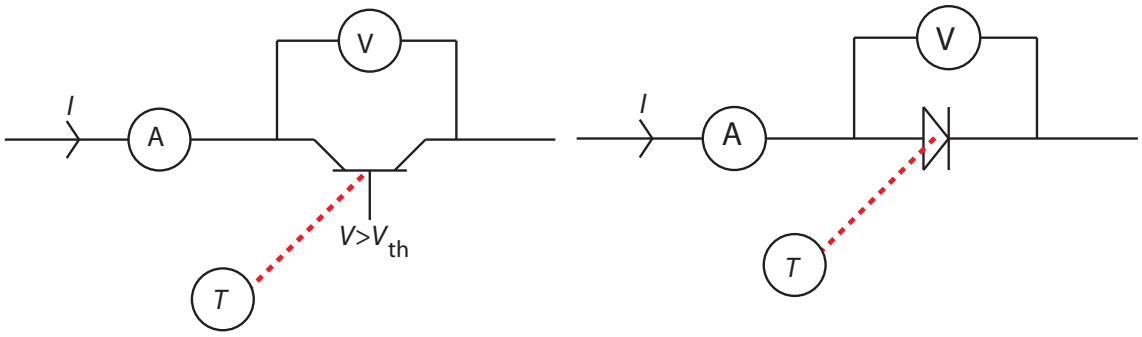

Figure 79 ***Calibrating thermal resistance for transistor (left) and diode (right)***

To obtain reliable measurement results proved to be problematic. The temperature meter was very sensitive to movement and different angels. Also, the temperature seemed to differ with tens of degrees depending at where on the component casing the temperature was measured. In an attempt to improve the results the casings where taped with black tape to have a homogenous surface finish. This proved to be of some help for stabilizing the measurements. The data acquired in these measurements can be seen for the transistors in Figure 80 and for the diodes in Figure 81.

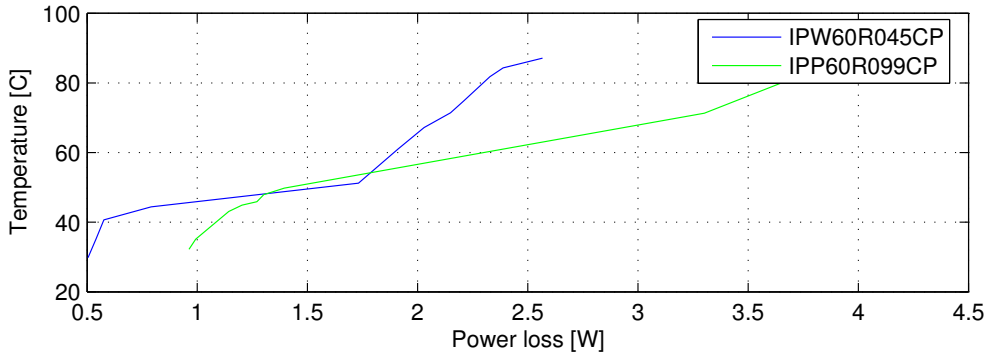

Figure 80 ***Temperature vs. power loss for the two transistors used***

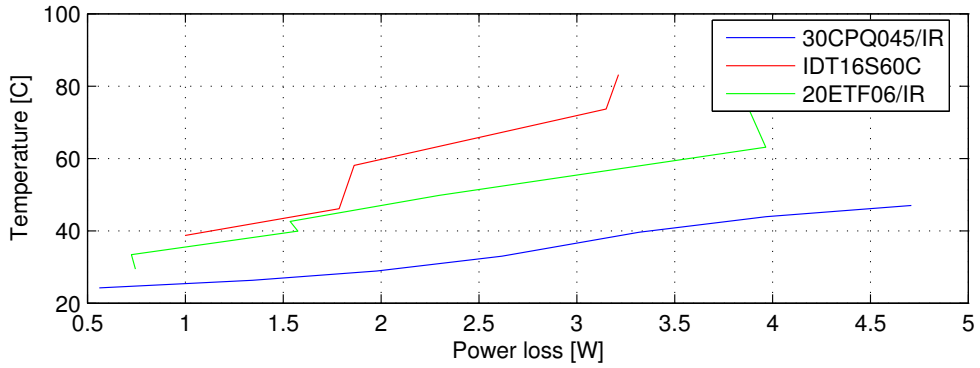

Figure 81 ***Temperature vs. power loss for the three diodes***

From Figure 80 and Figure 81 the assumption that the thermal resistance was lower than 63K/W were verified. However, measuring temperature with the non contact device does not give measurements stabile enough to use when calculating the component losses. At this time it was decided that these measurements wouldn't lead to any useful results.

The next approach to calculating the component losses was to observe the current and voltage waveforms during one whole period. By simply multiplying the voltage drop and current through each component, the power for each time instant would be found. The current was measured as described earlier in this chapter using an extra wire loop. The main problem with these measurements is that most of the power loss is in the form of extremely fast transients, with rise times in the length of only a few nanoseconds. When using probes with a bandwidth of only 50 megahertz, the possible phase shift and to slow sampling makes reliable calculations impossible.

3.3.4 Testing Limits

When all the interesting circuit dynamics were identified and well documented, the limits of the board were to be examined. The limit tests could be divided into two categories, one that included a major risk of destroying the circuit when exceeded, and one that would simply result in a malfunction. The tests that included a risk of destroying the circuit and components were maximum current, maximum voltage and minimum blanking time.

The tests that were likely to cause a malfunction without destroying the circuit are maximum switching frequency and minimum gate resistance.

3.3.4.1 Switching Frequency and Gate Resistance

The maximum frequency showed that the circuit were capable of switching frequencies of more than 100 kHz at voltages lower than 300 V. A switching pattern from this test can be seen in Figure 82. When, however, the voltage was raised, the drive circuit seemed to fail when the frequency approached 100 kHz. The drive circuit malfunction can be seen in Figure 83.

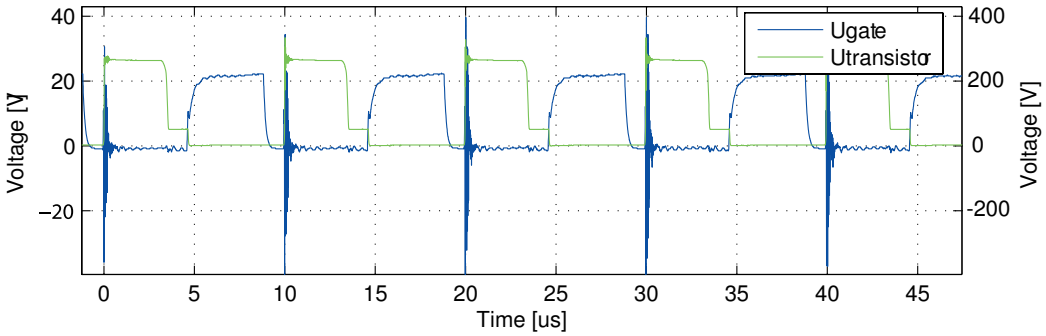

Figure 82 ***Measured gate- and drain-source voltage***

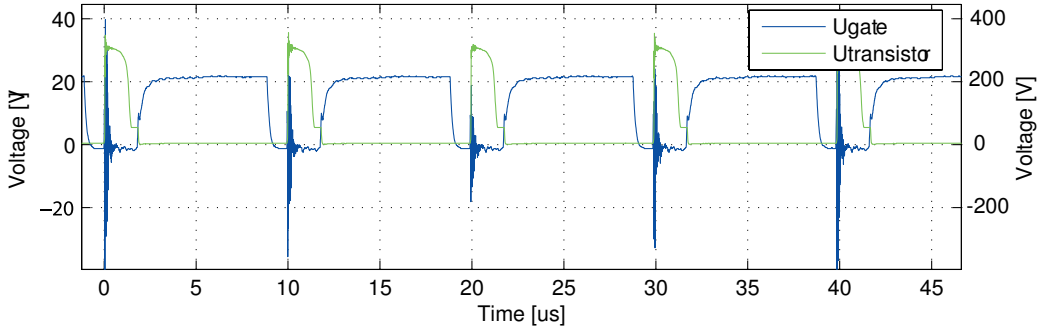

Figure 83 ***Measured gate and drain-source voltage malfunction***

To push the switching frequency higher, the gate resistance was reduced to half of its original value in an attempt to stabilize the gate voltage. This did not lead to any improvement in stability, but after a few minutes of operation, the drive circuit got overheated and broke down. When the drive circuit failed, the gate voltages were left floating. This allowed the CoolMOS to operate in its linear region with very high losses as a result. Almost instantly the temperature of the silicon got too high and the transistor broke down. This resulted in a short circuit through both transistors and the two diodes connected in series. The short circuit current destroyed all the components before the fuse in the transformer disconnected the circuit. A picture of the circuit board after the short circuit can be seen in Figure 84.

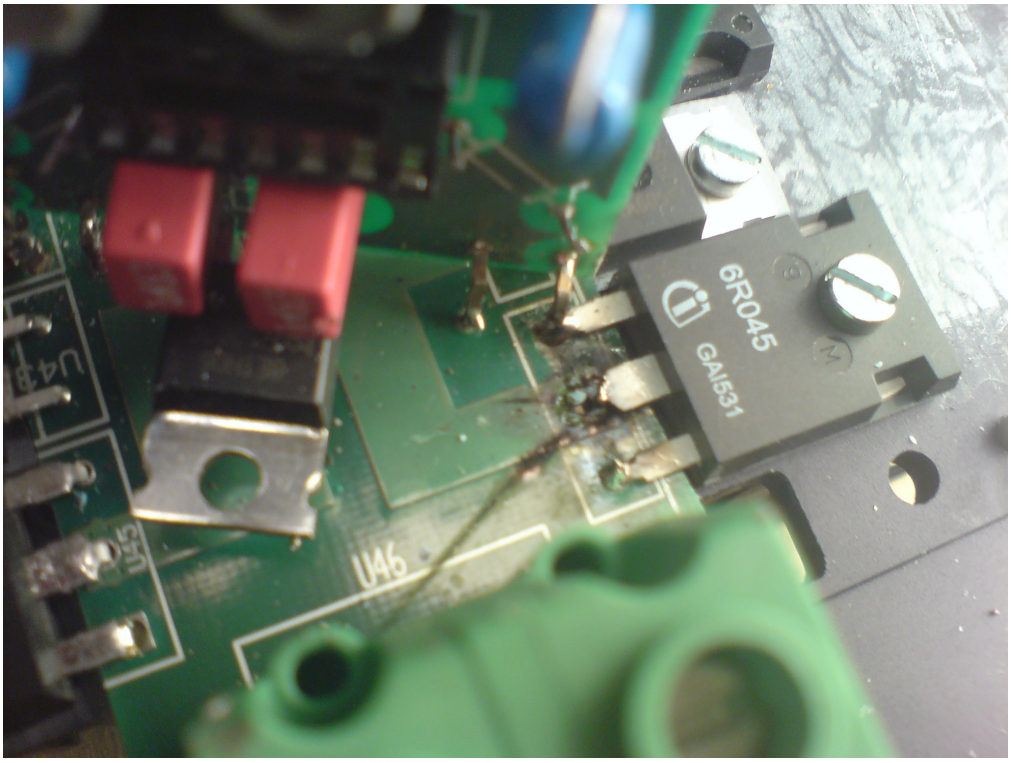

Figure 84 *The PCB after the break down*

3.4 Selecting Heat Sink Configuration for Semiconductor Casings

Some different heat sink configurations where considered before the high power tests could be executed. Three different setups are discussed below.

One large heat sink for all the components on one side, mounted with an isolating layer.

Positive

- Large heat sink resulting in a more efficient cooling, especially for the middle component
- Easy mounting
- No voltage on the heat sink

Negative

- The components will heat each other
- Impossible to measure the temperature of a specific component
- The isolating layer presents a higher thermal resistance

Separate heat sinks for each component, mounted with an isolating layer

Positive

- Possible to measure temperature of each component
- No voltage of the heat sink

- Little thermal interference between components

Negative

- Small heat sink area for each component

Separate heat sinks with no isolating layer

Positive

- Low thermal resistance
- Possible to measure the temperature of each component
- Little thermal interference between components

Negative

- Voltage on the heat sink
- Small heat sink area

From the analysis it was decided to use one large heat sink mounted with isolating layers.

4 Calculations

4.1 Calculations for the Drive Circuit

The drive circuit is designed around the UC3800 IC which creates the switching pattern and the IR2113 IC which is used to control the half bridge.

4.1.1 Setting the Switching Frequency

From the data sheet to the UC3800 IC the (2) was acquired. With a variable resistance of 0 to 200kΩ and a capacitor of 1.5nF, the switching frequency can be set to anything from 5kHz and upwards.

$$f = \frac{1.5}{R \cdot C} \tag{2}$$

4.1.2 Blanking Time

To achieve blanking time, an asymmetric RC network where connected between the PWM IC and the IR2113 drive IC. By using a variable resistance in the circuit, a variable blanking time where achieved. The component values where set so that the blanking time could be anything from two micro seconds and down to zero.

By letting the capacitor charge through the resistor, the drive IC will not turn on until the capacitor voltage reaches the trigger voltage of the input. Then, when the PWM IC voltage turns low, the capacitor discharges through the diode in virtually no time. Using (3) the blanking time was set to 2 microseconds or less.

$$\frac{U}{R} = C\frac{dV}{dt} \tag{3}$$

4.1.3 Decoupling

To stabilize the voltage around the PWM circuit, decoupling capacitors are used for the reference voltage and source voltage.

4.1.4 Boot strap

The upper transistor will, when conducting, have a source voltage of approximately the feeding DC voltage. This means that to get a gate-source voltage of 12V, it requires the DC-link voltage as offset. This is achieved with a so called boot strap configuration. The idea is that when the transistor is turned off, a capacitor is charged through a diode with the 12V gate voltage. Then, on turn on, the capacitor is connected to gate and source of the transistor, causing it to follow the source voltage. At the same time, the diode prevents the voltage from leaking to the low voltage side. The schematic can be seen in Figure 85.

The boot strap capacitors are supposed to charge the gate of the transistor and deliver leakage current during the on state. The capacitors where set to 1uF.

The diode is a quick switch diode so that there is time to charge the capacitor even at high switching frequencies.

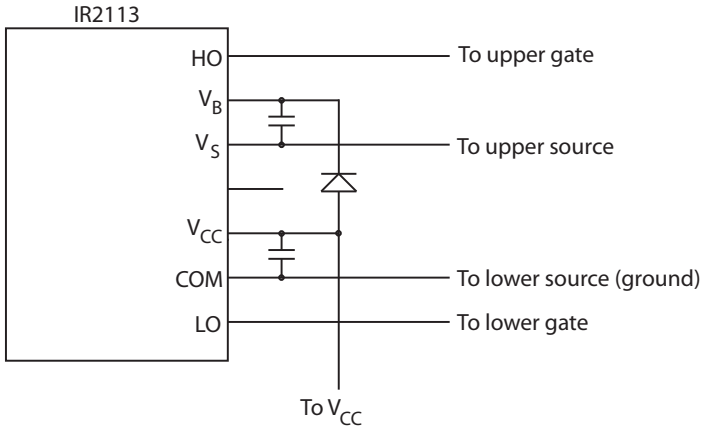

Figure 85 ***Boot strap capacitors and diode connected to the drive circuit***

4.1.5 Gate Resistance

Since the IR2113 are only rated to deliver a current of 2A, the current to charge the gate must be limited. At the same time it is crucial that the gate is charged as quickly as possible to avoid high switching losses. With a gate voltage of 12V and current limited to 2A, the gate resistance was set to 6.8Ω.

5 Conclusions

From the measurements and simulations it can be seen that the basic functions of the circuit is in order. The problem that can be seen throughout all the tests is the transients from the switching that appear at the transistors. The importance of minimizing stray inductance and capacitance in the design of switch mode converters can be observed directly in these results.

When running with higher switching frequencies, it becomes simpler to filter away the high frequency ripple. This result in smaller, lighter and cheaper filter inductors, which all three are factors that would suit the automotive industry well.

To minimize the inductance, the design cannot be done with discrete components. The entire bridge should be put in one power module based on mono crystalline silicon in a single chip. When all the components are on the same chip, no extra inductance from component legs and unnecessary copper traces will be added. The power module could then be controlled from a drive circuit connected via an optical connection to electrically isolate the control system from the high power module.

When running the circuit at high switching frequency with 300 V DC link, the drive circuit had problems with misfiring. This was most likely the results of EMI from the switching getting picked up by the gate driver. To prevent this phenomenon, the drive circuit could possibly be shielded from the main board. Another way to solve the problem is naturally to reduce the EMI with snubber circuits.

The SiC schottky diode has a relatively high voltage drop of two volts, but instead it can withstand a much higher frequency than a regular silicon diode. In the measurements it could be seen that the voltage transients where a bit smaller with the silicon switch diodes. The major difference between the diodes is the reverse recovery. One theory is that the current transient at switching can go down to ground through the lower free wheeling diode during its reverse recovery. Since the SiC diode has practically no reverse recovery, the voltage transient would be larger with this diode.

To improve the circuit even more, a more powerful drive circuit could be used. By adding an extra pair of transistors capable of delivering more current in between the gate driver and the gate, the switching could be even faster.

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