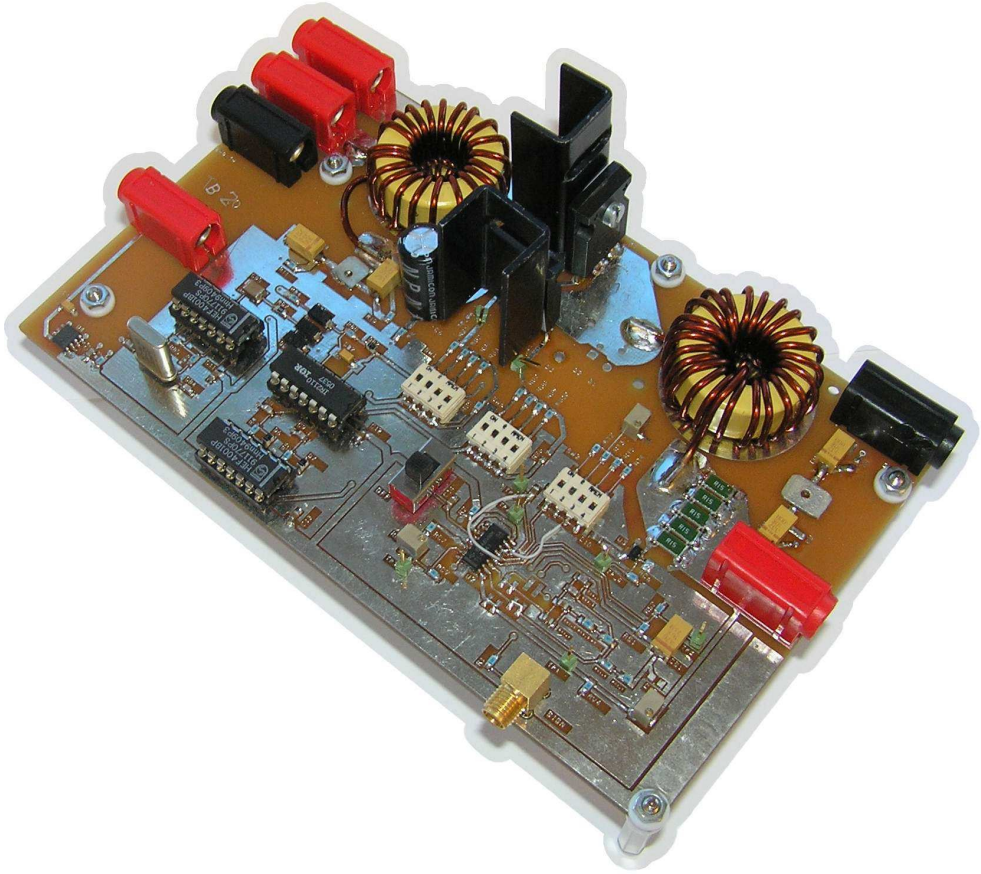
# EMI measurements and modeling

of a DC-DC Buck converter



*Master Thesis in Electrical Engineering by:*

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**Abstract**

This thesis report focuses on how the EMI behavior of a simple step-down or buck converter can be simulated. A very basic switching circuit is first examined and the knowledge gathered from this study, in terms of how parasitic and stray components can be modeled, is applied to a more complex step-down converter. A lot of work has been placed on implementing a detailed diode model in simulations, the Lauritzen model, the implementation proved difficult and requires more work. A second diode model, the modified charge control model, was implemented in order to produce more accurate EMI behavior from simulations that should be comparable to results from simulations were the Lauritzen diode model is properly implemented. EMI measurements was performed on the step-down converter according to the guidelines recommended by IEC in their CISPR 25 standard and these measurement results were then compared to those gathered from simulations.

**Keywords:** *EMC, EMI, Lauritzen diode model, SPICE, buck converter, modified charge control model.*

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# Acronyms

**ABM** Analog Behavioral Model

**ADE** Ambipolar Diffusion Equation

**ALSE** Absorber-Lined Shielded Enclosure

**AN** Artificial Network

**CISPR** Comité international spécial des perturbations radioélectriques

**DUT** Device Under Test

**EMC** Electromagnetic Compatibility

**EMI** Electromagnetic Interference

**ESL** Equivalent Series Inductance

**ESR** Equivalent Series Resistance

**EUT** Equipment Under Test

**FMC** Ford Motor Company

**IEC** International Electrotechnical Commission

**LISN** Line Impedance Stabilization Network

**MCC** Modified Charge Control

**MW** Medium Wave

**PCB** Printed Circuit Board

**PEEC** Partial Element Equivalent Circuit

**RPWM** Random Pulse Width Modulation

**SMPS** Switch-Mode Power Supply

**TB1** Testboard 1

**TB2** Testboard 2

**ZVT** Zero Voltage Transition

# 1 Introduction

## 1.1 Problem background

Potential problems related to Electromagnetic Interference (EMI) is a growing concern as more and more systems in our environment are being electrified. The problems related to EMI have of course been present for as long as the presence of electrical equipment, but nowadays electrical equipment is squeezed in to smaller volumes. Thus, potential problems are imminent if the design of each equipment or component is not properly considered. Everyone have probably noticed the annoying interference caused by cellular phones which gets amplified in sound equipment which can be seen as a tolerable disturbance. However if the interference was related to the airbag deployment of a car, life threatening situations can arise which of course is not acceptable.

As a consequence of the problems related to EMI, the concept of Electromagnetic Compatibility (EMC) was founded. EMC is basically the absence of effects due to EMI.

## 1.2 Purpose and goal

The purpose of this thesis is to investigate the electromagnetic (EM), properties of switching components by both simulations and measurements. This will hopefully provide information that makes modeling of EMI properties more accurate and give the reader an awareness of eventual design problems. Moreover, by comparing simulations of a detailed model with measurements of its physical counterpart, sources of EMI can more easily be identified. Identifying the magnitude of different contributions of interference can provide hints of how to approach problems of EMI. This awareness shall give the designer the possibility to deal with possible future problems at an early stage in the design phase.

## 1.3 Delimitations

The layout of circuits and components has a big influence on the overall performance of electrical equipment due to introduction of parasitic elements. However, the layout aspect is not the primary focus in this report; it is instead aimed at modeling individual components such as MOSFETs and diodes to determine how overall system performance is affected.

EMI is a very wide concept covering various types of different phenomenon. EMI can take form of both conducted and radiated emissions and thus can influence its surroundings in different manners. There are many aspects which have to be considered but this report only deal with two kinds of “EMI standards” or phenomenon: radiated RF emissions and conducted RF emissions. The Device Under Test (DUT) is thus only seen as a source of EMI and not as a victim.

The final results from this thesis, such as simulated intensities of EM-radiation are not assumed to match measurements to the last decimal value. They should rather point out trends and relative changes between different designs and simulation models.

# 2 Theoretical background

## 2.1 EMI and EMC

Electromagnetic Interference is defined by [1] which states that EMI is a: “Degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance.” EMI is thus, most often, an unwanted property but can also be a desired property in for example radio jammers which exploit the shortcomings of other equipment. As mentioned in the delimitation section, EMI is a wide concept and this report only focus at radiated and conducted RF emissions.

A definition of EMC is given in [1] which states that: “The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment.” Or more simply, electromagnetic compatibility is achieved when two devices can interact without disturbances. In other words must the manufacturer produce a system that is: not susceptible to interference from other systems, not susceptible to interference from itself, and not a source of interference to other systems.

### 2.1.1 Standards and legislations

A lot of different standards and legislations today address a range of different sectors and electrotechnical areas such as the civil, military and automotive sector etc. As this project was started by Volvo Cars AB and Chalmers, only standards and legislations concerning the automotive industry are further looked into. In this case, the CISPR 25 standard [2] and the Ford Motor Company (FMC) guidelines [3] are of special interest, for further reading see [4] and [5].

The guidelines used by Volvo Cars AB coincide very well with the guidelines established by the International Electrotechnical Commission (IEC) in their CISPR 25 standard. In fact some of the guidelines presented in the FMC document are direct references to the CISPR 25 standard e.g. the test verification and test set-up.

#### Ford motor company guidelines

The Ford Motor Company (FMC) guidelines concerning component and subsystem EMC [3] presents limits and methods of measurements which apply worldwide within FMC. The methods of measurement coincide well with those presented in the CISPR 25 standard, see section *CISPR 25* below, and thus only the limits concerning conducted and radiated emissions will be presented here. The conducted emissions falls under a category called CE420 in the FMC EMC document [3] and the radiated emissions under category RE310. Limits for each category are presented in Table 2.1 and 2.2. The level of emission in the tables is presented in units measured with different

**Table 2.1** – CE420, Conducted emissions requirements.

| Band # | RF Service | Frequency Range (MHz) | Limit Quasi-Peak dB$\mu$V |
|---|---|---|---|
| EU1 | Long Wave (LW) | 0.15–0.28 | 80 |
| G1 | Medium Wave (AM) | 0.53–1.7 | 66 |
| JA1 | FM 1 | 76–90 | 36 |
| G3 | FM 2 | 87.5–108 | 36 |

**Table 2.2** – RE310, Level 1 radiated emissions requirements.

| Band # | Frequency range (MHz) | Limit A Peak (dB$\mu$V/m)[a] | Limit B Quasi Peak (dB$\mu$V/m)[a] |
|---|---|---|---|
| M1 | 30–75 | $52-25.13\cdot Log(f/30)$ | $62-25.13\cdot Log(f/30)$ |
| M2 | 75–400 | $42+15.13\cdot Log(f/75)$ | $52+15.13\cdot Log(f/75)$ |
| M3 | 400–1000 | 53 | 63 |

[a] f=Measurement frequency (MHz)

types of detectors, peak and quasi-peak detectors; a description of each type of detector can be found in Appendix A.

Table 2.2 shows the limits for Level 1 requirements which is applicable to all FMC vehicle brands worldwide. Level 2 requirements are based on a specific brand or on specific market demands and will not be treated further in this thesis.

### CISPR 25

Comité international spécial des perturbations radioélectriques (CISPR), or in English: Special International Committee on Radio Interference, was founded in Paris 1934 by among others the IEC with the intent to document standard EMI measurement methods and to determine internationally acceptable noise level limits. The intention of the CISPR 25 standard can be found by looking at the title of the CISPR 25 document: "Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers"[1]. Thus these are the limits and methods of measurement which apply to most, if not all, electrical systems of a car. There are of course additional standards produced by IEC which concern other electrotechnical areas. As the FMC guidelines refers to the methods of measurement in the CISPR 25 standard, it is also of interest to look at the limits for disturbances in the CISPR 25 standard.

The FMC guidelines refer to specific methods of measurements in the CISPR 25 standard; voltage method in the case of conducted emissions and Absorber-Lined Shielded Enclosure (ALSE) method in the case of radiated emissions. The limits related to these methods are presented in Tables 2.3 and 2.4.

[1] IEC CISPR 25 ed.3.0 "Copyright ©2008 IEC, Geneva, Switzerland. www.iec.ch".

**Table 2.3** – Limits for broadband conducted disturbances according to CISPR 25. (Table courtesy of IEC.)

| Service /Band | Frequency MHz | Levels in dB($\mu$V) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Class 1 | | Class 2 | | Class 3 | | Class 4 | | Class 5 | |
| | | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak |
| BROADCAST | | | | | | | | | | | |
| LW | 0.15–0.30 | 110 | 97 | 100 | 87 | 90 | 77 | 80 | 67 | 70 | 57 |
| MW | 0.53–1.8 | 86 | 73 | 78 | 65 | 70 | 57 | 62 | 49 | 54 | 51 |
| SW | 5.9–6.2 | 77 | 64 | 71 | 58 | 65 | 52 | 59 | 46 | 53 | 40 |
| FM | 76–108 | 62 | 46 | 56 | 43 | 50 | 37 | 44 | 31 | 38 | 25 |
| TV Band I | 41–88 | 58 | - | 52 | - | 46 | - | 40 | - | 34 | - |
| Band | > 108 | Conducted emission - Voltage method not applicable | | | | | | | | | |
| MOBILE SERVICES | | | | | | | | | | | |
| CB | 26–28 | 68 | 55 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 |
| VHF | 30–54 | 68 | 55 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 |
| VHF | 68–87 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 | 38 | 25 |
| Band | > 87 | Conducted emission - Voltage method not applicable | | | | | | | | | |

**Table 2.4** – Limits for broadband radiated disturbances according to CISPR 25. (Table courtesy of IEC.)

| Service /Band | Frequency MHz | Levels in dB($\mu$V/m) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Class 1 | | Class 2 | | Class 3 | | Class 4 | | Class 5 | |
| | | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak | Peak | Quasi-peak |
| BROADCAST | | | | | | | | | | | |
| LW | 0.15–0.30 | 86 | 73 | 76 | 63 | 66 | 53 | 56 | 43 | 46 | 33 |
| MW | 0.53–1.8 | 72 | 59 | 64 | 51 | 56 | 43 | 48 | 35 | 40 | 27 |
| SW | 5.9–6.2 | 64 | 51 | 58 | 45 | 52 | 39 | 46 | 33 | 40 | 27 |
| FM | 76–108 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 | 38 | 25 |
| TV Band I | 41–88 | 52 | - | 46 | - | 40 | - | 34 | - | 28 | - |
| TV Band III | 174–230 | 56 | - | 50 | - | 44 | - | 38 | - | 32 | - |
| DAB III | 171–245 | 50 | - | 44 | - | 38 | - | 32 | - | 26 | - |
| TV Band IV/V | 468–944 | 65 | - | 59 | - | 53 | - | 47 | - | 41 | - |
| DTTV | 470–770 | 69 | - | 63 | - | 57 | - | 51 | - | 45 | - |
| DAB L band | 1447–1494 | 52 | - | 46 | - | 40 | - | 34 | - | 28 | - |
| SDARS | 2320–2345 | 58 | - | 52 | - | 46 | - | 40 | - | 34 | - |
| MOBILE SERVICES | | | | | | | | | | | |
| CB | 26–28 | 64 | 51 | 58 | 45 | 52 | 39 | 46 | 33 | 40 | 27 |
| VHF | 30–54 | 64 | 51 | 58 | 45 | 52 | 39 | 46 | 33 | 40 | 27 |
| VHF | 68–87 | 59 | 46 | 53 | 40 | 47 | 34 | 41 | 28 | 35 | 22 |
| VHF | 142–175 | 59 | 46 | 53 | 40 | 47 | 34 | 41 | 28 | 35 | 22 |
| Analogue UHF | 380–512 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 | 38 | 25 |
| RKE | 300–330 | 56 | - | 50 | - | 44 | - | 38 | - | 32 | - |
| RKE | 420–450 | 56 | - | 50 | - | 44 | - | 38 | - | 32 | - |
| Analogue UHF | 820–960 | 68 | 55 | 62 | 49 | 56 | 43 | 50 | 37 | 44 | 31 |
| GSM 800 | 860–895 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| EGSM/GSM 900 | 925–960 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| GPS L1 civil | 1567–1583 | - | - | - | - | - | - | - | - | - | - |
| GSM 1800 (PCN) | 1803–1882 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| GSM 1900 | 1850–1990 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| 3G/IMT 2000 | 1900–1992 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| 3G/IMT 2000 | 2010–2025 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| 3G/IMT 2000 | 2108–2172 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |
| Bluetooth/802.11 | 2400–2500 | 68 | - | 62 | - | 56 | - | 50 | - | 44 | - |

**Methods of measurement**

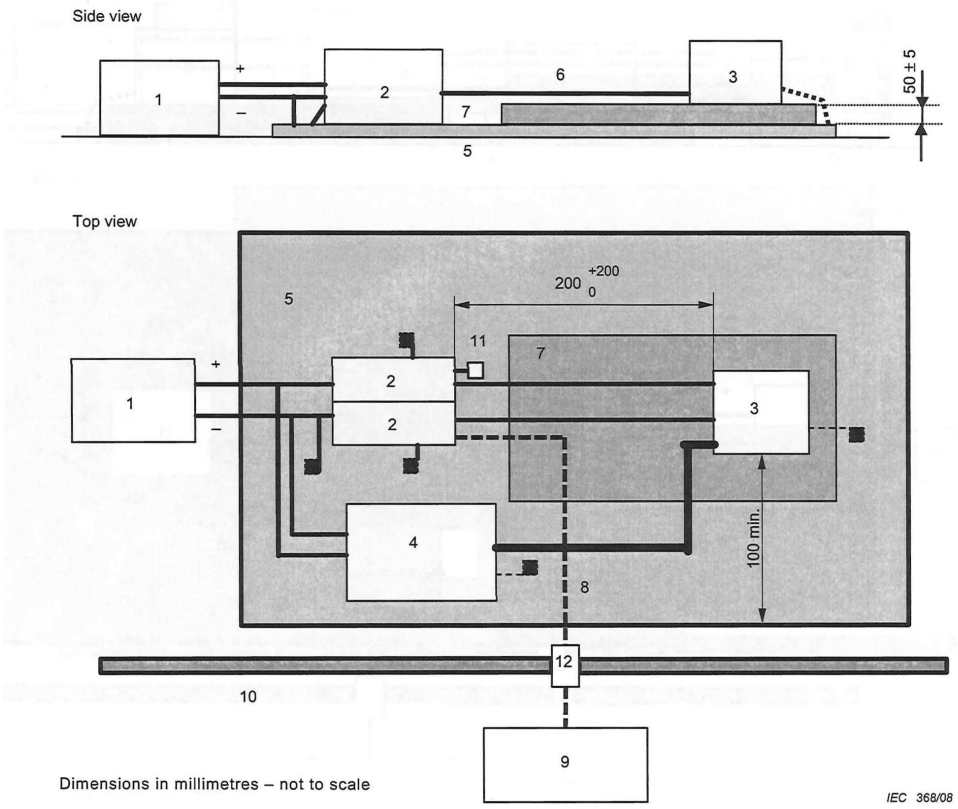
The measurements have to be made in such a way that the results are repeatable. The repeatability is insured by using a coherent and structured measurement setup, CISPR 25 state in great detail how measurements are to be made. Some of the contents in the method description in CISPR 25 is recited below[2] in order to give the reader basic knowledge of what to expect from it.

- "The Equipment Under Test (EUT) shall be placed on a non-conductive, low relative permittivity material ($\varepsilon_r \leq 1.4$), at $50 \pm 5$mm above the ground plane."
- "All sides of the EUT shall be at least 100mm from the edge of the ground plane. In the case of a grounded EUT, the ground connection point shall also have a minimum distance of 100mm from the edge of the ground plane."
- "The power supply line(s) between the connector of the AN(s) and the connector(s) of the EUT ($l_p$) shall have a standard length of $200^{+200}_{0}$mm."
- "The EUT shall be made to operate under typical loading and other conditions as in the vehicle such that the maximum emission state occurs. These operating conditions must be clearly defined in the test plan to ensure supplier and customer are performing identical tests."
- "The conducted emissions on power lines are measured successively on positive power supply and power return by connecting the measuring instrument on the measuring port of the related AN, the measuring port of the AN in the other supply lines being terminated with a 50Ω load."

These are just some of the points mentioned in CISPR 25 regarding measurement setup; by following the complete method description repeatable results can be assured. In addition to these points describing the arrangement and positioning of the DUT, power lines etc. there are figures showing the setup. In the conducted emissions case there are different setups depending on the situation e.g. whether the power return line is remotely or locally grounded and if the measurements are made according to the voltage or current probe method. There are also special measuring setups for the DUT connected to a load that is either an alternator or a generator and a special case for ignition system components. The setup for an EUT with power line remotely grounded and with measurements done using the voltage method can be seen in Figure 2.1.

In the list above, references are made to an Artificial Network (AN), which is more known as a Line Impedance Stabilization Network (LISN). A LISN is a low pass filter placed between the power supply and the EUT. A LISN provides the following properties to the measurement of the EUT: it filters the mains voltage and isolates the EUT from unwanted RF signals and noise, it maintains characteristic impedance to the EUT and it provides an easy way of measuring the

[2]IEC CISPR 25 ed.3.0 "Copyright ©2008 IEC, Geneva, Switzerland. www.iec.ch".




**Key**

1 Power supply (may be placed on the ground plane)
2 Artificial network
3 EUT (housing grounded if required in test plan)
4 Load simulator (metallic casing grounded if required in test plan)
5 Ground plane
6 Power supply lines
7 Low relative permittivity support ($\varepsilon_r \leq 1{,}4$)
8 High-quality coaxial cable e.g. double-shielded (50 Ω)
9 Measuring instrument
10 Shielded enclosure
11 50 Ω load
12 Bulkhead connector

NOTE The EUT housing ground lead, when required in the test plan, should not be longer than 150 mm.

**Figure 2.1** – Measurement setup for measurement of conducted emissions, EUT with power return line remotely grounded. (Figure courtesy of IEC.)

emissions generated by the EUT. This device is very important if the EUT is to comply with the emission levels. Two LISN's were constructed during the thesis to get a deeper understanding of the construction principles involved. The workflow and design of the LISN's is presented in section 3.

### 2.1.2 Reported examples of electromagnetic incompatibility

The following four examples are gathered from the EMC Journal website, see [6]. The examples are taken from real life and they all deal with problems due to electromagnetic incompatibility. For more non-automotive oriented examples see [6]. The succeeding two examples are gathered from [5] where additional examples can be found.

**Tuning car with tape - Banana skin 57**

A control cable to the engine management system of a motor car was damaged. This was repaired with a terminal block, but the engine ran rough. Wrapping the repair all over with EMC copper tape (conductive adhesive) made the engine run smooth again. (Arthur Harrup, Chief Engineer, William Tatham Ltd, Rochdale, 16th Feb 1999)

**Mobile phones triggers air bag - Banana skin 78**

78 Millions of motorists are risking their lives every time they use mobile phones while driving. New research has revealed (that) signals sent from mobiles can disrupt sophisticated electronic control units fitted in most modern cars. It is feared that, in some instances, this disturbance can scupper vehicles' braking and engine systems. One major manufacturer has also warned that transmissions from mobiles can trigger air bags fitted to the car.

**Video surveillance locks cars - Banana skin 144**

Gun Wharf, a leisure center in Portsmouth, opened in Easter 2001. It had an underground car park, and the car park had a video surveillance system. Electromagnetic emissions from the video system often interfered with car central-locking and security systems - locking the cars as soon as they were unlocked, or just not allowing them to be unlocked at all. Many people had to leave their cars in the car park and take taxis home. (From Anne Cameron, Alenia Marconi Systems, 6th July 01)

**Son of Star Wars - Banana skin 235**

The upgrading of the security and surveillance systems at the RAF Fylingdales base in Yorkshire is knocking out the electrical systems of expensive cars. High power radar pulses trigger the immobilising devices of many makes of cars and motorcycles - BMW, Mercedes and Jeep among them. Many have had to be towed out of range of the base before they can be restarted. The RAF admits it is a problem but says it is down to the car manufacturers to change their frequencies. However, Jeep claims this is not possible because of government restrictions.

**Fuel system stall due to FM transmitter**

A new version of an automobile had a microprocessor-controlled emission and fuel monitoring system installed. A dealer received a complaint that when the customer drove down a certain street in the town, the car would stall. Measurement of the ambient fields on the street revealed

the presence of an illegal FM radio transmitter. The signal from the transmitter coupled onto the wires leading to the processor and caused it to shut down.

**Brakes "lock up" while tuning radio transmitter**

Certain trailer trucks had electronic breaking system installed. Keying a citizens band[3] (CB) transmitter in a passing automobile would sometimes cause the brakes on the truck to "lock up". The problem turned out to be the coupling of the CB signal into the electronic circuitry of the braking system. Shielding of the circuitry cured the problem.

## 2.2 EMI mitigation techniques

Many strategies and techniques to mitigate emissions from electrical devices exist. An awareness of EMI shall always be present at an early design stage since relatively low efforts can reduce the cost and time needed to design a certain device. Depending on how far in the design process the product has come, the available mitigation techniques become more and more limited. If the device has already been produced, the only option that remain is either to patch it together with filters and shielding or in the worst case cancel the product. A better way to go is to design the device in a way that minimizes the EMI. A rule of thumb [8] in assigning emissions to its origin is that only one third of the emissions arises from the ideal circuit, the second third from parasitic elements in components and the last third from the PCB which include trace routing, component mounting and orientation/positioning of components. The effects of external parameters such as cabling and apparatus arrangements should of course not be neglected. Various types of "pre" and "post" actions in order to reduce EMI are presented in sections 2.2.1 to 2.2.5 together with references to previous work.

### 2.2.1 Shaping the switching waveform

Fast current and voltage transitions lead to broad frequency contents in the emissions from a Switch-Mode Power Supply (SMPS). The rise and fall times should thus be chosen with this fact kept in mind. A decrease in rise and fall time from the switching element, usually a MOSFET in low voltage SMPS-converters, is obtained by increasing the gate resistance. This is perhaps the simplest way of controlling the frequency contents in the SMPS. However an extended fall and rise time also give an increased power dissipation which needs to be considered if the efficiency and cooling is a critical issue.

This discussion of shaping the waveform coincides somewhat with the strategy mentioned in [9] where a Zero Voltage Transition (ZVT) technique is investigated which in theory promises

[3]Citizens' Band radio (CB) is, in many countries, a system of short-distance, simplex radio communications between individuals on a selection of 40 channels within the 27 MHz (11 meter) band [7].

reduced emissions. As the diode in a ZVT converter is softly turned on and off, both fast voltage transitions across the main switch and fast current change in the diode are avoided and the high frequency harmonics is reduced. The authors of [9] have compared a hard switched converter with a ZVT converter with the result that the ZVT technique only marginally reduce the emissions.

### 2.2.2 Random pulse width modulation

Mihalič and Kos [10] have showed that it is possible to reduce the emissions from a switched-mode DC-DC power converter by utilizing a Random Pulse Width Modulation (RPWM) technique. When RPWM is used, the switching harmonics are spread over a wider range compared to a conventional hard-switched power converter.

Studies have shown that RPWM is effective in reducing emissions from SMPS. The effects are best seen in the higher frequency domain were multiples of the switching frequency are transformed into a continuous density spectrum. The randomness needs to be created somehow which calls for additional components and computational power. By reducing the number of possible switching frequencies the pressure on computational power decreases while a reduced emission magnitude can be maintained [8].

### 2.2.3 Symmetrical switching

In [11], Paixao et al. have presented a switching strategy which reduces the EMI produced by the circuit. The strategy is known as “symmetrical switching”; a name that describes the strategy pretty well. By using two tuned and synchronized switches, in this case a N-channel and a P-channel MOSFET, the radiated and conducted EMI is cancelled or reduced as the variations in electric field on each load conductor are canceled out due to the phase-shift.

### 2.2.4 Shielding

Shielding is one way to patch a device suffering from problems caused by EM-noise. An external shield can reduce the coupling of radio waves, electromagnetic fields and electrostatic fields, though not static or low-frequency magnetic fields. The amount of reduction depends very much upon the material used, its thickness, and the frequency of the fields to be shielded. Shielding is of course a very effective way in reducing the radiated emissions but if the possibility exists shielding should be kept to a minimum as it is expensive. Shielding in combination with a well designed circuit should produce a device that is likely to show good EMC behavior. Further reading about shielding can be found in [4].

### 2.2.5 Filtering

Applying a filter to the input or output terminals of an electronic or device is, just as shielding, a very effective way of reducing EMI. Adding filters to a device adds both weight and volume and thus also cost. Basic filter theory can be found in [4] and a thorough walkthrough in designing both input and output filters is presented in [12].

## 2.3 EMI Modeling

Assessing EMI during the design process is not an easy task if high accuracy is the goal. Simulation tools are an invaluable asset if they can simplify the design process, reduce project cost and the time frame needed to finalize a project. This section presents some strategies where modeling of EMI is in focus.

### 2.3.1 Mapping contributions

The authors of [13] presents a strategy to assess the EMI emitted from an SMPS. Each component is not modeled in a way which generates time-domain data. The individual sources of EMI is mapped in a way so that the designer can add the different contributions together and thus get a picture of the magnitude of the total emitted EMI.

### 2.3.2 Modeling of layout parasitic elements

The authors of [14] shows a way to forecast the EMI emitted from a DC-DC converter taking all parts of the converter into consideration. All parts refer to switching components, Printed Circuit Board (PCB) layout and passive components. The switching components are modeled by conventional models in Saber® with parameters extracted in a way described by [13] above. The passive components are first measured by an impedance bridge and then modeled by an electrical equivalent circuit. The PCB layout is modeled by a Partial Element Equivalent Circuit (PEEC) modeling software and together they form a complete converter.

## 2.4 Modeling of typical converter components

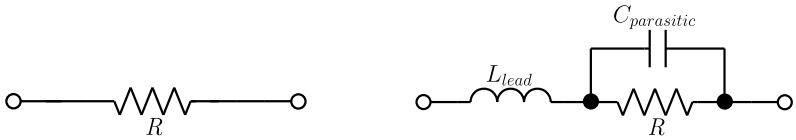
To accurately model an electric circuit, all details influencing its behavior have to be represented in the model. A passive component can no longer be regarded as a perfect resistor, inductor or capacitor, as the frequency contents of the signal or current/voltage increases. For example a resistor begin to behave more and more like an inductor. As the frequency is increased, or decreased depending on the reference point, all parts of the circuit begins to suffer from a be-

havioral change. The PCB itself could start act as a very effective antenna at a certain operating frequency.

If accurate, or at least more realistic, emission results are expected from simulations it is not enough to use conventional component models available in circuit simulation packages such as SPICE. These models needs a refinement in the aspect of details and behavior as they often exhibit a behavior that is not adapted to high power applications such as those found in an SMPS. The behavior of the MOSFET and diode are presented in the following sections which emphasize the shortcomings of the conventional models.

### 2.4.1 Resistor

If a resistor's behaviour at higher frequencies needs to be accounted for, a more detailed model than the ideal one has to be used, see Figure 2.2.a. One way to model the resistor in a better way is depicted in Figure 2.2.b. The frequency response of the impedance for both models can be seen in Figure 2.3, the phase characteristics also changes with frequency, although not presented here. Resistors can be constructed in different ways; the most common types of resistors are carbon composition, wire wound and thin film where each type has its benefits and drawbacks [5].




2.2.a: Ideal resistor model.

2.2.b: Nonideal resistor model with parasitic capacitance and lead inductance.

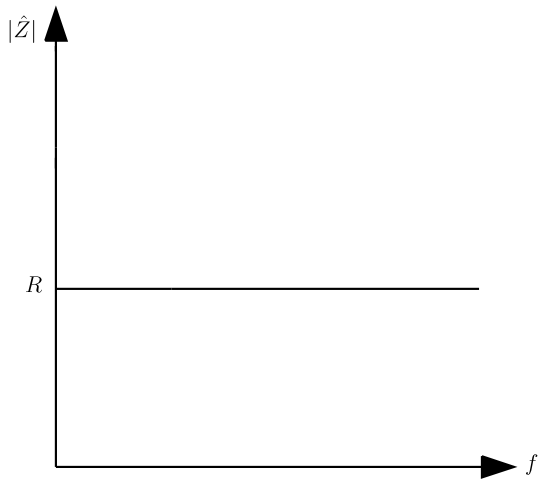
**Figure 2.2** – Ideal resistor (a) and a nonideal resistor (b).

### 2.4.2 Capacitor

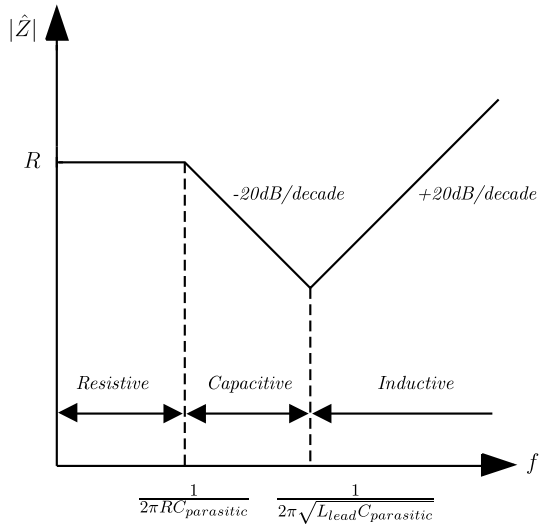
A common way of modeling capacitors at higher frequencies is depicted in Figure 2.4.b with the corresponding frequency response seen in Figure 2.5.b. Just as for the resistor, there are many different types of capacitors depending on production techniques, see [5], thus are some types more suitable for certain types of applications.

### 2.4.3 Inductor

A common way of modeling inductors at higher frequencies is depicted in Figure 2.6.b with the corresponding frequency response seen in Figure 2.7.b.

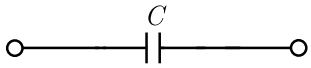



2.3.a: The impedance of the ideal resistor plotted against frequency.

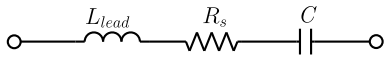



2.3.b: The impedance of the nonideal resistor plotted against frequency.

**Figure 2.3** – The frequency dependence of the impedance for the two resistor models, ideal (a), nonideal (b).




2.4.a: Ideal capacitor model.




2.4.b: Nonideal capacitor model with equivalent series resistance, or ESR, and lead inductance.

**Figure 2.4** – Ideal capacitor (a) and a model of the nonideal capacitor (b).

### 2.4.4 PCB strip inductance

Interconnections between components on a PCB are all of different shapes and length which means that each segment has to be considered to be a unique component. [15] describes an equation for a flat strip over a ground plane. A relatively accurate inductance model of the strip can be expressed as.

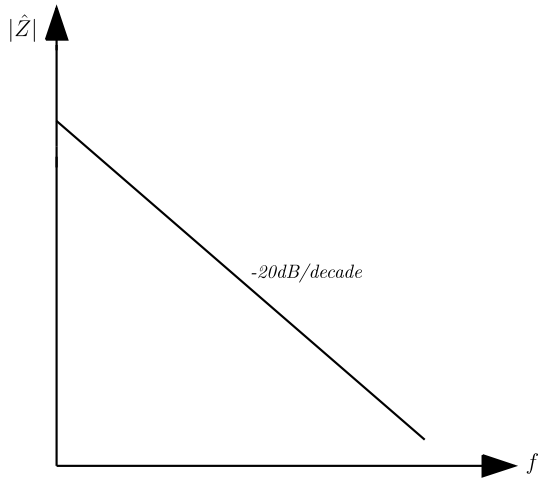
$$L = 0.0002b\left[ln\left(\frac{2b}{w+h}\right)+0.5+0.2235\left(\frac{w+h}{b}\right)\right] \tag{2.1}$$

where L = inductance in $\mu$H, b = length in mm, w = width in mm and h = thickness in mm.

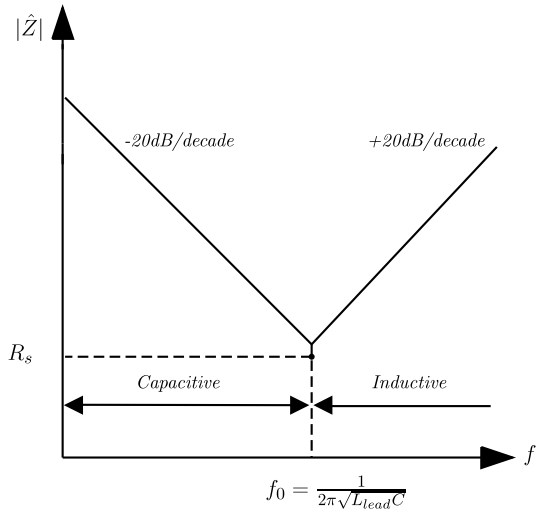
### 2.4.5 Wires and leads

All wires and leads present on the PCB are assumed to have a circular cross section, this is of course a simplification, and thus the following equation presents the model of the inductance [4].

$$L = 0.0002l\left[ln\left(\frac{2l}{r}\right)-0.75\right] \tag{2.2}$$

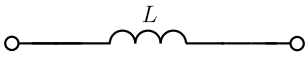



2.5.a: The impedance of the ideal capacitor plotted against frequency.

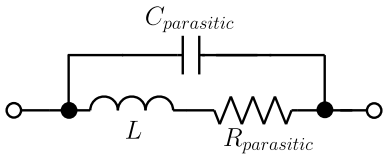



2.5.b: The impedance of the nonideal capacitor plotted against frequency.

**Figure 2.5** – The frequency dependence of the impedance for the two capacitor models, ideal (a), nonideal (b).




2.6.a: Ideal inductor model.




2.6.b: Nonideal inductor model with parasitic resistance and lead elements.

**Figure 2.6** – Ideal inductor (a) and a model of the nonideal inductor (b).

where L = inductance in $\mu$H, r = wire radius in mm, l = wire length in mm.

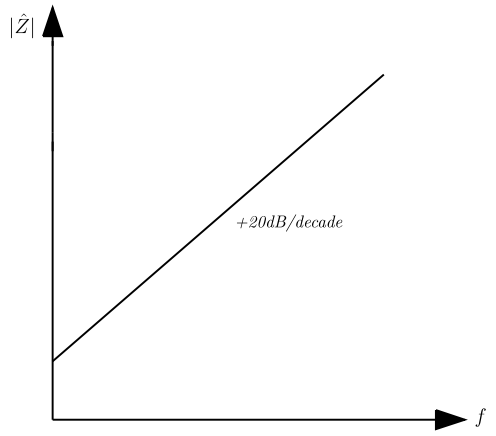
In the case that there are a pair of parallel conductors the mutual inductance can be found from

$$M = 0.0002l\left[ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right] \tag{2.3}$$

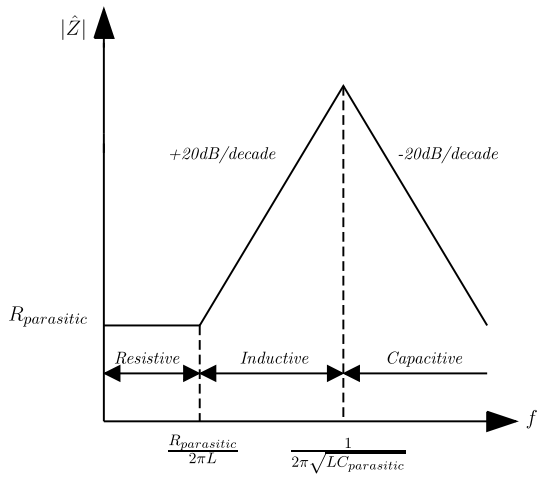
where M = mutual inductance in $\mu$H, l = wire length in mm, D = distance apart in mm, for D/l<<1.

### 2.4.6 Diodes

If the conventional SPICE diode model is used to simulate a high-voltage high-current diode, the transient response obtained is not fully adequate. During the past 20 years a number of new models for the power diode have been proposed [16]. However, for the practicing engineers, the most pressing issue is which of these models to adopt for their computer-aided design as they want reliable models that are easy to use. Issues which has to be considered when choosing a model is accuracy of simulated results, validity range of the model, compatibility with existing




2.7.a: The impedance of the ideal inductor plotted against frequency.




2.7.b: The impedance of the nonideal inductor plotted against frequency.

**Figure 2.7** – The frequency dependence of the impedance for the two inductor models, ideal (a), nonideal (b).

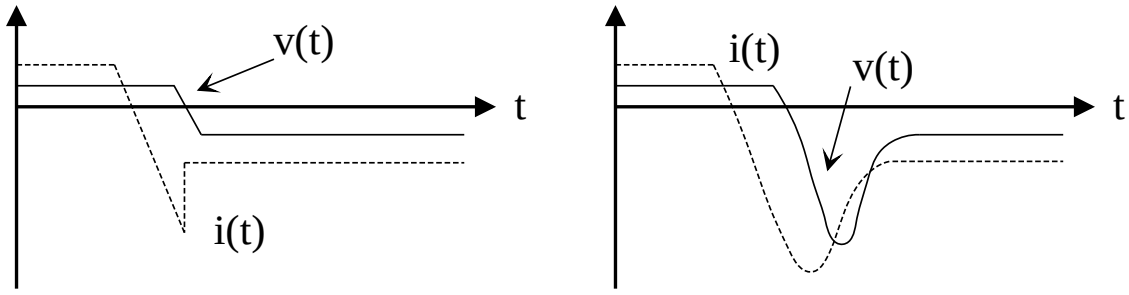
simulators, implementation know-how, availability of model parameters, parameter extraction techniques and CPU-time required which is related to convergence performance of the model.

This section presents two shortcomings of the conventional diode model; reverse and forward recovery, and different modeling approaches to overcome these shortcomings. A more detailed presentation of two diode models referred to as the Lauritzen model and the Modified Charge Control (MCC) diode model will be given in section 4.

### Forward and reverse recovery

The conventional diode model used in circuit simulators such as SPICE is based on the original charge control model [17]. This model include the effects of minority charge storage during reverse recovery but it does not include the reverse recovery itself. Diodes modeled in this way exhibit an instantaneous recovery during commutation when the single charge-node becomes depleted and lacks the effect of soft reverse recovery, see Figure 2.8. The reverse recovery occurs when a forward conducting diode is turned off rapidly and the internally stored charges cause a reverse current to flow at high reverse voltage. If the reverse recovery can be successfully modeled during the design phase of the circuit, information concerning both power dissipation and EM emissions would most likely better correspond to reality. The reverse recovery phenomenon is present in most of the diodes available but the reverse recovery time, $t_r$, can differ much between different types of diodes. Schottky diodes have a very short recovery time since they are majority carrier devices and do not suffer from minority carrier storage problems.

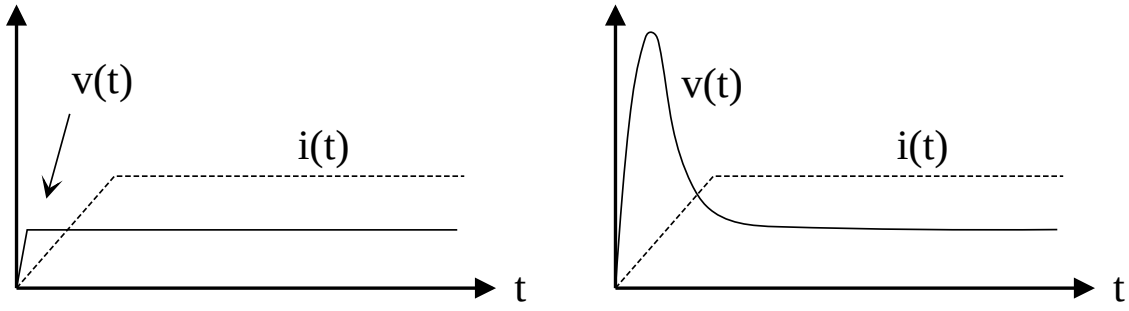
Forward recovery occurs, in opposite to reverse recovery, during commutation from blocking to the conductive state. During turn-on, a high forward voltage builds up across the intrinsic region (i) because of the initially low conductivity. As the injected carrier concentration increase, the voltage across the i-region soon decrease to a normal steady state diode forward drop. Thus




2.8.a: Without reverse recovery. 2.8.b: With reverse recovery.

**Figure 2.8** – Current through and voltage over diode during turn-off without and with reverse recovery respectively.

forward recovery only occurs in diodes with an intrinsic or “near intrinsic” region such as PiN-diodes which are commonly used in high voltage applications.




2.9.a: Without forward recovery. 2.9.b: With forward recovery.

**Figure 2.9** – Diode during turn-on without and with forward recovery respectively.

### Diode models

A major difference between available models is how the model is formulated, in other words, whether the model is based on physical or analytical principles. Generally speaking can all models be classified as either micromodels or macromodels. Micromodels are closely based on the internal device physics and, if properly formulated, yield good accuracy over a wide range of operating conditions [16]. Because device physics unavoidably require mathematical equations, micromodels are also known as mathematical models. Macromodels on the other hand, reproduce the external behavior of the device largely by using empirical techniques without considering the geometrical structure and the internal physics of the diode.

Table 2.5, taken from [16] with some modifications, summarizes some of the diode models published during the nineties. The model classes analytical, numerical, hybrid and empirical all fall under the micromodel category. Micromodels are generally more computationally efficient, more accurate and more related to the device structure and fabrication process. Macromodels were frequently reported in literature before the nineties but because of their limitations concerning accuracy and flexibility they are rarely used nowadays [16].

**Table 2.5** – Summary of various power diode models, [16].

| Model | Year | Applicabilities | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Type of diode | | | Rating of power diode | | | DC | Simulator type | | # of input | Parameter[c] |
| | | p-i-n | p-v-n[a] | p+n/n+ | low PIV[b] | high PIV | high current | | PSPICE | Saber | parameters | extraction |
| **Analytical model** | | | | | | | | | | | | |
| Liang | 1990 | | | x | x | | | | x | | 7 | yes |
| Lauritzen | 1991 | x | | | x | | | | | x | 5 | yes |
| Jin | 1991 | x | x | | | | | | | x | 4 | yes |
| Kraus | 1992 | x | x | | x | x | x | x | | x | 17 | no |
| Ma I | 1993 | x | | | x | | | x | | x | 9 | yes |
| Ma II | 1993 | x | x | | x | | | x | | x | 6 | yes |
| Yang | 1994 | | | x | | | | | | x | 7 | no |
| Tseng I | 1994 | x | x | | x | | | x | x | x | 6 | no |
| Analogy | 1995 | x | x | | x | x | x | x | | x | 59 | no |
| Strollo | 1996 | x | x | | x | x | x | x | x | | 20 | no |
| Ma III | 1997 | x | x | | x | x | x | x | | x | 8 | yes |
| Tseng II | 1997 | x | x | | x | x | | | x | x | 8 | no |
| **Numerical and hybrid model** | | | | | | | | | | | | |
| Vogler | 1992 | x | x | | x | x | x | x | | x | 26 | yes |
| Winterheimer | 1992 | | | x | x | x | | | | | 6 | no |
| Goebel | 1992 | x | x | | x | x | x | x | | x | 11 | no |
| **Empirical model** | | | | | | | | | | | | |
| Bertha | 1993 | x | x | x | x | x | x | x | x | | 18 | yes |

[a] The n- region is referred to as a v region and the resulting diode as a p-v-n diode.
[b] Peak inverse voltage, the specified maximum voltage that a diode rectifier will block.
[c] Availability of parameter extraction procedure.

Numerical models use a partial differential equation set describing the semiconductor physics and solves them using finite-element or finite-difference methods. These equations describe the physical behavior within the semiconductor, consisting of carrier drift and diffusion components, carrier generation and recombination effects and the relationship between space charge and electrical field. The semiconductor parameters needed to properly incorporate a model of this type requires data not commonly provided by the manufacturer; e.g. doping profile and doping levels. This makes numerical models more suitable for device manufacturers who want to evaluate the performance of their devices. In [18] the authors present a numerical model based on the Ambipolar Diffusion Equation (ADE)[4]. In [19] the same authors present the same model integrated in a SMPS and state that the parameters needed can be extracted by curve fitting results from standard characterization measurements.

Analytical micromodels rely on a set of mathematical functions that describe the devices' terminal characteristics without resorting to FEM calculations; diode and transistor models used in SPICE is modeled in this way. The computational demand of analytical models are far lower then the demands on the numerical models which gives an important advantage if the model is to be used in a complex design.

The hybrid model is a combination of a numerical and analytical approach. The idea is to use fast numerical algorithms that solves the semiconductor equations in the drift region only and then apply analytical equations to the rest of the device structure. This combination has the advantage of simulation with high accuracy of charge carrier behavior but without the long execution time.

The modeling approaches presented above all rely on accurate parameter extraction, the simulation accuracy are more due to the accuracy of the input parameters rather then due to the model itself. In the conclusions of [16] the following is said: "Although the rate of publication of papers containing power diode models has been tapering off in the last few years, this does

[4]The dynamics of the carrier concentration can be described by the Ambipolar Diffusion Equation.

not indicate all outstanding issues have been resolved.", and even though this was said almost 10 years ago, this statement holds true today.

### 2.4.7 MOSFET

As it, evidently, is not trivial to model the diode in an accurate and satisfying way it would be more than surprising if it was so for the MOSFET. This section presents some of the most commonly used MOSFET models for the SPICE simulator together with a short description of the model with its strengths and shortcomings. It should be noted that simulations performed later on in this report will only use conventional models made available by the manufacturer, what type of model used will be clearly stated.

#### Level 1

The level 1 SPICE MOSFET model is the original model developed in the beginning of 1960's. It is the simplest and most basic of all models and is also known as the Shichman-Hodges model. The equations describing the model are simple and produces results that are mostly idealized. Because of its simplicity, it has many limitations. Among the limitations is the lack of voltage-dependent capacitance which is modeled using the Meyer model which thus is not a charge-conserving model [20]. The lack of detail limits the model's ability to accurately simulate switching events.

#### Level 2

This model covers several short-channel effects but because of the complicated mathematical implementation it suffers from many convergence problems. The voltage-capacitance relation can be approached in the same manner as in the Level 1 model, using the Meyer model, but it can also be approached using the Ward-Dutton model which is a charge-conservative model. The Ward-Dutton model forms the backbone of all present models [20].

#### Level 3

The fundamental equations for this model are formulated in the same way as for the Level 2 model although the implementation uses simplifications such as Taylor series expansion which results in more manageable equations. Many of the equations used are empirical which gives a model that is both precise and easily implemented but as empirical equations are used the model is not very scalable between different power levels. The model has proven to be robust and is popular for digital circuit design.

### BSIM models

BSIM is an acronym for Berkeley Short-Channel IGFET Model. There are many BSIM model versions available and the first versions placed less emphasis on the exact physical formulation of the device and instead used empirical parameters and polynomial equations to handle various physical effects. This approach generally leads to improved circuit simulation behavior compared to previous models. Models of type Level 1 through 3 are generally referred to as first generation models which emphasizes on device physics. As these models focus on an accurate physical formulation, the mathematical representation is often complex leading to numerical problems during simulation. The first BSIM models, often referred to as second generation models, solves these convergence problems by an increased focus on mathematical implementation. Empirical parameters without physical meaning are thus introduced which weakens the link between model parameters and manufacturing technique. This makes the device parameter extraction difficult, on the other hand this can be seen as a protection for the manufacturers as they make reverse-engineering of their product difficult.

In addition to the model types mentioned here, many more exist. See Appendix B for a list of available MOSFET models.

# 3 Test equipment

This section presents a description of the measuring equipment used throughout this thesis work. The equipment used to obtain certain results will be mentioned throughout the rest of this report only with reference to the name of the equipment in question.

## 3.1 General test equipment

- *Spectrum analyzer*
  The spectrum analyzer used was a HP 8591EM EMC Analyzer with a frequency range of 9kHz-1.8GHz.
- *Oscilloscope*
  An oscilloscope of the type Tektronix TDS2004B was used. It has 4 channels, a bandwidth of 60MHz and a sampling rate of 1GS/s.
- *Function generator*
  Wavetek 10MHz DDS function generator model 29.
- *RCL meter*
  Philips PM 6303 RCL meter, 1kHz measuring frequnecy
- *Agilent 8753ES S-parameter Network Analyzer*
  This network analyzer was available at Volvo Cars AB.
- *Schwarzbeck Mess - Elektronik, Single path Vehicle LISN NNBM 8126-A*
  LISN according to CISPR 16 ($5\mu$H+5$\Omega$||50$\Omega$). Two units were available, serial number 124 and 125, and they are both the property of Volvo Cars AB.

## 3.2 Artificial mains network

As mentioned in section 2.1.1, it is recommended to do all measurements in combination with an artificial mains network. To acquire a deeper understanding of the construction principles involved two LISN's were constructed during the thesis. This section presents the design flow of the LISN and also some measurements which validates its functionality.

### 3.2.1 Construction of LISN

Using the schematic seen in Figure 3.1 as a starting point [2], and selecting appropriate components the LISN could be built.

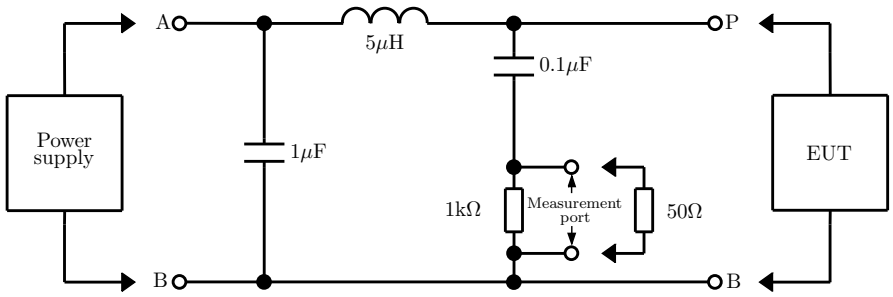



**Figure 3.1** – Schematic of a LISN or AN required for measurements according to the CISPR 25 standard. EUT refers to, just as DUT, to the device under test. (Figure courtesy of IEC.)

### Choice of components

A single layer air coil was chosen for the inductor. The air coil inductor is unaffected by the current it carries and thus it has a more linear behavior providing lower distortion. The coil was constructed using only one layer because of the lower self-capacitance and higher resonant frequency in comparison with multi layer coils. It was constructed by winding a 1.6mm copper conductor on a piece of PVC tubing. The finalized coil was measured to 5.2$\mu$H at 100kHz using a RCL meter.

The 1$\mu$F capacitor in Figure 3.1 was realized by combining three smaller ones in parallel: one 0.68$\mu$F MKP, metalized polypropylene, capacitor and two FKP, polypropylene, capacitors with values 0.22$\mu$F and 0.1$\mu$F.

The 0.1$\mu$F capacitor was chosen to be a metalized polypropylene precision capacitor of 0.1$\mu$F.

A metal film resistor of 1k$\Omega$ was chosen as the measurement port resistor. The metal film resistor gives low noise and high stability.

The components were soldered onto a copper board which was handtooled to get the right layout. The finalized LISN can be seen in Figure 3.2.

**Figure 3.2** – The inside of the finalized LISN and two LISN's in their casing.

### 3.2.2 Validation of LISN

To assure that the self constructed LISN performs well, a validation was performed using the Agilent S-parameter network analyzer. In order to obtain accurate measurement results the network analyzer was calibrated while connected to the measurement fixture required to interface the DUT. The cables, adapters and the positioning of the DUT was kept fixed at a certain position for all measurements.

Besides from doing measurements on the newly built LISN's, measurements were also made on the LISN's available at Volvo Cars AB. It should be noted that the LISN's at Volvo Cars AB are to comply with CISPR 16 rather than CISPR 25 and because of this they do not match in behavior. The results can still be of interest to the reader for comparative reasons.

The results from the measurements can be seen in Figure 3.3 and 3.4, the upper and lower tolerance limits of the impedance refers to the tolerance of $\pm 20\%$ mentioned in the CISPR 25 document [2].

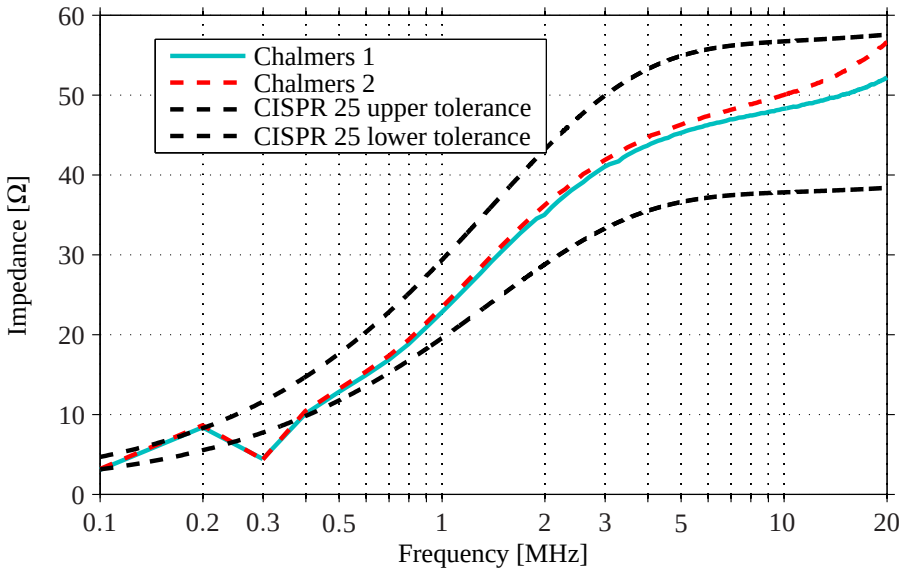



**Figure 3.3** – Results from measurements on the self constrcuted LISN.

Figure 3.3 and 3.4 shows the impedance up to 20MHz, above this point the impedance of the constructed units (denoted as "Chalmers 1" and "Chalmers 2") head towards 100Ω instead of 50Ω. There are also some clear deviations at 200kHz and 300kHz which extends beyond the tolerance limits. Judging from these measurements using the constructed LISN's below frequencies of 20MHz will satisfy the CISPR 25 standard.

## 3.3 Diode tester

The diode tester is a device that can be used to characterize diodes. The characterization is accomplished by letting an inductive current freewheel in the diode and then reverse biasing it

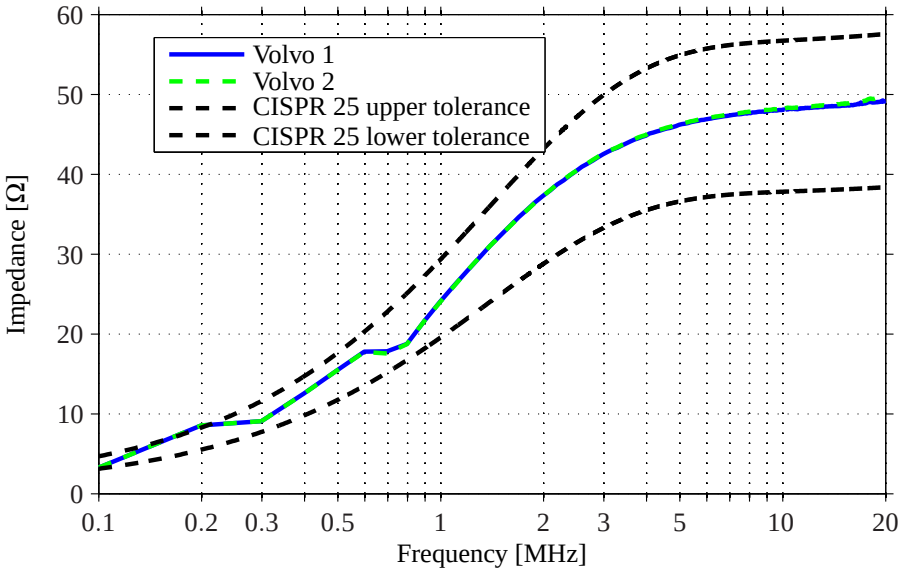
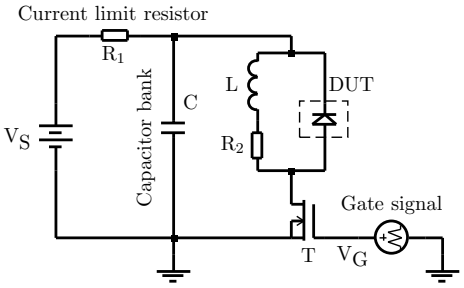



**Figure 3.4** – Results from measurements on the LISN available at Volvo Cars AB.

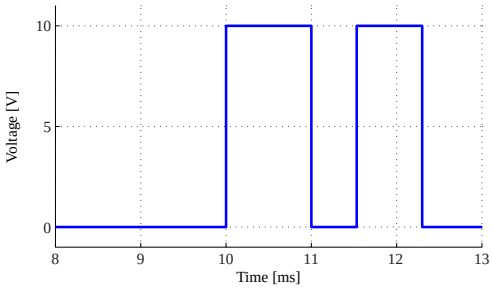
which produces a reverse recovery. The simplified schematic of the diode tester can be seen in Figure 3.5.a. The capacitor bank is large and can thus provide large currents during short times. The gate signal is generated by a timer circuit which produces well-defined gate signals such as the one seen in Figure 3.5.b.

During 10 to 11ms the transistor is on and the diode reverse biased, see Figure 3.5.a and 3.5.b. At 11ms the transistor turns off and during the subsequent 1ms the energy that was stored in the inductor now freewheels through the diode, resistor and inductor. At 11.5ms the transistor turns on again but the diode now performs a reverse recovery before switching to blocking mode.

By using this setup, diode behavior can be accurately measured and because of the capacitor bank the diode can also be tested at different biasing and current conditions.




3.5.a: Simplified diode tester schematic.




3.5.b: An example of a MOSFET gate voltage produced by the timer circuit.

**Figure 3.5** – Diode tester circuit and MOSFET gate voltage.

# 4 Diode model implementation

This section presents two diode models which were implemented in simulations. The first one, referred to as the Lauritzen model, is said to be both relatively simple to implement and accurate [21]. The second model, referred to as the Modified Charge Control (MCC) model [22], is from a designer point of view a poorer model as it lacks a procedure to extract the required parameters but it was still implemented for comparative reasons.

## 4.1 Lauritzen model

The model referred to as Lauritzen [21] in Table 2.5 was chosen for implementation as it is relatively easy to describe with mathematical equations and it require few parameters. The Lauritzen model extends the basic charge-control diode model with the effect of reverse recovery by using semiconductor charge transport equations. Since the publication the same author has published two additional articles which extends the model even further. The second article [23] extends the first one by also adding forward recovery effects. The third article [24] presents a model that differ from [21] and [23] by using a different design flow and that it models additional features such as tail current effects. As the first Lauritzen model is simpler than succeeding versions it was chosen as a starting point, when the model is correctly implemented it should be easy to add additional features.

### 4.1.1 Model description

The exact derivation of the model is not presented in this thesis. Only the final steps in deriving the model is presented, the reader is encouraged to look at [21] for more details about the model.

The reverse recovery effects are obtained by utilising additional charge storage locations within the intrinsic region. These additional charge storage locations enable the new model to emulate a diffusion of charge from the middle of the depletion region which cause the reverse recovery. The Lauritzen diode model is described by

$$i(t) = \frac{(q_E - q_M)}{T_M} \tag{4.1}$$

$$0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} - \frac{(q_E - q_M)}{T_M} \tag{4.2}$$

$$q_E = I_s \tau \left[ e^{\frac{v}{nV_T}} - 1 \right] \tag{4.3}$$

where (4.1) represents the diffusion current over a charge storage location. $T_M$ represents the approximate diffusion time across charge region $q_M$, $q_E$ has the unit of charge but does not represent charge storage. Equation (4.2) is the charge control continuity equation for $q_M$, the first term is charge storage, the second is recombination with lifetime $\tau$ and the third term represents

the diffusion current as seen in (4.1). The third equation, (4.3), is the junction equation which shows the relationship between $q_E$ and the junction voltage $v$. In (4.3) $n$ represents the emission coefficient, $n \to 2$ at high level injections and by letting $n \to 1$ the model can also function as a low-voltage p-n junction diode. $I_s$ in (4.2) is similar to the diode saturation current which can be found in the conventional idealized diode model and finally the variable $V_T$ is the thermal voltage.

If (4.1),(4.2) and (4.3) are combined the steady state dc forward-bias i-v characteristics is obtained. By letting $T_M \to 0$ the familiar expression of the original charge control model is obtained.

$$i = \frac{I_s}{(1+\frac{T_M}{\tau})}\left[e^{\frac{v}{nV_T}} - 1\right] \tag{4.4}$$

So far only the current due to the charge behavior has been described, this can be represented by the current source $I_D$ in Figure 4.1. To completely describe the diode, the junction capacitance $C_D$ and the parasitic resistance $R_S$ also needs to be accounted for.

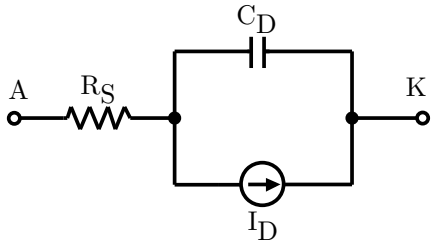



**Figure 4.1** – Diode model.

The junction capacitance $C_D$ is according to [17] described by

$$C_D = \frac{dQ_D}{DV_D} = \begin{cases} \underbrace{\tau_D \frac{dI_D}{dV_D}}_{C_d} + \underbrace{C_j(0)(1-\frac{V_D}{\phi_0})^{-m}}_{C_j} & \text{for } V_D < FC \times \phi_0 \\ \underbrace{\tau_D \frac{dI_D}{dV_D}}_{C_d} + \underbrace{\frac{C_j(0)}{F_2}(F_3 + \frac{mV_D}{\phi_0})^{-m}}_{C_j} & \text{for } V_D \geq FC \times \phi_0 \end{cases} \tag{4.5}$$

where $C_j(0)$ is the diode junction capacitance at zero bias ($V_D = 0$), $m$ is the grading coefficient, $\phi_0$ is the junction potential and $FC$ is the forward-bias junction capacitance coefficient. The value of $\phi_0$ typically ranges from 0.2V to 1V, $m$ is set to 0.33 for a linearly graded junction or 0.5 for an abrupt junction. $FC$ is a factor between 0 and 1 which determines how the junction capacitance is calculated when the junction is forward-biased, by default this factor is set to 0.5. $F_2$ and $F_3$ are SPICE2 constants which can be calculated as

$$F_2 = (1-FC)^{1+m} \tag{4.6}$$

$$F_3 = 1 - FC(1+m) \tag{4.7}$$

The junction capacitance equations thus needs the following parameters if a diode is to be properly implemented, transit time $TT$ or $\tau_D$, zero-bias junction capacitance $C_j(0)$ or $CJ0$, grading coefficient $m$, junction potential $\phi_0$ and the coefficient for forward-bias depletion capacitance formula $FC$. To fully satisfy the simplified model the series resistance also needs to be included as seen in Figure 4.1. The resistance is accounted for by including the voltage drop over it, how this is done can be seen in Appendix F.

Mentioned parameters can most often be found in the SPICE model supplied by the diode manufacturer and thus little or no work is required in the parameter extraction.

### 4.1.2 Model implementation

Thus are all parts for an implementation available. The diode model was implemented in Matlab Simulink by using an S-function. An S-function is a function block where dynamic nonlinear equations can be solved through the use of an iterative process were a state-space system is solved in each step. The exact implementation of the model can be found in Appendix F were the Matlab code and the Simulink design is presented.

As mentioned in section 2.4.6 the simulation accuracy is more dependent on the accuracy of the input parameters then on the model itself and when parameters are missing from the conventional model there is a need for a reliable extraction procedure.

### 4.1.3 Parameter extraction

The parameters associated with the Lauritzen model and the extraction procedure is described in [21]. In order to extract the required parameters for the model, measurement data must be available. As mentioned in [21], the parameters $\tau$ and $T_M$ can be determined from a diode turn-off current waveform, see Figure 4.2. This measurement waveform was acquired using the diode tester described in section 3. The equations describing the theoretical waveform are

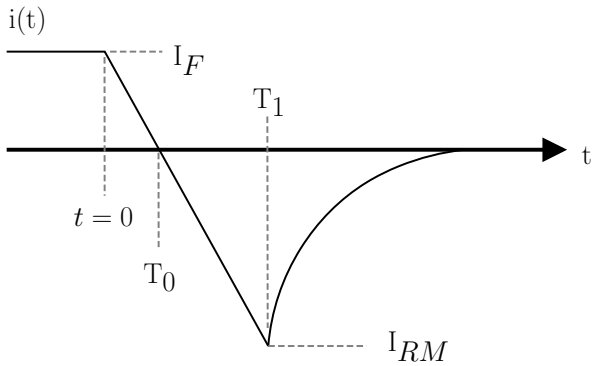



**Figure 4.2** – Diode turn-off current waveform used in the parameter extraction.

$$i(t) = -I_{RM} e^{-\frac{t-T_1}{\tau_{rr}}} \text{ for } t \geq T_1 \tag{4.8}$$

$$I_{RM} = a(\tau - \tau_{rr})\left[1 - e^{-\frac{T_1}{\tau}}\right] \tag{4.9}$$

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau} + \frac{1}{T_M} \tag{4.10}$$

To obtain $\tau$ and $T_M$, the parameter extraction is a curve fitting procedure combined with some equation solving. At first, the parameter $\tau_{rr}$ has to be determined, this is done by using an arbitrary curve-fitting technique in order to make (4.8) correspond to the waveform of Figure 4.2. The remaining parameters in (4.8) are easily obtained by studying the turn-off waveform, see Figure 4.2. Next can the parameter $\tau$ be extracted by solving (4.9) and finally $T_M$ can be found by using (4.10). Figure 4.3 shows one example were curves are fitted to a reverse recovery measurement obtained from the diode tester setup.

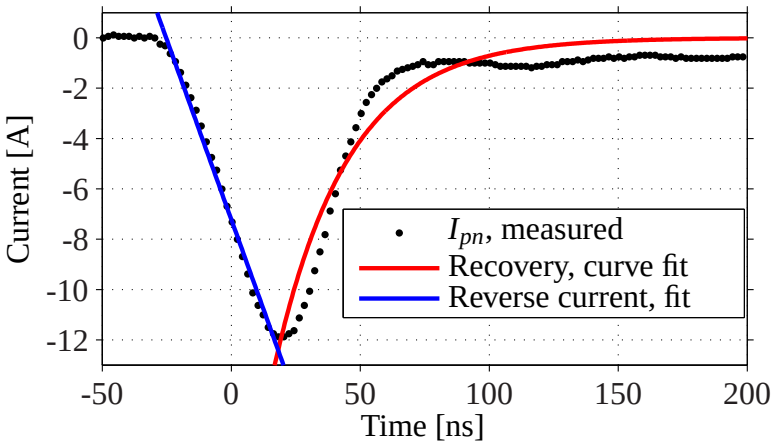



**Figure 4.3** – Reverse recovery waveform processed with the curve fitting toolbox in Matlab in order to extract required parameters.

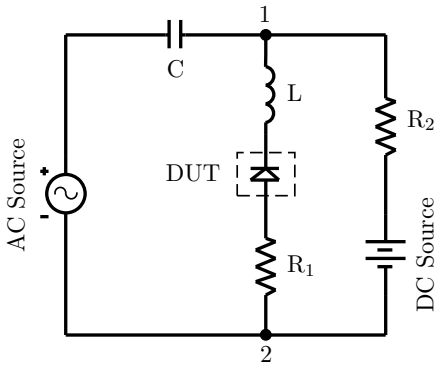
### Extraction of parameters used in the junction capacitance equations

From the model description section above it is clear that the parameter that needs to be extracted is the zero-bias junction capacitance $C_j(0)$. The other parameters mentioned in (4.5) describes the physics of the p-n-junction at large and must be made available by the manufacturer or be approximated. According to [25] the junction capacitance of an abrupt junction can be expressed by (4.11) where the physical parameters describing the junction is collected in the constant K.

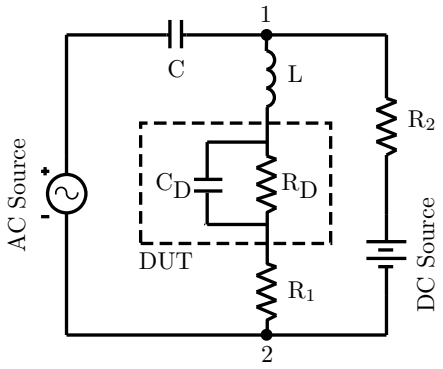
$$\frac{1}{C_j^2} = \frac{2}{qN_B K_S \varepsilon_0 A^2}(V_{bi} - V_A) = K(V_{bi} - V_A) \tag{4.11}$$

Thus the junction capacitance $C_j$ only varies with the reverse voltage $V_A$ applied over the junction as the built-in potential ($V_{bi}$) is constant. It is clear that a plot of $1/C_j^2$ versus $V_A$ should produce a straight line. Note that (4.11) only produces the junction capacitance for a reverse bias, $V_A < 0$. If the junction capacitance can be obtained for different reverse bias values the zero-bias capacitance can easily be acquired by a curve fitting procedure showing the capaci-

tance at zero-bias. One way of finding the junction capacitance at different bias points is by utilising a resonance circuit and varying the input frequency, see Figure 4.4.a.




4.4.a: Measurement setup.




4.4.b: The diode is replaced by a capacitance in parallel with a resistor for analysis purpose.

**Figure 4.4** – Measurement setup (a) and the same circuit but with the DUT expressed as a capacitance in parallel with a resistor (b).

For analyses purpose the diode can be represented by the capacitance $C_D$ in parallel with $R_D$, see Figure 4.4.b. Looking at the impedance between node 1 and 2 and treating the DUT as a pure capacitance for simplicity, it can be expressed as

$$Z_{12} = R_1 + \frac{1}{j\omega C_D} + j\omega L = R + j\left(\omega L - \frac{1}{\omega C_D}\right) \tag{4.12}$$

Resonance occurs when $Z_{12}$ is minimized, which occurs for the following capacitance $C_D$.

$$C_D = \frac{1}{\omega^2 L} = \frac{1}{(2\pi f)^2 L} \tag{4.13}$$

As the inductance in the circuit is constant the only way to minimize the impedance is by tuning to the right frequency $f$ which then provides the junction capacitance at that bias point according to (4.13).

Having presented the background of the circuit the measurements were made in the following way. After biasing the DUT, the voltage over resistor $R_1$ was measured while tuning the AC-frequency. When the maximum voltage over $R_1$ is found, which implies that the $Z_{12}$ impedance is at a minimum, the frequency value of the AC-source is noted. Repeating this process for several bias points provides the characteristics of the junction capacitance. Figure 4.5 shows one result from this procedure applied on the 20ETS12 diode from IRF. Note that the amplitude of the AC-source has to be kept low enough such that the DUT does not become forward biased, or even biased beyond breakdown. In order to be at a somewhat correct frequency range initially the junction capacitance can be estimated to be somewhere in the 100pF range, this provides a starting point for the frequency of the AC-source.

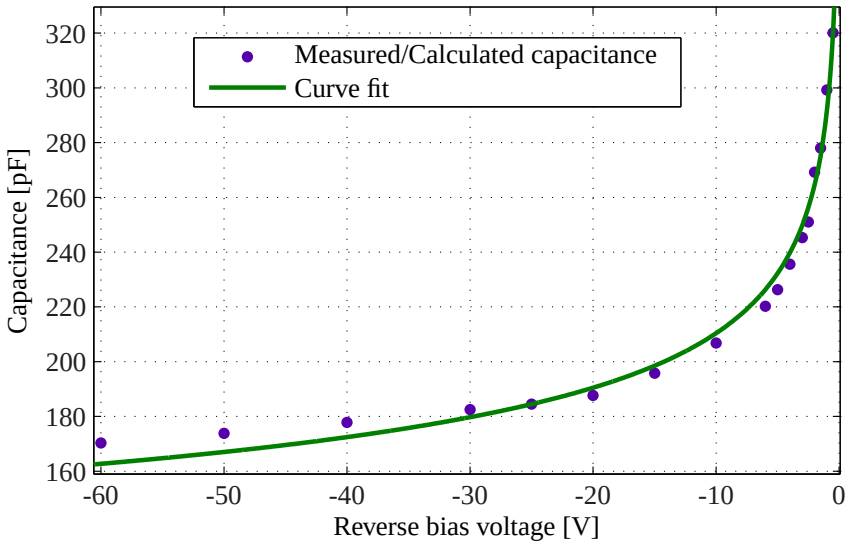



**Figure 4.5** – Junction capacitance measured by utilizing a resonant circuit.

## 4.2 MCC diode model

The MCC model is referred to as Tseng II in Table 2.5. As already mentioned, this model lacks a procedure of parameter extraction which makes it less usable then the Lauritzen model. The model uses a conventional SPICE diode model and extends it to also include reverse and forward recovery. The model, which is presented in [22], is implemented in SPICE using Analog Behavioral Model (ABM) blocks. The ABM blocks may contain expressions that consist of circuit voltages, currents, time and other simulation parameters. The SPICE implementation is presented in Figure 4.6 and in this case the model extends the IRF diode 20ETS12 to exhibit forward and reverse recovery during simulations.

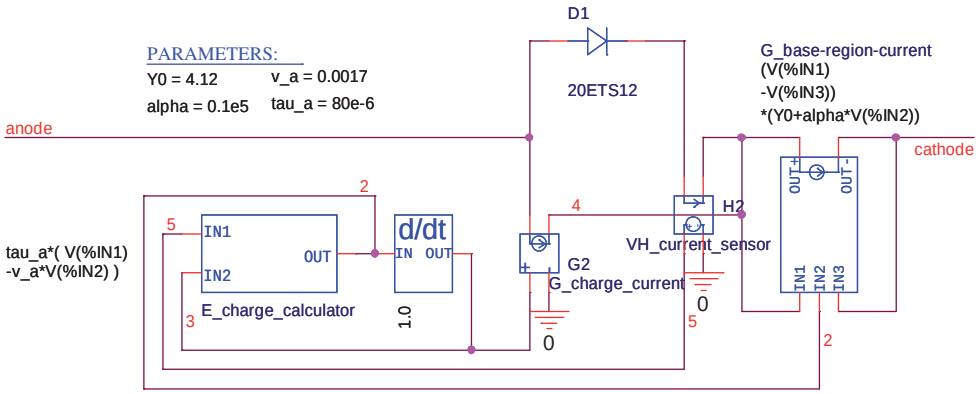



**Figure 4.6** – Implementation of MCC in SPICE using ABM blocks.

As can be seen in Figure 4.6 the model depends on four adjustable parameters: $v_a$, $\alpha$, $Y_0$ and $\tau_a$. These parameters must be adjusted so that the model corresponds to a measured waveform and these adjustments can prove to be quite tedious. The relation between model behavior and the parameters can be seen in Figure 4.7.

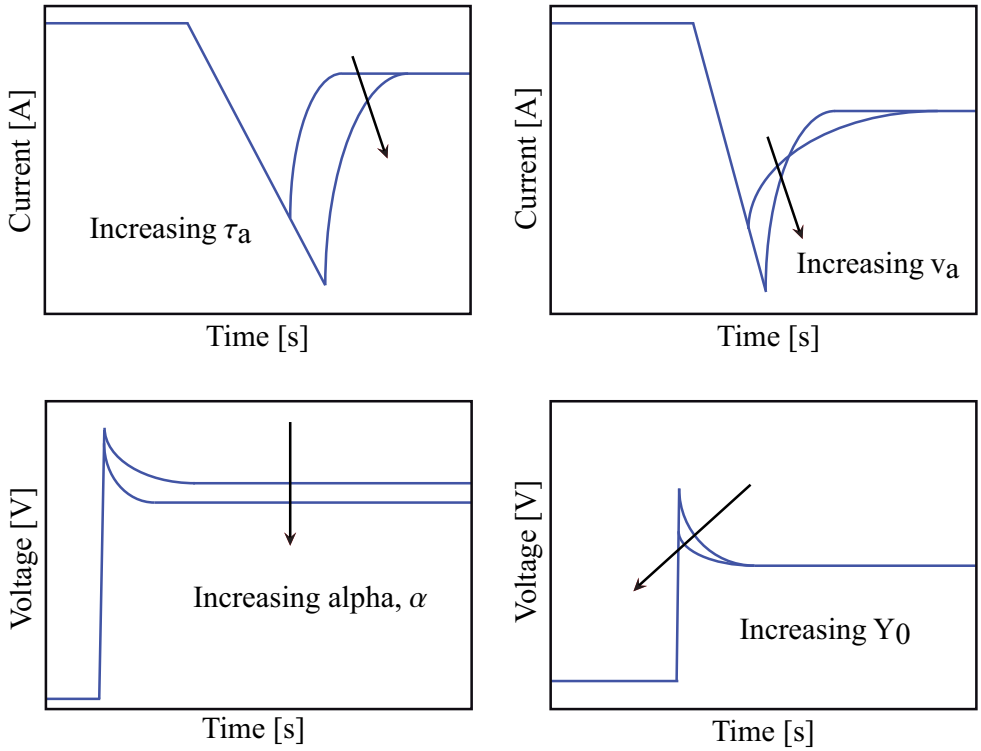



**Figure 4.7** – How to adjust the MCC model in order to achieve a certain behavior.

In [22] the author adjusts the model so that the reverse recovery coincide with the recovery from a measurement made at the rated operating current of that particular diode. Having done this the author finds that behavior of the model falls within a 10% error tolerance for other operating points. The derivation of the model will not be presented, instead the reader is referred to [22].

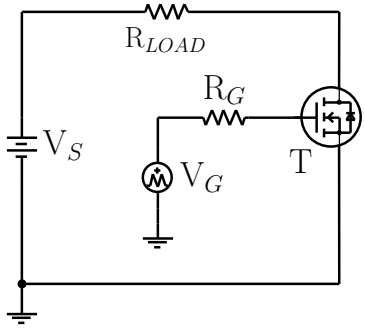
# 5 Construction and modeling of basic MOSFET circuit

In order to see how well a simple circuit can be modeled, a very basic switching circuit was designed, see Figure 5.1.a. The circuit is very basic and consist mainly of a load resistor in series with a MOSFET transistor. Given that the MOSFET has a good model available in SPICE the behavior of the model representing the complete circuit should correspond well to the actual circuit.

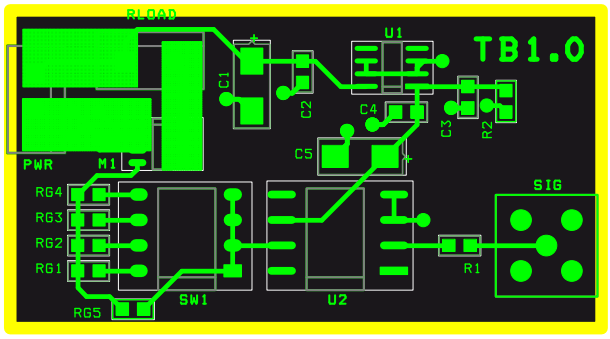
## 5.1 Construction of circuit on PCB

The switching circuit, from here on referred to as Testboard 1 (TB1), was realised on a PCB that was designed using Orcad Layout. The PCB layout is shown in Figure 5.1.b. While creating this layout, the design guidelines which can be found in [4] was kept in mind. This can be seen by observing e.g. the separation between high and low current path regions and minimizing the length of high current strips while making the strip width relatively wide.

When comparing Figure 5.1.a and 5.1.b, it can be seen that there are some additional components needed for the gate drive. The drive circuit (ICL7667) is complemented with an LM7815 voltage regulator and a resistor switch which makes it possible to alternate the MOSFET gate resistance. A side from these components there are also some capacitors and resistors which are recommended to be present alongside the IC components. A complete schematic over the switching circuit can be found in Appendix C.




5.1.a: Basic switching circuit with a MOSFET in series with a load resistor.




5.1.b: PCB layout of the test circuit created in OrCAD Layout.

**Figure 5.1** – Basic switching circuit and the PCB layout where the circuit was realised.

## 5.2 Modeling of circuit in SPICE

Figure 5.1.a was used as a starting point in modeling TB1. The gate driver part of the circuit was neglected during modeling as this part was assumed not to add to EMI emissions in a measurable way. Thus was the gate driver replaced by an ideal pulsed voltage source in SPICE. Figure 5.2

shows a straightforward model of TB1 which normally would be used for simulations of this kind of circuit.

As capacitors from Kemet were used a software[5] from Kemet was used to generate detailed capacitor models. These capacitor models can be seen in Figure 5.3.

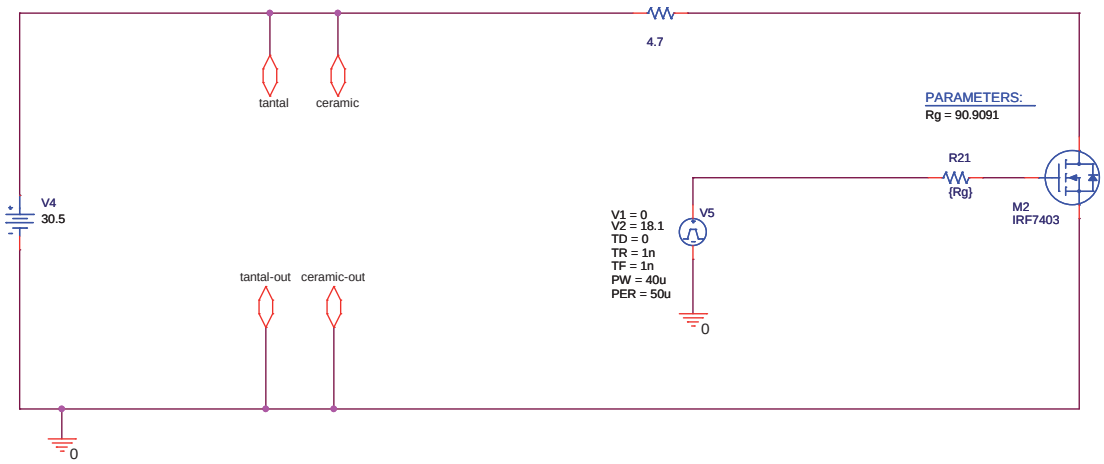



**Figure 5.2** – Simple model of TB1.

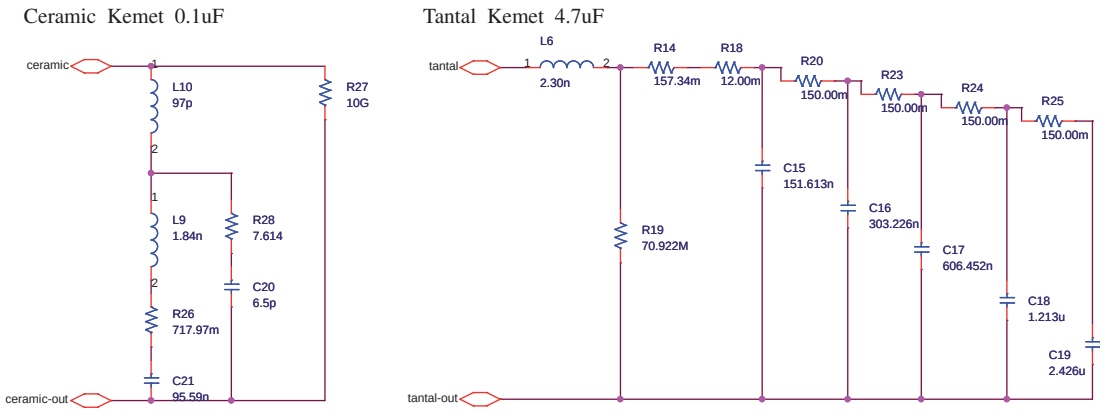



**Figure 5.3** – Detailed capacitor model from Kemet.

The next step was to model TB1 as accurately as possible. This requires that, besides from the elements being present in the model shown in Figure 5.2, impedances originating from copper strips, stray impedance from component leads and parasitic impedance from various components are added. The impedance of the PCB or copper strips are easily realised by using the formulas mentioned in section 2.4 together with the PCB layout software. Besides modeling of the PCB stray impedances, additional stray or parasitic component impedances needs to be accounted for. Common parameters mentioned in data sheets are Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) and can thus be translated into lumped passive elements. Figure 5.4 shows the detailed model of TB1 with stray and parasitic elements accounted for.

The circuit of Figure 5.4 also contains some capacitors in the pico-size-range originating from capacitive coupling, the formulas leading to these values has not been presented earlier in this

[5]KEMET Spice Software - Version 3.5.3, see www.kemet.com .

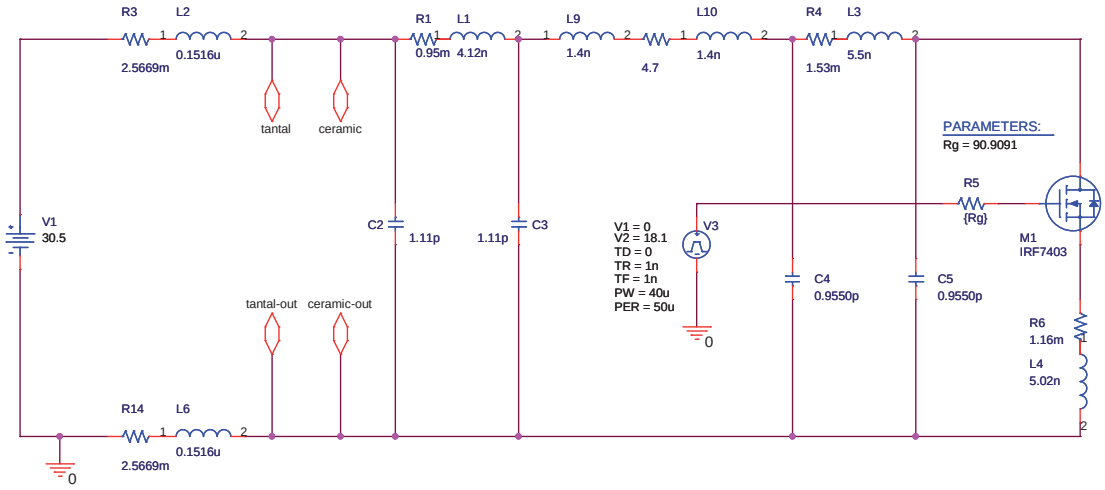



**Figure 5.4** – A more detailed model of TB1 including parasitic and stray components.

report but can be found in [26]. The reason for skipping these formulas are that capacitors of this size does not effect the behavior of the circuit in any substantial way.

## 5.3 Comparison between measurement and simulations

With both models and a physical circuit available comparisons were made to see how well the switching waveforms correspond to each other. A Tektronix oscilloscope was used to measure the MOSFET drain-source voltage, $V_{ds}$, and the drain current, $I_d$, during both turn-on and turn-off of the MOSFET.

In Figure 5.5; are the measured waveforms presented together with the corresponding waveforms from simulations from the simple model during turn-on. The measured and simulated waveforms correspond fairly well but there are some clear deviations. E.g. is the slope of the waveforms from the simulations much steeper then those measured.

Figure 5.6 shows the turn-on transition again but here the measured waveforms are compared to waveforms from a simulation using the detailed model which accounts for parasitic and stray elements. The correspondence is now better with almost equal $dv/dt$ and $di/dt$.

During turn-off the measured $V_{ds}$ voltage shows a clear overshoot between $0.15\mu$s and $0.2\mu$s and this behavior is not replicated by simulations with the simple model. Except the overshoot is the correspondance fairly good, see Figure 5.7. However, with the detailed model is the over voltage present due to the parasitic and stray elements, Figure 5.8.

It is clear that using a simulation model where various stray and parasitic impedances are accounted for, simulation results correspond a lot better to actual measurements. A simple circuit gives good agreement, both in amplitude and in frequency.

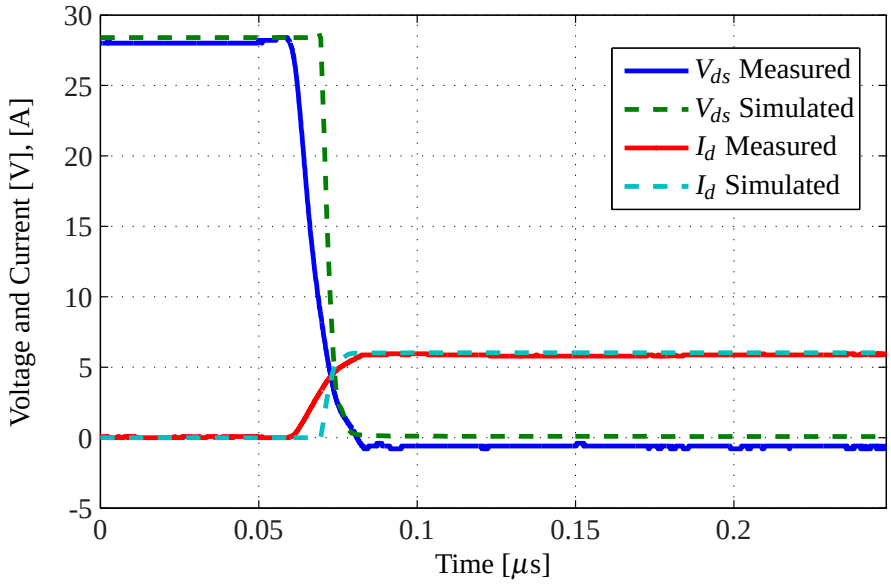



**Figure 5.5** – The turn-on transition from both measurement and simulation. The simulation result is gathered from a model were all parasitic and stray components are omitted.

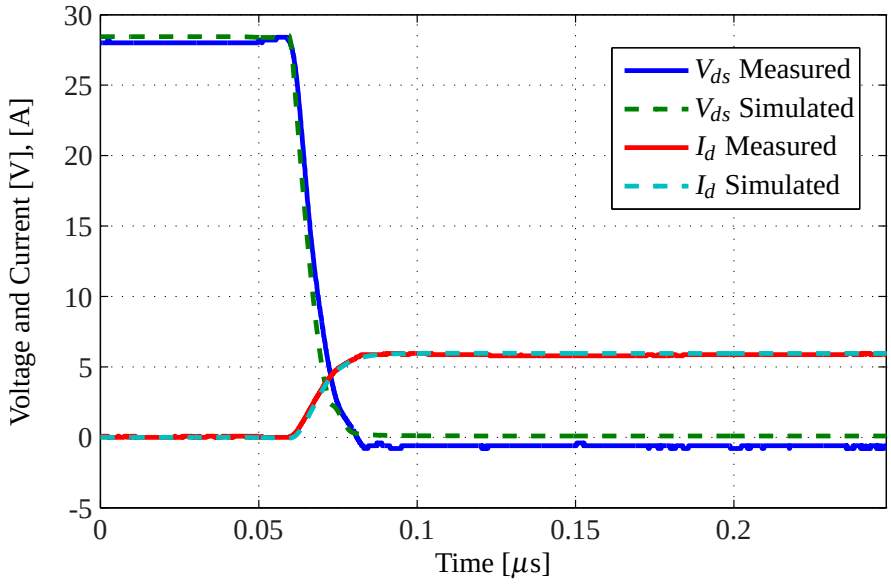



**Figure 5.6** – The turn-on transition from both measurement and simulation. The simulation result is gathered from a model were parasitic and stray components are accounted for.

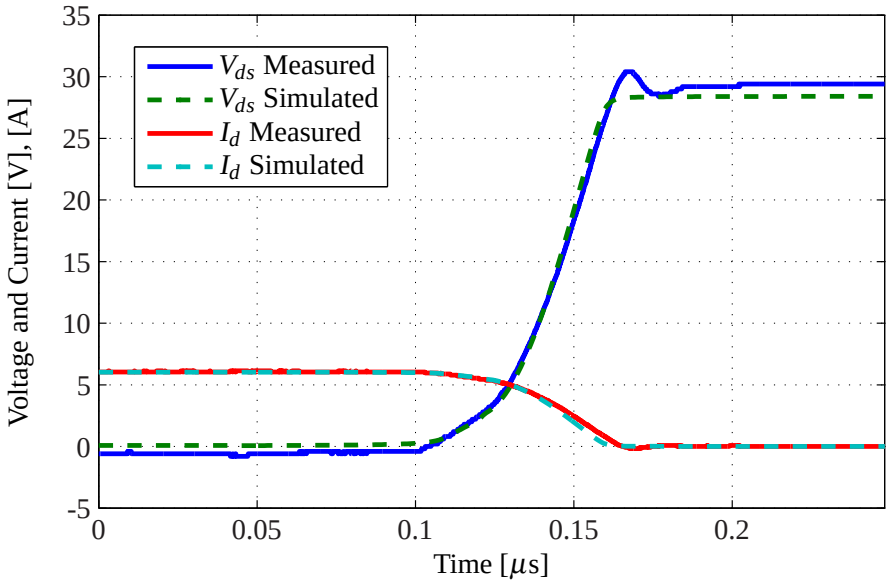



**Figure 5.7** – The turn-off transition from both measurement and simulation. The simulation result is gathered from a model were all parasitic and stray components are omitted.

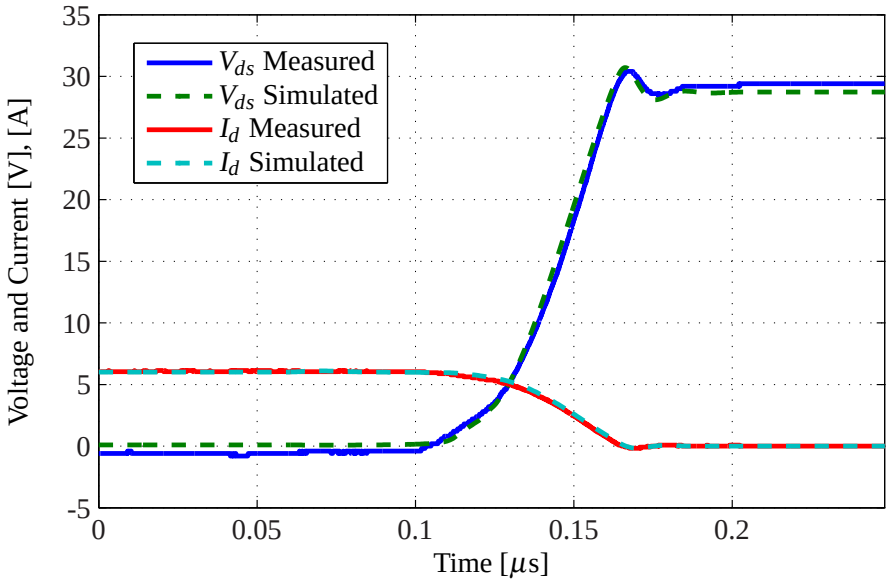



**Figure 5.8** – The turn-off transition from both measurement and simulation. The simulation result is gathered from a model were parasitic and stray components are accounted for.

# 6 Buck converter

A buck converter, also known as a step-down, is a DC-DC converter, whose basic design can be seen in figure 6.1. It is a switched-mode power supply that in its most basic form uses two switches (a transistor and a diode) together with an inductor and a capacitor. The switching of the transistor either connects the inductor to the input voltage (on-state) to store energy in the inductor, or allows the inductor to discharge into the load (off-state). By controlling the on- and off-state times the input voltage is lowered to the desired level. The two basic modes of operation of the converter are continuous conduction mode, CCM, and discontinuous conduction mode, DCM. The Buck converter operates in CCM if the current through the inductor never falls to zero during the commutation cycle and in DCM if it does.

The advantages of using a buck converter over a simple voltage divider are higher efficiency (easily up to 95% for integrated circuits) and control (regulated output voltage).

## 6.1 Design of buck converter

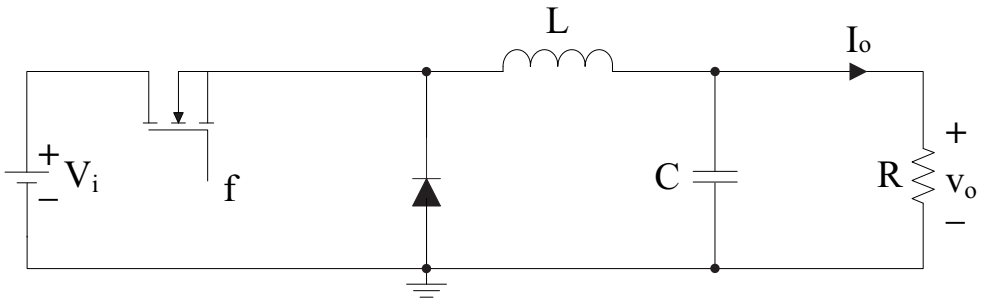



**Figure 6.1** – A basic buck converter.

The basic design parameters set for the buck converter were as follows and can be found annotated in figure 6.1:

- $V_O = 12\text{V}$
- $V_I = 60\text{V}$
- $I_O = 10\text{A}$
- $f = 200\text{kHz}$
- $\Delta V_O = 50\text{mV}$
- $\Delta I_L = 1\text{A}$

$\Delta V_O$ is the desired maximum output voltage ripple, $\Delta I_L$ is the desired current ripple in the inductor and $f$ is the desired switching frequency. If CCM is assumed the inductance and capacitance

values can be calculated as [27]:

$$d = \frac{V_O}{V_I} = 0.2 \tag{6.1}$$

$$t_{on} = 1/f \cdot d = 1\mu\text{s} \tag{6.2}$$

$$t_{off} = 1/f \cdot (1-d) = 4\mu\text{s} \tag{6.3}$$

$$L \approx (V_I - V_O) \cdot t_{on}/\Delta I_L \approx 48\mu\text{H} \tag{6.4}$$

The minimum capacitance necessary to maintain the $\Delta V_O$ ripple voltage at less than the 50mV design objective was calculated according to:

$$C = \frac{\Delta I_L}{8 f \Delta V_O} = 125\mu\text{F} \tag{6.5}$$

The output capacitor can be seen as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important. So, the two components of interest are the capacitance and the Equivalent Series Resistance (ESR). The maximum ESR is calculated according to the relation between the desired output voltage ripple and the inductor ripple current:

$$ESR_{MAX} = \frac{\Delta V_O}{\Delta I_L} = 50\text{m}\Omega \tag{6.6}$$

The choice of a tantalum capacitor from Kemet is made because of good available models and because of its use in the MOSFET test circuit. Two 330$\mu$F T510 Kemet electrolytes are selected with an ESR of 21m$\Omega$ at 200kHz and a maximum ripple current of 1.1A.

The inductor was constructed on a T106 seized iron powder core (material number 26) using 24 turns of 1.6mm copper wire. Measurement of the constructed inductor showed an inductance of 57.1$\mu$H and a DC resistance of 53m$\Omega$.

### 6.1.1 Voltage control

Since the output voltage of the converter is influenced by change in load condition, voltage feedback control is required to maintain a constant output voltage. Figure 6.2 shows a circuit diagram of the buck converter with the chosen voltage control loop layout. To calculate the proper values of the circuit elements $R_1$, $R_2$, $C_1$ and $C_2$ of the error amplifier a conventional procedure described in [28] was used and is summarized below.

- Plot the bode diagram of the converter's transfer function,

$$G_p(s) = \frac{V_i/V_p}{LC}\left[\frac{1+sr_CC}{s^2\left(1+\frac{r_C}{R}\right)+s\left(\frac{1}{RC}+\frac{r_C}{L}+\frac{(r_C+R)r_L}{RL}\right)+\frac{r_L+R}{RLC}}\right]$$

- Select a desired bandwidth $\omega_{CO}(=\omega_S/10\sim\omega_S/5)$, where $\omega_S$ is the switching frequency. Find $R_1$ and $R_2$ such that $G_p(j\omega_{CO}) = R_1/R_2$.

- Choose a proper phase margin $(PM)$ usually greater than or equal to 45°. Solve the following equations:

$$\varphi_{CO} = PM - \angle G_p(j\omega_{CO}) - 180^\circ,\ \ K^2 - tan(\varphi_{CO}+90^\circ)K - 1 = 0$$

- Find the zero frequency and pole frequency using the relations:

$$\omega_Z = \frac{\omega_{CO}}{K},\ \ \omega_P = K\omega_{CO}$$

- Finally $C_1$ and $C_2$ are obtained as follows.

$$C_1 = \frac{1}{R_2\omega_Z},\ \ C_2 = \frac{1}{R_2\omega_P}$$

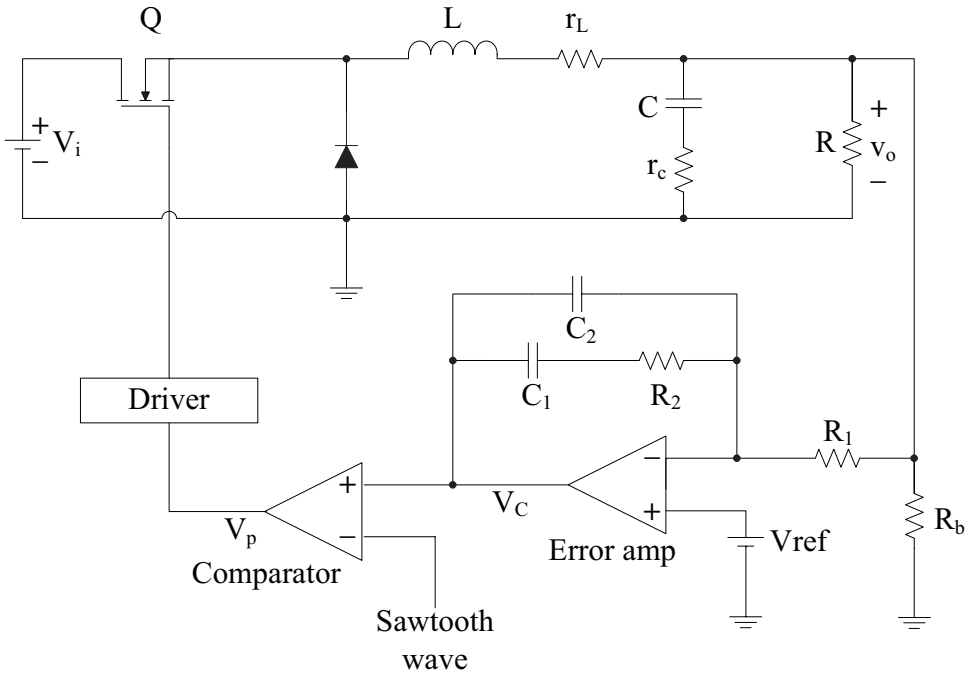



**Figure 6.2** – Buck converter with voltage control loop.

Using this control design strategy with $\omega_{CO}$ at a fifth of the switching frequency, a phase margin of 90°, all inductance, capacitance and series resistance values results into the following parameters: $R_1 = 181\Omega$, $R_2 = 5.38\text{k}\Omega$, $C_1 = 210\text{pF}$ and $C_2 = 2.6\text{nF}$. See chapter 6.4 for the validation of the control strategy.

### 6.1.2 Input filter

As SMPS are normally noisy a filtering circuit must be inserted between the supply output and the converter input. This filtering circuit is very important regarding EMI behaviour but not a lot of effort has been put on this part, the goal was not to design a high performance Buck-converter but rather a converter which could be easily modeled. The guidelines regarding the design of an input LC-filter presented in [12] was followed but the resulting filter has not been thoroughly examined and thus the exact performance can not be reported here. However, the work flow in designing the filter and the choice of components is presented below.

In [12] the author breaks down the filter design in 9 steps and the first 4 of these will now be presented and adapted to the current converter design. Step 5 to 9, which has been skipped, deals with filter instability and damping which ensures high efficiency. The reader is advised to look at [12] for further information regarding filter design and SMPS design in general.

1. The filter specification is used as a starting-point and in this case the input ripple limit was set to 15mA. This ripple limit gives the required attenuation as the peak fundamental of the converter is known or can be obtained.

   $$A_{filter} < \frac{15\text{m}}{4} < 3.7\text{m}$$

   which implies an attenuation better than 48dB. In this case the peak fundamental of 4A was obtained from simulations in SPICE.

2. The cut-off frequency of the LC filter is obtained by the following inequality:

   $$f_0 < \sqrt{0.0037} \times F_{sw} < 12.247\text{kHz}$$

   it was selected to $f_0$ =12kHz.

3. An inductance of 40$\mu$H was chosen and the required capacitance is then determined from the following formula:

   $$C = \frac{1}{4\pi^2 f_0^2 L} = 4.4\mu\text{F}$$

   the value of the capacitor was chosen to be 5$\mu$F because of availability of components. The capacitor must be able to withstand a fairly high ripple current and this current can be obtained from the following expression:

   $$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

   in this case $I_{ac} = 4.65$A, $I_{rms}$ and $I_{dc}$ was obtained from SPICE simulations. A capacitor from the Kemet T495 series was chosen, the exact current ripple durability was not specified but the Kemet T495 series is specified to withstand “high current ripple”. The

chosen capacitor had the value $10\mu$F and connecting two of these in series produces a total capacitance of $5\mu$F.

The parasitic components of the inductor and capacitor are needed. The capacitor is specified to have an ESR of 300m$\Omega$, this is a very large value but no other capacitor was available at the time. As two are connected in series the total resistance is thus 600m$\Omega$. Regarding the inductor series resistance, it was estimated to 4.4m$\Omega$ making it almost negligible in relation to the capacitor ESR.

4. The final attenuation can now be calculated according to the following expression:

$$\left|\frac{I_{in}}{I_{out}}\right| = \sqrt{\frac{R_C^2 + \frac{1}{(\omega C)^2}}{(R_L + R_C)^2 + \frac{1}{(\omega C)^2} - \frac{2L}{C} + (\omega L)^2}} = 12.4\text{m}$$

the attenuation no longer fulfils the current ripple requirement and this is mainly because of the very large ESR in the capacitors. The attenuation now corresponds to around 38dB which is 10dB lower then the initial aim.

Steps 5 through 9 deals with filter instability and validation through simulation. In case of filter instability a damping resistor in series with a capacitor is added in parallel to the converter input. As no filter evaluation was performed, the size of the damping resistor can not be motivated but was nonetheless set to 10$\Omega$ as this was recommended as an initial value. The size of the series capacitor is recommended to be four times the filter capacitor and was thus chosen to $33\mu$F as this was the closest to $20\mu$F of what was available but still voltage durable enough.

### 6.1.3 Additional components and circuits

The PWM control circuit chosen for the buck is a TL494 from Texas Instruments, (TI). This circuit has been on the market for a long time (more then 20 years) but provides the basic functions needed; two operational amplifiers for controls and a soft start etc. The TL494 needs external components and lacks some functions that are addressed in the following paragraphs.

#### Current limiter

To avoid damage to the buck during non ideal operation (e.g. short circuiting of the output terminals) a current limiting addition is necessary. The MOSFET is the most likely component to fail during a high load situation. Consequently is the desired current to limit the current through the inductor ($I_L$). To measure this current, shunt resistors are added in series with the inductor and an operational amplifier specially designed for current shunt measurements (INA169 from TI) manages the actual measuring. Since the TL494 have two integrated operational amplifiers, one can be used for the voltage control while the other is connected in a direct comparative way to the current monitoring circuit, see Figures D.1 through D.3.

#### Soft start

During start-up of the converter, the controller will demand a near to 100% duty cycle since the output voltage is far below the desired. The connected load together with the uncharged output capacitance will draw an undesirably large current if this is not limited. The soft start function limits the maximum duty cycle during the initialization by overriding the comparator used for the voltage control. The soft start implementation can be seen in Figures D.1-D.3. For more information on the dimensioning of the soft start see [29].

#### Low side alternatives

High- and low side is used to denote the two switching elements; in the buck the high side element switches the source voltage and the low side discharges the inductor into the load. Since versatility in the design is sought, a low side MOSFET alternative to the diode was integrated in the design. A low side MOSFET is switched in opposite of the high side but with an added delay to avoid short circuiting of the source voltage. The delay is accomplished with an RC-filter together with a diode, the circuit is denoted “Dead time” in Figure D.2. The dimensioning of this filter was made in an empirical way through measurements.

#### MOSFET Drive Circuits

To drive the MOSFET(s) reliably and efficiently a gate driver is necessary. Since the source terminal of the high side MOSFET is not grounded, a gate drive operating in a bootstrap configuration is needed. IR2110 from International Rectifier meets the requirements. A bootstrap circuit boosts the voltage of a capacitor above the supply voltage that is then discharged to drive the MOSFET [30]. A bootstrap circuit can only operate as long as the converter is switching. If the duty cycle approaches 100% for a prolonged time the charging of the bootstrap capacitor will cease causing the gate driver to fail. A charge pump is added to handle this eventuality. Charge pumps operate in a similar way as a bootstrap but employs its own switching element [31]; in this design a CMOS powered oscillating crystal at 2MHz. The MOSFET drive circuits can be seen in Figure D.3.

## 6.2 Construction of circuit on PCB

The PCB layout of the buck converter, referred to as Testboard 2 (TB2), was realised using Orcad Layout and printed on a two sided 35$\mu$m copper board. The PCB layout guidelines used for TB1 were used for TB2 [4]. The complete PCB layouts can be seen in Appendix E with the schematics in Appendix D. Some implemented PCB layout details of note are;

- Short high current paths, with an added option to bypass the input filter.

- A large unbroken ground plane.
- Separated control section, the lower part of the PCB is dedicated to small signal components.
- A grounded copper pour fills out all empty spaces in the controller part of the board for better shielding.

## 6.3 Modeling of circuit

The simulation models built of TB2 were numerous since different simulation environments and diode models were tested. The two final simulation environments used were, Orcad Pspice and Matlab Simulink with SimElectronics. In Orcad Pspice the basic SPICE diode model and the MCC diode was used. The Lauritzen model was implemented in Matlab Simulink.

Simulating the complete converter with controls, drive circuits, current sensor etc. is complex, resource demanding and not always necessary. Simplifications were made based on previous results from TB1 and depending on the model environment. The controls and MOSFET drive circuits of the board were never modelled since dynamic performance so far is of lower concern.

### 6.3.1 Pspice modeling

As with TB1 the PCB parasitic elements of TB2 were added to the model using the methods described in section 2.4. Supplier capacitor and MOSFET models were used together with either the SPICE diode or the MCC diode models. Figure F.1 and F.2 in Appendix F show the models for the complete measurement setup with the two different diode models.

### 6.3.2 Simulink modeling

The Lauritzen diode model was written in an S-function that can be seen in Appendix F. Connecting the implemented diode model to a complete circuit proved difficult but was attempted using the SimElectronics environment. SimElectronics is a new addition to the Simulink environment that allows for more complex electrical circuit simulations and also an option to import SPICE netlist files.

As can be seen in Figure F.3 Appendix F a heavily simplified circuit, lacking input filter and using no parasitic components or advanced capacitor models, had to be settled for. Trying to add more complexity generated convergence errors and initialisation problems.

## 6.4 Comparison between measurement and simulations

The diode used during the measurements that are to be presented was the 20ETS12. The reason for this being that it proved to be an easy diode to parameterize. The switching diodes that were tested in the diode test circuit showed a very small reverse recovery. The 20ETS12 diode is however a rectifying diode and not designed to be used as a switching diode. The efficiency off TB2 was low, $\approx 60\%$, but not unexpected since the diode has a lot of reverse recovery.

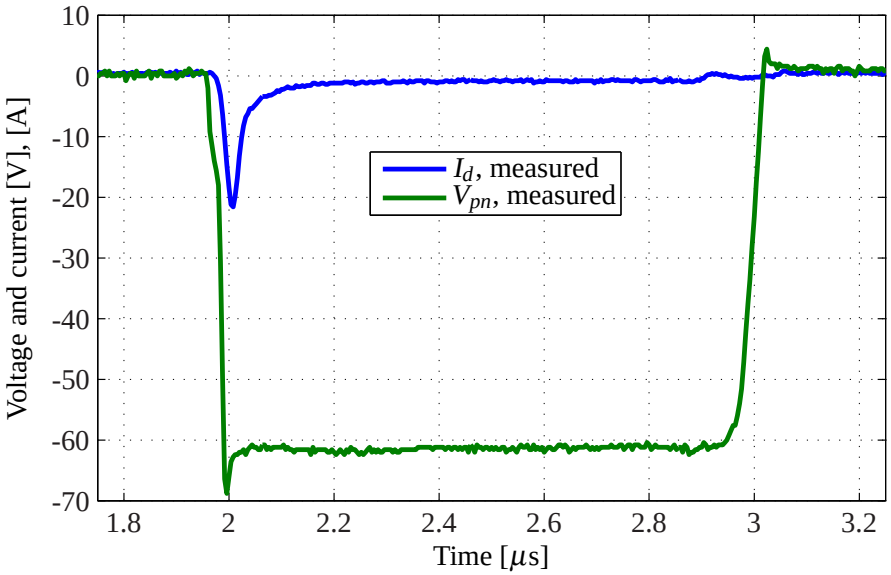



**Figure 6.3** – Measured MOSFET drain current and diode voltage.

The time measurement seen in Figure 6.3, were made with a Tektronix oscilloscope and a Rogowski coil during a 45% load ($\approx$ 54W output power). The reverse recovery is clearly visible at the start of the on-state when the diode has to stop conducting.

### 6.4.1 SPICE diode evaluation

A comparison between a simulation using the manufacturer's SPICE model, and the time measurement can be seen in Figure 6.4. As previously discussed the SPICE diode model does not include reverse recovery so lack thereof is not surprising. What is surprising is the behaviour of the diode voltage just before the on-state. The voltage raise can only stem from the diode model itself since modeling with a different SPICE diode removed the phenomenon. The results from the simulation using the SPICE diode model and the measurements agree rather poorly.

### 6.4.2 Lauritzen diode evaluation

The Lauritzen diode model proved to be hard to simulate in a complete electrical circuit as previously mentioned. The reverse recovery in the simulation transpires at a quicker rate then

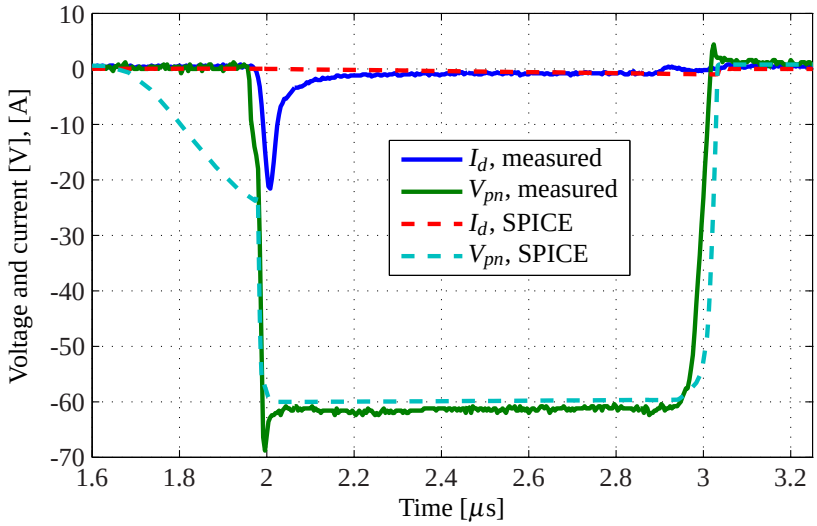



**Figure 6.4** – Measured and simulated drain current and diode voltage. The diode used during simulation is the conventional diode model supplied by the manufacturer.

it ought to when compared to the measurements, see Figure 6.5. This can be explained by the absence of stray inductances in the simulation and other left out elements. The form of the reverse recovery is however correct except for the time scale. A close up of the simulation reverse recovery can be seen in Figure 6.6.

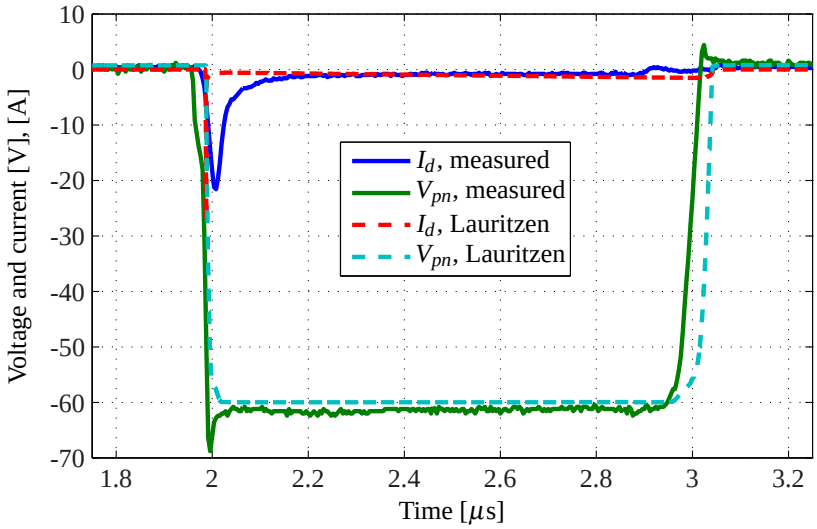



**Figure 6.5** – Measured and simulated drain current and diode voltage. The diode used during simulation is the implementation of the Lauritzen diode model.

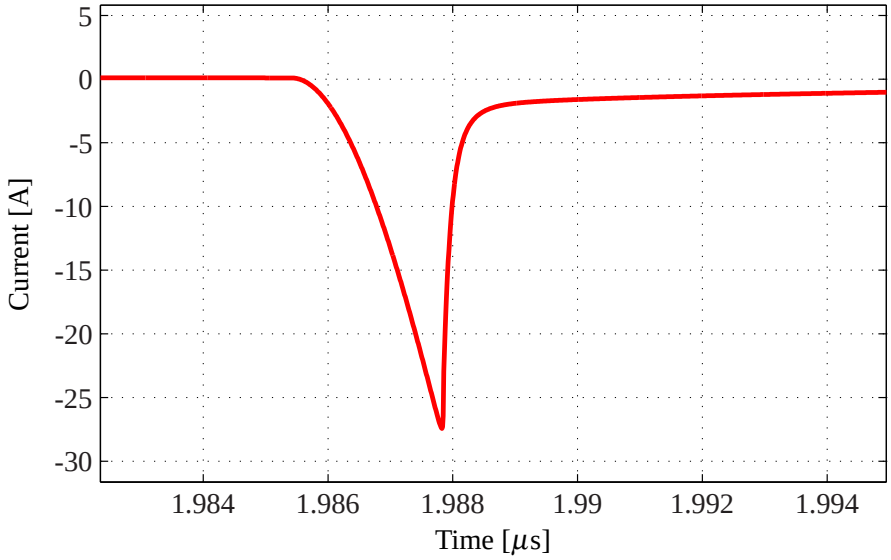



**Figure 6.6** – Simulation showing the MOSFET drain current. The model produces the correct reverse recovery shape although during a very short time.

### 6.4.3 MCC diode evaluation

The adjustments of the MCC diode parameters proved difficult, the model tended to cause large oscillations when seeking to increase the reverse recovery current peak. The parameters used in the simulation presented in Figure 6.7 were set to match the peak reverse current. Note the significant oscillations on the diode voltage.

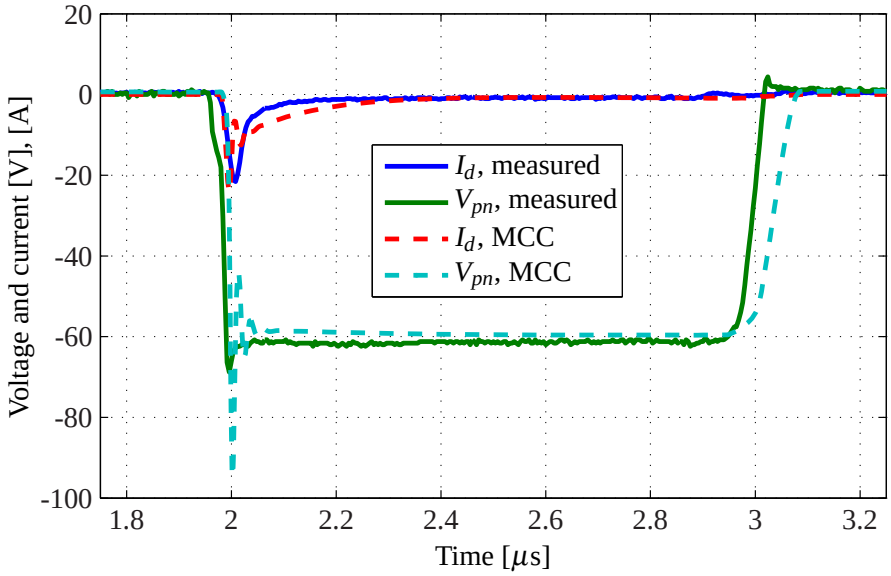



**Figure 6.7** – Measured and simulated drain current and diode voltage. The diode used during simulation is the implementation of the MCC diode model.

### 6.4.4 Conducted EMI measurements

Conducted EMI was measured at Volvo Cars and following the CISPR 25 guidelines. The test object and measuring devices were positioned as seen in Figure 2.1. The frequency range of interest was set to the Medium Wave (MW) band. Figure 6.8 shows the frequency content of TB2 using the 20ETS12 diode and a 45% resistive load. As previously discussed, the efficiency of TB2 is very low and as expected is the EMI performance also rather poor; it barely passes the CISPR 25 Class 1 limit which is the most tolerant class.

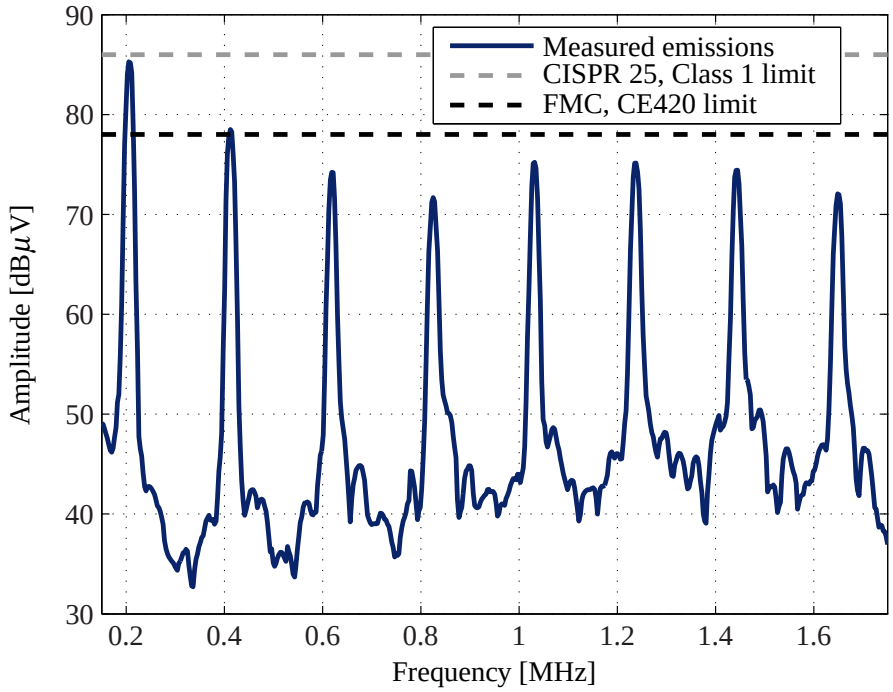



**Figure 6.8** – Measured frequency content in the MW band, conducted emissions.

The comparative results presented are from simulations of TB2 with external components such as wires, loads and LISN's with both a regular SPICE diode and the MCC implementation, schematics can be found in Appendix F Figure F.1 and F.2. The Lauritzen diode model was also intended to be compared with the measurements, but this was not possible due to simulation difficulties caused by the system size.

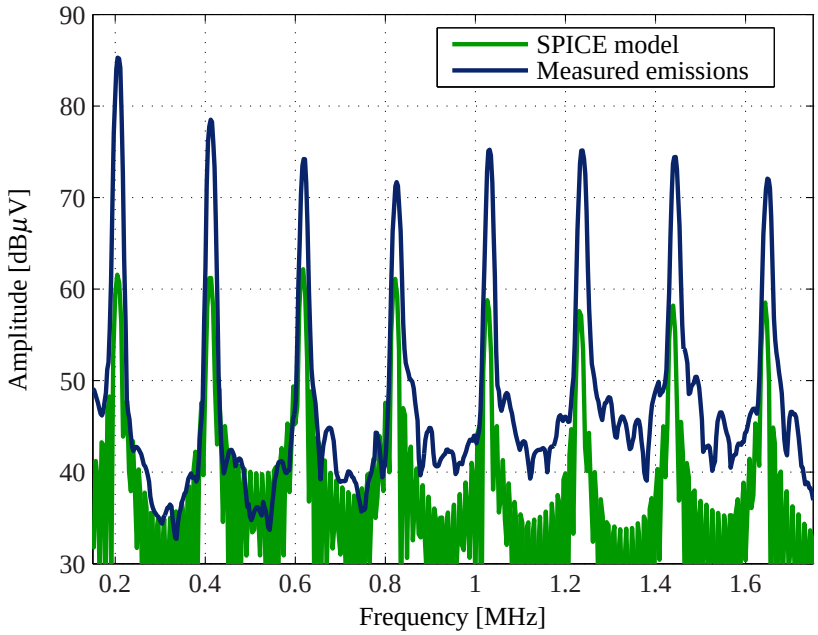



**Figure 6.9** – Frequency content from the simulated Buck converter using the conventional SPICE diode model from the supplier together with the measured frequency content.

The frequency content when simulating with the SPICE diode model was significantly lower then the measured content, see Figure 6.9. This is attributed to the lack of reverse recovery in this model. The simulation result using the MCC model shows a better likeness to the measurement, see Figure 6.10. The MCC model has certain limits in its feasability, but represents a step in the direction that a working Lauritzen model would have shown.

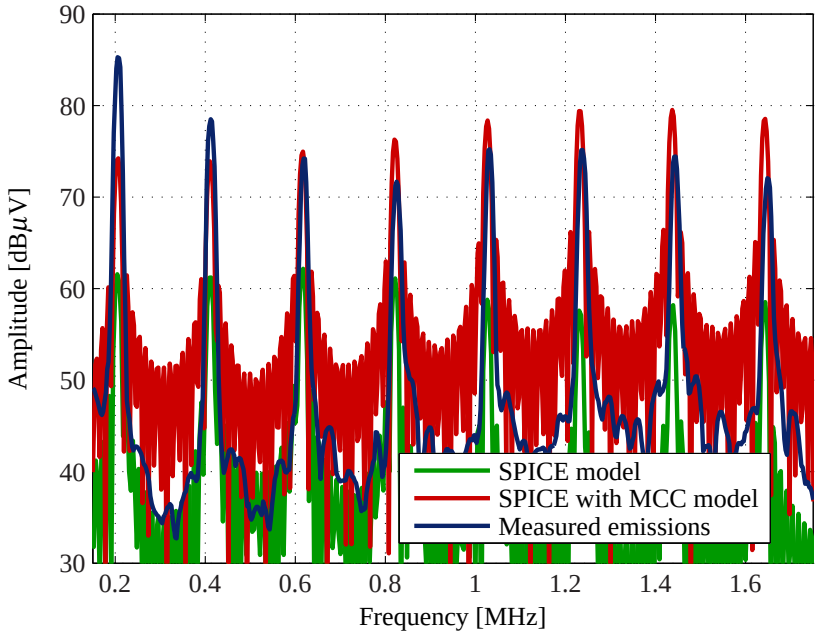



**Figure 6.10** – A comparison between measured frequency content and frequency content from simulations using both the conventional diode model and the MCC model.

### 6.4.5 Controller validation

A verification of the voltage control was made by generating load steps at the output of TB2. This was accomplished by using an external MOSFET to switch in extra load and by changing the external MOSFET gate resistance the transition time of the load step could be adjusted. Several steps were tested and a typical step response of the output voltage can be seen in Figure 6.11. The control keeps the output voltage overshoot within 0.5V which can be defined as a satisfactorily low variation. Since no application for the TB2 was set, the acceptable output voltage variation and settling time were unknown. Such design parameters vary from application to application.

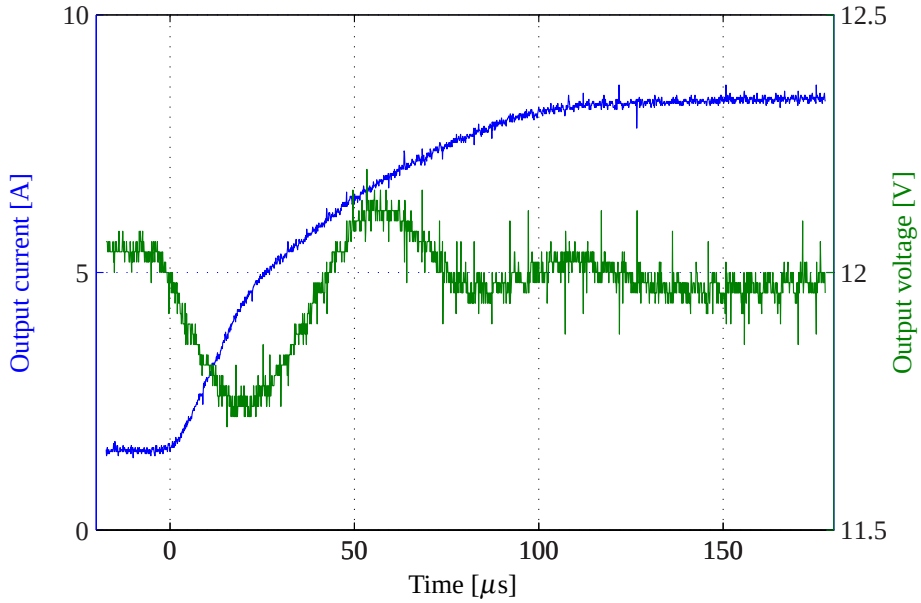



**Figure 6.11** – Load step response, 15% to 85% in 100$\mu$s.

# 7 Conclusions

The simulation model of a device or circuit can easily be refined by inserting lumped elements representing various stray and parasitic impedances. This simple measure makes the result from simulations correspond a lot better to actual measurements and this could perhaps be an effective way to pinpoint specific EMI components originating from the device.

Parasitic and stray elements improve the model accuracy only to a certain point. To improve the accuracy even further, all parts of the device need good simulation models. In the case of the diode, the effects of forward and reverse recovery adds a great deal to the EMI behavior. Thus is the diode model very important and the conventional SPICE model available today is not enough. If an accurate model is available to the designer, he or she can utilise the simulation software to get better results concerning emitted EMI.

Both development time and cost can be saved if an accurate model is available. This is, or at least should be, a powerful driving force in the research and development for new diode models with improved EMI performance.

# 8 Future work

Implementation of the Lauritzen diode model proved difficult and requires additional work. The model is still a good candidate for future work as compared with other models that either require more input parameters or were parameter extraction procedures are absent.

A side from the diode there are other components which needs a model refinement. Modeling of MOSFETs and IGBTs needs attention. Depending on the desired depth of detail all semiconductor components could be modeled better producing more accurate simulation results.

Even if all parts of the device can be perfectly modeled, it is still not taken into account how different parts influence each other. If some types of components are placed close together how will this affect the total performance? Certain parts, e.g. large magnetic components or long wires and conductors, might couple to each other making them perform poorly. This can be a future topic related to EMI.

This thesis work has only considered the DUT to be a source of EMI. It can be of interest to investigate the susceptibility to EMI. This topic might coincide with the topic mentioned above where the placement and positioning of components are at focus. What parts are more susceptible than others and how should the result from this work effect future design guidelines?

In section 5 the increased correspondence between measurements and simulations was presented but this was done using only one reference circuit. It could be interesting to investigate how the correspondence changes with different MOSFET individuals. If for example the measurement could be made on many individuals, lets say 50 MOSFET individuals, a spread related to the behavior of the MOSFET could be determined and the MOSFET model should perhaps be compared to this spread of results rather than just one reference measurement.

In this thesis each copper strip was manually translated to a lumped component including resistance, capacitance and inductance. The procedure could perhaps be automatized, this future tool would save a lot of time for the designer and it would increase the PCB model accuracy substantially.

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Figures without reference in the caption are designed by the authors of this report. Some of the figures were designed with inspiration gathered from the text references, these figures are listed below.

Figure 2.2 through 2.7 - Inspired by [5]
Figure 4.1 - Inspired by [17]
Figure 4.2 - Inspired by [21]
Figure A.1 - Inspired by [4]

# A Peak, average and quasi-peak measurements

Emission measurements can be done in various ways, the most common detectors used are peak, average and quasi-peak detector. The characteristics for each detector can be found in CISPR 16, [32]. As the interference emissions seldom appear at a continuous and fixed level the measurement of the emissions depend on the choice of detector. The indicated level received using different detectors are shown in Figure A.1.

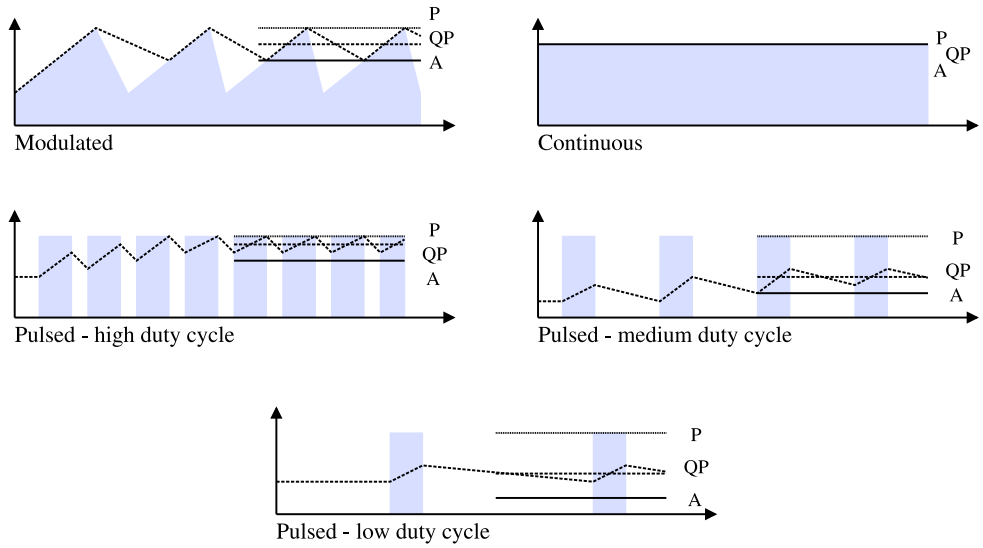


**Figure A.1** – Peak(P), quasi-peak(QP) and average(A) detectors indicating different levels of the same signal.

## Peak

A peak detector responds very rapidly, near-instantaneously, to the peak value of the signal and discharges fairly rapidly. If the receiver resides on a single frequency the peak detector output will follow the envelope of the signal and because of this, the peak detector is sometimes referred to as an envelope detector. The peak detector is often used to fulfill military specifications because of their stringent standards but CISPR emissions standards do not require it at all for frequencies below 1GHz. As the peak detector has a very fast response it is suitable for diagnostics or quick tests.

## Average

The average detector measures, as its name impies, the average value of the signal. In the case where the signal is continuous, the average detector will measure a value equal to that measured by a peak detector. In the case where the signal is not continuous, the measured value will be lower than that measured by a peak detector.

## Quasi-peak

Historically, the intention of CISPR based tests have been to protect the voice and broadcast users of the radio spectrum and thus was this detector developed to correlate the EMI receiver readings with the broadcast disturbances heard by the human ear. Interference with low pulse repetition frequencies is subjectively less annoying on radio reception than interference at high pulse repetition frequencies and thus was the quasi-peak detector developed with reference to the human ear. The quasi-peak detector works in a similar way as the peak detector with the difference that it uses weighted charge and discharge times and therefore a pulse-type emission will be treated more moderately by a quasi-peak detector than by a peak detector. To get an accurate result, the measurement must dwell on each frequency for a longer time than the peak detector. Long charge and discharge times makes QP-measurements time consuming. Because of the history of broadcasted radio transmissions, CISPR emphasized on the use of the quasi-peak detectors. In the future, the QP detector might not play such a significant role as digital transmissions are sensitive in different ways.

# B MOSFET models

The contents of this appendix has been borrowed from a SPICE exercise booklet used in a course at Chalmers University of Technology with permission from the author. As it originally was published in Swedish it has been translated into English with the authors consent.


Appendix A to booklet “SPICE-exercises” in the course EDA351Circuit Electronics, version 080113

Appendix A: MOSFET model types
In the table below a large number of available Level types for different SPICE simulators are listed

| Level | MOSFET description | Level | MOSFET description |
|---|---|---|---|
| 1 | Schichman-Hodges model | 27 | SOSFET |
| 2 | MOS2 Grove-Frohman model | 28 | BSIM derivative; Avant! proprietary model |
| 3 | MOS3 empirical model | 29[c] | not used |
| 4 | Grove-Frohman: LEVEL 2 model derived from SPICE 2E.3 | 30[c] | VTI |
| 5 | AMI-ASPEC depletion and enhancement (Taylor-Huang) | 31[c] | Motorola |
| 6 | Lattin-Jenkins-Grove (ASPEC style parasitics) | 32[c] | AMD |
| 7 | Lattin-Jenkins-Grove (SPICE style parasitics) | 33[c] | National Semiconductor |
| 8 | advanced LEVEL 2 model | 34[a] | (EPFL) not used |
| 9[b] | AMD | 35[b] | Siemens |
| 10[b] | AMD | 36[c] | Sharp |
| 11 | Fluke-Mosaid model | 37[c] | TI |
| 12[b] | CASMOS model (GTE style) | 38 | IDS: Cypress depletion model |
| 13 | BSIM model | 39 | BSIM2 |
| 14[b] | Siemens LEVEL=4 | 41 | TI Analog |
| 15 | user-defined model based on LEVEL 3 | 46[c] | SGS-Thomson MOS LEVEL 3 |
| 16 | not used | 47 | BSIM3 Version 2.0 |
| 17 | Cypress model | 49 | BSIM3 Version 3 (Enhanced) |
| 18[b] | Sierra 1 | 50 | Philips MOS9 |
| 19[c] | Dallas Semiconductor model | 53 | BSIM3 Version 3 (Berkeley) |
| 20[b] | GE-CRD FRANZ | 54 | UC Berkeley BSIM4 Model |
| 21[b] | STC-ITT | 55 | EPFL-EKV Model Ver 2.6, R 11 |
| 22[b] | CASMOS (GEC style) | 57 | UC Berkeley BSIM3-SOI MOSFET Model Ver 2.0.1 |
| 23 | Siliconix | 58 | University of Florida SOI Model Ver 4.5 (Beta-98.4) |
| 24[b] | GE-Intersil advanced | 59 | UC Berkeley BSIM3-501 FD Model |
| 25[b] | CASMOS (Rutherford) | 61 | RPI a-Si TFT Model |
| 26[b] | Sierra 2 | 62 | RPI Poli-Si TFT Model |

[a] = not officially released
[b] = equations are proprietary - documentation not provided
[c] = requires a license and equations are proprietary - documentation not provided

# C Basic switching circuit schematic

Layout schematic of TB1, components in the schematic can be related to the PCB layout in Figure 5.1.b in section 5.

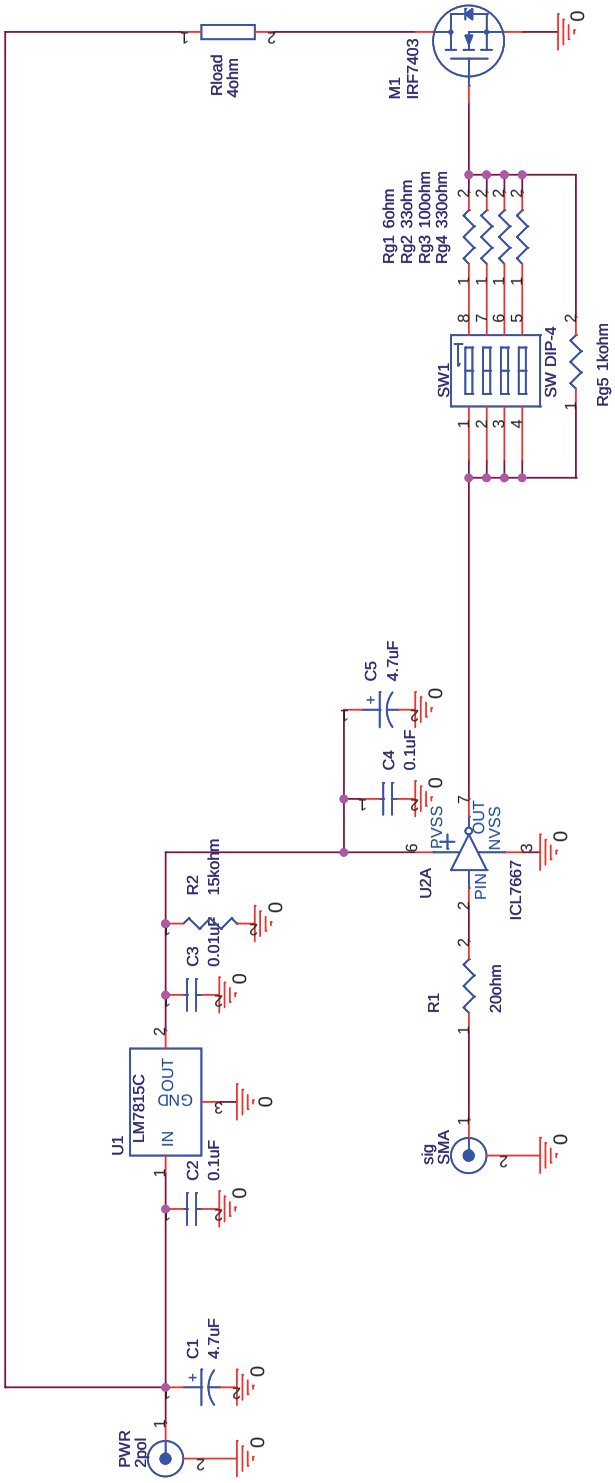


**Figure C.1** – Schematic used to design the PCB.

# D Buck layout

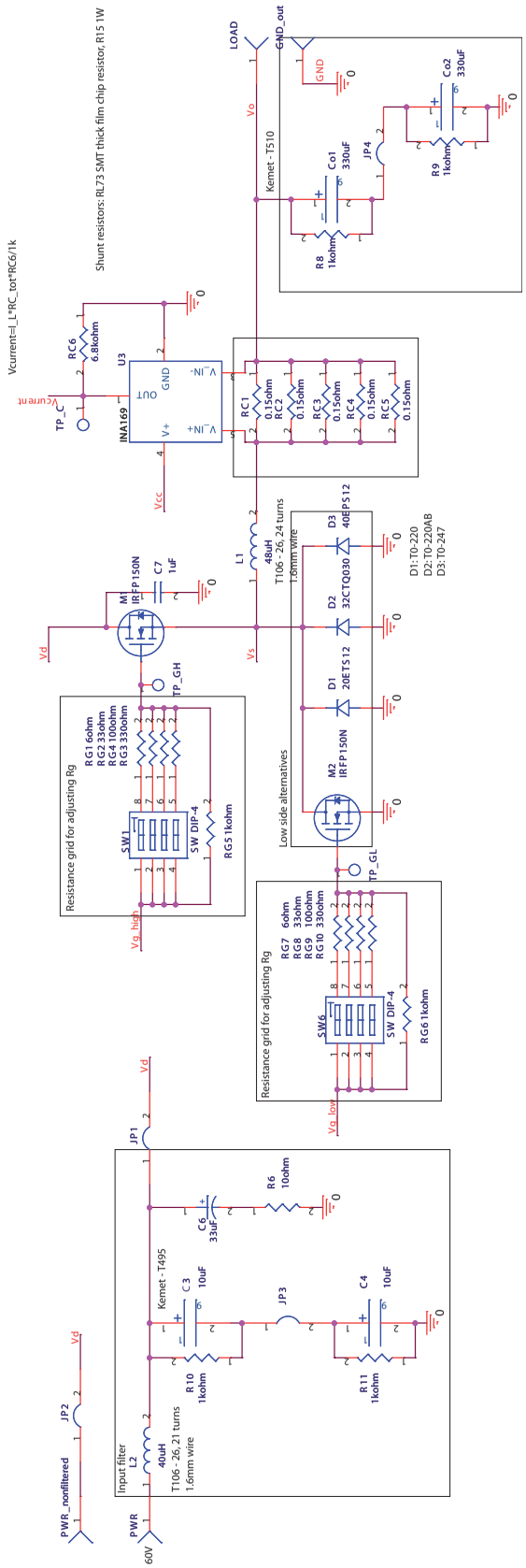


**Figure D.1** – Buck converter SPICE schematic designed in order to utilise the PCB layout software OrCad Layout. Sub-schematic 1 of 3.

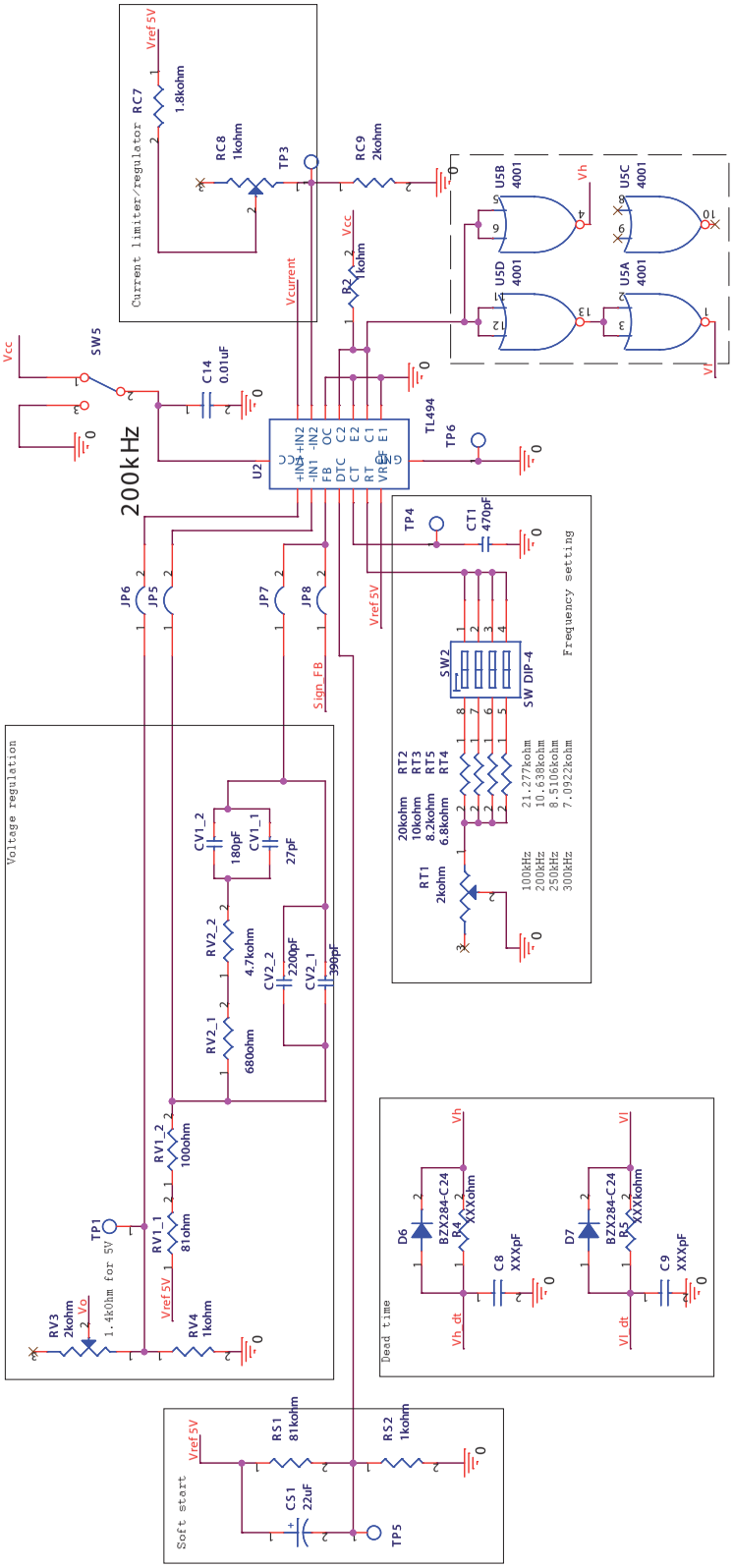


**Figure D.2** – Buck converter SPICE schematic designed in order to utilise the PCB layout software OrCad Layout. Sub-schematic 2 of 3.

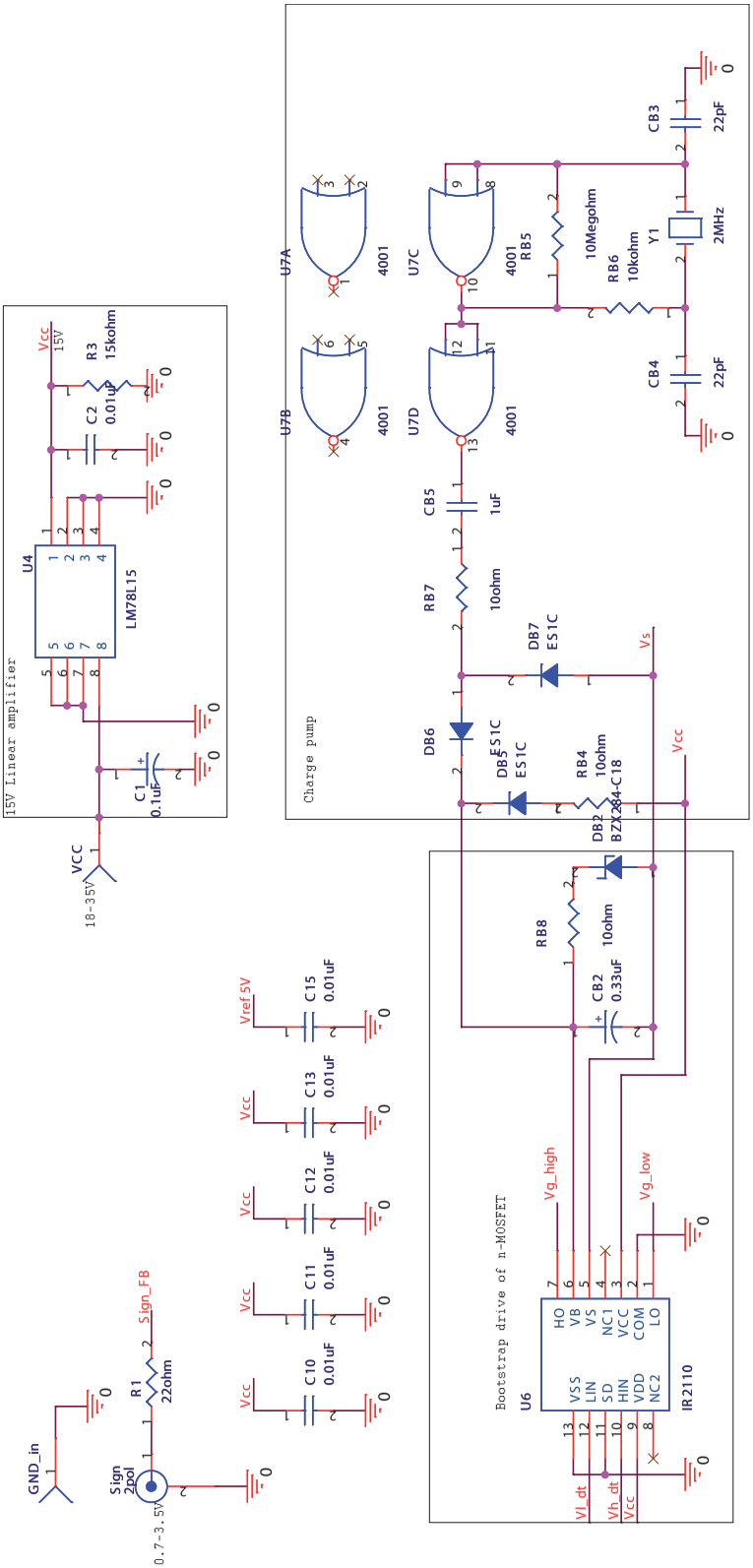


**Figure D.3** – Buck converter SPICE schematic designed in order to utilise the PCB layout software OrCad Layout. Sub-schematic 3 of 3.

# E Buck converter PCB designs



**Figure E.1** – Drill mask for the PCB of the buck converter.

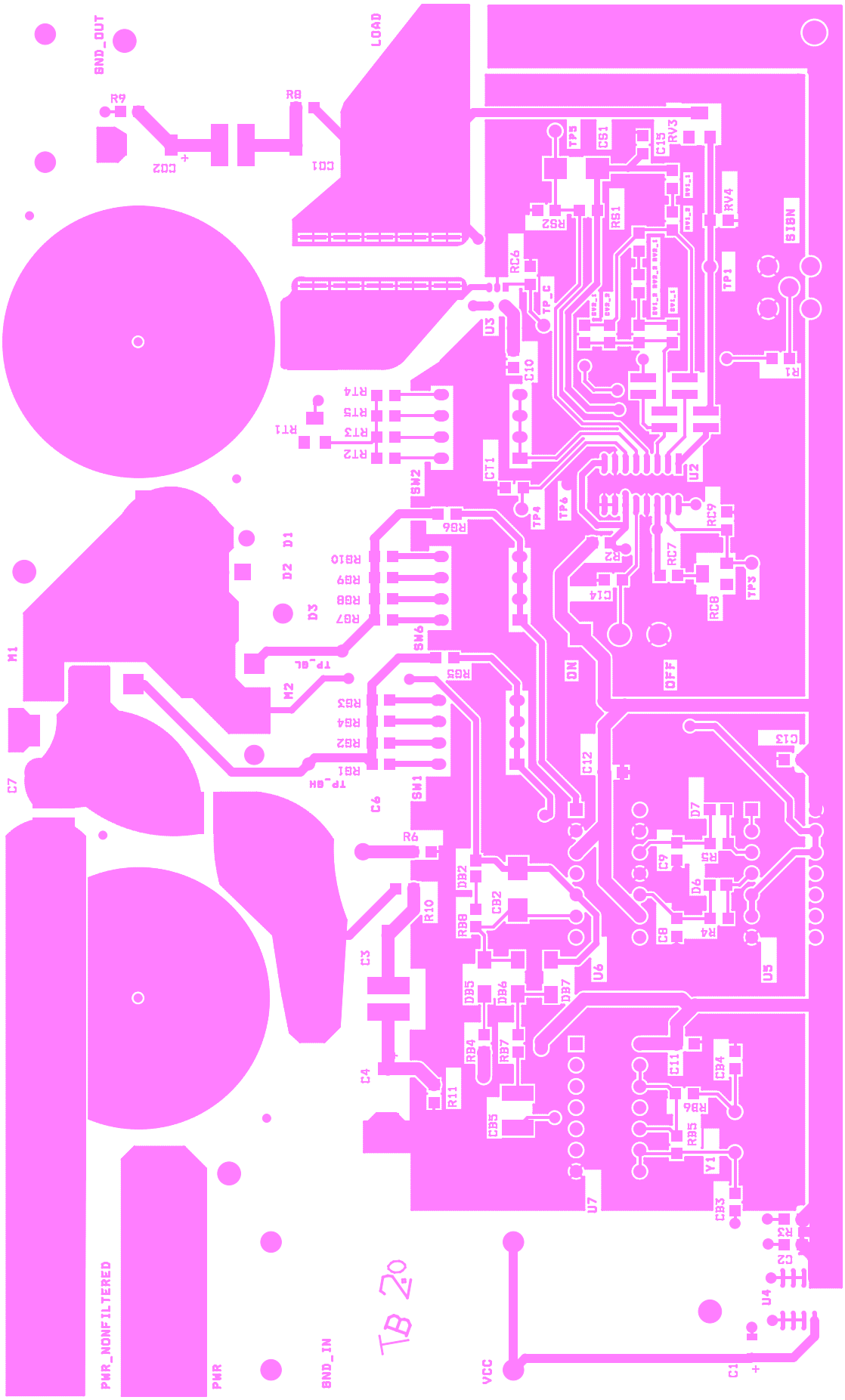


**Figure E.2** – Top PCB layer of the buck converter.

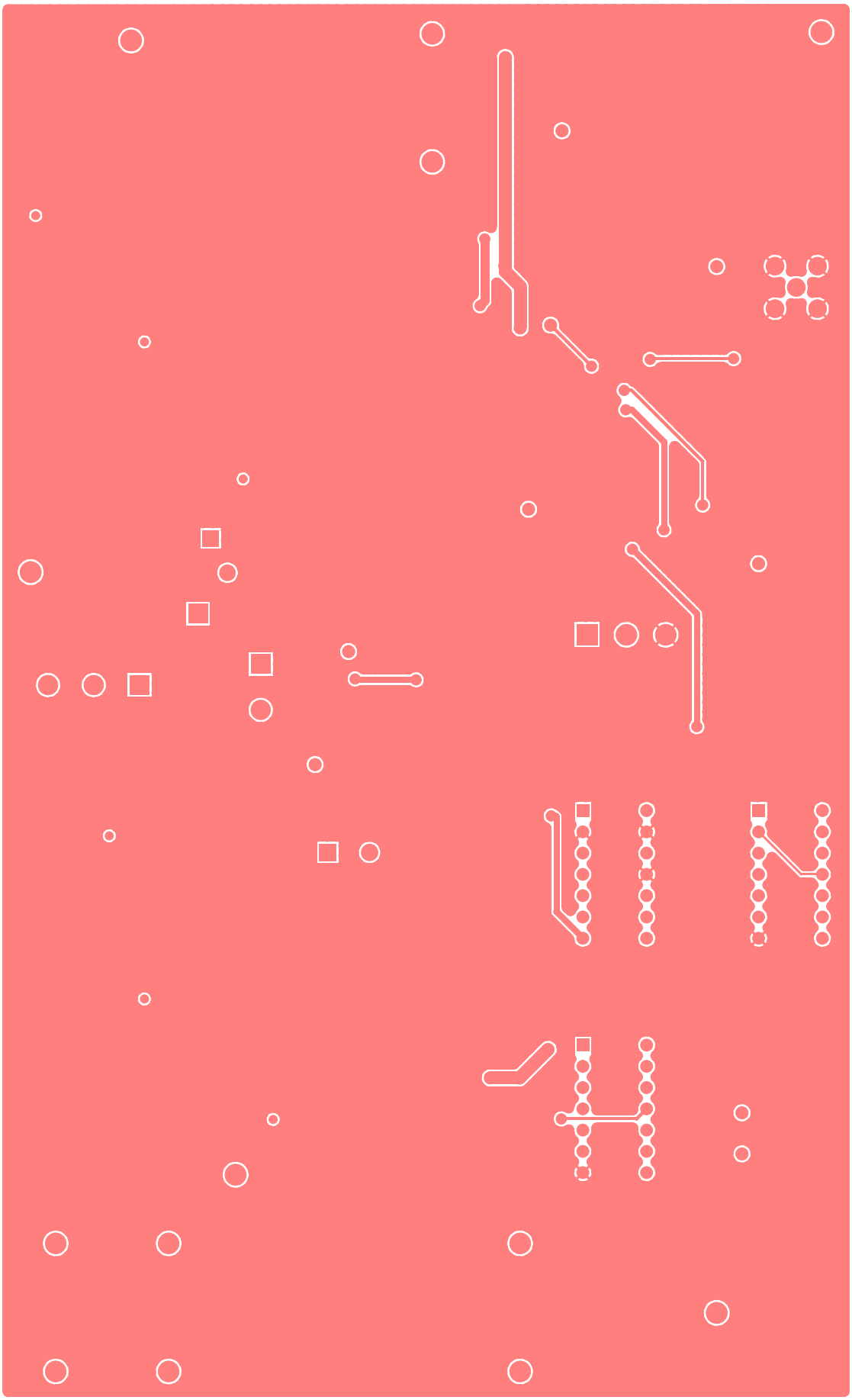

**Figure E.3** – Bottom PCB layer of the buck converter.

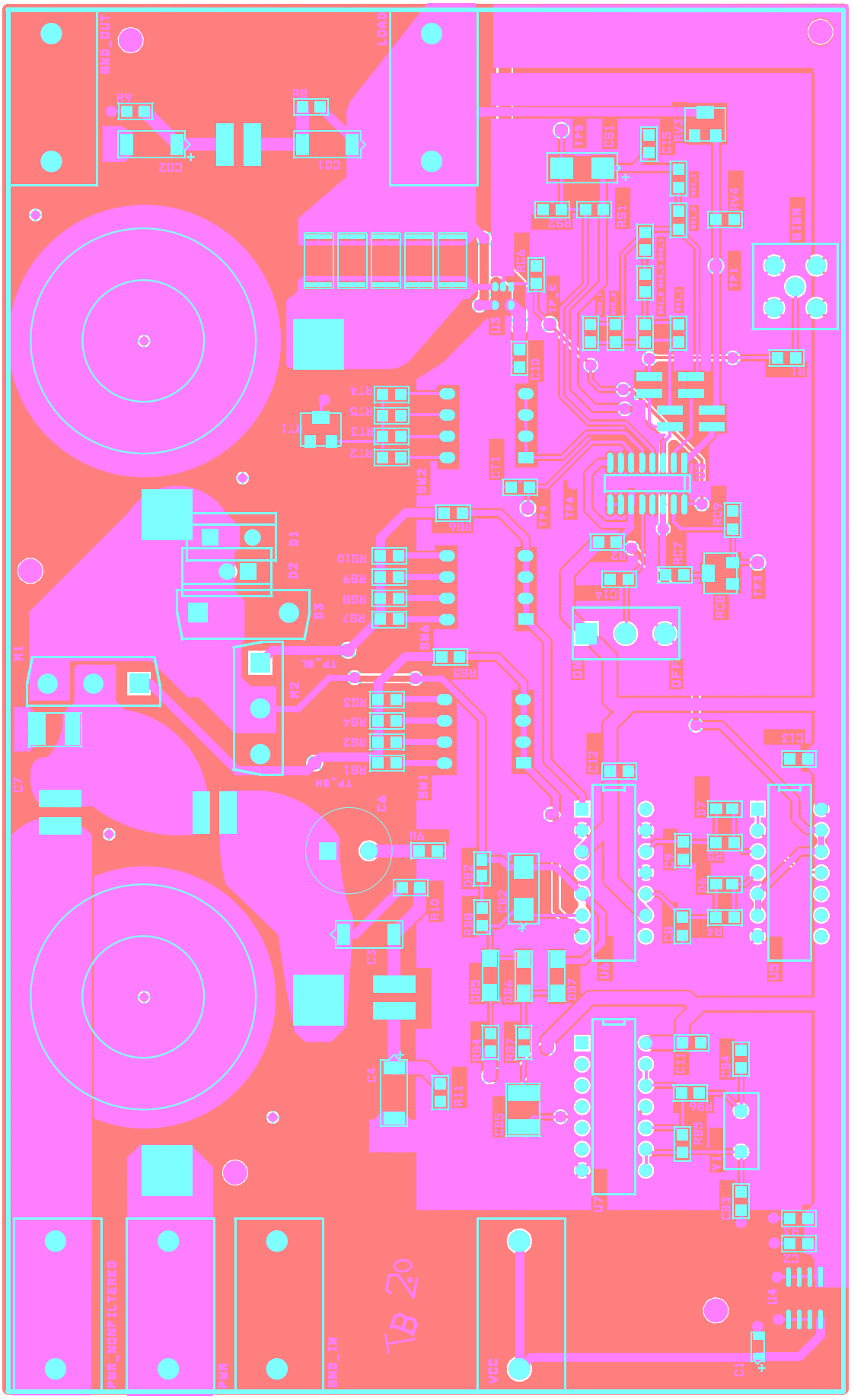


**Figure E.4** – Component placement outlined over the PCB of the buck converter.

# F Diode model implementation

### Initialisation file

```
1
2  % *****************
3  % Lauritzen 1991 with Cj
4  % *****************
5  clear all;
6  close all;
7  clc;
8
9  % Component constants taken from measurements on 20ETS12
10 % Diode constants for all models
11 IS = 900e-9;
12 N = 2;
13 tau = 2.455e-8;
14 Tm = 3.23e-8;
15 RS = 10e-4;
16 % Exta resistor for lauritzen 1991 with capacitor Cj..
17 Rc = 1e-10;
18 % Cj, capacitance constants
19 CJ0 = 6.986e-010;
20 VJ = 0.7;
21 M = 0.5;
22 FC = 0.5;
23 % Temperature constants
24 k = 1.381e-23;
25 q = 1.602e-19;
26 T = 300;
27 Vt = k*T/q;
28
29 % Simulation time
30
31 x_init = [0, -60];
32 Tstart = 0;
33 Factortime=4.8709e-006*10;
34 Outputtimes=linspace(0,1e-4,1e-4/10e-12);
35 Tstop = 15e-3;
36 Tstepmax = 60e-12;
37 residualtol = 1e-9;
38
39 sim('MOSFET_model_with_Cj_simple');
```

### Lauritzen diode s-function

```
function [sys, x0, str, ts] = Lauritzen_1991_s_function_with_Cj(t, x, u,
flag, x_init, IS, tau, Tm, N, RS, Vt, CJ0, VJ, M, FC, Rc)

    %*************************************************************************
    % A test of making an s-function for a MOSFET
    %*************************************************************************

    switch flag,

        %*************************************************************************
        % Initialization
        %*************************************************************************
        case 0,
            [sys,x0,str,ts] = mdlInitializeSizes(x_init);

        %*************************************************************************
        % Derivatives
        %*************************************************************************
        case 1,
            sys = mdlDerivatives(t, x, u, flag, x_init, IS, tau, Tm, N, RS
            , Vt, CJ0, VJ, M, FC, Rc);

        %*************************************************************************
        % Update
        %*************************************************************************
        case 2,
            sys = mdlUpdate(t, x, u, flag, x_init, IS, tau, Tm, N, RS, Vt,
            CJ0, VJ, M, FC, Rc);

        %*************************************************************************
        % Outputs
        %*************************************************************************
        case 3,
            sys = mdlOutputs(t, x, u, flag, x_init, IS, tau, Tm, N, RS, Vt
            , CJ0, VJ, M, FC, Rc);


        %*************************************************************************
        % Unhandled flags %
        %*************************************************************************
        case {4, 9},
            sys = [];

        %*************************************************************************
        % Unexpected flags
        %*************************************************************************
        otherwise
            error(['Unhandled flag = ',num2str(flag)]);
    end;
```

```
50
51
52
53
54
55 %*************************************************************************
56 % mdlInitializeSizes
57 % Return the sizes, initial conditions, and sample times
58 % for the S-function.
59 %*************************************************************************
60
61 function [sys,x0,str,ts] = mdlInitializeSizes(x_init)
62
63
64     %*********************
65     % call simsizes for a sizes structure.
66     % Fill it in and convert it to a sizes array.
67     %*********************
68     sizes = simsizes;
69     sizes.NumContStates  = 2;
70     sizes.NumDiscStates  = 0;
71     sizes.NumOutputs     = 9;
72     sizes.NumInputs      = 1;
73     sizes.DirFeedthrough = 1;
74     sizes.NumSampleTimes = 1;
75     sys = simsizes(sizes);
76
77     %*********************
78     % Initial conditions specified in main file.
79     %*********************
80     x0 = x_init;
81
82     %*********************
83     % str is always an empty matrix
84     %*********************
85     str = [];
86
87     %*********************
88     % initialize the array of sample times
89     %*********************
90     ts  = [0 0];
91
92
93 %*************************************************************************
94 % mdlDerivatives
95 % Return the derivatives for the continuous states.
96 %*************************************************************************
97
98 function sys = mdlDerivatives(t, x, u, flag, x_init, IS, tau, Tm, N, RS,
99 Vt, CJ0, VJ, M, FC, Rc)
100
101     %*********************
```

```
102     % Inputs (u)
103     %*********************
104     Vak = u(1);
105
106     %*********************
107     % States (x) and voltages
108     %*********************
109     qm = x(1);
110     Vc = x(2);
111
112     % If the capacitor Cj is connected directly on the pn-junction, then
113     % both voltages will become the same.
114     Vpn = Vc;
115
116     %*********************
117     % Model description
118     %*********************
119
120     % Vpn = fzero(@(Vpn) func_1991_C(Vpn, Vak, Vt, RS, N, IS, tau, qm, Tm,
121     % Rc, Vc), 1);
122     f2 = (1-FC)^(1+M);
123     f3 = 1-FC*(1+M);
124     if (Vpn < FC*VJ)
125         Cj = CJ0*(1 - (Vpn/VJ))^(-M);
126         Cd = IS*tau^2/(Tm*N*Vt)*exp(Vpn/(N*Vt));
127     else
128         Cj = (CJ0/f2)*(f3*M*Vpn/VJ);
129         Cd = IS*tau^2/(Tm*N*Vt)*exp(Vpn/(N*Vt));
130     end;
131
132     qe = IS*tau*(exp(Vpn/(N*Vt))-1);
133     dqm_dt = - qm/tau + (qe - qm)/Tm;
134
135     % The derivative of the capacitor voltage if a small resistor is
136     % connected in series.
137     % dVc_dt = (Vpn - Vc)/((Cd + Cj)*Rc);
138
139     % Derivation without Rc..
140     %
141     % We know that:
142     % qe = IS*tau*(exp(Vpn/(N*Vt))-1);
143     % ipn = (qe - qm)/Tm;
144     %
145     % iqj = Ctot*dVpn_dt;
146     % Vpn = Vak - (ipn + iqj)*RS;
147     % Vpn = Vak - (ipn + Ctot*dVpn_dt)*RS;
148     % dVpn_dt = ((Vak - Vpn)/RS - ipn)/Ctot;
149     % dVpn_dt = ((Vak - Vpn)/RS - ((qe - qm)/Tm))/Ctot;
150     % dVpn_dt = ((Vak - Vpn)/RS - (((IS*tau*(exp(Vpn/(N*Vt))-1)) - qm)/Tm))
151     % /Ctot;
152
153     dVpn_dt = ((Vak - Vpn)/RS - (((IS*tau*(exp(Vpn/(N*Vt))-1)) - qm)/Tm))
```

```
154      /(Cd + Cj);
155      sys(1) = dqm_dt;
156      sys(2) = dVpn_dt;
157
158  %*************************************************************************
159  % mdlUpdate
160  % Handle discrete state updates, sample time hits, and major time step
161  % requirements.
162  %*************************************************************************
163
164  function sys = mdlUpdate(t, x, u, flag, x_init, IS, tau, Tm, N, RS, Vt,
165  CJ0, VJ, M, FC, Rc)
166
167      sys = [];
168
169
170  %*************************************************************************
171  % mdlOutputs
172  % Return the block outputs.
173  %*************************************************************************
174
175  function sys = mdlOutputs(t, x, u, flag, x_init, IS, tau, Tm, N, RS, Vt,
176  CJ0, VJ, M, FC, Rc)
177
178      %**********************
179      % Inputs (u)
180      %**********************
181      Vak = u(1);
182
183      %**********************
184      % States (x) and voltages
185      %**********************
186      qm = x(1);
187      Vc = x(2);
188
189      % If the capacitor Cj is connected directly on the pn-junction, then
190      % both voltages will become the same.
191      Vpn = Vc;
192
193      %**********************
194      % Model description
195      %**********************
196
197      % Vpn = fzero(@(Vpn) func_1991_C(Vpn, Vak, Vt, RS, N, IS, tau, qm, Tm,
198      % Rc, Vc), 1);
199      f2 = (1-FC)^(1+M);
200      f3 = 1-FC*(1+M);
201      if (Vpn < FC*VJ)
202          Cj = CJ0*(1 - (Vpn/VJ))^(-M);
203          Cd = IS*tau^2/(Tm*N*Vt)*exp(Vpn/(N*Vt));
204      else
205          Cj = (CJ0/f2)*(f3*M*Vpn/VJ);
```

```
206         Cd = IS*tau^2/(Tm*N*Vt)*exp(Vpn/(N*Vt));
207     end;
208
209     qe = IS*tau*(exp(Vpn/(N*Vt))-1);
210     ipn = (qe - qm)/Tm;
211     dVpn_dt = ((Vak - Vpn)/RS - (((IS*tau*(exp(Vpn/(N*Vt))-1)) - qm)/Tm))
212     /(Cd + Cj);
213     iqj = (Cd + Cj)*dVpn_dt;
214     itot = ipn + iqj;
215
216     % The derivative of the capacitor voltage if a small resistor is
217     % connected in series.
218     % dVc_dt = (Vpn - Vc)/((Cd + Cj)*Rc);
219     % iqj = (Cd + Cj)*dVc_dt;
220
221     %*********************
222     % Outputs (from the s-function)
223     %*********************
224     sys(1) = Vpn;
225     sys(2) = Vc;
226     sys(3) = ipn;
227     sys(4) = iqj;
228     sys(5) = itot;
229     sys(6) = qe;
230     sys(7) = qm;
231     sys(8) = Cd;
232     sys(9) = Cj;
```

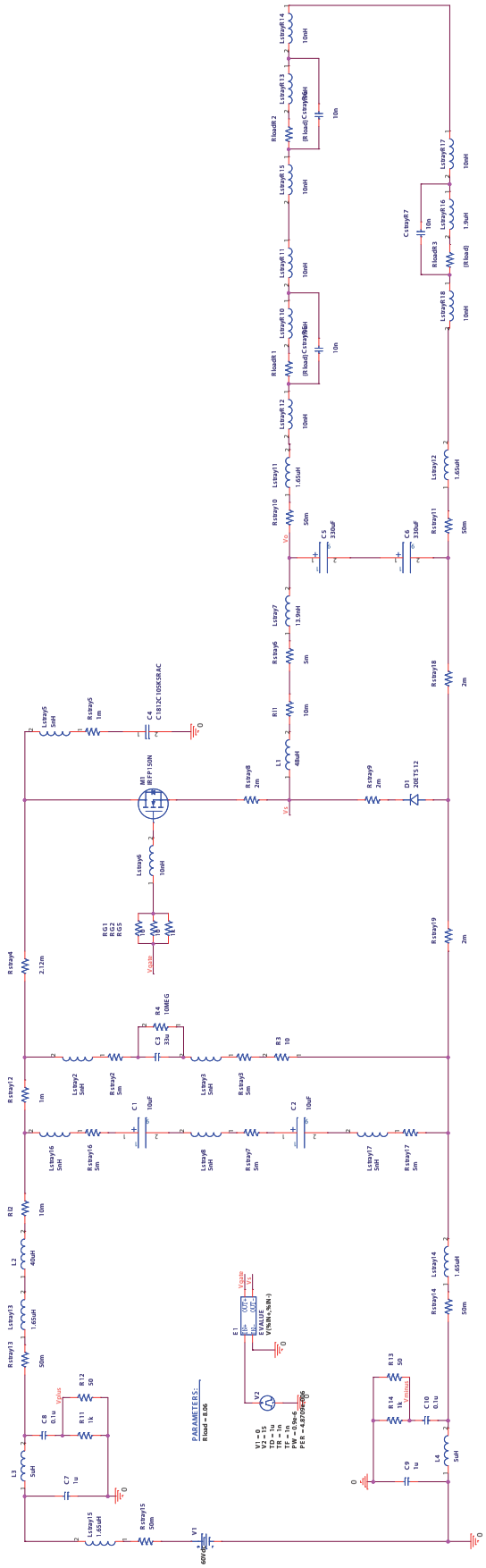

**Figure F.1** – SPICE model of the buck converter using the conventional diode model, in this case the 20ETS12 diode from IRF.

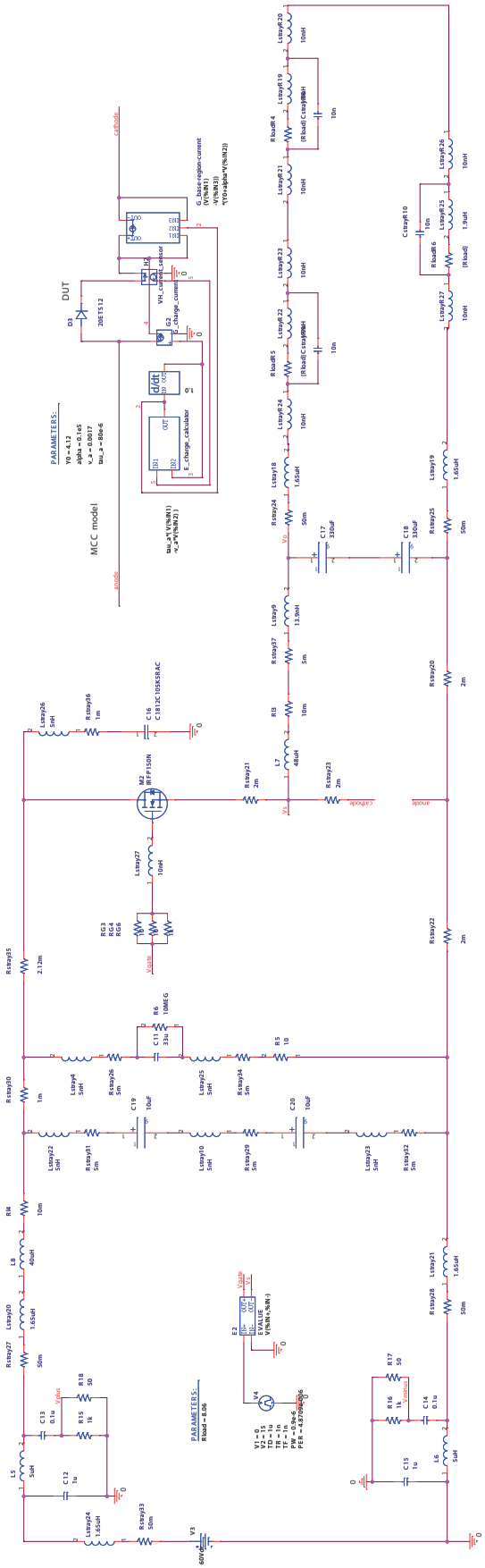


**Figure F.2** – SPICE model of the buck converter using the MCC diode model.

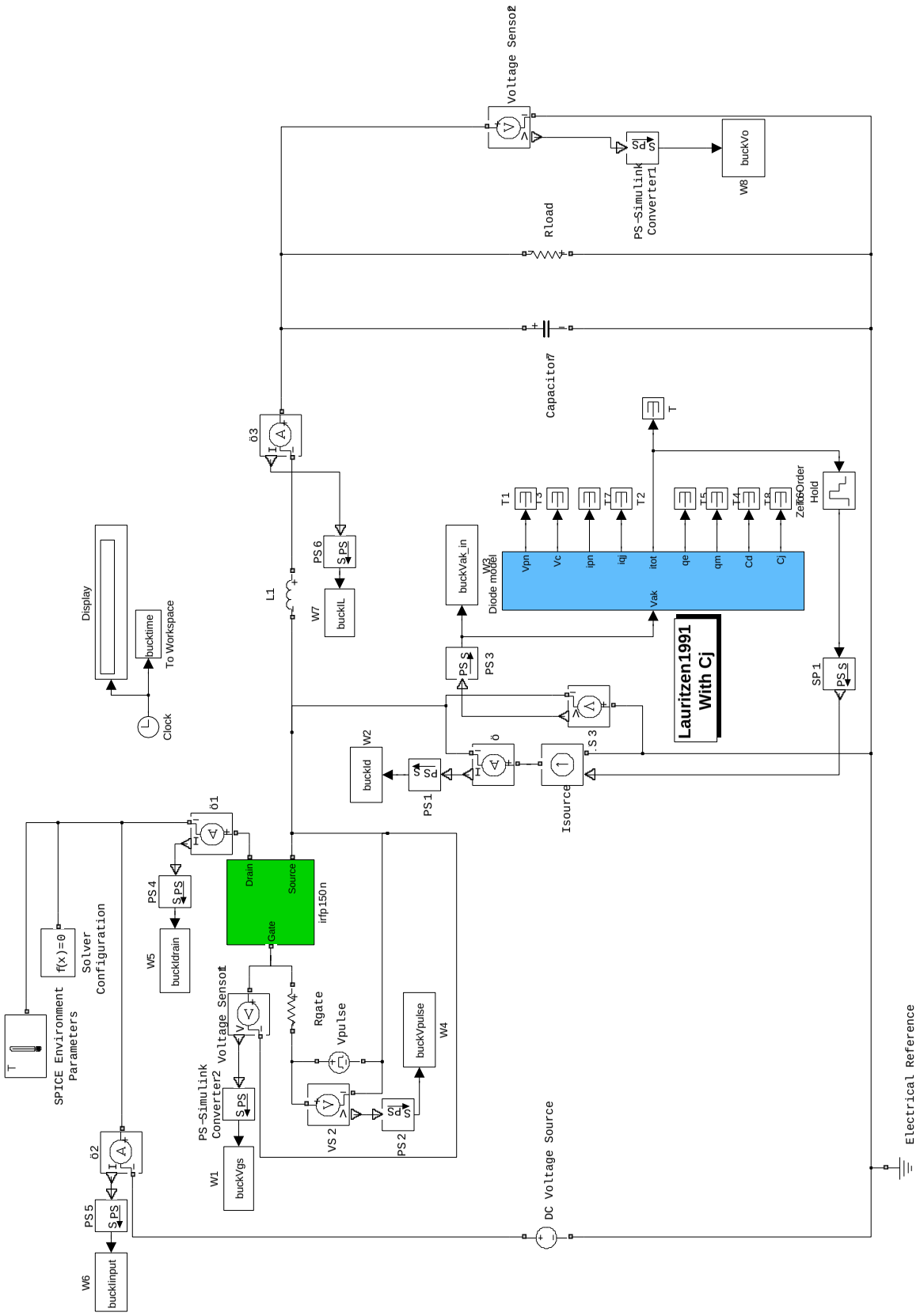


**Figure F.3** – Buck converter implemented in SimElectronics with the Lauritzen diode model.

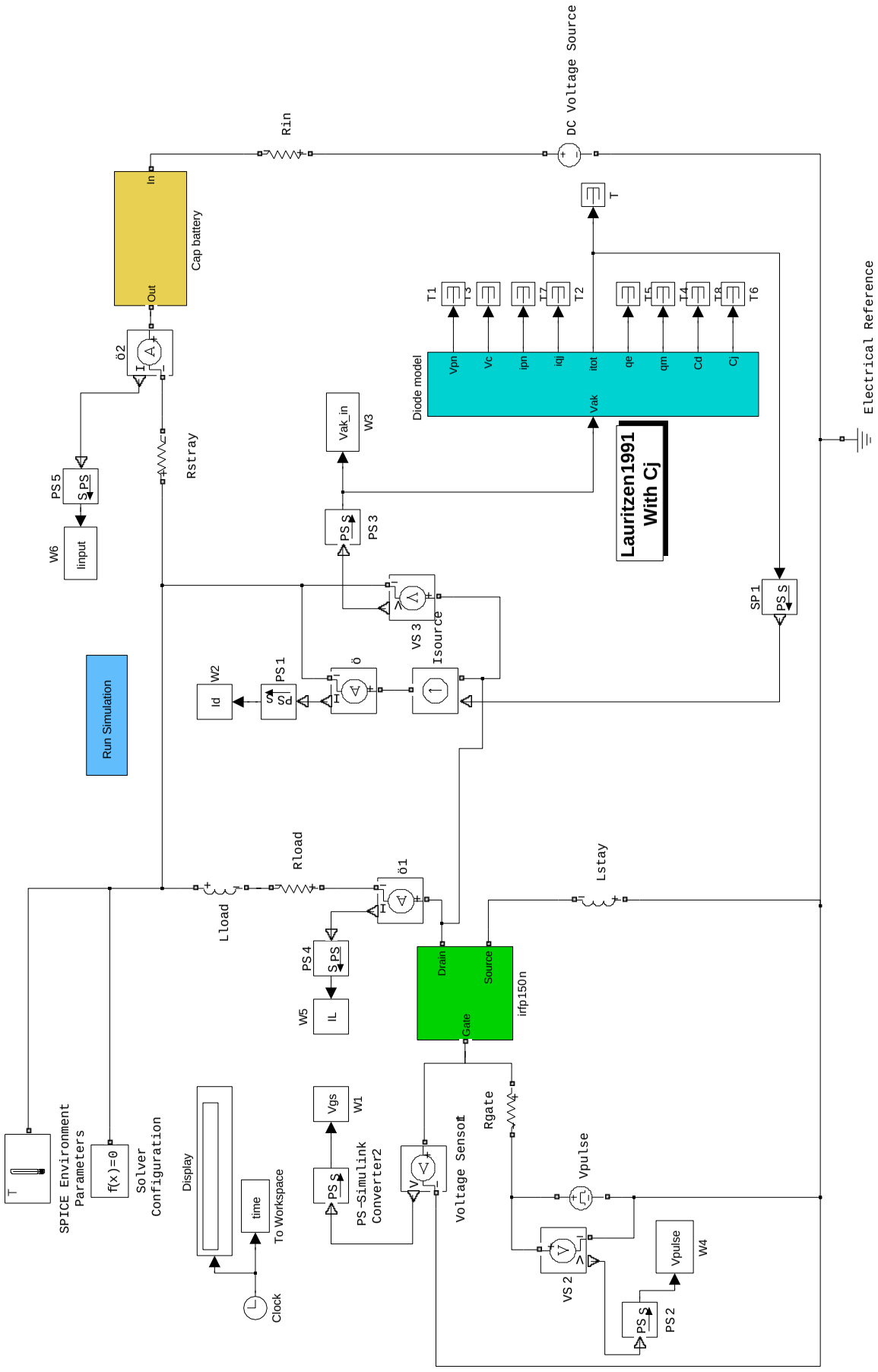


**Figure F.4** – Diode tester circuit implemented in SimElectronics.