Voltage Oriented Control of Three-Phase Boost PWM Converters
Design, simulation and implementation of a 3-phase boost battery charger

Master of Science Thesis in Electric Power Engineering

Sylvain LECHAT SANJUAN

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden, 2010
Voltage Oriented Control of Three-Phase Boost PWM Converters

Design, simulation and implementation of a 3-phase boost battery charger

By

Sylvain LECHAT SANJUAN

Supervisor
Saeid Haghbin, PhD Student

Examiner
Ola Carlson, Associate Professor

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden, 2010
VOLTAGE ORIENTED CONTROL OF THREE-PHASE BOOST PWM CONVERTERS
DESIGN, SIMULATION AND IMPLEMENTATION OF A 3-PHASE BOOST BATTERY CHARGER
SYLVAIN LECHAT SANJUAN

© SYLVAIN LECHAT SANJUAN, 2010

Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
SE-412 96 Göteborg
Sweden
Telephone: + 46 (0)31-772 1000
ABSTRACT

Voltage Oriented Control of Three-Phase Boost PWM Converters
Design, simulation and implementation of a 3-phase boost battery charger

Sylvain LECHAT SANJUAN
Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology

In a plug-in hybrid electric vehicle, the utility grid will charge the vehicle battery through the battery charger. For a three-phase grid supply voltage, three-phase boost rectifiers are a commonly used scheme for chargers. Bi-directional power transfer capability and unit power factor operation are interesting features that can be achieved by the method proposed in this thesis. Different control strategies have been proposed to control the converter. The Voltage Oriented Control is one of these methods based on high performance dq-coordinate controllers.

The Voltage Oriented Control method for a three-phase boost rectifier have been designed and simulated. Moreover, an implementation of the system has been started. The system simulation has been done using Matlab/Simulink software. Feedforward decoupled current controller has been designed along with Pulse Width Modulation scheme to control the battery charging. The controller, that is, a current controller and a DC-link voltage controller, have been designed using a method called Internal Model Control. The simulation results have been presented and the control system performance evaluated in response to the load and dc-bus voltage step changes. dSpace system have been used for practical implementation. The system is directly running a Simulink model as a controller. The Simulink files have been developed for this purpose. A brief explanation of the system configuration has been provided for the experimental system.

Key words: battery charger, decoupled controller, dSpace, Internal Model Control (IMC), Pulse Width Modulation (PWM), three-phase boost PWM rectifier, Voltage Oriented Control (VOC).
ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to Saeid Haghbin, my supervisor, for his total availability during the thesis, for his understanding, technical guidance and friendliness.

My gratitude also goes to Ola Carlson, for giving me the opportunity to do this Master’s Thesis work in the Electric Power division of Chalmers University of Technology.

A very special thanks to Stefan Lundberg and Massimo Bongiorno, for all help, their availability, technical guidance and nice discussions.

Thanks to all the employees and staff in the division who made my thesis work such a pleasant stay. Furthermore, I would like to thank Magnus Ellsen for his availability and help for laboratory set-up.

Finally, many thanks to my fellow Master’s Thesis students with Saman Babaei, Thinley Gyeltshen, Francisco Montes Venero, Peng Hou, Sergio Garcia Collino and Johan Andersson. Thanks for their support, guidance and nice discussions. They also made my stay in Sweden an unforgettable experience.

Sylvain Lechat Sanjuan
Göteborg, Sweden
Wednesday, June 16, 2010
LIST OF SYMBOLS, SUPERSCRIPTS, SUBSCRIPTS AND ABBREVIATIONS

ABBREVIATIONS

DPC       Direct Power Control
IC        Initial Condition
IGBT      Insulated Gate Bipolar Transistor
IM        Induction Machine
IMC       Internal Model Control
PWM       Pulse Width Modulation
PLL       Phase Locked Loop
PMSM      Permanent Magnet Synchronous Machine
SVM       Space Vector Modulation
VF-DPC    Virtual Flux Direct Power Control
VFOC      Virtual Flux Oriented Control
VOC       Voltage Oriented Control

SYMBOL

$U$       Line voltage
$E$       Line voltage
$E_g$     Grid phase-to-ground voltage amplitude
$E_d$ and $E_q$ dq-coordinates of line or grid voltage (amplitude invariant transformation)
$V_{pcc}$ Voltage at the point of common connection
$U_s$     Converter voltage
$V$       Converter voltage
$V^*$     Converter voltage reference from current controller
$V_{LL}$  Line-to-Line voltage
$V_{LN}$  Line-to-Neutral voltage
$V_{LN(peak)}$ Amplitude of Line-to-Neutral voltage
$E_m$     Amplitude of Line-to-Neutral voltage
$v_{dc}, V_{DC}$ DC-link voltage
$v_c$     Voltage across AC-side capacitor
$i_l$     Line current
$i$       Line current
$i_{conv}$ Line current, current flowing into the converter
$i_{dc}$  DC-link current
$i_{load}$ Load current
$R$       Line resistance
$L$       Line inductance
$C$       DC-link capacitor
$R_g$     Grid resistance
$L_g$     Grid inductance
$R_b$     Breaker SW1 resistance
$C_{ac}$  AC capacitor
$C_{dc}$  DC capacitor
$R_{load}$ Load resistance
$R_{load, temp}$ Temporary load resistance
$\theta$  Voltage angle
$F_s$     Sampling frequency
$T_s$     Sampling time
\( F_{SW} \)  
Switching frequency

\( F_c \)  
Triangular wave frequency (PWM)

\( F_{Triangle} \)  
Triangular wave frequency (PWM)

\( \alpha_i \)  
Current controller bandwidth (rad/s)

\( \alpha_v \)  
Voltage controller bandwidth (rad/s)

\( Ga \)  
Active damping conductance

\( Ki_v \)  
Voltage controller integrator coefficient

\( Kp_v \)  
Voltage controller proportional coefficient

\( Ki_i \)  
Current controller integrator coefficient

\( Kp_i \)  
Current controller proportional coefficient

\( \gamma_1 \)  
PLL Integrator coefficient

\( \gamma_2 \)  
PPL proportional coefficient

\( \rho \)  
PPL bandwidth

\( F(s) \)  
Controller transfer function (PI)

\( G(s) \)  
Process transfer function

\( L(s) \)  
Open-loop transfer function

\( S(s) \)  
Closed-loop transfer function

\( W \)  
\( v^2_{dc} \)

\( P_g \)  
Grid power

\( P_{load} \)  
Load power

**SUPERSCRIPT, ACCENTS**

\( \hat{E}_g, \hat{C}, \hat{L}, \hat{R} \)  
Estimated values

\( x^s \)  
Space vector

\( x^{dq} \)  
dq-coordinate system

\( x^* \)  
Reference value of \( x \)

**SUBSCRIPT, UNDERLINE**

\( x_{dq} \)  
dq-coordinate system

\( \underline{x} \)  
dq-coordinate system, complex value
# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSTRACT</td>
<td>IV</td>
</tr>
<tr>
<td>ACKNOWLEDGEMENTS</td>
<td>V</td>
</tr>
<tr>
<td>LIST OF SYMBOLS, SUPERSCRIPTS, SUBSCRIPTS AND ABBREVIATIONS</td>
<td>VI</td>
</tr>
<tr>
<td>1 INTRODUCTION AND SCOPE</td>
<td>1</td>
</tr>
<tr>
<td>2 THREE PHASE CONTROLLED RECTIFIERS</td>
<td>3</td>
</tr>
<tr>
<td>2.1 Introduction</td>
<td>3</td>
</tr>
<tr>
<td>2.2 Universal bridge topology</td>
<td>5</td>
</tr>
<tr>
<td>2.2.1 Steady state operation</td>
<td>5</td>
</tr>
<tr>
<td>2.2.2 Mathematical model</td>
<td>5</td>
</tr>
<tr>
<td>2.2.3 Limitations</td>
<td>9</td>
</tr>
<tr>
<td>2.3 Control strategies</td>
<td>11</td>
</tr>
<tr>
<td>2.3.1 Introduction</td>
<td>11</td>
</tr>
<tr>
<td>2.3.2 Direct Power Control and Virtual Flux Direct Power Control</td>
<td>12</td>
</tr>
<tr>
<td>2.3.3 Voltage and Virtual Flux Oriented Control</td>
<td>13</td>
</tr>
<tr>
<td>2.3.4 Comparison and discussion</td>
<td>14</td>
</tr>
<tr>
<td>2.4 Pulse Width Modulation</td>
<td>15</td>
</tr>
<tr>
<td>2.4.1 Sinusoidal PWM</td>
<td>15</td>
</tr>
<tr>
<td>2.4.2 Digital implementation</td>
<td>16</td>
</tr>
<tr>
<td>2.4.3 Dead time effect</td>
<td>16</td>
</tr>
<tr>
<td>3 VOLTAGE ORIENTED CONTROL – SIMULATION</td>
<td>18</td>
</tr>
<tr>
<td>3.1 Introduction – References chosen</td>
<td>18</td>
</tr>
<tr>
<td>3.2 System block diagram</td>
<td>19</td>
</tr>
<tr>
<td>3.3 PWM Simulation</td>
<td>20</td>
</tr>
<tr>
<td>3.3.1 Simulink implementation of PWM</td>
<td>20</td>
</tr>
<tr>
<td>3.4 Current controller</td>
<td>22</td>
</tr>
<tr>
<td>3.4.1 Internal Model Control</td>
<td>22</td>
</tr>
<tr>
<td>3.4.2 Synchronous PI control</td>
<td>22</td>
</tr>
<tr>
<td>3.4.3 Design of the synchronous PI controller</td>
<td>23</td>
</tr>
<tr>
<td>3.4.4 Active damping, voltage saturation, anti-windup</td>
<td>25</td>
</tr>
<tr>
<td>3.4.5 Current controller simulation</td>
<td>27</td>
</tr>
<tr>
<td>3.5 DC-link voltage controller</td>
<td>30</td>
</tr>
<tr>
<td>3.5.1 DC-link model and linearization</td>
<td>30</td>
</tr>
<tr>
<td>3.5.2 Design of voltage controller</td>
<td>30</td>
</tr>
<tr>
<td>3.5.3 Voltage saturation, anti-windup, active damping</td>
<td>31</td>
</tr>
<tr>
<td>3.5.4 Voltage controller simulation</td>
<td>33</td>
</tr>
<tr>
<td>3.5.5 Simulation with current controller</td>
<td>36</td>
</tr>
<tr>
<td>3.5.6 Controller improvements</td>
<td>39</td>
</tr>
<tr>
<td>3.6 Stability analysis</td>
<td>41</td>
</tr>
</tbody>
</table>
1 INTRODUCTION AND SCOPE

PHD PROJECT

The master thesis is part of a PHD project titled “Integrated charger for plug-in Hybrid Electric Vehicles”. The PHD project is funded by the Swedish Hybrid Vehicle Centre (SHC) and is being done by the PHD student Saeid Haghbin under supervision of Associate Professor Ola Carlson. Moreover, Assistant Professor Sonja Lundmark is the project co-supervisor.

The scope of the PHD project is:

- Investigating and evaluating existing plug-in HEV’s in general and especially the charging systems. This collection of available information also includes listing all as well as the most interesting parameters of the charger, i.e. speed of charging, power rating, cost, volume and weight, number of phases, voltage levels, ease of charging and availability of charging places, limitations on power electronic components, power factor, harmonic distortion, monitoring equipment, standards, and persons safety. The study should involve battery knowledge, so that the charger could be fully adapted to the battery, giving a long battery life length.

- Suggest and evaluate possible integrated chargers, meaning integration of the charger and the available drive system used for propulsion of the vehicle.

- Prototype building in cooperation with the whole group (including industry). One prototype coordinator from industry administers the task. The task also incorporates preparations for lab testing.

MASTER THESIS SCOPE

The thesis is part on the sub project “On Board Integrated Charging”. The main goal is to design, simulate and implement a 3-phase boost battery charger with power factor correction.

![Rectifier schematic with AC machine](image)

\[\text{Figure 1.1: Rectifier schematic with AC machine}\]

The Figure 1.1 represent our system. The first idea was to use an AC motor on the AC-side. Some data are given is Table 1.1.

---

1 SHC is composed with three different partners: three universities with Lund Institute of Technology (LTH), Royal Institute of Technology (KTH) and Chalmers University of Technology (CTH), The Swedish Energy Agency (Energimyndigheten) and automotive industry with AB Volvo, Volvo Car Corporation, Saab Automobile AB, GM Powertrain Sweden AB, Scania CV AB, BAE Systems Hägglunds AB.
At the beginning of thesis, a first plan had been established.
1) Literature review (how the system work/find literature resources)
2) Topology selection (VFOC is preferred method regarding to this specific application)
3) System design (inductance value, switching frequency, control design)
4) Simulation with Matlab/Simulink
5) Addition of PMSM to the model and using the leakage inductance of the machine as energy storage device (Re-design/Re-simulation)
6) Implementation
   a. dSpace system
   b. Software development
   c. Hardware test (in development)
7) Testing and debugging / Report

Nevertheless, after a couple of weeks we decided to simplify the system to keep a grid connected rectifier and try to implement it in the laboratory to test the controller.

The main goal of the thesis is to develop and test the control algorithm of the converter.

* * *

We will start this thesis with an overview of three-phase controlled rectifiers (chapter 2), with steady state operation, modeling, limitations. Then, the overview will focus on control strategies, and finally, a Pulse Width Modulation (PWM) will be describe.
Chapter 3 will be the main part of the report with Voltage Oriented Control design and simulation. We will see the current and voltage controller, stability analysis, Phase Locked Loop (PLL), and finally a simulation of grid connected converter.
The last part chapter 4 will give the main guidelines for implementation of the controller using dSpace system.
2 THREE PHASE CONTROLLED RECTIFIERS

2.1 Introduction

In the following part, we will see some topologies for 3-phase rectifiers. But we can start to explain why those topologies appeared. The high harmonic content and a low power factor cause some problems in power distribution system. New standards have been introduced by governments or organizations to limit the harmonic content of the current drawn from the power line by rectifiers. Consequently, new topologies have been deployed for rectification applications [9].

We can introduced five topologies (Figure 2.1).

The figure a) present a simple solution of Boost converter. The main drawback of this solution is stress on the components and low frequency distortion of the input current.

The topologies b) and c) use PWM rectifier modules with a very low current rating (20-25% level of RMS current comparable with e) topology). Hence they have a low cost potential and provide only the possibility of regenerative braking mode b) or active filtering c).

Figure d) presents a converter called a Vienna rectifier. The main advantage is low switch voltage, but non-typical switches are required.

Figure e) presents the most popular topology. This universal topology has the advantage of using a low-cost three-phase module with a bidirectional energy flow capability, and it can also provide a unity power factor (UPF). However, its disadvantages are a high per-unit current rating, poor immunity to shoot-through faults, and high switching losses [9].

Topologies are compared in a table (see Table 2.1). A diode rectifier is also included to the table for comparison.
Figure 2.1: Three-phase rectifier topologies [9] [13]

<table>
<thead>
<tr>
<th>FEATURE TOPOLOGY</th>
<th>REGULATION OF DC OUTPUT VOLTAGE</th>
<th>LOW HARMONIC DISTORSION OF LINE CURRENT</th>
<th>NEAR SINUSOIDAL CURRENT WAVEFORMS</th>
<th>POWER FACTOR CORRECTION</th>
<th>BIDIRECTIONAL POWER FLOW</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode rec.</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Rec. (a)</td>
<td>+</td>
<td>–</td>
<td>–</td>
<td>+</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Rec. (b)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>+</td>
<td>–</td>
</tr>
<tr>
<td>Rec. (c)</td>
<td>–</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>–</td>
<td>UPF</td>
</tr>
<tr>
<td>Rec. (d)</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>–</td>
<td>UPF</td>
</tr>
<tr>
<td>Rec. (e)</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>–</td>
<td>UPF</td>
</tr>
</tbody>
</table>

Table 2.1: Three-phase rectifier topologies, performance comparison [9] [13]
2.2 Universal bridge topology

2.2.1 Steady state operation

Figure 2.2 shows basic diagram of the three-phase boost converter. $u_l$ is the line voltage and $u_f$ is the bridge converter voltage controllable from de the dc-side. We can draw a general phasor diagram and diagrams for both rectification and regeneration operation at unity power factor (UPF).

Figure 2.3: Phasor diagrams [9]

The line current $i_L$ is controlled by the voltage drop across the inductance $L$ interconnecting the two voltage sources (line and converter).

When we control the phase angle $\varepsilon$ and the amplitude of converter voltage $u_s$, we control indirectly the phase and amplitude of the line current. In this way, the average value and sign of the dc current is subject to control that is proportional to the active power conducted through the converter. The reactive power can be controlled independently with a shift of the fundamental harmonic current $i_l$ with respect to voltage $U_l$ [9].

Remark: Inductors connected between the line and the rectifier input bring a current source character of the input circuit and provide the boost feature of the converter [9].

2.2.2 Mathematical model

DESCRIPTION OF INPUT VOLTAGE AND CURRENT

The three-phase line voltage and current are
THREE PHASE CONTROLLED RECTIFIERS

\[ u_a = E_m \cos(\omega t) \]
\[ u_b = E_m \cos\left(\omega t - \frac{2\pi}{3}\right) \]
\[ u_c = E_m \cos\left(\omega t - \frac{4\pi}{3}\right) \]  \hfill (2.1)

\[ i_a = I_m \cos(\omega t + \varphi) \]
\[ i_b = I_m \cos\left(\omega t + \varphi - \frac{2\pi}{3}\right) \]
\[ i_c = I_m \cos\left(\omega t + \varphi - \frac{4\pi}{3}\right) \]  \hfill (2.2)

and since there is no neutral connection, we obtain

\[ i_a + i_b + i_c = 0. \]  \hfill (2.3)

A three-phase system can be described with only two components \( \alpha \) and \( \beta \) (real and imaginary respectively). Furthermore, we call a space vector the quantity ([4] [12])

\[ v^s(t) = v_a(t) + jv_\beta(t) = \frac{2}{3} K \left( v_a(t) + v_b(t)e^{j\frac{2\pi}{3}} + v_c(t)e^{j\frac{4\pi}{3}} \right). \]  \hfill (2.4)

where \( K \) is a scaling constant (amplitude invariant \( K = 1 \), RMS-invariant \( K = 1/\sqrt{2} \), power invariant \( K = \sqrt{3/2} \) – Refer to APPENDIX A for details).

RECTIFIER ABC-MODEL [9]

\[ u_{Sab} = (Sa - Sb) \, u_{dc} \]
\[ u_{Sbc} = (Sb - Sc) \, u_{dc} \]
\[ u_{Sc} = (Sc - Sa) \, u_{dc} \]  \hfill (2.5)

with \( Si \) the switching function defined by: \( Si = \begin{cases} 1 & \text{upper switch ON} \\ 0 & \text{bottom switch ON} \end{cases} \) with phase \( i = a, b, c \).

\[ u_{Sa} = f_a \cdot u_{dc} \]
\[ u_{Sb} = f_b \cdot u_{dc} \]
\[ u_{Sc} = f_c \cdot u_{dc} \]  \hfill (2.6)

\[ f_a = S_a - S^* = S_a - \frac{1}{3}(S_a + S_b + S_c) = \frac{2S_a - (S_b + S_c)}{3} \]
\[ f_b = \frac{2S_b - (S_a + S_c)}{3} \]
\[ f_c = \frac{2S_c - (S_a + S_b)}{3} \]  \hfill (2.7)

\( (f_{abc} \text{ are } 0, \pm 1/3 \text{ or } \pm 2/3) \).

The rectifier in defined by four equations, one for each phase (voltage) and one for the currents (dc-link).

\[
\begin{bmatrix}
u_a \\
u_b \\
u_c
\end{bmatrix} = R \begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} + L \frac{d}{dt} \begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix} + \begin{bmatrix}
u_{Sa} \\
u_{Sb} \\
u_{Sc}
\end{bmatrix} \]  \hfill (2.8)
The combination of the previous equations can be represented as a block diagram.

\[
C \frac{du_{dc}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_{load} \tag{2.9}
\]

**RECTIFIER αβ-EQUATIONS**

We define the amplitude invariant Clarke transformation (see APPENDIX A) with \([4] [12]\)

\[
\begin{bmatrix}
\alpha \\
\beta \\
\gamma
\end{bmatrix} =
\begin{bmatrix}
\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\
0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}}
\end{bmatrix}
\begin{bmatrix}
\alpha \\
\beta \\
\gamma
\end{bmatrix}
\tag{2.10}
\]

\[
\begin{bmatrix}
\alpha \\
\beta \\
\gamma
\end{bmatrix} =
\begin{bmatrix}
1 & 0 & 0 \\
-\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \\
-\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0
\end{bmatrix}
\begin{bmatrix}
\alpha \\
\beta \\
\gamma
\end{bmatrix}
\tag{2.11}
\]

Then, applying this transformation we can find the voltage equations in αβ-coordinates

\[
\begin{bmatrix}
u_\alpha \\
u_\beta
\end{bmatrix} = R \begin{bmatrix}i_\alpha \\
i_\beta
\end{bmatrix} + L \frac{di_\alpha}{dt} + \begin{bmatrix}u_{\alpha \alpha} \\
u_{\beta \beta}
\end{bmatrix}
\tag{2.12}
\]

\[
C \frac{du_{dc}}{dt} = \frac{3}{2} (S_a i_\alpha + S_\beta i_\beta) - i_{load}.
\tag{2.13}
\]
**Rectifier dq-equations**

Now, we need to apply the Park transformation (see APPENDIX A and [4][12]) which is

\[ v_{dq} = v^s e^{-j\theta} \]  \hspace{1cm} (2.14)

where \( v^s \) is a space vector \( \{v^s = v_\alpha + jv_\beta\} \). We get

\[ u^s = Ri^s + \frac{di^s}{dt} + u^S_d \]  \hspace{1cm} (2.15)

\[ \Leftrightarrow u_{dq}e^{j\theta} = R_i_{dq}e^{j\theta} + \left(e^{j\theta}\left(j\omega i_{dq} + \frac{di_{dq}}{dt}\right)\right) + e^{j\theta}u_{Sdq} \]

\[ \Leftrightarrow u_{dq} = R_i_{dq} + \frac{di_{dq}}{dt} + jL\omega i_{dq} + u_{Sdq} \]  \hspace{1cm} (2.16)

And finally, with separation of Real and Imaginary part we obtain

\[ u_d = R_i_d + \frac{di_d}{dt} - \omega Li_q + u_{Sd} \]  \hspace{1cm} (2.17)

\[ u_q = R_i_q + \frac{di_q}{dt} + \omega Li_d + u_{Sq} \]  \hspace{1cm} (2.18)

\[ C \frac{du_{dc}}{dt} = \frac{3}{2}(S_i i_d + S_q i_q) - i_{load} \]  \hspace{1cm} (2.19)

**Instantaneous Power [4]**

From the well known relation \( P = Re\{V^I\} \) for single phase rms-value-scaled phasors \( V \) and \( I \) ("*" indicates complex conjugate), we know that instantaneous power for three-phase system will be proportional to

\[ Re\{v^s (i^s)^*\} = Re\{v^{dq} (i^{dq})^*\} \]  \hspace{1cm} (2.20)

Note that the formula is independent of the coordinate system.

From the space vector definition we get (the time argument "(t)" is removed for simplicity)

\[ v^s (i^s)^* = \left(\frac{2}{3}K\right)^2\left(v_a + v_be^{\frac{2\pi}{3}} + v_ce^{\frac{4\pi}{3}}\right)\left(i_a + i_be^{\frac{2\pi}{3}} + i_ce^{\frac{4\pi}{3}}\right)^* \]

\[ = \left(\frac{2}{3}K\right)^2\left[v_ai_a + v_bi_b + v_ci_c + j\frac{1}{\sqrt{3}}\left(v_a(i_c - i_b) + v_b(i_a - i_c) + v_c(i_b - i_a)\right)\right] \]

And finally, the Real part gives us the active power

\[ P = \frac{3}{2K^2} Re\{v^s (i^s)^*\} = \frac{3}{2K^2} Re\{v^{dq} (i^{dq})^*\} = v_ai_a + v_bi_b + v_ci_c. \]  \hspace{1cm} (2.21)

And with Imaginary part we obtain the reactive power

\[ Q = \frac{3}{2K^2} Im\{v^s (i^s)^*\} = \frac{3}{2K^2} Im\{v^{dq} (i^{dq})^*\} \]

\[ = \frac{1}{\sqrt{3}}\left[v_a(i_c - i_b) + v_b(i_a - i_c) + v_c(i_b - i_a)\right]. \]  \hspace{1cm} (2.22)
For ideal, positive sequence space vectors (voltage is reference)

\[ v^s = KE_m e^{j\omega t} \quad \text{and} \quad i^s = KI_m e^{j\omega t + \varphi} \]

where \( E_m \) and \( I_m \) are amplitude, the active power is given by

\[
P = \frac{3}{2K^2} \text{Re}\{v^s (i^s)^*\} = \frac{3}{2K^2} \text{Re}\{v^{dq} (i^{dq})^*\} = \frac{3}{2} E_m I_m \cos \varphi = 3V_1 \cos \varphi \quad (2.23)
\]

Where \( V \) and \( I \) are rms-values. This previous relation will be use in the DC-link voltage controller design.

### 2.2.3 Limitations

**MINIMUM DC-Link VOLTAGE**

For proper operation of the rectifier, a minimum dc-link voltage is needed to obtain undistorted current waveforms. To have a full control of the rectifier, its six diodes must be polarized negatively at all value of ac-voltage supply. To keep the diodes blocked, we need to ensure a dc-link voltage higher than the peak dc-voltage generated by the diodes alone. Theoretically for diode rectifier, the maximum dc output voltage is the peak value of line-to-line RMS voltage [9].

\[
V_{DC_{\text{min}}} > \sqrt{2} V_{LL_{\text{rms}}} = \sqrt{2} \cdot \sqrt{3} \cdot V_{LN_{\text{rms}}} \quad (2.24)
\]

![Figure 2.5: DC-link voltage condition](image)

It will be better to select a DC-link voltage about 15-20% more than \( \sqrt{2} V_{LL} \).

**IMPORTANT**: The previous voltage \( V_{LL_{\text{rms}}} \) correspond to the converter voltage (Us). There is no line impedance taking in account here.

Nevertheless, if there is no line impedance (\( R = 0 \Omega \), \( L=0H \)) we can continue to write the equation (2.24) according to the amplitude of supply voltage \( E_m \):

\[
V_{DC_{\text{min}}} > \sqrt{2} \cdot \sqrt{3} \cdot V_{LN_{\text{rms}}} = \sqrt{3} E_m. \quad (2.25)
\]

**ATTENTION**: This is a true definition but doesn’t apply in all situation [9]. The DC-link voltage depends on the PWM method. In our case, we will use a sinusoidal PWM. In this case the maximum reference voltage is Vdc/2 (Figure 2.6 [23]).
Finally, our minimum DC-link voltage will be

\[ V_{L,N(peak)} = \frac{V_{DC}}{2} \]  
\[ V_{LL(rms)} = \frac{2}{\sqrt{3}} V_{DC} \]

\[ V_{DC_{\text{min}}} > 2 V_{L,N(peak)} = \frac{2\sqrt{2}}{\sqrt{3}} V_{LL(rms)} = 1.663 V_{LL(rms)} \]  
(2.27)

**Minimum DC-link voltage and inductance**

The book [9] (chapter11 p434) defines a minimum DC-link voltage taking in account the line inductance value. The demonstration seems to be valid in our case for amplitude invariant (they assume a maximum converter voltage equal to \( \frac{2}{3} V_{dc} \) (i.e. radius of switching hexagon). It will be \( \sqrt{\frac{2}{3}} V_{dc} \) for power invariant). They define a DC-link voltage as

\[ V_{dc} > \sqrt{3 \left[ E_m^2 + (\omega L d)^2 \right]} \]  
(2.28)

We can observe that R is neglected and if L = 0 (if there is no inductance voltage), we find again the equation (2.25) where \( V_{DC_{\text{min}}} > \sqrt{3} E_m \).

From this equation we can get the maximum inductance value as

\[ L < \frac{\sqrt{\frac{V_{DC}^2}{3} - E_m^2}}{\omega L d} \]  
(2.29)

A low inductance will give a high current ripple and will make the design more dependent on the line impedance (refer to “3.8 Grid modeling” and “3.9.3 Simulation results”). According to [9], a high value of inductance will give a low current ripple, but simultaneously reduce the operation range of the rectifier. The voltage drop across the inductance controls the current. This voltage drop is controlled by the voltage of the rectifier but its maximal value is limited by the dc-link voltage. Consequently, a high current (high power) through the inductance requires either a high dc-link voltage or a low inductance (low impedance).
2.3 Control strategies

2.3.1 Introduction

The control of PWM converter can be considered as a dual problem with vector control of an induction motor IM (see figure and table below).

<table>
<thead>
<tr>
<th>Control of PWM rectifier</th>
<th>IM control</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPC</td>
<td>DTC</td>
</tr>
<tr>
<td>Direct Power Control</td>
<td>Direct Torque Control</td>
</tr>
<tr>
<td>VOC</td>
<td>FOC</td>
</tr>
<tr>
<td>Voltage Oriented Control</td>
<td>Field Oriented Control</td>
</tr>
</tbody>
</table>

*Figure 2.7: PWM rectifier and IM control duality*

<table>
<thead>
<tr>
<th>Control of PWM rectifier</th>
<th>IM control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed control loop of vector drive</td>
<td>dc-link voltage</td>
</tr>
<tr>
<td>Reference angle between stator current and rotor flux</td>
<td>Reference angle of line voltage</td>
</tr>
</tbody>
</table>

*Table 2.2: PWM rectifier and IM control duality [9]*

We can classify the PWM rectifier method in two categories: **voltage** based and **virtual flux** based control (See following Figure 2.8).

*Figure 2.8: Control strategies [9]*

All these control strategies can achieve the same main goals, such as high power factor and near sinusoidal input current waveforms.

**The Voltage Oriented Control (VOC)** guarantees high dynamic and static performance via an internal current control loop. But the quality depends mainly on the current control strategy.

**The Direct Power Control (DPC)** is based on the instantaneous active and reactive power control loop. There are no internal current control loop and no PWM modulator block. The switching state are determined with a switching table based on the instantaneous errors between the commanded and estimated values of active and reactive power.

**The Virtual Flux Based Control (VF-)** correspond to a direct analogy of IM control.
2.3.2 Direct Power Control and Virtual Flux Direct Power Control

The DPC method is similar to Direct Torque Control (DTC) for induction motor. Instead of torque and stator flux the instantaneous active and reactive powers are controlled. The following figure shows the scheme of the DPC method.

![Figure 2.9: Block scheme (DPC, VF-DPC)[9]](image)

The power estimation of DPC is based on the line voltage. An important disadvantages of the method is the need of current differentiation to estimate this power. Other relevant points can be found ([9]):
- Need high sample frequency because the estimated value are changing all the time.
- Need high inductance value because the switching frequency is not constant.
- A non-constant switching frequency means trouble to design an input filter.
- Calculation of power and voltage should be avoid during switching (errors).

The virtual flux method is an improvement of Voltage Oriented Control (VOC). The virtual flux is an integration of line voltage $u_L$.

For the VF-DPC, we can summaries the following characteristics.
- No line voltage sensors required. Furthermore, a voltage sensor-less line power estimation is much less noisy due to natural low-pass behavior of the integrator.
- Simple and noise robust power estimation algorithm, easy to implement in a DSP.
- Lower sampling frequency (as conventional DPC).
- Sinusoidal line currents (low THD).
- No separate PWM voltage modulation block.
- No current regulation loops.
- Coordinate transformation and PI controllers not required.
- High dynamic, decoupled active and reactive power control.
- Power and voltage estimation gives the possibility to obtain instantaneous variables with all harmonic components, which has an influence for improvement of total power factor and efficiency.
- Easier calculations for $p$ and $q$ than voltage based method, no differentiation of line current.

The typical disadvantages of VF-DPC are:
- Variable switching frequency.
2.3.3 Voltage and Virtual Flux Oriented Control

The Voltage Oriented Control (VOC) and Virtual Flux Oriented Control (VFOC) are close to Field Oriented Control for induction motor. The method is based on the transformation between stationary coordinates \( \alpha \beta \) and synchronous rotating coordinates \( dq \). This strategy guarantees:
- Fast transient response
- High static performance via internal current control loop.
Consequently, the performance depends on the quality of the current control loop.

We can find several strategies that can be applied for current control. A widely used scheme for high performance current control is the \( dq \) synchronous controller, where the regulated current are DC quantities. This eliminates steady-state errors.

VOC and VFOC provide some advantages compared to DPC.
- Low sampling frequency for good performance (cheaper A/D converters and microcontroller)
- Fixed switching frequency (easier design of input filter)

Furthermore, VFOC provides improved rectifier control under non-ideal line voltage condition (because ac voltage sensorless operation is much less noisy thanks to the natural low-pass behavior of the integrator used in the flux estimator).

Both methods also have some disadvantages:
- Coupling occurs between active and reactive components and some decoupling solution is required.
- Coordinate transformation and PI controllers are required.
2.3.4 Comparison and discussion

The following table summarizes the main characteristics of the different control strategies.

<table>
<thead>
<tr>
<th>TECHNIQUE</th>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
</table>
| VOC       | • Fixed switching Freq. (easier design input filter)  
• Advanced PWM strategies can be used  
• Cheap A/D converters | • Coordinate transformation and decoupling between active and reactive components is required  
• Complex algorithm  
• Input power factor lower than for DPC |
| DPC       | • No separate PWM block  
• No current regulation loop  
• No coordinate transformation  
• Good dynamics  
• Simple algorithm  
• Decoupled active and reactive power control  
• Instantaneous variables with all harmonics components estimated (improve power factor and efficiency) | • High inductance and sample frequency needed  
• Power and voltage estimation should be avoid at the moment of switching  
• Variable switching frequency  
• Fast microprocessor and A/D converters required |
| VFOC      | • Fixed switching Freq. (easier design input filter)  
• Advanced PWM strategies can be used  
• Cheap A/D converters | • Coordinate transformation and decoupling between active and reactive components is required  
• Complex algorithm  
• Input power factor lower than for VF-DPC |
| VF-DPC    | • Simple and noise resistant power estimation algorithm, easy to implement in a DSP  
• Lower sampling frequency than for DPC  
• Low THD of line currents with distorted or unbalanced supply  
• No separate PWM block  
• No current regulation loop  
• No coordinate transformation  
• Good dynamics  
• Simple algorithm  
• Decoupled active and reactive power control | • Variable switching frequency  
• Fast microprocessor and A/D converters required |

Table 2.3: Control strategies comparison [9]

VOC vs. VFOC
One of the only advantages of VFOC against VOC is that VFOC provides improved rectifier control under non-ideal line voltage condition (because ac voltage sensorless operation is much less noisy thanks to the natural low-pass behavior of the integrator used in the flux estimator).

Switching Frequency
A FIXED switching frequency is required in our project mainly because it means: easier design (input filter for eg.) and the sample frequency can be lower. Only VOC or VFOC can provide this feature.

Power factor
DPC has better power factor than VOC but has variable switching frequency. DPC also means complicated calculations for p and q (need differentiation of line current, risk of instability).
A good power factor can be achieved with VF-DPC and the method has lots of advantages but as we want a fixed switching frequency, VOC or VFOC should be chosen.
If the switching frequency can be variable, the VF-DPC strategy is obviously the best solution (but the cost can become a problem. The method need fast microprocessors and A/D converters).
2.4 Pulse Width Modulation

The Pulse Width Modulation used in our system, a sinusoidal PWM will be used.

2.4.1 Sinusoidal PWM

Sinusoidal modulation is based on a triangular carrier signal. The idea is to compare three sinusoidal reference voltages $U_a^*$, $U_b^*$ and $U_c^*$ to this triangular wave. By comparison, the logical signals $S_a$, $S_b$ and $S_c$, which define switching instants of power transistor, are generated. Operation with constant carrier signal concentrate voltage harmonics around switching frequency and multiple of switching frequency.

![Figure 2.11: Sinusoidal PWM](image)

![Figure 2.12: Sinusoidal PWM basic waveforms](image)

- **Maximum sinusoidal reference voltage**
  Using a sinusoidal PWM, the maximum reference value is $V_{dc}/2$.

![Figure 2.13: Maximum sinusoidal reference voltage (sinusoidal PWM)](image)

- **Maximum slope**
  The slope of the triangular wave should be higher than the slope of the reference voltage. We can write
\[
\frac{dU_{\text{triangle}}}{dt} > \frac{dU_{\text{reference}}}{dt}
\]

\[
(2.30)
\]

2.4.2 Digital implementation

\textbf{Synchronous sampling [4]}

In a digital current control system, the current is sampled with interval \( T_s \). To avoid electromagnetic interference (EMI) due to ON/OFF switchings of the valves, it is useful to synchronize the sampling with converter switching. Current sampling is taken in between switchings. This coincides with the positive and negative peak values of the triangular waveform.

Using synchronous sampling, approximately the mean value of the current is obtained. Thus, not only EMI is avoided, but also the current ripple is reduced. This method can be effective enough to avoid low-pass filtering before sampling.

We will select the sample frequency as:

\[
F_s = 2 F_{\text{triangle wave}} = 2 F_{SW}
\]

\[
(2.31)
\]

\( F_{SW} \) is the switching frequency, \( F_{\text{triangle wave}} = F_{SW} \)

\textbf{Figure 2.14 : Asymmetric PWM – Synchronous sampling illustration [23]}

Two samples can be acquired over each switching period. According to [4] a fast sampling enables higher bandwidth of the current controller, then it’s possible to reduce the sampling rate for example to the switching rate: \( F_s = F_{SW} \) (or less).

2.4.3 Dead time effect

When we speak about implementation of converter, we need to inject deadtime (delay) in PWM signals to avoid short circuit in DC-link (i.e. both transistor of one leg are conducting). The system becomes safer but, the performance are affected. This is temporary a loss of control. For example in an inverter, the output voltage waveform deviates from that for which it is originally intended. Since this is repeated over and over for every switching operation, its detrimental effect may become significant in PWM inverters that operate in high switching frequency. This is known as the deadtime effect. During the delay time, both transistors of the leg cease to conduct. Another consequence of the deadtime effect is the appearance of undesirable harmonics ([31] [32]).

We can find several strategies for deadtime injection. An example is given below.
Figure 2.15: One leg with transistors B1 and B2 – On/Off states, deadtime $T_d$ [32]
3 VOLTAGE ORIENTED CONTROL – SIMULATION

3.1 Introduction – References chosen

As we explain in the previous section, Voltage Oriented Control (VOC) or Virtual Flux Oriented Control (VFOC) should be chosen. We decided to start with a VOC.

Before going further in the design and simulation of the controller, we need to precise some important references chosen in this report.

3-PHASE SYSTEM DEFINITION

\[ u_a = E_m \cos(\omega t) \]
\[ u_b = E_m \cos\left(\omega t - \frac{2\pi}{3}\right) \]
\[ u_c = E_m \cos\left(\omega t - \frac{4\pi}{3}\right) \]

COORDINATE TRANSFORMATION

\[
\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix}
\]

(2.10)(2.11)

\[
\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} a \\ \beta \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix}
\]

(3.1)(3.2)

You can refer to APPENDIX A for details. We only use AMPLITUDE INVARIANT in this thesis. Indeed, after transformation from ABC-to-dq coordinates, the d-components is equal to \(E_m\), and the q-component equal to zero.

POWER, CURRENT DIRECTION

We chose a reference as shown in the following schematic, the current is flowing from the grid to the rectifier.

![Figure 3.1 Reference for I, P, Q](image)
3.2 System block diagram

The voltage oriented control scheme is shown Figure 3.2.

First of all, the line voltage $U_{abc}$ need to feed the PLL (Phase Locked Loop, see “3.7 Phase Locked Loop (PLL)”) and the voltage angle calculated is used for three-phase to dq-coordinate transformation of line current and voltage.

Secondly, the dq-coordinate values and the DC-link voltage value are used in a decoupled controller which will be described in the section “3.4 Current controller” and “3.5 DC-link voltage controller”.

Finally, the reference voltages created by the controller are sent to the PWM block (Pulse Width Modulation) to create the switching patterns $S_{abc}$ ($S=1$ means upper switch ON, lower switch OFF; $S=0$ means upper switch OFF, lower switch ON).

Remark: The reference voltage from the controller correspond to the converter voltage $U_s$ (see design of the current controller in section “3.4 Current controller”).

The system will be simulated in Matlab/Simulink. According to the previous figure, we will have four main parts in the model: the PLL, a decoupled controller composed by a current and voltage controller, a PWM block, and a rectifier model (with grid impedance R and L included).
3.3 PWM Simulation

A description of the sinusoidal PWM implemented here is available in section “2.4 Pulse Width Modulation”.

3.3.1 Simulink implementation of PWM

◮ PWM block using switch

The amplitude of triangular wave should be Vdc/2. But Vdc is not constant in our case. We should first normalized the reference value by Vdc/2 and compare this value with a triangular wave with an amplitude of 1. The following figure show the Simulink block diagram.

◮ PWM block without switch

We can also use a PWM block without switching to create the switching pattern. The reference voltage is normalized by Vdc/2 to obtain a signal within a range [-1 ; +1], then divide by 2 and translate to get signal in the range [0 ; +1] like the switching function $S_{abc}$. This simple model can be useful in Simulink to reduce the simulation time if needed. In a complete simulation with controller, the behavior of the system is similar using Figure 3.3 or Figure 3.4.
Synchronization verification

We have to check which carrier wave we should have (at t=0, triangle amplitude is 1 or 0?). We need to be sure that we sample every triangular wave peak (we need to check if at t=0, Matlab take a sample or not).

We can verify it by sampling the triangular wave, using a “sample and hold” block. The signals before and after sampling are plotted below. As we can see, we sample on each triangle peak (blue point).

\[ F_S = 2 F_{tri} \]
\[ T_S = T_{tri}/2 \]

Figure 3.5: Synchronization verification
3.4 Current controller

This section is mainly based on the reference [4] and [14]. We are giving a summary for controller design based on Internal Model Control (IMC) with synchronous PI control (decoupled controller).

To make the following more understandable, a first schematic for decoupled controller is given Figure 3.6 with the current controller and the dc-link voltage controller (describe in section “3.5 DC-link voltage controller”).

![Decoupled controller schematic](image)

**Figure 3.6**: Decoupled controller (current and dc-link voltage controller)

### 3.4.1 Internal Model Control

Internal Model Control (IMC) is a method for controller design, for which the resulting controller becomes directly parameterized in terms of the plant model parameters and the desired closed-loop bandwidth.

For example, the controller transfer function will be

$$F(s) = \frac{\alpha^n}{(s + \alpha)^n - \alpha^n \hat{G}^{-1}(s)} \quad (3.3)$$

that is, a low pass filter with bandwidth $\alpha$, $\hat{G}$ is an estimation of the plant (process), and $n$ the order or $G$.

A brief tutorial is available in [14], Chapter 6, page 83. This method is used for the following controller design.

### 3.4.2 Synchronous PI control

PI controllers are inherently incapable of giving zero steady state control error for a sinusoidal reference. The integral action removes the error only if the reference value is constant in steady state.

Using Clarke and Park transformations, the current measurements are transformed to DC-quantities, then, a simple PI controller can give good results (but not always optimal performances).

Main qualities for dq-frame current controller are then:
- fast dynamic response,
- good accuracy current tracking,
- less sensitive to parameter variations.

(Sources: [4] [9].)

### 3.4.3 Design of the synchronous PI controller

![Figure 3.7: Synchronous coordinates schematic (see APPENDIX A-A.5)](image)

**Synchronous coordinates equation** (notation, \( x = x_{dq} = x_d + jx_q \))

\[
L \frac{di}{dt} = E - (R + j\omega L)i - v \quad (3.4)
\]

\[
(R + sL + j\omega L)\dot{i} = E - v \quad \Rightarrow \quad i = \frac{E - v}{R + sL + j\omega L}
\]

And the system transfer function \( G(s) \) is

\[
G(s) = \frac{i}{v} = -\frac{1}{R + sL + j\omega L} \quad (3.5)
\]

![Figure 3.8: Current control with inner decoupling loop](image)

**Cross coupling cancellation**

The first step in the controller design is to cancel the cross coupling initiated by the term \( j\omega L \) (since multiplication by \( j \) maps the \( d \) axis on \( q \) axis and vice versa). This easily possible if we have an accurate estimation of \( L \) which is \( \hat{L} \).

According to [9], a PI current controller has no satisfactory tracing performance for the coupled system described by equations (2.17)(2.18). For high performance and accuracy current tracking we need to cancel this cross-coupling. We select \( v \) as

\[
v = -v' + \hat{E} - j\omega \hat{L}i \quad (3.6)
\]

with \( \hat{E} \) the estimated value of \( E \). Then, if \( \hat{L} = L \) and \( \hat{E} = E \) we get
\[
\dot{i} = \frac{v'}{R + sL} \Rightarrow G'(s) = \frac{i}{v'} = \frac{1}{R + sL} \tag{3.7}
\]

with \(G'(s)\) the decoupled system transfer function from \(v'\) to \(i\).

**Controller transfer function \(F(s)\)**

As the complex transfer function is a first order (representing two non-interacting first order system in the \(d\) and \(q\) directions), a PI controller is enough:

\[
F(s) = k_p + \frac{k_i}{s} \tag{3.8}
\]

Based on IMC method of [14], we can write

\[
F(s) = \frac{\alpha_i}{s} \hat{G}^{-1}(s) = \frac{\alpha_i}{s} (\hat{R} + s\hat{L}) = \alpha_i \hat{L} + \frac{\alpha_i \hat{R}}{s} \tag{3.9}
\]

with \(\alpha_i\) (rad/s) the current controller bandwidth where the pole of \(G'(s)\) is placed, and \(\hat{G}'(s)\) the estimation of \(G'(s)\). Finally, we obtain the PI coefficients:

\[
| k_p = \alpha_i \hat{L} \text{ and } k_i = \alpha_i \hat{R}. \tag{3.10} \tag{3.11} \]

For this inner current control loop, the bandwidth \(\alpha_i\) should be selected smaller than a decade below the sampling frequency (Fs [Hz]) [14].

\[
\alpha_i < 2\pi \frac{F_s}{10} \tag{3.12}
\]

**Decoupled current control design**

In order to establish the decoupled current control diagram, we have to continue with equation (3.6). We define \(\hat{L}\), complex integrator state variable as:

\[
\frac{d\hat{L}}{dt} = \varepsilon \tag{3.13}
\]

\[
\varepsilon = -v' + \hat{E} - j\omega \hat{L} i
\]

\[
\Rightarrow \varepsilon = \hat{E} - k_p \varepsilon - k_I \hat{I} - j\omega \hat{L} i
\]

\[
\Rightarrow \varepsilon = (\hat{E}d + j\hat{E}q) - k_p(\varepsilon d + j\varepsilon q) - k_I(1d + j1q) - j\omega \hat{L}(id + jq)
\]

Then, we can write the real and imaginary part to get our reference voltage and draw our current controller block diagram.
In our system, the line current $i_L$ is split into a q-component $i_{Lq}$ and a d-component $i_{Ld}$. $i_{Ld}$ determines the active power flow whereas $i_{Lq}$ the reactive power. The unit power factor (UPF) condition is met when the line current vector $i_L$ is aligned with line voltage $u_L$. In this case, we have to set $i_{Lq}$ to zero in our controller ($i_q^* = 0$).

Furthermore, we can write down the equation for power and see that the reactive power is set to zero. From the power equations established in section “2.2.2 Mathematical model” we can write

\begin{align}
P &= \frac{3}{2} \text{Re}\{v^{dq} (i^{dq})^*\} = \frac{3}{2} (v_d i_d + v_q i_q) = \frac{3}{2} (E_d i_d + E_q i_q) \tag{3.16} \\
Q &= \frac{3}{2} \text{Im}\{v^{dq} (i^{dq})^*\} = \frac{3}{2} (v_q i_d - v_d i_q) = \frac{3}{2} (E_q i_d - E_d i_q) \tag{3.17}
\end{align}

Now if we set the reference $i_q$ to zero and we know that the line voltage vector is aligned with the d-axis, so $E q = 0 V$. Finally, we get

\begin{align}
P &= \frac{3}{2} E_d i_d \tag{3.18} \\
Q &= 0
\end{align}

### 3.4.4 Active damping, voltage saturation, anti-windup

**Active damping**

As it’s fully explained in [4] (section 1.4–p24), the current control error $\varepsilon$ could be decrease be increasing $R$. Therefore, we can add a inner feedback loop which add $Ra$ (just using signal, there is no energy transfer or more losses). This method improve disturbance rejection capability because
the dynamics are speeded up from \( L/R \) to \( L/(R+Ra) \). Active damping is also used when R and L value are not estimated precisely.

This active damping is not implemented in this thesis.

**REFERENCE VOLTAGE SATURATION**

We have treated the current control loop as an ideal and linear system. In practice, this is not correct because the reference voltage is limited to an upper and lower value. For large step of the \( d \)-current, the controller might demand a large voltage vector (outside the switching hexagon that defines the switching possibilities). This exceeds the realizable voltage modulus of a PWM converter ([4][14]).

The saturation is applied on the modulus of the complex value of the reference voltage
\[
\nu = v_d + j v_q,
\]
that is, \( |\nu| = \sqrt{v_d^2 + v_q^2} \).
The saturation value depends on the DC-link voltage. The maximum value of reference voltage is \( V_{\text{max}} = V_{\text{dc}}/2 \).

The simplest method to create the saturation \([V_{\text{dc}}/2 ; -V_{\text{dc}}/2]\) in Simulink is to normalized the modulus of reference voltage by \( V_{\text{dc}}/2 \) before the saturation block. Then, the saturation block is the set to \([1 ; -1]\) (it means a saturation between \( V_{\text{dc}}/2 \) and \(-V_{\text{dc}}/2\)). Finally, we multiply back the output of the saturation block by \( V_{\text{dc}}/2 \).

![Reference voltage saturation – Simulink implementation](image)

**INTEGRATOR ANTI-WINDUP**

**Principle**

As we said in the previous section, for large step of the \( d \)-current, the controller might demand a too large voltage vector (outside the switching hexagon). This exceeds the realizable voltage modulus of a PWM converter ([14]).

We call \( \nu \) the reference voltage. The PI controller is:

\[
\frac{dl(t)}{dt} = \varepsilon \\
\nu(t) = k_p \varepsilon(t) + k_i I(t)
\]

Once \( \nu \) become limited (\( \bar{\nu} \)), the integrator part of the PI controller can introduce a phenomenon called integrator windup. An integrator windup generally manifest itself by an overshoot (to the step response). In order to avoid windup, the integrator part \( I \) should not be updated with too large error \( \varepsilon \). We should feed the integrator with another error \( \bar{\varepsilon} \), so that \( \nu = \bar{\nu} \).

\[
\bar{\nu}(t) = k_p \bar{\varepsilon}(t) + k_i I(t)
\]
Then, writing the difference $\bar{v} - v$ we can obtain

$$\bar{e} = e + \frac{\bar{v} - v}{k_p}$$

The following controller results:

$$\frac{dl(t)}{dt} = \bar{e}$$
$$v(t) = k_p e(t) + k_i l(t)$$
$$\bar{v} = [v]_{max}^{min}$$

(source: [4] [14])

In our case...
For the decoupled controller, the following equation have been found:

$$v^*_{dq} = \hat{E}_{dq} - k_p e_{dq} - k_i l_{dq} - j\omega \hat{L}i_d + \omega \hat{L}i_q.$$  

Now we call $\bar{v}$ the value of $v^*_{dq}$ after saturation, we can write:

$$\bar{v} = \hat{E}_{dq} - k_p \bar{e}_{dq} - k_i l_{dq} - j\omega \hat{L}i_d + \omega \hat{L}i_q$$

By writing the difference $v^*_{dq} - \bar{v}$, we can find $\bar{e}_{dq}$:

$$\bar{e}_{dq} = e_{dq} + \frac{v^*_{dq} - \bar{v}}{k_p}$$  \hspace{1cm} (3.19)

The PI current controller will be created as follow.

**Figure 3.12**: PI controller with anti-windup

3.4.5 Current controller simulation

**BLOCK DIAGRAM**

The simulation have been done following the following equations (equation (2.8) of section “2.2.2 Mathematical model”):

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{di}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix}$$

For each phase we know that the current is equal to

$$i = \frac{u - u_s}{R + sL}$$

Also, we can draw the following diagram block (Figure 3.13).
- $i_d^*$ will be chosen;
- $U_a \; U_b \; U_c$ are line voltage;
- $E_d \; E_q$ are the dq-transformation of $U_a \; U_b$.

**Remark**: The tests can also be simulated in dq but we’ve decided to stay in ABC-frame to model the rectifier and the grid impedance to be as close as possible to the real system.

### Simulation

The system have been simulated in continuous and discrete (only the continuous simulation is shown here). No saturation or anti-windup are present in this simulation. They will be added later.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$ (Ω)</td>
<td>0.1</td>
</tr>
<tr>
<td>$L$ (H)</td>
<td>5e-3</td>
</tr>
<tr>
<td>$\omega$ (rad/s)</td>
<td>$2\pi 50$</td>
</tr>
<tr>
<td>$E_m$ (V), ph-to-gnd amplitude ($=E_d$)</td>
<td>$115\sqrt{2}$</td>
</tr>
<tr>
<td>$I_d^*$ (A)</td>
<td>3</td>
</tr>
<tr>
<td>$I_d^*$ step (A) at 0.025s</td>
<td>3</td>
</tr>
<tr>
<td>$I_q^*$ (A)</td>
<td>0</td>
</tr>
<tr>
<td>$F_{sw}$ (kHz), switching frequency</td>
<td>20</td>
</tr>
<tr>
<td>$\alpha_i = 2\pi \frac{F_{sw}}{10}$ (rad/s)</td>
<td>$1.26e4$</td>
</tr>
<tr>
<td>PI controller, $K_p$</td>
<td>62.8</td>
</tr>
<tr>
<td>PI controller, $K_i$</td>
<td>$1.26e3$</td>
</tr>
</tbody>
</table>

**Table 3.1**: Current controller simulation parameters

- The bandwidth of the current controller have been selected at: $\frac{F_{sw}}{10} = 2 \text{ kHz}$ (we chose to take a decade smaller than the switching frequency).
- $\hat{L}$ is selected equal to $L$.
- The Simulink block diagram is available in APPENDIX B-B.1, Figure 0.7. We also advice to read the simulation of coordinate transformation in APPENDIX A-A.4 before.
Remark: The value of iq is zero when a zoom is done (even if a q-current is visible in the previous figure).

Figure 3.14: Current control simulation
3.5 DC-link voltage controller

3.5.1 DC-link model and linearization

DC-LINK MODEL

The DC-link voltage is modeled as a pure capacitor. This capacitor is an energy storage where the stored electrical energy in Joule is

\[ E_c = \frac{1}{2} C \cdot v_{dc}^2 . \]  

(3.20)

The time derivative of this stored energy should be equal to the sum of instantaneous grid power and load power [14].

\[ \frac{1}{2} C \frac{d v_{dc}^2}{dt} = P_g - P_{load} \]  

(3.21)

As we can see, the previous equation is not linear with respect to Vdc.

LINEARIZATION

The design of the voltage controller is facilitated thanks a feedback linearization. The feedback linearization transforms the nonlinear dc-voltage dynamics to a equivalent linear system, on which traditional linear controller design can be applied.

We now choose a new state variable \( W \).

\[ W = v_{dc}^2 \]  

(3.22)

Then, equation (3.21) becomes

\[ \frac{1}{2} C \frac{dW}{dt} = P_g - P_{load} \]  

(3.23)

which is linear with respect to \( W \). The physical interpretation is that the energy is chosen to represent the dc-link voltage dynamics instead of the voltage itself. Other type of linearization can be found [14].

3.5.2 Design of voltage controller

System transfer function

Following [14] and the Internal Model Control method, we can write

\[ \frac{1}{2} C \frac{dW}{dt} = P_g - P_{load} \]  

\[ P_g = \frac{3}{2} E_g i_d \]  

(3.18)

\[ P_{load} = \frac{v_{dc}^2}{R_{load}} = \frac{W}{R_{load}} \]  

(3.24)

where \( i_d \) is the d-current, and the grid voltage \( E_g = E_d \). The coefficient \( \frac{3}{2} \) comes from the amplitude invariant transformation (see section “2.2.2 Mathematical model” about power calculation).

\[ \frac{1}{2} C \frac{dW}{dt} = \frac{3}{2} E_g i_d - P_{load} \]  

(3.25)
\begin{align*}
\mathcal{L} & \Rightarrow \frac{1}{2} CsW = \frac{3}{2} E_g id - P_{load} \\
\Rightarrow CsW & = 3E_g id - 2P_{load} \\
\Rightarrow W & = \frac{3E_g}{sC} id - \frac{2}{sC} P_{load}
\end{align*}

Then, the system transfer function \( G(s) \) is
\[
G(s) = \frac{W}{id} = \frac{3E_g}{sC}
\]

\[\text{(3.26)}\]

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{voltage_control_loop.png}
\caption{Voltage control loop}
\end{figure}

**Controller transfer function**
\[
F(s) = \frac{\alpha_v}{s} \tilde{G}^{-1}(s) = \frac{\alpha_v \tilde{C}}{3E_g}
\]

where \( \tilde{G}(s) \) is the estimation of \( G(s) \) and \( \alpha_v \) (rad/s) is the bandwidth of the voltage controller. Then, \( F(s) \) give us a proportional coefficient \( KP_v \):
\[
KP_v = \frac{\alpha_v \tilde{C}}{3E_g} = \frac{\alpha_v \tilde{C}}{3E_m}
\]

\[\text{(3.28)}\]

with \( \tilde{E}_g = \tilde{E}_d = \tilde{E}_m \) (\( E_m \) is the amplitude of the three-phase input voltage in the model section “2.2.2 Mathematical model”)

We will choose \( \alpha_v \) at least a decade smaller than the current control bandwidth.

\[
\alpha_v < \frac{\alpha_i}{10}
\]

\[\text{(3.29)}\]

As we can see there is no integrator part in the controller. In our controller, we will add a small integrator part with gain \( Ki_v \) (for example \( Ki_v = 0.01 \)).

**3.5.3 Voltage saturation, anti-windup, active damping**

**SATURATION, ANTI-WINDUP**

Exactly as the current controller, we have to add a saturation (on current \( id^* \)) and an anti-windup is highly recommended (useful is the saturation limit is reached).

In this case we can write :
\[
id^* = k_p \epsilon + k_i I
\]
with \( I = \frac{\varepsilon}{p} \). If we do the same calculation than the current controller case, we can find:

\[
\dot{\varepsilon} = \varepsilon + \frac{id - id^*}{k_p}
\]  

(3.30)

Then, the PI voltage controller scheme will be as below.

![Figure 3.17: PI controller with anti-windup](image)

**ACTIVE DAMPING**

Previously, we found a system transfer function \( G(s) \) (equation (3.26)) as

\[
G(s) = \frac{W}{id} = \frac{3E_g}{sC}
\]

which has a pole at the origin. [14] advice to add an active damping in this case, to place the pole at \(-\alpha_p\), with \( \alpha_p \) the bandwidth of the voltage controller.

**System transfer function**

Based on [14], we can find the following equations and block diagram (Figure 3.18). We can start again with equation (3.25):

\[
\frac{1}{2} C \frac{dW}{dt} = \frac{3}{2} E_g id - P_{load}
\]  

(3.25)

We chose to define \( id \) with

\[
id = id' - GaW
\]

(3.31)

where \( Ga \) is the active conductance that provides active damping. Then, by substituting equation (3.31) into (3.25), the system model becomes

\[
\frac{1}{2} C \frac{dW}{dt} = \frac{3}{2} E_g id' - \frac{3}{2} E_g GaW - P_{load}
\]  

(3.32)

The system transfer function becomes

\[
G'(s) = \frac{W}{id'} = \frac{3E_g}{sC + 3E_g Ga}
\]

(3.33)

As we can see, we still have a first order system but the pole can be chosen with \( Ga \). Placing the pole at \(-\alpha_p\) we can find \( Ga \) as

\[
sC + 3E_g Ga = 0 \leftrightarrow (-\alpha_p)C + 3E_g Ga = 0
\]

\[
Ga = \frac{\alpha_p C}{3E_g}
\]

(3.34)
Controller transfer function

Following the previous IMC method, we obtain

\[
F(s) = \frac{\alpha_v}{s} \hat{G}^{-1}(s) = \frac{\alpha_v \hat{C}}{3E_g} + \frac{\alpha_v Ga}{s}
\]

\[F(s) = \frac{\alpha_v \hat{C}}{3E_g} = \frac{\alpha_v \hat{C}}{3E_m}\]

\[K_p = \frac{\alpha_v \hat{C}}{3E_g} = \frac{\alpha_v \hat{C}}{3E_m}\]

\[K_i = \alpha_v Ga = \frac{\alpha_v^2 C}{3E_m}\]

(3.28)

(3.35)

(3.36)

with \(E_g = E_d = E_m\).

3.5.4 Voltage controller simulation

The system represented in Figure 3.19 is first simulated without saturation, then with saturation, and finally, an anti-windup is added. The simulation parameters and Simulink scheme are presented below.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C (μF)</td>
<td>2200</td>
</tr>
<tr>
<td>(\omega) (rad/s)</td>
<td>2\pi50</td>
</tr>
<tr>
<td>(E_m) (V), ph-to-gnd amplitude (=Ed)</td>
<td>115\sqrt{2}</td>
</tr>
<tr>
<td>(F_{SW}) (kHz), switching frequency</td>
<td>20</td>
</tr>
<tr>
<td>(\alpha_v = 2\pi F_{SW}/100) (rad/s)</td>
<td>1.26e3</td>
</tr>
<tr>
<td>PI controller, (K_p)</td>
<td>0.0057</td>
</tr>
<tr>
<td>PI controller, (K_i)</td>
<td>0.01</td>
</tr>
<tr>
<td>Vdc reference (V)</td>
<td>400</td>
</tr>
<tr>
<td>(R_{load}) (Ω)</td>
<td>500</td>
</tr>
</tbody>
</table>

Table 3.2: Voltage controller simulation
Figure 3.19: Voltage controller – Simulink block scheme

Figure 3.20: Voltage control – Without saturation
We can see a fast response, a small error close to zero (0.0001V at 2 seconds). But, we observe a very high current about 800A. We need to add the saturation here.

With saturation

The error has been increased lightly (Error 0.06V with Rload = 5000, Error 0.1V with Rload = 500). We observe that the error depends on the saturation upper and lower value and depends also on the load.

As the current is now limited the response is much slower. Finally, we also observe the so called integrator windup due to the saturation.
With saturation and anti-windup (Figure 3.22)
We now include the back calculation anti-windup and as we can see, the overshoot disappeared. The error is also reduced.

With saturation, anti-windup and active damping (APPENDIX B-B.2, Figure 0.8, Table 0.1)
In this simulation, the active damping doesn’t influence the system.

3.5.5 Simulation with current controller
The whole system can now be simulated. The rectifier is modeled according to the following Simulink scheme (Figure 3.23 and Figure 3.24) and data (Table 3.3)

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>R (Ω)</td>
<td>0.1</td>
</tr>
<tr>
<td>L (H)</td>
<td>5e-3</td>
</tr>
<tr>
<td>C (μF)</td>
<td>2200</td>
</tr>
<tr>
<td>ω (rad/s)</td>
<td>2π50</td>
</tr>
<tr>
<td>Em (V), ph-to-gnd amplitude (=Ed)</td>
<td>115√2</td>
</tr>
<tr>
<td>Fsw (kHz), switching frequency</td>
<td>20</td>
</tr>
<tr>
<td>Rload (Ω)</td>
<td>500</td>
</tr>
<tr>
<td>Vdc reference (V)</td>
<td>400</td>
</tr>
<tr>
<td>( α_l = \frac{2π F_{SW}}{10} (\text{rad/s}) )</td>
<td>1.26e4</td>
</tr>
<tr>
<td>( α_v = \frac{2π F_{SW}}{100} (\text{rad/s}) )</td>
<td>1.26e3</td>
</tr>
<tr>
<td>V controller, Kpv</td>
<td>0.0057</td>
</tr>
<tr>
<td>V controller, Kiv</td>
<td>0.01</td>
</tr>
<tr>
<td>I controller, Kpi</td>
<td>62.8</td>
</tr>
<tr>
<td>I controller, Kii</td>
<td>1.26e3</td>
</tr>
<tr>
<td>I saturation (A)</td>
<td>±15</td>
</tr>
<tr>
<td>Vdc step at 0.03 (V)</td>
<td>50</td>
</tr>
</tbody>
</table>

Table 3.3: Current and voltage controller simulation parameters
In the previous figure, the signals \( u_{abc\_ref} \) come from the controller (after dq-to-abc transformation).

**Figure 3.23**: Simulink block scheme – Grid impedance and dc-link model

**Figure 3.24**: Simulink block scheme – Controller
In the Figure 3.25, we observe a very high current when the system start (id reaches 70A), and we can see also a small overshoot on Vdc. This is due to the capacitor charging. Now we apply a small step on Vdc reference (50V), and we can see that the d-current reaches the saturation limit (15A) when Vdc is increasing towards the reference value (450V). Finally, when Vdc reaches the reference value (without overshoot), the current is stabilize around 1.3A (steady state value).

**DISCRETE SIMULATION**

All the previous design and simulation have also been implemented in discrete time since the controller will be discrete in reality. You can find a discrete simulation of the controller (same scheme as Figure 3.24) in APPENDIX D.
3.5.6 Controller improvements

**FILTERS**

\[
\mathbf{E}_{dq} \text{ represent the line voltage (grid, or } V_{PCC} \text{) and } V_{dq} \text{ the converter voltage. We received a piece of advice regarding the feed-forward term } \mathbf{E}_{dq} \text{ in the controller Figure 3.26. This feed-forward could turn the system unstable if some high frequency oscillations appear on } \mathbf{E}_{dq}. \\
\text{To remove any high frequency oscillations, we decided to add a filter for each feed-forward. We chose a first order discrete filter with a bandwidth a decade lower than the current control bandwidth:} \\
\alpha_{filter} = \frac{\alpha_i}{10} \quad (3.37)
\]

If the grid is stiff enough, the bandwidth of the filter can be equal to the current controller bandwidth.

**INTEGRATORS**

We can see in the previous scheme that two integrator are in cascade, an integrator in the voltage controller and one in the current controller. The current controller integrator can probably be removed (then, the anti-windup also).

**LOAD COMPENSATION**

In the papers [11], a load compensation has been proposed to minimized the influence of rapid changes of the converter load. The feed-forward information (see schematic on Figure 3.27) about the actual converter load has also contributed to improve the transient response of the DC-link voltage. This compensation is not implemented in this report.
Figure 3.27: Improvement proposed in [11]
3.6 Stability analysis

We decided to do a small stability analysis with the current controller only, voltage controller, then both voltage and current controller together. Furthermore, the analysis is done for three different voltage controller. First, only a proportional controller is taking in account ($K_{p_v}$). In a second time, the integration part is added ($K_{i_v} = 0.01$). And finally, the active damping coefficient $Ga$ is added.

3.6.1 Current controller

If the cross coupling cancellation is ideal, that is, $\hat{L} = L$, we saw in section “3.4.3 Design of the synchronous Pi controller” (and see Figure 3.8) that the system transfer function becomes

$$G'(s) = \frac{1}{R + sL} \quad (3.7)$$

If we see $\hat{E}$ as a disturbance that we neglect, we obtain the following diagram

![Figure 3.28: stability analysis of current control](image)

Now, following the IMC, we saw that the controller is calculated with

$$F(s) = \frac{\alpha_i}{s} G'^{-1}(s) = \frac{\alpha_i}{s} (\hat{R} + s\hat{L})$$

The open- and closed-loop transfer function are noted respectively $L_i(s)$ and $S_i(s)$

$$L_i(s) = F(s)G'(s) \quad (3.38)$$

$$S_i(s) = \frac{L_i(s)}{1 + L_i(s)} \quad (3.39)$$

Furthermore, if $\hat{L} = L$ and $\hat{R} = R$, we can obtain the open- and closed-loop transfer function

$$L_i(s) = \frac{\alpha_i}{s} \quad (3.40)$$

$$S_i(s) = \frac{s}{s + \alpha_i} \quad (3.41)$$

$S_i(s)$ is a first order system, low pass filter, with a cut-off frequency $\alpha_i$ rad/s.
There is only one pole for $S_i(s)$ and it’s located at $-\alpha_i$ (negative Real part of the Imaginary domain means stability).

3.6.2 Voltage controller

PROPORTIONAL CONTROL ONLY

We consider again the Figure 3.16 without load disturbance $P_{load}$ and we obtain the following diagram. The system transfer function is (equation (3.26))
The open- and closed-loop transfer function are noted respectively \( L_v(s) \) and \( S_v(s) \).

\[
L_v(s) = \frac{\alpha_v}{s} \quad (3.42)
\]

\[
S_v(s) = \frac{\alpha_v}{s + \alpha_v} \quad (3.43)
\]

As the previous case, if \( \hat{C} = C \) and \( \hat{E}_g = E_g \), \( S_v(s) \) is a first order system, low pass filter, with a cut-off frequency \( \alpha_v \) rad/s.

There is only one pole for \( S_v(s) \) and it’s located at \( -\alpha_v \) (negative Real part of the Imaginary domain means stability).

**PROPORTIONAL AND INTEGRAL CONTROL**

As we explain during the voltage controller design, we decided to add a small integration constant.

The open- and closed-loop transfer function are noted respectively \( L_v(s) \) and \( S_v(s) \).

\[
L_v(s) = F(s)G(s) = \left( Kp_v + \frac{K_i_v}{s} \right) \frac{3E_g}{sC} = \left( \frac{\alpha_v}{3\hat{E}_g} + \frac{K_i_v}{s} \right) \frac{3E_g}{sC} = \frac{\alpha_vCs + 3E_gK_i_v}{Cs^2} \quad (3.44)
\]

\[
S_v(s) = \frac{L_v(s)}{1 + L_v(s)} = \frac{\alpha_vCs + 3E_gK_i_v}{Cs^2 + \alpha_vCs + 3E_gK_i_v} \quad (3.45)
\]

**WITH ACTIVE DAMPING GA**

In this case, we consider the following diagram.

\[
L_v(s) = F(s)G(s) = \left( Kp_v + \frac{K_i_v}{s} \right) \frac{3E_g}{sC + 3E_gGa} = \frac{\alpha_vCs + \alpha_v^2C}{Cs^2 + 3E_gGa s} \quad (3.46)
\]

\[
S_v(s) = \frac{L_v(s)}{1 + L_v(s)} = \frac{\alpha_vCs + \alpha_v^2C}{Cs^2 + \left( 3E_gGa + \alpha_vC \right)s + \alpha_v^2C} \quad (3.47)
\]

### 3.6.3 Complete controller

To study the complete controller, we consider the following diagram.
We can now write the open- and closed-loop transfer function $L_{vi}(s)$ and $S_{vi}(s)$:

$$L_{vi}(s) = F(s)S_i(s)G(s) = L_v(s)S_i(s)$$  \hspace{1cm} (3.48)

$$S_{vi}(s) = \frac{L_{vi}(s)}{1 + L_{vi}(s)}$$  \hspace{1cm} (3.49)

The following table sum-up the different transfer functions of the controller.

<table>
<thead>
<tr>
<th>$S_i(s)$</th>
<th>$L_v(s)$</th>
<th>$S_v(s)$</th>
<th>$L_{vi}(s)$</th>
<th>$S_{vi}(s)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha_i$</td>
<td>$\frac{\alpha_v}{s}$</td>
<td>$\alpha_iCs + \frac{3E_gK_i}{Cs^2}$</td>
<td>$\frac{\alpha_vCs + \alpha_i^2C}{Cs^2 + 3E_gGa s}$</td>
<td>$\frac{\alpha_vCs + \alpha_i^2C}{Cs^2 + (3E_gGa + \alpha_iC)s + \alpha_i^2C}$</td>
</tr>
</tbody>
</table>

Table 3.4: Transfer functions

### 3.6.4 Nyquist and Bode diagram

We can now plot the Nyquist and bode diagram for the complete controller. The Nyquist diagram should be plot for the open-loop transfer function $L_{vi}(s)$. Bode plot are given for the closed-loop transfer function $S_{vi}(s)$.

The following table shows the data used for Matlab script.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$ (Ω)</td>
<td>0.05</td>
</tr>
<tr>
<td>$L$ (H)</td>
<td>3e-3</td>
</tr>
<tr>
<td>$C$ (μF)</td>
<td>2200</td>
</tr>
<tr>
<td>$\omega$ (rad/s)</td>
<td>2π50</td>
</tr>
<tr>
<td>$E_m$ (V), ph-to-gnd amplitude (=Ed)</td>
<td>$115\sqrt{2}$</td>
</tr>
<tr>
<td>$F_{sw}$ (kHz), switching frequency</td>
<td>10</td>
</tr>
<tr>
<td>$R_{load}$ (Ω)</td>
<td>500</td>
</tr>
<tr>
<td>$\alpha_i = \frac{2\pi F_{sw}}{10}$ (rad/s)</td>
<td>$6.283e+003$</td>
</tr>
</tbody>
</table>
PROPORTIONAL CONTROL ONLY

<table>
<thead>
<tr>
<th>PARAM.</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kvp</td>
<td>0.0028</td>
</tr>
<tr>
<td>Kiv</td>
<td>0</td>
</tr>
<tr>
<td>Kpi</td>
<td>18.8496</td>
</tr>
<tr>
<td>Kii</td>
<td>314.1593</td>
</tr>
<tr>
<td>Ga</td>
<td>0</td>
</tr>
<tr>
<td>Pole1</td>
<td>-5575.1</td>
</tr>
<tr>
<td>Pole2</td>
<td>-708.1</td>
</tr>
</tbody>
</table>

*Table 3.5: Calculation data*

**Figure 3.32**: P control – Nyquist plot of open-loop \( L_{vi}(s) \)

**Figure 3.33**: P control – Bode plot of closed-loop \( S_{vi}(s) \)
PROPORTIONAL AND INTEGRAL CONTROL

PARAM. VALUE
Kpv 0.0028
Kiv 0.01
Kpi 18.8496
Kii 314.1593
Ga 0
Pole1 -5575.6
Pole2 -704.1
Pole3 -3.5

Figure 3.34: PI control – Nyquist plot of open-loop $L_{vi}(s)$

Figure 3.35: PI control – Bode plot of closed-loop $S_{vi}(s)$
WITH ACTIVE DAMPING GA

<table>
<thead>
<tr>
<th>PARAM.</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kpv</td>
<td>0.0028</td>
</tr>
<tr>
<td>Kiv</td>
<td>1.7801</td>
</tr>
<tr>
<td>Kpi</td>
<td>18.8496</td>
</tr>
<tr>
<td>Kii</td>
<td>314.1593</td>
</tr>
<tr>
<td>Ga</td>
<td>0.0028</td>
</tr>
<tr>
<td>Pole1</td>
<td>-5575.1</td>
</tr>
<tr>
<td>Pole2</td>
<td>-708.1</td>
</tr>
<tr>
<td>Pole3</td>
<td>-628.3</td>
</tr>
</tbody>
</table>

Figure 3.36: PI Ga control – Nyquist plot of open-loop $L_{vi}(s)$

Figure 3.37: PI Ga control – Bode plot of closed-loop $S_{vi}(s)$

3.6.5 Conclusion

All the previous Nyquist plot show stability, the blue curve is far enough from the point “-1”. The phase margins are about 84deg (a good phase margin is higher than 60deg). The Gain margin
are also good in our cases (infinite). Nevertheless, we feel that the delay margin is really too small compared to the system time constant.

ATTENTION, this analysis is probably too simplistic. We assumed that the converter and grid parameters are perfectly known and it’s not correct in reality. The cross coupling cannot be perfectly cancelled and the estimated values are not exactly equal to the real values, that is: \( \hat{C} \neq C \), \( \hat{E}_g \neq E_g \), \( \hat{L} \neq L \), \( \hat{R} \neq R \).

Another important point is that the analysis have been done in continuous time and should be also done in discrete time in order to be close to the real system (discrete controller).

More Nyquist and Bode graph are plotted in APPENDIX E.
3.7 Phase Locked Loop (PLL)

The PLL is an important and critical part of the system. Its aim is to give the voltage angle of the three-phase system (Ua Ub Uc Figure 2.4). This angle is then used for all the dq-transformations in the model.

3.7.1 Design

The PLL was design according ([4] [14]).

\[
\dot{\omega} = \gamma_1 \varepsilon \\
\dot{\theta} = \omega + \gamma_2 \varepsilon
\]

(3.50) (3.51)

where \(\gamma_1\) and \(\gamma_2\) are gain parameters and \(\varepsilon\) the error signal (\(\gamma_1\) is the Ki, and \(\gamma_2\) is the Kp of a PI controller). The main difference is that in our case, with d-oriented control, the error signal is selected as:

\[\varepsilon = \hat{E}q\] instead of \[\varepsilon = -\hat{E}d\] (chosen for flux oriented control).

Following the analysis of the thesis (or compendium), we can find the following PI parameters and the following scheme:

\[\gamma_1 = \frac{\rho^2}{\hat{E}_g}, \quad \gamma_2 = \frac{2\rho}{\hat{E}_g}, \quad \hat{E}_g = \sqrt{\hat{E}_{d}^2 + \hat{E}_{q}^2}\]

(3.52) (3.53) (3.54)

where \(\rho\) can be seen as the bandwidth of the PLL (rad/s), and \(\hat{E}_g\) is the estimated “grid” voltage modulus.

Figure 3.38: PLL scheme

Comments:

- The PI coefficients can be fixed or calculated in Simulink according to the estimated value (or measured value) \(\hat{E}_g = \sqrt{\hat{E}_{d}^2 + \hat{E}_{q}^2}\).
- The reference value (\(\omega_{ref} = 2.\pi.50\) rad/s) can be also included as a initial condition in the PI controller integrator.
- The first selection of the PLL bandwidth is about 20Hz. It will be adjust later.

3.7.2 Simulations

The model was implemented in continuous first, then in discrete using the following scheme for a discrete integrator:
The sample frequency is chosen as: \( F_s = 2 \cdot F_{SW} = 2 \cdot F_{\text{triangular wave}} \) (\( F_{sw} \) is the switching frequency, 20kHz).

**Simulation1: Balanced 3-phase system**

The results show that the original angle and the angle from the PLL are equal (angular frequency is also the same, 314.1593rad/s).
Figure 3.41: Simulation-Balanced 3-phase system
Simulation 2: Unbalanced 3-phase system

Now we create a voltage dip on phase C at 0.025s (30% dip, 70% of the voltage left).

Figure 3.42: Simulation-Unbalanced 3-phase system

Now an oscillation is produced and we can see a small oscillation on theta_pll too.

Simulation 3: Balanced 3-phase system, noise

We comeback to a balanced grid and we add noise to the 3-phase voltages (random noise for A, square wave for B, sawtooth wave for C, at different frequencies). We can see on the simulation below that the angles are similar (a small error about 0.03deg can be seen with a zoom).

<table>
<thead>
<tr>
<th>Noise phase A</th>
<th>Noise phase B</th>
<th>Noise phase C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random wave form</td>
<td>square wave</td>
<td>sawtooth wave</td>
</tr>
<tr>
<td>At different frequencies: 100, 150, 200, 250, 1000, 5000, 10000Hz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.6: Noise parameters
Remark and conclusion

We saw that the coefficients $\gamma_1$ and $\gamma_2$ can be calculated in Simulink according to $E_g$. Nevertheless, this can create a simulation issue at beginning of the simulation. We assume that for a first implementation and a stiff grid, fixed coefficients can be easily used. Another solution could be to start with fixed coefficients then switch to variable values.

To remove the oscillations on theta, we advice to reduce the PLL bandwidth to 5Hz.

3.7.3 Improvements and conclusion

As indicated in some papers (for example, see [30] in the case of amplitude distortion, frequency distortion, phase distortion, harmonics, phase loss, random noise, the conventional PLL presented here is not enough. For example, they use a controlled moving average algorithm to extract $\omega$ and a phase locker.
3.8 Grid modeling

![Grid connected converter](image)

Figure 3.45: Grid connected converter

The aim of this part is to modify the model introduced in section “2.2.2 Mathematical model” (Figure 2.4) to simulate a grid connected converter. We are going to add the grid voltage and impedance Eg, Rg, and Lg. A switch will be modeled with a resistor Rb (high value for an open switch, very small value for a switch closed). We can write four equations as below.

First equation: \( i_g \)

\[
\begin{align*}
e_g - v_c &= (R_g + R_b)i_g + L_g \frac{d i_g}{dt} \\
\Rightarrow i_g &= \frac{1}{sL_g} [e_g - v_c - (R_g + R_b)i_g]
\end{align*}
\]

(3.55)

Second equation: \( i \)

\[
\begin{align*}
v_c - u_s &= Ri + L \frac{d i}{dt} \\
\Rightarrow i &= \frac{1}{sL} [v_c - u_s - Ri]
\end{align*}
\]

(3.56)

Third equation: \( v_c \)

\[
\begin{align*}
i_g &= i_c + i = C_{ac} \frac{d v_c}{dt} + i \\
\Rightarrow v_c &= (i_g - i) \frac{1}{sC_{ac}}
\end{align*}
\]

(3.57)

Fourth equation: \( V_{pcc} \)

\[
v_{pcc} = i_g R_b + v_c
\]

(3.58)

With these four equations, we can establish the scheme Figure 3.47 to replace the simple grid model of Figure 3.46 (establish in section “2.2.2 Mathematical model” Figure 2.4).

![Simple grid model (phase A)](image)

Figure 3.46: Simple grid model (phase A)
We can also write more simple equations for a model without Cac.

\[
e_g - u_x = (R_g + R_b + R) i + (L + L_g) \frac{di}{dt} = R_{tot} i + L_{tot} \frac{di}{dt}
\]

\[
v_{pcc} = e_g - R_g i - L_g \frac{di}{dt}
\]

(3.59)

Then if we inject \( \frac{di}{dt} \) of the first equation in the second:

\[
v_{pcc} = e_g - R_g i - \frac{L_g}{L_{tot}} (e_g - u_x - R_{tot} i)
\]

If \( \frac{L_g}{L_{tot}} \ll 1 \Rightarrow v_{pcc} \approx e_g - R_g i
\]

(3.60) (3.61)

We can remark that if \( L_g \) is too big compare to \( L_{tot} \), the voltage \( V_{pcc} \) will be highly dependent on the current \( I \) and will vary. In the other hand, if \( L_g \) is very small compare to \( L_{tot} \), the last term of the equation can be removed and \( V_{PCC} \) is more stable.
3.9 Grid connected converter simulation

This section shows the simulations results of the complete system built with (Figure 3.49):

- **A DISCRETE block**
  - Sampling system (sample and hold block)
  - PLL
  - Decoupled controller

- **PWM block (sinusoidal PWM)**
  An asymmetric PWM is used here, as we saw in the section “2.4.1 Sinusoidal PWM”, we have $F_{S}\text{ampling} = 2 F_{\text{triangle wave}} = 2 F_{\text{witching}}$.

- **Grid and rectifier model**
  We are now using the model presented in the previous part “3.8 Grid modeling” with small unknown grid impedance $R_g L_g$ and a switch (beaker) $SW_1$. We also add a second switch in the output as we can see in Figure 3.48.

![Figure 3.48: Single phase schematic](image)

3.9.1 Simulation steps, Simulink block diagram

**SIMULATION STEPS**

The simulation is composed by three steps. In the step I : SW1 and SW2 are open, step II : SW1 closed and SW2 open, step III : SW1 and SW2 closed.

- **Step I : Synchronization**
  - SW1 and SW2 are open.
  - The voltage $V_{PCC}$ is sent to the PLL and the voltage angle $\theta$ is calculated.
  - All IGBTs are OFF (the rectifier becomes a simple three-phase diode rectifier). No current is flowing into the rectifier.
  - The controller is in **standby mode**. All discrete integrators are disabled. All integrators should be disabled when all IGBTs are OFF. Otherwise, the integrator part of the controller will try to set the error to zero but since there are no switches activated, the error cannot be set to zero. The integrator value will increase.
  - DC-link link capacitor is charged to the reference value $V_{DCE}\text{ref}$ (in the simulation, this action is done by setting the Initial Condition to $V_{DCE}\text{ref}$ into the integrator of the DC-link model). **ATTENTION**, the value $V_{DCE}\text{ref}$ should respect the condition explain in “2.2.3 Limitations” : $V_{DCmin} > 2 V_{PCC(LN,peak)}$ where $V_{PCC(LN,peak)}$ is the Line-to-Neutral amplitude of $V_{PCC}$.
- The load is now $R_{LOAD_TEMP}$. This resistor is set to a high value to avoid the discharge of $C_{DC}$.

**Step II : Closing SW1**
- The AC-side capacitor (filter) is charged (small transient).
- All IGBTs are OFF and the controller is in standby mode (no integration).
- As $V_{DC} > 2 V_{PCC(LN,peak)}$, there is no current flowing into the rectifier.

**Step III : Closing SW2 and START**
- SW2 is closed. $R_{LOAD_TEMP}$ can now be neglected since $R_{LOAD_TEMP} \gg R_{LOAD}$.
- The controller is fully activated and the IGBTs can be turned ON.

### SIMULINK BLOCK DIAGRAM

![Simulink Block Diagram](image)

**Figure 3.49 : Top level Simulink model**

The Figure 3.49 shows the top level block diagram of Simulink. You can find the details of different block in APPENDIX F.

Before presenting the simulation results, we have to precise two important points, that are, how the IGBT OFF-state and how the disabled integrators are modeled in Simulink.

- **IGBT OFF-state**
  When the IGBTs are OFF in our simulation, no current is flowing into the rectifier (DC-link voltage is high enough and the body diode of the IGBTs are blocked). Consequently, we decided to force the current to zero with the Figure 0.39 in APPENDIX F.

- **Disabled integrators**
  The integrators are disabled by forcing the value to zero (another solution could be to set $K_i$ to zero).
  You can see the Simulink block in APPENDIX F, Figure 0.35.

#### 3.9.2 Verification

In this sub-section, we verify that the equation presented in the second Chapter ("2.2.3 Limitations").
Grid voltage

\[ U_{RMS} = 400 \text{ V (Line-to-Line)} \]

\[ V_{RMS} = \frac{400}{\sqrt{3}} = 230.9 \text{ V (Phase-to-Ground)} \]

\[ E_g = \sqrt{2} \times 230.9 = 326.6 \text{ V (Phase-to-Ground amplitude)} \]

Minimum DC-link voltage

The minimum DC-link voltage is found with the equation (2.27) of section “2.2.3 Limitations”.

\[ V_{DC\text{min}} > 2 V_{LN(\text{peak})} = 2 E_g \]

\[ V_{DC\text{min}} > 2 \times 326.6 \]

\[ V_{DC\text{min}} > 653.2 \text{ V.} \]

This minimum value have been verify in our simulation. In the Simulink simulation, we found a minimum DC-link voltage around 660V.

Finally, for our simulation we will select

\[ V_{DC\text{ref}} = 700 \text{ V.} \]

This value is probably a bit low for an experiment. In reality, it will be better to select 15% or 20% more (about 750V or 790V. Refer to “2.2.3 Limitations”).

Inductance value

The equation (2.29) of section “2.2.3 Limitations” applied in our system becomes :

\[ L < \sqrt{\frac{V_{DC}^2 - E_g^2}{\omega I_d}}. \]

As we saw during the voltage controller design, section “3.5.2 Design of voltage controller” equation (3.18), the d-current is calculated by

\[ i_d = \frac{2}{3} E_g P_g \]

Then, in steady-state we can write the equality of power

\[ P_g = P_{load} = \frac{U_{dc}^2}{R_{load}} \]

Finally, the current becomes

\[ i_d = \frac{2}{3} E_g \frac{U_{dc}^2}{R_{load}} \]

\[ \Rightarrow i_d = \frac{2}{3} \frac{700^2}{326.6 \times 150} = 6.668 \approx 6.7 \text{ A} \]

This value is totally verified in the following simulation. We can now calculate the inductance.

\[ L < \sqrt{\frac{V_{DC}^2 - E_g^2}{\omega I_d}} \]

\[ \Rightarrow L < \sqrt{\frac{700^2}{3} - 326.6^2} \]

\[ \Rightarrow L < \frac{2\pi 50 \times 6.7}{0.1131 H} \]

We think that this value too high according to results read in some papers. We decided to select the inductance around 3mH (it could be 5mH or 10mH).
3.9.3 Simulation results

**Simulation 1 and 2**

The following Table 3.7 presents a summary of the simulation parameters. All the parameters for this “Simulation 1” are presented in APPENDIX F, Table 0.3.

The simulation is performed with approximation:
- We assume that the $V_{PCC}$ voltage is equal to the grid voltage $E_g$ (Figure 3.48). That is only true if the grid impedance is small enough compared to impedance $RL$.
- We assume that we know exactly the converter parameters, that is:
  $$\hat{R} = R \ ; \ \hat{L} = L \ ; \ \hat{C} = C$$

<table>
<thead>
<tr>
<th>GRID AND CONVERTER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid $U_{RMS}$ (V), line-to-line RMS</td>
<td>400</td>
</tr>
<tr>
<td>$R_g$ (Ω), grid resistance</td>
<td>1e-3</td>
</tr>
<tr>
<td>$L_g$ (H), grid inductance</td>
<td>1e-5</td>
</tr>
<tr>
<td>$R$ (Ω)</td>
<td>0.05</td>
</tr>
<tr>
<td>$L$ (H)</td>
<td>3e-3</td>
</tr>
<tr>
<td>$C$ (F)</td>
<td>2200e-6</td>
</tr>
<tr>
<td>$V_{DCref}$ (V)</td>
<td>700</td>
</tr>
<tr>
<td>$V_{DCref}$ step (V)</td>
<td>30</td>
</tr>
<tr>
<td>$R_{LOAD}$ (Ω)</td>
<td>150</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PWM VALUE</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Triangular freq. $Fc$ (kHz)</td>
<td>10</td>
</tr>
<tr>
<td>Mode</td>
<td>Asymmetric</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TIME</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>STEP II: SW1 closing at ... (s)</td>
<td>0.005</td>
</tr>
<tr>
<td>STEP III: IGBTs ON at ... (s)</td>
<td>0.01</td>
</tr>
<tr>
<td>$V_{DCref}$ step at ... (s)</td>
<td>0.025</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CONTROLLER VALUE</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_p$, current controller</td>
<td>37.6991</td>
</tr>
<tr>
<td>$K_i$, current controller</td>
<td>628.3185</td>
</tr>
<tr>
<td>$K_{p_v}$, voltage controller</td>
<td>0.0028</td>
</tr>
<tr>
<td>$K_{i_v}$, voltage controller</td>
<td>0.01</td>
</tr>
<tr>
<td>Sample freq. $F_s = 2F_c$ (kHz)</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 3.7: Summary of simulation 1 parameters

The basic waveforms are plotted in Figure 3.50. All voltages are phase-to-ground voltages. For this simulation 1, we selected a small grid impedance and we observe a voltage $V_{PCC}$ without distortions, and we can say that $V_{PCC}$ and the grid voltage $E_g$ are equal (stiff grid). We will see the influence of the grid impedance in the simulation 3.

On the current plot ($i_{abc}$), when the breaker SW1 is closing at time 0.005s, no current is flowing into the rectifier. Then, at time 0.01s, we activate the IGBTs, we close SW2 and the system is starting. We observe a small ripple on the current due to the switching. This ripple increases if the switching frequency decreases or if the line inductance decreases.

Finally, at time 0.025s, the step on $V_{DCref}$ is starting. The current is reaching the saturation limit of ±15A and the DC-link voltage is increasing linearly from 700V (initial condition) to 730V. Another Simulation have been done with a bigger step of 100V on $V_{DCref}$ with saturation limit in the current controller about ±50A (see APPENDIX F, Figure 0.27).

Furthermore, we observe a small overshoot on the DC-link voltage $V_{DC}$. This overshoot may increase if the switching frequency decreases. On Simulation 2 Figure 3.51a, we plot the DC-link voltage for a switching frequency selected at 3kHz. We observe oscillations. These oscillations can be removed by adjusting the PI controller coefficients. The calculation for the PI coefficients depends on the bandwidth $\alpha_i$ and $\alpha_v$ selected as follow:

$$\alpha_i = 2\pi F_s / 10 \quad \text{and} \quad \alpha_v = 2\pi F_s / 100.$$
Nevertheless, when we select a switching frequency 3kHz, we modify the bandwidth \( F_S = 2F_{SW} \) and we modify the PI controllers. For example, if we select the bandwidth with \( \alpha_i = 3 \times 2\pi F_S/10 \) and \( \alpha_v = 3 \times 2\pi F_S/100 \), the oscillations are highly reduced (Figure 3.51b.).
SIMULATION 3 — INFLUENCE OF THE GRID IMPEDANCE

The simulation have been done to show the influence of the grid impedance on the system. We multiplied by 10 both \( R_g \) and \( L_g \).

<table>
<thead>
<tr>
<th>GRID MODIFICATION</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_g ) (Ω), grid resistance</td>
<td>1e-2</td>
</tr>
<tr>
<td>( L_g ) (H), grid inductance</td>
<td>1e-4</td>
</tr>
</tbody>
</table>

Table 3.8: Simulation 3 — New grid impedance parameters

As we explain in section “3.8 Grid modeling”, if \( L_g \) is too big compared to the total inductance value \( L_{tot} \), the voltage \( V_{PCC} \) will be highly dependent on the current and will vary. The Figure 3.52a. shows the effect of the grid impedance, the voltage is distorted. Despite that, the system is still working well even if this voltage is used by the PLL to calculate the voltage angle. Figure 3.52b. shows the voltage angle under simulation 3 condition, there is no visible distortion.

SIMULATION 4 — TEST WITH ACTIVE DAMPING GA

The results of simulation 4 is plotted in APPENDIX F, Figure 0.28. The simulation parameters are the same as simulation 1 with the following modification on controller parameter. We also rewrite the equation to find them (equation XXX section “3.5.3 Voltage saturation, anti-windup, active damping”).

\[
Ga = \frac{\alpha_v C}{3E_g} \\
Kp_v = \frac{\alpha_v C}{3E_g} \\
Ki_v = \alpha_v Ga
\]

We can see on Figure 0.28 that the controller doesn’t work properly anymore, some oscillation appear on DC-link voltage and the current is completely distorted.

We observed that the simulation becomes stable again by reducing the controller parameters values. The Figure 0.29 shows a simulation with the following modified parameters:
The Simulink diagram is given in APPENDIX F, Figure 0.41.

**SIMULATION – ESTIMATED PARAMETERS $\hat{R}$, $\hat{L}$, $\hat{C}$**

For simulation5, we now assume that $\hat{R} \neq R$; $\hat{L} \neq L$; $\hat{C} \neq C$. One by one, we modify (increase and decrease) the estimated value and verify the effect on the waveforms.

** Resistance influence $\hat{R} \neq R$**

A couple of tests have been done and we didn’t see any problem due to a bad estimation of the line resistance.

<table>
<thead>
<tr>
<th>Tests with $\hat{R}$ equal to...</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R + 3R$</td>
<td>No visible influence</td>
</tr>
<tr>
<td>$R - 3R$</td>
<td>$R &lt; 0$, instability</td>
</tr>
<tr>
<td>$R - 0.9R$</td>
<td>No visible influence</td>
</tr>
</tbody>
</table>

*Table 3.11: Resistance influence*

** Inductance influence $\hat{L} \neq L$**

<table>
<thead>
<tr>
<th>Tests with $\hat{L}$ equal to...</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L + 3L$</td>
<td>See Figure 0.30 in APPENDIX F.</td>
</tr>
<tr>
<td></td>
<td>- Distorted reference voltage</td>
</tr>
<tr>
<td></td>
<td>- Vdc oscillations</td>
</tr>
<tr>
<td>$L - 0.9L$</td>
<td>See Figure 0.31 in APPENDIX F.</td>
</tr>
<tr>
<td></td>
<td>- Distorted reference voltage</td>
</tr>
<tr>
<td></td>
<td>- Vdc oscillations</td>
</tr>
<tr>
<td></td>
<td>- Distorted line current</td>
</tr>
</tbody>
</table>

*Table 3.12: Inductance influence*

** Capacitor influence $\hat{C} \neq C$**

<table>
<thead>
<tr>
<th>Tests with $\hat{C}$ equal to...</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C - 0.9C$</td>
<td>See Figure 0.32 in APPENDIX F.</td>
</tr>
<tr>
<td></td>
<td>- Line current oscillation</td>
</tr>
<tr>
<td></td>
<td>- Vdc oscillation</td>
</tr>
<tr>
<td>$C + 3C$</td>
<td>No visible influence</td>
</tr>
</tbody>
</table>

*Table 3.13: Capacitor influence*

** Conclusion**

As we can see in the previous tables, inductance and capacitor estimation are more critical than resistance estimation. Nevertheless, we saw in simulation that a bad estimation with an error about 20-40% is not problematic. The waveforms are pretty similar.
SIMULATION 6 – LOAD STEP

Simulation 6 is done by modifying the load resistance from 150Ω to 30Ω, that corresponds, to a load asking suddenly for 16kW (30Ω) instead of 3kW (150Ω).

![Simulation 6 results](image)

**Figure 3.53 : Simulation6 results**

The input power (blue) is calculated with the following equation (3.18):

\[ P_g = \frac{3}{2} E_g i_d \]

The output power (black) as below (equation (3.62)):

\[ P_{load} = \frac{v_{dc}^2}{R_{load}} \]

As we can see in the previous figure (Figure 3.53), an overshoot appears in the d-components of the current (6A overshoot). Nevertheless, this overshoot is not so visible on the 3-phase current.

Regarding the DC-link voltage, we observe a small drop (5.5V, 0.7%). The controller is acting and after a couple of millisecond, the error is set to zero again. The controller performance seems to good for disturbance rejection.
4 VOLTAGE ORIENTED CONTROL – IMPLEMENTATION

4.1 Block diagram

The set-up present in the lab can represented with the following block diagram. It shows one power stage, electronic stage, and software stage.

![Block diagram](image)

**Figure 4.1: Laboratory set-up**

<table>
<thead>
<tr>
<th>MATERIAL</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>dSpace system</td>
<td>DS1103</td>
</tr>
<tr>
<td>Computer</td>
<td>PC</td>
</tr>
<tr>
<td>Matlab / Simulink</td>
<td>Real Time Workshop library and dSpace library</td>
</tr>
<tr>
<td>Control Desk software</td>
<td>Used for real time control</td>
</tr>
<tr>
<td>Measurement box</td>
<td>Voltage and current</td>
</tr>
<tr>
<td>Emitter card</td>
<td>Optical emitters</td>
</tr>
<tr>
<td>Receiver card and IGBT drivers</td>
<td>Optical receivers</td>
</tr>
</tbody>
</table>

**Table 4.1: Lab material**

This set-up is not running yet. No experiments have been done in this thesis.

4.2 Principle

From your Simulink model (see next section), Matlab generates a C-code and send it to the hardware (dSpace DS1103) connected to the PC.
Then, using Control Desk software, you can build an interface with control panel: knobs, control buttons. You can also add visualizations: led, gauge, graph and so on.

To be able to run our system, some modification need to be done on our Simulink model.

### 4.3 Simulink model modification

The top level Simulink model for implementation is show in Figure 4.2.

![Simulink model](image)

**Figure 4.2**: Top level Simulink model for dSpace implementation

ADC

![ADC example](image)

**Figure 4.3**: ADC example (see APPENDIX G. Figure 0.42)

The important information using ADC and DAC is shown in the following table. You need to multiply by 10 a value from ADC, and divide by 10 before sending to DAC.

<table>
<thead>
<tr>
<th>ADC</th>
<th>DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>Correspondance in Simulink</td>
</tr>
<tr>
<td>-10V...+10V</td>
<td>-1...+1</td>
</tr>
</tbody>
</table>

**Table 4.2**: ADC/DAC value range
PWM

The PWM block have been replaced by the dSpace PWM block “DS1103SL_DSP_PWM3”. This is a sinusoidal symmetric PWM (F\text{triangle} = F\text{switching} = F\text{sampling}). You can modify the carrier wave (triangle) and the deadtime duration. “PWM stop” allows to enable (PWM stop = 0) or disable (PWM stop = 1) the PWM block. This signal needs double type and not Boolean (but following “Simulink help” it should be Boolean). The \textit{Termination and Initialization} values of the block should be set (see next section for explanation about \textit{Termination} and \textit{Initialization}).

The input range for “duty cycle abc” is [0;+1]. Finally, we have to send our three-phase reference voltage to this block but a scaling block is needed. This block is included to the control block and shown in Figure 4.4.

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{scaling_block}
\caption{Scaling block}
\end{figure}

\textbf{CONTROL SYSTEM AND PLL}

You can find the detail of this block in APPENDIX G. Figure 0.43. You can see that the scaling block presented above is included to this block. The control is totally similar to the one presented in Chapter 3 except that:

- All the sample & hold block have been removed but the system is still discrete.
- The sample time ”Ts” is replaced by ”-1” (inherited).

The enable signal is maybe not useful. It could be removed. It depends how will be run the system. But if it’s used, the output port “Uabc\_ref range [0;1]” should be set to the following characteristics:

- Reset when disabled
- Initial output = 0.

In this configuration, when the block is disabled, the output will be zero and the PWM block will see zero duty cycle and will open the switches.

\textbf{TRIGGER SIGNAL, SYNCHRONIZATION}

The sample & Hold have been removed. Now, we need to specify when acquire a sample. We know that we need to sample on the peak of the triangular wave of the PWM, ideally, on every peak that is the asymmetric PWM.

We guess that more than one solution is possible to run the system. But for simplicity, as we said above, we decided to use the PWM block “DS1103SL_DSP_PWM3” using a symmetric PWM.

Furthermore, this block is link to an interruption “DS1103SLAVE_PWMINT”. The interruption is generated every \textit{POSITIVE PEAK} of the triangular wave of block PWM3 as shown in Figure 4.5. Consequently we have : F\text{interuption} = F\text{sampling} = F\text{triangle} = F\text{switching}.
The interrupt is generated that can be shifted nearly over the whole PWM period by specifying the interrupt alignment (Source: dSpace Help in Matlab [33]).

In Simulink, a block “DS1103SLAVE_PWMINT” is available. To trigger the whole Simulink model, we have to link this block to another block called “Timer Task Assignment” as shown in the top-level model Figure 4.2. Finally, every interruption signal, ONE sample will be acquired.

Nevertheless, the “overrun” condition should be checked. We need to be sure that the calculation (in the controller) is finished before a new sample is acquired.

**CONTROL SIGNAL “GO”**

The “GO” signal (Figure 4.2) is used to activate the integrator part of the controller (see section “3.9.1 Simulation steps, Simulink block diagram” for explanation). It is also used to enable or disable PWM block.

**HOW TO FORCE IGBTs OFF**

It’s possible to force IGBTs OFF disabling the block “Control system and PLL” since the output will be zero when disable (if set correctly...). A zero value will be sent to the PWM block and the switches will be open.

Another solution in presented in Figure 4.6 and is present in the main block diagram in APPENDIX G. Figure 0.43.
The switches are activated by the “GO” signal in our model.

- If GO = 0: Output = 0  IGBT = OFF
- If GO = 1: Output = Uabc range [0;1]  IGBT = ON

4.4 Running an experiment

To run an experiment we need to introduce some important points that are: STOP/PAUSE/RUN mechanism, simState variable, Initialization and Termination value, how to build a model and which parameters should we used, and how to use Control Desk software.

A tutorial is also available in [37], and we also advice to use the dSpace Help in Simulink (more useful than the dSpace books).

**simState Variable**

The simState variable is an internal variable that allows to read or set the simulation state of the application [33]. This variable is created when the system is built (see how to build a model in the following).

It can take the following value (Table XXX).

<table>
<thead>
<tr>
<th>Simulation State</th>
<th>simState variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>STOP</td>
<td>0</td>
</tr>
<tr>
<td>PAUSE</td>
<td>1</td>
</tr>
<tr>
<td>RUN</td>
<td>2</td>
</tr>
</tbody>
</table>

*Table 4.3: simState values*

**STOP/PAUSE/RUN Mechanism**

The STOP/PAUSE/RUN mechanism depends on the simState variable. By controlling it, you can stop, pause or run your experiment.

In our case, we chose to control it via Control Desk. When your system is built and your variable description file (“.sdf”) is opened in Control Desk (see next paragraph), you can find this variable in the main group of variable.

The following figure shows a part of control panel in Control Desk, the simState is linked to “Push Buttons”.

![Diagram showing the switch activation by the “GO” signal and the states of IGBTs](image)
In each Simulink block, you can specify an *Initialization* and *Termination* value. The following table shows the links with the `simState` variable.

<table>
<thead>
<tr>
<th>STATE</th>
<th>simState</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>STOP</td>
<td>0</td>
<td>Termination code executed. Termination value are used.</td>
</tr>
</tbody>
</table>
| PAUSE   | 1        | ▪ If the previous state was in RUN, no Termination values are used, the current outputs are kept.  
          |          | ▪ If the system was in STOP mode, the Initialization values are used.  |
| RUN     | 2        | ▪ If the simulation was previously in the PAUSE mode, the execution of the application is re-enabled.  
          |          | ▪ If the previous state was STOP, the states of the model are reset to their initial values and the execution of the application is restarted.  |

*Table 4.4: Relation between application state and Initialization and Termination values*

**SIMULATION PARAMETERS AND “BUILD MODEL”**

When your Simulink model is modified, you can *BUILD* the model from Simulink using:

//Tools/Real Time Workshop/Build Model (or CTRL+B)

But before that, you may need to modify the *Configuration Parameters* as follow:

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solver/Step</td>
<td>Fixed</td>
</tr>
<tr>
<td>Solver/Stop Time</td>
<td>INF</td>
</tr>
<tr>
<td>Optimization/block reduction</td>
<td>Disable</td>
</tr>
<tr>
<td>Real Time Workshop/System Target File</td>
<td>rti1103.tlc</td>
</tr>
</tbody>
</table>

*Table 4.5: Configuration Parameters before BUILD*

Before pressing “CTRL+B” (*build*), we advice to open Control Desk software. In this case, Control Desk will automatically detect that a new file have been built (variable description file with extension “.sdf”).

Then, a “new experiment” should be created, and the “.sdf” file should be “added to experiment”. You can now create a new “layout”. Since you have the layout open, you can add buttons, knobs, display, gauge, numeric input (to write a value) and so on. After that, you can link your Simulink variables (or labels) to graphical instruments, for example, a button to control this variable or a
graph for visualization. The variables are visible in the “Tool Window” in the bottom part of the Control Desk interface.

**ATTENTION !**

When you *build* the model, the C-code generated is automatically sent to your hardware and the application **START TO RUN** (*simState = 2*). So, as you can see in the Figure 4.2, the signal GO and the Enable are set to zero. Consequently, when our system is built and start running, the PWM is OFF and the controller is disabled.
5 CONCLUSIONS AND FUTURE WORK

Controller lab-tests

In the Chapter 3, some simulations were presented. The controller seems to be correct and stable. We suppose that some lab-tests can now be achieved with a grid-connected converter with simple resistive load. The Simulink file prepared for implementation may need to be slightly modified but the idea was presented in Chap4 with some key point to run an experiment with dSpace. A tutorial is available at the reference [37].

Stability analysis

In this report, a simple stability analysis have been done. Nevertheless, this analysis is quite simplistic (with approximations) and have been realized in continuous time only. It should be also complete in discrete time because the controller is implemented in discrete time.

Deadtime

As we explain in the first part (2.4.3 Dead time effect), the performances of the converter are affected by injection of deadtime in the PWM signals to avoid short circuit of the DC-link. We suppose that some simulations of this deadtime and some compensation should be done before testing the controller in the laboratory.

Modulation method

The modulation method could be improved. In our system, we decided to implement a sinusoidal Pulse Width Modulation mainly for its simplicity and acceptable performances. We advice to test it in the lab. Nevertheless, a simulation with Space Vector Modulation (SVM) should be also simulated and a deep comparison to sinusoidal PWM could be done. The SVM is known for its effectiveness, simplicity for implementation, harmonics reduction.

Control method

A last possible improvement could be done by implementing a Virtual Flux Oriented Control (VFOC). It could improve the performance under non-ideal line voltage conditions. Furthermore, this method could be useful if a machine is added to the model (AC side) because machine models are generally done with flux-oriented reference.

We also advice to implement a load current controller. Reading some papers, we saw some battery charger configuration with another stage after the rectifier (on more leg with two IGBTs for DC-DC conversion). A load current controller was responsible of the switches for this stage ([3] ).
REFERENCES

Control and Modeling of PWM rectifiers


Power Electronics


PWM

Carrier-based PWM

SVM

REFERENCES

[27] JIN-WOO JUNG. “Project #2 Space Vector PWM inverter”. Project performed at Mechatronic Systems Laboratory, Department of Electrical and Computer Engineering, The Ohio State University, USA. 2005. Available at: 
http://www2.ece.ohio-state.edu/ems/PowerConverter/SpaceVector_PWM_Inverter.pdf

PLL


Deadtime


dSpace

[33] dSpace Help in Simulink.

[34] JUSTIN D. LANGDON. “Design and Adaptive Control of a Lab-based, Tire-coupled, Quarter-car, Suspension Test Rig for the Accurate Re-creation of Vehicle Response”. MSc Thesis, Virginia Polytechnic Institute and State University, USA. January 31, 2007. Available at: 


[36] Laboratory Tutorial, Massachusetts Institute of Technology, Department of Mechanical Engineering, 2.737 Mechatronics–Spring 2006, February 14, 2006. Available at: 

A. Three-phase system – Coordinate transformations

A.1 Voltage and current definition

First of all, we can define the voltage and current of a three-phase system:

\[ v_a(t) = E_m \cos(\omega t) \]
\[ v_b(t) = E_m \cos \left( \omega t - \frac{2\pi}{3} \right) \]
\[ v_c(t) = E_m \cos \left( \omega t - \frac{4\pi}{3} \right) \]

(positive sequence here)

\[ i_a(t) = I_m \cos(\omega t + \varphi) \]
\[ i_b(t) = I_m \cos \left( \omega t + \varphi - \frac{2\pi}{3} \right) \]
\[ i_c(t) = I_m \cos \left( \omega t + \varphi - \frac{4\pi}{3} \right) \]

For any three-phase system composed of positive and negative sequence we have

\[ v_a(t) + v_b(t) + v_c(t) = 0 \quad \forall t \]

If the system present an asymmetry, a zero sequence appears and is define as the mean value

\[ v_0(t) = \frac{v_a(t) + v_b(t) + v_c(t)}{3} \]

A good thing is that there will never be any zero sequence in the currents, provided that there is no neutral connection.

A.2 Equivalent two-phase system, \( \alpha \beta \)-transformation (Clarke)

A three-phase system can be described with only two components \( \alpha \) and \( \beta \) (real and imaginary respectively). Furthermore, we call a space vector the quantity

\[ v^s(t) = v_a(t) + jv_b(t) = \frac{2}{3} K \left( v_a(t) + v_b(t) e^{j\frac{2\pi}{3}} + v_c(t) e^{j\frac{4\pi}{3}} \right) \]

where \( K \) is a scaling constant. The transformation from ABC-to-\( \alpha \beta \) (Clarke transformation) depending on the scaling constant \( K \) is:
A.3 Synchronous coordinate, dq-transformation (Park)

We can now define a transformation of the previous space vector \( v^s = v_\alpha + jv_\beta \) (we now drop the time argument “(t)” for simplicity) with

\[
v_{dq} = v^s e^{-j\theta}
\]

where \( \theta = \omega t \). This transformation makes \( v_{dq} \) similar to fixed complex phasor. This transformation is called dq-transformation and can be regarded as observing the space vector from a coordinate system rotating with the frequency \( \omega \) (synchronous coordinate or dq-coordinate). We denote the space vector in synchronous coordinates as

\[
v_{dq} = v_d + jv_q.
\]

![Figure 0.1: Relation between αβ-frame and dq-frame (rotating) [23]](image)

Giving dc-steady state quantity, the synchronous coordinates are very useful for analysis, implementation of control algorithm (controller design is easier on dc-quantities).

We can write

\[
v^s = v_{dq} e^{j\theta} = (v_d + jv_q)(\cos \theta + j\sin \theta) = (v_d \cos \theta - v_q \sin \theta) + j(v_d \sin \theta + v_q \cos \theta)
\]

\[
= v_\alpha + jv_\beta
\]

\[
\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix}.
\]

Source: [4]
A.4 Simulation

These transformations and the theta angle (voltage angle) are very critical for all the simulations in the project. To be sure that we have the correct angle, we created this angle first, then, a three-phase voltage system is created according to this angle as we can see in the following block diagram.

\[ \omega = 2\pi 50 \text{ rad/s} \]

\( E_m \) will be the amplitude of the 3-phase voltages (amplitude invariant transformation).

The transformations are implemented as below.

The simulation results are plotted on the following figure.
Simulation comments:
- Theta is positive.
- Voltage is placed on the d-axis.
- Beta signal is delay (lag).
- We verify a direct three-phase system (A first[0 rad], B in second[-2π/3 rad], C third[-4π/3 rad]).

A.5 Impedance in synchronous coordinates

We assume in the report (current controller design) that the impedance is : \( Z(s) = (s + j\omega)L \). We can prove this relation with the following.

\( y^s \) is a general space vector, its transformation in synchronous coordinates is

\[ y_{dq} = y^s e^{-j\theta} \]

and its time derivative is transformed as

\[ \frac{dy^s}{dt} = \frac{d(e^{j\theta} y_{dq})}{dt} = e^{j\theta} \left( j\omega y_{dq} + \frac{dy_{dq}}{dt} \right) \]

Then, using the derivative operation \( p = d/dt \) we get

\[ py^s = e^{j\theta} (p + j\omega) y_{dq} \]

In the Laplace domain, the following substitution is made : \( s \rightarrow s + j\omega \). This implies that the complex impedance of an inductor in synchronous coordinates is

\[ Z(s) = (s + j\omega)L \]
Source: [4]

**Figure 0.6**: Illustration $\alpha\beta$- and $dq$-impedance
B. Voltage and current control, continuous simulation

B.1 Simulink current control tests – Block diagram

Figure 0.7 : Simulink current control tests – Block diagram
B.2 Continuous voltage controller, simulation with saturation, anti-windup, active damping

**Figure 0.8**: Voltage controller – Simulation with saturation, anti-windup, active damping

<table>
<thead>
<tr>
<th>NEW PARAMETERS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ga</td>
<td>0.0057</td>
</tr>
<tr>
<td>Kiv</td>
<td>7.1205</td>
</tr>
</tbody>
</table>

**Table 0.1**: New parameters for voltage controller with active damping
C. Digital simulation

DISCRETE INTEGRATOR

As the controller will be digital, we decided to simulate the control system in discrete time. The integrator have been implemented as below.

\[
\begin{align*}
\hat{y}(k) &= y(k-1) + Ts \ u(k-1) \\
\Leftrightarrow Y(z) &= Y(z) z^{-1} + Ts \ U(z) z^{-1} \\
\Leftrightarrow Y(z)(1 - z^{-1}) &= Ts \ U(z) z^{-1} \\
\frac{Y(z)}{U(z)} &= \frac{Ts z^{-1}}{1 - z^{-1}} = \frac{Ts}{z - 1}
\end{align*}
\]

We can also draw the block scheme with the following equation:

\[
Y(z) = [Y(z) + Ts \ U(z)] z^{-1}
\]

**Figure 0.9**: Discrete integrator

REMARK FOR SIMULINK SIMULATION

In a simulation where discrete and continuous blocks are used at the same time, in order to come back from discrete to continuous, we should add a zero to the discrete signal with sampling time “INF” as below. Then, the output signal is treated as continuous by Simulink.

\[
T_s = \text{INF}
\]

**Figure 0.10**: Simulink discrete-to-continous
D. Voltage and current control, discrete time simulation

![Graphs showing voltage and current control results](image)

**Figure 0.11**: Controller simulation results (discrete)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$ (Ω)</td>
<td>0.1</td>
</tr>
<tr>
<td>$L$ (H)</td>
<td>5e-3</td>
</tr>
<tr>
<td>$C$ (μF)</td>
<td>2200</td>
</tr>
<tr>
<td>$\omega$ (rad/s)</td>
<td>$2\pi 50$</td>
</tr>
<tr>
<td>$E_m$ (V), ph-to-gnd amplitude ($=E_d$)</td>
<td>115\sqrt{2}</td>
</tr>
<tr>
<td>$F_{sw}$ (kHz), switching frequency</td>
<td>20</td>
</tr>
<tr>
<td>$R_{load}$ (Ω)</td>
<td>500</td>
</tr>
<tr>
<td>$V_{dc}$ reference (V)</td>
<td>400</td>
</tr>
<tr>
<td>$\alpha_l = 2\pi F_{sw}/10$ (rad/s)</td>
<td>1.26e4</td>
</tr>
<tr>
<td>$\alpha_y = 2\pi F_{sw}/100$ (rad/s)</td>
<td>1.26e3</td>
</tr>
<tr>
<td>V controller, $K_{pv}$</td>
<td>0.0057</td>
</tr>
<tr>
<td>V controller, $K_{iv}$</td>
<td>0.01</td>
</tr>
<tr>
<td>I controller, $K_{pi}$</td>
<td>62.8</td>
</tr>
<tr>
<td>I controller, $K_{ii}$</td>
<td>1.26e3</td>
</tr>
<tr>
<td>I saturation (A)</td>
<td>±15</td>
</tr>
<tr>
<td>$V_{dc}$ step at 0.03 (V)</td>
<td>50</td>
</tr>
<tr>
<td>Triangular wave Freq. (kHz)</td>
<td>20</td>
</tr>
<tr>
<td>Sampling frequency (kHz), $F_s=2 F_{tri}$</td>
<td>40</td>
</tr>
</tbody>
</table>
E. Stability analysis cont.

E.1 Simulations

Figure 0.12: Nyquist of $L_i$

Figure 0.13: Bode of $L_i$
Figure 0.15: Nyquist of $L_v$ ($P$ only)

**PROPORTIONAL CONTROL ONLY**
Figure 0.16: Bode of $L_v(P$ only$)$

Figure 0.17: Bode of $S_v(P$ only$)$
APPENDICES

PROPORTIONAL AND INTEGRAL CONTROL

Figure 0.18: Bode of Lvi (P only)

Figure 0.19: Nyquist of Lv (PI)
Figure 0.20: Bode of $L_v$ (PI)

Figure 0.21: Bode of $S_v$ (PI)
Figure 0.22: Bode of $L_{vi}$ (PI)

**WITH ACTIVE DAMPING $\text{Ga}$**

Figure 0.23: Bode of $L_v$ (PI Ga)
**Figure 0.24**: Bode of $L_v (PI\ Ga)$

**Figure 0.25**: Bode of $S_v (PI\ Ga)$
Figure 0.26: Bode of Lvi (PI Ga)
F. Grid connected converter simulation cont.

F.1 Data and simulations

<table>
<thead>
<tr>
<th>GRID</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (Hz)</td>
<td>50</td>
</tr>
<tr>
<td>$U_{RMS}$ (V), line-to-line RMS</td>
<td>400</td>
</tr>
<tr>
<td>$V_{RMS}$ (V), line-to-neutral RMS</td>
<td>230</td>
</tr>
<tr>
<td>$E_g$ (V), line-to-neutral amplitude</td>
<td>327</td>
</tr>
<tr>
<td>$R_g$ (Ω), grid resistance</td>
<td>1e-3</td>
</tr>
<tr>
<td>$L_g$ (H), grid inductance</td>
<td>1e-5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PWM</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Triangular freq. $F_c$ (kHz)</td>
<td>10</td>
</tr>
<tr>
<td>Mode</td>
<td>Asymmetric</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CONVERTER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R$ (Ω)</td>
<td>0.05</td>
</tr>
<tr>
<td>$L$ (H)</td>
<td>3e-3</td>
</tr>
<tr>
<td>$C$ (F)</td>
<td>2200e-6</td>
</tr>
<tr>
<td>$F_{SW}$ (kHz), switching freq.=$F_c$</td>
<td>10</td>
</tr>
<tr>
<td>$R_{LOAD}$ (Ω)</td>
<td>150</td>
</tr>
<tr>
<td>$R_{LOAD}.TEMP$ (Ω)</td>
<td>1e5</td>
</tr>
<tr>
<td>$V_{DCref}$ (V)</td>
<td>700</td>
</tr>
<tr>
<td>$V_{DCref}.STEP$ (V)</td>
<td>30</td>
</tr>
<tr>
<td>Step at... (s)</td>
<td>0.025</td>
</tr>
<tr>
<td>Power $V_{DCref}.Z/R_{LOAD}$ (W)</td>
<td>3267</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISCRETE SYSTEM</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample freq. $F_s = 2F_c$ (kHz)</td>
<td>20</td>
</tr>
<tr>
<td>Sample time $T_s$ (s)</td>
<td>5e-005</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SIMULATION</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solver Step</td>
<td>Variable</td>
</tr>
<tr>
<td>Step max</td>
<td>$1/(10F_{SW})$</td>
</tr>
<tr>
<td>Faster solver</td>
<td>Ode23tb</td>
</tr>
<tr>
<td>Tolerance</td>
<td>1e-3</td>
</tr>
</tbody>
</table>

Table 0.3: Parameters of simulation1
Figure 0.27: Simulation1 – 100V Step on $V_{D_{Cref}}$, saturation limit ±50A (current controller)
Figure 0.28: Simulation4 with active damping
Figure 0.29: Simulation4 with active damping, modified controller parameters
Figure 0.30: Inductance influence – Test: $\hat{L} = L + 3L$

Figure 0.31: Inductance influence – Test: $\hat{L} = L - 0.9L$

Figure 0.32: Capacitor influence – Test: $\hat{C} = C - 0.9C$
Figure 0.33: Simulink – DISCRETE BLOC
Figure 0.34: Simulink – DISCRETE BLOCK / PLL

Figure 0.35: Simulink – DISCRETE BLOCK / DECOUPLED CONTROLLER / Discrete PI V Controller

Figure 0.36: Simulink – GRID AND RECTIFIER MODEL / eg_abc
Figure 0.37: Simulink – DISCRETE BLOCK / Decoupled Controller
Figure 0.38: Simulink – PWM block

Figure 0.39: Simulink – GRID AND RECTIFIER MODEL / GridPhaseB
Figure 0.40: Simulink – GRID AND RECTIFIER MODEL
Figure 0.41: Simulink – DISCRETE BLOCK / Decoupled Controller with active damping
close all; clear all; clc

%***********************************************************************
% GRID / BREAKER / COMMAND
%***********************************************************************
grid_f = 50;
w = 2*pi*grid_f;    % Line frequency
Urms = 400;         % Line-to-line RMS voltage
Vrms = 400/sqrt(3); % Line-to-ground RMS voltage
Eg = Vrms*sqrt(2)   % Phase-to-ground voltage amplitude
Rg = 1e-3;          % 1e-2
Lg = 1e-5;          % 1e-4

%BREAKER
Rb_open = 1e5;   %ATTENTION VALUE
Rb_close = 0.01;
Cb = 1e-9 ; %Cac - ATTENTION VALUE (NEED DESIGN FILTER, avoid resonance frequency)

%STEP breaker SW1 command : 0/1
breaker_step_time = 0.005; %Close switch at...
b sucker_initial_value = 0;
b sucker_final_value = 1;   %Or more than 0

%IGBTS ON/OFF SIGNAL (To activate switching)
IGBTONOFF_step_time = 0.01;
IGBTONOFF_initial_value = 0;
IGBTONOFF_final_value = 1;

%***********************************************************************
% CARRIER BASED PWM PARAMETERS
%***********************************************************************
Carrier_amp = 1;   % Triangular wave Amplitude
Carrier_f = 10e3;  % Triangular wave frequency = Fsw
Tc = 1/CARRIER_f;  % Triangular wave period

%***********************************************************************
% CONVERTER PARAMETERS
%***********************************************************************
R = 0.05;          % Line Resistance
L = 3e-3;          % Line inductance
C = 2200e-6;       % DC bus capacitor
Fsw = Carrier_f;   % Converter switching frequency = Triangular wave f
Rload = 150;       % Output load, Pout about 800W
Rload_temp = 1e5;  % Temporary output load to avoid discharge of C
Vdc_ref = 700;     % Output voltage reference
initial_condition_integrator = Vdc_ref; % IC model integrator
% CONTROLLER PARAMETERS
Ts = 0.5*Tc;  % Sample time, half of triangular wave period, Fs = 2*Fc
Fs = 1/Ts;

% ESTIMATED PARAMETERS
R_hat = R;
L_hat = L;
C_hat = C;      % probably, C_hat = C OK
Vpcc_hat = Eg ; % Ph-to-gnd - Possible for stiff grid, otherwise, Vpcc < Eg

% CURRENT PI Regulator (thesis, state-variable W=Vdc^2)
alphaI = Fs/10*2*pi;     % Bandwidth in rad/s
Kpi = alphaI*L_hat
Kii = alphaI*R_hat

% VOLTAGE PI Regulator (thesis, state-variable W=Vdc^2)
alphaV = Fs/100*2*pi;    % Bandwidth in rad/s
Kpv = alphaV*C_hat/(3*Vpcc_hat)
Kiv = 0.01

% SATURATION (TO MODIFY, depends on rectifier limit)
Isaturation_upper_limit = 50; %saturation on Iref, V PI controller
Isaturation_lower_limit = -50;

% FEEDFOWARD Ed_hat/Eq_hat FILTER
alphaf_ff = alphaI/10;

% PLL PARAMETERS
% Gain gamma1&2 : calculated in simulink (we assume Ed_hat and Eq_hat can change)
Fbandwidth_pll = 20;        %bandwidth in Hz
rho_pll = 2*pi*Fbandwidth_pll;  %bandwidth in rad/s
gam1 = (rho_pll^2)/Vpcc_hat
gam2 = 2*rho_pll/Vpcc_hat

% TESTS
% INPUT STEP
input_step_time = 0.025;
input_step_value = 100;
G. Implementation

Figure 0.42: ADC block
Figure 0.43: Control block

- All the sample & hold block have been removed but the system is still discrete.
- The sample time "Ts" is replaced by "1" (inherited).

Output "Uab_ref range [0:1]" set to:
--> "Reset when disabled"
--> "Initial output = 0"

IF GO=0 --> Output = 0  IGBT = OFF
IF GO=1 --> Output = Uab[0:1]  IGBT=ON