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Selection of Dynamic performance Control Parameters for Classic HVDC in PSS/E

Optimization of CCA and VDCOL parameters

Master of Science Thesis

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Conducted at: ABB Power Systems, Ludvika

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Abstract

The objective of this thesis work is to define the strategy of tuning current controller amplifier and voltage dependent current order limiter parameters to achieve good dynamic performance with a wide range of a.c. systems in PSS/E. The defined control parameter could be adapting independent of different power levels and configurations. Basically, three different HVDC transmission types are used such as overhead lines, cables and back to back. The dynamic control performances are varied with respect to transmission types. Hence, the control parameters could be different. The control parameters could be intended for stability improvement of HVDC system connected with wide range of AC system parameters.

As a part of a HVDC project design, large efforts are made in tuning control system parameters for the specific project conditions. However, for customer support, in planning studies it is necessary to provide a set of robust control parameters giving a representative performance for “any” configuration.

This thesis work mainly deals with dynamic response of HVDC system. The dynamic instabilities occur mostly at d.c. system connected to weak receiving a.c. network. It causes high ac voltage fluctuations as a consequence very difficult to recover the dc system after the fault clearing instant due to repetitive commutation failures. Therefore, good dynamic dc control strategy has to define by tuning the current control amplifier and voltage dependent current order limiter.

This will be done by analyzing the responses of the HVDC model for different transmission types, network strengths and control parameters. Results will be evaluated, and presented so that it is possible to define performance and what needs to be improved. Evaluation will be made of the responses obtained using the existing parameters and those obtained using the set of rules proposed in the thesis.

Acknowledgement

This thesis work was conducted at ABB AB Power systems, Ludvika, Sweden.
I would like to thank Mr. David Shearer, for providing me this big opportunity and helpful discussions during this period.
I would like to express my sincere gratitude to my leading supervisor Mr. Per-Erik Björklund for his guidance and encouragement. Also, thank him again for helping me with writing and correcting this report.
I would like to thank Mr. Wenkan Huang for his assistance regarding modeling and support during the whole period of this work. Further, I wish to thank Mr. Per Holmberg and Mr. Boris Nordström for their good suggestions and comments.
I wish to thank also Mr. Massimo Bongiorno, my examiner at Chalmers University of Technology for reading carefully and correcting the manuscript even though he is in parental leave.
Eventually, I would like to thank my family for their love and unconditional support.

Arunkumar Muthusamy

List of abbreviation

AC	Alternating Current
HVDC	High Voltage Direct Current
CCA	Current Control Amplifier
VDCOL	Voltage Dpendent Current Order Limiter
VCA	Voltage Control Amplifier
VSC	Voltage Source converter
CFC	Converter Firing Control
CEA	Constant Extinction Angle
CC	Constant Current
RAML	Rectifier Alpha Minimum Limiter
PSS/E	Power System Simulator for Engineers

List of Symbols

α	Valve ignition delay angle
μ	Overlapping angle
γ	Commutation margin angle
Udio	No load direct voltage
d_{XN}	Commutation reactance
d_{RN}	Commutation resistance
Udc	Direct voltage
Iorder	DC current order
α_{max}	Alpha maximum
α_{minRec}	Alpha minimum rectifier
α_{minINV}	Alpha minimum Inverter
Imargin	Current Margin
U_{dref}	DC voltage reference
IorderLim	Current order limited (VDCOL output)
Porder	Power order
γ_{ref}	Gamma reference
Gammao	Commutation margin angle
UD Low	Direct voltage lower threshold
UD High	Direct voltage higher threshold
AMAX	Alpha maximum (rectifier)
AMIN	Alpha minimum (rectifier)
Io low	Current order lower limit
Io abs max	Current order maximum limit
αorder	Alpha order
CFprev_angle	Commutation failure prevention angle
Idmeas	Measured direct current
Ud_Tc_Dn	Direct voltage down time constant
Ud_Tc_Up	Direct voltage UP time constant

Contents

Scope of thesis work:

ABB have different types of HVDC simulation models. One type is called rms-models or ac quantities represented as phasor. This type of model is suitable for planning studies and stability studies, typically performed by utilities. The rms-model used in this thesis work was Power System Simulator for Engineers (PSSE). It is mainly used for steady state analysis like load flow analysis, optimal power flow, switching studies etc. and dynamic simulations like transient, dynamic and long-term stability analysis. The PSSE HVDC classic model has to be robust and user friendly to the customer, so the control parameters should be optimized to get good dynamic performance. Mainly, this document describes about dynamic performance studies of HVDC classic system connected to weak ac networks.

Outline of thesis work:

- Performance analysis of HVDC classic models

The dynamic performance of the HVDC system could be analysed by applying faults at ac or dc bus nearer to the converter, it could be inverter or rectifier. There are certain factors which shall be verified, like recovery time of dc system after fault clearing, non-repetitive commutation failure during recovery, avoid rectifier inrush current at inverter fault or dc fault in order to prevent commutation failure at rectifier, oscillatory power recovery after fault clearing due to improper damping. Basically, dynamic performance study is to investigate the performance of the HVDC control system. Also, some specific tests could be done to check the performance of the each controller i.e. current control, voltage controller.

- Control parameter optimization

The overall good dynamic and steady state performance of HVDC classic system is dominated by the CCA and VDCOL parameters.

- Verification of optimized parameters

The optimized parameters have been verified by simulating with these parameters in different cases which has defined in the performance analysis. The results are plotted.

- Modelling of HVDC links in Nordic-32 system

The classic HVDC links and Light links are implemented and applied shunt faults at different nodes which nearer to rectifier and inverter in order to analyse the control system performance during transients.

- Conclusion and future work
- Frequency dependent representation of dc system

1.0 Introduction:

1.1 HVDC technology:

The tradition HVDC classic technology is used to transmit power for long distances via overhead lines or submarine cables with reduced losses. There is a breakpoint between ac and dc transmission distance, where after this point dc transmission is smarter and effiecient.It also reduces the synchronous constraints between the two ac systems. It enhances steady state and dynamic stability of the ac system. The recent 15 years, also a new technology is used, HVDC Light, based on VSC (Voltage Source Converters). HVDC Light has considerably higher dynamic performance compared to HVDC Classic, but still HVDC Classic is dominating for low cost bulk transmissions.

1.2 History:

The first HVDC transmission in the world was begun in 1954. It was 150KV, 20MW DC link between Swedish main land and island of Gotland by ASEA. Until 1970, mercury valves are used for conversion of direct current.

After a powerful invention of high power electronic device so called thyristors for static power transfer has been encouraged by power industries and its substantial increase of rating and reliability over the years.

1.3 Types of HVDC configuration:

There are different configurations of DC links used for transmitting power based on power capacity.

Monopole, ground return

The power is transmitted from one converter station to another station through one conductor (positive or negative polarity) and return is grounded at both stations (figure **1**).

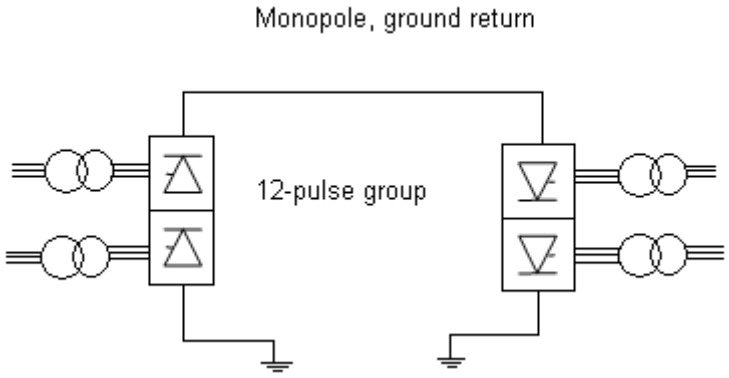


Figure 1 Monopole, ground return

Monopole, metallic return.

The power is transmitted from one converter station to another converter station through one conductor and metallic conductor is used as return and grounded at one end (figure **2**).

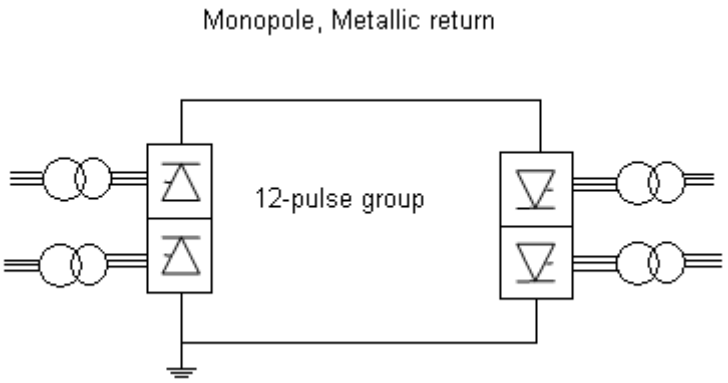


Figure 2 Monopole, metallic return

Bipolar

Bipole (figure **3**) has two conductors, upper pole is operating in positive current and positive voltage and lower pole is operating in negative voltage and negative current. Both poles transmit a power in same direction. It is grounded at both stations. Both poles are operating at equal currents during steady state, therefore zero current through the ground. It can be operating as a single pole during fault at another pole.

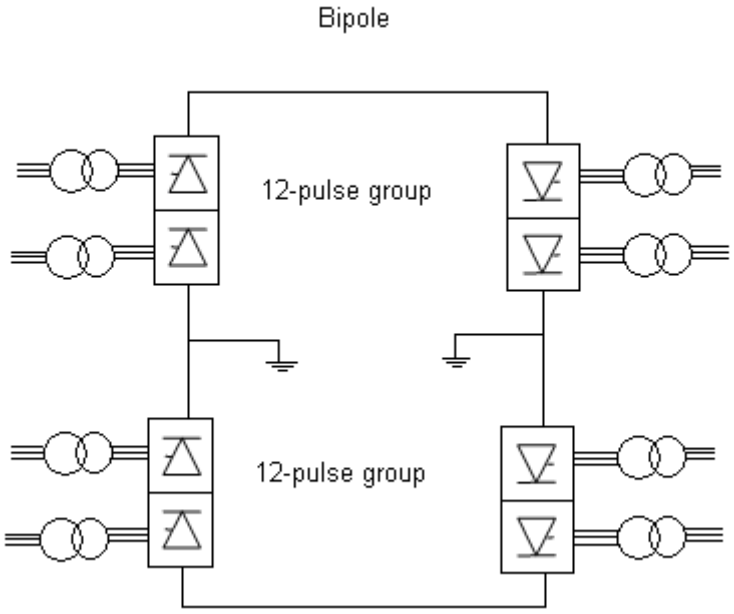


Figure 3 Bipole

Monopole, midpoint grounded.

Monopole, midpoint grounded (figure **4**) has two conductors as same as monopole metallic ground, but instead of using the return conductor as power transmission conductor, grounded at one end. It reduces the transmission loss since cables can have full voltage, the total transmission voltage is doubled, and consequently the current needed is half for same power and transmission capacity has been increased.

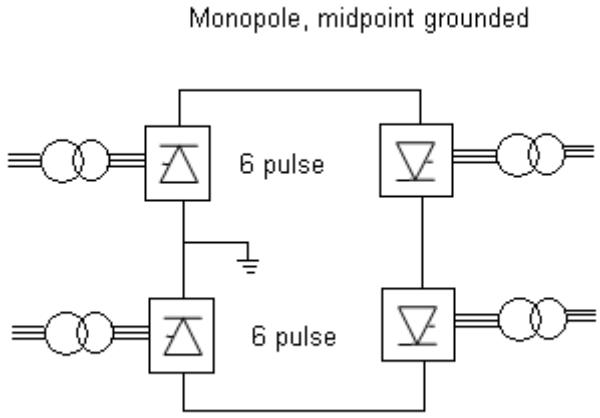


Figure 4 Monopole, mid-point grounded

Back to back.

Both rectifier and inverter stations are located at same place (figure **5**). The normal configuration is to use monopolar blocks, but several converter blocks can be installed in parallel, each with separated dc circuit. The purpose of this kind of configuration is to connect two asynchronous systems. It reduces the total system cost, due to absence of lines/cables; current rating of the system shall be increased with reduced voltage. Thus, transformer size could be reduced.

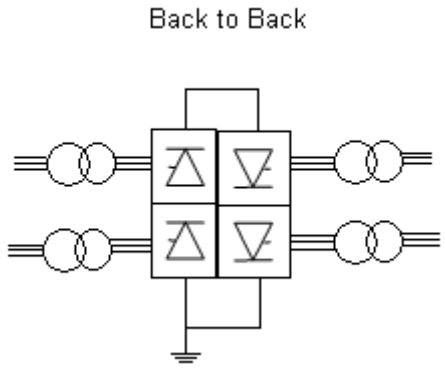


Figure 5 Back to Back

1.4 Line commutated converter. 6 Pulse Bridge

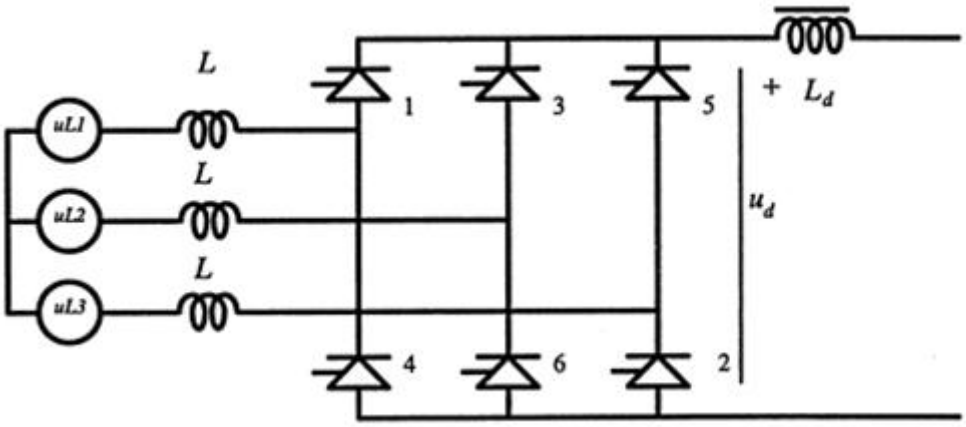


Figure 6 6-pulse GRAETZ bridge

Since the operation of 6 pulses GRAETZ circuit is well documented in many books, even though some basics are needed to understand the below chapters.
Line commutated converter is nothing but current source converter, in order consider the theoretical analyse of 6-pulse bridge (figure **6**) we have to assume infinite 3-phase ac source connected to the converter transformer with finite leakage inductance (L) , ideal valves and infinite smoothing reactor.
Because of finite leakage inductance in converter transformer (protect the valves during valve short circuit) commutation from one valve to another valve is not instantaneous. During commutation, three valves will be conducting. Such a period is called overlapping period (μ) which is normally less than 60 degrees.

1.5 Case with no overlapping period

Instantaneous line to neutral voltages of three phases is

$$Ua = Em \cdot \cos(\omega t + 60) \quad (1.1)$$

$$Ub = Em \cdot \cos(\omega t - 60) \quad (1.2)$$

$$Uc = Em \cdot \cos(\omega t - 180) \quad (1.3)$$

Corresponding line to line voltages are

$$Uac = Ua - Uc = 1.732 \cdot Em \cdot \cos(\omega t + 30) \quad (1.4)$$

$$Uba = Ub - Ua = 1.732 \cdot Em \cdot \cos(\omega t - 90) \quad (1.5)$$

$$Ucb = Uc - Ub = 1.732 \cdot Em \cdot \cos(\omega t + 150) \quad (1.6)$$

The instantaneous direct voltage(shown in figure **7**) across the 6-pulse bridge is composed of 60 degrees of line to line voltage across the upper and lower conducting valves. Therefore, the average direct voltage can be found by integrating the 60 degree area with no ignition delay.

$$Udo = \frac{3}{\pi} \int_{-60}^{0} Uac \cdot d\theta = \frac{3}{\pi} \int_{-60}^{0} Em \cdot \cos(\theta + 30) \cdot d\theta$$

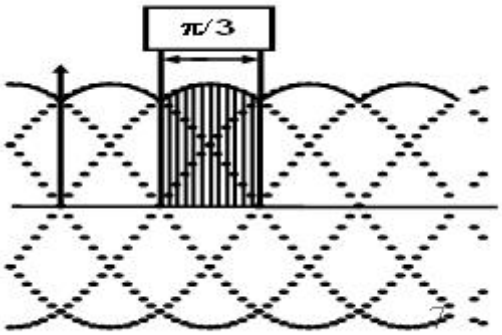


Figure 7 DC voltage waveform without delay angle

$$\text{Udo} = \frac{3\sqrt{3}}{\pi} \cdot \text{Em} \qquad (1.7)$$

Where, Em is the peak value of the line to neutral voltage.
Udo is the ideal no load direct voltage with α=0

$$\text{Udo} = \frac{3\sqrt{2}}{\pi} \cdot E_{LL} \qquad (1.8)$$

Where, E_{LL} is the rms Line to Line voltage.
With ignition delay angle α (shown in figure **8**), the integration limit simply increased by α and therefore

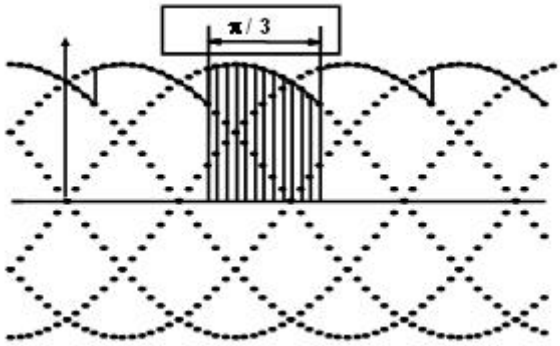


Figure 8 DC voltage waveform with delay angle

$$\text{Udo} = \frac{3\sqrt{3}}{\pi} \cdot \text{Em} \cdot \cos\alpha = \frac{3\sqrt{2}}{\pi} \cdot E_{LL} \cdot \cos\alpha \qquad (1.9)$$

The effect of delayed angle will reduce the average direct voltage by cosα factor.
Since the practical alpha can be varied from 5 degrees to 142 degrees, dc voltage polarity can be changed for power reversal and current can not be reversed since unidirectional device has been used.

1.6 AC and DC current relationship*:*

Assuming no losses in the converter bridge, Power sending from the AC network is equal to the DC power

$$\text{Pd} = \text{Ud} \cdot \text{Id} = 3 \cdot U_{LN} \cdot I_{L1} . \cos\phi \qquad (1.10)$$

Where, Pd is direct current power
U_{LN} is the line to neutral voltage

I_{L1} is the fundamental frequency line current

ϕ is the phase angle between line voltage and line current shown in figure

The line current is in rectangular shape (figure **9**) since Id is constant (smoothing reactor prevents current from changing). Each valve in the 6 pulse bridge conducts 120 degree per cycle. With no delay angle, line current is in phase with voltage. With delay angle, the line current lags voltage. This is the reason why the converter consumes reactive power.

By fourier analysis, rms value of line current is given by

$$I_{L1} = \frac{\sqrt{2}}{\pi} \int_{-60}^{60} Id \cdot \cos\theta \cdot d\theta$$

$$I_{L1} = \frac{\sqrt{6}}{\pi} Id \qquad (1.11)$$

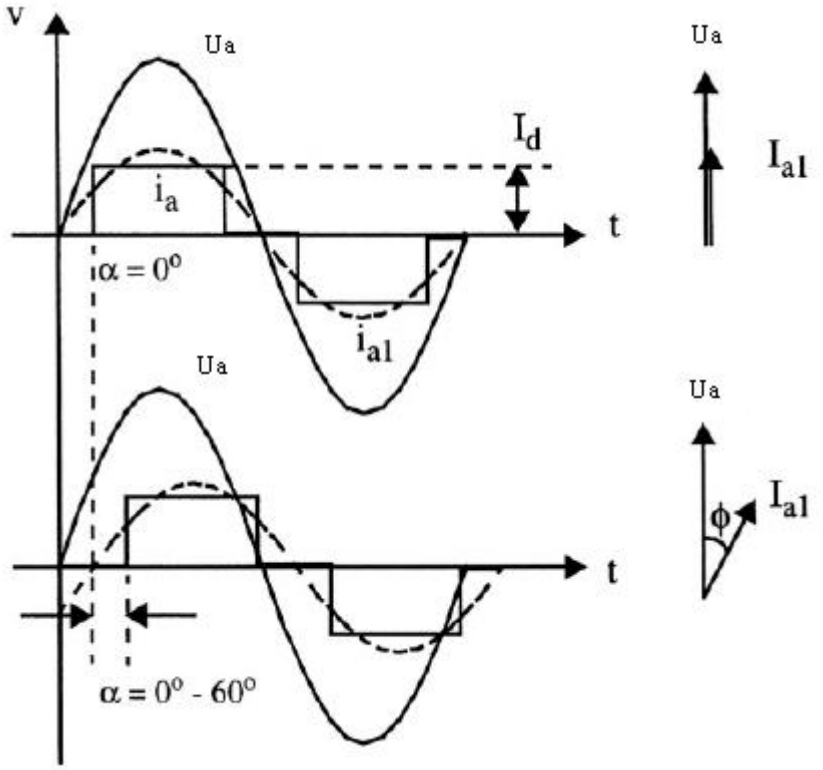


Figure 9 AC and DC current relationship with and without delay angle

1.7 Case with overlapping period less than 60 degrees

As same reason as explained before, due to converter transformer inductance, valve takes some finite time to transfer a current from one valve to another valve. Such as called overlapping time.

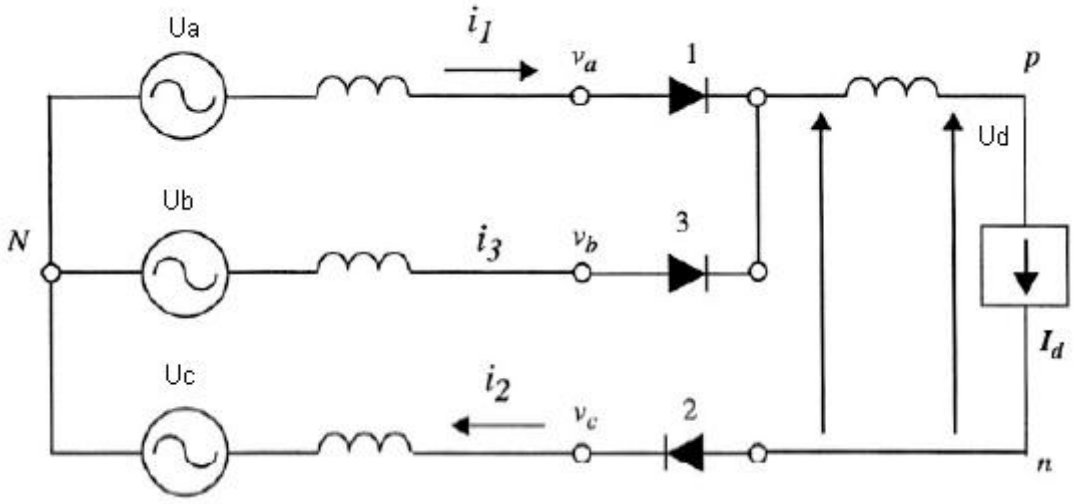


Figure 10 converter bridge circuit with valves 1,2 and 3

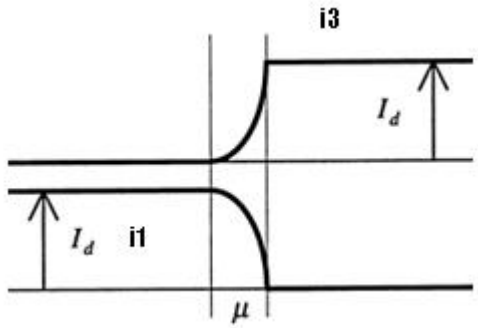


Figure 11 commutation of current in valve 1 and 3

If suppose the valve 1 and valve 2 is conducting at an instant (figure **10**), and valve 3 is fired and starts conducting. But still valve 1 is conducting until the stored magnetic energy in the converter transformer goes to zero. During the commutation Id is summation of i1 and i3, i1 is decreasing from Id to zero and i3 is increasing from 0 to Id (figure **11**).

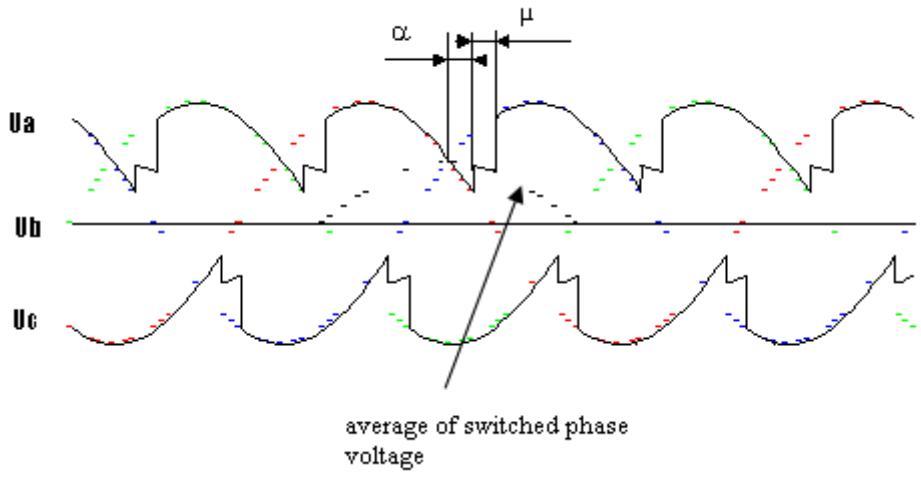


Figure 12 direct voltage with effect of delay angle and overlapping angle

Voltage drop due to overlapping angle μ (figure **12**) can be achieved by

$$\Delta Ud = 6 \cdot f \cdot L \cdot Id = 6 \cdot \frac{\omega}{2 \cdot \pi} \cdot L \cdot Id$$

$$\Delta Ud = 3 \cdot \frac{\omega}{\pi} \cdot L \cdot Id \qquad (1.12)$$

Since the current changes through the inductance is 6 times for 6-pulse converter

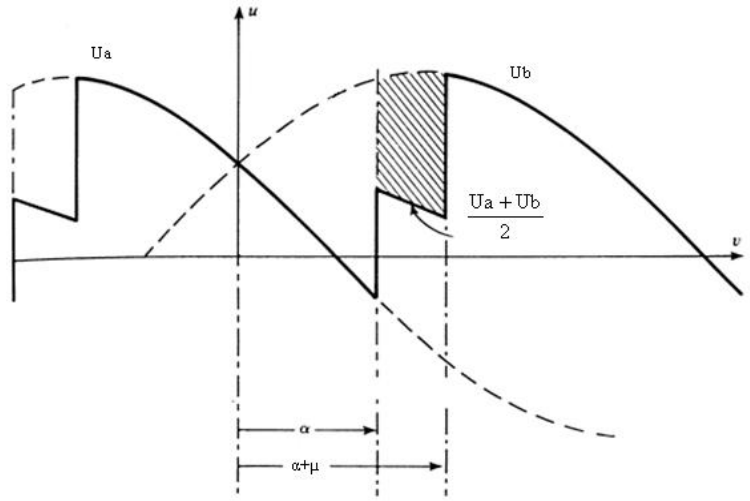


Figure 13 rectifier direct voltage

Therefore, the total rectifier DC voltage will be

$$Ud = 1.35 \cdot U_{LL} \cdot \cos\alpha - \frac{3}{\pi} \cdot \omega \cdot L \cdot Id \qquad (1.13)$$

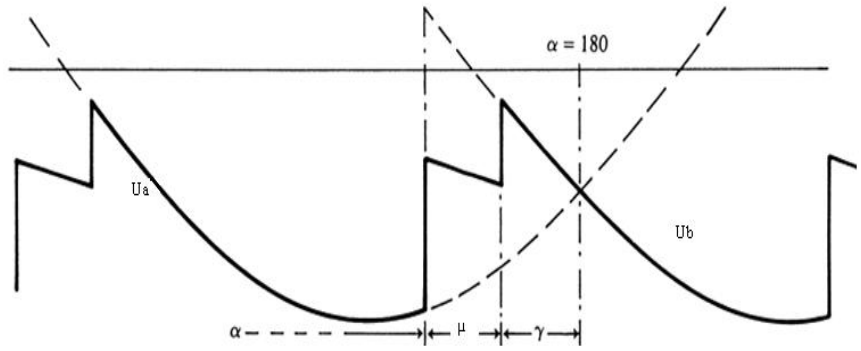


Figure 14 Inverter direct voltage

15

The inverter DC voltage will be found by

$$\alpha + \mu + \gamma = 180$$

$$Ud = (1.35 \cdot ULL \cdot \cos\gamma - \frac{3}{\pi} \cdot \omega L \cdot Id) \qquad (1.14)$$

2.0 HVDC Classic control characteristics:

2.1 HVDC control overview

Normally, HVDC system operates in constant power control mode. Power order is given by the user. Current order (Iorder) derived from the power controller, which is send to the VDCOL (voltage dependent current order limiter) and into the current control amplifier (CCA). The alpha order from the CCA is send to the converter firing control which determines the firing instant of valves (shown in figure **16**). The function of VDCOL and CCA will be explained later in this report.

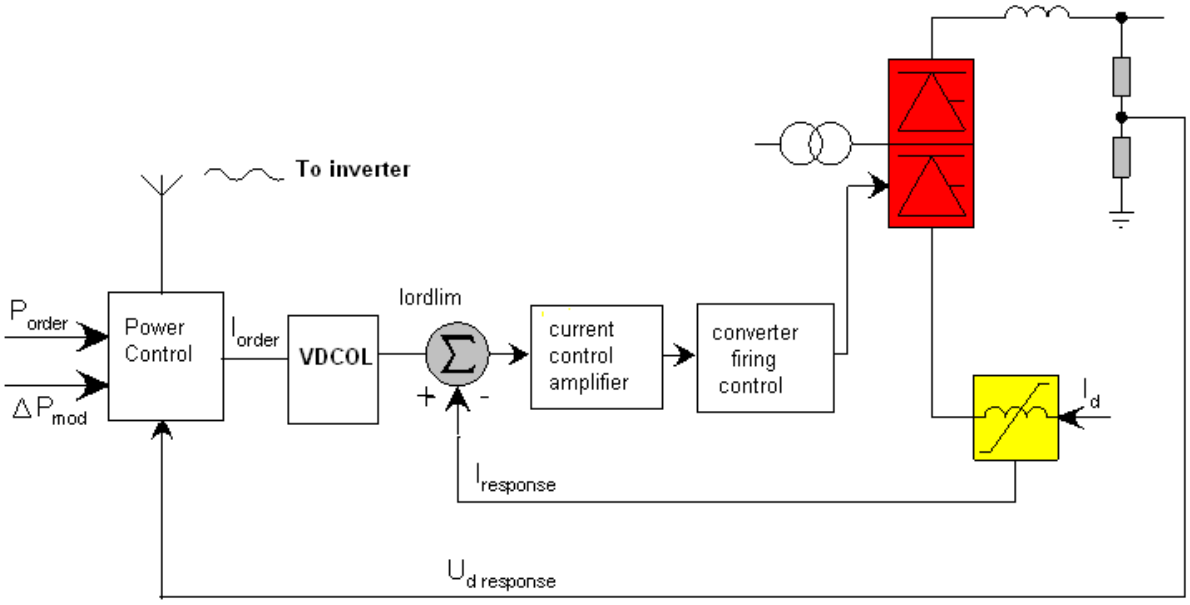


Figure 16 HVDC control overview

The primary function of HVDC controls are:

Fast and flexible power control between the terminals under steady state and transient operation.

Better stability of ac system.
Fast protection of ac and dc system faults.

i) it minimizes over voltage across the valves
ii) it reduces the short circuit current through the valves and lines/cables
iii) it reduces the reactive power consumption
iv) avoids repetitive commutation failures

These above advantages are achieved by varying exact firing instant of valves.

The converter firing control which determines the firing instants for each valve to determines the rated DC voltage. The input for the firing control system could be the output of current control, voltage control, minimum alpha control, and minimum commutation margin control mode or alphamax control.

Usually, dc transmission controlling and co-operation between rectifier and inverter has been explained based on Ud/Id characteristics (figure **17**). Traditionally rectifier controls the current and inverter operates with constant commutation margin under normal operation.

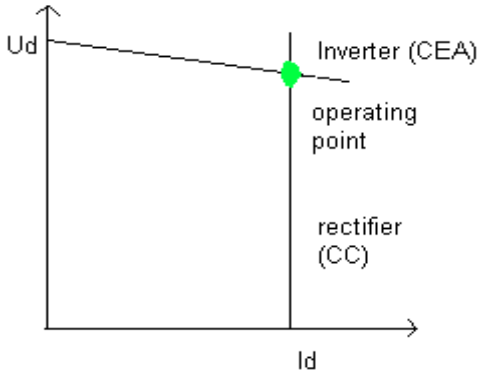


Figure 17 Ud-Id characteristics

Under steady state, typically rectifier would be act as constant current source i.e. constant current control and inverter will operate as constant counter voltage source i.e. constant extinction angle. The current order at the rectifier is determined by the manipulation of power order and inverter dc voltage. To maintain stability at rectifier, it is necessary to have less (I_{dref} – I_d) deviation in dc current and also (γmeas-γref) deviations should be keep as low as possible for inverter stability. The intersection of two modes gives normal operation point.

2.2 Alpha-minimum characteristics at rectifier:

This characteristics is determined by the equation shown below,

$$U_{\mathrm{dc}} = U_{di0} \cdot \cos\alpha - \left(d_{xN} + d_{rN}\right) \cdot \frac{U_{di0N}}{I_{dcN}} \cdot I_{dc} \qquad (1.15)$$

The above equation determines the dc voltage across the converter. If we assume practical minimum alpha of 5 degrees in order to have certain voltage across the valve before firing and transformer reactance (d_{xN} + d_{rN})·U_{di0N}/I_{dcN} are also always constant. Hence, increasing dc current reduces the dc voltage i.e. negative slope determined by the transformer reactance and dc current (reduced voltage due to overlapping of valve currents).

2.3 Constant current characteristics at rectifier:

This characteristic could also be explained by the same equation (**1.15**), by assuming current as constant and alpha as variable. It can be seen from the figure **18** that higher dc voltage at minimum alpha and increasing of alpha decreases the dc voltage. The direct current is determined based on the current order, which could be selected between minimum current capability and the rated current of valves. The maximum current carrying capacity of valves would be determined for a transient time period to limit valve stress.

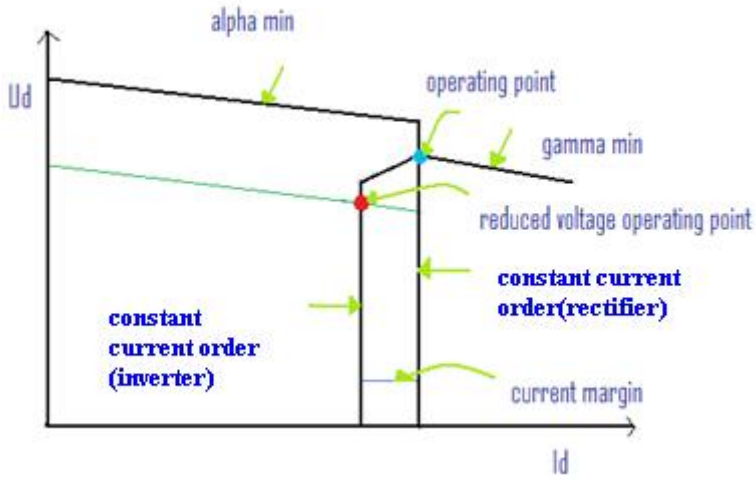


Figure 18 Ud-Id characteristics

2.4 Constant extinction angle characteristics:

Inverter is normally operating as alpha-max or constant commutation margin mode in order to have certain extinction angle to commutate the valves without fail. Under normal operation, inverter operates at γ=17 at 50Hz, it is not recommended to increase or decrease to limit reactive power consumption and avoid commutation failure. At steady state, inverter operates normally as constant dc voltage control mode. Assuming gamma constant and Idc as variable gives negative slope characteristics. This slope would be even more negative if the ac system is weaker.

$$U_{dc} = \left(U_{di0} \cdot \cos\gamma - \left(d_{xN} - d_{rN}\right) \cdot \frac{U_{di0N}}{I_{dcN}} \cdot I_{dc} \right) \tag{1.16}$$

2.5 Alpha minimum at inverter:

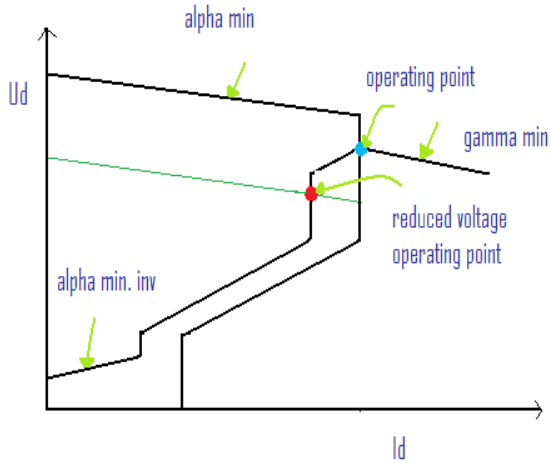
The power reversal could be obtained by increase the current order of the inverter higher than rectifier. In case of dc line fault, it is recommended that both converters should operate as inverter to make the fault current in dc line to zero as fast as possible. If there is no minimum alpha limit at inverter, it could also operate as rectifier by reduced alpha cause feeding of dc fault. Therefore, always minimum alpha (figure **19**) at the inverter is limited to 110^0. However, rectifier could be operating as inverter for reason explained above. Also because of one more reason, inverter should have minimum counter voltage to start current flow after the fault clearance.

2.6 Current margin:

To de activate the inverter current controller at normal operation, current order at inverter is subtracted from rectifier by 10% .such as called current margin. The solution with a current controller also at the inverter, but normally deactivated by the current margin, avoids the current to become zero during disturbances at rectifier. When there is sudden voltage drop at the rectifier ac system cause hit the minimum alpha limit, if there is no current controller at inverter, reversed potential difference between inverter and rectifier will force the current to

zero since the unidirectional current device has been used. Alpha at inverter could increase up to when it hits minimum extinction angle.

2.7 Modified inverter characteristics:



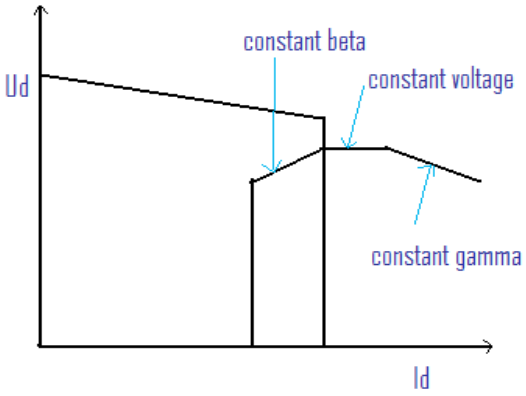


Figure 19 Ud-Id characteristics with VDCOL **Figure 20 constant Beta and constant voltage**

Constant beta control (figure **20**) is nothing but Alphamax control which is explained in the previous page. Constant voltage control is normally used under reduced voltage operation; the U_{dref} is set to higher value at normal voltage operation to avoid hunting between Alphamax and Voltage controller. But in reduced voltage operation U_{dref} shall be reduced to nominal reduced voltage.

2.8 Regulator Overview

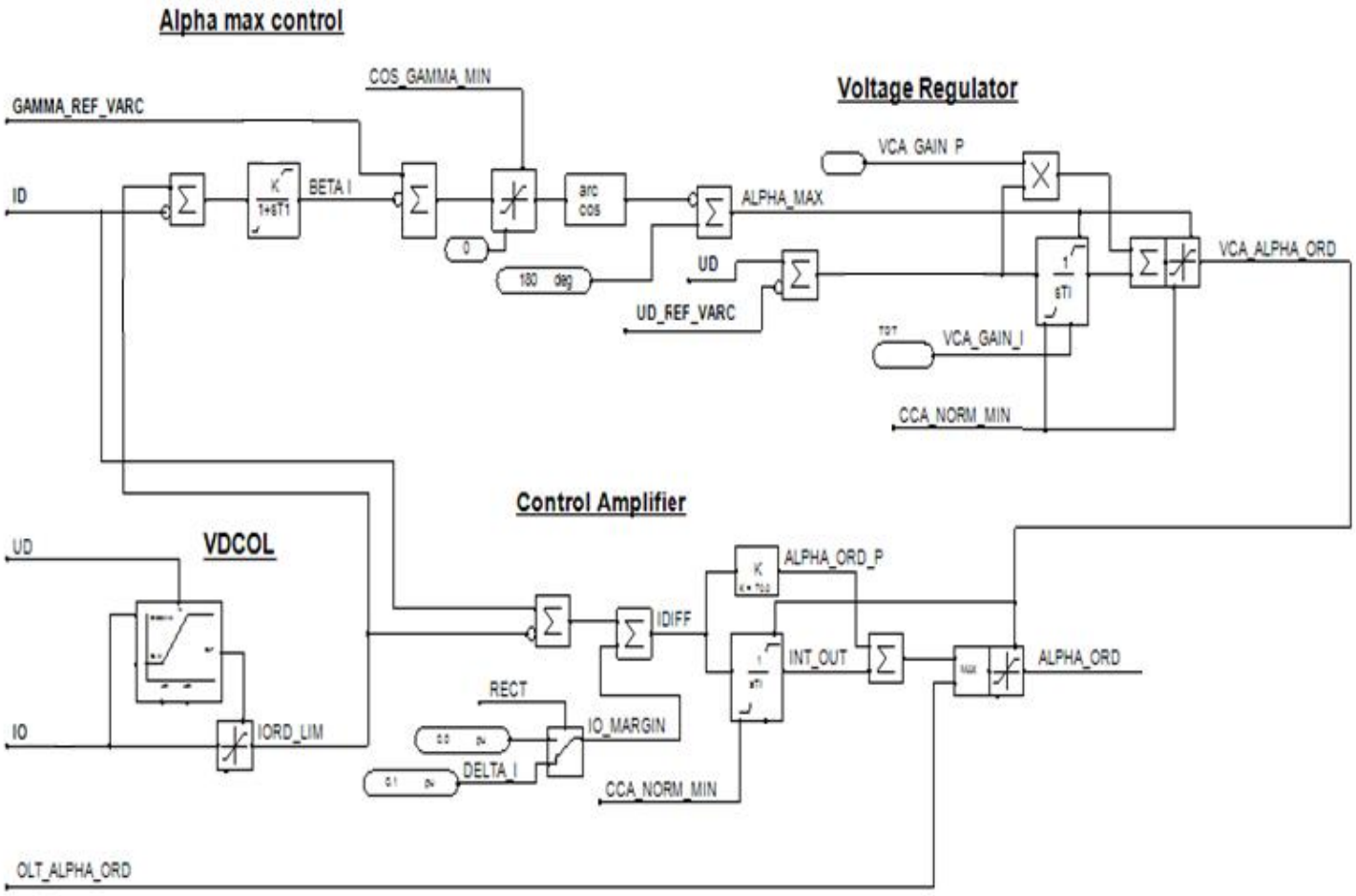


Figure 21 Overview of HVDC regulator

2.9 Active power control:

Power control is normally a closed loop control required for stable operation of HVDC system. The power order is determined by the user at master station (rectifier). The current order to the current control amplifier can be derived from the equation

$I_{ord} = P_{ord}/U_d$

Current controller is normally a PI regulator, input for the PI regulator will be error of measured value and reference value of current, the output from the regulator determines the firing instant of valves hence the dc voltage to maintain constant potential difference between converters.

U_d is determined by the inverter under normal operation (constant extinction angle). The current order is sent to slave station (inverter) by telecommunication link. In order to de activate the current controller at inverter, current order is reduced by current margin, typically 10% of nominal current.

Under normal condition, system operates in constant power control mode; it can be switched to constant current control mode when telecommunication failure happens.

2.10 Voltage dependent current order limiter (VDCOL):

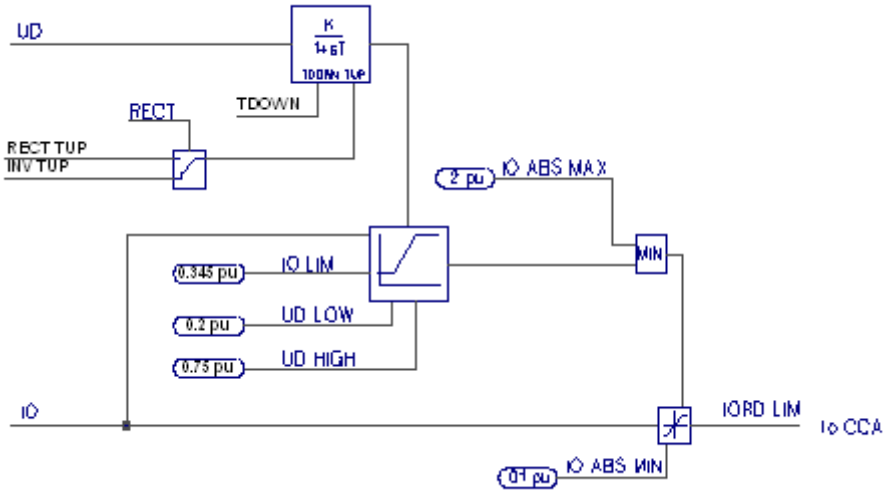


Figure 22 Voltage dependent current order limiter

The main function of VDCOL (figure **22**) control is to reduce the current order to lower value when there is a reduction in dc voltage due to contingencies, in order to prevent the higher consumption of reactive power and valve voltage stress. If the system is operating in constant power control mode, current would be increased to maintain the constant power at low voltage causes higher consumption of reactive power will decrease the ac voltage further and induce commutation failure during the recovery of dc system. The break points (figure **23**) for dc voltages are typically between 70% and 30%. These breakpoints could vary relative to the strength of the ac system. Normally, the long lines have same Udhigh breakpoints for both rectifier and inverter but in contrast long cables need different Udhigh break points for charging the cable i.e. 50% for rectifier and 90% for inverter. If there is fault in the inverter end, voltage would decrease greatly, if the VDCOL is not activated, the power control mode will increase the current to keep the power constant. Increased current will increase the reactive power consumption of converter; it will increase the risk of subsequent commutation failures if the ac system is relatively weak. The low pass filter time constants (figure **23**) Ud_Tc_Dn and Ud_Tc_Up are down time and up time delay of break point limits. The down time for the inverter should be fast to prevent commutation failures but for rectifier it need not be too fast during inverter fault there is a threshold limit for VDCOL (0.8), if the dc voltage reaches threshold value; current order is decreased down rapidly to predefined lower value to prevent the consecutive commutation failure during inverter side ac fault. The down time constant could be same for both stations. But the up time constant could not be, rectifier should restart before the inverter. So the up time constant for inverter should be higher than rectifier (mostly depends upon how strong the ac system is). Contrary, if the inverter restart first, it start build the counter voltage thus the dc current, might loose the current margin causes power reversal. This function prevents the commutation failures during the recovery. Obviously the valve stress is reduced.

2.10.1 Current limits of current order:

Maximum current is depends upon the thermal overload of valves.

Minimum current should be around 0.3 p.u. in order to avoid valve extinction and high valve voltage stress since the overlapping angle is directly proportional to the dc current. So very low dc current gives small overlapping angle causes voltage spikes at starting and ending of commutation combines together creates twice the voltage spike.

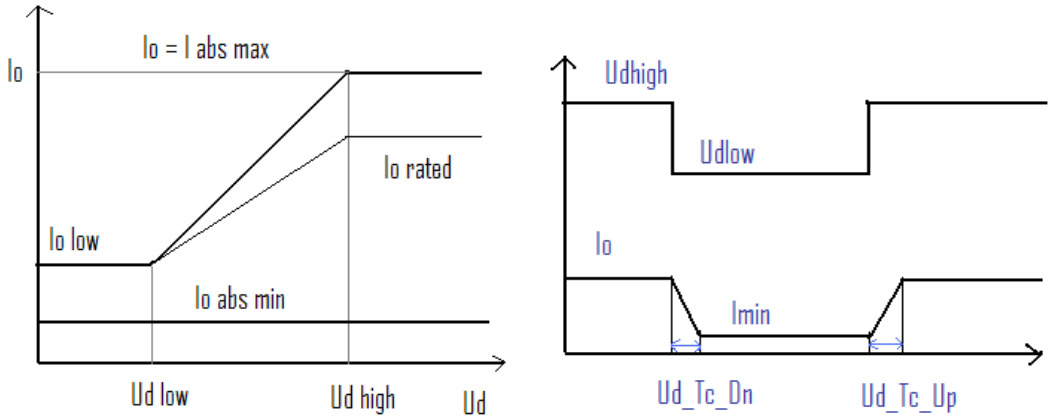


Figure 23 VDCOL characteristics with voltage and current limits

The power reversal could be obtained by increase the current order of the inverter higher than rectifier. In case of dc line fault, it is recommended that both converters should operate as inverter to make the fault current in dc line to zero as fast as possible. If there is no minimum alpha limit at inverter, it could also operate as rectifier by reduced alpha cause feeding of dc fault. Therefore, always minimum alpha at the inverter is limited to 110^0. However, rectifier could be operating as inverter for reason explained above. Inverter should have at least minimum counter voltage (i.e. cos(110)) to have current flow during start-up after fault with zero dc current.

2.11 Current control Amplifier (CCA):

The current control amplifier (figure **24**) is used as the main function which used to control the firing angle of the converter under steady state and dynamics of HVDC system. The current controller is basically a Proportional and Integral regulator. As we all know the proportional part helps to give fast response with respect to the feedback and integral part is a slower part which used to make steady state error zero. The current error (I_{order}-I_{dc}) is send as input to the PI regulator. It gives out alpha order as output to the converter firing control. Traditionally, rectifier will operate as current controller in order to have optimal operation point with reduced consumption of reactive power. Direct current is indirectly regulated by controlling the firing angle of the thyristor. The firing angle at rectifier station kept within a steady state range of ±2.5º by tap changer control. The ac voltage can be maintained constant by switching in and off of shunt capacitor and filter banks at nominal frequency. During steady state, current order I_{0LIM} from voltage dependent current order limiter (VDCOL) and measured dc current are same; hence the error of zero would be send to the saturated PI regulator in current control amplifier. In contrary, during transients I_{oLIM} would be varied as a function of dc voltage when the dc voltage hits the breakpoint of VDCOL, the error of I_{oLIM} and measured current will be sent to PI regulator with maximum limit (AMAX =164) and minimum limit (AMIN = 5). The max and min limit of CCA is determined by voltage control

amplifier. The output from the PI regulator would be change in alpha order which is directly proportional to the change in current. There is one more important function called alpha retard, it will be activated only when the dc line fault occurs. The current controller gives output of AMAX when dc fault happens.

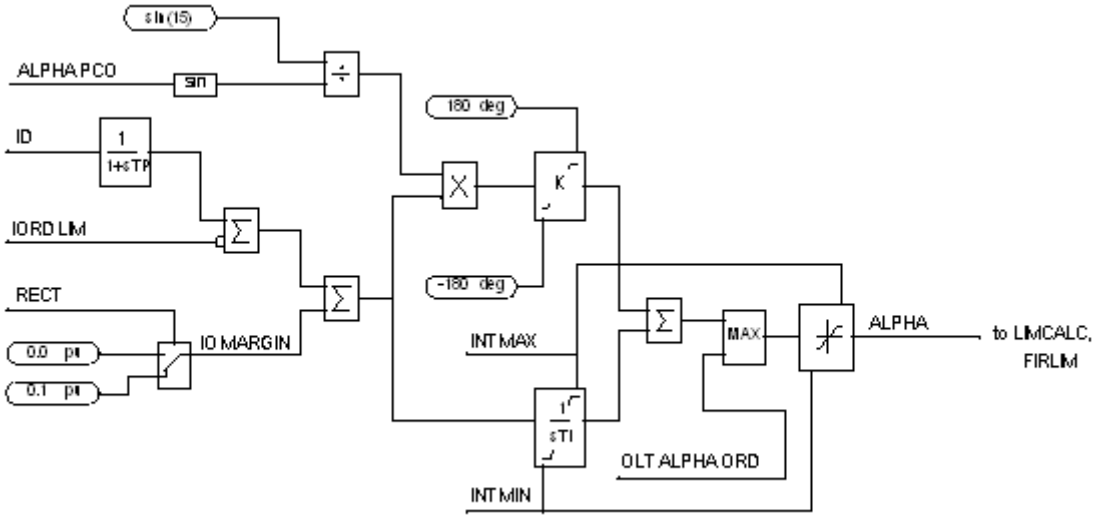


Figure 24 current control amplifier

In order to eliminate the non-linearization of the current controller, since the dc voltage dependent on change in firing angle i.e. cosα causes decrease in loop gain as increase in alpha; thus leads to instability of current controller. Therefore, linearization factor 1/sinα is added to improve the stability.

The current margin would be added based on controller (rect/inv).

The maximum limits of CCA integrator are output from voltage controller(VCA α_{order}) and α_{max} as well as minimum limits are RAMLα_{order}, U_{min}, overvoltage α_{order}, VCA α_{order} and α_{mininv}, these limits are selected depends upon the contingency of the system. If it is inverter, lower limit of alpha should be defined as 110 (α_{mininv}) and it could be reduced even 10 degrees further by commutation failure prevention function.

CCA set value would be activated at higher remaining voltage inverter ac fault by the function called Gamma0 explained below. CCA set value is nothing but α_{max} or VCA α_{order}. Once it is activated by gamma0 function, both limits max and min limit of integrator would be CCA set value.

During inverter side 3 phase to ground ac fault, the inverter voltage would collapse consequently abrupt rise of dc current. CCA maximum and minimum limits of PI regulator would be selected as output of voltage regulator and (α_{mininv} – Cfprev_angle).

When 3 phase ac fault occur at rectifier side, voltage would collapse consequently current decreased to zero. The maximum and minimum limits of CCA would be Alphamax and output of voltage regulator (α_{min} or RAML α_{order}).

In order to have a good dynamic operation of current controller, proper value of K_P and K_i should be selected. The proportional part is a faster part which executes the instantaneous change in feedback and integral part which reduces the steady state error. The proportional

and integral gain shall be chosen to give fast response and well damped oscillation with minimum overshoot.

2.12 Voltage controller:

The input for the voltage regulator (figure **25**) is measured direct voltage and reference voltage error. The maximum and minimum limits of PI regulator are determined by the direct current (ID low). If the direct current is less than Idlowref value, maximum and minimum limits are manipulated by normal dc voltage equation $\alpha = \cos^{-1}(Ud/Udio)$. On the other hand, Alphamax as maximum limit and lower limits are RAML alpha order, Umin, Alphamin inverter and overvoltage alpha order, these limits could be chosen depends upon the converter (rectifier/inverter) and contingency of the system.

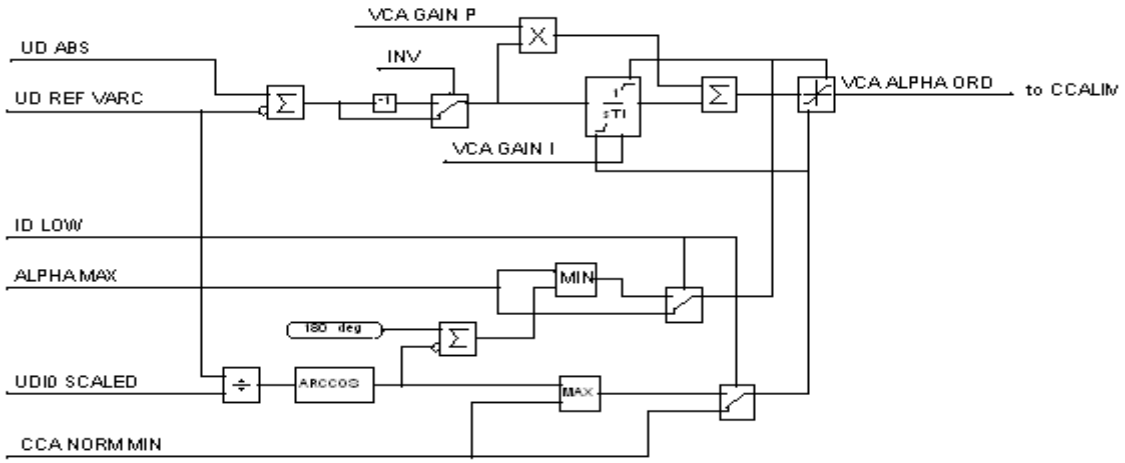


Figure 25 voltage control amplifier

The output of voltage regulator (figure **26**) is used as maximum and minimum limits of current control amplifier with respect to converter (rectifier/inverter). In normal voltage operation the reference voltage of the voltage regulator is set above the operating voltage in order to avoid the hunting between normal tap changer controller and voltage controller. The output from the voltage and angle reference calculation has multiplied by factor of one tap changer step for inverter voltage. This reference voltage is sent as input for voltage regulator. Even higher reference value shall be used in rectifier voltage controller in order to de-activate if it is active at inverter station.

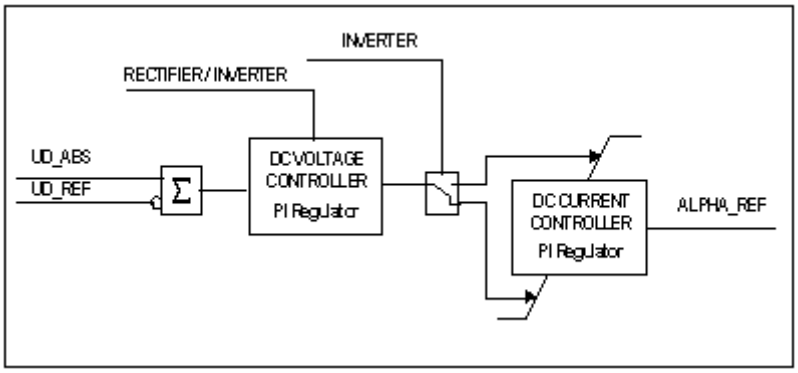


Figure 26 combined CCA and VCA

At reduced dc voltage operation, reference voltage could be set lower than operating voltage in order to reduce the dc voltage. It can be see that voltage regulator gives output of higher limit of integrator for inverter operation and lower limit for rectifier operation.

When 80% remaining voltage fault at inverter occurs, commutation failure happens due to the increase of dc current cause's higher overlapping angle. If it is high remaining voltage fault, commutation failure will be detected by the comparison of dc short circuit current and ac current, thus increase the γ by 15 degrees. Hence, it advances from alphamax position by 15 degrees. The dc current in the inverter would be reduced to zero by decreasing the voltage at the rectifier faster by current controller since voltage difference is reversed. The Alphaminref_inv will become 100 degrees from 110 degrees. It will be used as a minimum limit of integrator of voltage controller until the Idlow is activated and also Alphamax will be used as maximum limit of integrator until the Idlow is detected. The Idlow gives an output signal of 1 after 40ms delay from the instant it detects the Id_{meas} is less than 0.015p.u. Once the Idlow gives output of 1, maximum and minimum limits of the integrator will be based on the equation $U_d = U_{dio}*\cos\alpha$. Otherwise, maximum alpha will be increased further since there is no overlapping angle effects increase of dc voltage above rated at pole until the voltage error becomes zero.

$$\alpha_{max} = 180 - \cos\gamma \qquad (1.17)$$

Consequently, dc system recovery time will be increased.

Gamma0 function will be activated after 50ms time delay from when the inverter fault is detected gives Udlowinv output equal to 1, consequently CCA set output will be 1. So the CCA set value output will be voltage regulator output or Alphamax with respect to the Udabovezero signal. Just before the CCA set is activated, maximum limit of current controller integrator is output of voltage regulator and minimum limit is (alphamin_inv-Cfprev_angle). Hence the output of inverter current controller gives advanced alpha order in order to prevent the consecutive commutation failure. But it is not good to have higher commutation margin during the recovery, since it consumes more reactive power as current increases causes ac voltage reduction leads to voltage collapse or could take longer time to recover from the fault if the ac system is weaker. Therefore, the CCA set value will be used as both max and min limits of current controller integrator until the voltage error becomes zero to reduce the recovery time, CCA set value is nothing but Alphamax or output of voltage regulator as explained above.

During inverter side 3-phase ac fault, voltage at inverter would collapse hence sudden rise of dc current Idlow signal will select the maximum and minimum limits of Alphamax and

(Alphamin_inv-Cfprev). Cfprev is an output of commutation prevention failure function; this value could be maximum of 10 degrees. Same sequence happens as 80% rem. Voltage fault.

2.12.1 Control sequence in dynamics

When ~80% remaining voltage 3 phase ac fault occurs at rectifier, dc pole voltage decreased to ~80% of rated causes decrease in dc current since potential difference becomes reversed. Current controller will advance the firing angle in rectifier in order to increase the voltage to set the current equal to reference value. Once the alpha at rectifier hits the minimum limit ($U_{min,}$ minimum voltage required to turn on the valves), no further possible to increase the voltage in order to have constant potential difference between two converters. Therefore, converter will be recommended to operate in reduced voltage or reduced power. This forces the rectifier into constant voltage controller and inverter into constant current controller operation by increasing the gamma. As soon as fault cleared, ac voltage recovered to nominal value causes transient increase of current since the alpha is at minimum value. Hence the alpha increased transiently to a value higher than nominal to decrease the current then the alpha settles in nominal value. In this case RAML function is not activated because of higher impedance fault.

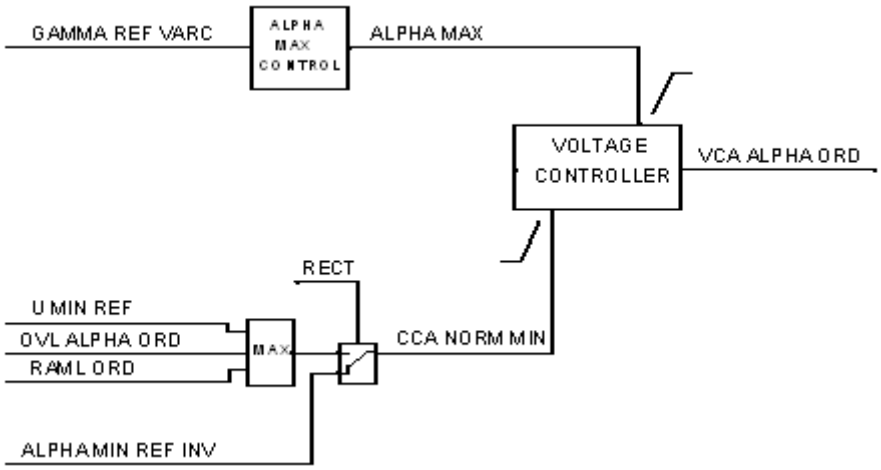


Figure 27 Maximum and minimum limits of VCA

When 3 phase ac ~10% remaining voltage fault occur at rectifier side, ac system voltage would collapse consequently current decreased to zero, alpha at rectifier hits the minimum limit. Collapsed commutation voltage would also leads to commutation failure at the rectifier. RAML function will be activated with a delay of 20ms from the instant measured dc voltage is less than RAML reference value. It increases the alpha to predefined value (ex. 60 for cables since higher charging current) and keeps it constant until the measured voltage is greater than reference value. When the fault clears, voltage would increase to nominal value results RAML alpha order ramp down to nominal value (ramp step depends upon the type of transmission, normally the value in the range of 0.2 deg/ms to 0.8deg/ms). It can be seen from the result, the alpha order will be increased transiently from 60 to 70 deg at fault clearing due to the abrupt increase of dc current. The current controller at inverter would try to advance the alphamax to set the reference value equal to measured value at starting. But the decreasing current due to reversed voltage difference retarding the alphamax thus the ac voltage at the inverter will increase. Once the Ud below reference value is detected by gamma0, activates the Udlow_inv after 50ms time delay. Thus the CCA set value gives alphamax output for both max and min limits of integrator in order to reduce the recovery time as same explained

in inverter ac fault. The ac voltage at inverter hits the maximum limit when the dc current goes to zero due to the switching capacitance.

We can conclude that during the inverter fault, α_{max} output as same as VCA α_{order} until Idlow is detected. The VCA α_{order} will be sent as input for CCA as max limit and min limit would be obviously α_{minINV}. In the rectifier side, output of VCA α_{order} is α_{minREC}; it will be used as CCA min limit and max limit will be obviously α_{max} in order to increase alpha above 90 transiently to decrease the fault current.

During the rectifier side ac fault, the output of VCA α_{order} is minimum limit of VCA i.e. RAML α_{order} or α_{minREC} (Umin). VCA α_{order} would be min limit and α_{max} as max limit of rectifier CCA.

In the inverter side, α_{max} would be the output of VCA α_{order}, it probably a max limit of inverter CCA and α_{minINV} as min limit until CCA set is not activated.

2.13 Alfamax inverter control:

This control is nothing but constant beta control in order to have positive slope in the current margin region to increase the stability of the current controller. If there is no positive slope, during the mode shift sudden change in current causes power oscillations in system. Therefore, constant gamma operation gives stability problem, if the inverter ac network is weak.

Since constant extinction angle characteristics could be written as

$$\alpha = \arccos(Xt * \frac{Id}{Udio} - \cos\gamma ref) \quad (1.18)$$

Increase in current will give negative slope; especially receiving end network is weaker leads to more number of crossing point's results instability.

The key is constant alpha or beta operation gives positive slope.
The direct voltage can be calculated by using the equation

$U_d = 0.5\ U_{dio}\ (\cos\gamma + \cos(\gamma+\mu))$ (1.19)

$\gamma+\mu = \beta.$ (1.20)

Therefore,

$$\cos\beta = \arccos(\cos\gamma - 2 * \frac{U_d}{U_{dio}}) \quad (1.21)$$

$$Ud = Udio(\cos\gamma - (dx - dr) * \frac{Io}{IdN} * \frac{UdioN}{Udio}) \quad (1.22)$$

Insert equation (1.7) in (1.6), will get

$$\beta = \arccos(\cos\gamma - 2 * dx * \frac{Io}{IdN}\frac{U_d}{U_{dio}}) \quad (1.23)$$

Where, dr is neglected since resistance will not play any role in commutation of valves.

The stabilization could be introduced if a contribution derived from the difference between current order and measured current is added when calculating beta. The gain and time constant of this added regulator shall be varied to get better stability.

$$\beta = \arccos(\cos\gamma - 2 * dx * \frac{Io}{IdN}\frac{U_d}{U_{dio}} - K(Io - Id)) \quad (1.24)$$

$Alphamax = 180-\beta$ (1.25)

During the transients γ will be increased by commutation failure prevention function based on how severe the fault is. If it is high remaining voltage fault, commutation failure will be detected by the comparison of dc short circuit current and ac current, thus increase the γ by 15 degrees. Otherwise, if it is solid fault gamma will be increased based on the comparison of fault voltage and pre-fault voltage. It is explained briefly in commutation failure prevention function.

2.14 Rectifier alpha min limiter (RAML)

When there is fault in ac system at rectifier station, ac voltage will drop down, thus the dc voltage at pole decreases. But if it is cable, voltage after the smoothing reactor will decrease slowly (large capacitance). This reduces the dc current to zero faster. Therefore the current controller will decrease the alpha to minimum value (5 degree). When the fault clears, voltage will bring back to normal value instantaneously; it leads to high dc current if the alpha is still in minimum value at fault clearing time.

There is two different function Uac_min_hold and Uac _max _hold. This function detects the maximum and minimum ac voltage and compared with nominal reference value (0.6) and triggers the alpha to predefined minimum value (ex. 60 degrees). Uac_min_hold function is used to detect the unbalanced fault and Uac_max_hold function is used to detect the balanced fault.

After the fault, alpha is decreased to nominal value by 0.2deg/ms.

This function forces the inverter into current controller during rectifier shunt fault and recovery to avoid consecutive commutation failures.

2.15 Commutation failure prevention control:

It is not possible at all to avoid commutation failure at inverter when sudden increase of dc current and decrease of commutating voltage. However, it could be possible to avoid subsequent commutation failures during the high remaining voltage fault at inverter ac network by advancing the firing angle in order to increase the commutation margin. This makes the system could transfer power during disturbance. There are two possibilities for commutation failure such as commutation voltage reduction or distortion and phase angle jump at unbalanced fault. Therefore, two different sets of control function used to avoid consecutive commutation failure caused by balanced and unbalanced fault. Since the reduction of voltage at single phase fault is not severe as three phase fault, but creates phase shift. So the unsymmetrical fault is detected by zero sequence voltage detection, then it compared with pre-defined voltage level, if zero sequence voltage is lower than predefined level, it advances the firing angle and keeps it for whole fault duration. Symmetrical fault will not give zero-sequence, therefore it directly compared with predefined value and voltage (prefault voltage – fault voltage) difference, it will decrease the firing angle if the difference is higher than predefined value. In brief, the three phase voltages are transformed to dc quantity by alpha-beta transformation; it gives dc output only when the three phases are symmetrical. However, three phase fault will not decrease the voltage instantaneously in all the phases, it decrease the voltage phase by phase hence creates negative sequence the same happens when clearing the fault. Therefore, oscillations will occur in alpha-beta output. It is not possible to compare the oscillating waveform with pre-fault voltage, so max-hold function is used here to keep the maximum value for half cycle.

Commutation failure is more often detected when there is higher dc current compared to ac current, since the short-circuited dc grid effects open circuited ac grid for $2/6^{th}$ time period of one cycle.

2.16 Tap changer control:

The purpose of Tap changer control is to maintain the delay angle alpha in a certain range at rectifier station. If the alpha reduces below the predefined value, it starts increase the voltage by varying the number of turns in the primary side to keep the alpha in certain range for fast controlling of current. Also, if alpha increased above a certain predefined maximum value then the tap changer would decrease the voltage to keep the alpha within the limit.

In inverter station, tap changer control maintains the dc voltage equal to reference voltage. Normally gamma is kept as constant for proper commutation. Any increase or decrease in dc voltage will be controlled by tap changer. Since tap changers would take more time to control the converter voltage than current or voltage controller, dynamic interaction between both controllers can be avoided.

2.17 Inverter gamma0 start function:

If the measured voltage is lower than the predefined minimum value of 0.8p.u. This function indicates an output of 1 after a certain delay. It will be reset to 0 after the voltage recovered to nominal value with certain time delay. Gamma0 function is used only under ac faults, if the measured voltage is less than reference value for a certain time period would give udlowInv output as 1. It activates the CCAset value. CCA set value could be an output of voltage regulator alpha order and Alphamax with respect to measured voltage whether it is above or below zero.

Gamma0 function is mainly used to recover the dc system as soon as possible with reduced consumption of reactive power. As soon as inverter side ac fault occurs, Udlowinv value will be activated after a 50ms time delay with delay off time of 100ms. It will be reset to zero after 150ms time delay from the instant voltage recovered.

If gamma0 function is not activated, the lower limit of PI regulator of current controller would be alphamininv; hence it consumes more reactive power causes ac voltage reduction leads to collapse especially if the ac system is weaker. To avoid this, during the recovery it recommended to operate the inverter in Alphamax position.

2.18 Equidistant firing control:

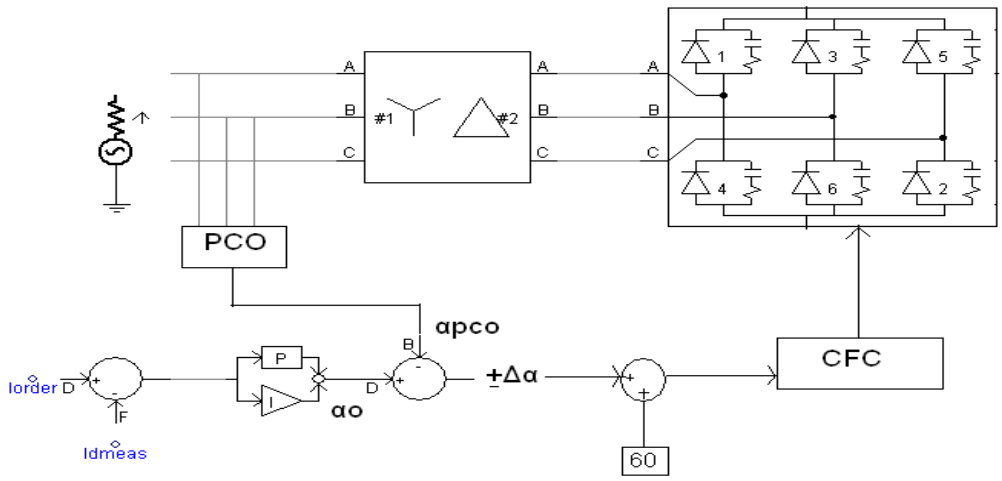


Figure 28 Equidistant firing control

Equidistant firing control (figure **28**) method of firing the valves will determine the equal distance between two firing. The converter firing control (CFC) is normally open loop control. It provides firing of each valves of 12 Pulse Bridge with delay of 30 degrees between each firing. It is always synchronized with ac voltage before firing using phase locked oscillator. Equidistant firing control automatically adds the change in angle to 30 degrees ($30\pm\Delta$), 60 degrees for 6 pulse bridge circuit. Typically, the change in firing angle is determined by current control amplifier.

2.17 Recovery of AC and DC system faults:

2.17.1 AC system faults:

The ac system fault could occur both rectifier and inverter station. The fault at the rectifier station would suddenly collapse the voltage at bus bar, since the thyristor is unidirectional device the dc current goes to zero immediately. Therefore, no power would be transferred to sending end unless the fault is cleared. Also fault at the inverter station cause counter voltage collapse at inverter ac bus, resulting sudden rise of dc current causes increased overlapping angle reduce the commutation margin. Hence commutation failure occurs .Commutation failure is nothing but short-circuited dc grid and open circuited ac grid. Therefore, no power transfers by the valves into ac network. These energy losses due to these faults should be recovered as fast as possible to prevent transient instability of synchronous machines and energy loss to customers.

The recovery of the dc system is mainly depends upon how strong the ac network is. If the SCR of the receiving end ac system is very low, more difficult in system recovery without commutation failure.

2.17.2 DC system faults:

Dc line faults are most probably dc line to ground faults, cable fault, station equipment faults and insulation breakdowns. For some special reasons the dc breakers are not used as main

equipment to clear the fault, even though the dc circuit breaker has resonance circuit to achieve zero crossing for arc absence opening of switch. The HVDC control system plays main role in clearing of dc fault. The function called retard, as soon as the dc fault is sensed the retard function will be activated. The retard is nothing but operating the rectifier with high alpha i.e. inverter to send energy back to the ac system to make zero current at dc system.

If there is a fault in pole one dc line of bipolar system, it will be operated as a monopolar system with reduced power. During the de-energization the of rectifier station, it is acting as pure inductance. If the rectifier station ac system is weak, it could be possible for commutation failure at rectifier.

In some cases, the recovery of pre-fault voltage may not be recovered successfully due to some reason like insulator failure. The dc faults are detected by derivatives of the dc voltage and current if it is still negative after fault clearing; it would be good to restart with reduced voltage.

2.17.3 Commutation failure:

Commutation failure is inevitable at inverter during disturbance at ac system. Mostly the inverter would always operate at constant beta; let's say gamma reference value at normal operation is around 18 degrees in order to have certain negative valve voltage to deionize the outgoing valve. The minimum extinction angle need to turn off the valves is ~8 degrees. This could not be higher than 18 degrees for reducing the consumption of reactive power and valve voltage stress. Most probably the commutation failures will take place at the inverter side during ac faults since low commutation margin at inverter compared to rectifier. The commutation failure could be expected at inverter side at 90% to 85% remaining voltage fault at this margin. If the margin is increased bit, it could withstand up to even some lower remaining voltage fault. The commutation voltage of the converter valves nothing but phase to phase ac voltage at converter transformer. Commutation failure would take place not only due to voltage reduction and also depends on phase shift of voltage. The leading (advanced zero crossing) voltage phase shift will reduce the commutation margin leads to failure. The phase shift will occur not only for unbalanced fault, it also depend on the ac system active power injection reduction during fault.

In general, weaker receiving ac system would cause more commutation failures when remote ac system fault happens due to higher reduction of commutation voltage. The recovery time after the fault clearing will be longer for low SCR than high SCR system. Since fast recovery of dc system with weak ac system causes voltage instability resulting consecutive commutation failures during recovery. Hence, very weak systems may be provided switching capacitors or SVC to avoid voltage instability.

Most probably, commutation failure happens at the star winding transformer connected valves of 6 Pulse Bridge at high remaining voltage ac fault. However, the valves in the lower bridge commutating normally causes short circuit of dc grid for $2/6^{th}$ time period since the valve fails to commutate once, it will get next chance to commutate after a cycle or 360 el degrees. Most often the commutation failure happens in star winding connected bridge but not in delta connected bridge. It mainly depends upon the type of transmission, ac system strength and how fast the commutation failure prediction is.

The well defined control strategies shall be included to have good recovery of dc system without following fault consecutive commutation failures. The main control used for proper recovery of dc system after fault clearing is voltage dependent current order limit (VDCOL). The purpose of this control is to limit the current order as a function of the reduction of direct

voltage. This reduces reactive power consumption during recovery hence reduce the risk of commutation failures.

2.18 Conclusion:

This chapter gives some introduction of traditional control system of HVDC classic. The consequences of ac and dc faults of HVDC system connected to weak ac network. Moreover, the basics of commutation failure and prediction of commutation failure was covered. In the next chapter, ac/dc system interaction of HVDC link connected to weak network will be analyzed with existing control parameters.

3.0 Performances scan of HVDC classic models:

3.1HVDC Modelling in PSS/E*:*

3.1.1Introduction to PSS/E:

Power System Simulator for Engineers (PSS/E), which is kind of software using for studies on power system transmission network and generation in steady state and dynamic conditions.

3.2 Power Flow data:

In this paragraph, data required for power flow in steady state analysis is described.

Figure 29 HVDC model diagram in PSS/E

3.2.1Bus data:

Each bus data should be recorded in PSS/E. bus data includes not only basic bus properties but also shunt capacitance or reactor connected to the bus.

Bus data format:
I, 'NAME' , BaseKV, IDE,GL,BL,AREA,Zone,VM,VA,owner

I ,	Bus number
NAME	Name of the bus
BaseKV	Base voltage
IDE	Bus type, whether load bus, generator bus or swing bus.
GL	Active component of shunt admittance to ground
BL	Reactive component of shunt admittance to ground
Area	Area of the bus
Zone	Zone number of the bus
VM	Bus voltage magnitude in p.u.
VA	Bus voltage phase angle
Owner	Owner number

3.2.2 Load data:

Each network bus at which load should be represented.
Load data format:
I, ID, STATUS, AREA, ZONE, PL, QL, IP, IQ, YP, YQ, Owner

I	Bus number
ID	Number of loads connected in bus
STATUS	whether it is in service or out of service
AREA	Area number

ZONE Zone number
PL Active power component of constant MVA load
QL Reactive power component of constant MVA load
IP Active power component of constant current load
IQ Reactive power component of constant current load
YP Active power component of constant admittance load
YQ Reactive power component of constant admittance load
Onwer Owner number

3.2.3 Generator data:

The generator data should be recorded in PSS/E

Generator data format:

I, ID, PG, QG, QT, QB, VS, IREG, MBASE, ZR, ZX, RT, XT
I Bus number
ID Number of generators connected
PG Active power generation
QG Reactive power generation
QT,QB Maximum and minimum generator reactive power output
VS Regulated voltage in p.u.
IREG Extended bus number
MBASE Total MVA Base
ZR,ZX Complex machine impedance in p.u.
RT,XT Transformer impedance in p.u.

3.2.4 Branch data:

Branch data format:

I, J, CKT, R, X, B
I Branch from bus number
J Branch to bus number
CKT number of branches
R branch resistance in p.u.
X branch reactance in p.u.
B Total branch charging suceptance in p.u.

3.2.5 Fixed shunt data:

Fixed shunt data format:

I, Bus name, ID, Status, G-shunt, B-shunt
I Bus number
ID number of shunt element
Status In-service or out of service
G-shunt Active component in MW
B-shunt Reactive component in MVAr

3.2.6 Two-terminal DC line data:

Record 1:
I, MDC, RDC, SETVL, VSCHD, VCMOD, RCOMP, METER,
I DC line number
MDC Control mode, whether blocked(0), power(1) or current(2)

RDC DC line resistance in ohms
SETVL Current or power demand
VSCHD Scheduled compounded DC voltage
VCMOD Mode switches dc voltage, if the inverter voltage falls below certain limit, mode switch to current control from power control mode.
RCOMP Compounding resistance in ohms, 0% resistance holds the dc voltage in inverter, 50% resistance holds the constant dc voltage in centre of dc line, 100% to control the rectifier end dc voltage.
METER Rectifier or inverter

Record 2:
IPR, NBR, ALFMX, ALFMN, RCR,XCR, EBASR, TRR,TAPR, TMXR, TMNR,

IPR rectifier converter bus number
NBR Number of bridges in series
ALFMX,ALFMN Alpha Max limit and Alpha Min limit
RCR Rectifier commutating transformer resistance per bridge
XCR Rectifier commutating transformer reactance per bridge
EBASR Rectifier primary base ac voltage
TRR Rectifier transformer ratio
TAPR Rectifier tap setting
TMXR Maximum rectifier taps setting
TMNR Minimum rectifier taps setting
Same format for inverter except alpha instead gamma.
The power flow data are loaded in PSS/E in a raw file format. Raw file is nothing but power flow input data file see appendix (**8.4**). Solve the raw file using Newton rapson method.

The HVDC model representation in PSSE is shown in figure (**29**). The generator at both station are represented as infinite source behind the short-circuit impedance with PSSE dynamic generator model GENCLS. The short circuit ratio at both converter terminals are 3, representing as weak ac network. The fixed shunt compensators are connected at converter bus which produce reactive power = 0.5 active power. The load flow data are called from raw file, such as bus data, branch data, generator data, fixed shunt data, and two-terminal dc line data. The dynamic data are called from dyr file shown in appendix (**8.5**), which has dc line data such as rated dc voltage, current, inductance of the line/cable, capacitance of the line/cable and smoothing reactor value. The main circuit, dc system and control systems are called by(software independent) dll file, which contains program written in fortran language.

Ac/dc system interaction studies are mainly about the recovery of the system after the disturbance, voltage stability and over voltages, especially HVDC system connected to weak network. However, the rms models are not used for dynamic performance studies, though selection of control parameters should be verified by dynamic performance studies. The good dynamic performance of HVDC system could be achieved by tuning of CCA and VDCOL control parameters.

HVDC system stability is measured by how fast the dc system recovered from the ac or dc faults.

Recovery time is defined as the time from fault clearing to the instant 90% of the pre fault power is restored. In general, recovery time depends on

- the characteristics of the dc and ac system

- DC control strategy

The characteristics of ac/dc system are nothing but strength of the network, dc line parameters i.e. line inductance, capacitance (especially if its cable), smoothing reactor and transformer reactance. The rate of power recovery affects system stability, since after a long period of ac system disturbance, fast recovery of power may cause voltage instability if the inverter ac system is weaker; effects subsequent commutation failures. In particularly, low SCR system requires slow recovery of power to ensure the ac system voltage maintained at satisfactory level.

Short circuit ratio (SCR):

The ratio between three phase short circuit MVA to dc power. Stronger the system lower the ac system impedance and weaker the system higher the impedance.

Effective short-circuit ratio (ESCR):

The shunt capacitors including ac filters connected at ac terminal of dc link can increase the effective ac system impedance considerably. Effective short circuit ratio is defined as

$$\mathrm{ESCR} = \mathrm{SCR} - \frac{\mathrm{Qc}}{\mathrm{PdN}} \tag{2.1}$$

Where, Qc is the three phase fundamental MVar
PdN is nominal rated dc power.

Voltage stability:

Voltage stability of the power system is, if any fault occurs; it is required to maintain the voltage within acceptable limits in all the connected buses except faulted bus. Otherwise, significant effects on the local ac network leads to voltage instability for some reasons like higher impedance line, or increase in load demand. In particular, the higher line impedance builds higher inductive voltage drop across the line, consequently voltage instability would occur if there is not enough capacitive reactive power to compensate. Thus, Voltage stability also mainly depends upon system strength.

The voltage stability is measured by factor called voltage stability factor. The voltage factor is defined as incremental change in voltage due to small reactive power injection in to commutation voltage bus bar at rated dc power.

$$VSF = \frac{dU}{dQ} \tag{2.2}$$

The control parameters of current control amplifier and VDCOL have to be optimized to have good response during transient operation. There are some specific time of dc system recovery based on the transmission types (line/cable). All benchmark models are designed with SCR of 3 for both sending and receiving station. The damping angle used for both station ac systems is 80 degrees. In order to optimize, following tests have to be investigated.

3.3 Benchmark cases:

configuration	Overhead Line transmission	Cable Transmission	Back to Back
	DC Power DC	DC Power DC	DC Power DC

	(MW)	Voltage (KV)	(MW)	Voltage (KV)	(MW)	Voltage (KV)
Monopolar, Ground return	3600	800			600	167
	3000	800	800	500		
	2500	800			500	139
	2000	660				
	1575	660				
	1500	500	500	500	150	42
	1000	500				
Monopolar, Metallic return	3600	800				
	3000	800	800	500		
	2500	800				
	2000	660				
	1575	660	500	500		
	1500	500				
	1000	500				
Bipolar	7200	800	1600	500		
	6000	800				
	5000	800				
	4000	660				
	3150	660	1000	500		
	3000	500				
	2000	500				
Monopole,Midpoint grounded	-	-	1000	900		
			600	900		
2XMonopole, ground return	7200	800	1600	500		
	6000	800				
	5000	800				
	4000	660				
	3150	660	1000	500		
	3000	500				
	2000	500				

Tabel 1 Benchmark models in PSS/E

3.4 Test cases

1) 100ms AC fault at the inverter side with 10% remaining voltage
2) 100ms AC fault at the rectifier side with 10% remaining voltage
3) 100ms AC fault at the rectifier side with 70% remaining voltage
4) 100ms AC fault at the inverter side with 70% remaining voltage
5) 0.92 p.u. DC power step for 100ms
6) DC fault for 100ms at node1 nearer to rectifier.
7) DC fault for 100ms at node1 and restart with reduced (80%) voltage.
8) Inverter side AC fault with range of %remaining voltage (95% to 10%)
9) 3 degree gamma step at the inverter.

3.4.1 3-phase to ground AC fault:

10% remaining voltage ac fault is used to investigate the transient stability of the ac system and how fast the dc system recovers the power to consumer after the fault clearance. The recovery should be smoother without any subsequent commutation failure. Also, one more important thing to note that fault current should be limited within permissible limits and within certain time.

~70% remaining voltage fault is to investigate the performance under reduced voltage operation i.e. current controller at inverter and U_{min} controller at rectifier.

	Fault type	Transmission type	Recovery time	
			Rectifier	Inverter
1	3-phase to ground-10% remaining voltage	Overhead line	100ms to 120ms	120ms to 150ms
2	3-phase to ground-10% remaining voltage	Cable	100ms to 150ms	120ms to 250ms
3	3-phase to ground-10% remaining voltage	Back to back	90ms to 120ms	120ms to 150ms
4	Dc line fault nearer to rectifier	Overhead line	120ms to 150ms	-
5	Dc line fault nearer to rectifier	cable	120ms to 200ms	-

Tabel 2 Power recovery time of different transmission types

3.4.2 Commutation failure:

Commutation failure could be expected at 90% to 80% remaining voltage ac fault at inverter for overhead lines and for cable, it happens at 95% to 90% remaining voltage ac fault.

3.4.3 DC line fault:

The dc line fault applied for 100ms, the order retard will be activated after 5ms from the fault applied instant and shall be de-activated after 50ms from fault clearing instant. The fault is applied nearer to the rectifier station.

3.4.4 Dc line fault and recovered with reduced voltage:

In some cases, faults are caused by insulator failures so recovered with full voltage in not possible. This is same as dc line fault, but recovered with 80% of nominal voltage.

3.4.5 Power step:

The negative power step is applied for 500ms, power decreased to 0.92p.u. at 0.1s and back to nominal at 0.6s This is to investigate the performance of the active power controller. The expected response time is between 70ms to 100ms.

3.4.6 D.C. voltage step:

The voltage step applied for 300ms, voltage decreased to 80% of nominal value at 0.1s and step back to nominal value at 0.4s. This is to investigate the performance of the voltage controller. The response time is typically in the range of 50ms to 100ms.

3.4.7 Gamma reference step:

The gamma step is applied for 500ms, positive 3 degree gamma step applied at 0.1s and step back to nominal at 0.6s. This is to investigate the performance of the Alphamax controller. The normal response time is in the range of 50ms to 100ms.

3.5 AC fault at inverter:

3.5.1 The basic control operation (fault at inverter ac system)

When 70% remaining voltage 3-phase ac fault to ground applied at the inverter end, suddenly dc voltage at the inverter end decreased but the dc voltage at the line would not be decreased as fast as pole voltage due to line capacitance. This potential difference builds a immediate rise in dc current. As a consequence, overlapping angle increases, alpha at the inverter could not change immediately to prevent the commutation failure hence shrink the margin of negative voltage for commutation of valves. At certain current, commutation failure occurs at inverter results abrupt increase of direct current due to short-circuited dc grid for $2/6^{th}$ period of 6 pulse bridge. This surge current will be limited by smoothing reactor. If the dc voltage at inverter reaches the VDCOL break point voltage, current order will be reduced to predefined value after down time constant of low pass filter as well as current order will be recovered to nominal value with different time constant as increased dc voltage hits breakpoint after clearing of fault. After a travelling time, dc line voltage at the rectifier decreases, but the internal dc voltage is constant. This potential difference builds an abrupt rise of rectifier current. Consequence, current controller at rectifier starts increase of alpha in order to decrease the current by reducing the pole voltage at rectifier to maintain equal voltage difference between both converters. VDCOL will start its action when the dc voltage at rectifier hits the threshold value. Increase in current makes a converter to consume more reactive power as a consequence ac voltage at rectifier decreases. Then the internal dc voltage at the rectifier decreases, current decreases and consumption of reactive power decreases .Thus, the ac voltage at the bus increases. But if the system is very weak, the decrease in voltage and increase in dc current make commutation failure at the rectifier. But the commutation failure could be prevented at rectifier proper value selection of CCA gain and VDCOL time constants.

If it is solid fault, collapse of commutating voltage leads to commutation failure. The transient current due to commutation failure will increase to 2 p.u. if it is line transmission; cable discharge current reaches maximum value of 8 p.u. at inverter. Commutation failure prevention function advances the firing angle alpha to its minimum limit of 110^{o} in order to increase the extinction angle to prevent consecutive commutation failure during the recovery. The alpha at rectifier also transiently increases above 90 to decrease the increase of dc

current. Alpha order at rectifier increased to maximum value of around 140 to decrease the increase of dc current. Rectifier VDCOL helps to decrease the current order to predefined value when the threshold dc voltage value reaches. The inverter will control the current to current order minus current margin.

3.6 Ac fault at rectifier station:

3.6.1 Basic control operation (rectifier side ac fault)

When there is voltage collapse at rectifier station ac system, suddenly voltage at the pole would decrease but not in after the smoothing reactor(inverter voltage), this voltage difference decrease the current rapidly to zero (since the current cannot reverse).As soon as the current start decreasing, current feed back sent to the current controller and it reduces the alpha to minimum value to increase the current to match the predefined reference .Then dc voltage reaches the break point ,VDCOL action forced to decrease the Iorder to predefined lower value. RAML function would be activated to increase the alpha to predefined maximum value when it hits the reference value; this prevents dc surge current at fault clearing. After the travelling time, voltage at the inverter node start decrease but not the pole counter voltage since the ac voltage is constant, results decrease in current .This decrease in current shall reduce the reactive power consumption hence voltage at the ac bus increase.

If dip in ac voltage is 70%, then the dc current would decrease as described above, results current controller at rectifier hits the minimum alpha limit to increase the dc voltage hence dc current to provide constant voltage difference. Current controller at the rectifier is valid until the alpha >alpha min limit. Once the alpha hits the minimum limit, no further increase of voltage is possible. Current control switch to inverter since we have large range of voltage at inverter and rectifier operate at alpha min or constant voltage.

3.7 DC line fault at rectifier end:

When dc line to ground fault occurs at the rectifier end, will collapse the dc voltage results abrupt increase of current effects higher consumption of reactive power. The short circuit shall be limited by smoothing reactor. As soon as the fault is detected, alpha retard will be activated to operate the rectifier at higher alpha of 164^0 to reverse the pole voltage hence dc current. Inverter also advances the alpha to minimum alpha limit of inverter 110^0. Technically, both converters operating as inverter to discharge the line or cable as fast as possible to extinguish the dc current. The retard will be released to normal value by ramp step after clearing the fault. The VDCOL increase the current to nominal current after the removal of fault.

3.8 Control sequence during step change

3.8.1 Gamma reference step:

Gamma reference step is to investigate the performance of the Alphamax controller at inverter. The proper value of gain should be selected to have good dynamic behavior.

$$\alpha_{max} = 180 - \arccos(\cos\gamma_{ref} - 2 * d_x * \frac{I_o}{I_{dN}} \frac{U_{dioN}}{U_{dio}} - K(I_o - I_d)) \qquad (2.3)$$

When apply 3 deg positive gamma step from 17 deg, alphamax will be suddenly advanced by 3 deg consequently voltage decreases hence current increases. Transiently gamma would decrease back to 16 deg by the term $K(I_o - I_d)$ in the alpha-max controller. The intention with

this term is add a positive slope at the operating point in Ud-Id diagram. The applied 3 degrees in gamma step will provoke a temporary current rise which activates this term. After a travelling time, increased rectifier current would increase the alpha in order to reduce the dc voltage to decrease the current consequently gamma starts increasing to the reference value. After 100ms gamma settle down to reference value of 20 deg and alpha increased to 18 deg from 15 deg. And at 0.6s the gamma reference step back to nominal value of 17 deg results undershoot in the dc current because of the overshoot in dc voltage. It back to steady state with response time 100ms (see section.**4.6.1.5**).

3.8.2 Power step:

To investigate the performance of the active power controller at rectifier, the power step of 0.92p.u. applied at 0.1 seconds, active power controller at rectifier sends the current order to the inverter to maintain the current margin and the rectifier waits for send back signal from inverter to change the current order (the transmission delay of 70ms back and forth). The activated current order at inverter start reduces current cause's alphamax controller decreases the gamma in order to increase the current as well as current controller at rectifier starts decreasing alpha to increase current transiently. After 70ms of telecommunication delay i.e. send back signal from inverter, dc current reduced to 0.92 p.u. then rectifier alpha increases transiently to 21 degrees and settles down in 17deg. Gamma at inverter would decreased transiently and send back to nominal value by alphamax controller. Once the power step back to nominal value at 0.6s; transiently reduces the alpha to 11 deg from 17deg at 0.92p.u. and send back to nominal value after 100ms. Also gamma at inverter decreased to 13 deg transiently and sends back to nominal value. Especially for the long cable with weak receiving network should have high gamma margin at inverter in order to avoid commutation failure during power step.

The power step response time is around 80 to 100ms. The response is well damped with minimum overshoot and controlled (see section **4.6.1.4**).

3.8.3 Dc voltage step:

In order to investigate the performance of the voltage control amplifier, the negative step in dc voltage has to apply, and also gamma reference shall be lowered to avoid hunting between Alphamax and VCA. The proper value of K_p and K_I shall be selected to attain good dynamic performance.

Under steady state, U_{dref} in voltage controller is set higher than U_{dN} in order to prevent hunting between alphamax and voltage controller. The output from the voltage and angle reference calculation has multiplied by factor of one tap changer step for inverter voltage. This reference voltage is sent as input for voltage regulator.

In order to investigate the voltage controller response, required to set the multiplication factor equal to 1 instead 1.025 to have correct voltage response output. Otherwise, the voltage response output would be 0.025 times higher than the step applied.

The response time of voltage controller is 50ms to 100ms. The response is well damped with minimum overshoot and controlled (see section **4.6.1.6**).

3.9 Control Parameters (default):

3.9.1VDCOL (Voltage dependent current order limiter)

No.	Control Parameters	Common values	BTB (strong AC network)	OH line (strong AC network)	Cable (strong AC network)	BTB (weak AC network)	Long OH line	Cable (weak AC network)
1	VdColFiltGain	1.0						
2	UdTcUpRe	0.02	0.02	0.04	0.02	0.02	0.04	0.02
3	UdTcDnRe	0.015	0.02	0.015	0.07	0.02	0.015	0.07
4	UdTcUpInv	0.05	0.05	0.04	0.04	0.05	0.04	0.055
5	UdTcDnInv	0.015	0.005	0.015	0.001	0.005	0.015	0.001
6	VdColFiltMax	1.0	-	-	-	-	-	-
7	VdColFiltMin	0	-	-	-	-	-	-
8	IoAbsMax	2	-	-	-	-	-	-
9	IoAbsMin	0.1	-	-	-	-	-	-
10	IoLim	0.345	-	-	-	-	-	-
11	UdLowParamRe	0.25	0.25	0.15	0.2	0.25	0.15	0.2
12	UdLowParamInv	0.25	0.25	0.15	0.3	0.25	0.15	0.3
13	UdHigh (rectifier)	0.75	0.8	0.8	0.5	0.8	0.8	0.5
14	UdHigh(Inverter)	0.75	0.8	0.8	0.9	0.8	0.8	0.9
15	ConstLim	0	-	-	-	-	-	-

Tabel 3 VDCOL parameters

3.9.2 CCA (current control Amplifier)

No.	Control parameters	Common values	BTB(strong AC network)	OH line (strong AC network)	Cable (strong AC network)	BTB (weak AC network)	Long OH line	Cable (weak AC network)
1	CcaLinAlpMax	164	-	-	-	-	-	-
2	CcaLinAlpMin	5	-	-	-	-	-	-
3	CcaLinMax	1.0	-	-	-	-	-	-
4	CcaLinMin	0.3	-	-	-	-	-	-
5	Sin_15_deg	0.25882	-	-	-	-	-	-
6	CcaKp	2.8	2.5	2.8	1.3	2.5	2.8	2.5
7	CcaGain	23	30	20	50	23	30	21
8	CcaTi	0.01	-	-	-	-	-	-

Tabel 4 CCA parameters

The control parameters shown above are used to simulate the HVDC classic benchmark models which are in appendix. The suggested transient simulations are done to analyse the dynamic performance of the HVDC classic control system. The shunt faults are applied at both rectifier end and inverter end with different voltage dips.

The shunt fault impedance with respect to remaining voltage could be calculated by using the formula,

$$Uf\angle\phi = \frac{Zf}{Zf + Zs} \tag{2.4}$$

Where, Uf is remaining voltage

Φ is phase angle jump during fault

Zf is fault impedance
Zs is ac system impedance.

The above mention test cases (see section **3.4**) have been done. The overhead line transmission and back to back transmission cases justified almost the PSCAD results but the cable cases did not. The recovery time of the dc system for rectifier ac fault was bit faster(less than 100ms) compared to the PSCAD results for both overhead lines and cable cases, in reality it should be more than 100ms. And, when 3-phases to ground fault applied at inverter for cable cases, dc system does not recover after fault clearing and commutation failure happened at rectifier causes dc current oscillation in dc system shown in figure **31**. Also commutation failure occurred for some cases when dc line fault applied near to the rectifier shown in figure **32**. Hence, the circulating dc current will be available in dc system causes difficult to clear the fault. The dc line fault will be applied only near to rectifier not to the inverter since the short circuit of dc line close to inverter will decrease the dc current to zero due to reversed voltage difference.

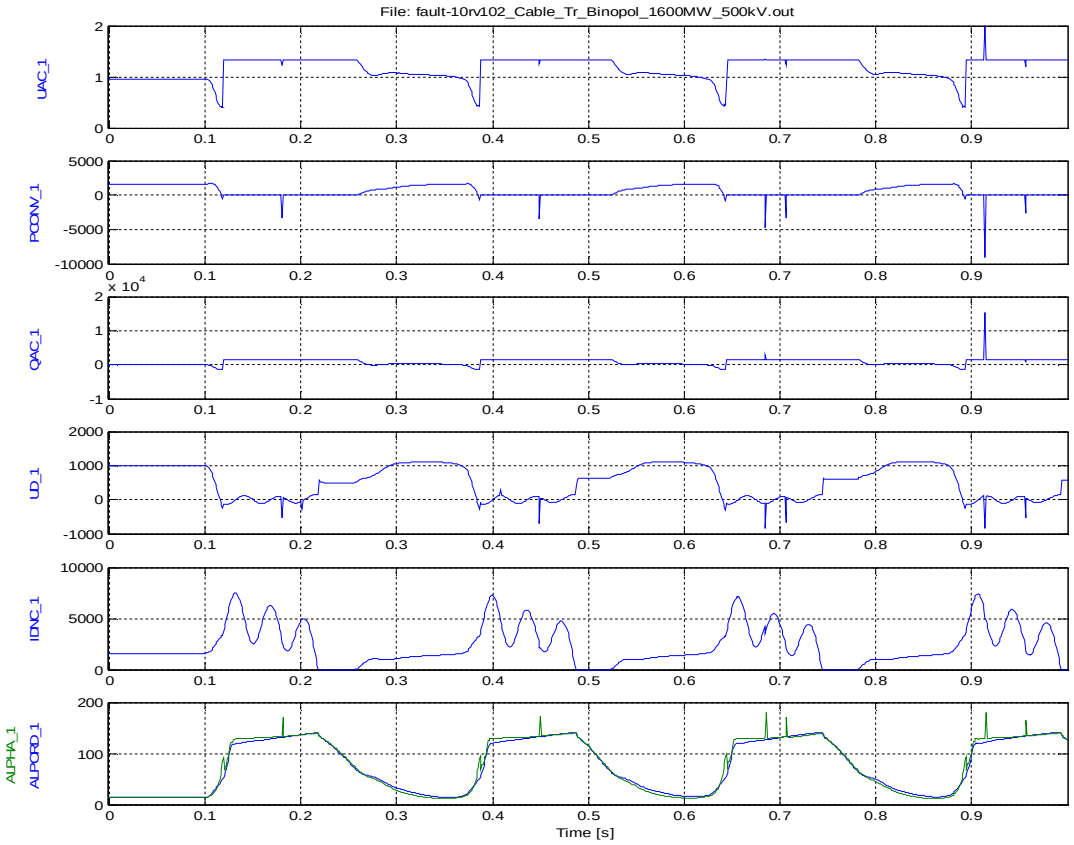


Figure 30 3-phase to ground,10% remaining voltage fault at inverter (rectifier outputs)

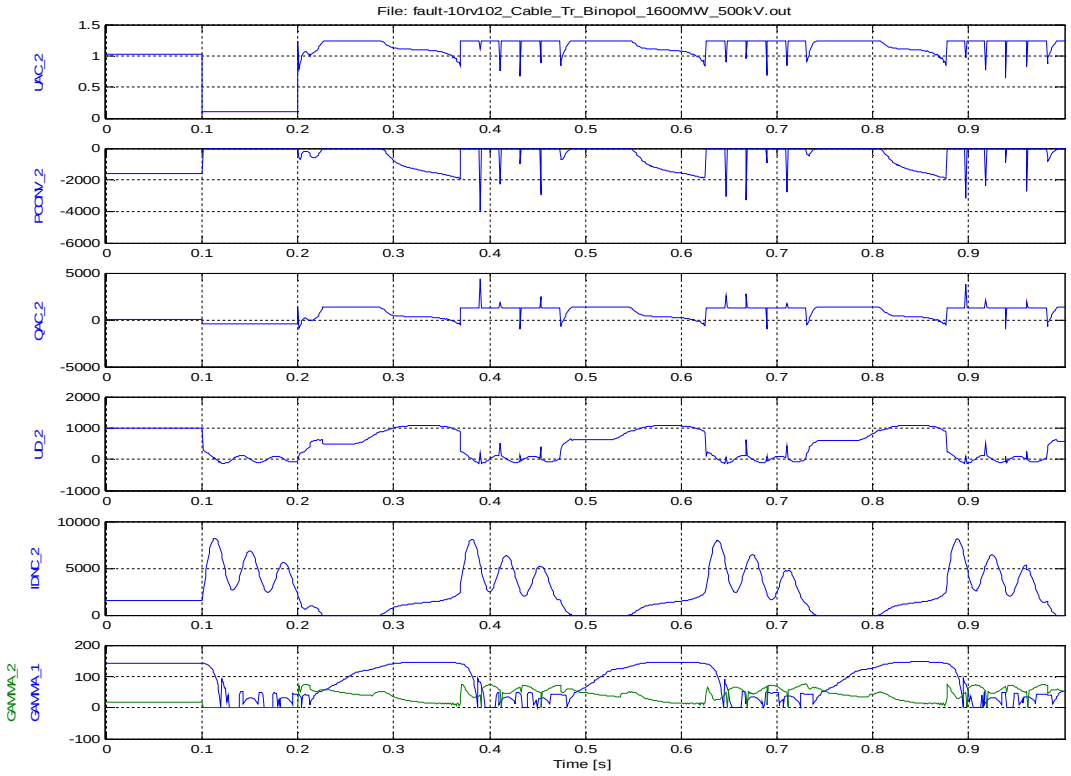


Figure 31 3-phase to ground,10% remaining voltage fault at inverter (rectifier outputs)

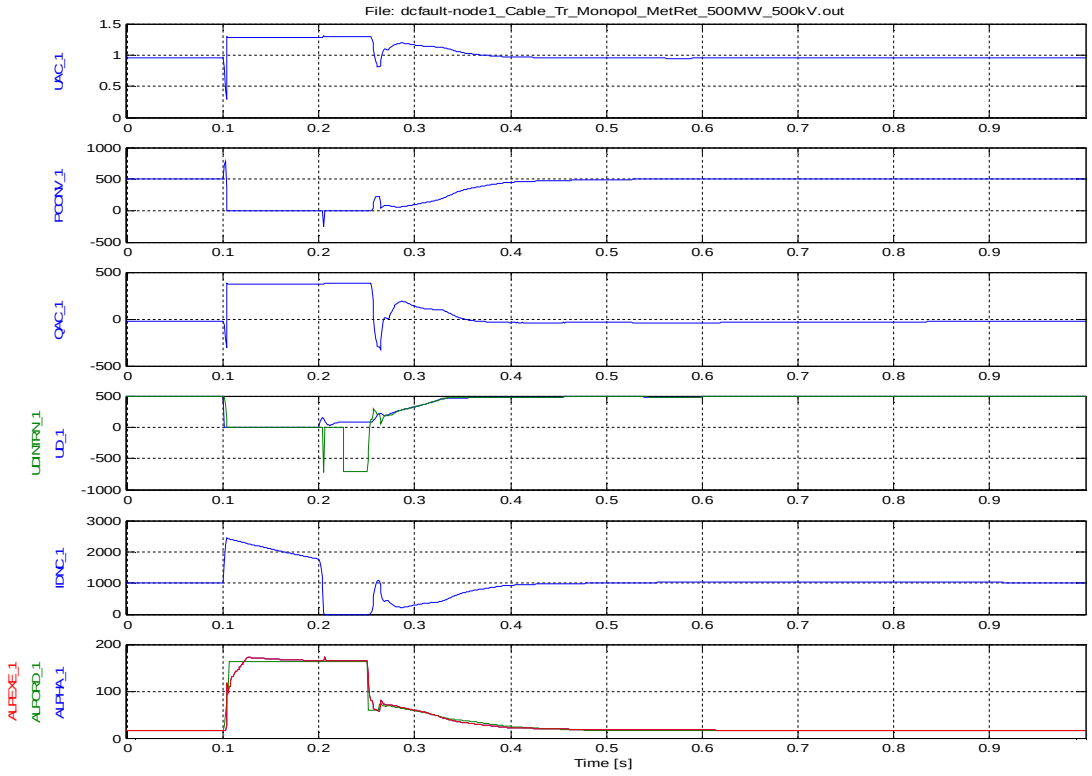


Figure 32 DC line fault near to rectifier

3.10 Conclusion of performance scanning:

The HVDC models were simulated in PSSE by using default existing control parameters; the obtained results are not justifying the PSCAD dynamic performance results. As an example of one case, it can be seen from the figure 30,31, that rectifier commutation failure creates dc current oscillation due to bad CCA parameters. As well as, dc system didn't recover at all due to bad control performance of VDCOL. The recovery of dc system after fault clearing instant is very fast for benchmark models with existing control parameters at rectifier and inverter ac faults. It results in consecutive commutation failures during the recovery at inverter ac faults and low CCA gain and slow ramping down of current order during inverter ac fault might cause commutation failure at rectifier if the sending end ac network is weaker. The dc system recovery time of rectifier ac fault would be increase or decrease by tuning the RAML alpha order decreasing time constant. Commutation failure occurs at rectifier during dc line fault close to rectifier.

4.0 Control parameter optimization:

The overall good HVDC classic dynamic performance could be achieved by tuning the Current control amplifier (CCA) and voltage dependent current order limiter (VDCOL).

4.1 Current controller amplifier:

Current controller amplifier is traditional Proportional plus Integral controller. The proportional part gives fast response to the change in output and integral part is a slower part which reduces the steady state error to zero. Nyquist diagram for CCA stability has been done and verified in document (**10**). The product of proportional and integral gain should be in the range of 50 to 90 in order to have well damped and controlled response (**3**). Time constant of the integrator to be kept constant since tuning of the gains are enough to get good response. If the frequency of current oscillation is within the bandwidth of current controller, current oscillations could be suppressed.

The transfer function of PI controller could be written as

$$G(s) = Kp + \frac{Ki}{sT} \tag{3.1}$$

Including linearization of the current controller, the proportional gain will be

$Kp = Kp1 * Kp2 * \frac{\sin 15}{\sin \alpha}$ and integral gain $Ki = Kp2$ =CCAgain

The dc voltage of the converter can be written as

$$U_{dc} = U_{di0} * \cos\alpha - (d_{xN} + d_{rN}) * \frac{U_{di0N}}{I_{dcN}} * I_{dc} \tag{3.2}$$

At constant current, small change in α gives

$$\frac{\Delta Udc}{\Delta\alpha} = -Udio * \sin\alpha \tag{3.3}$$

Therefore, the gain G = -Udio * Sinα (**11**)

$$G1(s) = \frac{G}{1+sT} \tag{3.4}$$

For twelve pulse bridge $T = \frac{1}{12 * f}$ (**11**)

At 50Hz, T= 1.66ms

Transfer function of dc circuit can be written as

$$G2(s) = \frac{\Delta Idc}{\Delta Udc} = \frac{1}{R + sL + \frac{1}{\frac{1}{(R+sL)} + sC}} \tag{3.5}$$

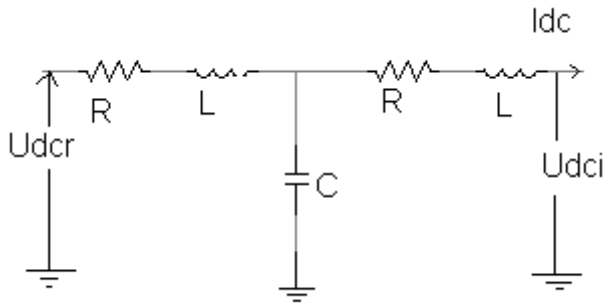


Figure 33 Dc system representation

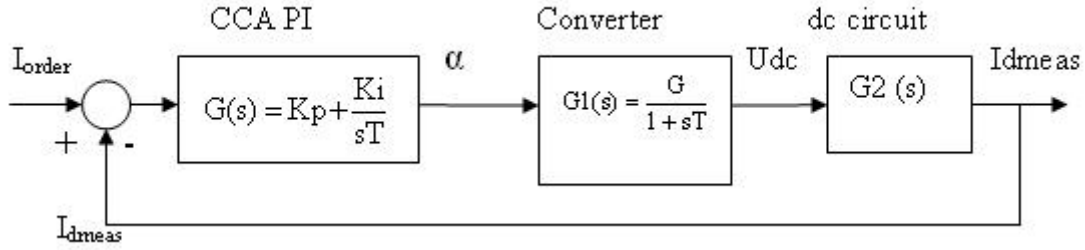


Figure 34 Block diagram of CCA

Traditionally, rectifier controls the current at steady state operation. The proper selection of proportional and integral constant of CCA is required to achieve the current controller stability. Obviously, it depends upon the strength of the network. Normally, choosing control parameters for cable is quite difficult than overhead lines. There is chance of commutation failure at the rectifier when 3-phase to ground fault at inverter if the ac network is weaker at rectifier station. Therefore, proper selection of CCA gain would prevent the commutation failure at rectifier.

Method of tuning CCA parameters:

The integrator gain or CCA gain shall be increased higher than 30 until the current follows the current order faster i.e. without any steady state error for cable with weak rectifier and proportional gain shall be within the range of 50 and 90 in order to get smooth response, hence based on these Kp value could be chosen, typically it is around 2.5. Since increased gain would give fast response, results decrease of current due faster increase of alpha. In contrast, slower response of CCA, effects larger dip in ac voltage and increased current leads to commutation failure at rectifier, thus current oscillation in dc system.

In particularly, low short-circuit ac system connected either should not have high CCA gain as explained before in order to prevent oscillations in dc system. Since, higher proportional gain at low SCR, small decrease in d.c. current might give larger change in alpha, consequence increased voltage and current causes decreased ac bus voltage. Hence, dc voltage and current would decrease. It repeats and creates high frequency oscillations. As well as, higher integral gain takes some time to settle down in steady state.

4.2 Voltage Dependent Current Order Limiter (VDCOL):

The VDCOL reduces the current order in a function of dc voltage. In constant power control mode, absence of VDCOL causes increase of current order during reduced voltage to set the power constant. Hence, the reactive power consumption will increase effects reduction of ac voltage; particularly weak ac network leads to voltage collapse. It mainly avoids the power instability during and after the a.c. faults, since weaker receiving ac system leads to voltage instability due to fast recovery during post-fault. Therefore, delayed recovery of power would be desirable to prevent repetitive commutation failures. The main function of VDCOL is to delaying and ramping of current limits.

Method of tuning VDCOL parameters:

The non-linear low pass filter is used to delaying and ramping of current limits as a function of measured dc voltage. The time constants for delaying and ramping should be different for both converters which is important to keep priority between rectifier and inverter current controllers. Normally the inverter have lower effective current order due to current margin and its important to maintain this priority during transients The main parameters need to tune in VDCOL are Ud_Tc_Up, Ud_Tc_Dn and Udhigh.

Too long up time will also disturb the recovery of dc system, it resulting into commutation failure. For example slow increase of current order will build a nominal voltage at 0.9 p.u. current itself. But still the current controller would increase the current to reach the reference point (1p.u.) therefore the alpha and gamma will be reduced further to reach nominal current. This reduced gamma will lead to commutation failure.

Same as for too fast time up constant will affect the recovery.

The down time constant for both rectifier and inverter shall be faster to reduce the surge current during ac faults at inverter end by decreasing the current order faster, especially for cable cases.

Fast down time rectifier time constant increase the commutation margin for rectifier, the peak value of rectifier dc current has been reduced. However long down time constant at rectifier would slightly reduce the recovery time since the slower decrease of current will charge the cable as fast as compared to the fast down time. In contrary, line shall have slow down time for quick recovery of dc system.

Selection of break points Udhigh for both rectifier and inverter.

There should not be very large difference between two corresponding rectifier and inverter breakpoints. Normally break points for both converters are same, for some case like long cable might need different break points let's say $U_{dhighrec}$=0.6 and $U_{dhighinv}$= 0.9. Because the cable would take long time to charge back to nominal voltage after the fault, it reduces the recovery time. This is also one of the ways to reduce the dc system recovery time. If the Udhigh is reduced in rectifier, it must be faster down time to prevent commutation failure at rectifier. Also, combination of very low Udhigh and slow down time at rectifier will give overshoot in power and dc current when inverter hits the breakpoint due to the overcharging of cable; it might leads to unstable if the ac network strength is weaker. Therefore, proper combination of values has to chosen.

In line cases, should avoid using different breakpoints of voltage for rectifier and inverter, for example if U_{dhighR}=0.6 and U_{dhighI} =0.9 with fast down time, even though the dc system

recovers faster, dc voltage at rectifier back to nominal voltage at 0.3 p.u. of dc current itself and alpha also hits the nominal value at 0.5 p.u. of current, hence the current controller at rectifier will start to oscillate; whether to increase the dc current or decrease the dc voltage. The same thing happens if there is very fast up time.

The recovery time is mainly depends upon the strength of the ac network, the up time constant could be faster if the system is stronger. In contrary, weaker receiving network should be recovering slowly i.e. longer up time in order to prevent consecutive commutation failures due to voltage instability.

The above **defined rules in this thesis** are used to tune the CCA and VDCOL parameters and obtained optimized parameters below. It handles the dynamic simulation independent of configuration, power and voltage levels.

4.3 Optimized VDCOL parameters:

	Overhead lines	Cables	Back to Back
Ud_Tc_Up_Rec in sec	0.06	0.055	0.05
Ud_Tc_Dn_Rec in sec	0.015	0.02	0.02
Ud_Tc_Up_Inv in sec	0.07	0.06	0.055
Ud_Tc_Dn_Inv in sec	0.015	0.001	0.015
Ud_High_Rec in pu	0.8	0.8	0.8
Ud_High_Inv in pu	0.8	0.8	0.8

Tabel 5 Tuned VDCOL parameters

4.4 Optimized CCA parameters:

	Overhead lines	Cables	Back to Back
CCA gain	26	33	25
Kp in deg/pu	2.5	2.5	2.1
Time constant(T) in deg/pu/sec	0.01	0.01	0.01

Tabel 6 Tuned CCA parameters

The optimized parameters have been used instead existing parameters and re-simulated all the test cases which have done in performance scan. The results of one example case from benchmark model with optimized CCA and VDCOL parameters for each type of transmission are plotted.

4.5 Parameters of Plot*:*

Rectifier (page 1)	Inverter (page 2)	(Page 3)
Uac, AC voltage	Uac, AC voltage	Alpha order and measured (inverter)
Pconv,power directed into	Pconv,power	Commutation failure

converter	directed into converter	detector
Qac, reactive power into ac network	Qac, reactive power into ac network	Gamma at rectifier
Ud, dc voltage (measured after smoothing reactor)	Ud, dc voltage (measured after smoothing reactor)	Ud internal(pole voltage)
Idc, DC current	Idc, DC current	IorderLim (output from VDCOL)
Alpha order and measured alpha	Gamma	

4.6 Results:

4.6.1 Cable transmission

4.6.1.1 Three phase to ground AC fault at inverter

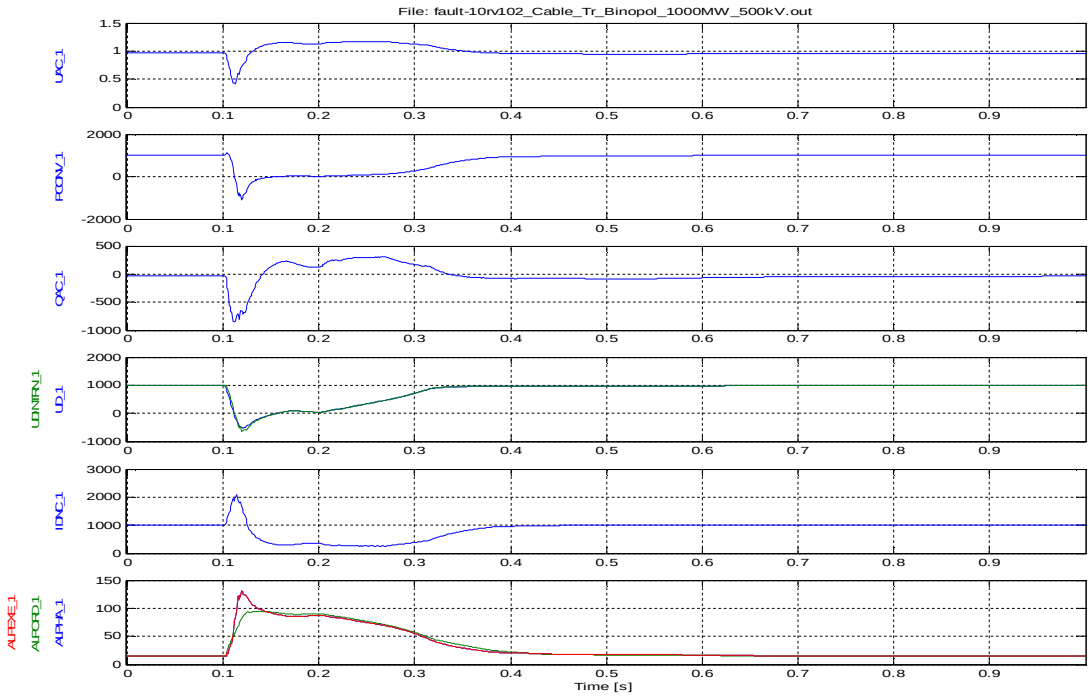


Figure 35 3-Phase to ground AC fault at Inverter(rectifier side)

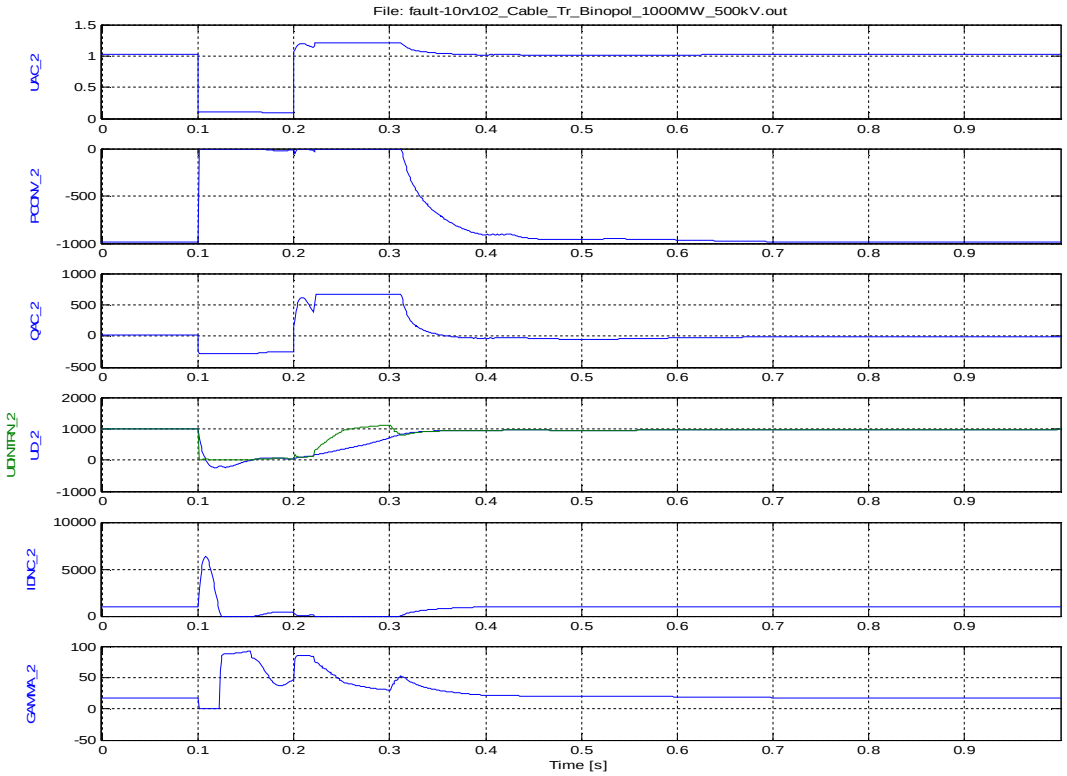


Figure 36 3-Phase to ground AC fault at Inverter (inverter side)

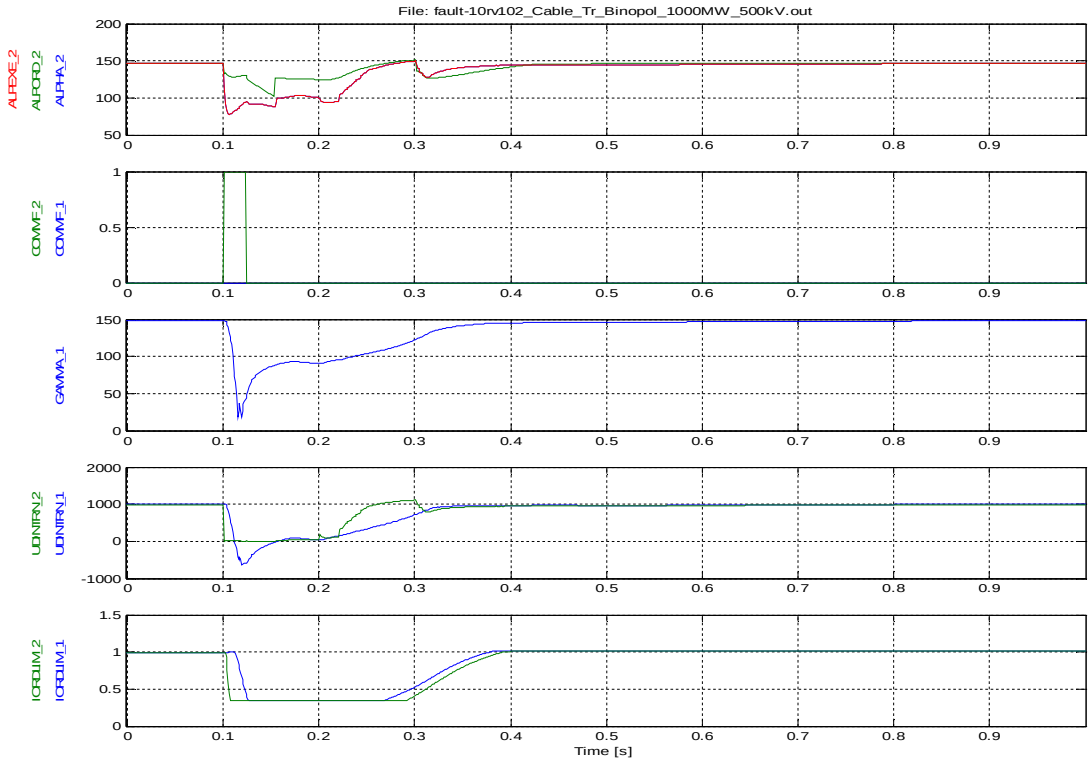


Figure 37 3-Phase to ground AC fault at Inverter

4.6.1.2 Three phase to ground AC fault at rectifier

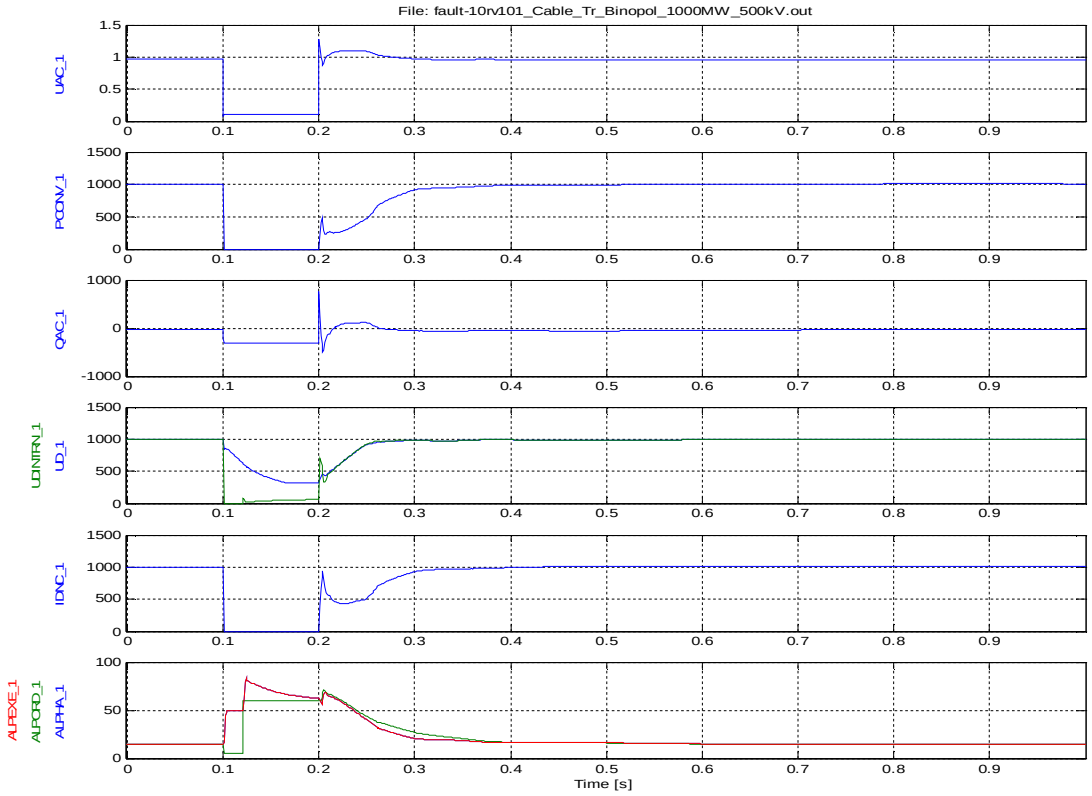


Figure 38 3-Phase to ground AC fault at rectifier(rectifier side)

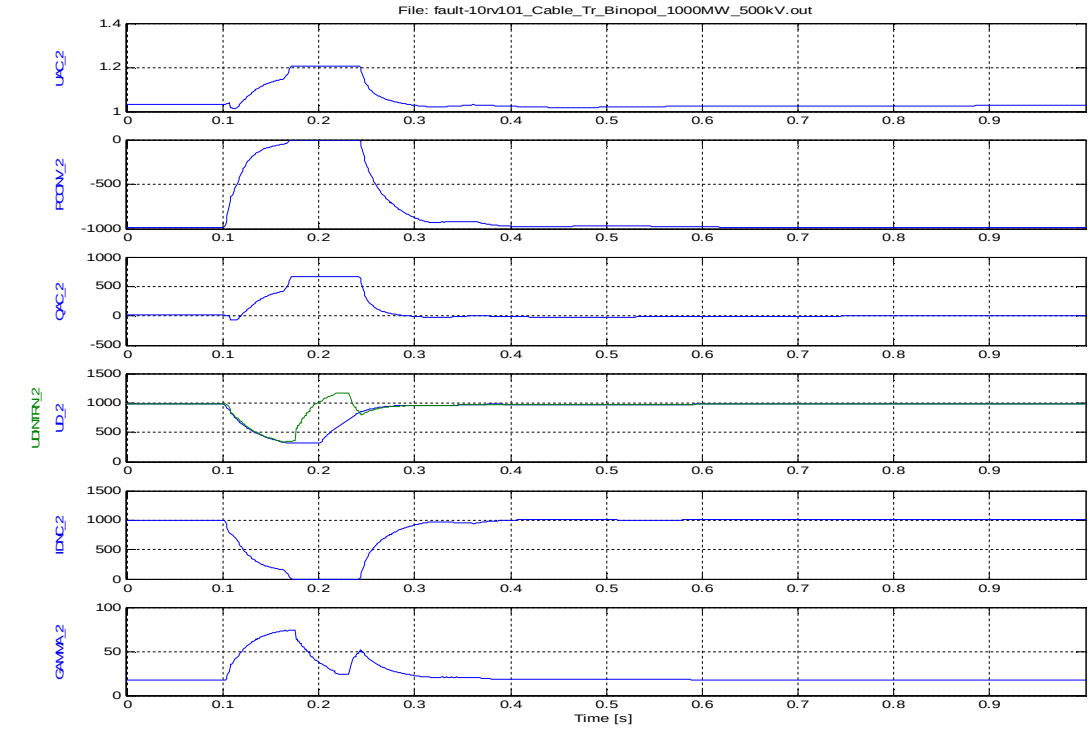


Figure 39 3-Phase to ground AC fault at rectifier (inverter side)

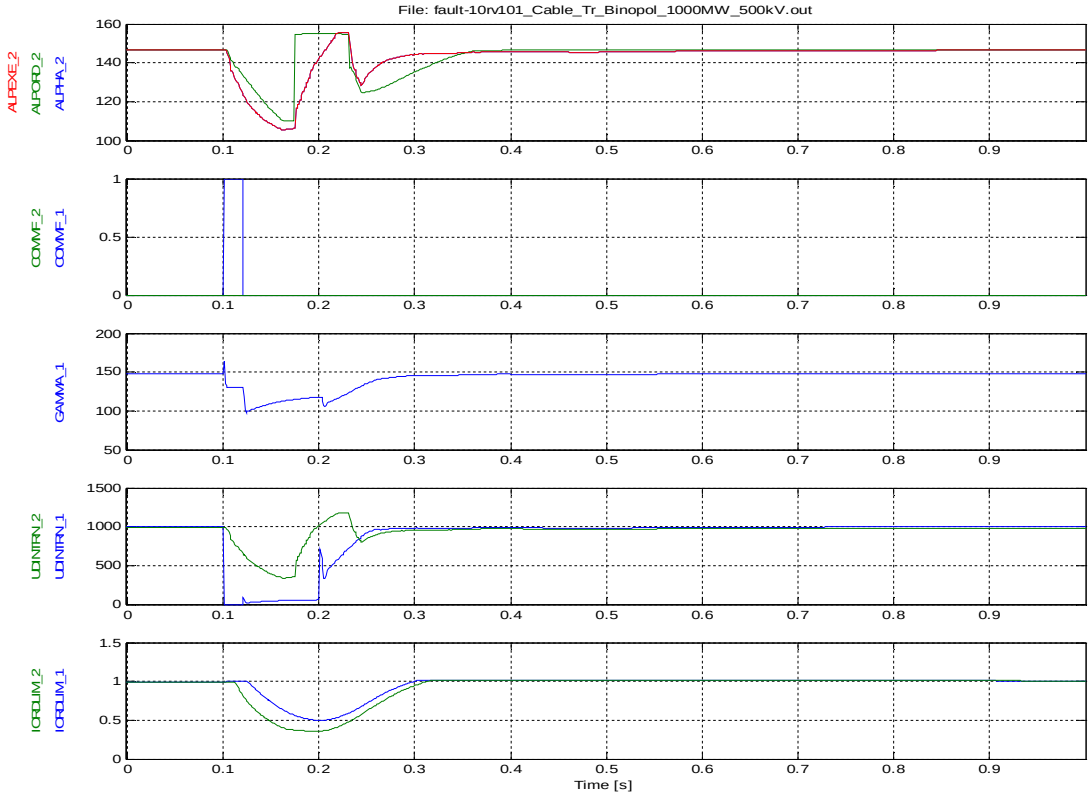


Figure 40 3-Phase to ground AC fault at rectifier

4.6.1.3 DC line fault close to rectifier

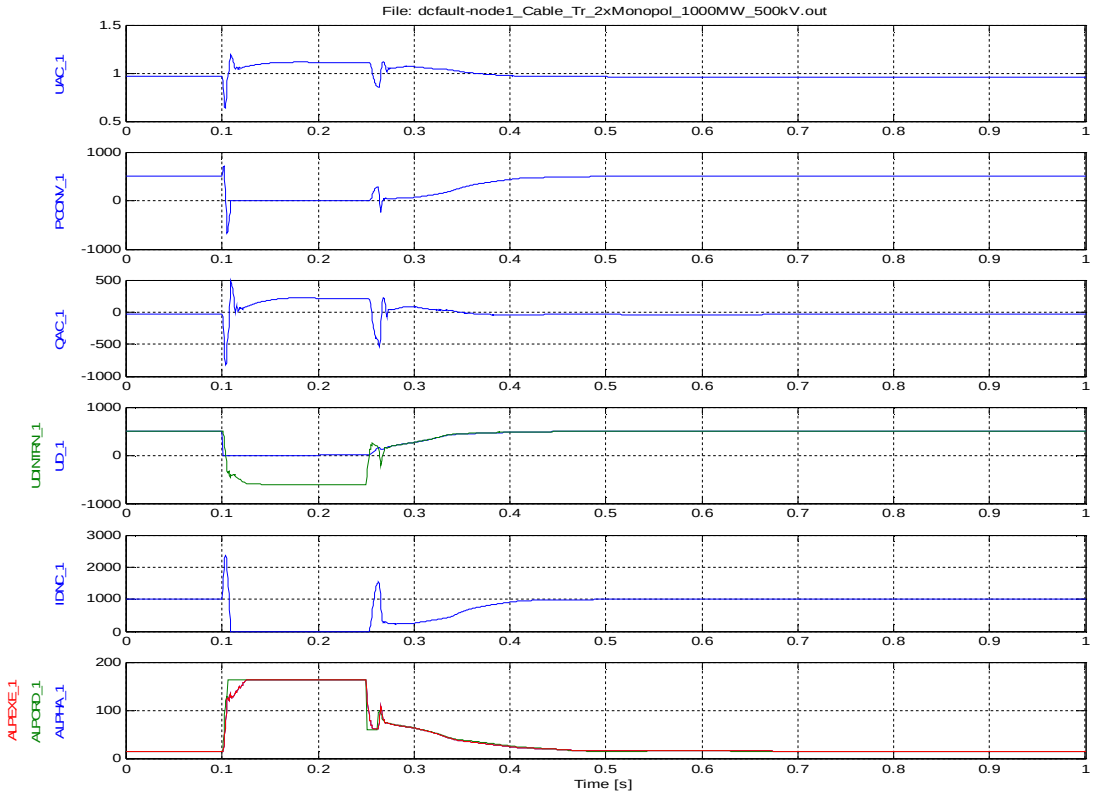


Figure 41 DC fault at rectifier (rectifier side)

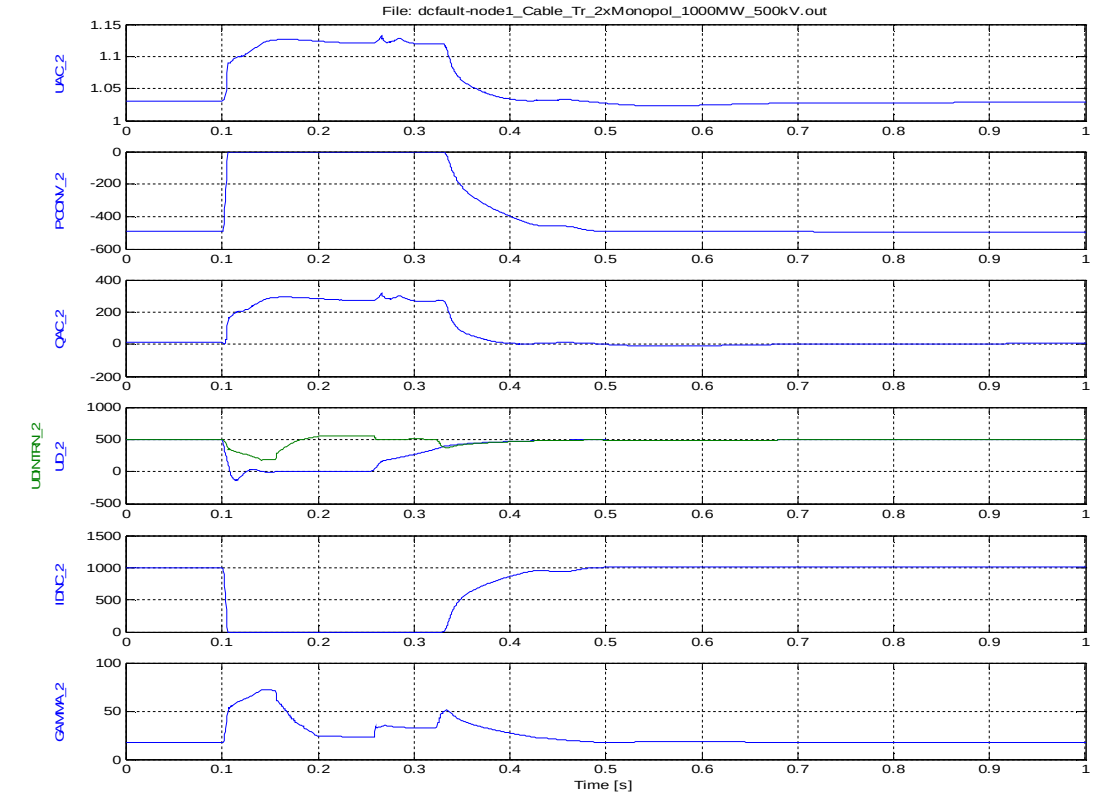


Figure 42 DC fault at rectifier(inverter side)

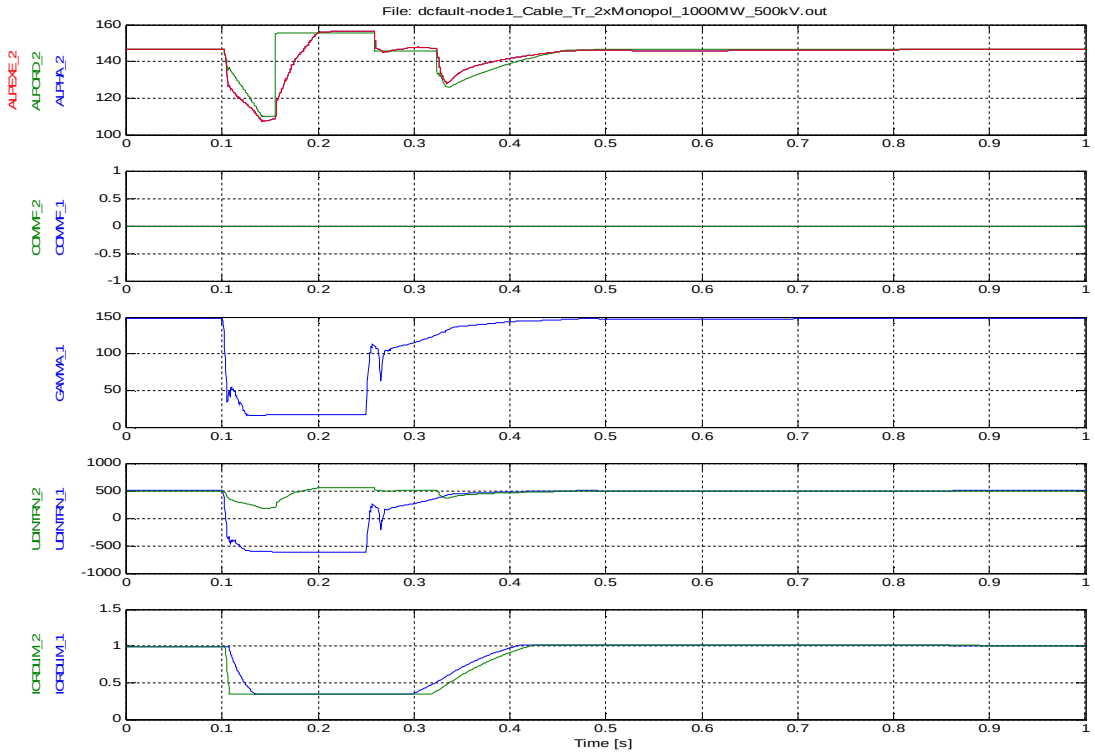


Figure 43 DC fault at rectifier

4.6.1.4 0.92 p.u. power step

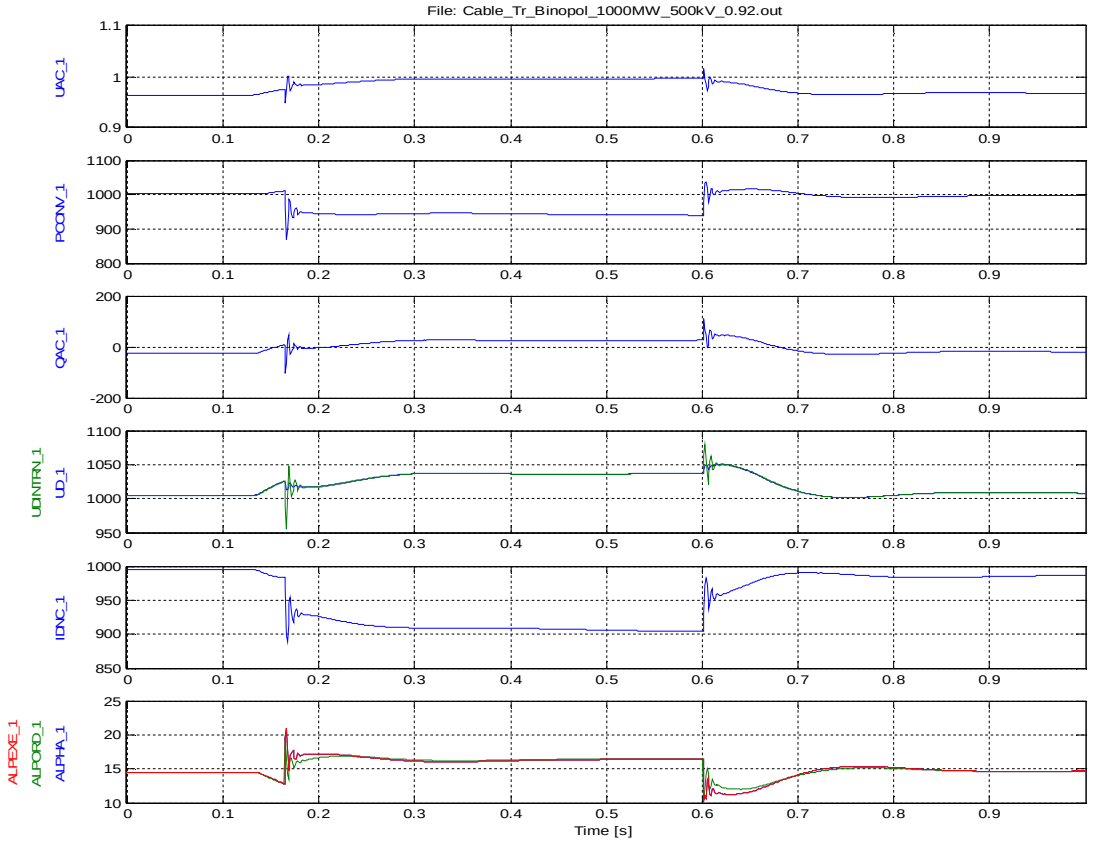


Figure 44 Power step(rectifier side)

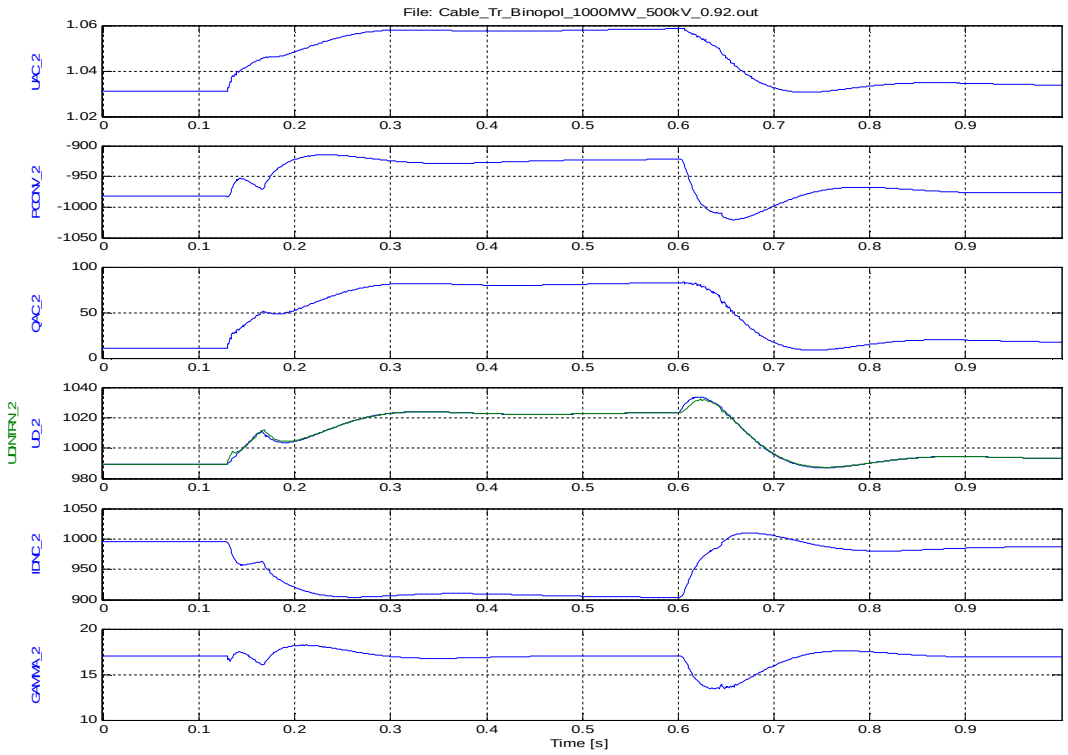


Figure 45 Power step (Inverter side)

4.6.1.5 3 degree gamma reference step

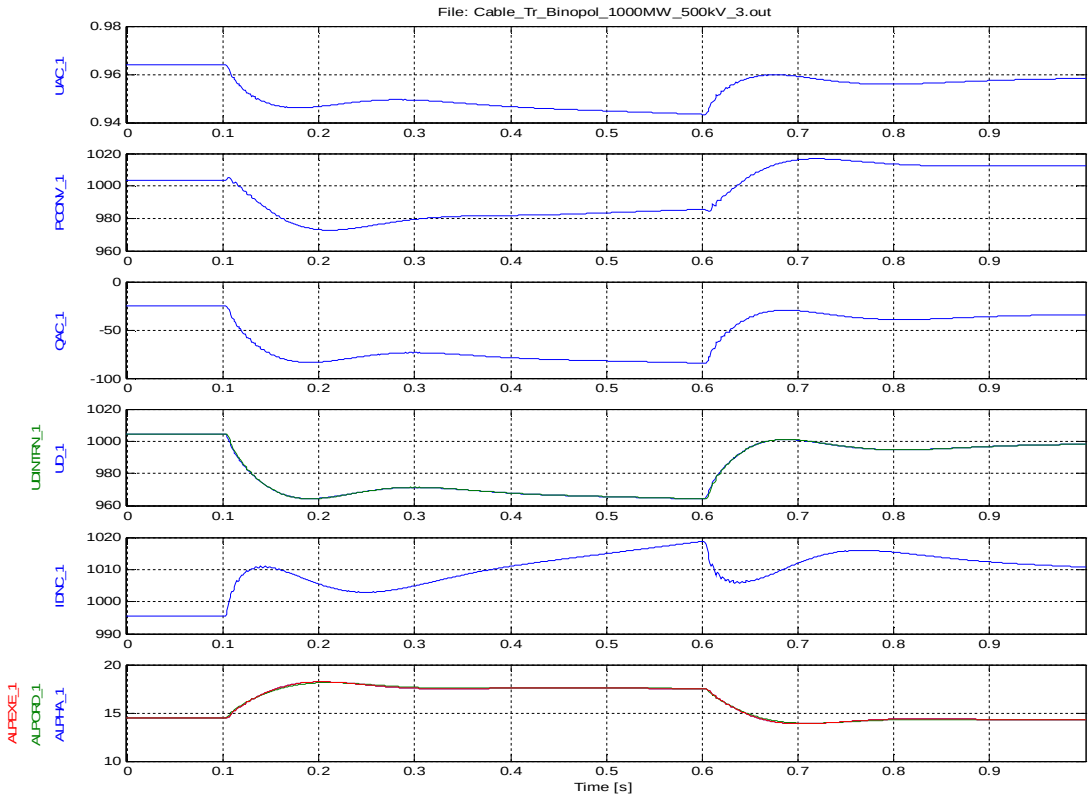


Figure 46 Gamma step(rectifier side)

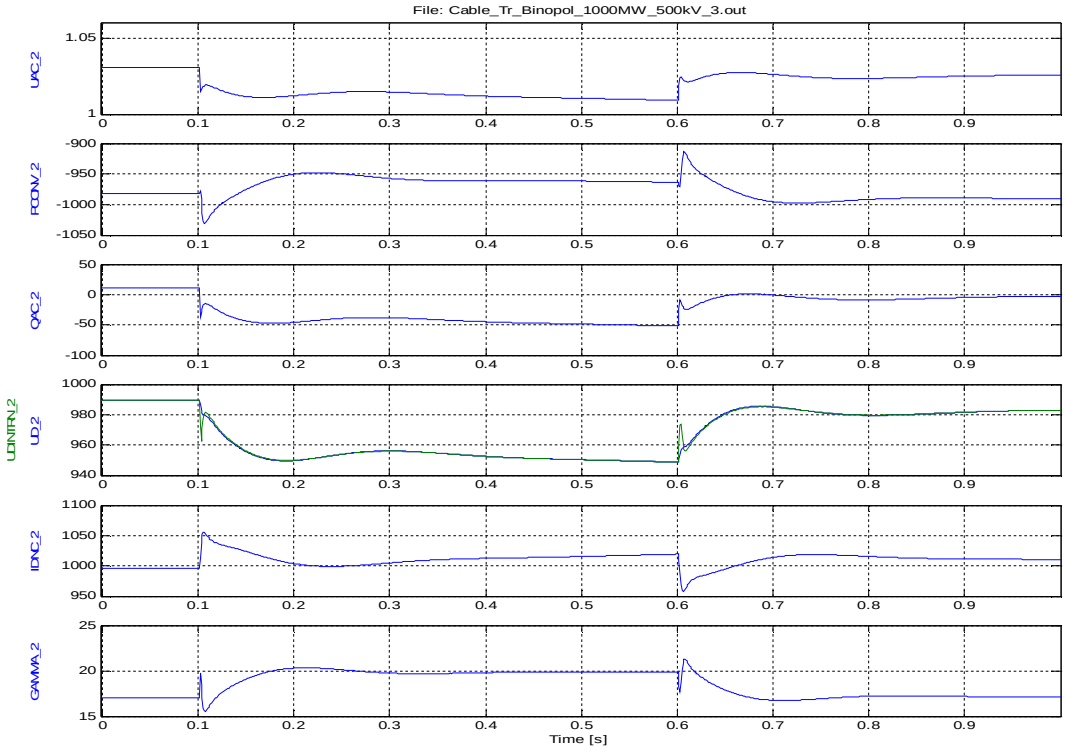


Figure 47 Gamma step (inverter side)

4.6.1.6 0.9p.u. dc voltage step

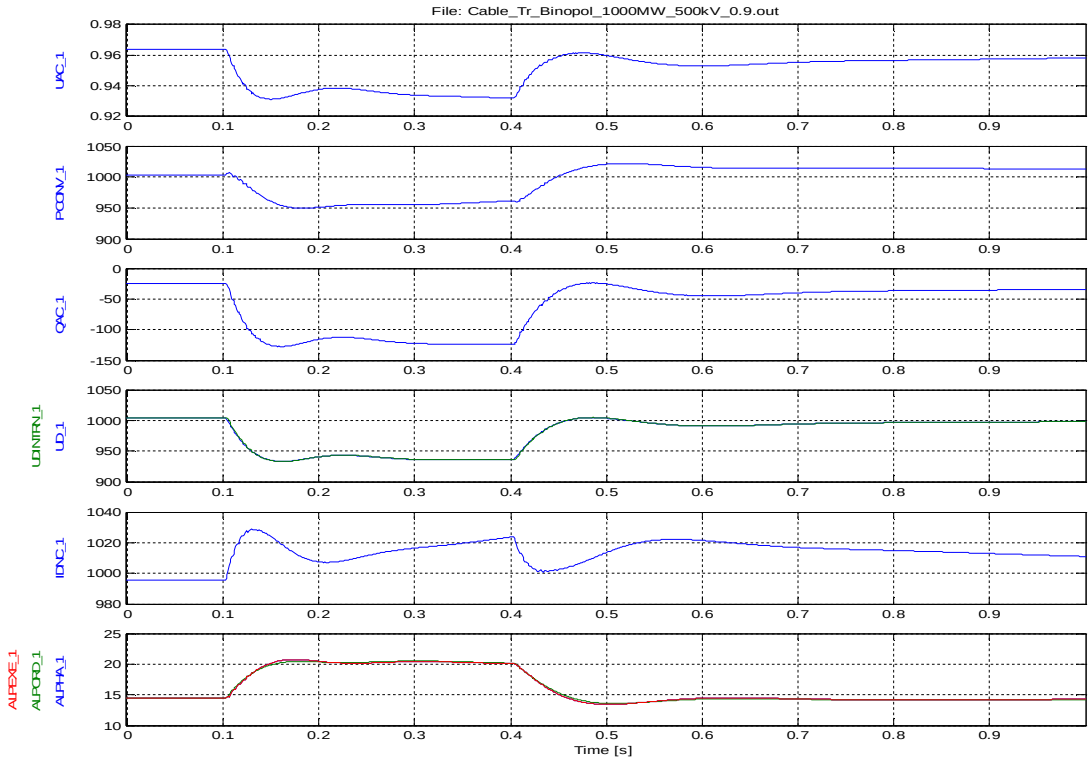


Figure 48 DC voltage step(rectifier side)

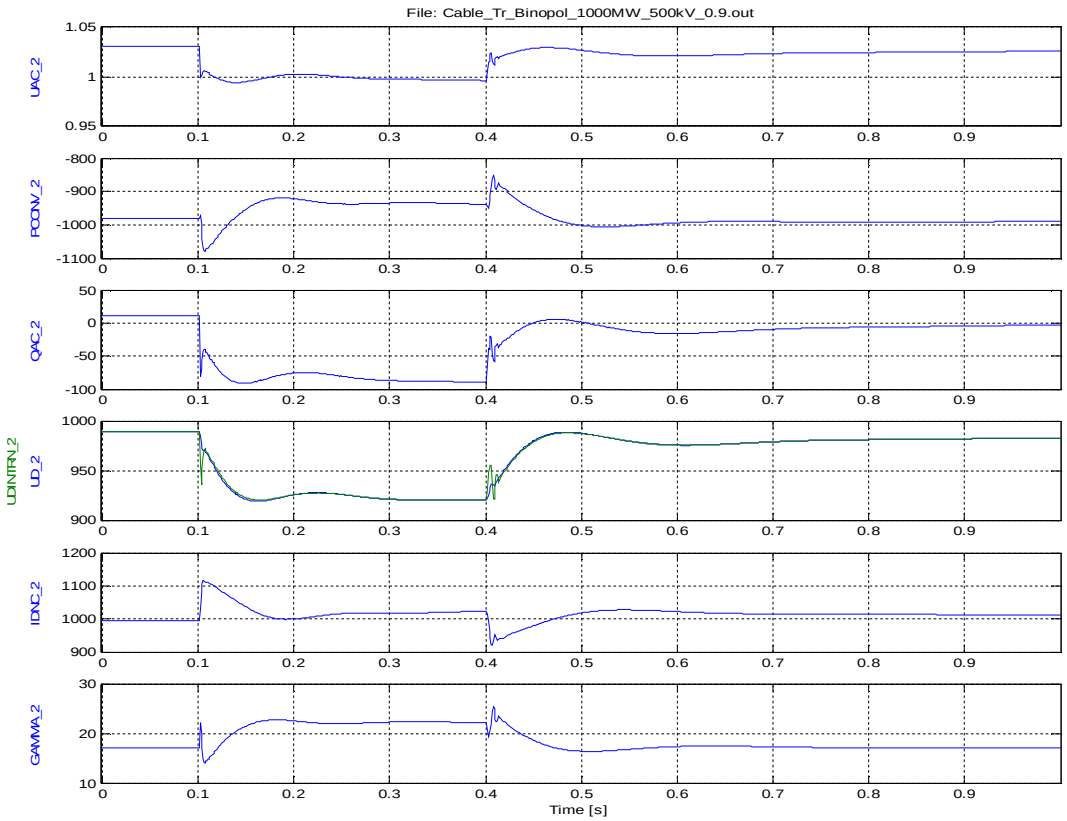


Figure 49 DC voltage step (inverter side)

4.6.2 Overhead line transmission

4.6.2.1 Three phase to ground AC fault at inverter

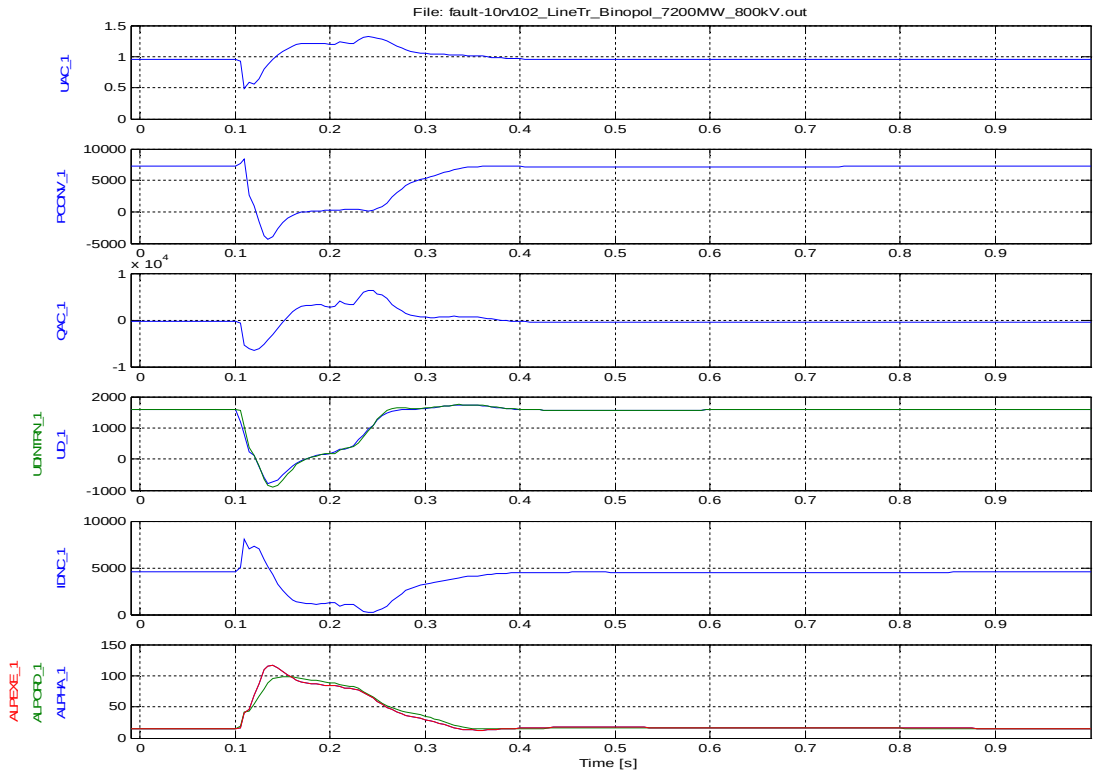


Figure 50 10% remaining 3-Phase to ground AC fault at Inverter (rectifier side)

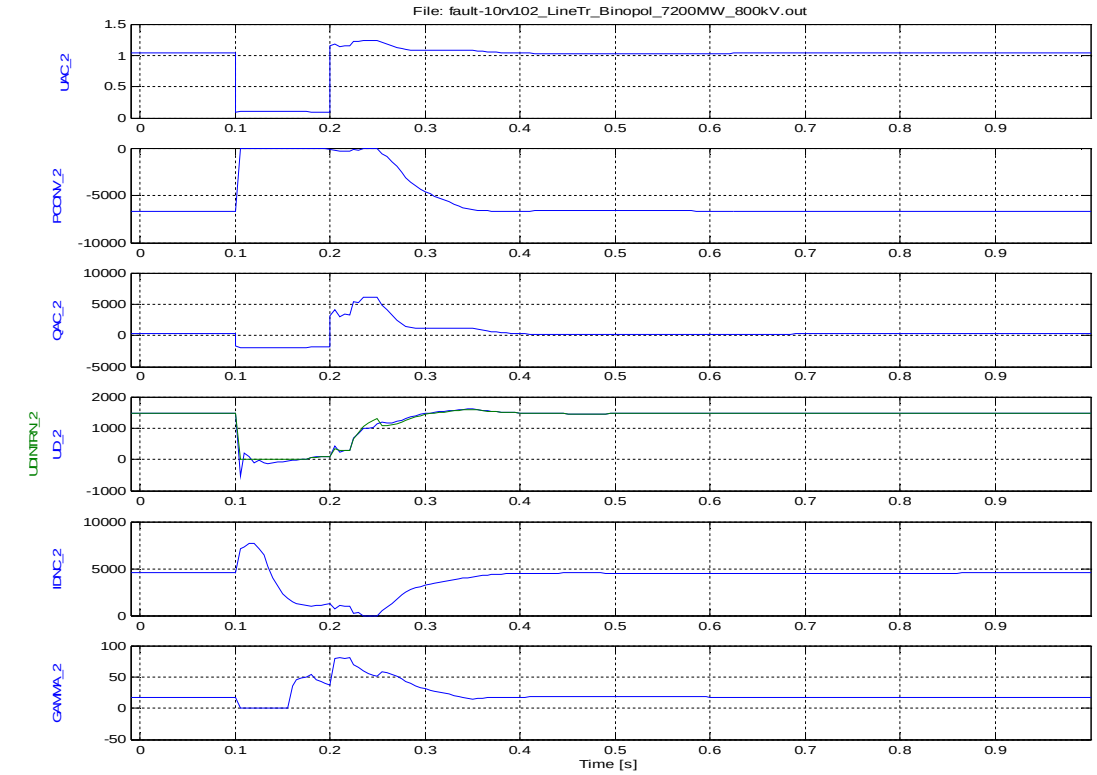


Figure 51 10% remaining voltage to ground AC fault at inverter (inverter side)

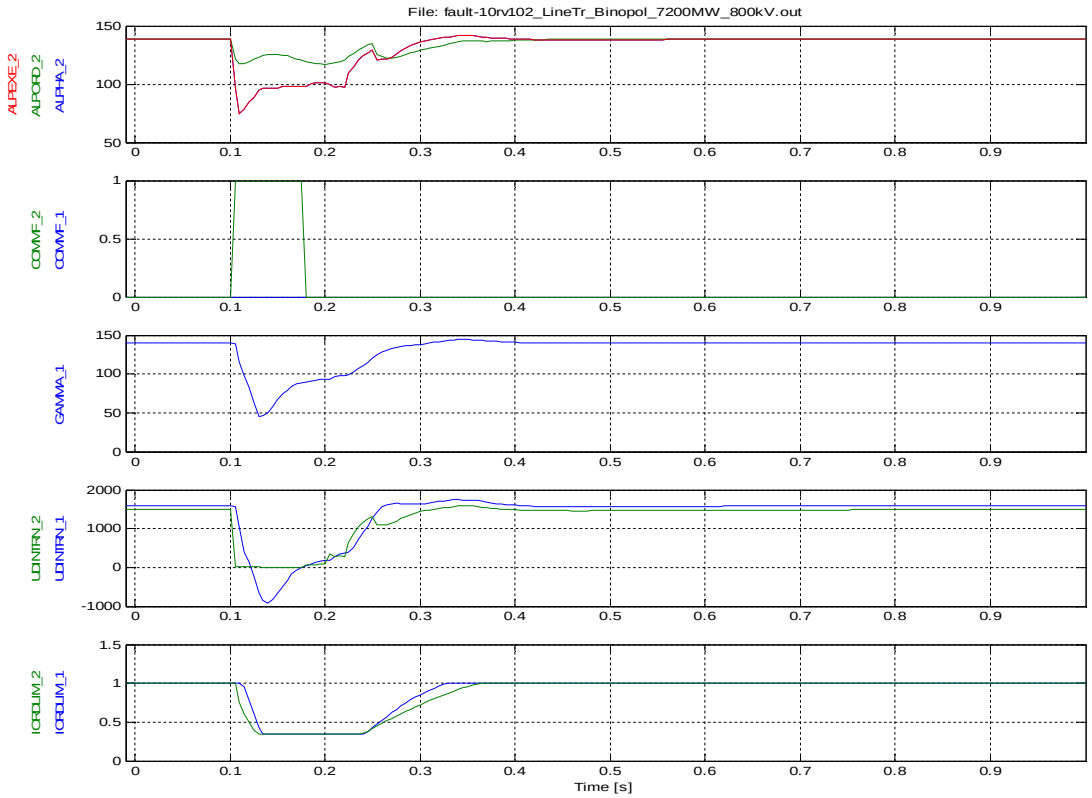


Figure 52 10%remaining 3-Phase to ground AC fault at Inverter

4.6.2.2 Three phase to ground AC fault at rectifier

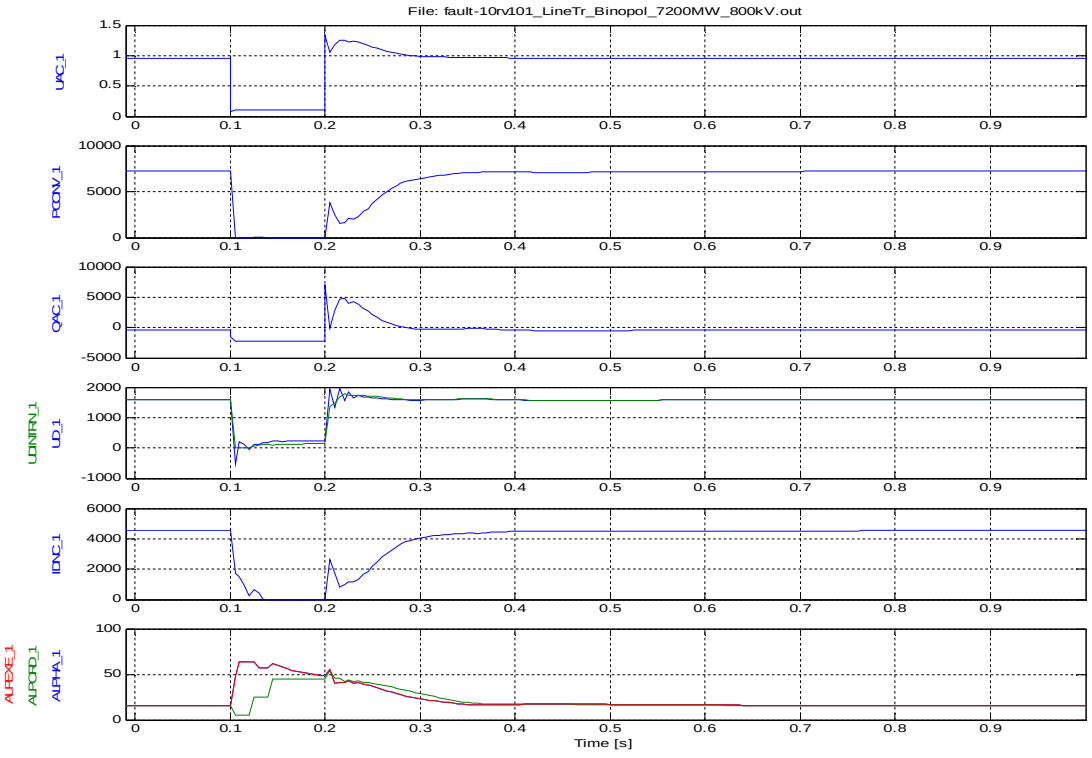


Figure 53 10% remaining voltage 3-Phase to ground AC fault at Rectifier(rectifier side)

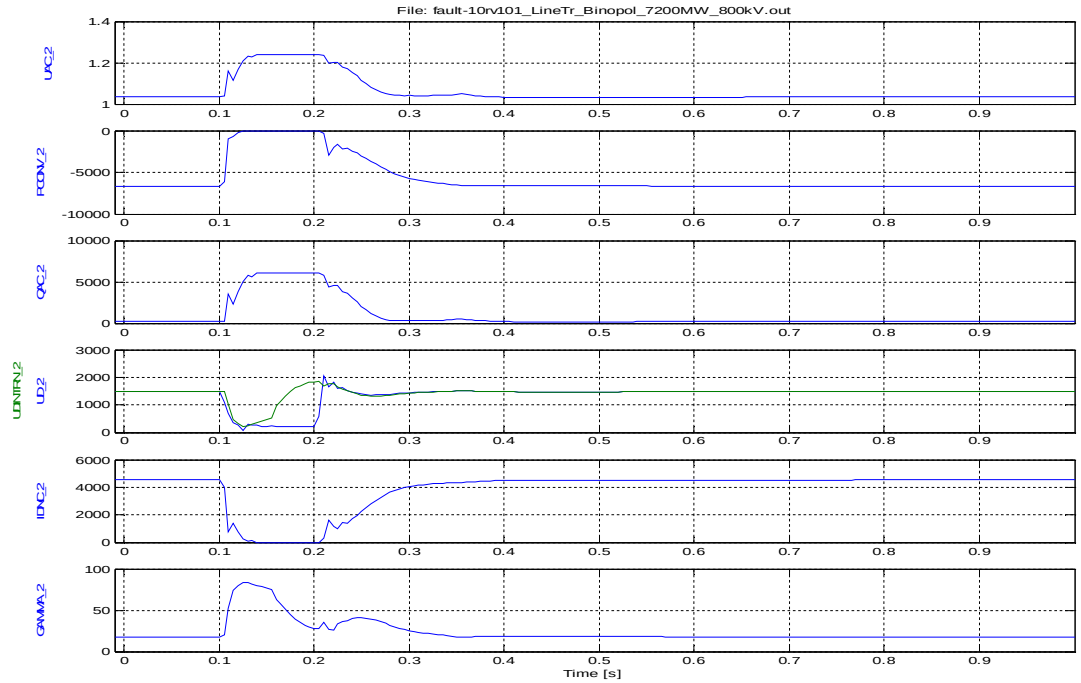


Figure 54 10% remaining voltage 3-Phase to ground AC fault at Rectifier(inverter side)

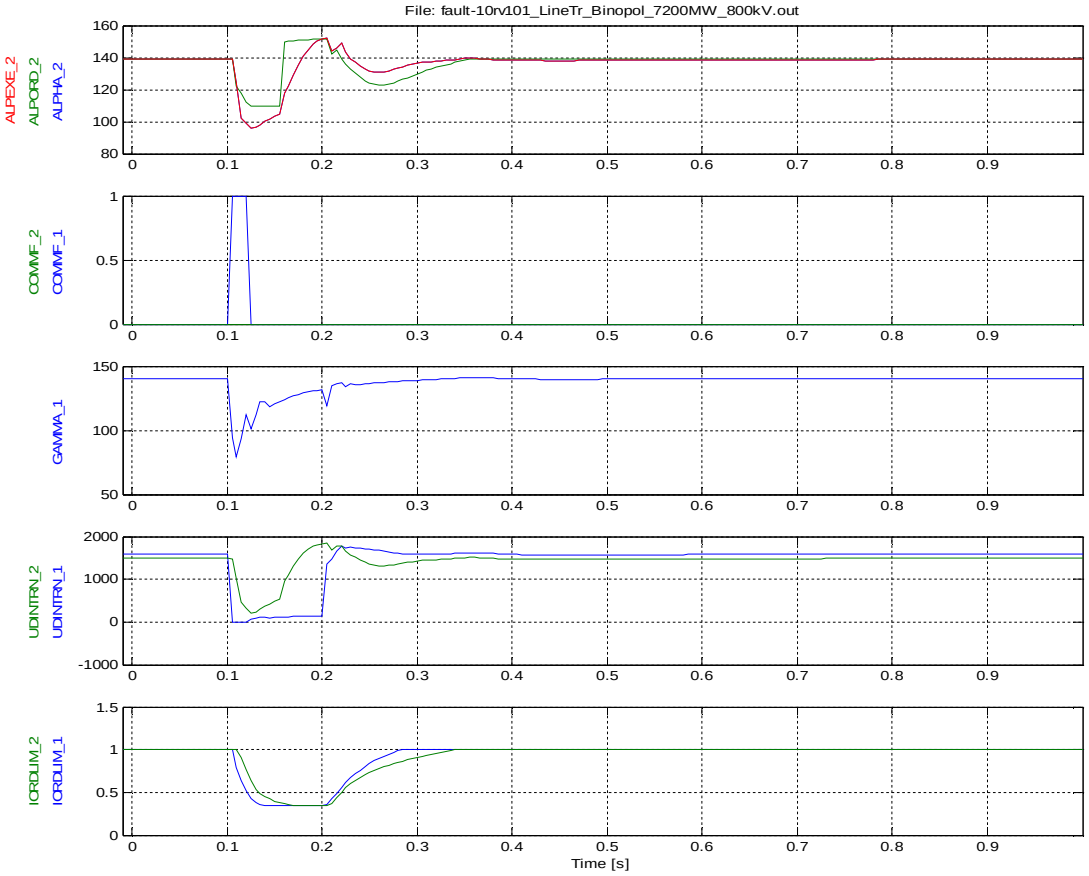


Figure 55 10% remaining voltage 3-Phase to ground AC fault at Rectifier

4.6.2.3 DC line fault close to rectifier

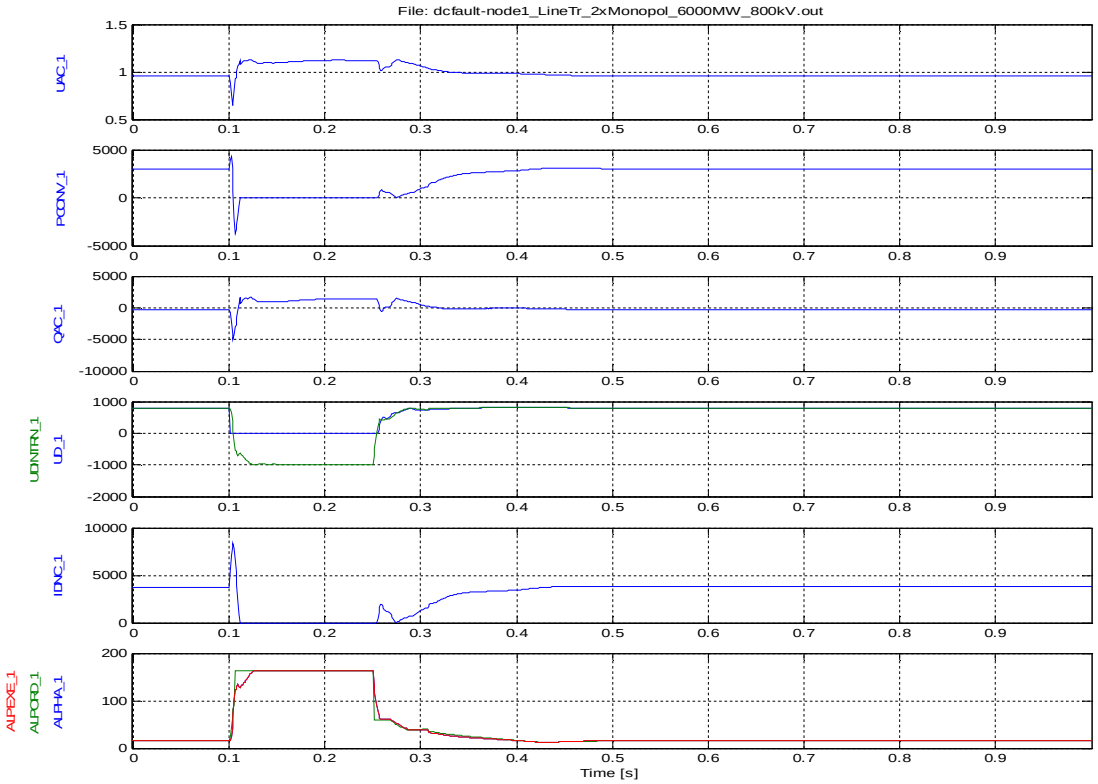


Figure 56 DC line fault at rectifier (rectifier side)

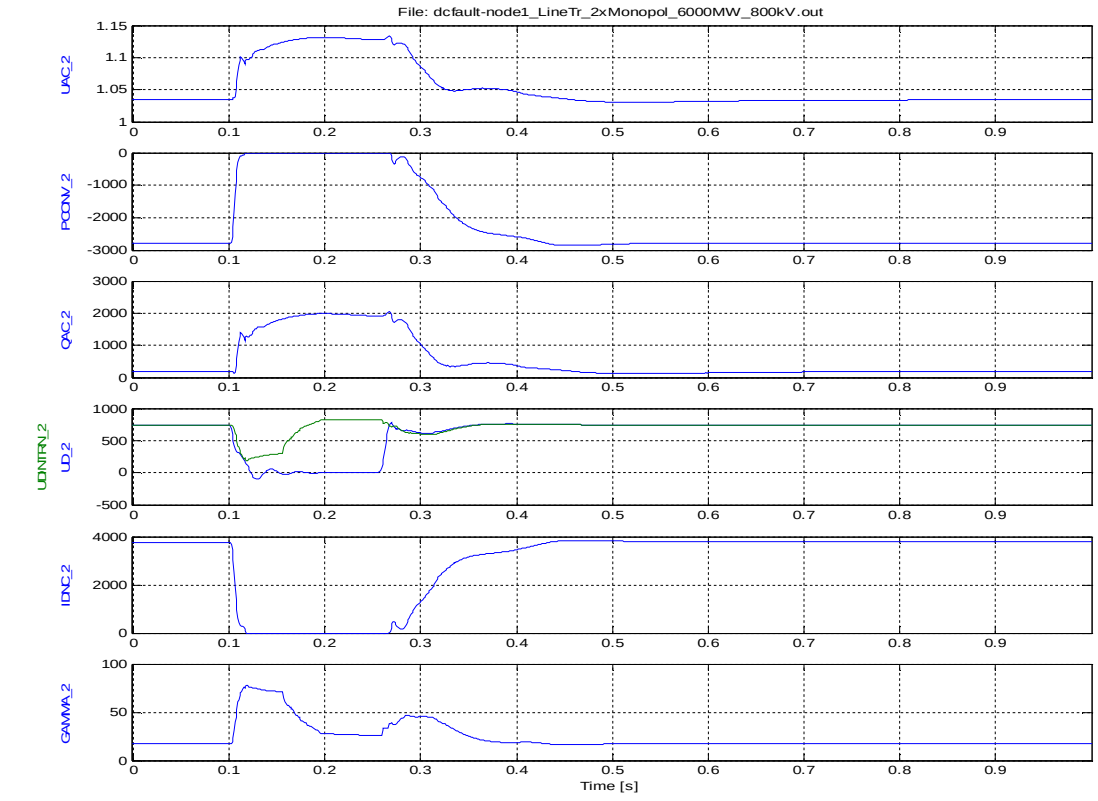


Figure 57 DC line fault at rectifier (inverter side)

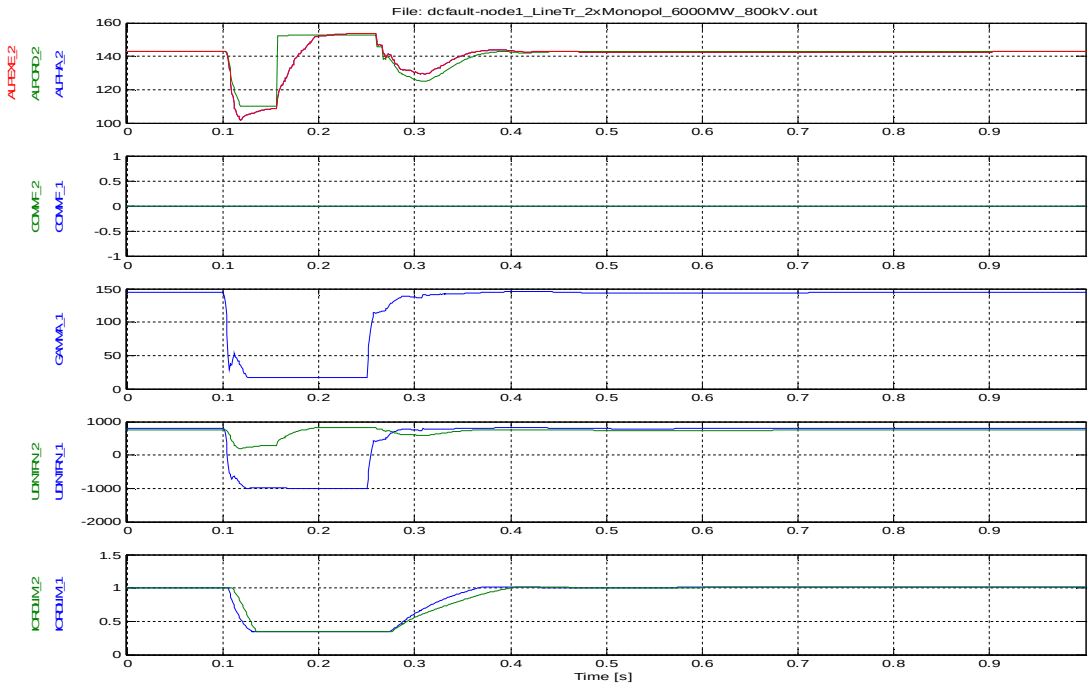


Figure 58 DC line fault at rectifier

4.6.3 Back to Back

4.6.3.1 Three phase to ground AC fault at inverter

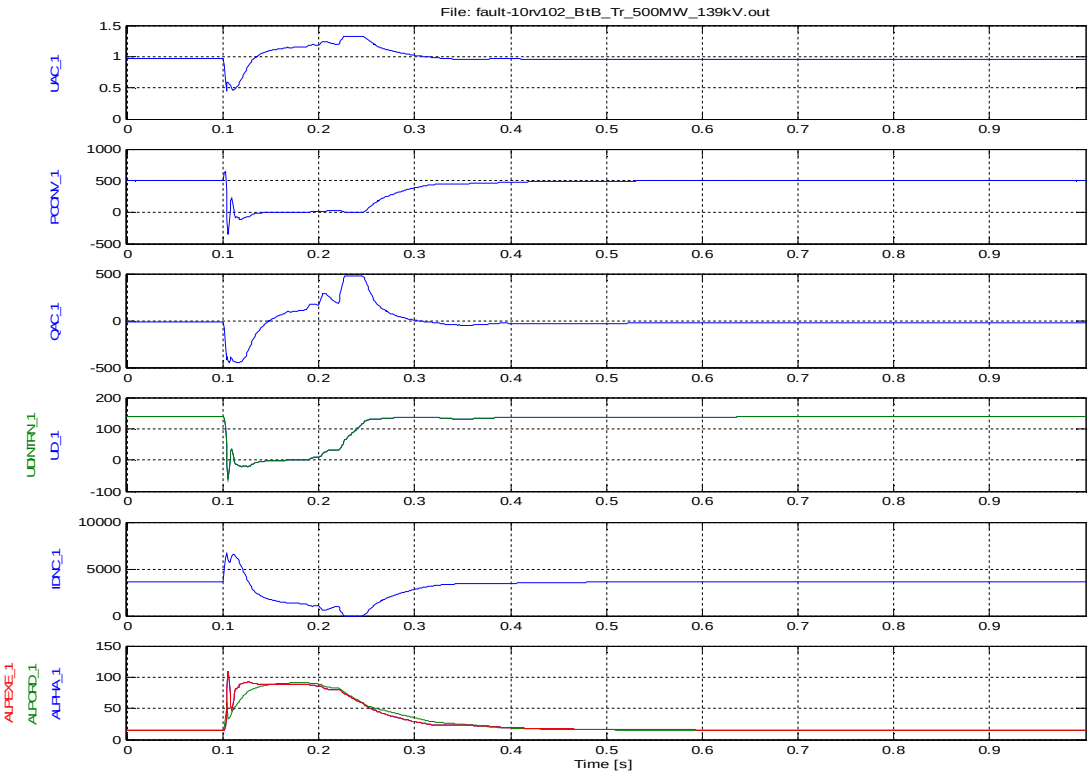


Figure 59 10% rem. Voltage 3-phase to ground ac fault at inverter (rectifier side)

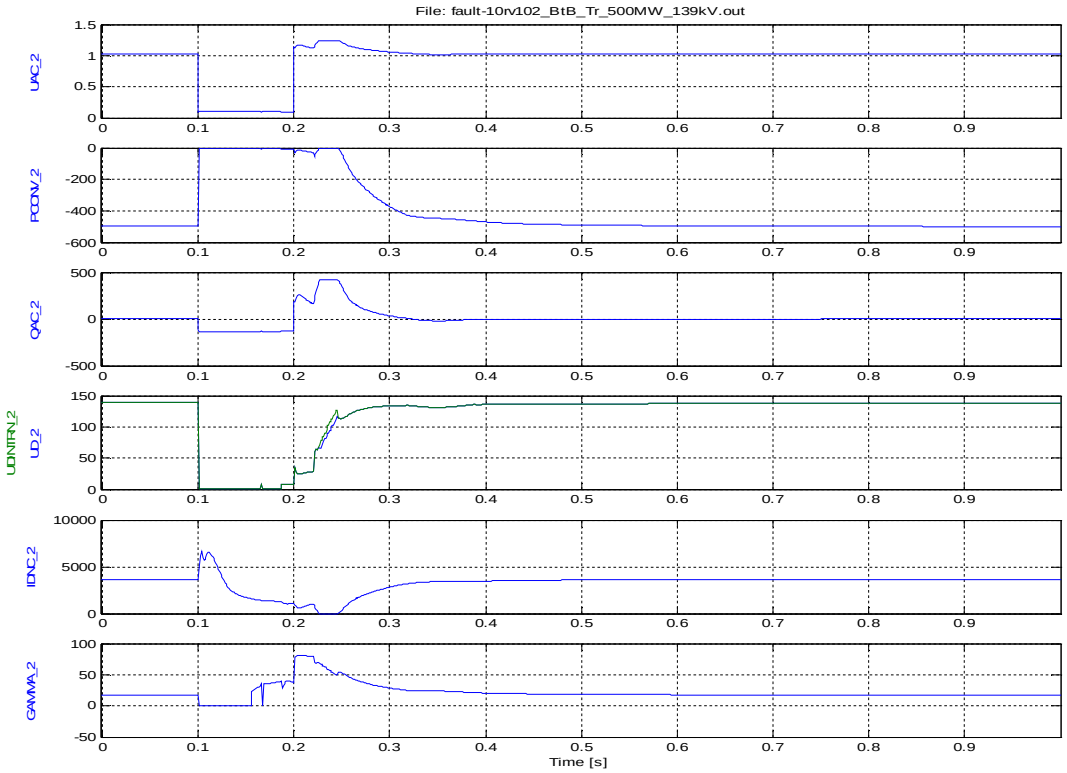


Figure 60 10% rem. Voltage 3-phase to ground ac fault at inverter (inverter side)

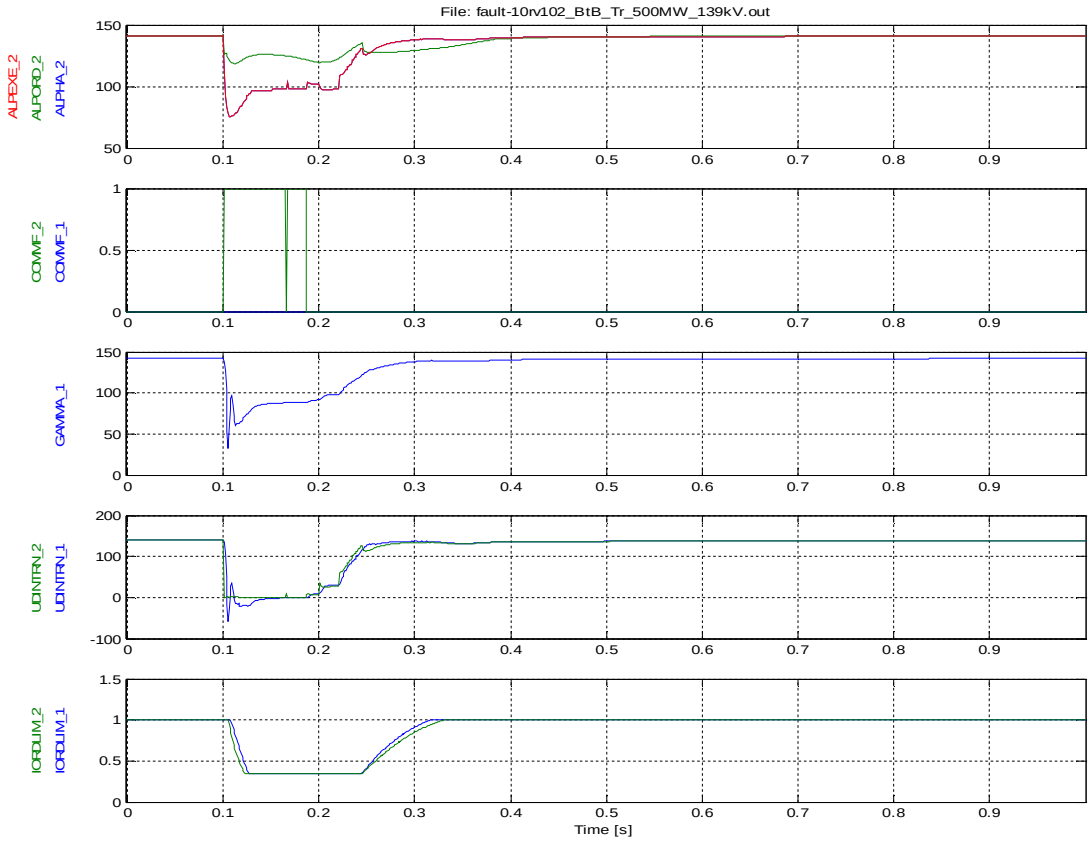


Figure 61 10% rem. Voltage 3-phase to ground ac fault at inverter

4.6.3.2 Three phase to ground AC fault at rectifier

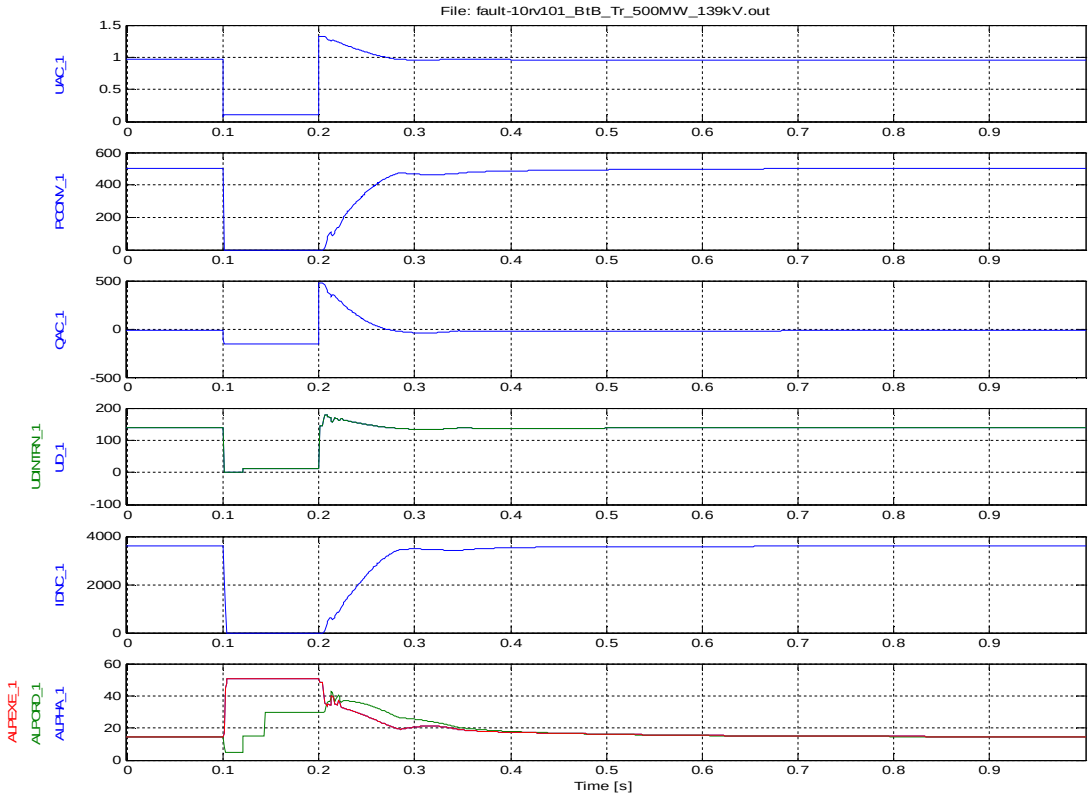


Figure 62 3-Phase to ground a.c. fault at rectifier (rectifier side)

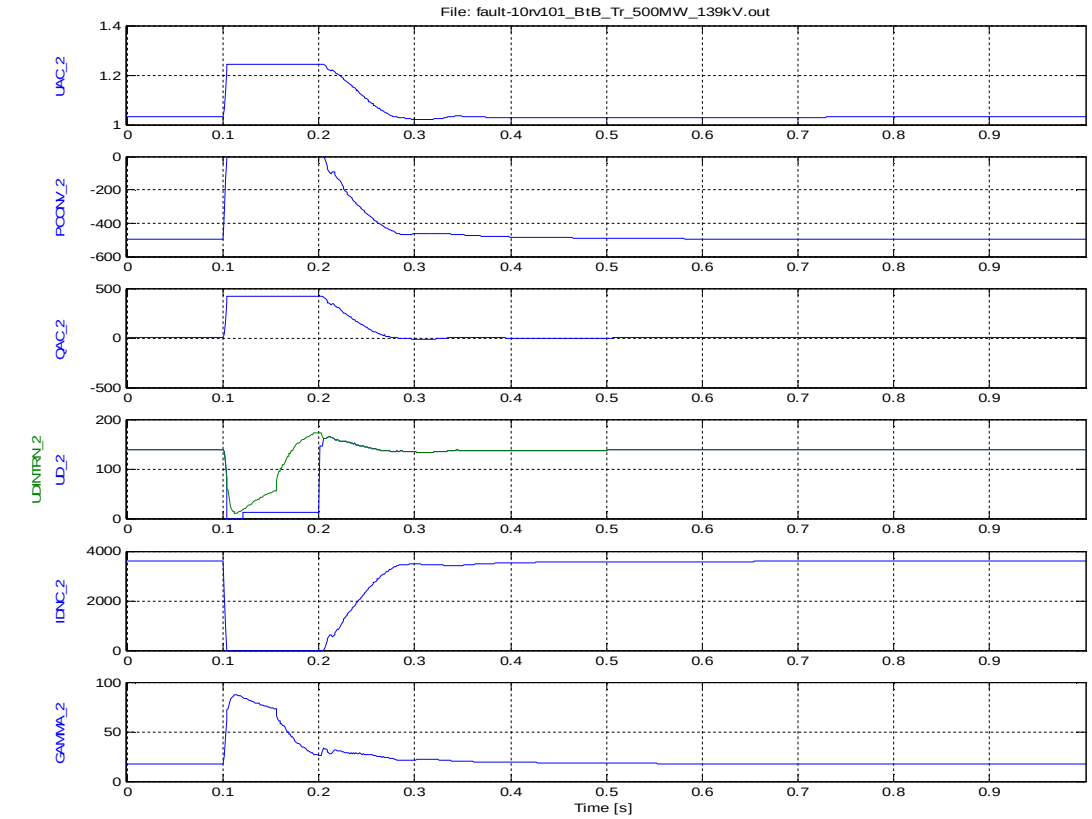


Figure 63 3-Phase to ground a.c. fault at rectifier(inverter side)

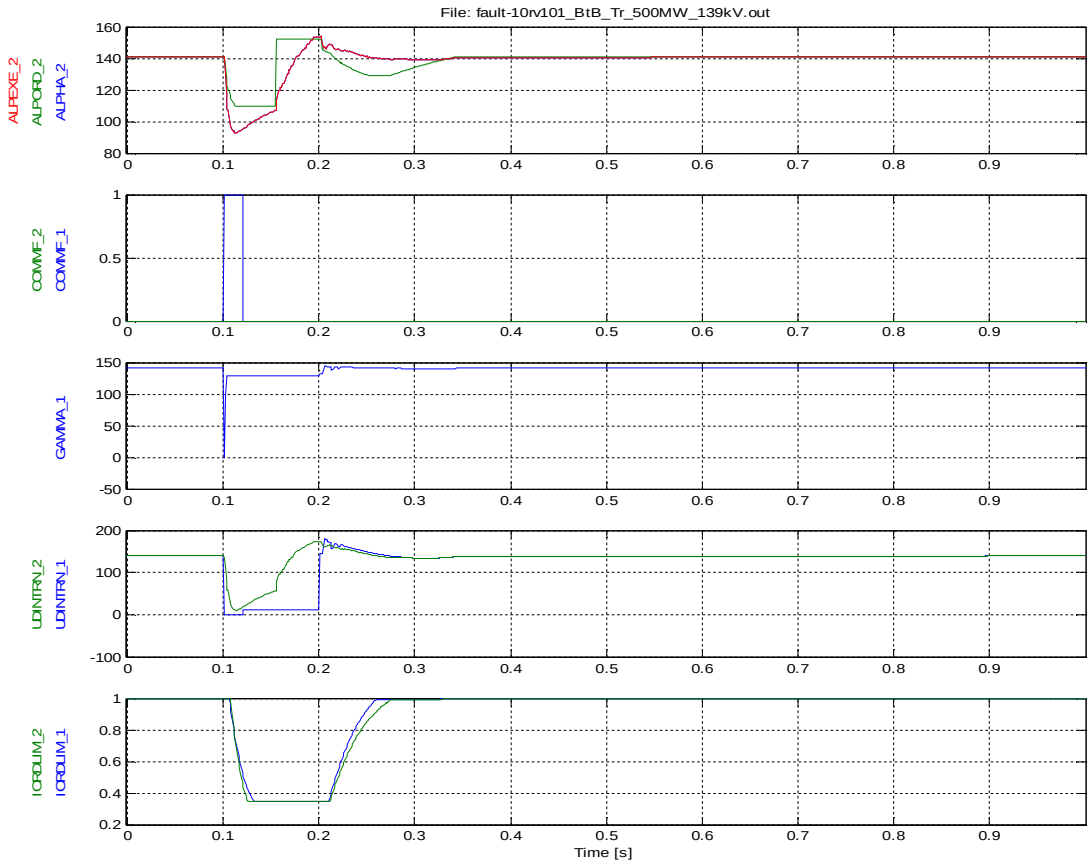


Figure 64 3-Phase to ground a.c. fault at rectifier

4.7 Conclusion:

The impacts of a.c. dynamics on d.c. system during and following of contingencies are presented to provide increased insight into the performance of HVDC system connected to weak ac network. It can be seen from the above figures that

a) Follows the basic HVDC classic control sequence during and following of faults.
b) The subsequent commutation failures at inverter have been improved. The rectifier commutation failure during inverter ac fault in cable transmission has been prevented.
c) There was no commutation failure occurs at rectifier during dc line fault close to rectifier.
d) The d.c. system is recovered to 90% of pre-fault power within reasonable recovery time after the fault clearing instant.
e) The recovery time of cable transmission dc system from rectifier side ac fault and inverter side ac fault are in the range of 100ms to 110ms and 160ms to 200ms respectively. The recovery time is longer compared to overhead line due to capacitance; it takes time to discharge and charging of cable.
f) The overhead transmission dc system recovered within 110ms from rectifier side ac faults and 150ms from inverter side ac faults.
g) The back to back system recovers in the range of 90 to 100ms for rectifier fault and 120ms to 150ms for inverter side ac faults.

h) As well as dc line faults also recovered to 90% of pre-fault power in typical time period.
i) The step responses in dc voltage reference, active power and gamma reference are well damped and controlled with typical response time (see section 2.4).

5.0 Nordic-32 network

The Nordic-32 network has been used to verify the HVDC control parameters. The node numbers starts with '4' are 400KV buses, '1' are 130KV buses and '2' are 220KV buses. The network is shown in appendix.
Base apparent power = 100 MVA
Base Impedance = 1600 ohm for 400KV line
Typical values
Resistance = 0.3 ohm/KM (duplex)
Inductance =1.3mH/km (single)
= 20% lower (duplex)
Capacitance = 9 .E-3 μF/km (single)
= 11.E-3 μF/km (double)

Node no.	**Geographic location**
4044	Nässjö-Norrköping-Hallsberg
4045	Hurva
4063	Barsebäck-Själland
4051	Oskarshamn-Karlshamn
1045	Västervik
4072	South of Finland
4047	Forsmark 1+2 + Dannebo
4042	Forsmark 3 + Finnböle
4040	oslo
4061	Göteborg (Lindome, Stenkullen)
701	Gotland (Ygne, Bäcks)
702	Gotland South (Näs)

Table 7 Geographical location and bus node numbers

In principle the Nordic32-system have no geographic locations of nodes. In this study, the following mappings of nodes to geographical locations are made.

Extension of Nordic-32 system:

Node no.	Bus generation/load/ line detail	Dynamic generador data	Dynamic exciter data
701	80KV bus with 50MW load and synchronous condenser (PSSE dynamic generator model GENCLS.	H=4, and X_d''=0.29	-
702	80KV bus with wind generation of 100MW (PSSE dynamic generator and exciter models are GENROU EXST1	T'_{do} =1.2 T''_{do} = 0.03 T'_{qo}=0.3 T''_{qo}= 0.06 H=5.04, D=0.02, X_d=3.29, X_q=2.96, X'_d=0.3, X'_q=0.889, X''_d=0.2, X_l=0.09	T_R =0, V_{IMAX}=2, V_{IMIN}=-2, T_C=1, T_B=10, K_A=50, T_A=0.15, V_{RMAX}=5, V_{RMIN}=-5, K_C=0, K_F=0
Branch 701-702	70km, R=0.14 p.u X=0.57 p.u. and Xc= 0.0097 p.u.		
4040	400KV bus generation of 1100 MW (PSSE dynamic	T'_{do} =1.2 T''_{do} = 0.03 T'_{qo}=0.3 T''_{qo}= 0.06 H=5.04, D=0.02,	T_R =0, V_{IMAX}=2, V_{IMIN}=-2, T_C=1, T_B=10, K_A=50,

	generator model GENROU is used) and load 1100MW(for proper load flow)	X_d=3.29, X_q=2.96, X'_d=0.3, X'_q=0.889, X''_d=0.2, X_l=0.09	T_A=0.15, V_{RMAX}=5, V_{RMIN}=-5, K_C=0, K_F=0
Branch 4040-4041	260km, R=0.006, X=0.05 p.u., and Xc=2.4 p.u.		
Branch 4045-4044	Disconnected		

Table 8 Parameters of extended Nordic 32-system

The PSSE dynamic generator models GENROU, GENSAL and GENCLS , exciter models SEXS, governor models HYGOV and stabilizer models STAB2A has been used.

There were five HVDC links added in Nordic-32 system, three HVDC classic and two HVDC light links. The power generation is mostly in the northern part, loads are in the central and southern part.
The power transmitted from north to central part is around 3260MW and to external part is around 0MW. Therefore, the HVDC links added between node 4072, 4047 and 4042 to reduce the power transmission in a.c. line.
The power transmission between node 4072 and 4047 is 500MW and between 4072 and 4042 is 800MW.
The third HVDC link between island of gotland and Swedish main land, wind generation of 100MW is transmitted from node 702 to 701 through HVDC light connected parallel with a.c. line. The next link is between node 701 and 1045 transmitting power of 50MW.
The fifth is HVDC light multi-terminal link between nodes 4040, 4044, and 4045. The active power 1100MW is transmitting from 4040, to 440MW to node 4044 and 600MW to 4045. The active power load 1100MW is added in central part of Sweden and also 400MVAr of reactive shunt compensators are disconnected. The adding of HVDC link and external loads reduce the overloading of transmission lines, and reduce the need of shunt compensations. The Nordic system is considerably very strong network, the short-circuit ratio is more than 10 at all buses.

External	North	Central	South
4071,4072	4011,4012,4021,4022, 4031,4032,2031,2032, 1011,1012,1013,1014, 1021	4041,4044,4046,4045, 4043,4047,4051,1041, 1043,1044,1042	4061,4062,4063

Table 9 Node numbers in each location

HVDC Link no. 1

	Rectifier (4072)	**Inverter (4047)**
Frequency in HZ	50	50
Rated power in MW	500	500
Rated DC voltage in KV	500	500

Configuration/distance	Monopole HVDC classic cable transmission/ 200Km	
AC voltage in KV	400	400
SCR	> 10	>10

Table 10 HVDC link no.1 data

HVDC Link no. 2

	Rectifier (4072)	**Inverter (4042)**
Frequency in HZ	50	50
Rated power in MW	800	800
Rated DC voltage in KV	500	500
Configuration /distance	Monopole HVDC classic cable transmission/ 200Km	
AC voltage in KV	400	400
SCR	> 10	>10

Table 11 HVDC link no.2 data

HVDC Link no. 3

	Rectifier (701)	**Inverter (1045)**
Frequency in HZ	50	50
Rated power in MW	260	260
Rated DC voltage in KV	300	300
Configuration / distance	Bipolar HVDC classic cable transmission / 2x96 Km	
AC voltage in KV	80	130
SCR		>10
Transmitting power in MW	50	50

Table 12 HVDC link no.3 data

HVDC link no. 4

	Rectifier (702)	**Inverter (701)**
Frequency in HZ	50	50
Rated power in MW	50	50
Rated DC voltage in KV	80	80
Configuration/ distance	HVDC light cable transmission / 2x70Km	

AC voltage in KV	80	80
SCR	>10	>10

Table 13 HVDC link no.4 data

HVDC link no. 5

	Rectifier (4040)	**Inverter (4044)**	**Inverter(4045)**
Frequency in HZ	50	50	50
Rated power in MW	1100	440	600
Rated DC voltage in KV	320	320	320
Configuration	HVDC light multi-terminal/ 200Km		
AC voltage in KV	400	400	400
SCR	>10	>10	

Table 14 HVDC link no.5 data

Suggested Fault nodes:

Node no.	**Geographical name**	**Fault type/ remaining voltage**	**Fault duration**
4072	South of Finland	3-phase to ground/ 10%	100ms
4040	Oslo	3-phase to ground/ 10%	100ms
4042	Forsmark 3 + Finnböle	3-phase to ground/ 10%	100ms
4045	Hurva	3-phase to ground/ 10%	100ms

Table 15 fault nodes

The benchmark models are recalculated with respect to the real system and modeled in PSSE. Then the benchmark model with new control parameters are added with existing Nordic-32 network. In order to verify the optimized VDCOL and CCA parameters, shunt faults are applied at the suggested nodes shown in Table 15. The simulated results are shown below.

5.1 Modified Nordic-32 network with HVDC links

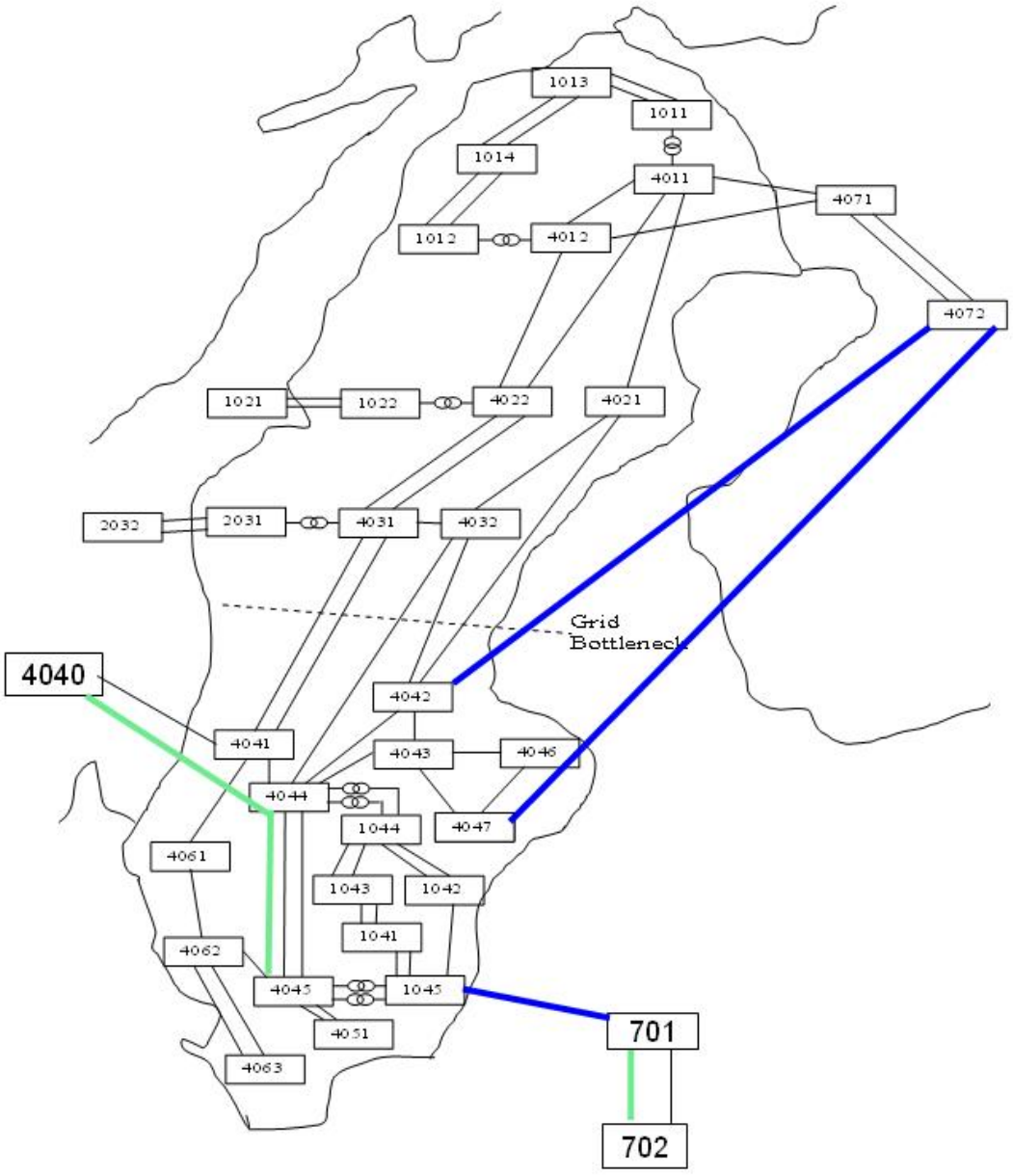


Figure 65 Map of Nordic-32 system

The blue lines in the figure(56) shows HVDC classic links and green lines are HVDC light links.

5.2 3-phase to ground fault at node 4072

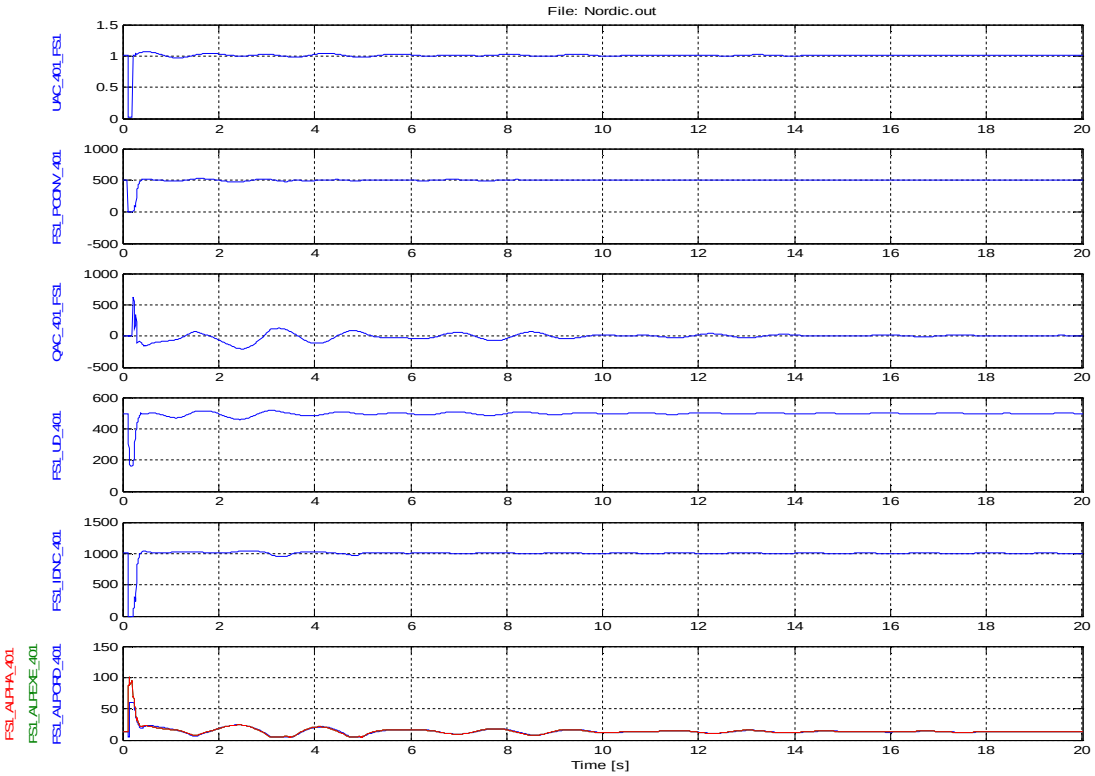


Figure 66 Recifier side of HVDC link no. 1(node 4072)

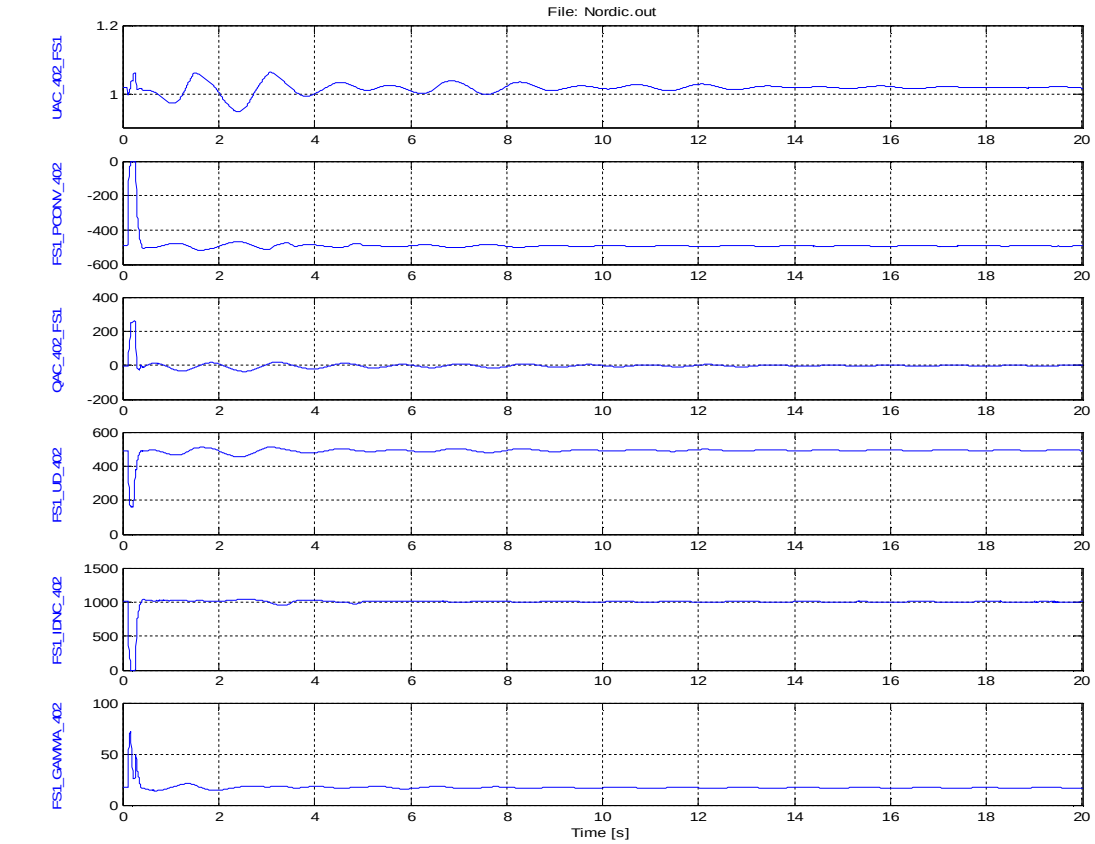


Figure 67 Inverter side of HVDC link no.1(node 4047)

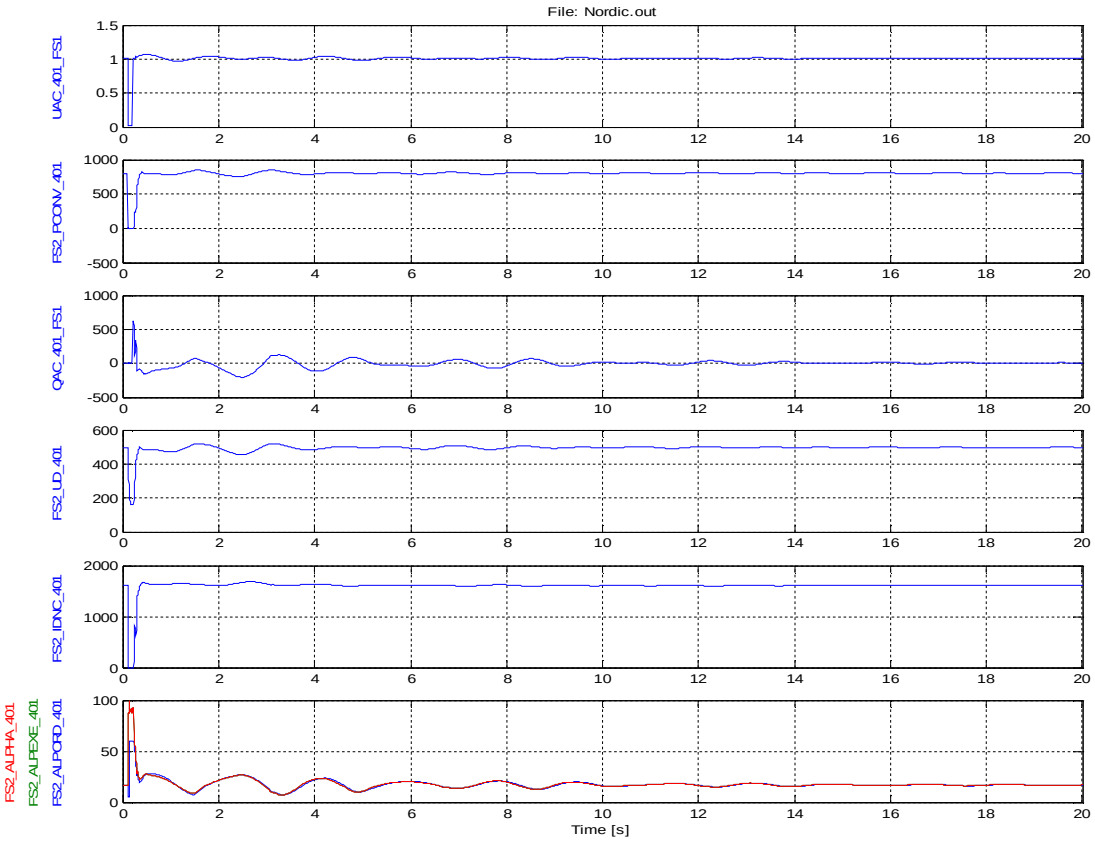


Figure 68 Rectifier side of HVDC link no.2(4072)

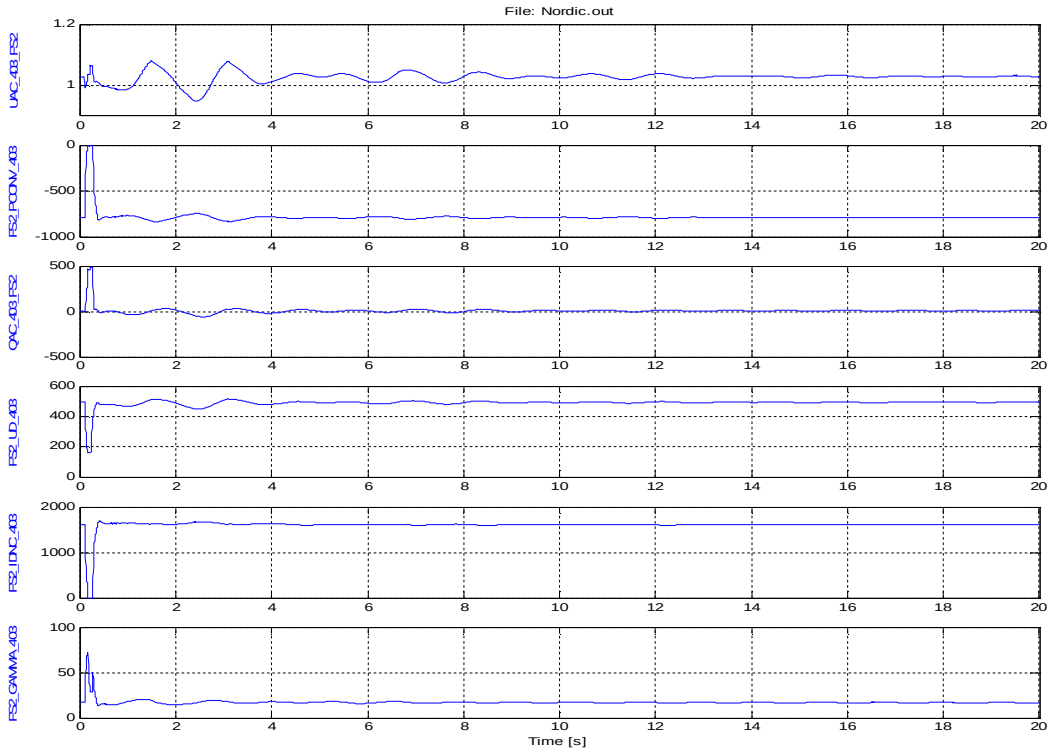


Figure 69 Inverter side of HVDC link no. 2 (4042)

5.3 3-phase to ground fault at node 4042

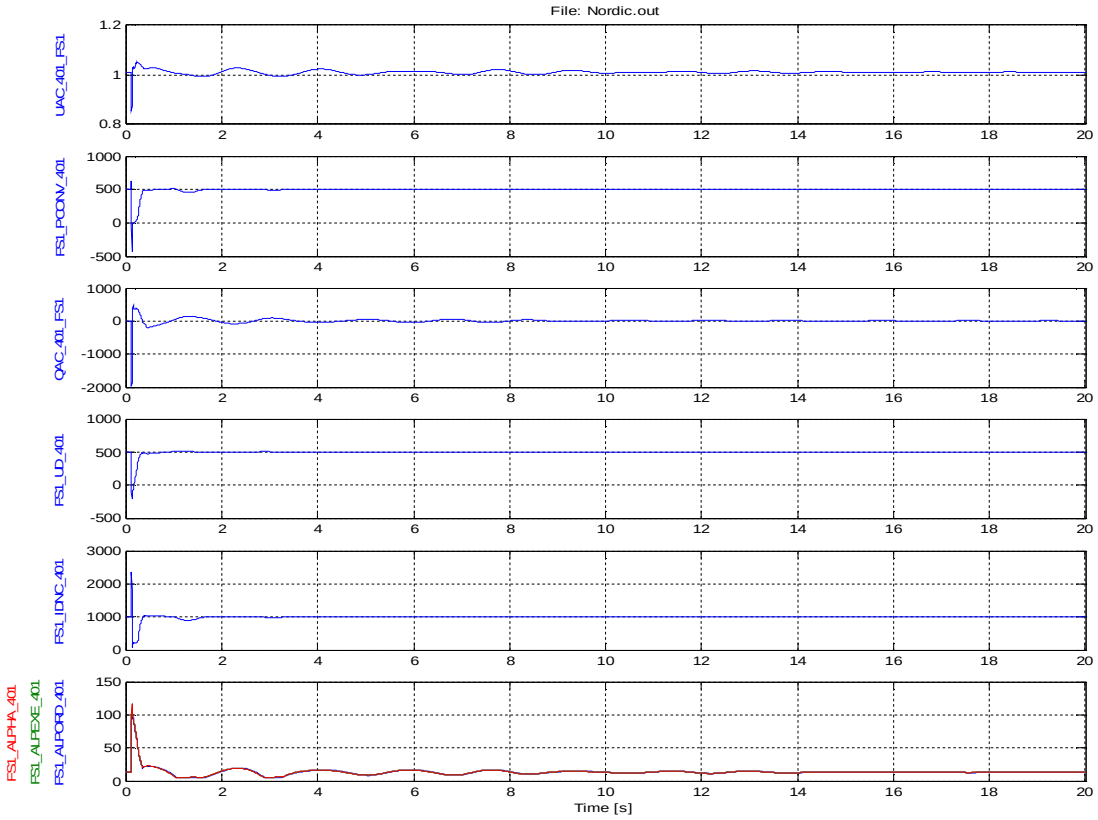


Figure 70 Rectifier side of HVDC link no.1 (4072)

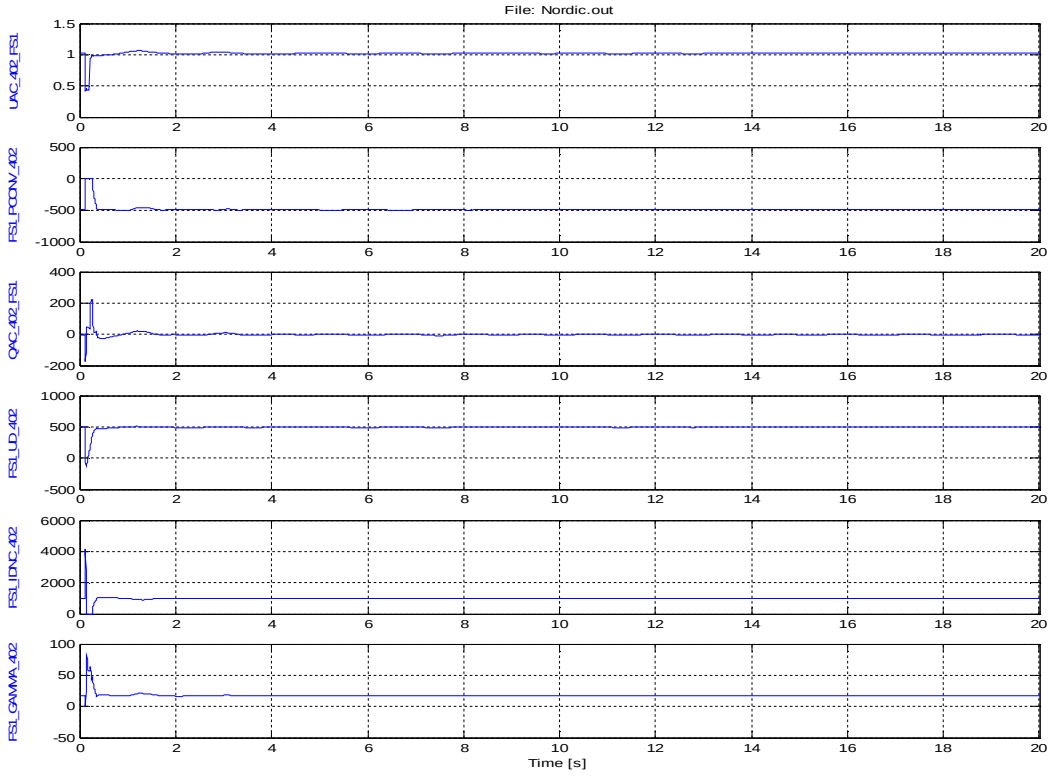


Figure 71 Inverter side of HVDC link no.1(4047)

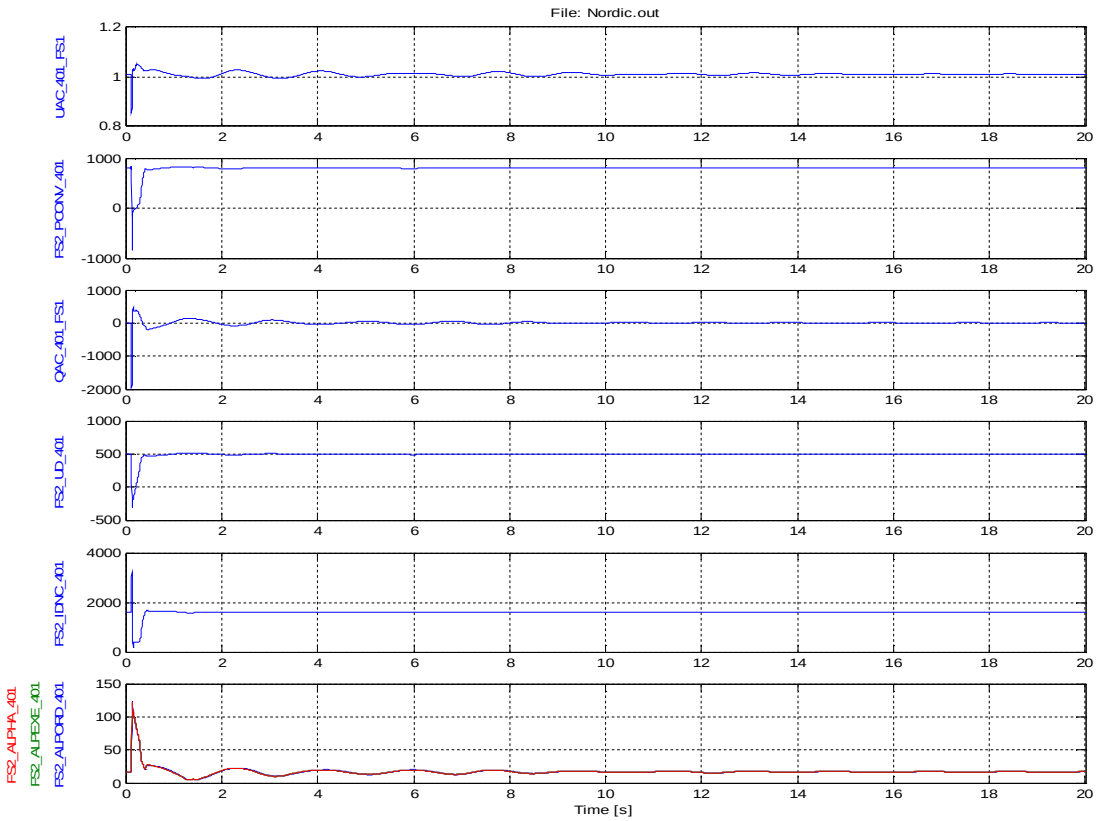


Figure 72 Rectifier side of HVDC link no.2 (4072)

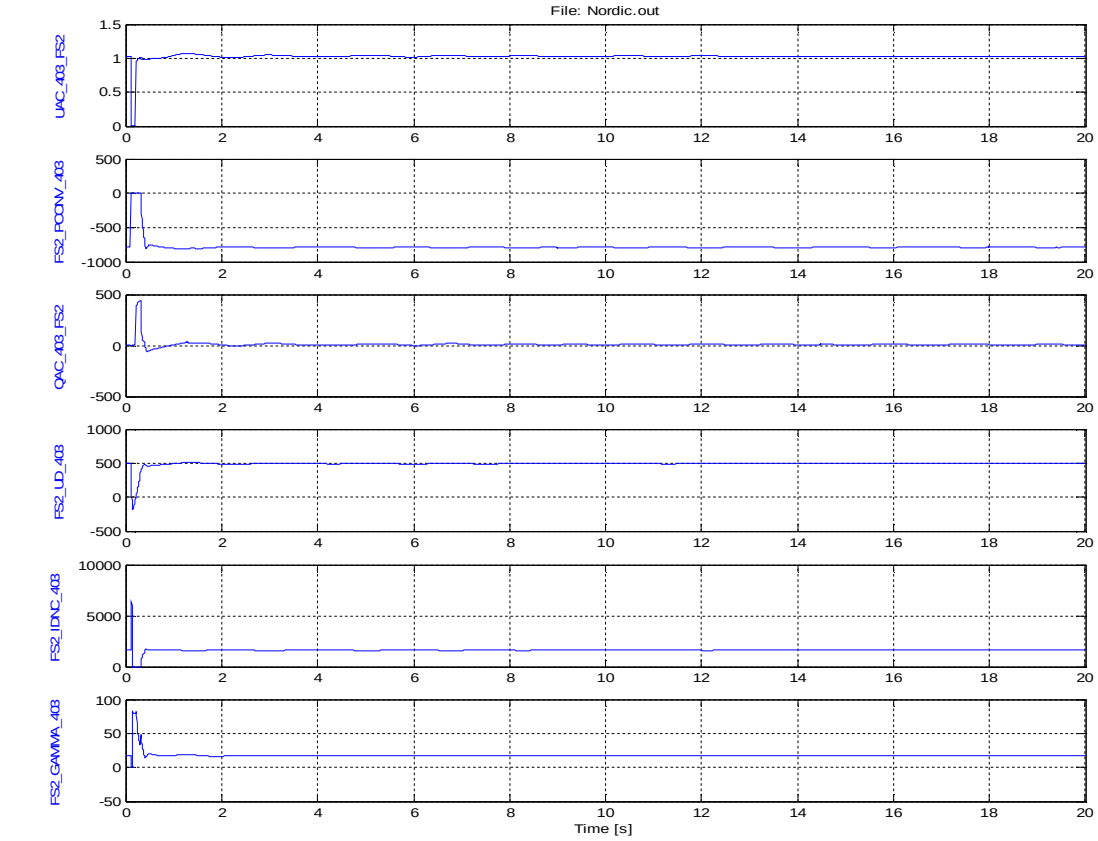


Figure 73 Inverter side of HVDC link no.2 (4042)

5.4 3-phase to ground fault at node 4045

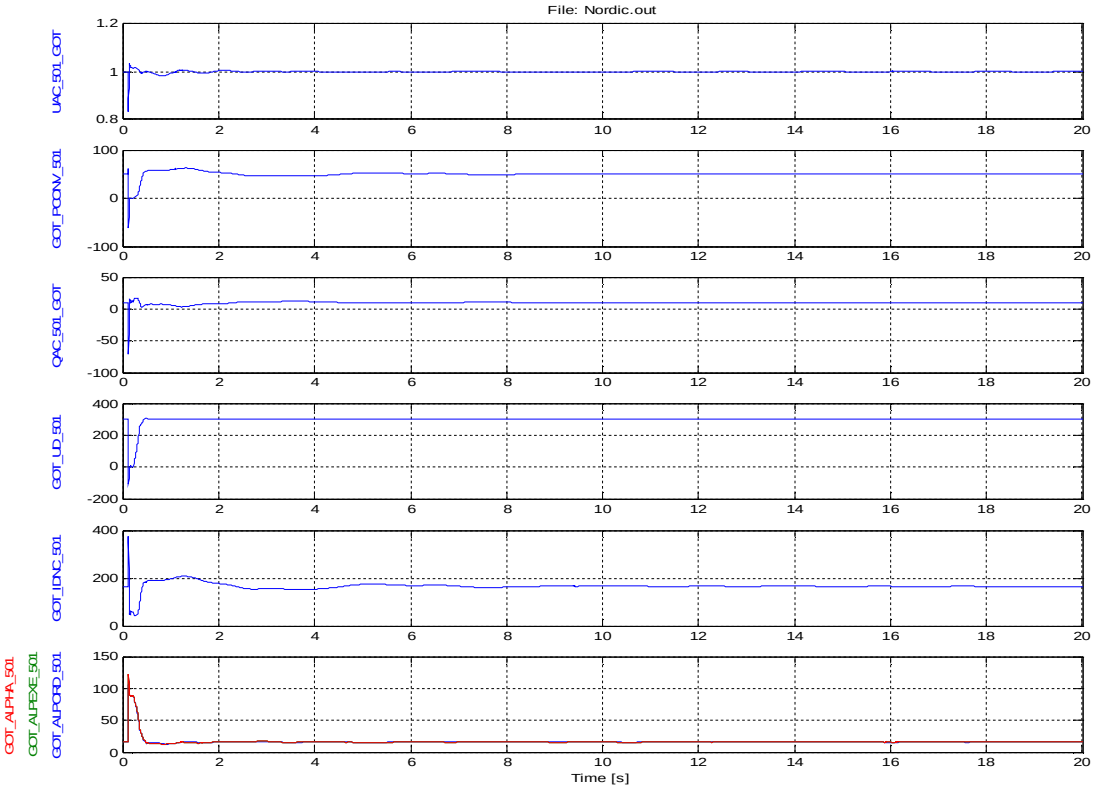


Figure 74 Rectifier side of HVDC link no.5 (4040)

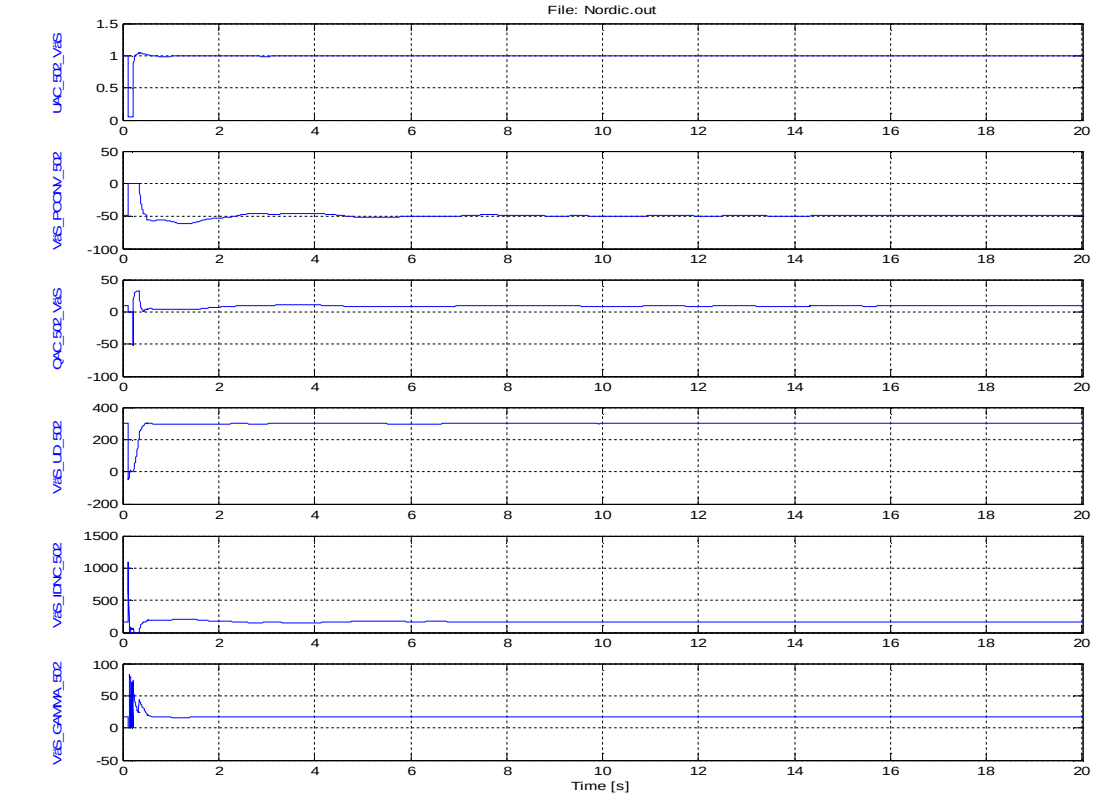


Figure 75 Inverter side of HVDC link no. 5 (4045)

5.5 3-Phase to ground fault at node 4040

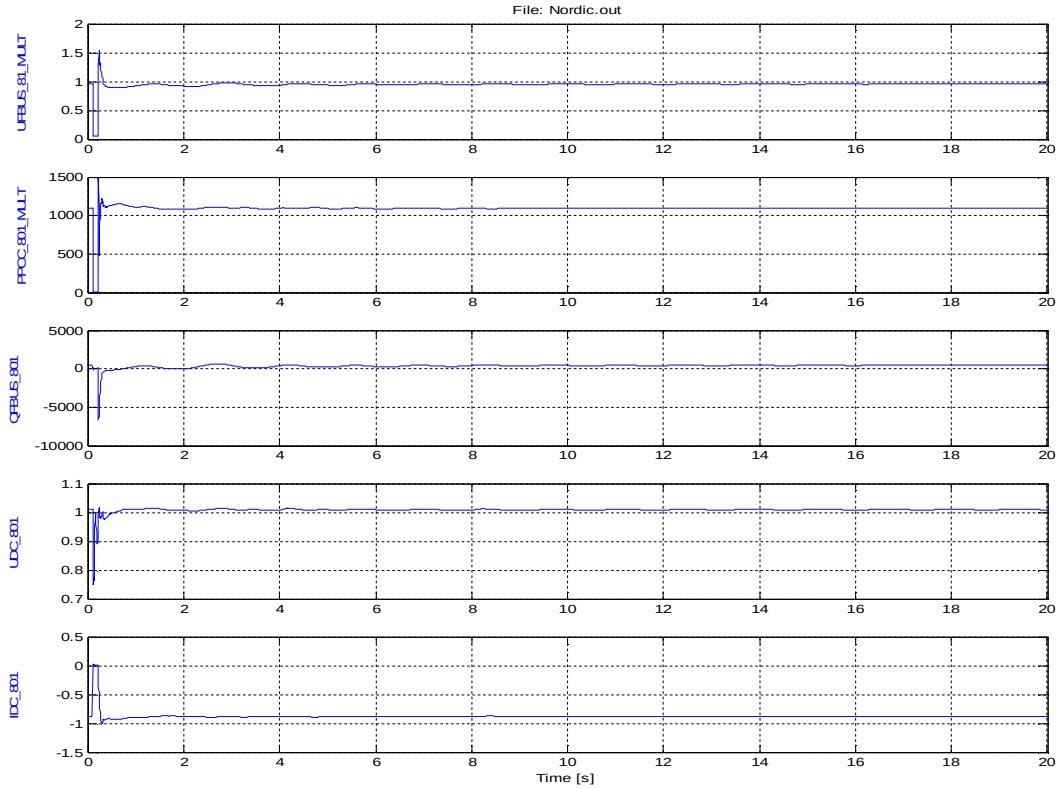


Figure 76 Rectifier side of HVDC link no. 5 (4040)

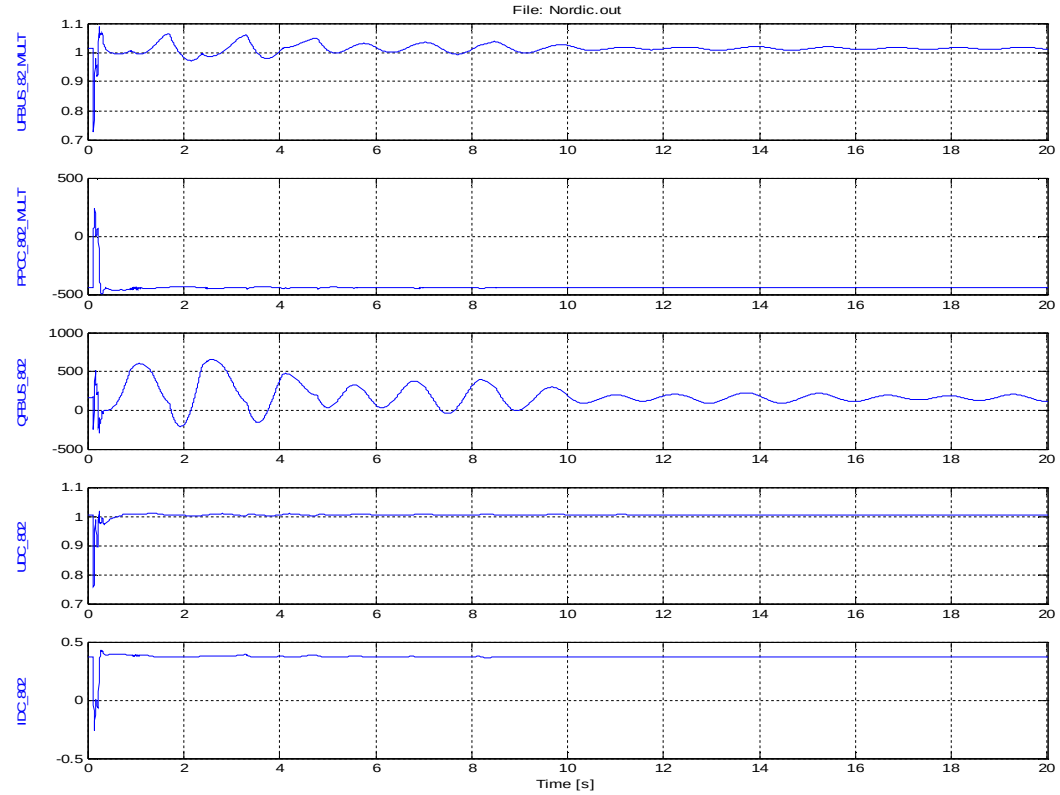


Figure 77 Inverter side of HVDC link no. 5 (4044)

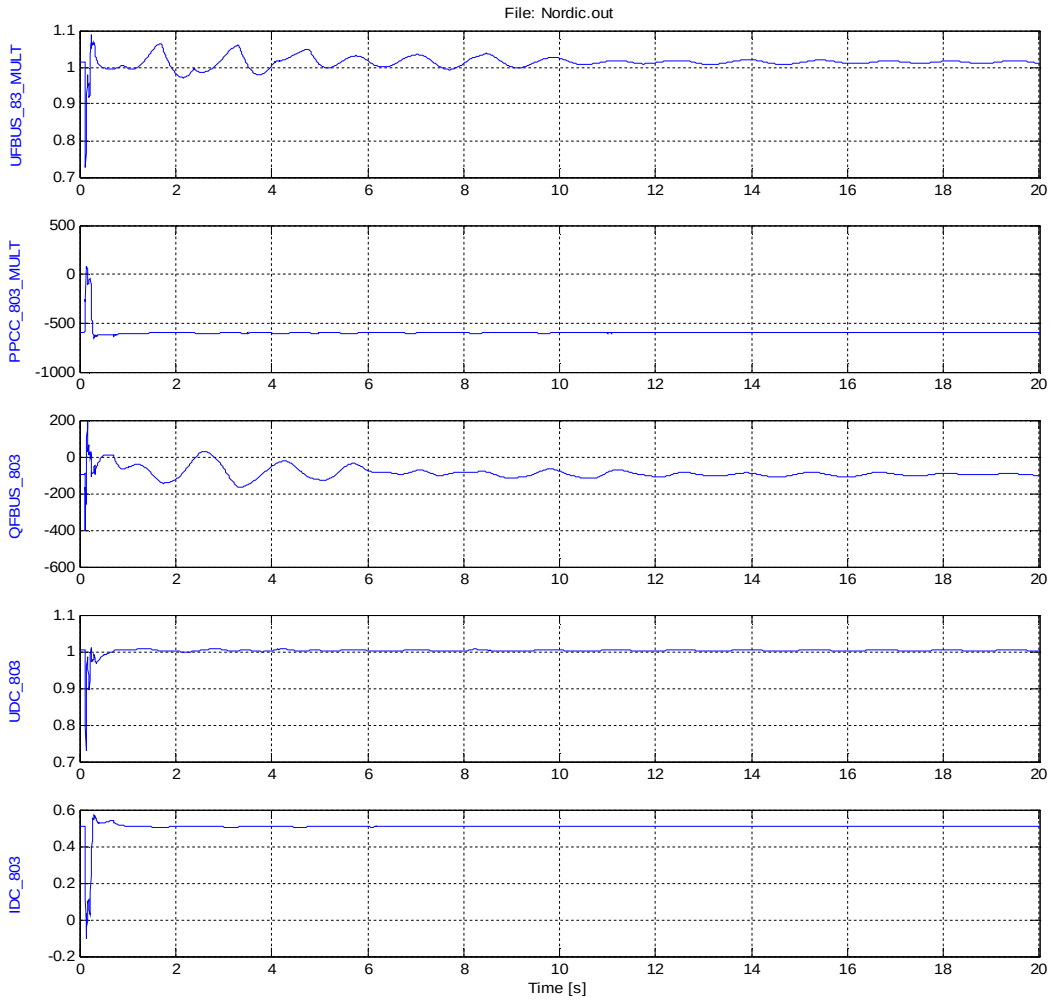


Figure 78 Inverter side of HVDC link no.5 (4045)

5.6 Conclusion:

In above simulation results proved that it's possible to run number of HVDC links in same simulation and also possible to run both HVDC classic and HVDC light in same simulation. Nordic-32 system is extended with five HVDC links in PSSE; load flow of this network has been solved with zero mismatch real and reactive power, and system is simulated with suggested shunt faults. The simulation results above are seen to be successfully handled the contingency of the system. The parameters are robust, independent of different types of HVDC configurations. It is proved that optimized parameters could manage the faults in largest network with strong and weak ac system also. Since the response is well damped and controlled for strong system with weak system parameters. The frequency controller has been used at Gotland and mainlands of Sweden in order to reduce the frequency deviations at disturbances hence reduce the increase of phase angle between the two isolated buses.

6.0 Future work:

There are some works can be done in future

- The tuning of current controller had been done by simple trial and error method in time –domain model in PSSE. It could be interest to analyze the HVDC system dynamic stability by frequency domain model in Matlab.(**17**)
- The dynamics of HVDC control are tuned by using infinite AC system; it will be interest to do small signal stability analysis by using real or weak ac system.
- In Nordic system, five HVDC links had been added between strong ac networks. It could be interest to check the dynamic performance of HVDC links with weak ac networks.
- And it will be good to add more number of HVDC links in Nordic system in PSSE and analyze the dynamic performance.

7.0 Reference:

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8.0 Appendix:

8.1 The case study simulation results (version 3.0.14.beta)

	Length of line/cable In KM	Recovery time 10% rem. volt	Commutation failure occurs at %remaining voltage	DC fault at node 1 restart with 80% rem.volt
MidpGrCable_Tr_1000MW_900kV_rec	300	80ms		207ms
MidpGrCable_Tr_1000MW_900kV_inv		265ms	95%	
MidpGrCable_Tr_600MW_900kV_rec.	300	93ms		221ms
MidpGrCable_Tr_600MW_900kV_inv.		276ms	95%	
LineTr_Monopol_MetRet_3600MW_800kV_rec.	2000	100ms		430ms
LineTr_Monopol_MetRet_3600MW_800kV_inv.		113ms	85%	
LineTr_Monopol_MetRet_3000MW_800kV_rec	2000	100ms		420ms
LineTr_Monopol_MetRet_3000MW_800kV_inv		111ms	85%	
LineTr_Monopol_MetRet_2500MW_800kV_rec	2000	100ms		412ms
LineTr_Monopol_MetRet_2500MW_800kV_inv		126ms	85%	
LineTr_Monopol_MetRet_2000MW_660kV_rec	2000	100ms		410ms
LineTr_Monopol_MetRet_2000MW_660kV_inv		128ms	85%	
LineTr_Monopol_MetRet_1575MW_600kV_rec	1500	100ms		400ms
LineTr_Monopol_MetRet_1575MW_600kV_inv		118ms	85%	
LineTr_Monopol_MetRet_1500MW_500kV_rec	1000	100ms		370ms
LineTr_Monopol_MetRet_1500MW_500kV_inv		124ms	80%	
LineTr_Monopol_MetRet_1000MW_500kV_rec	1000	100ms		336ms
LineTr_Monopol_MetRet_1000MW_500kV_inv		135ms	80%	
LineTr_Monopol_3600MW_800kV_rec.	2000	100ms		380ms
LineTr_Monopol_3600MW_800kV_inv.		143ms	85%	
LineTr_Monopol_3000MW_800kV_rec	2000	105ms		377ms
LineTr_Monopol_3000MW_800kV_inv		130ms	85%	
LineTr_Monopol_2500MW_800kV_rec	2000	100ms		355ms
LineTr_Monopol_2500MW_800kV_inv		118ms	90%	
LineTr_Monopol_2000MW_660kV_rec	2000	100ms		350ms
LineTr_Monopol_2000MW_660kV_inv		127ms	85%	
LineTr_Monopol_1575MW_600kV_rec	1500	100ms		350ms
LineTr_Monopol_1575MW_600kV_inv		125ms	85%	
LineTr_Monopol_1500MW_500kV_rec	1000	100ms		324ms
LineTr_Monopol_1500MW_500kV_inv		130ms	80%	
LineTr_Monopol_1000MW_500kV_rec	1000	100ms		273ms
LineTr_Monopol_1000MW_500kV_inv		136ms	80%	
LineTr_Binopol_7200MW_800kV_rec.	2000	100ms		332ms
LineTr_Binopol_7200MW_800kV_inv.		133ms	90%	
LineTr_Binopol_6000MW_800kV_rec.	2000	100ms		320ms
LineTr_Binopol_6000MW_800kV_inv.		138ms	90%	
LineTr_Binopol_5000MW_800kV_rec.	2000	100ms		302ms
LineTr_Binopol_5000MW_800kV_inv.		152ms	90%	
LineTr_Binopol_4000MW_660kV_rec.	1500	100ms		296ms
LineTr_Binopol_4000MW_660kV_inv.		124ms	90%	
LineTr_Binopol_3150MW_600kV_rec.	1500	100ms		288ms
LineTr_Binopol_3150MW_600kV_inv.		125ms	90%	
LineTr_Binopol_3000MW_500kV_rec.	1000	100ms		261ms

LineTr_Binopol_3000MW_500kV_inv.		139ms	85%	
LineTr_Binopol_2000MW_500kV_rec.	1000	100ms		235ms
LineTr_Binopol_2000MW_500kV_inv.		142ms	85%	
LineTr_2xMonopol_7200MW_800kV_rec.	2000	100ms		322ms
LineTr_2xMonopol_7200MW_800kV_inv.		134ms	90%	
LineTr_2xMonopol_6000MW_800kV_rec	2000	100ms		287ms
LineTr_2xMonopol_6000MW_800kV_inv		139ms	90%	
LineTr_2xMonopol_5000MW_800kV_rec	2000	100ms		289ms
LineTr_2xMonopol_5000MW_800kV_inv		152ms	90%	
LineTr_2xMonopol_4000MW_660kV_rec	1500	100ms		283ms
LineTr_2xMonopol_4000MW_660kV_inv		127ms	90%	
LineTr_2xMonopol_3150MW_600kV_rec	1500	105ms		280ms
LineTr_2xMonopol_3150MW_600kV_inv		125ms	90%	
LineTr_2xMonopol_3000MW_500kV_rec	1000	ms		250ms
LineTr_2xMonopol_3000MW_500kV_inv		125ms	90%	
LineTr_2xMonopol_2000MW_500kV_rec	1000	100ms		228ms
LineTr_2xMonopol_2000MW_500kV_inv		142ms	85%	
Cable_Tr_Monopol_MetRet_800MW_500kV_rec.	300	104ms		220ms
Cable_Tr_Monopol_MetRet_800MW_500kV_inv.		178ms	95%	
Cable_Tr_Monopol_MetRet_500MW_500kV_rec	300	100ms		220ms
Cable_Tr_Monopol_MetRet_500MW_500kV_inv		178ms	95%	
Cable_Tr_Monopol_800MW_500kV_rec.	300	100ms		222ms
Cable_Tr_Monopol_800MW_500kV_inv.		166ms	95%	
Cable_Tr_Monopol_500MW_500kV_rec	300	100ms		227ms
Cable_Tr_Monopol_500MW_500kV_inv		202ms	95%	
Cable_Tr_Binopol_1600MW_500kV_rec	300	100ms		218ms
Cable_Tr_Binopol_1600MW_500kV_inv		182ms	95%	
Cable_Tr_Binopol_1000MW_500kV_rec	300	100ms		225ms
Cable_Tr_Binopol_1000MW_500kV_inv		186ms	95%	
Cable_Tr_2xMonopol_1600MW_500kV_rec.	300	100ms		190ms
Cable_Tr_2xMonopol_1600MW_500kV_inv.		168ms	95%	
Cable_Tr_2xMonopol_1000MW_500kV_rec.	300	100ms		190ms
Cable_Tr_2xMonopol_1000MW_500kV_inv.		200ms	95%	
BtB_Tr_600MW_167kV_rec.	-	80ms		
BtB_Tr_600MW_167kV_inv.		136ms	85 %	
BtB_Tr_500MW_139kV_rect	-	80ms		
BtB_Tr_500MW_139kV_inv		146ms	85 %	
BtB_Tr_150MW_42kV_rec.	-	80ms		
BtB_Tr_150MW_42kV_inv.		150ms	85 %	

Table 1

*_rec = rectifier side fault

_inv= inverter side fault

8.2 Nordic-32 network

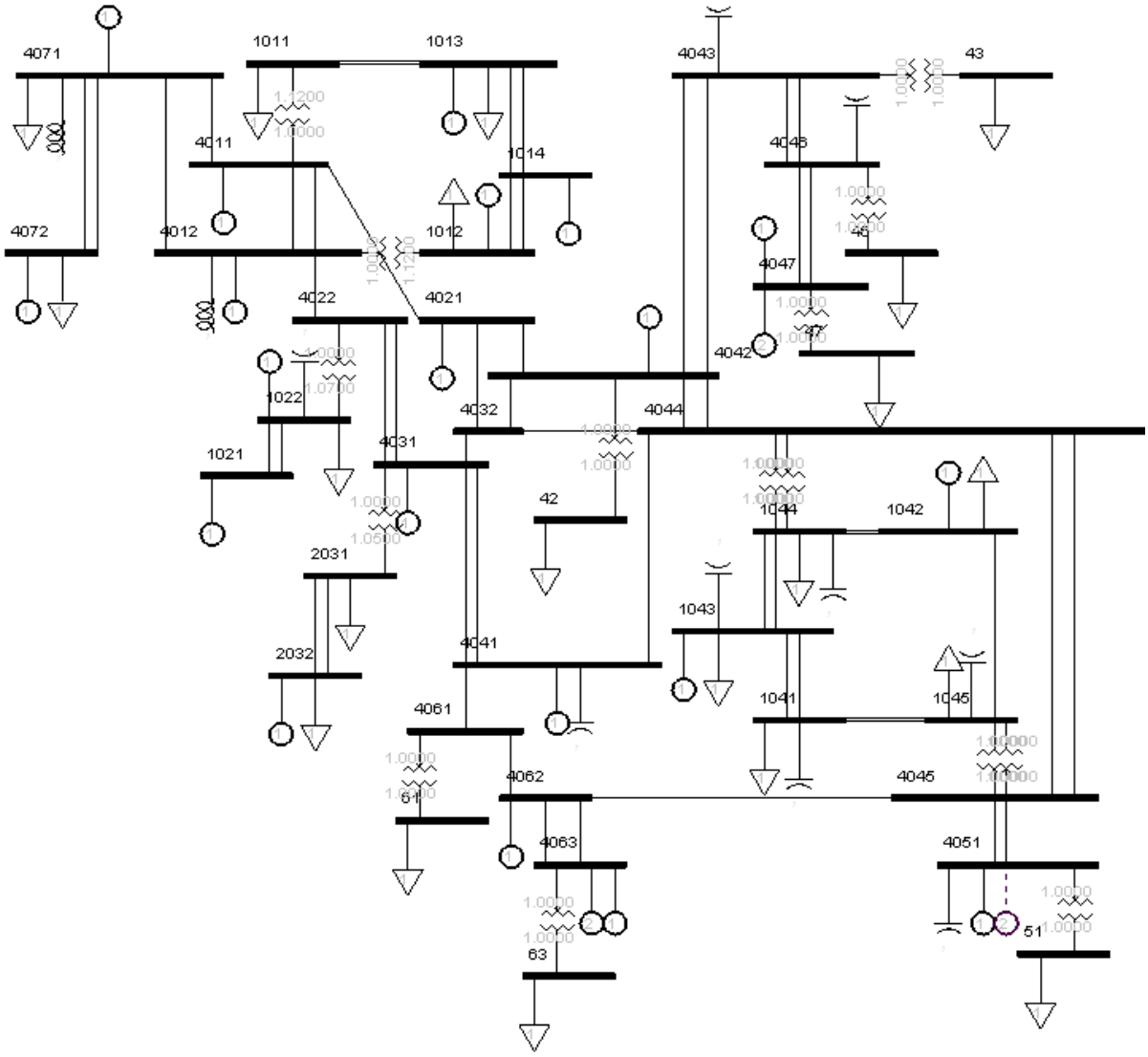

Figure 79

8.3 Frequency dependent representation of DC system

Introduction:
In ac/dc power systems, current and voltage oscillations in dc system during transients are quite common if the damping at high frequencies are not properly represented. Electromagnetic transient programs are normally used for dynamic and harmonic stability studies. Root mean square models like PSSE are used for load flow and stability studies.
In the simulation of fault transients on transmission lines (overhead lines/cables), the line parameters should be frequency dependent in order to damp the oscillations on the line.
In PSCAD, there is already inbuilt frequency dependent model is available. But, in root mean square(rms) models like PSS/E we have to create a frequency dependent model to damp the oscillations during and following of the transient period.

PI Equivalent Circuit:
Robust frequency dependent model for time domain transient simulation is created by parallel RL branches. The capacitance is constant for all frequencies, it does not effect on resultant impedance for certain length.

Background of oscillation:

The dc system with no higher frequency damping represented creates oscillations of 30Hz during the transient period. This oscillation produces unnecessary consecutive commutation failures at both stations during and following of the fault in ac system.

At dc, the current flowing through the conductor would be evenly distributed over the cross section. This is also one of the main reasons for using dc instead ac transmission. However, during the sudden disturbances in ac system induces time varying magnetic field and electric field; it causes an uneven distribution of current over the cross section of the conductor. This current flows only in the outer layer of the conductor, which in turn the resistance of the conductor increases and the internal inductance decreases. Such as called skin effect. Another important source of damping in the system at higher frequency is that the return current is forced closer to the main conductor, and uses a less “return area”. This is in opposite at direct current, were in principle the whole sea or soil can be used as return path, and the area is infinite large giving zero resistance.

Basic concept:
There are different layers in the cable 1) conductor 2) inner insulation 3) sheath 4) outer insulation layer 5)armor 6)insulation
Inner insulation (XLPE) layer is to ensure there is no electrical connection between conductors and sheath. The semiconducting layers also present between the conducting and non conducting layers in order to reduce the electrical stresses. Cable sheath is used as an return path for cable charging currents. Outer insulation layer is used to provide mechanical protections against surroundings. The purpose of steel armor is to provide mechanical strength.

In long HVDC cable transmission system, the lead sheath and steel armor of the cable are always connected together and earthed to the local earthing system at two terminations. The dc voltage is applied on the insulation between main conductor and lead sheath. The dc and low frequency current go through the main conductor and return through three different ways
a) The lead sheath b) the armor and c) the sea water
Impedance of cable system is highly frequency dependent. Therefore for the dynamic studies, we should use frequency dependent model to damp some unwanted oscillations in the system
The cable models in PSCAD, the line parameters are distributed and it exhibiting frequency dependent characteristics like damping. But in rms models, the line parameters are lumped in to 2xPI representation; this means that some high frequency oscillations are not damped during transients. The dc system frequency impedance scan has been done including transformer impedance. Since transformer impedance would also provide damping during commutation. As it can be seen from the Figure 80 Figure 81 resonance occurs at 30 Hz. Hence, current oscillations in the dc system create instabilities during heavy disturbances in ac system.

It seems easiest way to calculate the damper impedance to damp 30 HZ frequency oscillation. The base case used for this verification is existing project cable parameters. It has been

modelled using these cable parameters in PSCAD using Bergeron frequency dependent model. The frequency impedance graphs are shown in page below and also using the same cable parameters, lumped PI model shall be created. Then, by change the impedance of the PI network by trail and error method to match the Bergeron frequency dependent model impedance curve in the range of low frequencies such as 0 to 30Hz.

The PI link representation parameters are taken from existing cable project(190Km).The inductance L0=1.96mH/Km and C0=0.302microF/Km. These values are calculated without armor grounded.

.

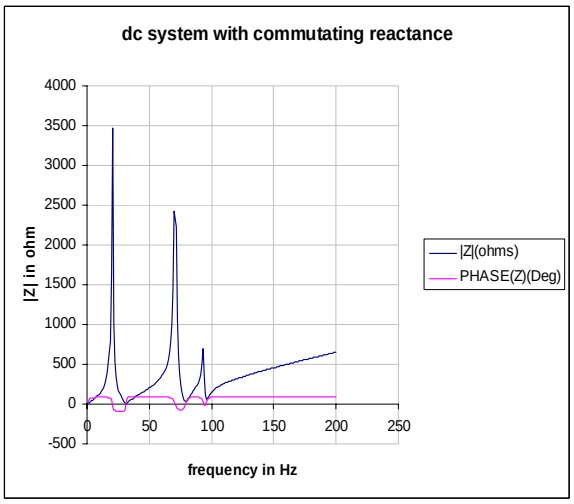

Figure 80

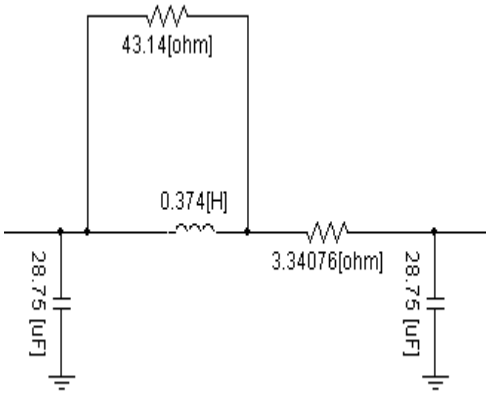

Figure 81

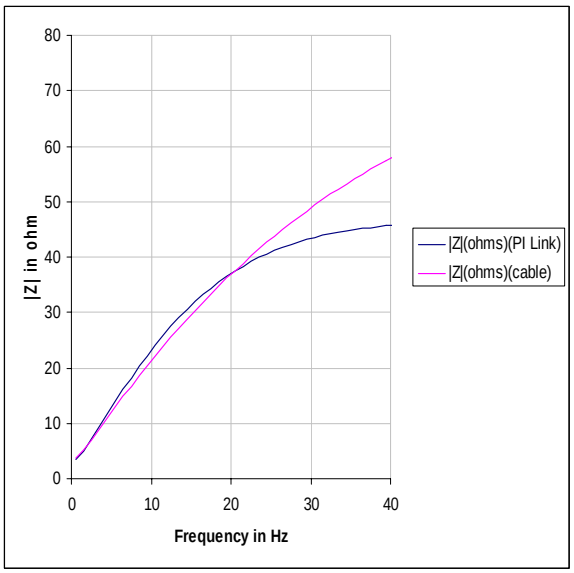

Figure 82

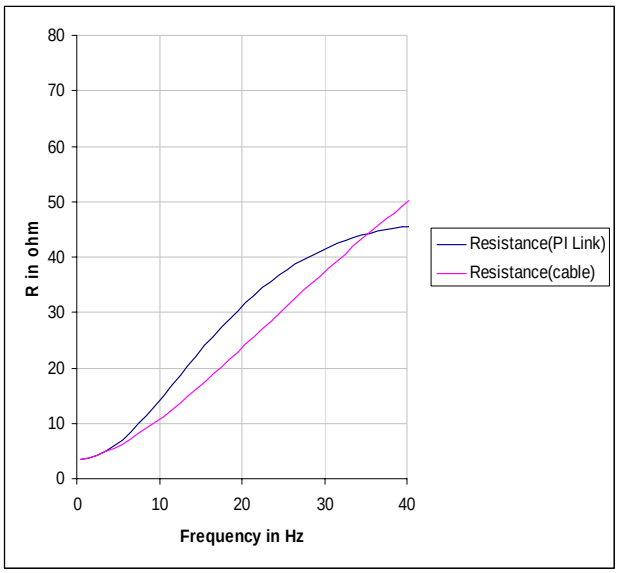

Figure 83

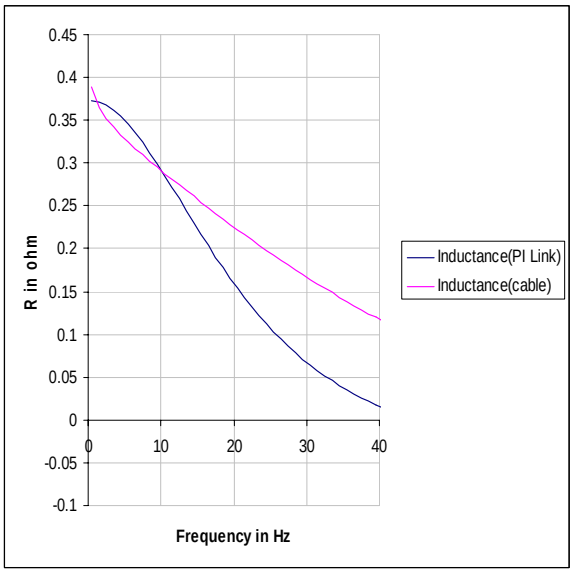

Figure 84

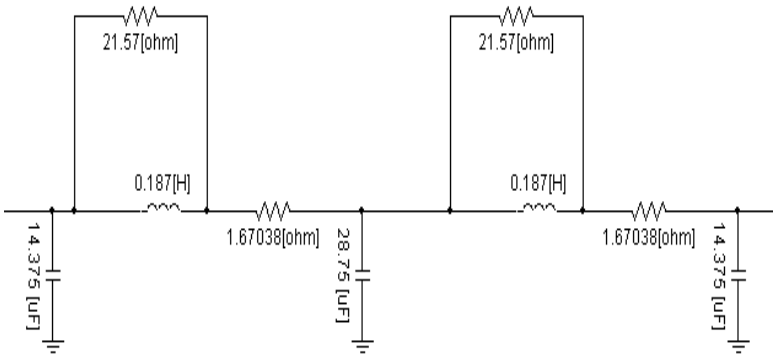

Figure 85

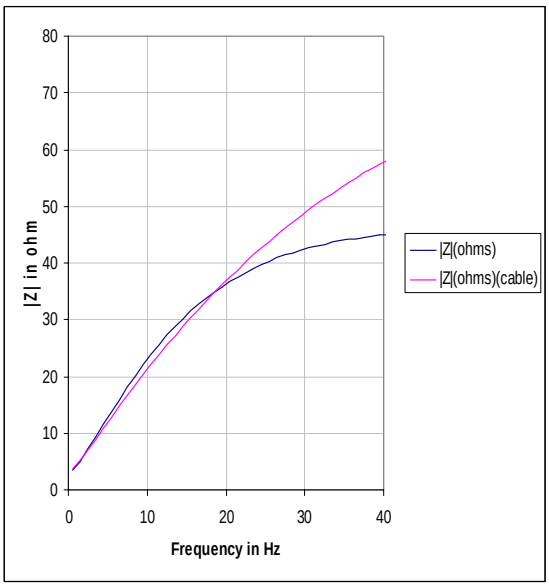

Figure 86

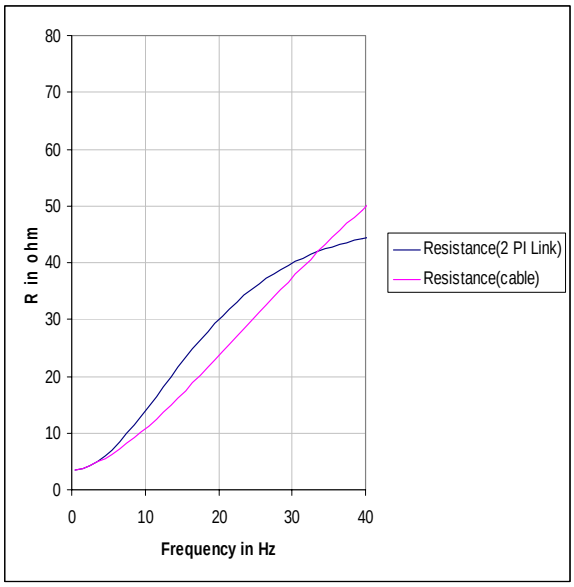

Figure 87

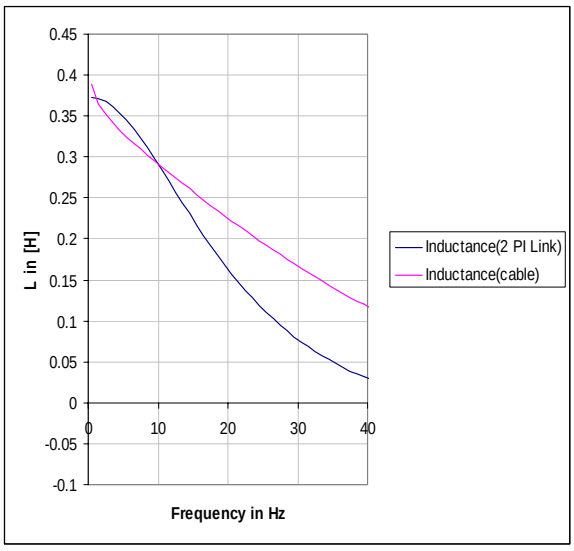

Figure 88

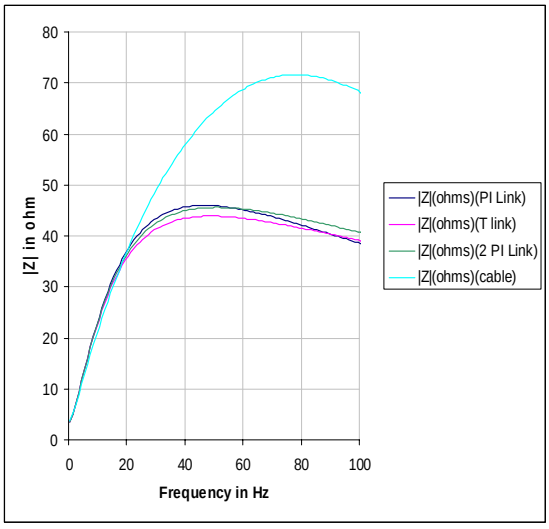

Figure 89

Conclusion:

As it can be seen from the above figures, the parallel resistance to the inductance is 13 times the dc resistance matches the real cable model at low frequencies. Therefore, it would damp the low frequency oscillations.

8.4 PSS/E raw file

```
0,      100.00,  31, , ,  50.00        / PSS/E-31.0: Benchmark file: ABB HVDC Classic model version 3.0.14, Created: 2010-06-01 14:34:53
Benchmark HVDC Classic ( rect SCR=5, Inv SCR=13.5)
Bipolar Cable transmission= 1600 MW, 500 kV, 50 Hz
    1,'BUS_1', 400.0000,3,   1,   1,   1,1.00000,   0.0000
    2,'BUS_2', 400.0000,3,   1,   1,   1,1.00000,   0.0000
   101,'CONV1',400.0000,1,   1,   1,   1,1.00000,   0.0000
   102,'CONV2',400.0000,1,   1,   1,   1,1.00000,   0.0000
0 / END OF BUS DATA, BEGIN LOAD DATA
0 / END OF LOAD DATA, BEGIN FIXED SHUNT DATA
   101,'1 ',1,     0.000,   410.0
   102,'1 ',1,     0.000,   428.4
0 / END OF FIXED SHUNT DATA, BEGIN GENERATOR DATA
    1,'1 ',     1000.000,     -9.2290,  9999.000, -9999.000,  1.01379,    0,     100.000,   0.006,   0.022,   0.00000,   0.00000,1.00000,1,  100.0,
    2,'1 ',     -980.48000,    68.947,  9999.000, -9999.000,  1.01379,    0,     100.000,   0.0022,   0.0082,   0.00000,   0.00000,1.00000,1,  100.0,
0 / END OF GENERATOR DATA, BEGIN BRANCH DATA
   101,    1,'1 ',   0.00,   0.00001,   0.00000,    0.00,    0.00,    0.00,  0.00000,  0.00000,  0.00000,  0.00000,1,1,   0.00,   1,1.0000
   102,    2,'1 ',   0.00,   0.00001,   0.00000,    0.00,    0.00,    0.00,  0.00000,  0.00000,  0.00000,  0.00000,1,1,   0.00,   1,1.0000
0 / END OF BRANCH DATA, BEGIN TRANSFORMER DATA
0 / END OF TRANSFORMER DATA, BEGIN AREA DATA
0 / END OF AREA DATA, BEGIN TWO-TERMINAL DC DATA
DC_1,  1,     21.16,  900.000,   1012.00,      0.00,     21.16,   0.10000,'I',      0.00,  20,   1.00000
   101,  4,   17.500,   12.500,     0.3706,    17.789,  400.0000,    0.51925,  1.000,   1.1750,   0.93750,   0.01250,    0,    0,    0,'1 ', 0.0000
   102,  4,   17.000,   17.000,     0.3706,    17.789,  400.0000,    0.51925,  1.025,   1.1750,   0.93750,   0.01250,    0,    0,    0,'1 ', 0.0000
0 / END OF TWO-TERMINAL DC DATA, BEGIN VSC DC LINE DATA
0 / END OF VSC DC LINE DATA, BEGIN IMPEDANCE CORRECTION DATA
0 / END OF IMPEDANCE CORRECTION DATA, BEGIN MULTI-TERMINAL DC DATA
0 / END OF MULTI-TERMINAL DC DATA, BEGIN MULTI-SECTION LINE DATA
0 / END OF MULTI-SECTION LINE DATA, BEGIN ZONE DATA
0 / END OF ZONE DATA, BEGIN INTER-AREA TRANSFER DATA
0 / END OF INTER-AREA TRANSFER DATA, BEGIN OWNER DATA
0 / END OF OWNER DATA, BEGIN FACTS DEVICE DATA
0 / END OF FACTS DEVICE DATA, BEGIN SWITCHED SHUNT DATA
0 / END OF SWITCHED SHUNT DATA
```

8.5 PSS/E DYR file

```
 1, 'GENCLS', 1, 0.0, 0.0 /
 2, 'GENCLS', 1, 0.0, 0.0 /
/                    IC IT NI NC NS NV DataList
'DC_1'  'USRDCL' 'CDCAB3' 18  1   95 50  0 233
                      3 1 1 0 0      0 102 0 0  0     0 102 0 0 0    0 0 0 0 0  0 0 0 0 0   0 0 0 0 0
                      0 0 0 0 0      0   0 0 0  0     0   0 0 0 0    0 0 0 0 0  0 0 0 0 0   0 0 0 0 0
                      0 0 0 0 0      0   0 0 0  0     0   0 0 0 0    0 0 0 0 0  0 0 0 0 0   0 0 0 0 0 0 0 0 0 0 0
                      1012. 988. 0.0 0.0 0.00    0.00 0.00 0.0 0.0 0.0     0.0 0.0 0.0 0.0 0.0   0.0 4.50
                      1012. 988. 0.0 0.0 0.00    0.00 0.00 0.0 0.0 0.0     0.0 0.0 0.0 0.0 0.0   0.0 13.0
                      18E-6 36.E-6 18E-6
                      0.605  0.605
                      0.5
                      450.E-3 450.E-3
                      0.0 0.0 0.0 0.0 0.0     0.0 0.0 0.0  /
'
```