APPLICATION OF AN EIGHT-CHANNEL COMPARATOR IN A CROSS-CORRELATOR FOR SYNTHETIC APERTURE RADIOMETRY

Erik Ryman[(1)(2)], Anders Emrich[(1)], Stefan Andersson[(1)], Johan Riesbeck[(1)], Per Larsson-Edefors[(2)]

[(1)]Omnisys Instruments AB
August Barks gata 6B, SE-421 32 Västra Frölunda, Sweden
Email: er@omniys.se

[(2)]Dept. of Computer Science and Engineering, Chalmers University of Technology
SE-412 96 Gothenburg, Sweden
Email: erirym@chalmers.se

INTRODUCTION

The ever-increasing demand for accuracy of weather forecasting and understanding of weather phenomena requires new weather observation methods. Earth observation in the microwave regions can provide important data on moisture and temperature distributions in the atmosphere, even within cloud formations where such observations are not achievable in the visible or infrared spectrum due to occlusion.

Highly detailed imagery of the earth in the microwave spectrum from GEO is however not easily attained. The high altitude and the long wavelengths combined require a very large aperture. A solution to this problem can be found in ground-based radio astronomy observatories where image synthesis using multiple antennas in array configurations has achieved a much higher spatial resolution than any single antenna can achieve by itself. The same concept can be applied on a space borne instrument and has previously been tried on the Soil Moisture and Ocean Salinity (SMOS) instrument launched to LEO in 2009 [1]. SMOS was the first polar orbiting instrument carrying a cross-correlator based synthetic aperture interferometric radiometer. There are currently two ongoing missions with the intent of deploying such an interferometer in GEO.

The Geostationary Atmospheric Sounder (GAS) is an initiative started in cooperation between Omnisys Instruments and RUAG Aerospace [2]. If realized, it will perform microwave sounding in four frequency bands, where the lowest, and most demanding, of them will be around 53 GHz. An aperture of around 8 m would be required to achieve a resolution target of 30 km when observing in the 53 GHz band. For this band it is expected to have 136 receiver elements. Foldable booms will serve as a base structure carrying the large number of receivers.

The Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) is a NASA mission for an instrument, similar in many respects to GAS [3]. The GeoSTAR instrument will observe microwave radiation in 50 GHz and higher frequency bands. It is expected to carry an even larger number of receiver elements, up to 300 for the 50 GHz band alone. These will be placed on a stationary, but also foldable, boom structure.

A cross-correlator system fitting the requirements of the ongoing missions is being developed. A signal processing ASIC designed for the purpose of performing the cross-correlation calculations has been presented in previous work [4]. This served as a concept demonstrator and will pave the way for a new version of a digital cross-correlator ASIC, which is currently being developed. The Comparator presented in this work will serve the purpose of digitizing the analog input signals in a future cross-correlator system and feeding these to the digital correlator ASIC.

It is estimated that the next generation cross-correlator system will have 256 input channels and hence, a cross-correlator with 256 inputs will serve as an example for some of the conclusions provided in this work. A power budget of 10 W is assumed for this correlator system. A rough estimate of the power consumption of the digital cross-correlator ASIC under development would be close 5 W. The requirement for the digitizing is thus below 5 W.

PREVIOUS WORK

The comparator presented in this work is specifically designed with the cross-correlator system in mind. The previously developed cross-correlator ASIC, implemented in a 65 nm CMOS process, proved that cross-correlation of 64 input channels could be handled at speeds up to 3.6 GHz. The cross-correlator ASIC had a data input system with banks of 8 data channels for each clock input. Phase matching between incoming clocks of the different input banks to within 147 degrees at an operating frequency of 1 GHz was required for the correlator to function. While this make for a very skew tolerant design the maximum skew tolerance would significantly decrease with increasing operating frequency. For the correlator ASIC, single ended communication was used and signal paths had to be externally terminated. A test board, featuring 16 analog input channels with commercial off-the-shelf comparators, was developed. The chip was mounted on an AlNi substrate. This substrate held decoupling capacitors and termination resistors. The comparators used on the test board were single channel, latching comparators with current mode logic (CML) output interface. CML is a differential signaling standard where both signal traces are terminated to the positive supply of the comparator. Since the correlator chip had single ended inputs, some kind of conversion scheme was necessary. A very simple solution was adopted; only one of the signal traces was connected to the correlator input. The correlator had a supply separate from the comparators, offset between comparator and correlator could thereby be adjusted so the input swing would be centered to the middle of the correlator supply range. While this approach is somewhat inefficient, due to only using half the input swing, it provided a simple and good enough solution for the test board.

A combination of factors led to the decision of designing a custom comparator for the next generation correlator. The comparators used for the test board had a power consumption of typically around 145 mW. In our 256-channel cross-correlator system this would translate to at power consumption of 37 W for the comparators alone. While this could possibly be manageable it is far over our intended power budget of 5 W and would introduce significant difficulties in heat disposal. System integration is another aspect that affected our decision to go for a custom made comparator. The large number of input channels means that the usage of single channel comparators would require an equally large number of components. Instead, a multi-channel comparator solution will reduce the hassle of placement and routing.

IMPLEMENTATION

While designing the comparator, experiences we got from the design and test of the previous correlator chip and test board were applied. As previously mentioned the large number of input channels meant a multi-channel comparator was desired. It was decided to go for an eight-channel comparator; matching the input bank system explored in the previous digital cross-correlator ASIC. With the same input bank system in mind a clock return path was also implemented. The clock return path makes system integration easier by avoiding the need for further clock splitting; it also simplifies the handling of clock/data synchronization.

Each channel of the comparator consist of two input amplifiers in series, a flip-flop and a CML output driving stage, Fig. 1. The comparators used for the previously developed test board had only latching functionality. Instead going for a flip-flop solution will double the time during which the input data to the digital cross-correlator ASIC is stable, increasing data/clock skew robustness of the system.

The continued use of CML signaling standard was decided upon since it gives an advantage in the way the comparator can be connected to the correlator chip. While the old correlator chip was not adapted for CML signaling, the intention is that the next chip will implement this standard in full, with differential inputs and termination resistors internally included. The comparator is designed for negative supply voltages while the correlator will operate on positive supply voltages around 1 V. The intended connection scheme is somewhat different from the one used on the test board. Since the new comparator operates on negative supply, the CML outputs can be directly connected to the cross-correlator chip by simply terminating it to the 1-V positive supply. This makes it possible for both circuits to share a common ground level while still not requiring level translation circuitry.

A very important aspect of the comparator is differential mode input offset voltages as these can severely impact sensitivity of the comparator. To make it possible to remove any such offsets an extra input pair has been added to each channel. Input offset voltages can be tuned out by simply adding the reverse offset voltages on the offset tuning inputs. The offset tuning inputs do not differ from the normal signal inputs except in wire routing, these are supposed to act on stable voltages so higher input capacitances are to be expected on these wires. Additionally, common-centroid design practices were used throughout all differential signal paths to reduce any temperature gradient caused offset drifts.

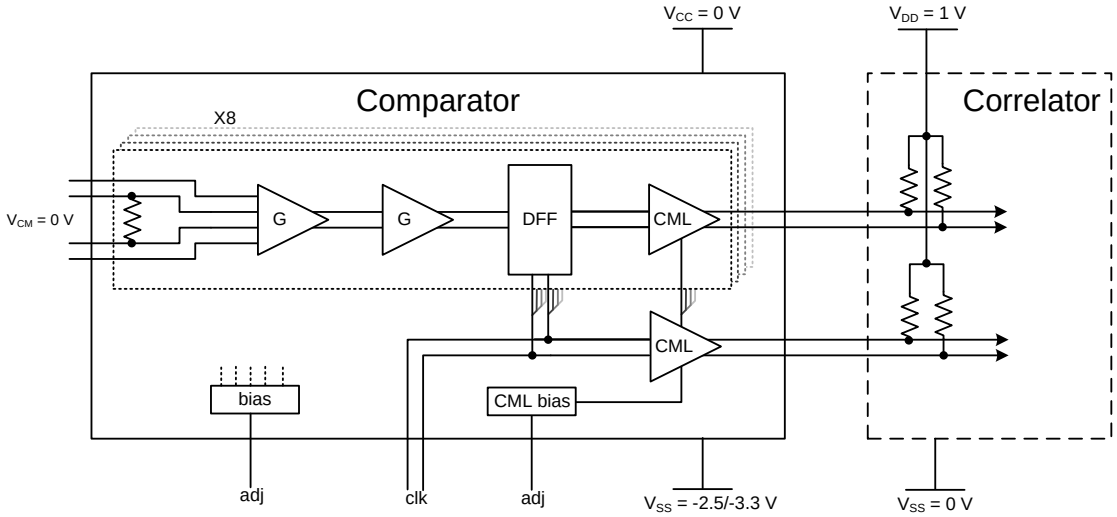

Fig. 1. Comparator schematic with intended cross correlation connection

There are a number of ways to control the performance and power consumption of the comparator. One reason for adding such flexibility is that the cross-correlator and, hence, the comparator might need to fit the requirements for different missions. Additionally these requirements are not yet fixed and are still subject to change. The comparator is designed to work with supply voltages in the range of -3.3 V to -2.5 V where performance and current consumption scales with voltage. Moreover there are two bias control pins that can tune internal current mirror levels. One controls the CML output stages, including a preamplifier; the other controls all remaining circuitry. This way comparator performance and output swing may be independently adjusted.

The comparator was implemented in a high speed 130-nm SiGe BiCMOS technology from STMicroelectronics. The decision of implementing the comparator in BiCMOS instead of regular CMOS was due to the good device matching provided by the bipolar devices in such technologies [5]. This meant an easier implementation, without the need for automatic offset cancelation techniques. The choice of the specific 130-nm technology was mainly due to the very high maximum cutoff frequency, f_T, of 230 GHz. Implementing the design using SiGe HBT rather than Si BJT is also advantageous for space application. The SiGe HBT demonstrates a higher tolerance against neutron radiation caused current gain degradation [6]. Both SiGe HBT and Si BJT show only minor degradation from ionizing radiation [7]. The complete comparator die, Fig. 2, has an area of 1.9 mm^2.

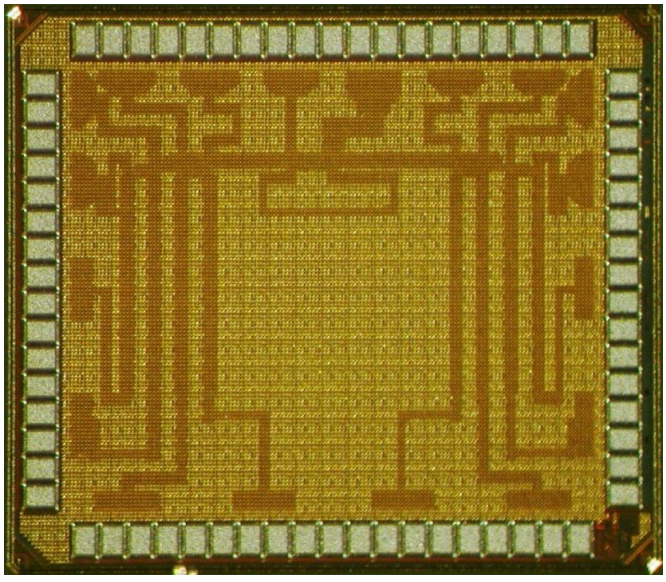

Fig. 2. Die photo of comparator

RESULTS

Simulations of the chip suggests it has the ability to sample a 1 mV_{p-p} input signal at a sampling frequency of 5GHz and at -3.3 V supply. Using the biasing capability of the comparator this could be further tuned for even higher performance or lower power consumption. At the default biasing performance level the comparator draws roughly 50 mA of current from the supply. Additionally The CML driver stages will consume 34 mA drawn from the positive supply termination of the nine differential outputs. Together this amounts to a power consumption of 300 mW for the comparator or 40 mW per channel. It is assumed the CML drivers are terminated to a 1 V supply of a digital correlator chip. In this case the output swing over a 100 Ω termination would be 375 mV. For the 256-input channel correlator the total power consumption would amount to more than 10 W for the digitizing alone. This would fall outside of the targeted power budget of 10 W for the entire correlator system where the digital correlator is to be included. A less power hungry solution can be achieved if the comparator is tuned for a lower performance target. If a 1 mV_{p-p} signal is instead to be sampled at a frequency of 1 GHz and the CML driver output swing can be lowered to 200 mV the power consumption of the comparator can be as low as 9 mW per channel by using a -2.5 supply voltage and tuning biases. In this case the total power for sampling would stay at around 2.3 W, well within our target.

The allowed common mode input voltage of the comparator, according to simulations, ranges from -1.3 V to 0.5 V. This will well encompass any expected input signal range as the intention is to keep the input signals at zero common mode voltage and input swing will be kept well below 500 mV due to the tight power budget.

Monte Carlo simulations were performed to give an idea of input offset. The simulation results suggest input offsets of up to 10 mV_{p-p} are to be expected in the case where no calibration is performed. This clearly points to the need for the offset calibration inputs as requirements of accuracy down to 1 mV might be imposed.

Awaiting more thorough measurements of the comparator a set of simple tests on a comparator in a 64-pin QFN package mounted on a simple carrier test board, Fig. 3, gives some indication of what to expect. The QFN package is not adapted for the high frequencies intended, also the cavity size means bond wires of up to 4 mm in length has to be used. Still the QFN packed comparator has proved the functionality of the chip, it should also provide at least a minimum performance number and more accurate power estimations. With a -3.3 V supply, sampling rates of at least 5 GHz can be obtained, matching the previously simulated results. The power consumption of the comparator when connected to a -3.3 V supply amounts to 70 mA, while this is somewhat higher than previously mentioned, it is still within expectations given the rough estimate of the simulation. Future measurements on a die directly wire bonded to PCB will yield more accurate results.

Using a -2.5 V supply and default biasing; a 3 GHz sampling rate can be obtained. With these settings the comparator consumes 23 mA. If the CML drivers are tuned for a 200 mV output swing over the 100 Ω terminations; the total power

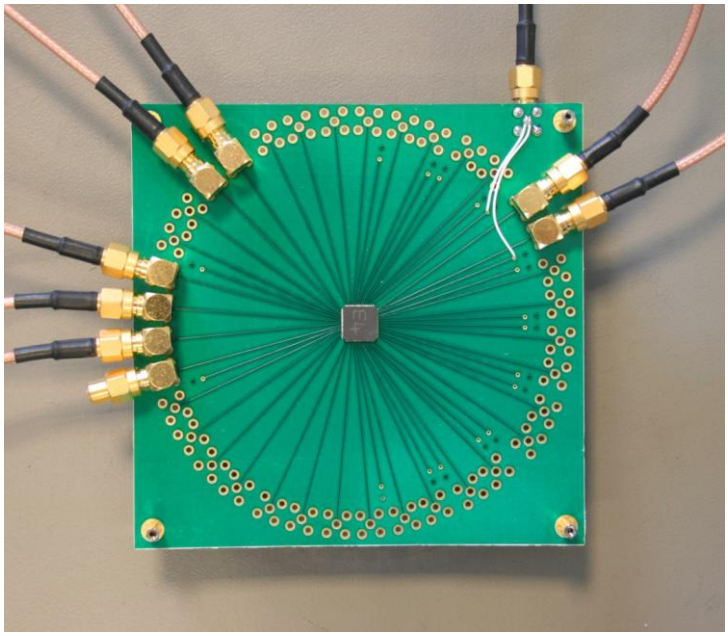

Fig. 3. QFN packaged comparator mounted on test board with one channel connected

consumption would be 120 mW or 15 mW per channel. These results suggest sampling might be handled at total power consumption below 4 W with performance to spare.

CONCLUSION

A comparator design specifically developed for a cross-correlator to be used in a synthetic aperture radiometer has been demonstrated. Features such as per channel offset trimming, bias control, clock return path and CML output drivers makes it a good solution for the intended application. Simulations and initial test results suggests it will fit nicely within performance and power requirements.

REFERENCES

[1] J. Font, A. Camps, A. Borges, M. Martín-Neira, J. Boutin, N. Reul, Y. H. Kerr, A. Hahne and S. Mecklenburg, "SMOS: The Challenging Sea Surface Salinity Measurement from Space," *Proc. IEEE,* vol. 98, no. 5, pp. 649-665, May 2010.

[2] A. Carlström, J. Christensen, J. Embretsén, A. Emrich and P. de Maagt, "A Geostationary Atmospheric Sounder for now-casting and short-range weather forecasting," in *Proc. IEEE Int. Symp. on Antennas and Propagation (APSURSI)*, 2009.

[3] B. Lambrigtsen, W. Wilson, A. Tanner and T. Gaier, "GeoSTAR - A Synthetic Aperture Approach for a Geostationary Microwave Sounder," *Proc. IEEE Aerospace Conf.*, vol. 2, pp. 1008-1014, March 2004.

[4] E. Ryman, A. Emrich, S. Andersson, J. Riesbeck, L. Svensson and P. Larsson-Edefors, "3.6-GHz 0.2-mW/ch/GHz 65-nm Cross-Correlator for Synthetic Aperture Radiometry," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2011.

[5] P. R. Kinget, "Device Mismatch and Tradeoffs in the Design of Analog Circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212-1224, June 2005.

[6] K. Petrosyants, E. Vologdin, D. Smirnov, R. Torgovnikov and M. Kozhukhov, "Si BJT and SiGe HBT Performance Modeling after Neutron Radiation Exposure," in *Proc. 9th East-West Design Test Symp. (EWDTS)*, 2011.

[7] J. A. Babcock, J. D. Cressler, L. S. Vempati, S. D. Clark, R. C. Jaeger and D. L. Harame, "Ionizing Radiation Tolerance and Low-Frequency Noise Degradation in UHV/CVD SiGe HBT's," *IEEE Electron Device Letters*, vol. 16, no. 8, pp. 351-353, August 1995.