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# A 30 GHz Integrated Subharmonic Mixer based on a Multi-Channel Graphene FET

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***Abstract*—A 30 GHz integrated subharmonic mixer based on a single graphene field effect transistor (G-FET) has been designed, fabricated and characterized. The mixer is realized in microstrip technology on a 250 $\mu m$ high resistivity silicon substrate. In order to enhance the current on-off ratio, the G-FET utilizes a channel consisting of an array of bow-tie structured graphene, yielding a current on-off ratio of 7. A conversion loss (CL) of 19 ± 1 dB over the frequency range of 24 to 31 GHz is obtained with an LO to RF isolation better than 20 dB at an LO power of 10 dBm. The overal minimum CL is 18 dB at 27 GHz. The mixer has a 3 GHz ±1-dB IF bandwidth which is achieved with a fixed LO signal of 15 GHz. The mixer linearity is characterized and the highest third order intercept point is measured to be 12.8 dBm.**

***Index Terms*—Graphene, Microwave FETs, MMIC, subharmonic resistive mixers, millimeter-wave mixers, harmonic balance analysis.**

## I. Introduction

GRAPHENE, a single layer of carbon atoms, has extremly high intrinsic carrier mobility and high carrier saturation velocity [1] which identifies it as a potential material for high frequency electronics, especially at millimeter and submillimeter wave range. The term "millimeter waves" generally refers to frequencies in the range of 30-300 GHz. Applications in this frequency range have traditionally been limited to radiometers for use in radio astronomy [2]. On the other hand, applications in high speed data communications [3] and imaging [4] are predicted to rapidly become important. For these applications, having a silicon compatible technology is a great advantage since it allows the integration of RF and digital circuits on a single chip. Graphene is compatible with silicon which makes graphene based circuits a potential candidate for above emerging applications.

There have been considerable efforts to develop high frequency devices and circuits based on graphene field effect transistors (G-FETs) [5]. Several G-FET based circuits have been demonstrated at microwave frequencies including: a small signal amplifier with 10-dB power gain at 1 GHz [6], a frequency doubler with conversion loss (CL) of 30 dB at 1.4 GHz [7], a fundamental transconductance mixer with 55 dB CL at 5 GHz [8], a fundamental resistive mixer with 27 dB CL at 4 GHz [9], subharmonic resistive mixers with 20-25 dB CL at 2-5 GHz [10], [11] and a direct signal detector with a responsivity of 33-71 V/W at 2-110 GHz [12]. As can be seen, the operating frequencies of the presented devices and circuits, except the one in [12], are limited to a few GHz which is far below the potential of graphene. Therefore increasing the operating frequency of the G-FET based circuits is essential in order to exploit the exceptional properties of graphene.

Moreover, the demonstrated G-FET based circuits generally have poor performance. This is mainly due to a low current on-off ratio in the G-FETs. For resistive mixers, a higher current on-off ratio results in a lower CL and for amplifiers it leads to a lower output conductance and consequently a higher gain can be achieved. Hence, increasing this parameter is an essential step. Moreover, in order to have less parasitics and more bandwidth at higher frequencies, a monolithic microwave integrated circuit (MMIC) is advantageous [13].

In this paper we demonstrate the first G-FET based IC in microstrip technology. The circuit is a subharmonic resistive mixer. This type of mixer utilizes the unique electron-hole duality feature of graphene and has a great potential for very compact heterodyne detectors [10]. In this design, in order to achieve a higher current on-off ratio and proper impedance levels, the G-FET channel is patterned in the form of an array of bow-tie structures. As part of the circuit design, a harmonic-balance load-pull simulation method is used to obtain the optimum mixer's embedding impedances. The mixer is characterized over the frequency range of 20 to 35 GHz. Moreover, the mixer linearity is examind by the third-order intercept point $IIP3$ and 1 dB compression point.

## II. Mixer Design and Fabrication

### A. G-FET Design and Fabrication

In resistive mixers, a FET channel is used as a time-varying resistor, $R_{ds}(t)$. In [14] it was shown that the CL of resistive mixers is essentially proportional to $1/(\Gamma_{max} - \Gamma_{min})^2$, where $\Gamma$ is the reflection coefficienet seen from the drain of the FET. Due to that, the G-FET design was focused on increasing the device current on-off ratio as well as getting proper impedance levels, i.e. $R_{ds,max} \gg Z_0$ ($\Gamma_{max} \rightarrow +1$) and $R_{ds,min} \ll Z_0$ ($\Gamma_{min} \rightarrow -1$) where $Z_0$ is the line impedance. Moreover, a symmetrical transfer characteristic is required for subharmonic mixing [10].

Due to the lack of bandgap in large area graphene, G-FETs have a low current on-off ratio. This becomes more critical as the gate length decreases. Recently it has been demonstrated that by forming a G-FET channel in a "bow-tie" structure called a nanoconstriction, high current on-off ratios (10-$10^3$) for the G-FET channel can be achieved [15]. Specifically, since the width of the contact and access area is more than that of

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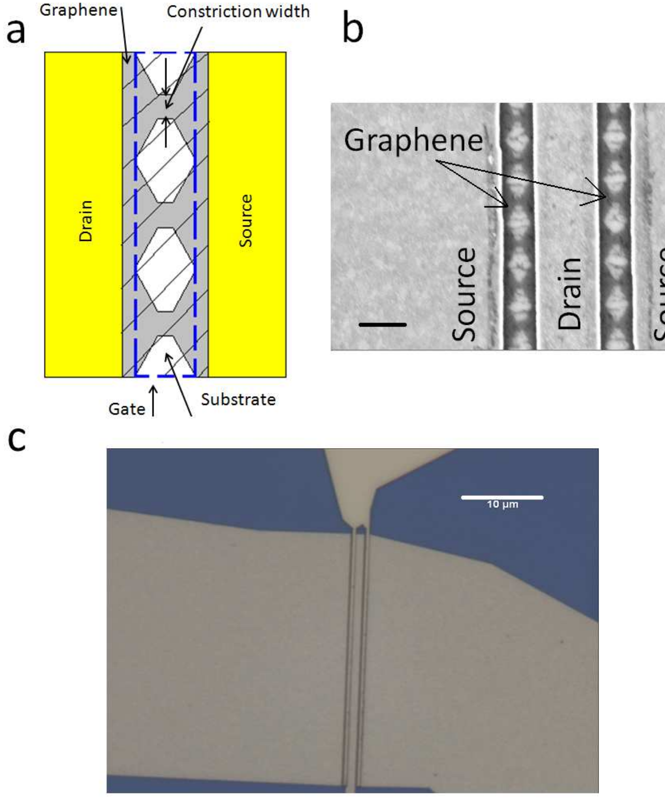


Fig. 1. a) A schematic of the G-FET with the nanoconstriction channels. The hatched lines indicate the gate dielectric and the dashed line is the gate area. NB! Figure is not to scale. b) SEM image of graphene nanoconstrictions in the G-FET channel before gate-dielectric deposition, scale bar 1 $\mu m$. c) Complete G-FET, scale bar 10 $\mu m$.

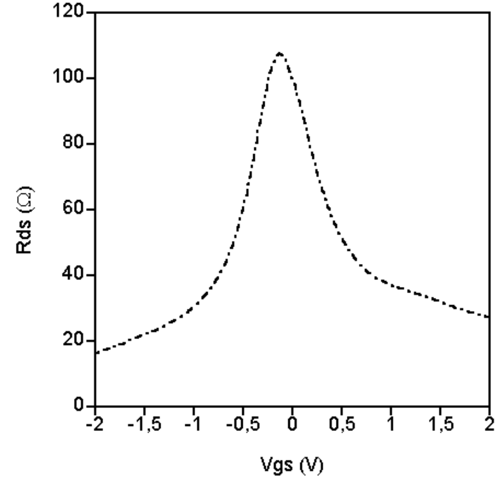


Fig. 2. $R_{ds}$ versus gate bias voltage obtained at $V_{ds}$ = 0.1 V.

the channel, a higher $R_{channel}/(R_{channel}+R_{contact}+R_{access})$ ratio is achievable. A device with a narrower constriction gives a higher on-off ratio. However, this generally leads to G-FETs with an asymmetrical transfer characteristic due to edge effects [15]. For a subharmonic G-FET mixer, a symmetrical transfer characteristic is required. Consequently, a constriction width of 100-150 nm is suitable which can result in an on-off ratio of ≈ 10 as well as a symmetrical transfer characteristic. Moreover, the impedance levels of the on-state of such structures are much higher than the circuit embedding impedance, e.g. 1-2 k$\Omega \gg 50\ \Omega$. Therefore an array of such structures shown in Fig. 1a is needed to lower the impedance level. As described in [14] the optimum embedding impedance can be estimated by $Z_{opt} \approx \sqrt{R_{ds,max}R_{ds,min}}$ and from circuit point of view it is more convenient to have $Z_{opt}$ close to 50 Ω. By assuming $R_{ds,max}/R_{ds,min} \approx 10$, we can attain a $Z_{opt} \approx 50\ \Omega$ by utilizing about 100 parallel bow-tie structures as the G-FET channels. In addition, since in this structure about half of the graphene in the channels is etched, the total gate capacitance is reduced approximately by a factor of 2. This improves the high frequency performance of the G-FET.

The G-FET was fabricated on a graphene flake (≈ 40 × 5 $\mu m^2$) produced by mechanical exfoliation on 300 nm silicon dioxide film, thermally grown on a high resistive ($\rho$ >10 k$\Omega.cm$) silicon substrate. The fabrication process is the same as in [6] except that one more ebeam lithography and oxygen plasma etching (at 10 mTorr pressure) step was added to pattern the channel structure. Fig. 1b shows the channel structure before gate-dielectric deposition and Fig. 1c shows the complete fabricated G-FET. The device has a gate-length of 0.5 $\mu m$ and a gate width of 70 $\mu m$ (2×35 $\mu m$), and the distance between source and drain contacts is 0.7 $\mu m$. Fig. 2 shows the $R_{ds}$ versus gate bias voltage. As can be seen $R_{ds,max}/R_{ds,min} \approx 7$.

FET resistive mixers are biased at $V_{ds}$ = 0 V, therefore figures of merit like $f_T$ and $f_{MAX}$ are not applicable for this application. The operating frequency of the FET mixer is limited by the switching time. This can be estimated by the $RC$ time constant of the device. Since $C_{ox} \approx 0.5$ $\mu$F $cm^{-2}$, we can roughly estimate a 3-dB cutoff frequency of $f_{c,FET} = (2\pi RC)^{-1} \simeq 120$ GHz. In the above expression $R$ corresponds the on-state resistance. Due to the electron-hole duality of the graphene channel [16], the on and off states varies with twice gate swing frequency and consequently the mixer operates subharmonically.

In resistive mixers, the FET is used as a variable resistance controlled by the gate voltage. In order to have a linear mixer, the output characteristic of the FET should be linear for all gate voltages. As can be seen in Fig. 3, the $I_{ds} - V_{ds}$ characteristic is approximately linear at low $V_{ds}$ for the entire gate voltage.

### *B. Circuit Design and Fabrication*

To operate at millimeter waves frequency range, the mixer is designed at 30 GHz. For estimating the optimum embedding impedances, harmonic-balance load-pull simulations were carried out in a standard circuit simulator (Agilent Advanced Design System) by utilizing the large-signal model proposed in [17]. Fig. 4 shows contour plots of simulated CL for $f_{RF}$ = 30.1 GHz , $f_{LO}$ = 15 GHz and $f_{IF}$ = 100 MHz at $P_{LO}$ = 10 dBm. In this figure the inner contours are for CL ≈ 17 and the outer contours are for CL ≈ 19 dB (0.5-dB step). As can be seen the optimum RF and LO embedding impedances are close to $\sqrt{R_{ds,max}R_{ds,min}} \approx 40\ \Omega$. Moreover, by relaxing the condition on the CL, $CL \leq CL_{min}$+0.5 dB, the mixer can be realized by a simpler circuit.

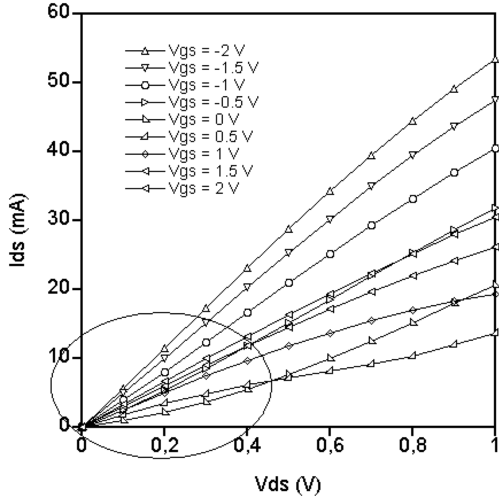


Fig. 3. Measured DC output characteristics of the G-FET at different gate bias voltages where the linear transport region is identified.

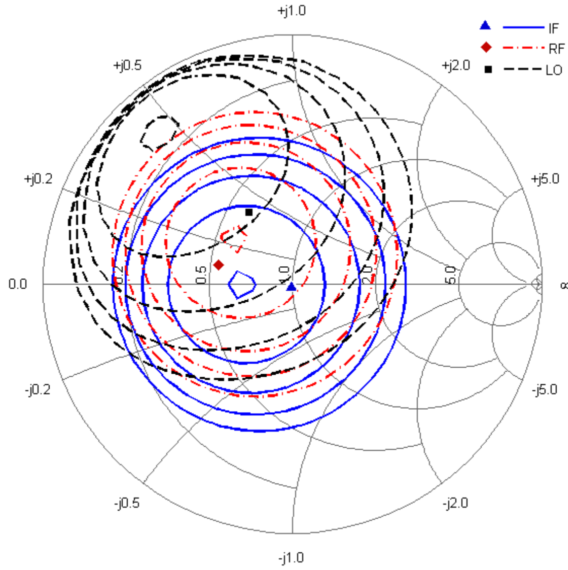


Fig. 4. Simulated CL contour plots for LO, RF and IF embedding impedances. The inner contour is for CL ≈ 17 dB and the outer contour is for CL ≈ 19 dB (0.5-dB step), $P_{LO}$ = 10 dBm and, all other mixing terms are terminated with 50 Ω. The RF, LO and IF chosen embedding impedances for the designed circuit are also depicted.

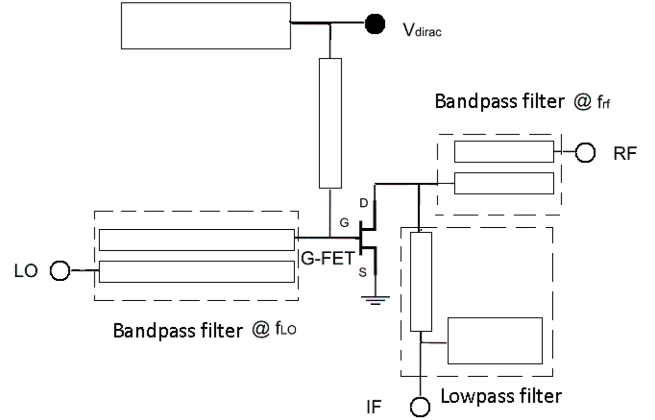


Fig. 5. The schematic of the designed subharmonic resistive G-FET mixer.

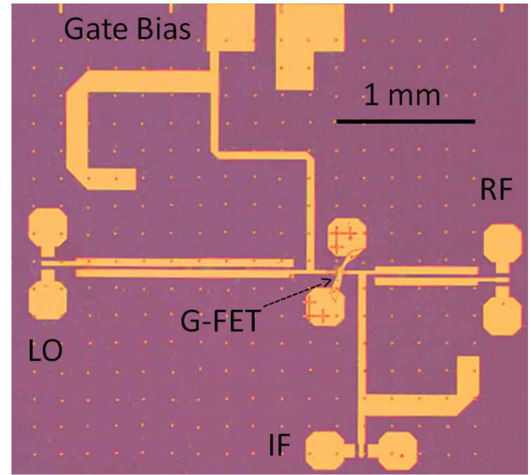


Fig. 6. Photomicrograph of the fabricated subharmonic mixer on high resistivity silicon substrate. The chip measures 3.4 ×3.2 $mm^2$.

The schematic of the designed subharmonic resistive mixer is shown in Fig. 5 and the corresponding embedding impedances are depicted in Fig. 4. The LO and RF signals are applied through coupled line filters to the gate and drain of the G-FET respectively. Since $f_{RF} \approx 2f_{LO}$ , the RF (LO) signal is in the stop-band of the LO (RF) filter and therefore a considerable RF-LO rejection is expected. The IF filter consists of an open stub instead of lumped elements to block the RF signal. The stub version of the filter has lower loss due to less parasitic elements and also it leads to much simpler fabrication steps. Because $f_{LO} \approx f_{RF}/2$, the IF filter does not significantly attenuate the LO signal. However, as described in [18] this type of IF filter gives a wideband IF signal. Finally, a DC voltage is needed to bias the gate at the voltage of minimum conductivity, $V_{dirac}$.

The mixer circuit was realized in microstrip technology. Although it needs backside processing such as wafer thinning and via holes etching, this types of processing are well-known for silicon substrates. The microstrip technology typically has lower loss than coplanar waveguide technology. Moreover it does not need air bridges and is based on verified models within standard circuit simulator softwares. The silicon substrate was thinned from the backside to 250 $\mu$m by deep reactive ion etching. The circuit was added to the fabricated G-FET by a photolithography process and e-gun evaporation of Ti(20 nm)/Au (1 $\mu$m). The through-substrate via holes with tapered sidewall for achieve proper ground were etched by a modified Bosch process [19]. Finally, via holes were metallized by magnetron sputter deposition with Ti(20 nm)/Au(600 nm). The mixer layout on the chip is shown in Fig. 6. The chip measures 3.4 ×3.2 $mm^2$.

## III. Results

The subharmonic mixer was biased at $V_{gs}$ = $V_{dirac}$ = -0.2 V and was characterized between 20 and 35 GHz frequency with Agilent signal generators (E8257C, 83650B) and spectrum

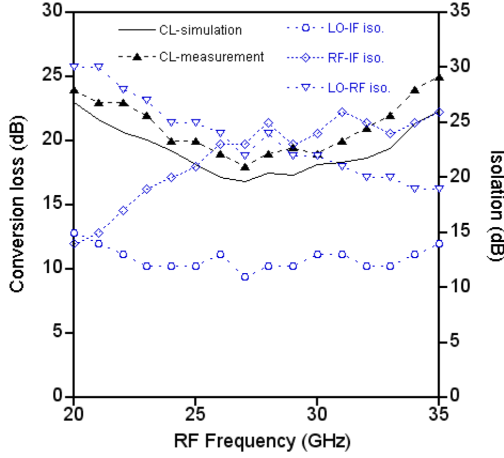


Fig. 7. Conversion loss and port isolations versus frequency at 10 dBm LO-power with $f_{IF}$ = 100 MHz, $f_{LO}$ = ($f_{RF}$ − $f_{IF}$)/2.

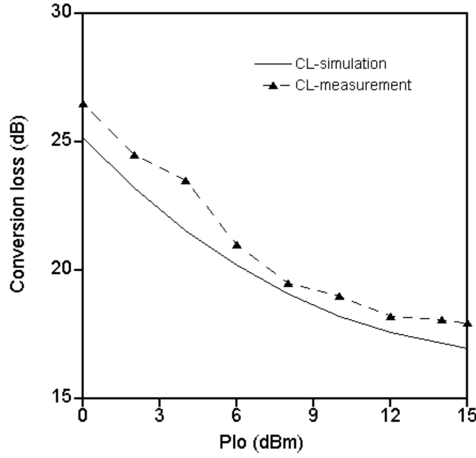


Fig. 8. Conversion loss versus LO power at 30 GHz with $f_{IF}$ = 100 MHz.

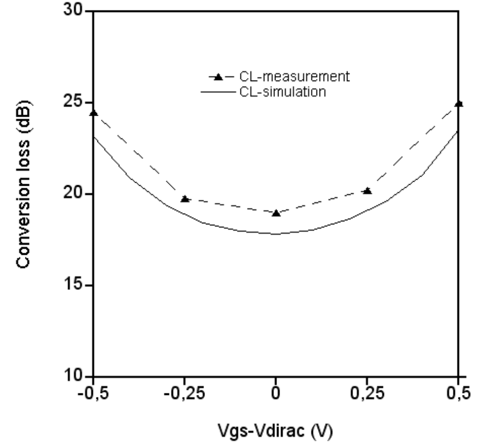


Fig. 9. Conversion loss versus gate bias voltage at 30 GHz RF frequency.

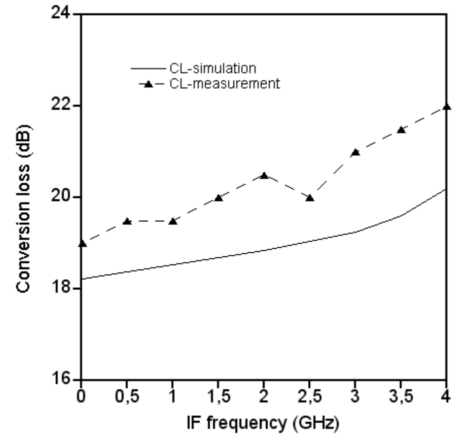


Fig. 10. Conversion loss versus IF frequency with fixed $f_{LO}$ = 15 GHz and 10 dBm LO power.

analyzer (8565EC). The default values for IF frequency and LO power were 100 MHz and 10 dBm respectively. The mixer CL was measured to be 19 ± 1 dB over the frequency range of 24 to 31 GHz and the overall minimum CL is 18 dB at 27 GHz (Fig. 7). The LO-RF and RF-IF isolations are better than 20 dB and the LO-IF isolation is about 12 dB for the same frequency range. The mixer CL at 30 GHz RF frequency versus LO power levels was measured and is shown in Fig. 8. As can be seen the CL at high LO power approaches 18 dB. This value of CL is only 3.8 dB higher than the minimum CL (14.2 dB) that can be achieved from subharmonic resistive G-FET mixers as predicted in [20]. The minimum theoretical value is higher than that of conventional mixers and it is due to the smooth transition between the on and off states and unequal duty-cycle for these states (Fig. 2). Moreover, by deviating from $V_{dirac}$ the CL increases rapidly as shown in Fig. 9.

Fig. 10 is the measured CL versus IF frequency with $f_{LO}$ = 15 GHz. The mixer exibits a 3 GHz ±1-dB IF bandwidth.

The mixer linearity is characterized by $CP_{1dB}$ as well as $IIP3$. The former was measured by increasing $P_{RF}$ up to -2 dBm at 30 GHz. The 1 dB compression point was measured to be -3 dBm. The latter was measured with two tones separated by 20 MHz. RF signals were applied on the RF port with an external standard power combiner and the first and third order IF tones were measured and the $IIP3$ figure was extrapolated. Table I shows the extracted $IIP3$ from the measured and simulated data for different LO power levels.

TABLE I
$IIP3$ VERSUS $P_{LO}$

| $P_{LO}$ | 5 dBm | 10 dBm | 15 dBm |
|---|---|---|---|
| $IIP3$ from measurement | 4.8 dBm | 8 dBm | 12.8 dBm |
| $IIP3$ from simulation | 5.5 dBm | 8.5 dBm | 13.5 dBm |

The comparison between the demonstrated mixer and mixers based on mature technologies at RF frequency of about 30 GHz is presented in table II. As can be seen further development is needed in order to approach the performance of mixers based on well established technologies. In this design, for the sake of fabrication simplicity, distributed coupled line filters are used which makes the mixer size relatively large. However, at higher frequencies ($f_{RF}$ > 100 GHz) using this type of filters is more beneficial. In addition, since G-FET subharmonic resistive mixers do not need a balun at the LO port, contrary to conventional mixers [25], more compact

TABLE II
COMPARISON OF THE G-FET SUBHARMONIC MIXER WITH OTHER RESISTIVE FET MIXERS AT 30 GHZ

| | [21] | [22] | [23] | [24] | This work |
|---|---|---|---|---|---|
| RF(GHz) | 27.5-28.5 | 26.5-30 | 9-31 | 18-26 | 24-31 |
| Technology | PHEMT | CMOS | CMOS | CMOS | G-FET |
| Type * | S | F | S | S | S |
| CL(dB) | 11 | 10.3 | 8-11 | 11-12 | 18-20 |
| LO(dBm) | 13 | 0 | 9.7 | 4-8 | 10-15 |
| LO-RF(dB) | 35 | 24 | 17 | 30 | 20-26 |
| LO-IF(dB) | 30 | 22 | 22.5 | 33.5 | 12 |
| $IIP3$(dBm) | — | 12.7 | 3 | 14-20 | 8-12.8 |
| IF-BW(GHz) | — | 1.5 | 1.8 | — | 3 |
| Size($mm^2$) | 1×2 | 0.5×0.3 | 0.9×1 | 0.7×0.6 | 3.4 ×3.2 |
| Gate length | 150 nm | 90 nm | 90 nm | 130 nm | 500 nm |

* F = Fundamental, S = Subharmonic

mixers can be achieved.

## IV. CONCLUSION

A 30 GHz integrated subharmonic resistive mixer based on a G-FET is realized in microstrip technology on a 250 $\mu m$ high resistivity silicon substrate. In order to simultaneously have proper impedance levels and a suitable on-off ratio, the G-FET utilizes a channel consisting of an array of bow-tie structured graphene. A harmonic-balance load-pull simulation approach is used to find the proper embedding impedances. The mixer shows a CL of 19 ± 1 dB over the frequency range of 24 to 31 GHz with an LO to RF isolation better than 20 at an LO power of 10 dBm. The result is the state-of-the-art among the G-FET based mixers in terms of performance and operating frequency. In addition, the mixer has a wide IF bandwidth of DC-3 GHz and it is fairly linear which is shown by a measured $IIP3$ figure as high as 12.8 dBm.

In order to compete with mature technologies, further device developement is required. One possible way could be to engineer the shape of nanoconstrictions in a way that the G-FET transfer characteristic has a sharp transition between the on and off states. Moreover, due to the unintentional doping which is generated during the fabrication process, $V_{dirac}$ deviates from zero voltage and therefor a DC bias is needed. If the process is developed in a way that $|V_{dirac}|$ < 0.1 V, the mixer operates unbiased, hence, requires no bias circuitry. This feature together with no need for a blun at the LO port makes G-FET subharmonic mixers a potential candidate for compact heterodyne array detectors.

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