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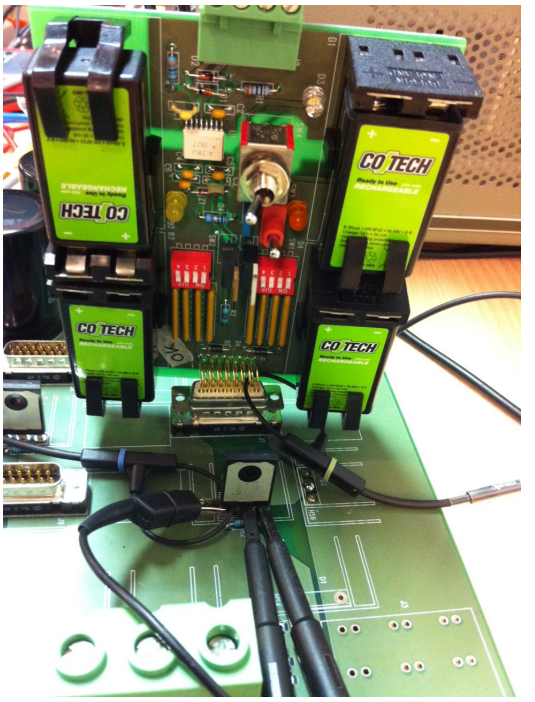

Analytical modeling and experimental evaluation of MOSFET switching characteristics

Master of Science Thesis

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Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2012

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Cover:
Text concerning the cover illustration. In this case: MOSFET test circuit.

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Abstract

In this thesis, analytical modeling of a MOSFET as well as investigation of its gate drive was studied. Firstly the performance of the gate drive during switching transients under different test conditions were studied. In order to do so, the elements in the drive were checked separately and their effect on the gate voltage and current were observed. Then two simple case set-ups consisting RC circuit were switched by the gate drive. For the first case a large capacitor and resistor was selected ($C = 68nF, R = 209\Omega$). The results match well with the simulations. The rise time of the voltage was $39\mu s$. For the second case very small values were selected to check the gate drive performance in higher currents($C = 13nF, R = 22\Omega$). The results in this case also were in agreement with the results from the simulation test set-up, the voltage rise time was 898ns in this case.

The next step was modeling a MOSFET analytically, using its turn-on and turn-off equations in MATLAB. Two cases were considered for this part. First large capacitors were attached between the gate-source and gate-drain of the device in order to overrule its inherent capacitors and slow down the switching transient($C_{gs} = 68nF, C_{gd} = 5nF$). The results from the simulation were in agreement with the experimental results. Afterwards the capacitors were detached and only the inherent capacitors of the MOSFET were charged and discharged during switching transients. For both cases gate voltage/current and drain-source voltage/current from the simulation were compared with the experimental results. Finally switching losses were calculated and compared for both experimental and simulation, which at switching frequency of 2kHz losses for simulation and measurement were 21mW and 28mW during turn-on and 28mW and 30mW during turn-off respectively.

Index Terms: Gate drive, MOSFET modeling, MOSFET switching, loss calculation

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Hamed Raee
Göteborg, Sweden
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Contents

List of Symbols and Abbreviations

BJT	Bipolar Junction Transistor
BV_{CBO}	Base-collector breakdown voltage
BV_{CEO}	BJT maximum collector-emitter sustained voltage while the base current is zero
BV_{SUS}	BJT maximum collector-emitter sustained voltage while i_c is big
C_{CE}	BJT collector-emitter capacitance
C_{gd}	MOSFET parasitic gate to drain capacitance
C_{gs}	MOSFET parasitic gate to source capacitance
C_{iss}	MOSFET parasitic input capacitance
C_{oss}	MOSFET parasitic output capacitance
C_{rss}	MOSFET parasitic gate to drain capacitance datasheet specification value
EMI	Electromagnetic Interface
E_{off}	Turn-off losses datasheet specified value
E_{on}	Turn-on losses datasheet specified value
E_{rr}	Reverse recovery energy losses
f_{sw}	Switching frequency
g_m	MOSFET transconductance
i_B	BJT base current
i_c	BJT collector current
$I_{d,RMS}$	MOSFET RMS current
i_{ds}	Drain source current
$I_f(V)$	Diode forward current as a function of voltage
I_G	Gate drive current
i_{gs}	Gate source current
IGBT	Insulated Gate Bipolar Transistor
I_{ref}	MOSFET current, test condition
ki	Current exponent datasheet specified value
kv	Voltage exponent datasheet specified value
LED	Light emitting diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Ω	Ohm
P_c	Conduction losses
$P_{con,D}$	Diode conduction losses
$P_{loss,D}$	Diode losses
Q_{rr}	Power diode reverse recovery charge
R_D	Diode resistor
$R_{ds,on}$	Drain source on-state resistor
R_g	Gate drive resistor
SMPS	Switch Mode Power Supply
τ	Time constant
TC	Temperature exponent datasheet specified value
t_{fv}	MOSFET voltage fall time during turn-on transient
$T_{j,ref}$	MOSFET temperature, test condition
t_{ri}	Rise time
t_{rr}	Power diode reverse recovery time

t_{rv}	MOSFET drain source voltage during turn-off transient
T_{sw}	Switching time
UVLO	Under Voltage Lock-Out
V_{ce}	BJT collector emitter voltage
V_{ds}	Drain source voltage
V_{gg}	Gate drive voltage
V_{gs}	Gate source voltage
$V_{gs,I0}$	Gate source voltage when MOSFET current reaches load current
$V_{gs,th}$	Gate source threshold voltage
$V_{ds,on}$	Drain source on-state voltage
V_{out}	Optocoupler output voltage
$V_{plateau}$	MOSFET plateau voltage
V_{in}	Input voltage
V_{ref}	MOSFET drain-source voltage, test condition

Chapter 1

Introduction

1.1 Problem background

Car industry is moving toward hybrid cars these days. Different configurations are suggested for the power train of a hybrid car. The most common types are series/parallel power trains, in which an engine and/or an electric machine are used to transfer power to the shafts and drive the car. The electric motor is supplied through batteries and inverters. Power electronic components are used widely for rectifying or inversion of the power according to their applications. Selection of appropriate devices which lead to high efficiency of the whole system is an important part of the system design.

Efficiency in a hybrid car is affected by the losses in the different parts of the power train. One of the devices is inverter. The selection of an appropriate switching speed is in this case very important. A fast switching speed leads to an overvoltage of transistor during the turn-off due to high $\frac{di}{dt}$, (The ratio between peak voltage value versus the mean dc-link voltage becomes high and accordingly so does the cost) and EMI is generated that jeopardizes the vehicle devices. On the other hand choosing slow switching speed slows down switching transients and therefore causes high losses. In order to calculate the losses correctly and find a way to reduce them, knowing the characteristics of the switching devices is necessary. Studying the behavior of the MOSFET during different conditions and the elements affecting their switching transients are the keys to have an efficient inverter. Moreover designing a suitable gate drive plays an crucial role in the performance of the MOSFET. Devices in the gate drive must be designed and selected based on the application of the inverter in order to achieve desired results.

1.2 Purpose

The purpose of this thesis is to model a MOSFET analytically, as well as design considerations of its gate drive. Different experiments under various test conditions are performed on the gate drive and the MOSFET. Comparison between the simulation and experimental results are performed. Finally switching losses are calculated.

Chapter 2

Technical background

2.1 Power MOSFET

2.1.1 Description

MOSFETs with considerable on-state current carrying (high current applications) and off-state blocking capabilities are widely used in power electronic circuits when the voltage levels are below 100-200V.

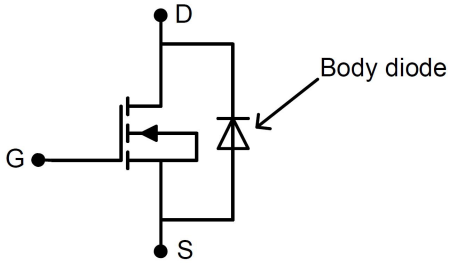


Figure 2.1: n-channel MOSFET

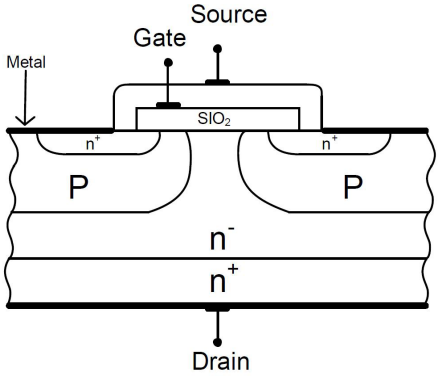


Figure 2.2: Cross section of a n-channel MOSFET

A MOSFET has a four-layer structure of alternative p-type and n-type doping depicted in Fig. 2.1. If the structure is $n^+pn^-n^+$ the MOSFET is designated as n-channel and if the structure is opposite it is known as a p-channel MOSFET. The n- layer is the drain drift region and is doped at $10^{14} - 10^{15}cm^{-3}$ [1]. The body diode between drain and source is created in the structure of the MOSFET during the manufacturing process and it has undesirable reverse recovery characteristics. If it is needed to cancel it then extra costs and losses are acceptable. Therefore a diode can be placed in reverse direction and a diode with acceptable reverse recovery performance will be connected (Fig. 2.3) [1].

2.1.2 Static characteristics

The gate in a MOSFET controls the flow of the current between the drain and the source. The drain current (i_{ds}) as a function of the drain-source voltage (V_{ds}) according to different gate-source voltage (V_{gs}) is shown in Fig. 2.4 [1]

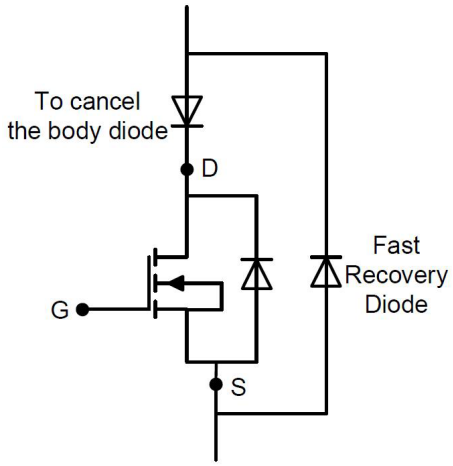


Figure 2.3: MOSFET with fast recovery diode in parallel

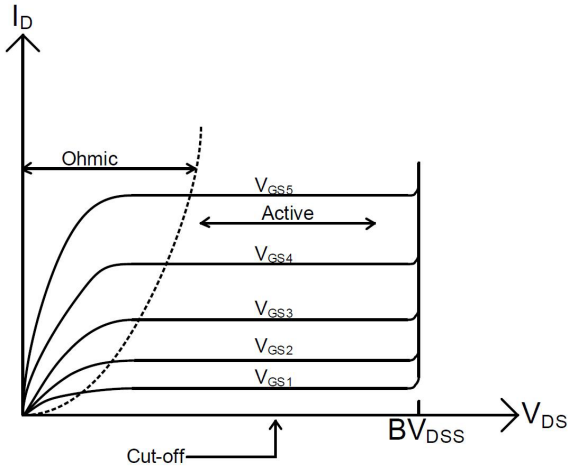


Figure 2.4: MOSFET i-v characteristics

These characteristics are the same for a p-channel MOSFET except that the current and voltage have opposite polarities. From Fig. 2.4 we can see three different regions of operations. When $V_{gs} > V_{gs,th}$ the device operates in the ohmic region,(also known as the linear region). When $V_{ds} > (V_{gs} - V_{gs,th})$, the device enters the saturation mode (active region). And finally when $V_{gs} < V_{gs,th}$ the MOSFET turns off (cut-off region) and the drain current becomes almost zero. The MOSFET will be in the ohmic and the cut-off region when it is used as switching device [2].

2.1.3 Dynamic characteristics

MOSFETs are fast switching devices in comparison to BJTs and IGBTs because they do not have any excess minority carriers that must be moved out or into the device when it is turned off or on. There are changes in the module which are represented by stray capacitances. The equivalent circuits in different device operational regions are depicted in Fig. 2.5(a). These models are used for detailed study of the MOSFET switching characteristics in order to achieve an appropriate gate drive circuit. The drain-source capacitance is considered when the snubber circuit is designed for the device. Even though the gate-source capacitance is very important, the gate-drain capacitance is actually more crucial and more complicated to deal with. Both capacitances are non-linear voltage variant but the latter is very sensitive to changes in the voltage. Since C_{gd} is a voltage dependant capacitor, its value mentioned in the data sheet is valid only for the test conditioned given in the data-sheet. Therefore in order to calculate the correct value for a certain application the following approximation is considered [3]. For the output capacitance there is also an approximation to calculate the correct value according to the applied voltage to the drain-source.

$$C_{gd,ave} = 2C_{rss}\sqrt{\frac{V_{ds,datasheet}}{V_{ds,off}}} \qquad C_{oss,ave} = 2C_{oss}\sqrt{\frac{V_{ds,datasheet}}{V_{ds,off}}}$$

As it can be seen in Fig. 2.5(b) when MOSFET is in cutoff or in active region, the gate-voltage-controlled current source shown in this figure becomes zero whenever $V_{gs} < V_{gs,th}$ and equals to $i_{ds} = g_m(V_{gs} - V_{gs,th}$)whenever the device is in active region. In Fig. 2.5(c), the device in on-state and in the ohmic region is shown ($V_{ds} > V_{gs} - V_{gs,th}$).

$r_{ds(on)}$ is the forward on-state resistance and can be used to determine the ohmic losses in the device. [1]

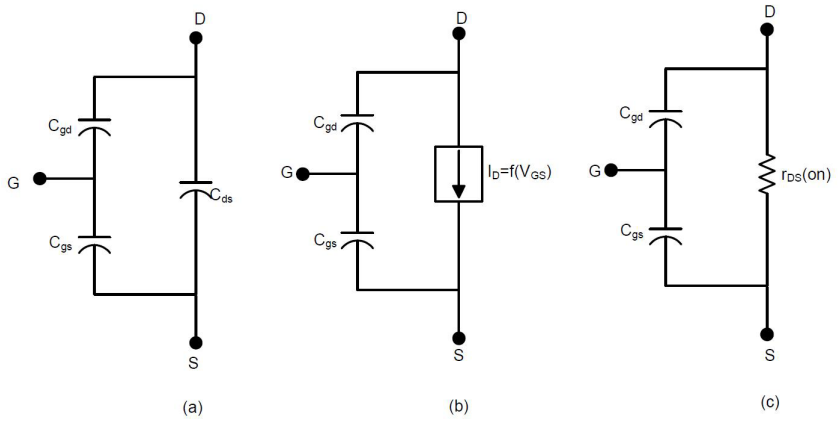


Fig. 2.5 MOSFET equivalent circuit

In Fig. 2.6 and Fig. 2.7 a typical drain current, drain-source voltage, gate current and gate-source voltage during turn-on and turn-off transients are shown.

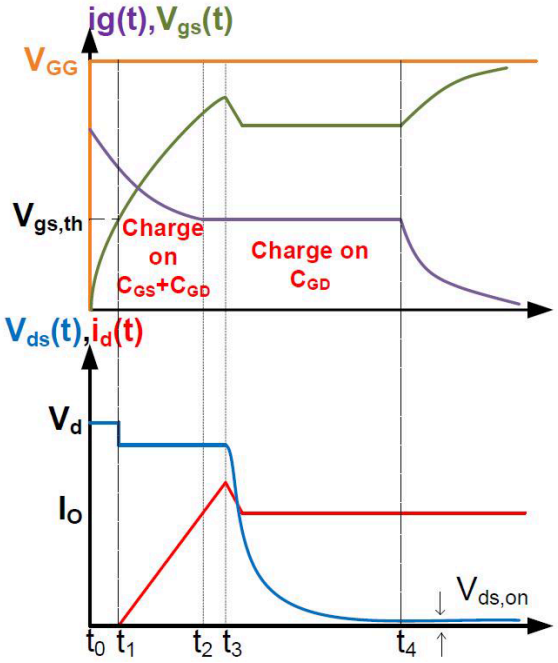


Figure 2.6: MOSFET turn on characteristics

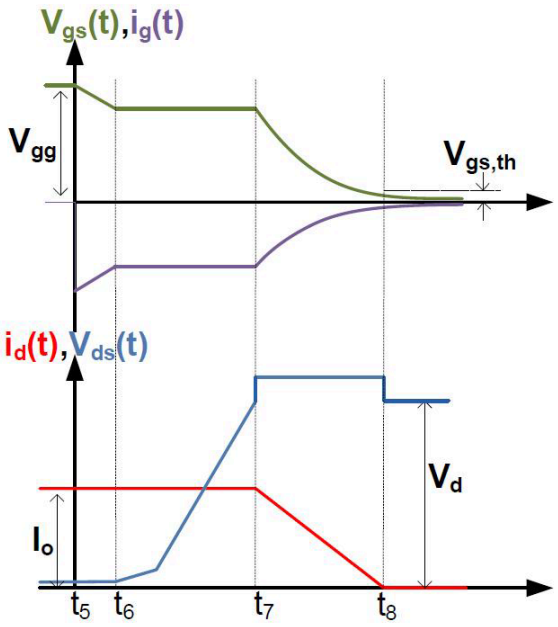


Figure 2.7: MOSFET turn off characteristics

Analytical approach to MOSFET switching

Switching behavior of a MOSFET depends on many factors including dc voltage, switching frequency, internal capacitances, etc. In this part switching transients of a MOSFET are discussed by its turn-on and turn-off equations.

- Turn-on process:

At the beginning the device is off and the load current is passing through the free-wheeling diode. The initial conditions are: V_{gg}=0V,V_{ds}= V_{in} and i_o= i_{diode}. At t=t_0, V_{gg} is applied and internal (and externally added) capacitors across the gate-source and

gate-drain start to be charged through the gate resistor R_g. The gate-source voltage (V_{gs}) increases exponentially with the time constant τ= R_g(C_{gs}+C_{gd}). The drain current remains zero until V_{gs} reaches the threshold voltage. Equations regarding time interval t_0-t_2 are depicted below

$$\begin{aligned} i_g &= \frac{V_{gg} - V_{gs}}{R_g} \\ &= i_{Cgs} + i_{Cgd} \\ &= C_{gs}\frac{dV_{gs}}{dt} - C_{gd}\frac{d(V_{gg} - V_{gs})}{dt} \end{aligned}$$

$$\rightarrow \frac{V_{gg} - V_{gs}}{R_g} = C_{gs}\frac{dV_{gs}}{dt} - C_{gd}\frac{d(V_{gg} - V_{gs})}{dt} \tag{2.1}$$

$$\rightarrow V_{gs}(t) = V_{gg}(1 - e^{-(t-t_0)/\tau}) \tag{2.2}$$

The delay time is the time takes for the gate-source voltage to reach the threshold voltage

$$t_d = -\tau ln(1 - \frac{V_{gs,th}}{V_{gg}}) \tag{2.3}$$

Afterwards the current increases linearly until it reaches the load current. But due to the reverse recovery of the free-wheeling diode there is an over-current in the device. Meanwhile there is a voltage drop over the device due to parasitic inductances in the circuit ($L_{par}\frac{di_{ds}}{dt}$).

From the data sheet of the MOSFET, V_{gs} at the load current is read to calculate the turn on time.

$$t_{on} = -\tau ln(1 - \frac{V_{gs,I0}}{V_{gg}}) - t_d \tag{2.4}$$

In order to apply the effects of the parasitic in the simulation the current rise time is defined as [4],

$$t_{on} = -\tau ln(\frac{(V_{gg} - V_{gs,th}) + \frac{(V_{gg} - V_{gs,th})g_m L_{par}}{\tau}}{V_{gg} - V_{gs,I0}}) - t_d \tag{2.5}$$

Drain current is calculated from gate-source voltage:

$$i_d(t) = g_m(V_{gg} - V_{gs,th}) - g_m V_{gg} e^{-(t-t_1)/\tau} \tag{2.6}$$

Whenever the current reaches to the load current again, V_{gs} and i_g remain constant (Plateau level), since the gate-source voltage is constant, all the gate current passes through the gate-drain capacitor, so the gate current will be

$$\begin{aligned} i_g &= i_{C,gd} \\ &= C_{gd}\frac{d(V_{gg} - V_{in})}{dt} \\ &= -C_{gd}\frac{dV_{ds}}{dt} \end{aligned}$$

$$\rightarrow i_g = -C_{gd}\frac{dV_{ds}}{dt} \tag{2.7}$$

Therefore the drain-source voltage is

$$V_{ds}(t) = -\frac{V_{gg} - V_{gs,th}}{R_g C_{gd}}(t - t_2) + V_{in} \tag{2.8}$$

When the drain-source voltage reaches to the on-state voltage drop, V_{gs} increases with the same time constant as in t_1-t_2 until it reaches to V_{gg}, and i_g becomes almost zero.

- Turn-off process:

The initial conditions for turn-off are

- $V_{ds,onstate} = R_{ds}I_o$
- $i_g = 0$
- $V_{gs} = V_{gg}$
- $i_d = I_o$

At the time t=t_5 the gate voltage becomes zero, causing the gate-source and gate-drain capacitors to discharge through R_g followed by below equations

$$\begin{aligned} i_g &= -\frac{V_{gg}}{R_g} \\ &= i_{Cgs} + i_{Cgd} \\ &= (C_{gs} + C_{gd})\frac{dV_{gs}}{dt} \end{aligned} \tag{2.9}$$

Hence V_{gs} will be

$$V_{gs}(t) = V_{gg}e^{-(t-t_0)/\tau} \tag{2.10}$$

V_{gs} continues to decrease until it reaches a constant level, while the drain current is constant at load current. The gate-source voltage at $i_{ds} = I_o$ is

$$V_{gs} = \frac{I_o}{g_m} + V_{gs,th} \tag{2.11}$$

From (2.10) and (2.11) the time takes for V_{gs} to reach a constant value can be obtained by

$$V_{gs} = \tau\frac{V_{gg}}{\frac{I_o}{g_m} + V_{gs,th}} \tag{2.12}$$

Since the gate-source voltage is constant in the time interval t_6-t_7, all the current is taken from the gate-drain capacitor

$$\begin{aligned} i_g &= C_{gd}\frac{dv_{gd}}{dt} \\ &= C_{gd}\frac{d(v_{gs} - v_{ds})}{dt} \\ &= -C_{gd}\frac{dv_{ds}}{dt} \end{aligned} \tag{2.13}$$

The gate current can be found as

$$i_g = \frac{V_{gs}(t_1)}{R_f} = \frac{1}{R_g}(\frac{I_o}{g_m} + V_{gs,th}) \tag{2.14}$$

Finally the drain-source voltage will be achieved by combining (2.13) and (2.15).

$$V_{ds} = V_{ds,on} + \frac{1}{R_g C_{gd}}(\frac{I_o}{g_m} + V_{gs,th})(t - t_1) \tag{2.15}$$

At the time t_7 the drain-source voltage reaches the dc-link voltage, forcing the free-wheeling diode to be turned on. Hence the current in the switch starts falling and is equal to

$$i_{ds}(t) = g_m(V_{gs} - V_{gs,th}) \tag{2.16}$$

where V_{gs} is obtained from following equation

$$V_{gs}(t) = (\frac{I_o}{g_m} + V_{gs,th})e^{-(t-t_2)/\tau} \tag{2.17}$$

The current fall time is calculated by having the time constant and the threshold voltage over V_{gs} at load current.

$$t_{fi} = -R_g C_{iss} ln \frac{V_{gs,th}}{V_{gs,Io}} \tag{2.18}$$

The rate of changes of the current in the device is achieved by dividing the MOSFET current over the current fall time.

$$\frac{di}{dt} = \frac{i_{ds}}{t_{fi}} \tag{2.19}$$

The gate current is increasing from a negative value and becomes zero according to following equation.

$$i_g = \frac{V_{gs}(t_1)}{R_g} = \frac{-1}{R_g}(\frac{I_o}{g_m} + V_{gs,th})e^{-(t-t_2)/\tau} \tag{2.20}$$

The time interval t_7-t_8 is finished when the gate-source voltage reaches the threshold voltage and the time t_8 can be calculated by putting $V_{gs}(t_8) = V_{gs,th}$. The gate-source voltage becomes zero and MOSFET is considered off after this point.

2.1.4 Losses in MOSFET

Conduction losses

The conduction loss in the MOSFET is calculated from an approximation using the drain-source resistance.

$$V_{ds(on)} = R_{ds(on)} i_{ds} \tag{2.21}$$

$R_{ds(on)}$ can be found in the datasheet. The instantaneous conduction loss is determined as

$$p_{cm}(t) = V_{ds(on)}(t) i_{d(on)}(t) \tag{2.22}$$

So the average conduction loss is

$$P_c = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{cm}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{ds(on)} i_d^2 .dt = R_{ds(on)} . I_{d,RMS}^2 \tag{2.23}$$

Switching losses

Switching losses are calculated using datasheet parameters [5].

$$E_{on} = E_{on,ref}(\frac{I_{out}}{I_{ref}})^{ki}(\frac{V_{in}}{V_{ref}})^{kv}(1 + TC_{sw}(T_j - T_{j,ref})) \tag{2.24}$$

$$E_{off} = E_{off,ref}(\frac{I_{out}}{I_{ref}})^{ki}(\frac{V_{in}}{V_{ref}})^{kv}(1 + TC_{sw}(T_j - T_{j,ref})) \tag{2.25}$$

Therefore the switching losses are

$$P_{sw} = (E_{on} + E_{off})f_{sw} \tag{2.26}$$

and overall power losses over MOSFET are

$$P_{loss} = P_{con} + P_{sw} = R_{ds(on)}I^2_{d,RMS} + (E_{on} + E_{off})f_{sw} \tag{2.27}$$

During the turn-on process the drive circuit voltage changes from 0 to V_{gg}. First the gate voltage increases to the threshold voltage ($V_{gs,th}$), the time constant is defined by the gate resistor and the MOSFET input capacitors ($C_{gd} + C_{gs}$). The output will not change until the gate voltage reaches the threshold voltage. When the voltage reaches to the threshold voltage, the drain current rises to the load current (t_{ri} can be found from the datasheet) while the voltage over the MOSFET is V_{in}. Since we have voltage and current simultaneously, there will be losses over the device. The free-wheeling diode is still conducting during this time interval. In order to turn off the diode, all the minority carriers must be removed. The reverse recovery of the diode causes another loss in the MOSFET. The reverse recovery time and charge can be found from the datasheet and are used in loss calculation. After the diode has been turned off, the drain-source voltage decreases to the on-state value. The fall time value is found in the datasheet. The fall time can also be calculated by using the gate-drain capacitance figure from the datasheet of the MOSFET.

Due to its non-linearity the method of two points is used. The gate current during fall time is calculated as [6]

$$I_g = \frac{V_{gg} - V_{plateau}}{R_g} \tag{2.28}$$

Therefore the voltage rise times are calculated as

$$t_{rv1} = (V_{in} - R_{ds(on)}.i_d)\frac{C_{gd1}}{I_g} = (V_d - R_{ds(on)}i_d).R_g.\frac{C_{gd1}}{V_{gg} - V_{plateau}} \tag{2.29}$$

$$t_{rv2} = (V_{in} - R_{ds(on)}.i_d)\frac{C_{gd2}}{I_g} = (V_d - R_{ds(on)}i_d).R_g.\frac{C_{gd2}}{V_{gg} - V_{plateau}} \tag{2.30}$$

$$t_{rv} = \frac{t_{rv1} + t_{rv2}}{2} \tag{2.31}$$

2.2 Power diodes

The physical realization of a diode is shown in Fig. 2.9. It consists of three layers. A heavily doped n-type n^- layer on top of a lightly doped, a n-type n^+ layer and finally a

pn junction is created by diffusion in a heavily doped p-type layer that forms the anode. The thickness of each layer and doping levels are depicted in Fig. 2.9 [1].

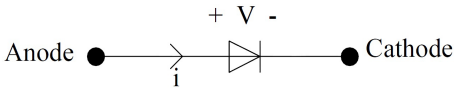


Figure 2.8: Diode circuit symbol

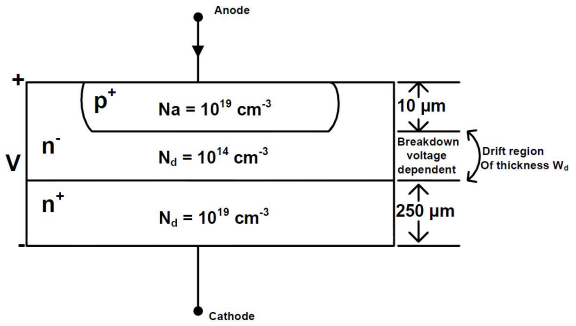


Figure 2.9: Cross section of a Diode

The I-V characteristic of the diode is shown in Fig. 2.10. In the forward operation the current flows linearly. An ohmic loss is created when a large current passes through diode. In the reverse operation a small leakage current flows until it reaches the breakdown voltage of the diode. In this condition the voltage remains constant, while the current is increasing significantly (limited by an external circuit). A large voltage and large current leads to a high power dissipation which can damage the device. Therefore operation of a diode at breakdown voltage must be avoided [1].

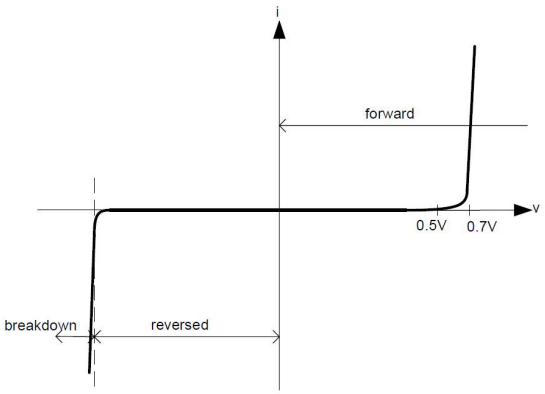


Figure 2.10: i-v characteristics of a diode

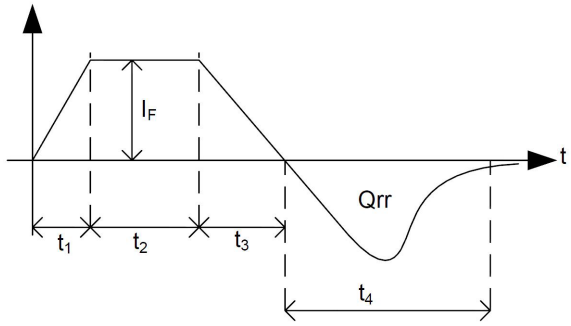


Figure 2.11: Changes in the diode current in one switching transient

Any power diode needs a specific time to transit from blocking state to conducting state and vice versa. This fact must be well thought-through while working in practical cases. These transitions are crucial because diodes are used in circuits either containing stray inductances which control the rate of change of the current ($\frac{di}{dt}$) or as a freewheeling diodes where the turn-off of a device controls $\frac{di}{dt}$. The changes in current of a diode are shown in Fig. 2.11 [1].

The time interval t_4 is called 'reversed recovery'. In the diode's datasheets plots of t_{rr} and Q_{rr} are given. The mathematical relations linking these quantitives are

$$I_{rr} = \frac{di_R}{dt} t_4 \tag{2.32}$$

$$t_{rr} = \frac{1}{2} I_{rr} Q_{rr} \tag{2.33}$$

The reverse recovery of the diodes influences the turn-on process of the switches, in which they cause current spikes in switches (over current). Hence a diode with good reverse recovery characteristics must be selected.

2.2.1 Diode lossess

Conduction losses of the diode can be estimated by using an approximation with a DC voltage source as on-state voltage drop and on-state resistance calculated from the forward current waveform ($I_f(V)$) [6].

The instantaneous diode conduction loss is

$$p_{con,D}(t) = V_D(t)i_F(t) = V_{D0}(t)i_F(t) + R_D i_F(t)^2 \tag{2.34}$$

The average diode conduction loss is

$$\begin{aligned} P_{con,D} &= \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{con,D}(t)dt \\ &= \frac{1}{T_{sw}} \int_0^{T_{sw}} (V_{D0}(t)i_F(t) + R_D i_F(t)^2)dt \\ &= V_{D0} i_{F,av} + R_{D(on)} I_{F,RMS}^2 \end{aligned} \tag{2.35}$$

During the turn-on switching transients the losses in diode is due to reverse recovery energy.

$$E_{rr} = \int_0^{t_{ri}+t_{fv}} V_D(t)i_F(t)dt = \frac{1}{4}Q_{rr}V_{in} \tag{2.36}$$

Therefore the losses in diode will be

$$P_{loss,D} = P_{con,D} + P_{rr,D} = V_{D0} i_{F,av} + R_{D(on)} I_{F,RMS}^2 + \frac{1}{4}Q_{rr}V_d \tag{2.37}$$

2.3 BJT

2.3.1 Introduction

A power transistor has a 4-layer construction that are oriented vertically and consists of p-type and n-type doping such as *npn* transistor shown in Fig. 2.13. The transistor has three terminals as indicated in Fig. 2.12, and they are labeled base, collector and emitter. In most power applications the base is the input terminal, the collector the output and the emitter the common between input and output. The vertical construction is preferable because of the maximum cross section area achieved for the current to flow. Another advantage of this construction is the minimization of the on-state resistance and thermal resistance therefore the power dissipation will be smaller.

The doping level in each layer and thickness of each layer affect the characteristics of the device significantly. The doping of the emitter layer is quite large, whereas the base doping is average. The n^- layer creates the half of the collector-base junction. It is named collector drift region and has small doping region. On the other hand the n^+

layer terminates the drift region and has a doping similar to emitter doping. This region connects the collector to the outside. The breakdown voltage of the transistors is defined by the thickness of the drift region. The thickness of the base drift region is a trade off between good amplification capability and breakdown voltage capability. Therefore this layer can be from several microns to tens of microns in thickness.

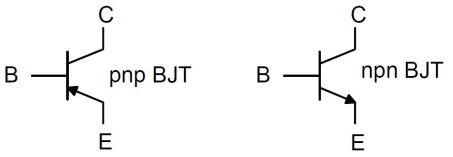


Figure 2.12: npn-BJT and pnp-BJT circuit symbols

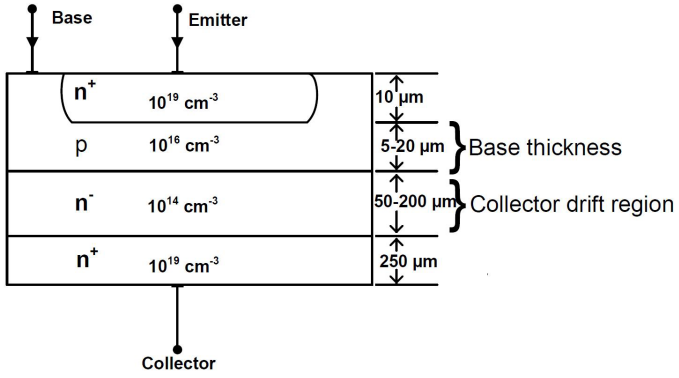


Figure 2.13: Vertical cross section of a npn BJT

2.3.2 I-V characteristics

The i-v characteristics of a transistor is shown in Fig. 2.12. Based on a different base current, different i_c as a function of V_{ce} is created.

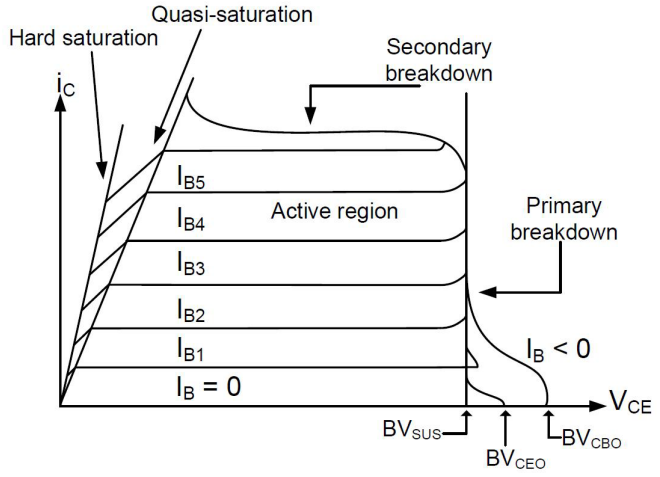


Fig. 2.14 BJT I-V characteristics

The maximum collector-emitter voltage that can be sustained to the transistor is named BV_{SUS} while a substantial amount of current is passing through the collector-emitter. When the base current is zero the maximum voltage that can be sustained to the device is called BV_{CEO} which is collector-emitter voltage when the base is open circuited. The transistor's voltage withstand capability is determined based on this voltage. The voltage BV_{CBO} is the collector-base breakdown voltage when the emitter is open circuited. The primary breakdown region is due to the breakdown of the collector-base junction and large amount of current passing through it. This region must be avoided due to substantial power dissipation that lead to such breakdown. The second breakdown region should also be avoided because of the large power dissipation that can cause a BJT failure.

2.3.3 Switching characteristics

The BJT is turned on when a voltage is applied to the base junction and results in creation of a collector current. During the delay time there is no build-up of charges because the charges on the BE capacitor must be discharged and the junction be forward biased so that the carrier junction can start conducting. Therefore during this time only base current is flowing and base-emitter voltage changes. After this time the base-emitter voltage changes sign and the growth in the stored charge starts thereby collector current start rising until it reaches its on-state value at 't_{ri}'. The collector-emitter voltage remains unchanged during this time interval. After current rise time this voltage start falling quickly. The voltage fall time has two parts. The first time interval is t_{fv1} when the device enters the Quasi saturation in which the carrier injection into drift region begins from the C-B junction. The second time interval is called hard saturation when the excess carriers have completely passed across the drift region and occurs after t_{fv2}. In Fig. 2.15 the turn-on waveforms are depicted

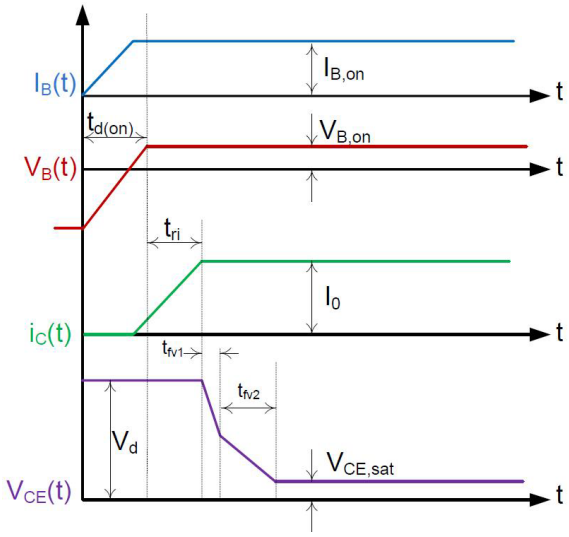


Figure 2.15: BJT turn-on waveforms

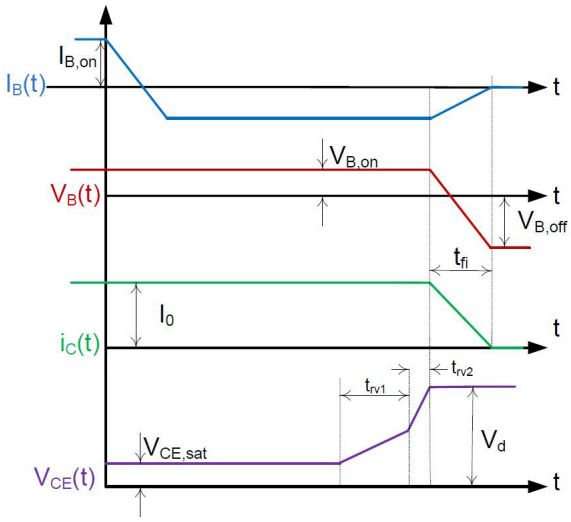


Figure 2.16: BJT turn-off waveforms

Turning off the transistor means removing all the stored charges in it. In order to do so the base current must be turned to zero. Removing all the charges could take a while so for expediting the process the base current is turned to a negative value. After this time the transistor enters the quasi region and the collector-emitter voltage starts increasing. As soon as the stored charges are reduced to zero at the C-B end of the drift region the transistor enters the active region. The V_{ce} reaches the dc voltage after t_{rv2} and the collector current then becomes zero. The waveforms regarding the turn-off transient of the BJT are shown in Fig. 2.16

2.4 Drive circuit

The drive circuits must be designed in such a way that they minimize the turn-on and the turn-off times due to the high power dissipation during the switching transients. During on state condition it must provide sufficient power to keep the switch on. Since the stray inductances that may trigger a turn-on of the switch, drive circuit should send a reversed bias signal to lower the turn off losses and keep the switch off during the off state

[1]. The drive circuit is an interface between the control system and the power switch. It augments the control signal to an adequate level for turning on and off the switches. It also creates electrical isolation between the control system and power circuit for protecting the control system against faults. In Fig. 2.17 the drive circuit of the MOSFET is shown.

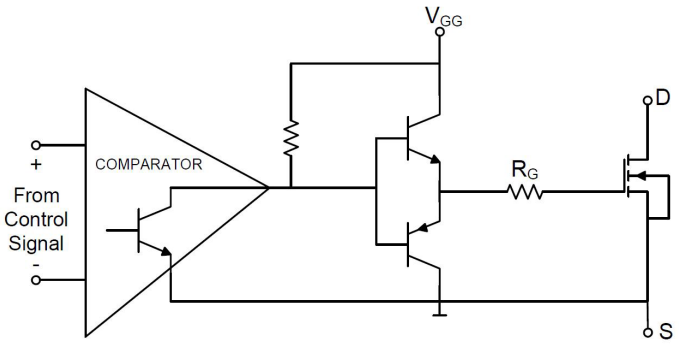


Figure 2.17: MOSFET drive circuit

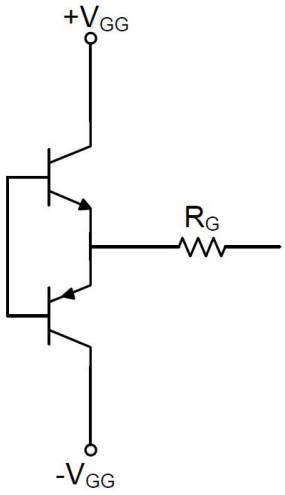


Figure 2.18: Bipolar output drive circuit

During the turn on process transistor in the comparator is turned off, therefore the npn transistor is turned on in order to supply a positive gate voltage to the MOSFET. During the turn off process the pnp transistor is turned on and the gate is shorted to the source through the gate resistance R_g [1].

In order to decrease the switching times the drive circuit must turn off the switch as fast as it turns it on. Thus the drive circuit with a bipolar output is needed in this case. Terminals of the control circuit are needed to be reversed to have a fast turn off (Fig. 2.18).

To isolate the drive circuit from signal generator optocoupler can be used. This device consists of a LED and an integrated circuit. In this project two light emitting diodes are used. First one transmits the gate control signal. The second one turns on during fault conditions.

2.4.1 Gate resistance

The switching behavior of the device to a large extent is controlled by the gate resistor. By changing this resistor the amount of current flowing to the MOSFET is varied so the charging and discharging times of the capacitors in the gate will be changed. Besides switching time, switching losses, reverse bias safe operating area, short circuit safe operating area, EMI, $\frac{dv}{dt}$, $\frac{di}{dt}$ and reverse recovery of the free-wheeling diode are affected by the gate resistor. Thus high accuracy is needed to design and selection of R_g [7].

By reducing R_g the gate current will increase and this will lead to a faster switching. However this causes high $\frac{di}{dt}$ in the switch which produces high voltage spikes in it, that can destroy it. In half bridge converters the blanking time is affected by the gate resistor. High values of R_g increases the switching fall time current, so the blanking time may exceeds its minimum value. In Table 2.1 different characteristics in the circuit are shown in accordance to the changes in the gate resistance [7].

Table 2.1: Switching behavior by changes in the gate resistor

Characteristics	High value of R_g	Small value of R_g
t_{on}	↗	↘
t_{off}	↗	↘
E_{on}	↗	↘
E_{off}	↗	↘
Turn-on peak current	↘	↗
Turn-off peak current diode	↘	↗
$\frac{dv}{dt}$	↘	↗
$\frac{di}{dt}$	↘	↗
Voltage spike	↘	↗
EMI noise	↘	↗

2.5 Measuring devices

Obtaining accurate results is one of the most importance issues in the laboratory tests. Therefore reliable equipments are needed in such a way that noises will not affect their performance. In this project Hall Effect sensor, rogowski coil, active differential probe and a coaxial shunt cable are used to measure voltage and current signals from the devices to the oscilloscope [8].

2.5.1 Voltage probe

In an ideal situation a probe must meet following qualifications to be used in a measurement set-up

- Easy and appropriate connection
- Safe signal transmission
- Zero signal source loading
- Minimum protection against noises

One of the most important features of having an accurate measurement is to have a correct physical connection. The size of selected probes must match with the test points including the head and the probe tips. The ideal probe should be able to transmit signals from the source to the oscilloscope safely, i.e. the original signal must be duplicated at the oscilloscope input. In order to do so the probes should have zero attenuation and very high bandwidth. The devices around the test point can be assumed as a signal source. Whenever a signal is sent from the circuit these devices act as a load and change the operation of the circuit and therefore the measured signal. An appropriate probe with high input impedance has the ability to damp the effect of these loads to keep the signal measured at the test point safe. These external devices may also introduce noises to the circuit which are added to the measured signal and are appeared as oscillations. By using effective shielding techniques we can get rid of these noises [9].

Probes circuitry

Depending on the type of measuring signal, the probe will form a different circuit. For measuring a DC signal (0 Hz frequencies) the probe appears as a simple conductor pair

with series resistors(Fig. 2.19). However for an AC signal the probe's circuit is much more complex (Fig. 2.20) [9].

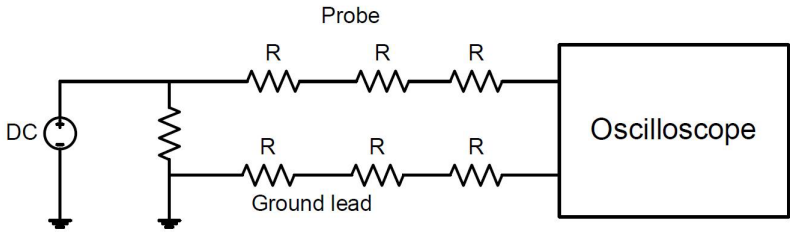


Fig. 2.19 Probe circuit for DC signals

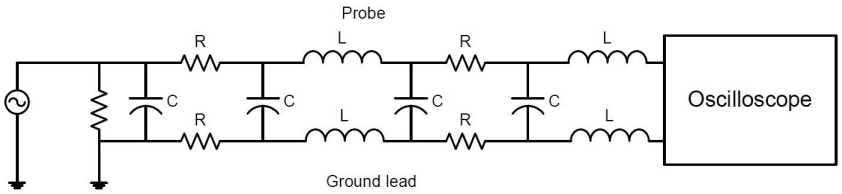


Fig. 2.20 Probe circuitry for AC signals

Bandwidth and rise time limitation

Bandwidth in measuring devices is the range of frequencies that the oscilloscope or probe are designed for. As a general rule in order to have an accurate measurement the bandwidth of the oscilloscope should be *five* time higher than the frequency of the measured signal. This "five-times" is sufficient to ensure measuring higher frequency components on non-sinusoidal waveforms such as square waves [9].

Moreover hand the rise time of the oscilloscope/probe must be high enough for the measured signal. The preferred rise time of the oscilloscope/probe should be *three* to *five* times higher than the measured signal to have accurate measurement [9].

If the rise time of the oscilloscope/probe is not mentioned one can calculate the rise time using following formula

$$T_r = \frac{0.35}{BW} \tag{2.38}$$

It is important to know the bandwidth and rise time limitation of both the oscilloscope and probe because when a probe with different bandwidth/rise time is connected to an oscilloscope a new set of bandwidth/rise time is achieved. The best way to cope with this problem is to refer to manufacturer's notes for appropriate probes for the specified oscilloscope [9].

Dynamic range limitations

All probes have a high voltage safety limit that should not be exceeded. In active probes the maximum safe voltage is in the range of tens of volts. Moreover the safety considerations of the oscilloscope should be noted. For example the oscilloscope used in this project has maximum sensitivity 1 mV - 10 V/div, which means that on a ten-division display an accurate measurement from 5 mV peak-to-peak to 50 V peak-to-peak is possible. With

a 1X probe the dynamic measurement range is the same as the oscilloscope sensitivity range. But if you want to measure voltages higher than this range the attenuation rate of the probe must be set to 10X [9].

Probe compensation

Before performing any measurement we have to make sure that our probes are fully compensated. If an uncompensated probe is being used to measure the signals errors are introduced exclusively during the signal rise times and fall times. Thus right after connecting any probe to the oscilloscope compensation is the job number one.

To perform probe compensation these instruction should be followed

1. Attach the probe to the oscilloscope.
2. Attach the probe tip the probe compensation test point (in some oscilloscopes named Calibration).
3. By using adjustment tool supplied with the probe tune the signal to obtain a flat signal.
4. If the oscilloscope has a calibration procedure, run it to gain better accuracy.

In Fig. 2.21 signals from under-compensated, over-compensated and properly compensated probes are depicted respectively.

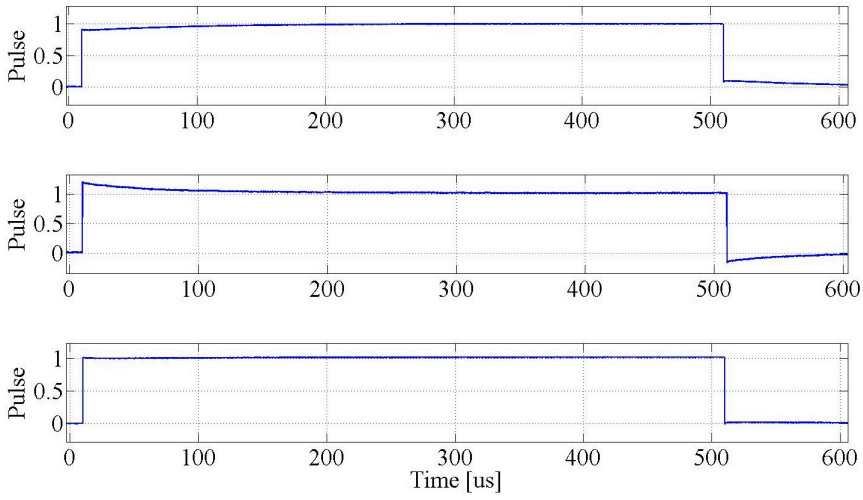


Fig. 2.21 Probe Compensation

Probe ground leads

In order to avoid unwanted ringing in the measured signals the ground leads of the probe should be as short as possible. Having large ground leads makes it possible to move the probe freely in the circuit and perform measurement on different test points. However the added inductance causes ringing in the measurement of fast transient waveforms.

Probe selection

Probe selection depends on the type of signal, signal frequency and rise time, signal amplitude, test point geometry and of course oscilloscope capability including bandwidth and rise time. In order to capture signals in fast transitions (rise and fall times) for high frequency applications, probes with high sensitivity are required. In this thesis 500 MHz probes are used due to our measurement during MOSFET turn-on and turn-off transients. These probes were selected based on their high bandwidth and quick rise time capability.

Differential measurement

Generally all measurements are differential measurements. A common application is to connect the probe to the test point and the probe ground lead is attached to the circuit ground. The measured signal is a difference between the test point and the ground. The other is to use either two probes and measure the voltage of a device or using an active differential probe. In this case the required signal is summed algebraically to one signal and is sent to the oscilloscope as a reference to the ground.

The oscilloscope must have "*Math*" option in order to be used with two voltage probes for creating the differential measurement. The selected probes are required to have same specifications such as bandwidth and rise time to be able to measure more accurately. Before performing this type of measurement one separate test must be performed on the probes in which for one specific signal both probes should give an identical response. If there are differences between the two measured signals, the probes must be tuned carefully. In the following figures before and after the tuning for two probes are depicted. Before tuning there is a distinctive difference between the probes therefore a fine tuning is performed and the probes gives identical response for a same signal.

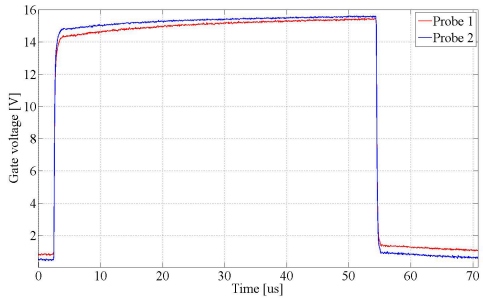


Figure 2.22: Probe comparison before tuning

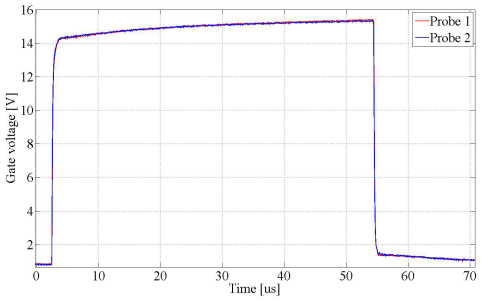


Figure 2.23: Probe comparison after tuning

2.5.2 Rogowski coil

Rogowski coils are used to detect and measure currents. They measure current using the magnetic field around the test object. This magnetic field induces a voltage in proportional to the rate of changes of current in the coil, therefore by integrating the voltage the measured current is achieved. The rogowski coil uses a long wire for measuring currents which is bent around the test object.

The accuracy of the measured current depends on the position of the coil. This is due to the small variation in the winding density and the coil cross section area. In Fig. 2.24 different positions of the coil are illustrated and the error of the device in area is specified in Table2.2 [10].

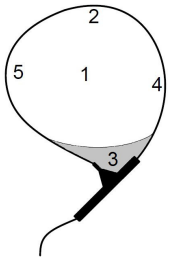


Figure 2.24: Conductor position in rogowski coil

Table 2.2: Rogowski coil accuracy areas

Conductor Position	Typical error(%)
1	0.2
2	±1.0
4 and 5	±2.0
3	-5

One simple measurement is performed on a rogowski coil to show how the position of the current transducer could affect the accuracy of the measurement. The drain-source current of the MOSFET is checked with two identical rogowski coils with the same sensitivity. One measurement is done in the zone 1 and the other in zone 3 specified in Fig. 2.24. As mentioned in the Table 2.2 if the conductor is positioned in zone 1 the highest accuracy is achieved. While in zone 3 there is -5 percentage of error in capturing the current signal. In Fig. 2.25 the result is shown.

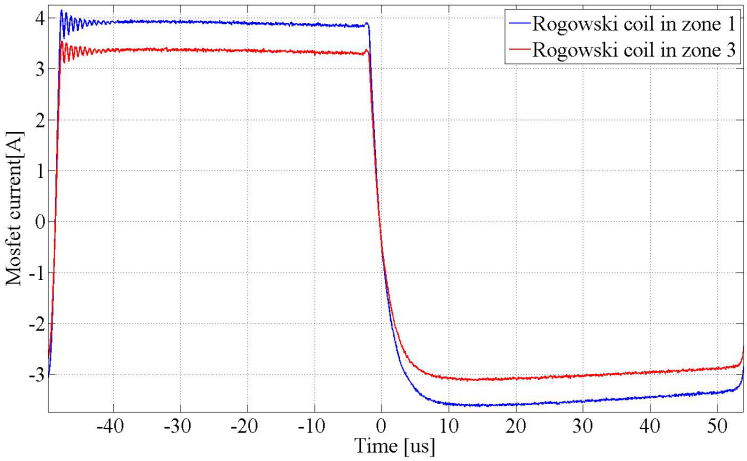


Fig. 2.25 Registered signals by rogowski coil

Some of the advantages of rogowski coil are

- Capable of measuring large current without saturating
- Ease of use
- Having a large bandwidth; 0.1 Hz up to 30 MHz
- Providing an isolate measurement at ground potential
- Capable of measuring fast changes in current up to 40kA/μs

There is a DC offset in rogowski coil which is a function of the amplifier and the circuit in the integrator. This value is below 1mV-50mV depending on the measured current. Due to low ranges of measured current, high gain in the integrator is required. This results in a

high DC offset. In Fig. 2.26 the gate current of a MOSFET measured by a rogowski coil is shown, the current is supposed to become zero after a while but due to the device error it is not.

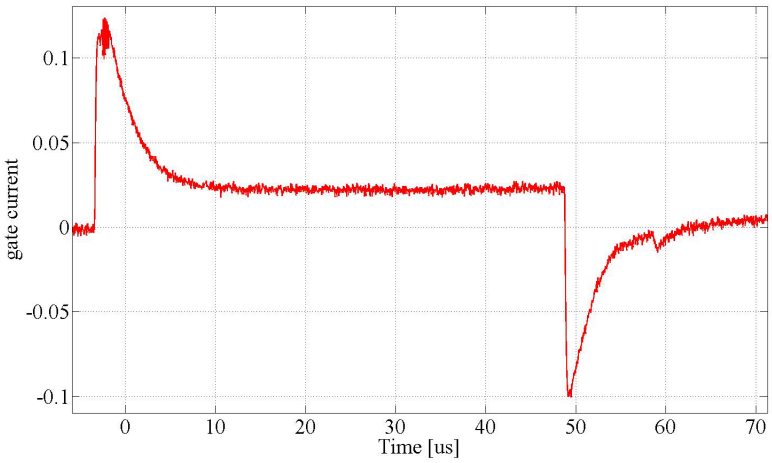


Fig. 2.26 MOSFET gate current measured by rogowski coil

In Table 2.3 a comparison between these measuring devices is shown [8]:

Table 2.3: Measuring device comparison

	Coaxial shunt	Hall effect sensor	Rogowski coil
Isolation	Worst	Best	Best
Weight	Worst	Average	Best
DC response	Best	Best	Worst
Low frequency response	Best	Best	Best
Fast current change	Best	Average	Best
Output	Voltage	Voltage	Voltage
Ease of installation	Worst	Average	Best
Cost	Worst	Average	Best

In this project these equipment were used for the measurement:

- Lecroy Wavepro 715Zi - oscilloscope
- PEM CWT015 - rogowski coil; sensitivity $200\frac{mv}{A}$
- Lecroy PP009 - voltage probe; sensitivity 500 MHz

Chapter 3

Case set-up

In this thesis different tests were performed on the drive circuit and MOSFET. Firstly drive circuit was used to switch a RC circuit and then to switch a COOLMOS. The MOSFET was tested in one phase leg set-up to analyze its gate drive and switching characteristics during the turn-on and turn-off transients.

The whole system is composed of two parts:

- High power circuit
- Drive circuit

3.1 High power circuit

The electric board that was used in this project is shown in Fig. 3.1. The board was originally built for one-phase-leg inverter. The input voltage is applied through the junctions 'J1-A' and 'J2-A'. Four capacitors are placed in the input to smooth the dc-link voltage. The place of switches and diodes are marked with Q and D respectively. Finally an inductive load is connected to junctions 'J4-A' and 'J5-A'. If the board is needed to be used for a three phase inverter then the junction 'J3-A' will be used to connect the board to the next phase.

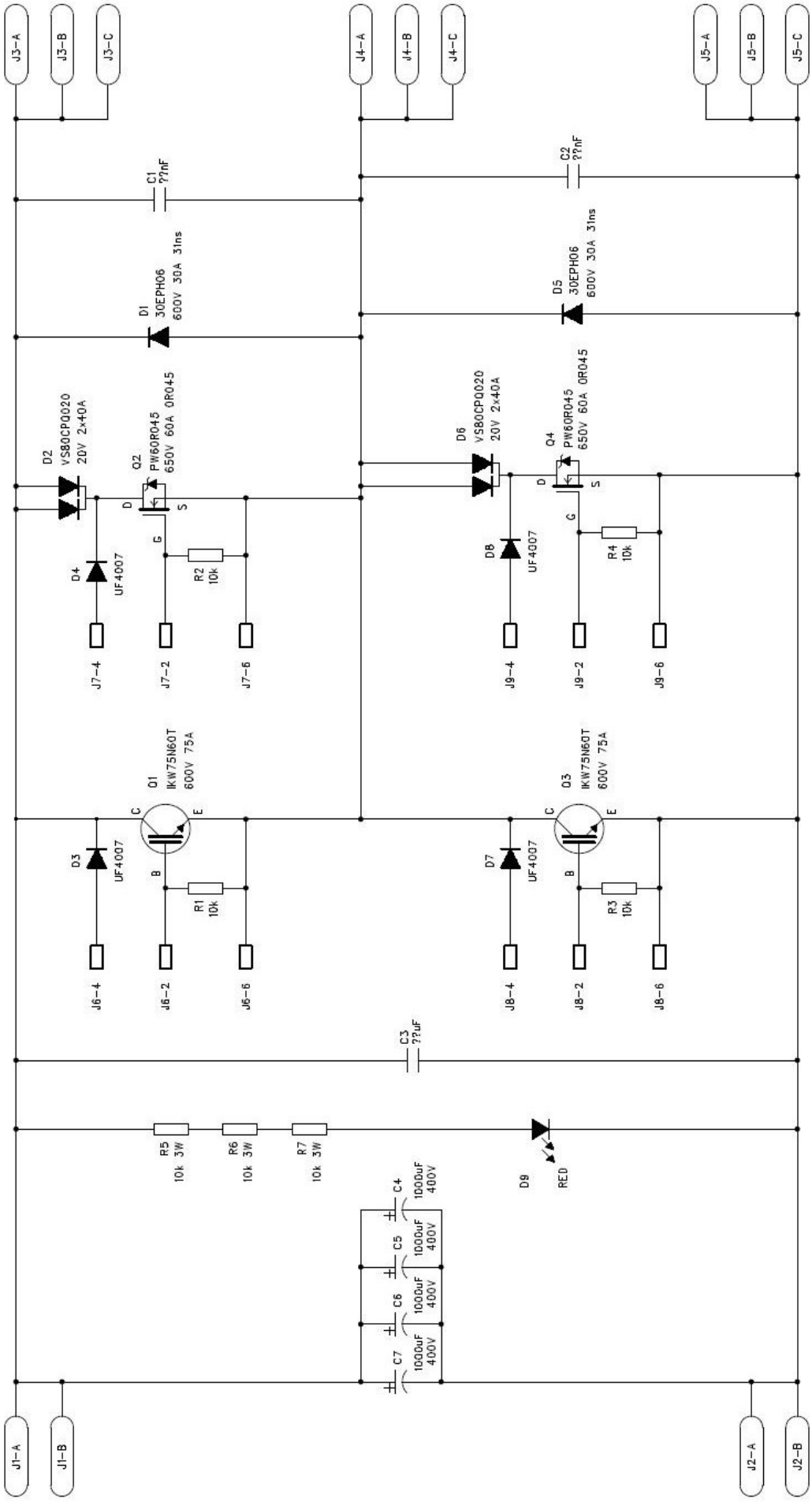


Fig. 3.1 Power circuit single line diagram

3.1.1 Voltage source

Input voltage is supplied through a DC voltage source. The range of the voltage are 10 to 50 volts for testing the switches and 20-200 volts for the inverter. The higher the input voltage the higher the current injected into the circuit. Hence more power will be dissipated in the devices. A small resistor is put in series with the voltage source in order to protect the switches against short circuit caused by turning on both switches in the leg.

3.1.2 Capacitor bank

The input capacitors are responsible to stabilize the input voltage applied to the switches. In this project four capacitors are put in parallel to each with the capacity of one millifarad to reach four millifarads.

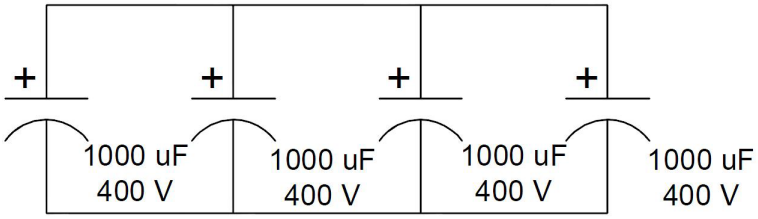


Fig. 3.2 Capacitor bank specifications

3.1.3 MOSFET

The MOSFET used in this project is an Infineon IPW60R045CP CoolMOS with specifications given in Table3.1:

Table 3.1: MOSFET specifications

Type	$V_{ds,Tjmax}$ (V)	$R_{ds(on)}(\Omega)$	$Q_{g,typ}$ (nc)	t_{rr} (ns)
IPW60R045CP	650	0.045	150	600

The features of these MOSFETs are,

- Very low on-state resistance
- Low gate charge
- High capability with di/dt and dv/dt
- Poor reverse recovery characteristics

3.1.4 Schottky Diode

For the free-wheeling diode a schottky diode with fast recovery characteristic is used. In the Table3.2 more specifications of this diode is shown:

Table 3.2: Diode specifications

Type	V_R (V)	$I_{F,av}(A)$	T_J (°C)
80CPQ020PbF	20	2x40	-50to150

The other features of this diode are,

- Ultra low forward voltage drop
- High frequency operation
- Lead (Pb)-free
- Designed and qualified for industrial level

3.1.5 Freewheeling Diode

Because of the low nominal voltage and current characteristics of the Schottky diode another diode was used as a freewheeling diode. This diode also has an appropriate reverse recovery characteristic with high breakdown voltage. In Table3.3 more specifications of this diode is shown:

Table 3.3: Diode specifications

Type	V_R (V)	$I_{F,av}(A)$	T_J (°C)	t_{rr}(nS)
30EPH06	600	30	-65 to 175	28

The other features of this diode are

- Fast recovery time
- Low forward voltage drop
- Low leakage current
- 175°C operating junction temperature

3.2 Load

In this thesis an inductive load is used. In order to have the load current stiffen a highly inductive load should be considered, in this case a 11mH as inductor and 14Ω as resistor were selected.

3.3 Drive circuit

The gate drive used for the experiments is HCPL-316J from ”AVAGO technology”. The gate driver is a highly integrated power control device for IGBT/MOSFET gate drive including fault protection package. Applying TTL signal as an input, allows direct interface with the microcontroller, moreover being facilitated by the optocouplers for an isolating of the control stage from the power stage, switches with power rating up to 150A and 1200V can be driven. The propagation delays between the microcontroller and the switch is reduced by using fast internal optimal links. The output IC protect the device during the overcurrent transients and the second optical link protects the controller. If a fault in switching device is detected the output detector of IC immediately starts a ’soft shutdown’ sequence, descending the MOSFET/IGBT current to zero in a controlled manner to avoid any damage to the switching device such as overvoltages. The buffer IC receive the fault signal via the LED2, which disables the gate control input [11].

The other important features of this drive circuit are

- Two sets of protections; Desat detection and under voltage lock out with hysteresis
- Wide operating V_{CC} range 15:30 V
- -40° to +100° operating temperature range
- User configurable: inverting, noninverting, auto-reset, auto-shutdown

In the datasheet some parameters regarding the internal devices are given, as well as propagation delays and rise times of the voltages. These times were checked with the experimental results and they match quite well. In the Fig3.3 signal generator's output signal, base voltage, collector voltage and gate voltage are depicted.

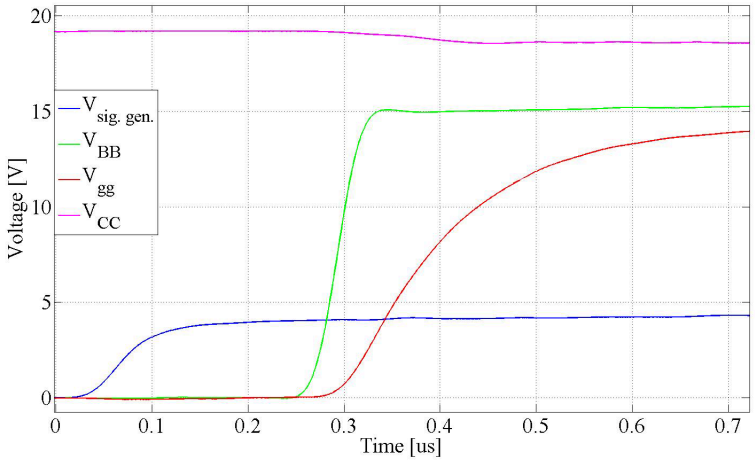


Fig. 3.3 Signal generator, Base Voltage, Gate voltage and Collector voltage signals

In the datasheet the delay time of the propagated signal from the signal generator to the V_{gg} is mentioned to be 300ns however in the experimental results, it is found to be 250ns.

Fig 3.4 shows the drive circuit used in this project. The operation starts by triggering SW4 which turn on the drive circuit. The optocoupler is specified in the figure as Q1 and Q2 are the transistors operating during turn on and turn off respectively. R5, R6, R7 and R8 are turn on gate resistors and R9, R10, R11 and R12 are turn off gate resistors. B1, B2, B3 and B4 are the batteries supplying the drive circuit power. By changing the SW3's status (Switch number three) the required voltage will be provided to the circuit. Generally batteries 1 and 2 are supplying the circuit and both aggregate to 18V. However about 2V of this voltage is dissipated in the BJTs. Therefore 16V will be applied to the switches as V_{gg}.

In order to change the gate resistor, 2 sets of switches are put in the drive circuit; one for the turn-on path and the other for the turn-off path. In each set there are 4 switches controlling the resistors. If all the switches are off then the gate resistor will be 100Ω. Switch 1 adds two paralleled resistors, switch2 adds four paralleled resistors, switch 3 adds eight paralleled resistors and finally switch4 adds 16 paralleled resistors (each resistor has 100Ω resistivity). By changing these switches, different gate resistor will be achieved. In this project two gate resistors were selected; 100Ω (all switches off), 14.5Ω. Decreasing the gate resistor to a very small value will cause oscillations in the waveforms and make it difficult to obtain good waveform. That is why 14.5Ω is the smallest value selected for the gate resistor.

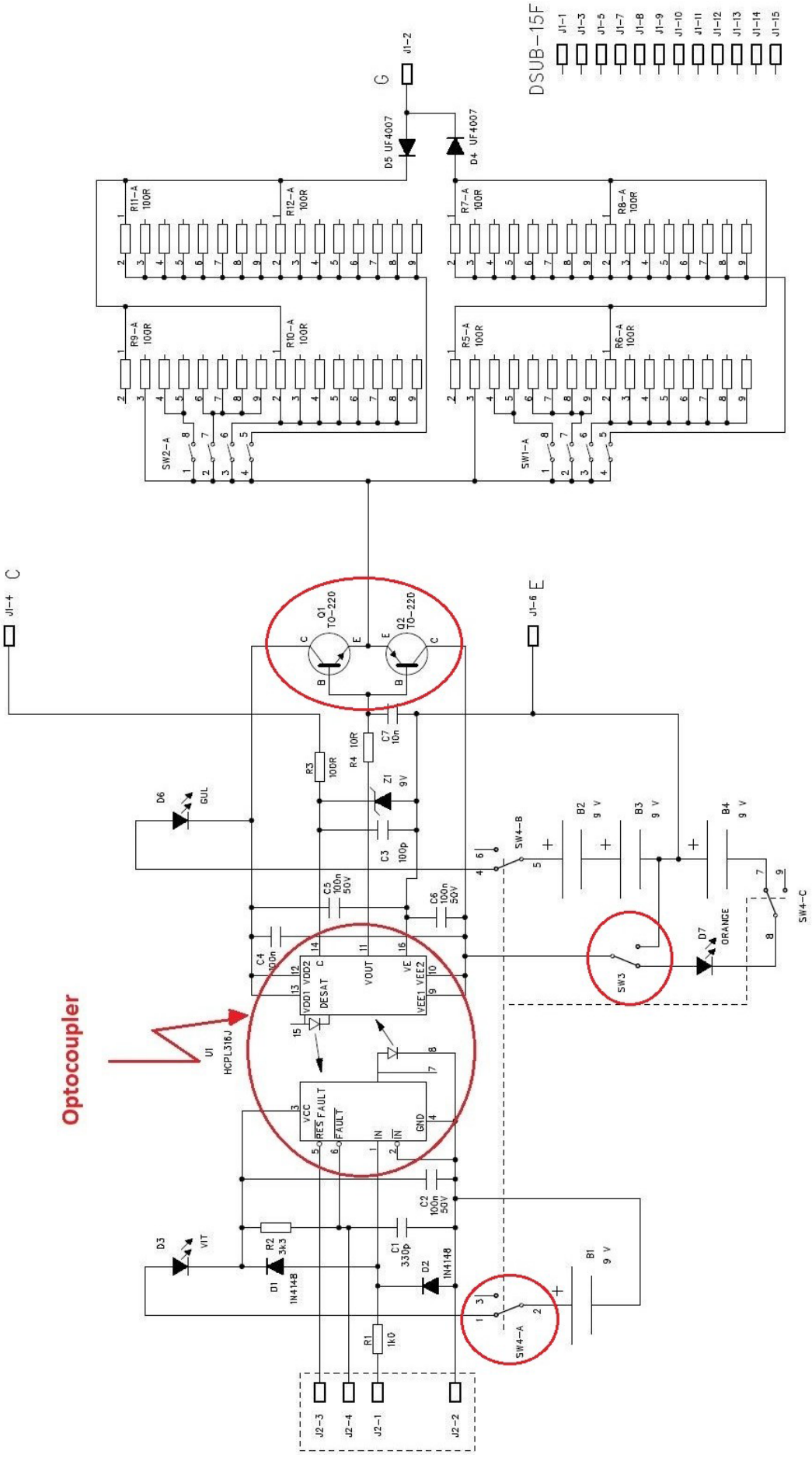


Fig. 3.4 Drive circuit single line diagram

3.3.1 Drive circuit modeling

In this part, the performance of the drive circuit is investigated. The aim is to check how the current signal is created. There are two batteries supplying the the circuit. The current is generated and passes through the BJTs and then through the gate resistors and finally to the gate of the MOSFET.

The path from the batteries to the MOSFET creates a R-C circuit and the gate voltage equation is affected by the resistors and capacitors in the circuit. So all the devices in the path must be checked for their internal resistors.

Firstly the performance of the BJTs must be checked. They are turned on and off by the current i_B that is generated from the 'V_{out}' of the optocoupler through R_4 which is 10Ω. In Fig 3.5, V_{ce} for different gate resistors are depicted

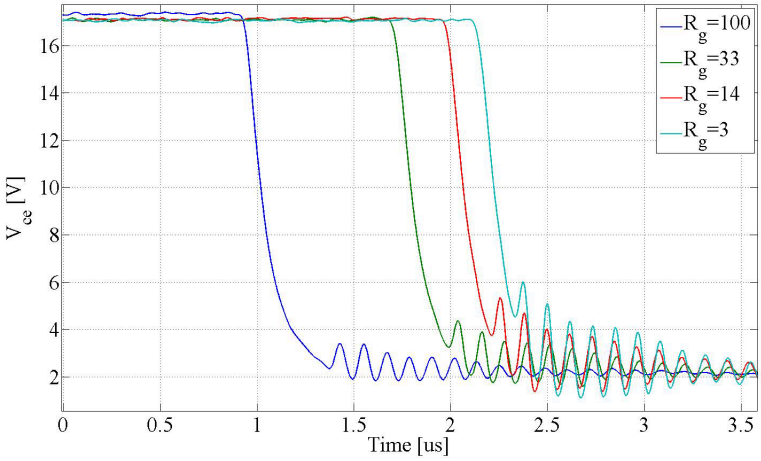


Fig. 3.5 Collector-emitter voltage for different gate resistors

It can be seen that there is a high voltage drop over the BJTs which abates the gate voltage. In order to test the effect of the BJTs, one other test is performed in which the gate voltage with and without the BJTs are observed. It is observed that rise time of the signal for the case without BJTs is 54ns, but when BJTs are involved the rise time is 230ns. Moreover there is an approximately 1V voltage drop between two cases. Fig 3.6 shows the signals for both cases.

The BJTs used in the drive circuit have a relatively high voltage drop. This value is not satisfying and in order to have a better performance from the circuit, transistors with lower voltage drop and faster transients are required.

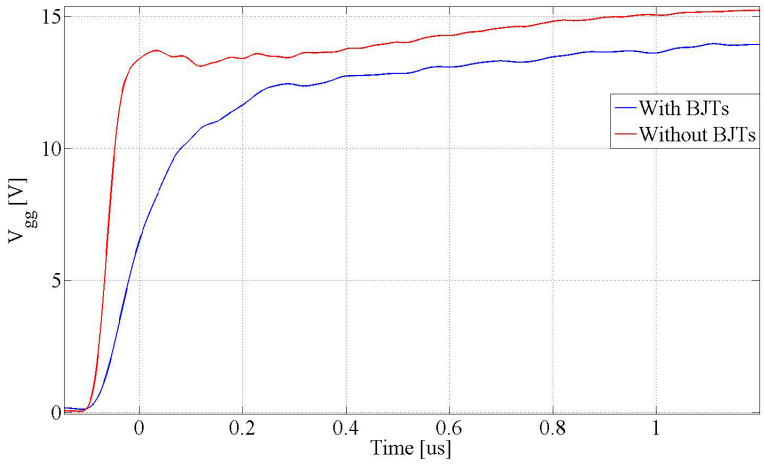


Fig. 3.6 Effect of BJTs on the gate voltage

D_4 and D_5 are the diodes which decide the path for the gate current during the turn-on and the turn-off transients respectively. The turn-on and turn-off path are separated in order to select different gate resistors for each transient. In the data sheet 17pF of capacitance is mentioned for the diode. This diode was put in a simple R-C circuit and the currents and voltages were checked and it was observed that the internal capacitance of this diode is not big enough to affect the currents and voltages of the drive circuit.

In order to simplify the circuit, both of these diodes are detached from the circuit and gate voltage and current are observed to determine how this diode could affect the mentioned variables. In Fig3.7 the gate voltage and current before and after attaching the diodes D_4 and D_5 are shown.

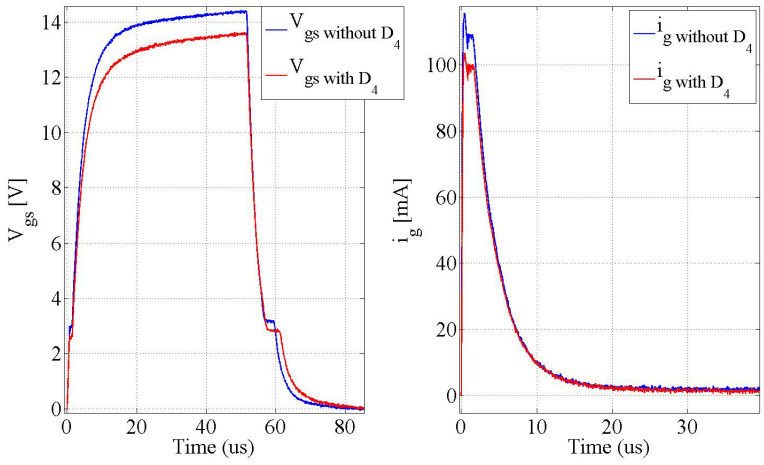


Fig. 3.7 Gate-source voltage and gate current with and without D4

It is obvious in the figures that when the diodes are in the circuit, less current is injected to the MOSFET due to their voltage drop. Also the voltage that appeared in the gate-source is less than the case when the diodes are removed. Moreover, inherent parasitics are not big enough to create delays in current and voltage signals.

Now the circuity of the gate drive is going to be investigated considering the devices involved during switching intervals and their effects are discussed.

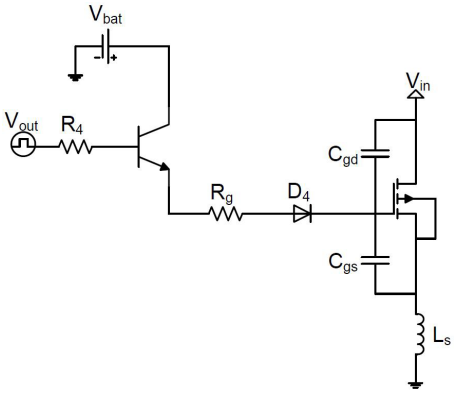


Figure 3.8: Drive circuit equivalent circuit

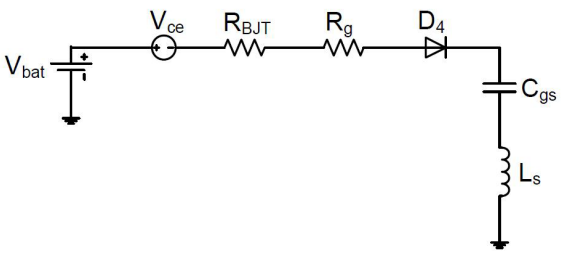


Figure 3.9: Drive circuit equivalent circuit during turn-on

In Fig 3.9 the equivalent circuit during turn-on is shown. If the parasitic inductances are assumed to be small and therefore be neglected, the rest forms a R-C circuit. The voltage of the capacitor ($V_{c_{gs}}$) is calculated as

$$V_{in} = Ri + V_{c_{gs}} \tag{3.1}$$

The current can be substituted with $\frac{dq}{dt}$ and the capacitor voltage with $\frac{q}{C_{gs}}$.

$$V_{in} = R\frac{dq}{dt} + \frac{q}{C_{gs}} \tag{3.2}$$

$$CV_{in}dt = RCdq + qdt \tag{3.3}$$

$$(CV_{in} - q)dt = RCdq \tag{3.4}$$

$$\int \frac{-dt}{RC} = \int \frac{dq}{q - CV_{in}} \tag{3.5}$$

The capacitor voltage is

$$V_{C_{gs}} = V_{in}(1 - e^{\frac{-t}{\tau}}) \tag{3.6}$$

where $\tau = RC$
Finally the gate voltage will be

$$\begin{aligned} V_{gg} &= V_{C_{gs}} + R_g i_g \\ &= V_{in}(1 - e^{\frac{-t}{\tau}}) + Ri_g \end{aligned} \tag{3.7}$$

The input voltage is supplied from the batteries, although it is affected by the voltage drop caused by BJTs.

3.4 Measurements

The measurement part is divided into two sections; RC circuit test set-up and MOSFET test set-up circuit. In another test the drive circuit characteristics, first of all a couple of test are performed on the simple RC circuit and then the gate dive are used for switching a COOLMOS.

In the first step V_{gg} and i_g are investigated. The gate current is observed by two methods. First by a rogowski coil the current is recorded. The problem with the rogowski coil is their incapablity of reading signals under specific frequencies. In the second method a differential measurement is used on the gate resistors and the gate current is observed. In Fig. 3.10 gate voltage and gate currents in the mentioned methods are shown.

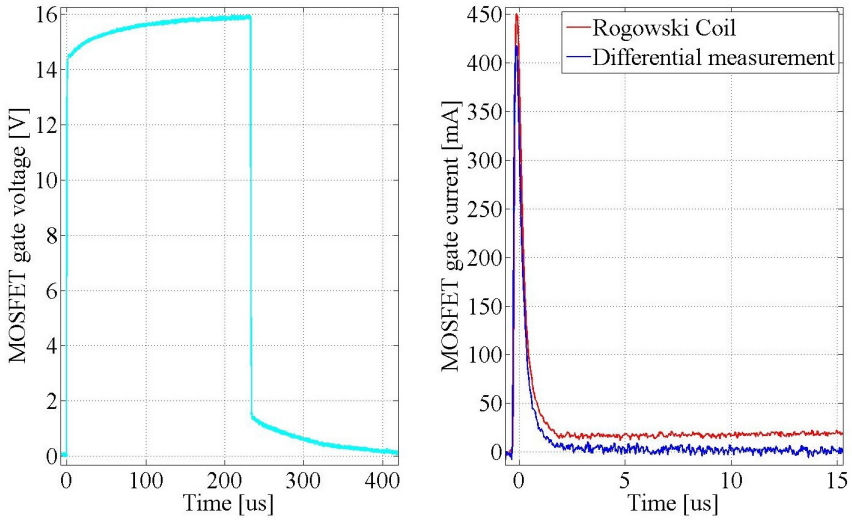


Fig. 3.10 MOSFET gate voltage and gate current

From the figures, one can say that the waveforms match in the initial part. However after fall of the current only the second method gives a correct answer. In rogowski coil's response there is a DC offset in the measured signal. The gate drive voltage(V_{gg}) has a sharp rise to 14.3V during the turn-on and increases to 16V. The delay time for the gate voltage to rise from zero to V_{gg} which in this case is 1.4μs which is off interest. This could cause a delay in the gate drive response. In order to create realistic cases, in all simulation set-ups the gate voltage from the experimental results was used so that the result would be comparable.

The other important thing to be considered is the checking the values of the resistors and capacitors. There is risk of errors in the values mentioned on the devices. Therefore the correct values will be used in the simulation test set-up.

3.4.1 RC circuit test set-up

In this part the gate drive was used to switch a RC circuit. In Fig. 3.11 the test set-up is depicted.

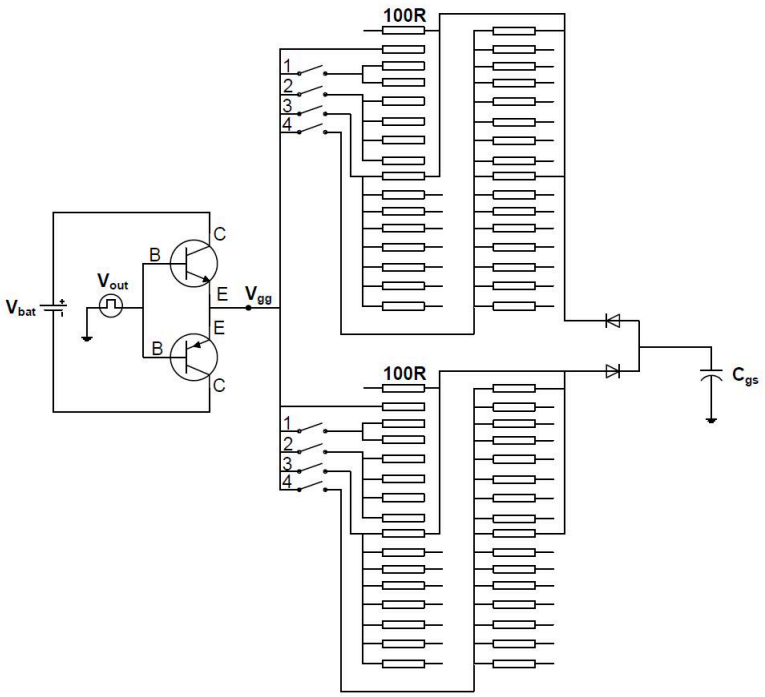


Fig. 3.11 RC test circuit

- RC circuit ($C_{gs} = 68nf$ and $R_g = 210\Omega$)

In the first test set-up, a big capacitor (68nF) and a gate resistor (210Ω) are selected. The maximum available resistor in the gate drive is 100Ω so another (110Ω resistor) is added in series to create the desired gate resistor. The switching frequency of the applied pulse to the circuit is 2kHz. In this case it was not possible to increase frequency to higher values, otherwise it would be difficult to investigate the waveforms. The simulation part was performed in MATLAB/Simulink.

- RC circuit ($C_{gs} = 10.0nf$ and $R_g = 22\Omega$)

In the second case smaller components are selected for a faster response from the gate drive and to test it for higher currents. The capacitor is replaced by a smaller capacitor (10.0nF) and the resistor in the drive circuit is reduced to 22Ω.

3.4.2 MOSFET test set-up

In order to get familiar with the MOSFET characteristics and its switching performance two test set-up are used and the results were compared with the simulation that is a MATLAB script of the MOSFET turn-on and turn-off switching and loss calculation in the whole switching process.

MOSFET measurement set-up

The MOSFET was considered in a phase-leg setup as shown in Fig. 3.12. In the bottom switch the diodes were put. The applied voltage should be in accordance to the devices nominal voltage. Besides in the datasheet of the MOSFET necessary information of the MOSFET switching capabilities such as minimum R_g are given. These data must be checked with the test set-up to prevent any damages to the equipments. The schottky

diode can only handle 20V. Therefore only 10V is applied in the input. The applied voltage for the other diode is 50V due to its high voltage capabilities. The load was a R-L load consisting of 14Ω resistor and 11mH inductance. The higher the inductor value the higher the current will be. So the MODFET and diode must be able to handle this current otherwise they will be damaged. The switching frequency is 2kHz. Although both devices can perform in higher frequencies, the lower frequency was selected to have slower transients.

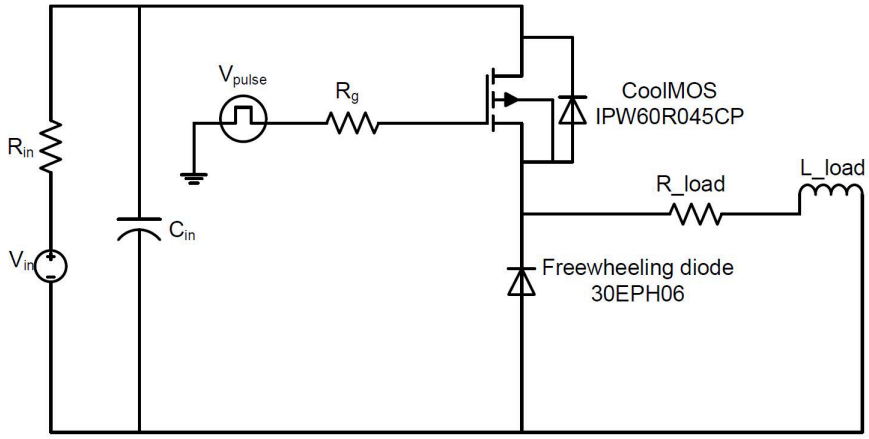


Fig. 3.12 MOSFET test set-up

As mentioned earlier during the switching transients the input capacitances are charged/discharged through the gate resistor. To overrule the influences of inherent capacitors of the MOSFET two capacitors are added in parallel to gate-source and to gate-drain of the MOSFET (68nF and 4.5nf respectively). The capacitors are 10 times higher than the parasitic capacitances in MOSFET.

The switching behavior of the device is observed and compared with simulation results. Two test set-ups are explained here.

- Test set-up 3: MOSFET with extra capacitors ($C_{gs} = 68nf$ and $C_{gd} = 4.5nF$)

Two capacitors are added to the device and tests are performed on the each circuit. The value of the capacitors must be checked achieve accurate results in the simulation. Moreover their voltage breakdown should be known before applying input voltage to prevent any damages to them ($C_{gs1} = 67.5nF$ and $C_{gd} = 5.3nF$).

Inherent capacitors of the MOSFET are changing bases on the voltage applied to the device. Therefore it is not possible to specify one value for the capacitors. Therefore by using datasheet diagrams the value for the C_{gs} and C_{gd} could be determined. ($C_{gs,Vin=50V}$ = 6.8nF and $C_{gd,Vin=50V}$ = 1nF)

So the new capacitors were

$C_{gs,new1}$=74.3nF

$C_{gd,new}$=5.6nF

- Test set-up 4: MOSFET test set-up

In this part all the capacitors are detached and the switching behaviour of the MOSFET, based on its inherent parasitics are investigated.

In all cases, gate voltage and current are observed. MOSFET's drain voltage and current for the last two cases are also observed and finally switching losses are calculated.

Chapter 4

Simulation, analysis and results

In this part the experimental and simulation results are shown. Results in each section are compared with the simulation results.

4.1 Test set-up 1

In this test the voltage over the capacitor and current through it are depicted for both experimental and simulation (Fig 4.1).

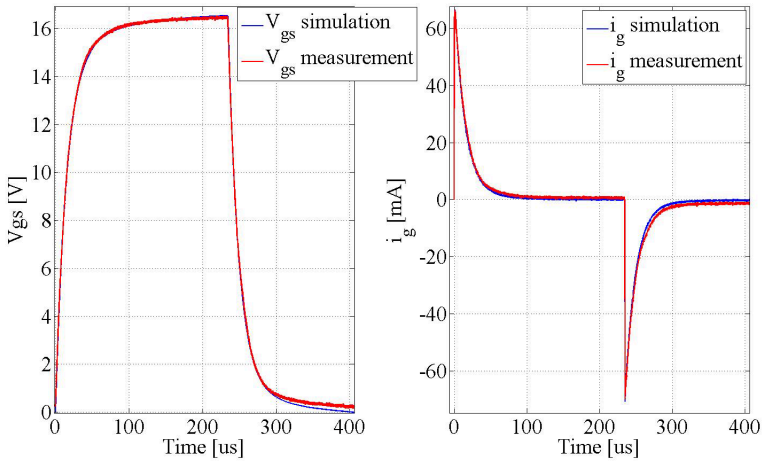


Fig. 4.1 Case1;Comparison between V_{gs} and i_g in simulation and measurement

The waveforms from both cases confirm each other. The currents have a sharp rising in the initial part and become zero simultaneously. Besides the voltages reach their maximum at the same time and have a sharp falling.

4.2 Test set-up 2

In Fig 4.2 results from the second case set-up are shown:

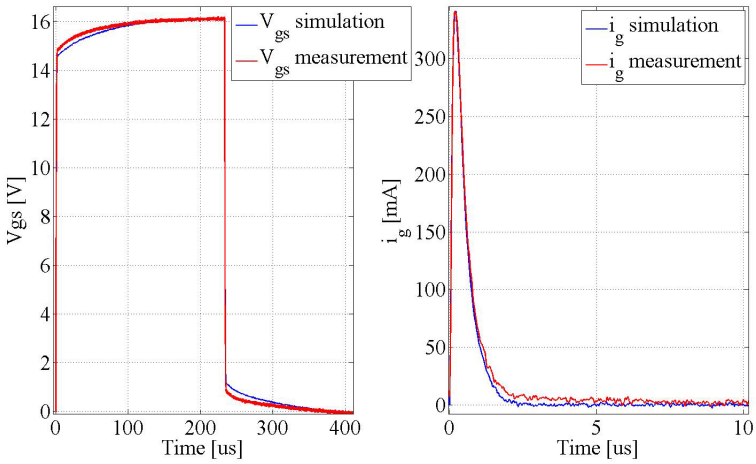


Fig. 4.2 Case2;Comparison between V_{gs} and i_g in simulation and measurement

It can be seen that the waveforms from simulation and measurement are in agreement with each other. Currents increase sharply and reaches their maximum at the same time and voltages are similar except in some parts that they do not match which could be due to errors in the measurement.

4.3 Test set-up 3

The results for this test set-up (extra capacitors on MOSFET($C_{gs} = 68nf$ and $C_{gd} = 4.5nF$)) are shown in Fig. 4.3

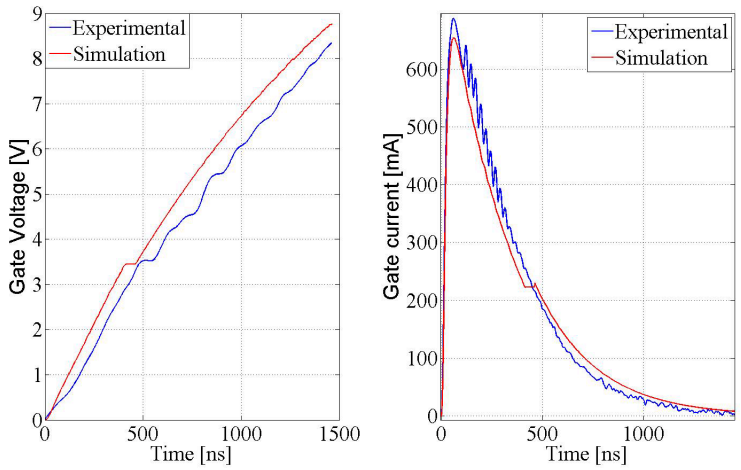


Fig. 4.3 Case3;MOSFET V_{gs} and i_g

The results from simulation and measurement show low discrepancies. Both voltages reach plateau level at the same time, although there is a mismatch between them. There is an oscillation on the gate current and this makes it difficult to observe the plateau level.

The delay time for the gate-source voltage to reach plateau level is 352ns and the rise time is 31ns. These times are based on the equations (2.3) and (2.4) respectively. The rate of changes in the drain current is $26\frac{A}{\mu s}$. MOSFET stray parasitics affect the rise time and currents and voltages. The voltage drop caused by the parasitics is 0.21V.

4.4 Test set-up 4

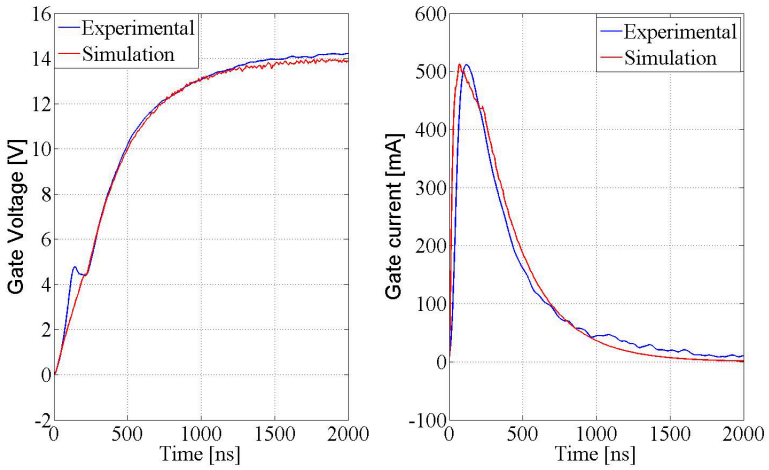


Fig. 4.4 Case4;MOSFET V_{gs} and i_g

Besides the differences at the beginning of the switching transient, results are in agreement with each other for the rest of the switching. The currents reach the maximum at the same time. But oscillations in the gate current cause the difference between the simulation and experimental results. The voltages also increase with different rate, but they reach the plateau level simultaneously and after that they increase with same speed.

Using (2.3) and (2.4) the delay time is 167ns and the current rise time is 33ns. The rate of changes in the drain current is $33\frac{A}{\mu s}$. The voltage drop caused by the stray parasitics of the MOSFET, is 163mV.

The voltage and current of the MOSFET's drain are depicted below for both experimental and simulation results. Waveforms confirm each other, except the oscillation in the experimental results that caused small differences.

The losses during turn-on were calculated for simulation and experimental, which were 21mW and 28mW respectively.

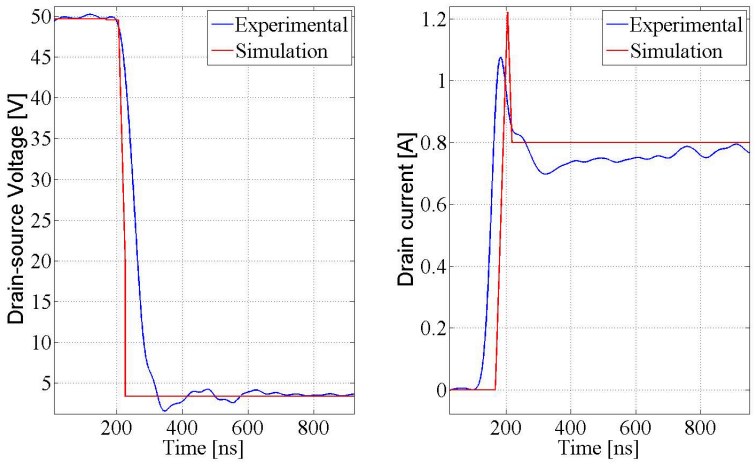


Fig. 4.5 Case4;MOSFET V_{gs} and i_g

During the turn-off the waveforms for drain voltage and current are observed and are shown in Fig. 4.6

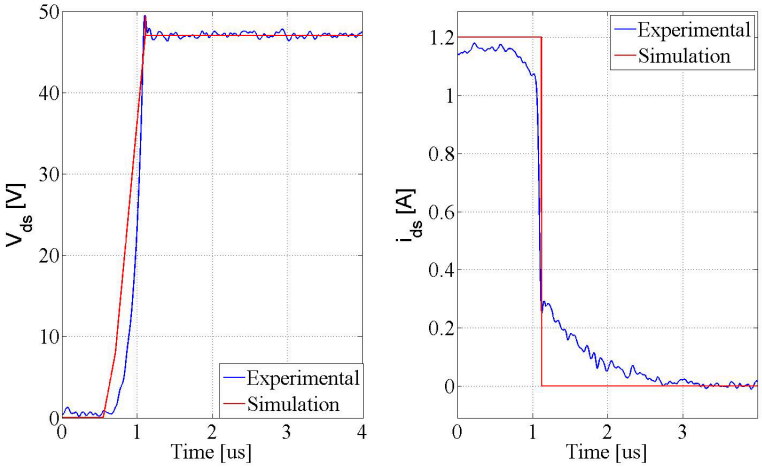


Fig. 4.6 Case4;MOSFET V_{gs} and i_g

The losses during the turn-off are 28mW for the simulation and 30mW for the experiment.

4.5 Simulation vs. Data-sheet

In this section a comparison between the simulation method and data-sheet values are performed. Certain test conditions are given for the values specified in the data-sheet, which are used in the simulation to be able to create a analogous comparison.

The test conditions are: $V_{ds} = 400V$, $I_{ds} = 44A$, $V_{gs} = 10V$ and $R_g = 3.3\Omega$. The parasitic capacitances mentioned in the data-sheet were $C_{iss_{V_{ds}=100V}} = 6800pF$ and $C_{rss_{V_{ds}=100V}} = 5pF$. Furthermore the delay time and rise time are 30ns and 20ns for the mentioned test condition given in the data-sheet. Besides the internal parasitics of the COOLMOS for drain and source are 5nH and 3nH respectively [12].

The delay time and rise time based on mentioned test condition are t_d=8nS and t_r=5nS.

There is a huge difference between the given time values and simulation results. As was mentioned before many factors are involved in the switching transients. The reason for this mismatch could be the differences in these factors. For instance the effect of inherent capacitors on the switching are considered. C_{iss} at low and high values of V_{ds} are increased to 20nF higher and it is observed that at higher values of these capacitors, longer delay and rise times achieved.

Moreover $\frac{di}{dt}$ is 1.85$\frac{A}{ns}$ and V_l=14.83V. In Fig. 4.7 the turn-on waveforms are depicted

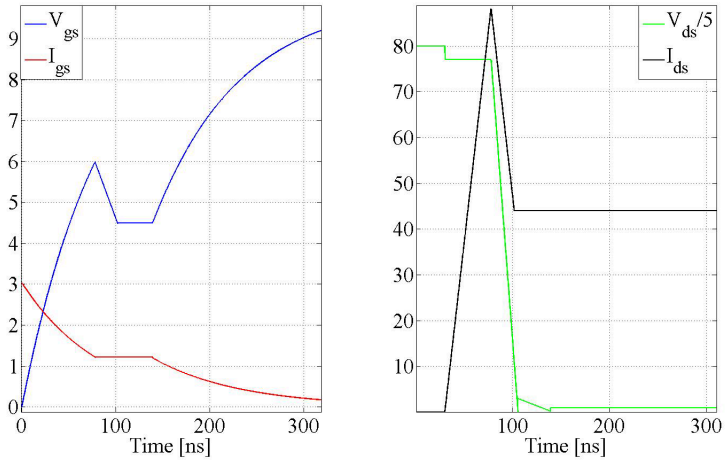


Fig. 4.7 Turn-on waveforms

During turn-off delay time and current fall time are 100ns and 10ns respectively based on the data-sheet information. However the results with the given data are different($t_d = 3.1ns$, t_{fi}=5.8ns). Therefore by changing the value of the capacitors to $C_{iss_{V_{ds}=400}} = 12nF$ and $C_{iss_{V_{ds}=Vds_{on}}} = 32nF$ the desired times are achieved. The overvoltage caused by the parasitics are 35V followed by the current changes $\frac{di}{dt}$=4.56$\frac{A}{ns}$.

In Fig. 4.8 the turn-off waveforms are shown.

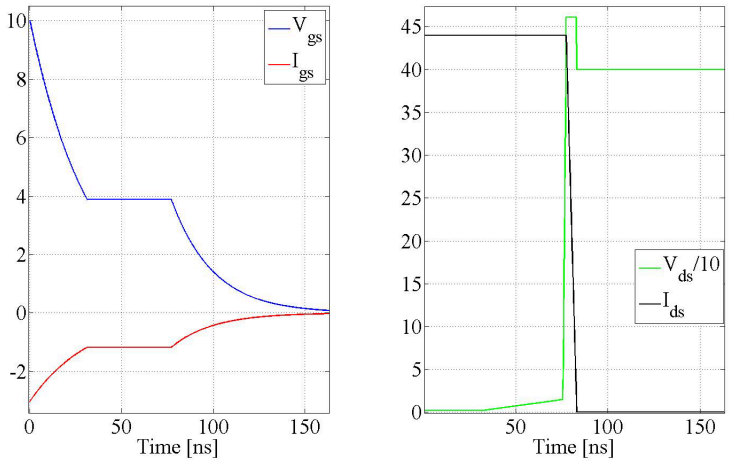


Fig. 4.8 Turn-off waveforms

Chapter 5

Conclusions

5.1 Results from present work

The main goal of this thesis was to model a MOSFET in MATLAB/Simulink. Moreover investigations on its gate drive were performed. Results from the experiments and simulations were compared and finally switching losses were calculated.

In order to study the performance of the gate drive two case set-ups were considered.Therfore the gate drive was used to switch a RC circuit for different component values. The results for these two cases showed that the devices in the gate drive influence the waveforms in different ways. The BJTs causes a delay in the gate voltage, as well as a voltage drop in gate voltage and gate current. Besides diodes D4 and D5 cause constant voltage drop in the gate voltage. Therefore a lower and slower gate current is injecting to the MOSFET. Gate voltage from the experimental results was used in the simulation for making a comparable case . The results were satisfactory for both cases.

Afterwards the drive was used to switch a COOLMOS in a phase leg. Instead of MOSFET, a freewheeling diode with suitable reverse recovery capabilities was used in the bottom switch. Two test set-ups were studied. In the first one two capacitors were attached to the gate of the switch to overrule the inherent capacitances of the MOSFET and slow down the switching transientswith. The second one was switching the MOSFET considering its own internal capacitors. For these tests satisfactory results were achieved, comparison of the simulation and experimental results proved the accuracy of the model. Furthermore the switching losses were calculated for the last case which were presented in Table 5.1

Table 5.1: Switching losses during turn-on and turn off

Case set-up	E_{on} (mW)	E_{off} (mW)
Simulation	21	28
Measurement	28	30

In the final test set-up, datasheet information was used in the simulation model. Same test conditions mentioned in the datasheet were applied in the simulation test set-up. The results showed the internal capacitors of the MOSFET have substantial effect on the delay time, rise/fall time of the component.

5.2 Future work

The following topics regarding this thesis are proposed for future work:

- Due to relatively high voltage drop caused by the BJTs used in the gate drive, use of BJTs with better capabilities such as faster fall/rise times, lower voltage drops is suggested.

  It is suggested to propose a model for the inherent capacitors of the MOSFET to increase the overall accuracy of the model.

- Investigation of parasitic effects on the MOSFET's switching characteristics and gate drive performance for different test conditions.

Appendix A

MOSFET Datasheet

IPW60R045CP

CoolMOS™ Power Transistor

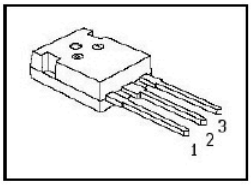
Features

- Worldwide best $R_{ds,on}$ in TO247
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

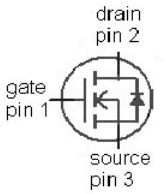
V_{DS} @ T_{jmax}	650	V
$R_{DS(on),max}$	0.045	Ω
$Q_{g,typ}$	150	nC

PG-TO247-3-1



CS CoolMOS is specially designed for:

- Hard switching SMPS topologies



Type	Package	Ordering Code	Marking
IPW60R045CP	PG-TO247-3-1	SP000067149	6R045

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	60	A
		T_C=100 °C	38	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	230	
Avalanche energy, single pulse	E_{AS}	I_D=11 A, V_{DD}=50 V	1950	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=11 A, V_{DD}=50 V	3	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		11	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	431	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	T_C=25 °C	44	A
Diode pulse current[2)]	$I_{S,pulse}$		230	
Reverse diode dv/dt[4)]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.29	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=3 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C	-	-	10	µA
		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C	-	50	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=44 A, T_j=25 °C	-	0.04	0.045	Ω
		V_{GS}=10 V, I_D=44 A, T_j=150 °C	-	0.11	-	
Gate resistance	R_G	f=1 MHz, open drain	-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	6800	-	pF
Output capacitance	C_{oss}		-	320	-	
Effective output capacitance, energy related[5]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 480 V	-	310	-	
Effective output capacitance, time related[6]	$C_{o(tr)}$		-	820	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=44 A, R_G=3.3 Ω	-	30	-	ns
Rise time	t_r		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	100	-	
Fall time	t_f		-	10	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=44 A, V_{GS}=0 to 10 V	-	34	-	nC
Gate to drain charge	Q_{gd}		-	51	-	
Gate charge total	Q_g		-	150	190	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=44 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	600	-	ns
Reverse recovery charge	Q_{rr}		-	17	-	µC
Peak reverse recovery current	I_{rrm}		-	60	-	A

[1] J-STD20 and JESD22

[2] Pulse width t_p limited by $T_{j,max}$

[3] Repetitive avalanche causes additional power losses that can be calculated as P_{AV}=E_{AR}*f.

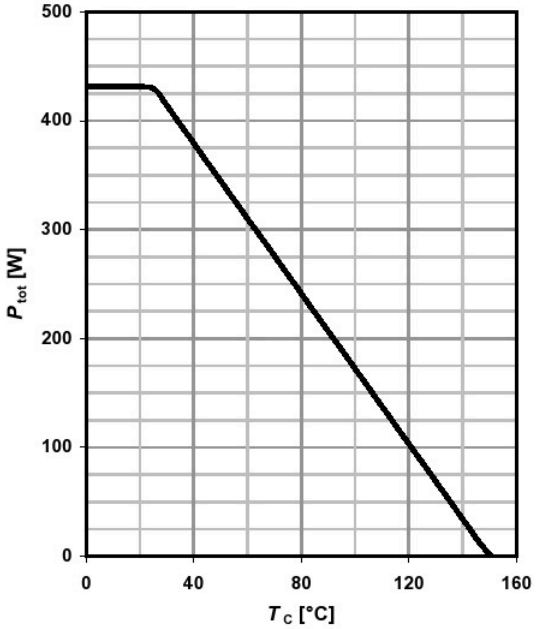
[4] I_{SD}<=I_D, di/dt<=100A/µs,V_{DClink} = 400V, Vpeak<$V_{(BR)DSS}$, T_j<T_{jmax}, identical low side and high side switch

[5] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

1 Power dissipation

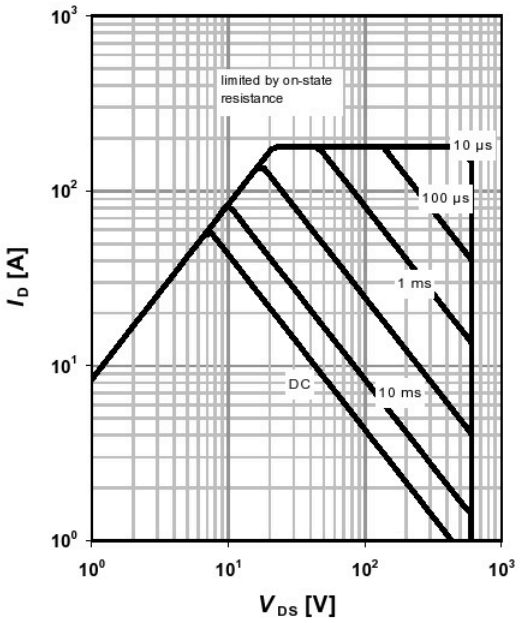
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

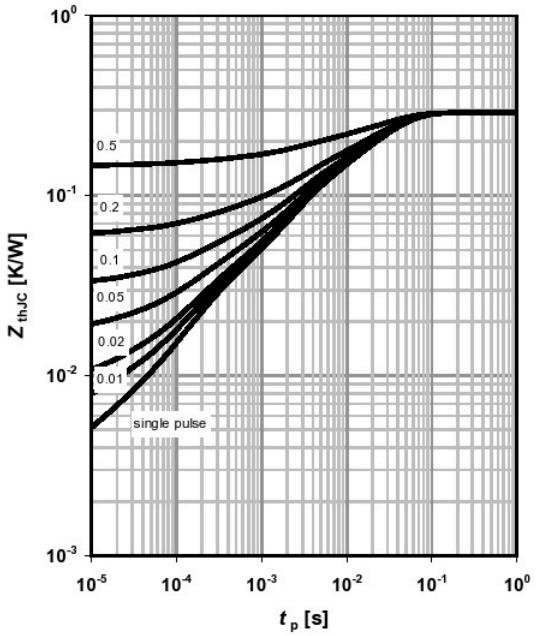
parameter: t_p



3 Max. transient thermal impedance

$Z_{(thJC)}=f(t_p)$

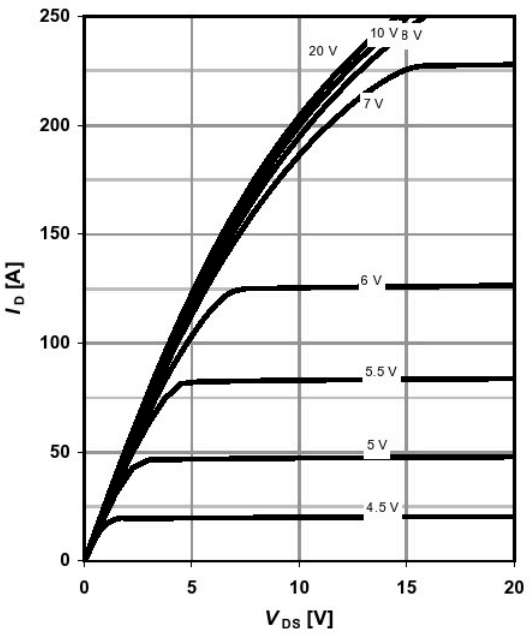
parameter: $D=t_p/T$



4 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

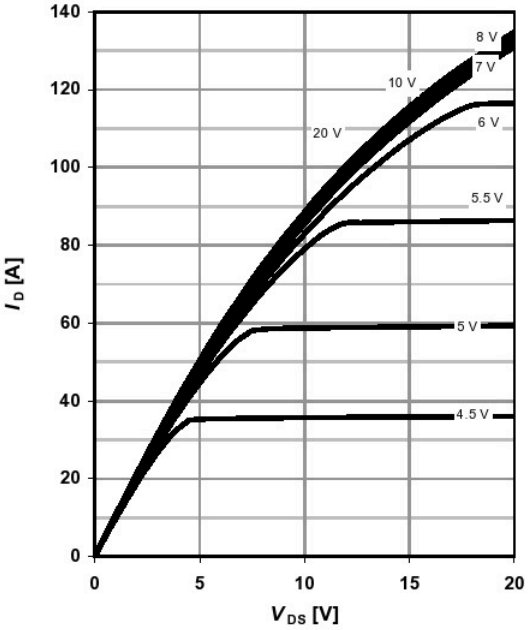
parameter: V_{GS}



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=150 °C

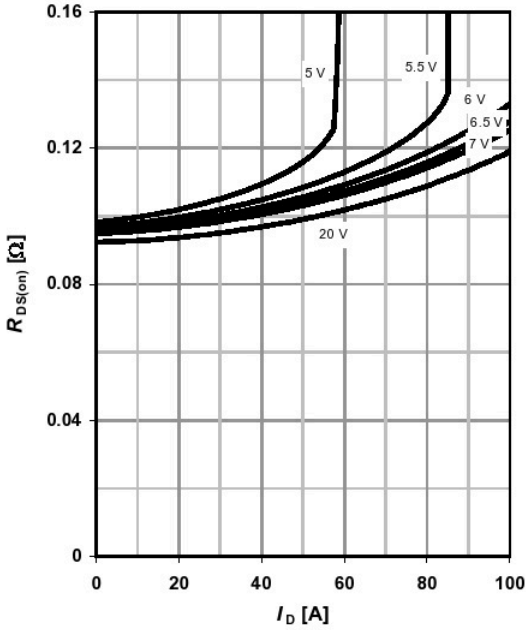
parameter: V_{GS}



6 Typ. drain-source on-state resistance

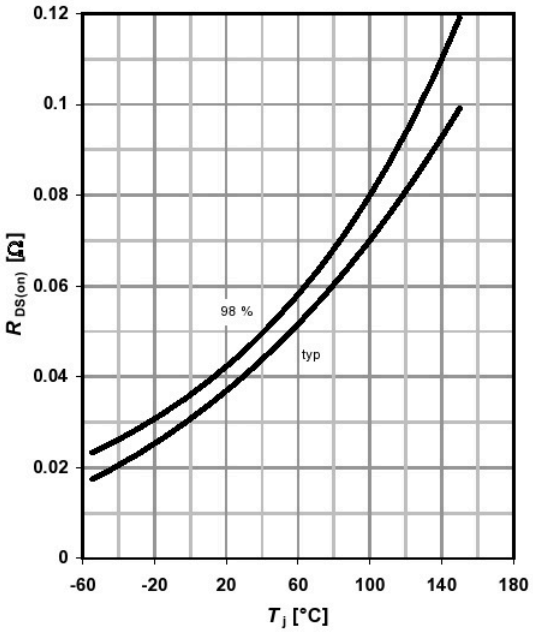
$R_{DS(on)}$=f(I_D); T_j=150 °C

parameter: V_{GS}



7 Drain-source on-state resistance

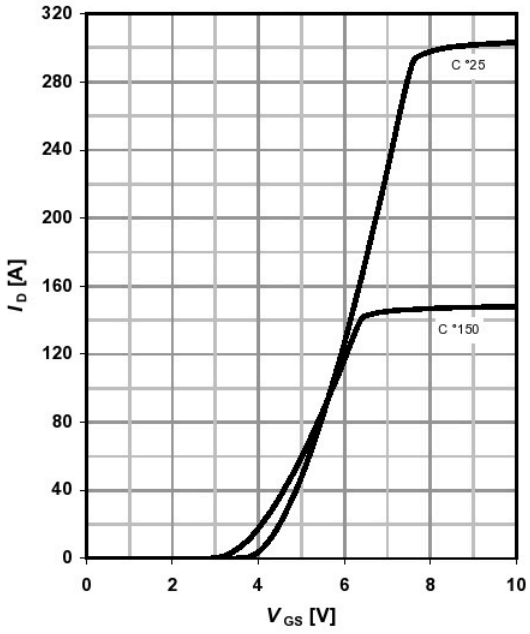
$R_{DS(on)}$=f(T_j); I_D=44 A; V_{GS}=10 V



8 Typ. transfer characteristics

I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

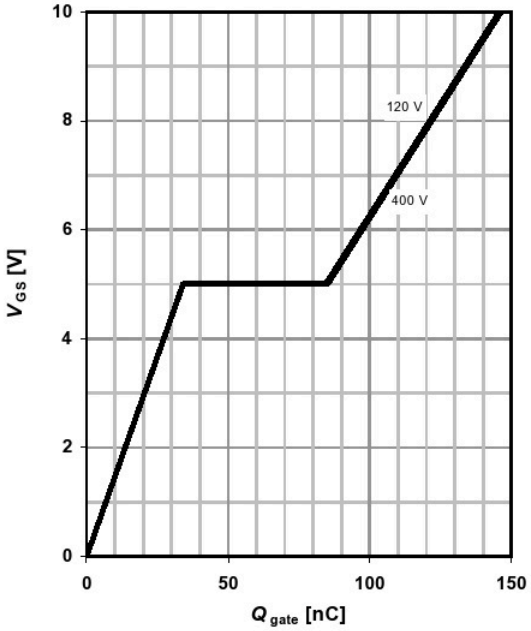
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=44 A pulsed

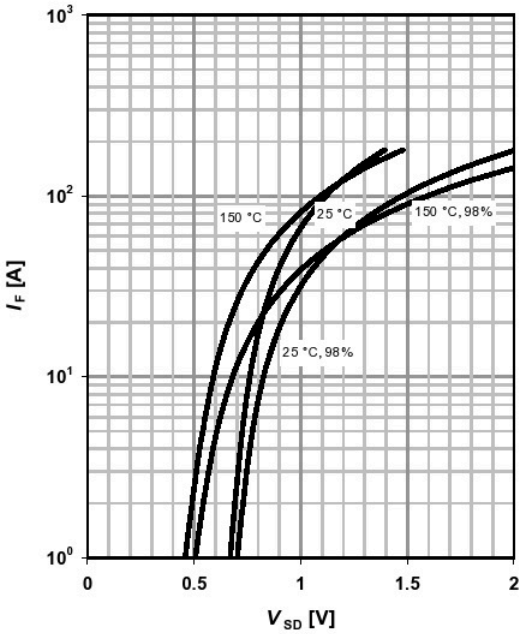
parameter: V_{DD}



10 Forward characteristics of reverse diode

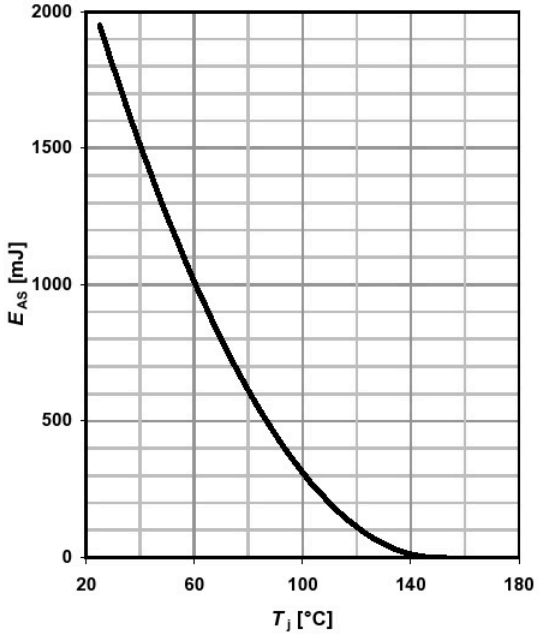
I_F=f(V_{SD})

parameter: T_j



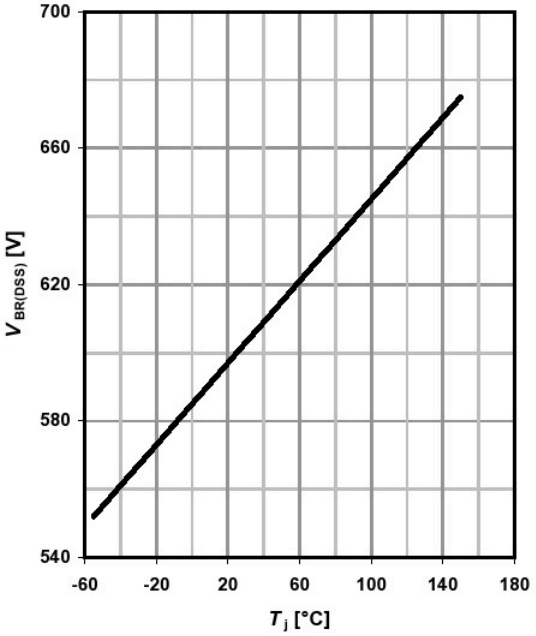
11 Avalanche energy

E_{AS}=f(T_j); I_D=11 A; V_{DD}=50 V



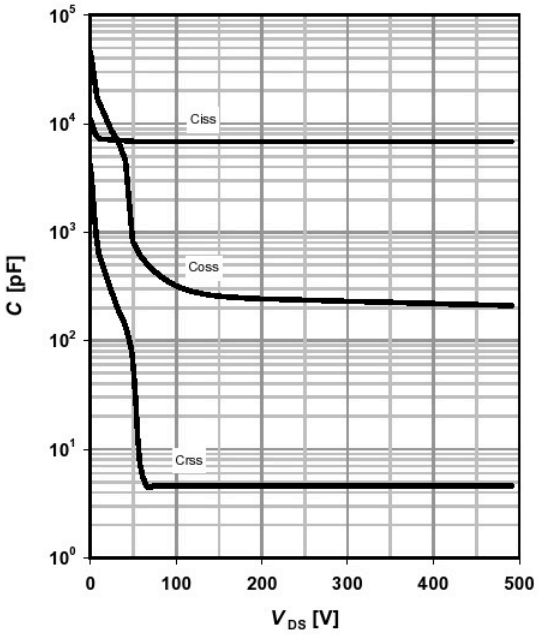
12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA



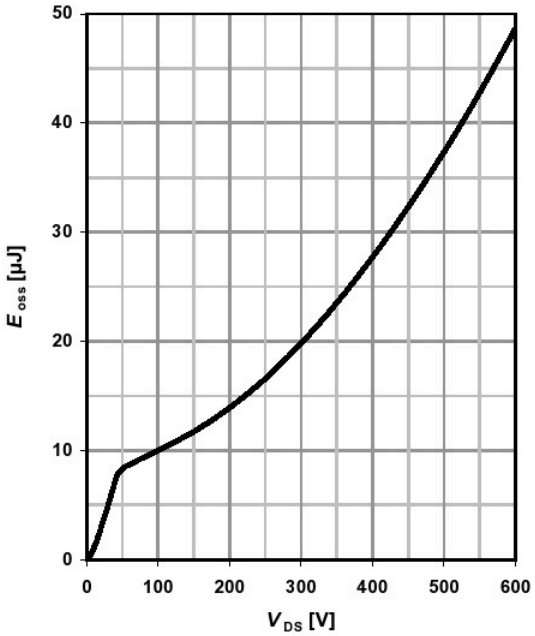
13 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

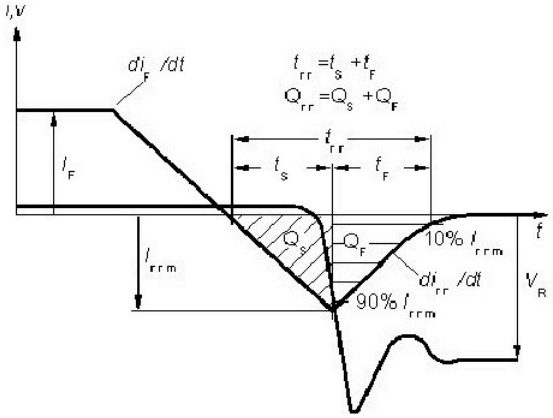


14 Typ. Coss stored energy

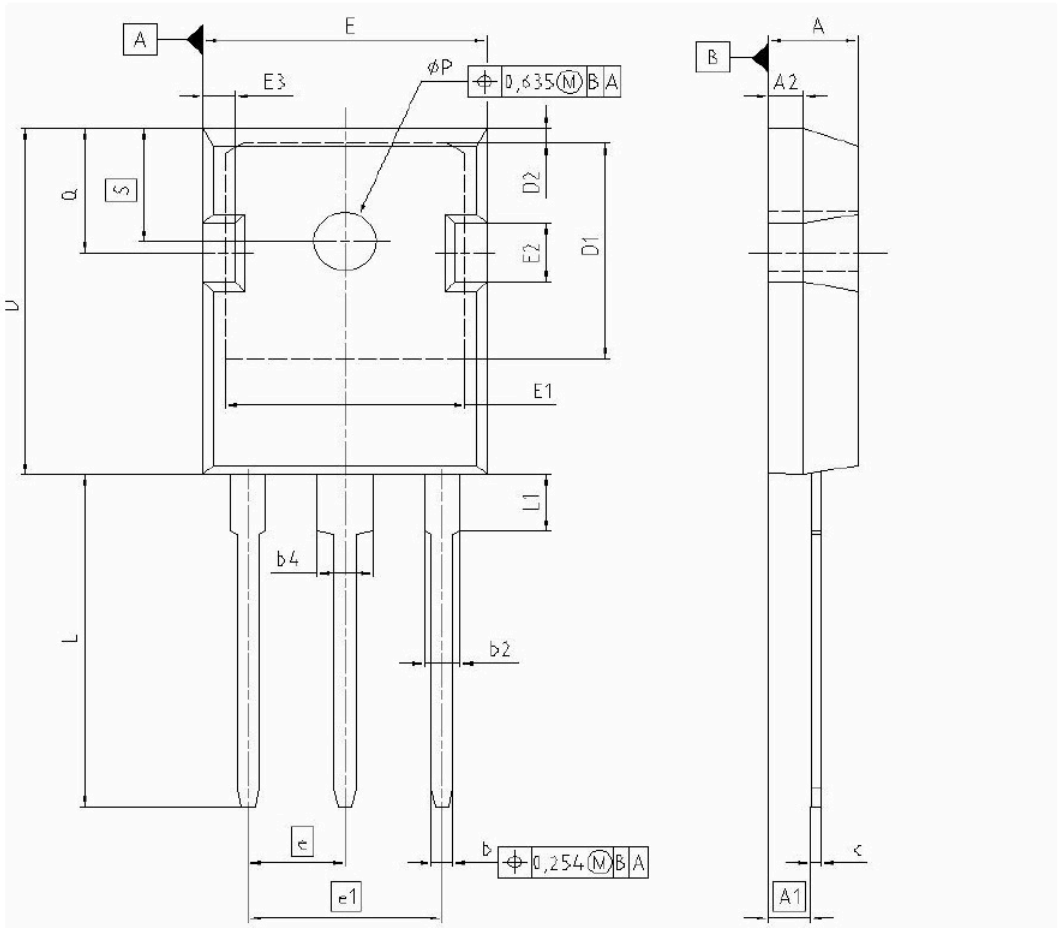
E_{oss}=f(V_{DS})



Definition of diode switching characteristics



PG-TO-247-3-1: Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.903	5.157	0.193	0.203
A1	2.273	2.527	0.092	0.096
A2	1.853	2.107	0.075	0.081
b	1.073	1.327	0.047	0.052
b2	1.903	2.386	0.075	0.094
b4	2.870	3.454	0.113	0.136
c	0.549	0.752	0.024	0.030
D	20.823	21.077	0.820	0.830
D1	17.323	17.831	0.682	0.702
D2	1.063	1.317	0.042	0.052
E	15.773	16.027	0.621	0.631
E1	13.893	14.147	0.547	0.557
E2	3.683	3.937	0.145	0.155
E3	1.683	1.937	0.066	0.076
e	5.450		0.215	
e1	10.900		0.430	
N	3		3	
L	20.053	20.307	0.789	0.799
L1	4.168	4.472	0.164	0.176
øP	3.559	3.661	0.140	0.144
Q	5.493	5.747	0.216	0.226
S	6.043	6.297	0.238	0.248

REFERENCE	JEDEC TO247-AD
SCALE	0 5 5 7.5mm
EUROPEAN PROJECTION	
ISSUE DATE	26-06-2005
FILE	TO247_1

Dimensions in mm/inches:

Published by
Infineon Technologies AG
81726 München, Germany

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