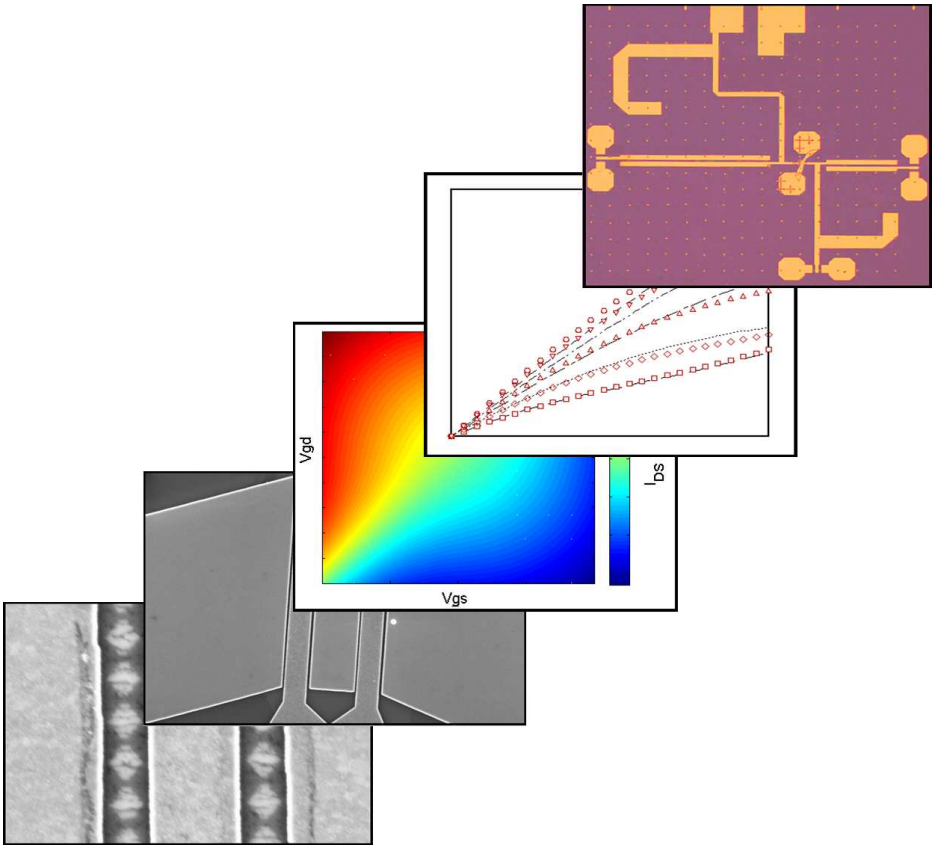

Graphene FETs in Microwave Applications

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Göteborg, Sweden 2012

Thesis for the degree of Doctor of Philosophy

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by

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ISBN 978-91-7385-777-2

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie Nr 3458
ISSN 0346-718X

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ISSN 1652-0769
Technical Report No. MC2-234

COVER: From left to right, a SEM image of graphene nanoconstrictions, a SEM image of a two-finger gate graphene FET, drain current versus intrinsic V_{gs} and V_{gd}, I-V output characteristic and an integrated subharmonic G-FET mixer.

Printed by Chalmers Reproservice
Göteborg, Sweden, November 2012

To my beloved family

Abstract

Graphene is a one-atom-thick sheet of carbon with numerous impressive properties. It is a promising material for future high-speed nanoelectronics due to its intrinsic superior carrier mobility and very high saturation velocity. These exceptional carrier transport properties suggest that graphene field effect transistors (G-FETs) can potentially outperform other FET technologies.

This doctoral thesis presents the realisation of G-FET circuits at microwave frequencies (0.3-30 GHz) with emphasis on a novel subharmonic resistive mixer. The work covers device manufacturing, modelling, circuit design, and characterisation.

The developed mixer exploits the G-FETs ability to conduct current in both n-channel and p-channel modes for subharmonic ($\times 2$) mixing. Consequently, the mixer operates with a single transistor and unlike the conventional subharmonic resistive FET mixers, it does not need any balun at the local oscillator (LO) port. In addition, the mixer has potential to operate unbiased. These aspects enable us to utilise G-FET subharmonic mixers in compact high frequency heterodyne detectors. A 30 GHz mixer is realised in microstrip technology on a 250 μm high resistivity silicon substrate. A conversion loss (CL) of 19 $\pm$ 1 dB in the frequency range of 24 to 31 GHz is obtained with an LO to RF isolation better than 20 dB.

For designing and analysing G-FET circuits a closed-form semiempirical large-signal model is proposed and experimentally verified under both DC and RF operation. The model is implemented in a standard Electronic Design Automation (EDA) software for device-circuit co-design. By using the model, the first G-FET microwave amplifier is realised. The amplifier exhibits a small-signal power gain of 10 dB at 1 GHz.

Keywords : Graphene, microwave FETs, microwave amplifiers, subharmonic resistive mixers, device modelling, device fabrication, S-parameters characterisation, harmonic balance analysis, integrated circuits, MMIC.

LIST OF APPENDED PAPERS

The thesis is based on the following papers:

Paper A
O. Habibpour, J. Vukusic and J. Stake, "A Large Signal Graphene FET Model," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 968-975, 2012.

Paper B
O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Mobility improvement and microwave characterization of a graphene field effect transistor with silicon nitride gate dielectrics," *IEEE Electron Device Letters*, vol. 32, no. 7, pp. 871-873, 2011.

Paper C
O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland and J. Stake, "A subharmonic graphene FET mixer," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 71-73, 2012.

Paper D
M. A. Andersson, O. Habibpour, J. Vukusic and J. Stake, "10 dB small-signal graphene FET amplifier," *Electronics Letters*, vol. 48, no. 14, pp. 861-862, 2012.

Paper E
M. A. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Resistive Graphene FET Subharmonic Mixers: Noise and Linearity Assessment," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, 2012.

Paper F
O. Habibpour, J. Vukusic, and J. Stake, "A 30 GHz Integrated Subharmonic Mixer based on a Multi-Channel Graphene FET," submitted to *IEEE Transactions on Microwave Theory and Techniques*, 2012.

OTHER PAPERS

The following papers are not included in this thesis due to an overlap in content or a content going beyond the scope of this thesis.

1. M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "Noise Figure Characterization of a Subharmonic Graphene FET Mixer," in *IEEE MTT-S International Microwave Symposium Digest, IMS*, Montreal, Canada, 2012.

2. J. Stake, O. Habibpour, J. Vukusic and O. Engström, S. Cherednichenko, "Graphene Millimeter Wave Electronics," invited paper presented at *6th ESA Workshop on Millimetre-Wave Technology and Applications and 4th Global Symposium on Millimeter Waves*, Espoo, Finland, 2011.

3. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Investigation of harmonic generation in a suspended graphene," *GigaHertz Symposium*, Lund, Sweden, 2010.

4. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Odd harmonic generation in a suspended graphene at microwave frequency," *Proc. of the 34th WOCSDICE*, Seeheim/Darmstadt, Germany, 2010.

5. O. Habibpour, S. Cherednichenko, J. Vukusic and J. Stake, "Characterisation of Exfoliated Graphene," *Proc. of the 33 rd WOCSDICE*, Malaga, Spain, 2009.

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List of abbreviations

ADS	Advanced Design System
ALD	Atomic Layer Deposition
CVD	Chemical Vapour Deposition
CL	Conversion Loss
CNT	Carbon nano tube
CPW	Coplanar Waveguide
DOS	Density of state
EDA	Electronic Design Automation
FET	Field Effect Transistor
G-FET	Graphene Field Effect Transistor
GHz	Gigahertz (10^9 Hz)
HB	Harmonic Balance
h-BN	Hexagonal Boron Nitride
HEMT	High Electron Mobility Transistor
HFET	Heterojunction Field Effect Transistor
IF	Intermediate Frequency
IIP3	Input 3rd-order Intermodulation Point
IMD	Intermodulation Distortion
JFET	Junction Field Effect Transistor
LO	Local Oscilator
MESFET	Metal Semiconductor Field Effect Transistor
MISFET	Metal Insulator Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
RF	Radio Frequency
SiC	Silicon Carbide
THz	Terahertz (10^{12} Hz)

List of acronyms

f_T	Cutoff Frequency
f_{MAX}	Maximum frequency of oscillation
$\hbar$	Reduced Planck constant
k_B	Boltzmann's constant
L_g	Gate length
q	Electron charge
T	Absolute temperature
W_g	Gate width

CHAPTER

ONE

INTRODUCTION

Carbon-based electronics offer a number of exciting properties [1] and may be considered as a complement to or extension of the existing silicon based electronics. Diamond, carbon nanotube (CNT) and a two-dimensional sheet of carbon atoms (graphene) are promising allotropes of carbon for use in high frequency electronics. Diamond is a wide band gap semiconductor with an excellent thermal conductivity [2]. Hence, diamond is nominated as a material candidate for future high-power devices [3]. On the other hand, CNT and graphene are attractive materials for high-speed nanoelectronics due to their ultra high carrier mobilities [4]. The primary advantage of graphene over CNT is its planar 2D structure that enables device and circuit design with standard processing techniques. In addition, due to the limited interface area between CNTs and metal contacts, CNTs show very high contact resistances which requires a large number of aligned CNTs for practical applications. This research project deals with study and development of graphene based devices for future high speed nanoelectronics.

1.1 Background

1.1.1 Microwave FET

The development of Field Effect Transistor (FET) dates back to 1950s [5], but it took a long time before FETs were fast enough to be used at microwave frequencies. The first microwave FET was reported in 1967 using a GaAs metal-semiconductor FET (MESFET) with maximum frequency of oscillation, f_{MAX}, of 3 GHz. While the operating frequency of GaAs MESFETs is limited to $f < 50$ GHz, the advent of the GaAs high electron mobility transistor (HEMT) in 1980 [6] allowed higher frequency operation. Today the state-of-the-art InP HEMTs have a $f_{MAX} > 1$ THz [7] and a cut-of frequency, f_T, of 628 GHz [8]. In addition, aggressive gate length down-scaling has improved the RF performance of silicon metal oxide semiconductor FETs (Si MOSFETs) significantly and some of them have exceeded the performance of GaAs HEMTs [9, 10]. This is due to very short transit times that can be achieved

in deep submicron devices. However, Si MOSFETs are outperformed by InP HEMTs especially in terms of f_{MAX}. With the development and maturity of InP technology, the microwave device community is constantly looking for novel structures such as III-V nanowires [11] and new materials showing a higher electron speed as well as a lower effective mass. Graphene can be one of the materials of choice since it has a maximum carrier speed of $10^8\ cms^{-1}$ given by its energy-momentum band structure and an extreme low effective electron mass [12].

1.1.2 Graphene

Graphene was first studied theoretically long ago and it was inferred that a single layer graphene is not thermodynamically stable [13]. In 2004 for the first time, graphene was demonstrated experimentally [14]. Due to their work, the 2010 Nobel Prize in Physics was awarded jointly to Andre Geim and Konstantin Novoselov.

Since its discovery in 2004, graphene has been the subject of extensive research both theoretically and experimentally. Graphene has exceptional electrical and mechanical properties which identify it as a new material candidate for several applications including, stronger/stiffer components [15], low cost display screens in mobile devices [16], storing hydrogen for fuel cells [17], biosensors [18], ultracapacitors [19], photonics and optoelectronics [20], plasmonics [21, 22] and high frequency electronics [23, 24].

Single-layer graphene can be produced by a mechanical exfoliation technique from natural graphite [14]. This method is still in use particularly for scientific purposes and proof of principle devices. A scalable method is to use chemical vapour deposition (CVD) process to grow graphene [25]. In this process a metallic substrate (Cu, Ni) is exposed to several precursor gases including a carbon-containing gas which is decomposed at high temperature. The CVD-grown graphene can be transferred to any insulating substrate, specially silicon, by etching the metallic substrate. In addition, large area graphene can be formed by the sublimation of silicon carbide (SiC) [26]. In this method SiC is heated to high temperatures in vacuum in order to decompose silicon atoms and form multilayered graphene in general. The quality of the graphene produced by these two latter methods is currently sufficient for applications like display screens. However, for other applications such as high frequency electronics, the quality of grown graphene needs to be enhanced.

1.2 Motivation

Applications such as very high-speed data communications [27] and THz imaging systems [28] are now emerging. Since the performance of silicon circuits are inferior to HEMTs, sub-THz systems are mainly implemented in III-V technologies. However, having a silicon compatible technology allows for a higher level of integration.

Graphene is compatible with silicon technology. In addition, the unique transport properties of graphene, given by its band structure, opens new niches for high speed nanoscale electronics. Due to the massless nature of carriers, electron and hole

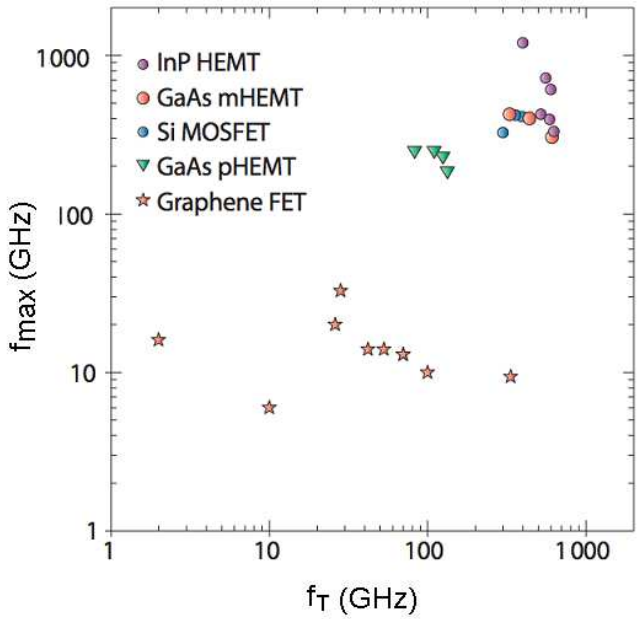

Figure 1.1: Intrinsic performance of the demonstrated G-FETs, where both f_{MAX} and f_T are available, versus mature CMOS and HEMT technologies [35].

mobilities in graphene exceed 200,000 cm^2/Vs at a few degrees Kelvin [29] and exceed 100,000 cm^2/Vs at near-room temperature [30]. These values of Hall mobility, are the highest reported for any material and therefore graphene has potential for room-temperature operation in the THz frequency range (0.3-3 THz). In addition, carriers in graphene exhibit very high drift velocities ($4 \times 10^7 cm/s$) at high fields [31, 32]. Finally, graphene has an excellent thermal conductivity of 5000 W/mK [33] and a high critical current density of 2×10^8 A/cm^2 [34]. These properties suggest that graphene has potential for high current density operation.

Realisation of high performance graphene field effect transistors (G-FETs) is the main step towards graphene high frequency circuits. This purpose requires overcoming several challenges. To begin with, the gate-dielectric formation process degrades the carrier mobility severely, $\sim$ 1000-3000 cm^2/Vs [36]. Although several methods have been developed to decrease this effect [37, 38], the carrier mobility of graphene in G-FETs is still far from its potential. Secondly, high contact and access resistances due to the high sheet resistivity of graphene can degrade the RF performance of G-FETs. The access resistance can be reduced by a self-aligned structure [39] and a contact resistance on the order of 200-500 $\Omega.\mu m$ at room temperature has been achieved [40]. However, this value should be reduced by about an order of magnitude in order to have high performance G-FETs. Thirdly, graphene is a zero band gap semiconductor. A small bandgap is required to have a pinch-off and enhance operational on-off ratios. To open a bandgap in graphene, quantum confinement can be used, e.g. patterning graphene in nano-scale structures [41, 42, 43]. Finally, the transfer characteristic of G-FETs exhibits hysteresis. The hysteresis originates from charge traps at the graphene/dielectric interface [44, 45]. Hence, developing

high quality gate-dielectric is a significant step forward to reduce the hysteresis in the transfer characteristic.

Already, huge efforts have been undertaken to mitigate the above challenges and improve G-FET performance. As a result, waferscale G-FETs with intrinsic f_T more than 350 GHz ($L_g = 40$ nm) [46] and a G-FET from exfoliated graphene with intrinsic f_T more than 300 GHz ($L_g = 140$ nm) [47] have been presented. However, due to lack of current saturation in short gate length devices, the demonstrated transistors have low intrinsic f_{MAX}. In addition, because of the currently high levels of contact and access resistances, the extrinsic f_T and f_{MAX} are below 50 GHz and 30 GHz respectively. Fig. 1.1 shows the frequency performance of the presented intrinsic G-FETs compared with that of competing RF FETs (HEMT, Si MOSFET) [35]. The main reason for the low intrinsic f_T is the low carrier mobility, $\sim$ 1000-2000 cm^2/Vs, in the demonstrated short gate length G-FETs. However, as shown in [48] the intrinsic f_T of 1 THz is achievable by a 65 nm G-FET with a carrier mobility of 14,000 cm^2/Vs.

As a first step towards high frequency circuits based on G-FET technology, the current PhD thesis aims to realise G-FET circuits at microwave frequencies (0.3-30 GHz) by investigating and analysing appropriate fabrication process, device modelling and circuit design. This work covers the complete G-FET manufacturing process. In addition, for determining G-FETs behaviour based on their transport characteristics and parasitic elements, a large signal model is developed. The model is implemented in a conventional EDA software for device-circuit co-designing. It enables us to evaluate the effect of process uncertainty on the circuit performance as well. The main circuit developed and discussed in this thesis is a novel subharmonic resistive FET mixer benefitting from the unique electron-hole duality characteristic of graphene. In addition, the first G-FET small-signal amplifier is presented.

1.3 Thesis outline

The thesis starts with an introduction to graphene band structure followed by carrier density and transport properties of graphene. In chapter 3 different aspects of G-FETs, including gate capacitive networks, modelling, fabrication and characterisation, are presented. Chapter 4 reviews and analyses the demonstrated G-FET circuits with focus on a G-FET amplifier and subharmonic resistive mixers. In chapter 5 conclusions are made and a future outlook for G-FETs is discussed. Finally in chapter 6 a summary of appended papers and my contributions are given.

CHAPTER

TWO

GRAPHENE ELECTRONIC PROPERTIES

Electronic properties of a material mainly depend on its band structure. As an example, effective mass which has important effects on the transport properties derives from the band structure. This chapter first provides a brief background of the graphene band structure. It then continues with descriptions of the graphene 2D electron system, charge density, carrier mobility and saturation velocity which are important parameters for any high frequency device.

2.1 Band structure

Graphene is a single two-dimensional layer of carbon atoms forming a dense honeycomb crystal lattice as shown in Fig. 2.1 Using a tight-binding Hamiltonian to

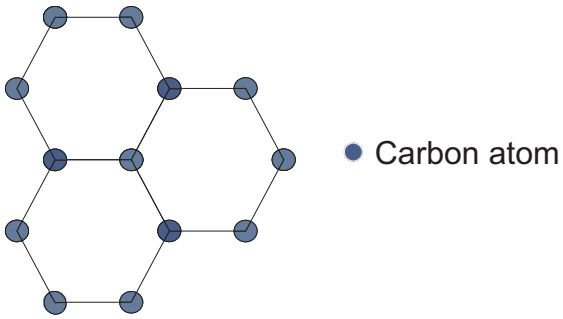

Figure 2.1: Graphene lattice structure.

model graphene electrons, thereby assuming that electrons can only hop to the nearest neighbour atoms, the energy band can be derived as [49].

$$E_{\pm}(\mathbf{k}) = \pm t\sqrt{3 + 2cos(\sqrt{3}k_y a) + 4cos(\frac{\sqrt{3}}{2}k_y a)cos(\frac{3}{2}k_x a)} \tag{2.1}$$

where t (2.8 eV) and a (1.42 Å) are the nearest neighbour hopping energy and the carbon-carbon distance respectively. In the above expression, the plus and minus

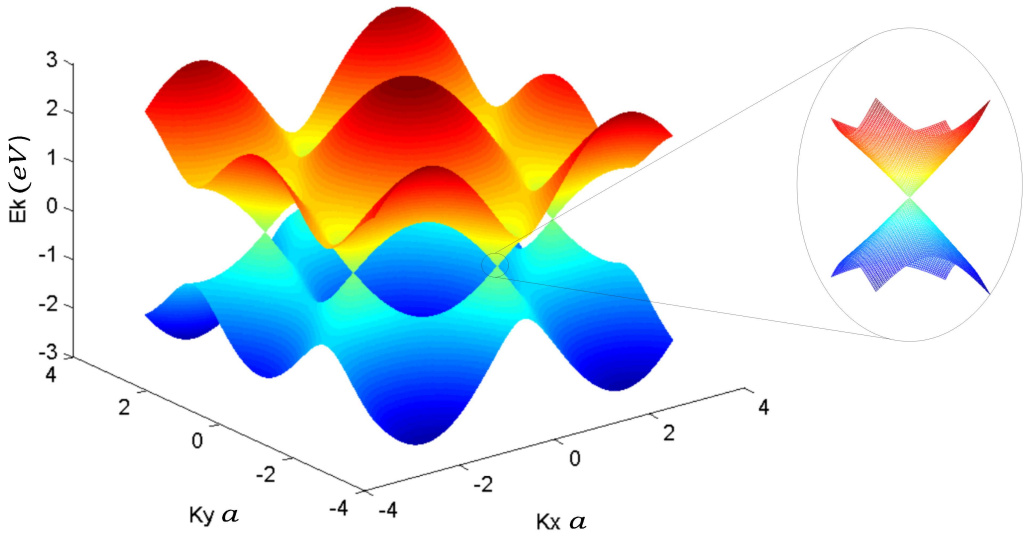

Figure 2.2: Left: Electronic dispersion in the honeycomb lattice, Right: lattice zoom in of the energy bands close to one of the Dirac points.

signs are applied to the upper (π) and lower (π^*) bands respectively. Fig. 2.2 shows the full band structure of graphene. As can be seen, the conduction and valence bands touch each other at singular points called Dirac points in the Brioullin zone. Thus graphene is a zero bandgap semiconductor (semi-metal). A zoom-in of the band structure close to the Dirac point is also shown in Fig. 2.2. In that range the dispersion is obtained as

$$E_{\pm}(\mathbf{K}) = \pm v_F|\mathbf{K}| \tag{2.2}$$

where $\boldsymbol{K}$ is the momentum measured relatively to the Dirac points and v_F is the Fermi velocity given by $v_F = 3ta/2\hbar \simeq 10^6$ m/s (1/300 of the speed of light). The positive sign in Eq. 2.2 represents energies in the conduction band, and the negative sign leads to energies in the valence band.

The linear energy-momentum relationship is the most important aspect of the energy dispersion of graphene. Due to the linear energy band diagram, electrons and holes behave like relativistic particles described by the Dirac equation, rather than the Schrödinger equation. Consequently, graphene exhibits electronic properties that are unique for a 2D gas of particles. For example, electrons behave as if they have no mass [12].

2.1.1 Bandgap engineering

A bandgap can be formed by confining graphene width in nanoribbon [41, 42] or nanoconstriction [43] structures. Nanoconstrictions create a band gap more effectively than nanoribbons. For example the induced bandgap by a 20 nm nanoribbon is about 50 meV [41, 42], while for a nanoconstriction with a 20 nm constriction

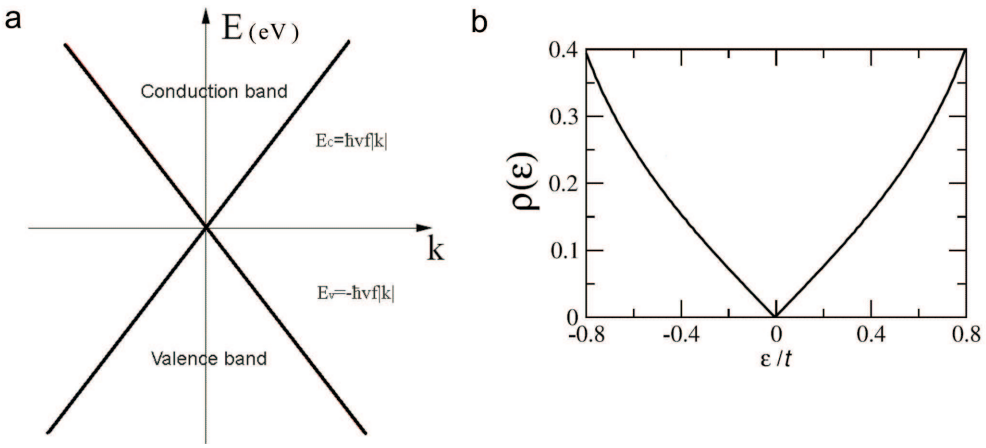

Figure 2.3: a) Energy dispersion model, b) Density of states versus energy [49].

width, it can be about 130 meV [43]. This is mainly attributed to the extra confinement in the longitudinal direction. In addition, in bilayer graphene a tunable band gap can be formed by applying a perpendicular electric field [50].

2.2 Two-dimensional electron system in graphene

Quantum mechanically, a system is defined to be 2D when its electronic wave function is a plane-wave in 2D while being a single quantised state in 3D. In other words, a system is considered 2D if

$$\lambda_F = \frac{2\pi}{k_F} > w \tag{2.3}$$

where λ_F is the Fermi wavelength and w could be the extent of a layer creating a potential well, as in 2D semiconductors, or just its thickness, as in graphene. For graphene, we have $\lambda_F \approx 35/\sqrt{\bar{n}}$ nm, where $\bar{n} = n/(10^{12} cm^{-2})$ [49], and since $w \approx 0.3$ nm (monolayer) the above condition is always satisfied, even for unphysically large $n = 10^{14} cm^{-2}$. Therefore, graphene is categorised as a 2D system. Note that in thin metal films it is impossible to have 2D electronic systems due to very high electron density of metals ($\lambda_F \approx 0.1$ nm).

2.3 Charge density and quantum capacitance

The energy dispersion model and the density of states (DOS) of graphene close to the Dirac point are depicted in Fig. 2.3. The density of states linearly depends on $|E|$ around the Dirac point and is given by [49]

$$\rho(E) = \frac{2|E|}{\pi(\hbar v_F)^2} \tag{2.4}$$

The electron and hole concentrations in a graphene sheet are given by the following expressions

$$n(E_f) = \int_0^\infty \rho(E) f(E - E_f) dE = N_g \mathfrak{F}(E_f/k_B T) \tag{2.5}$$

$$p(E_f) = \int_{-\infty}^0 \rho(E)(1 - f(E - E_f)) dE = N_g \mathfrak{F}(-E_f/k_B T) \tag{2.6}$$

Here, $f(E)$ is the Fermi-Dirac distribution function which describes the occupational probability of a state depending on its displacement in energy from the Fermi energy, E_f [51]. Further, N_g, the effective graphene density of states, is given by

$$N_g = \frac{2(k_B T)^2}{\pi(\hbar v_F)^2} \tag{2.7}$$

and $\mathfrak{F}$ is the complete Fermi-Dirac integral:

$$\mathfrak{F}(E_f/k_B T) = \int_0^\infty \frac{\eta}{1 + e^{\eta - E_f/k_B T}} d\eta \tag{2.8}$$

Fig. 2.4 shows the electron, n, and hole, p, concentration dependence on the Fermi level at room temperature. It can be seen that both electrons and holes contribute to the sheet charge density and depending on the Fermi level, the charge density of graphene can be dominated by either electrons or holes. The ability to switch between n-channel and p-channel modes is widely referred to as an *ambipolar* characteristic. However, as discussed in [52], this term does not explicitly describe the transport mechanism within graphene devices. For degenerate condition ($|E_f| \gg k_B T$) the channel carrier density can be found by $n_s \cong E_f^2/\pi(\hbar v_F)^2$. The type and the concentration of carriers in graphene can be controlled by the introduction of metals or molecules on the graphene surface. This process is mostly referred to as *graphene doping* [53, 54]. However, it should be noted that the process, e.g. chemical doping, does not involve substituting carbon atoms with any impurities (dopants).

In connection to the DOS, the quantum capacitance was first introduced in [55] to describe the 2D-electronic systems in silicon surfaces and GaAs junctions. This quantum capacitance was defined through standard DOS in the solids as

$$C_Q = q^2 \rho(E_f) \tag{2.9}$$

Graphene quantum capacitance, $C_{Q,G}$ can be calculated by means of Eq. 2.5 and Eq. 2.6. The total charge density in graphene is

$$Q_s(E_f) = -q(n(E_f) - n(-E_f)) = qN_g(\mathfrak{F}(E_f/k_B T) - \mathfrak{F}(-E_f/k_B T)) \tag{2.10}$$

and therefore

$$C_{Q,G}(E_f) = -\frac{d(Q_s)}{d(E_f/q)} = \frac{2}{\pi}\frac{q^2 K_B T}{(\hbar v_F)^2} ln(2 + 2cosh(E_f/k_B T)) \tag{2.11}$$

As can be seen for degenerate condition $|E_f| \gg k_B T$, $C_{Q,G} \cong 2q^2|E_f|/\pi(\hbar v_F)^2$ which obeys Eq. 2.9.

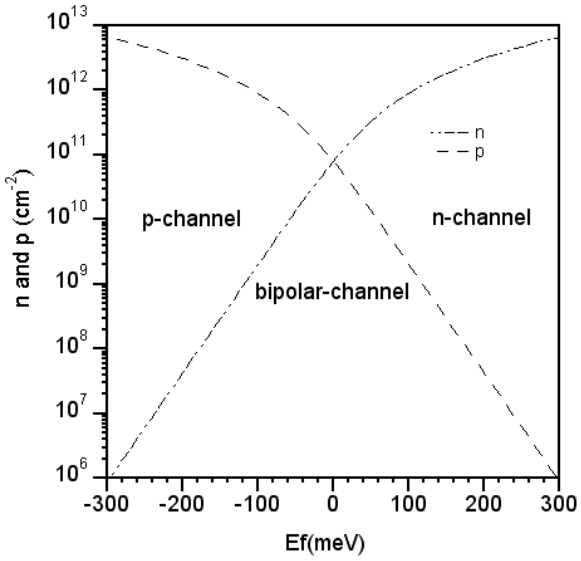

Figure 2.4: Electron concentration (n) and hole concentration (p) versus Fermi level at room temperature.

2.3.1 Residual carrier density

From Fig. 2.4 it is seen that due to the electron-hole duality in graphene, its minimum carrier density is attained at $E_f = 0$ and it is expected to be equal to the thermally generated carriers, $n_{th} = 8 \times 10^{10}\ cm^{-2}$ at room temperature. However, measured graphene minimum carrier density lies typically in the range of 10^{11}-10^{12} cm^{-2}. Hence an additional parameter which is usually referred to as the residual carrier density, n_0, is needed in order to explain this phenomenon at the Dirac point [56]. Due to potential fluctuation caused by the charged oxide defects and impurities, a graphene film at the charge neutrality point breaks into electron and hole *puddles* [57]. This phenomenon will be discussed more in Sec. 3.1. The electron and hole puddles are capable of significantly increasing the minimum carrier density [56] as well as the minimum quantum capacitance [58].

2.4 Carrier transport

The response of the free carriers to an external electric field, E, in steady state is represented by the carrier velocity versus electric field relationship. For sufficiently low fields the velocity-field relation is linear

$$v_{drift} = \mu E \tag{2.12}$$

with μ being the carrier mobility in units of cm^2/Vs. The carrier mobility can be obtained as

$$\mu = q\tau/m^* \tag{2.13}$$

where m^* is the effective mass and τ represents the average scattering time [59]. In table 2.1 mobilities for electrons and holes for a number of semiconductors as well as

Table 2.1: Properties of graphene compared with conventional semiconductors at T = 300 K and low carrier densities [2]

Semiconductor	Si	C	$Graphene$	GaN	$GaAs$	$InAs$	$InSb$
Electron effective mass (m^*/m_e)	0.98	1.4	0 *	0.19	0.067	0.023	0.013
$\mu_e(cm^2/Vs)$ at low doping	1200	1800	100000	1600	8000	33000	77000
$\mu_h(cm^2/Vs)$ at low doping	460	1200	100000	200	400	460	850
Bandgap (eV)	1.11	5.5	0	3.4	1.43	0.36	0.18
Saturation velocity ($10^7 cms^{-1}$)	1	2.7	4	1.1	1.2	3.5	5
Thermal conductivity (W/m-K)	130	2000	5000	110	55	27	18

*Ideal graphene, Dirac point

graphene are shown. These results are given for pure materials and are only limited by phonon scattering.

As the external field is increased, the simple expression of 2.12 does not hold and the carrier velocity versus electric field relationship is calculated by Monte Carlo simulations. However, for device simulations the following empirical relation can be used

$$v_{drift} = \frac{\mu E}{\sqrt[n]{1 + (\frac{\mu |E|}{v_{sat}})^n}} \tag{2.14}$$

with n being a fitting parameter and v_{sat} is a temperature-dependent saturation velocity [59].

The above discussion is valid when the electrons have sufficient time to undergo several collisions before reaching steady state. This usually needs a few picoseconds or a transit distance of $\geq$ 100 nm. If the transit distance becomes smaller than the mean free path the electrons move ballistically, without scattering. Transport in this region is not described by the usual carrier velocity versus electric field relationship. This region of transport is specified by the transient velocity-field curves [60].

2.4.1 Carrier mobility in graphene

It is both experimentally [29] and theoretically [61] shown that free standing graphene has the highest carrier mobility among all semiconductors. This is due to the very low effective mass (table 2.1). In suspended mode (Fig. 2.5), the carrier mobility is mainly limited by the acoustic phonon scattering of the graphene lattice [61] and it is referred to as the intrinsic carrier mobility. Due to the dependency of the carrier scattering on the acoustic phonons, the carrier mobility decreases linearly with increasing temperature. Nevertheless, near-room temperature (T = 240 K) it is still more than 100,000 cm^2/Vs and a mean free path of $\approx 1\ \mu m$ is obtained [30].

As soon as graphene is put in contact with/sandwiched between materials (e.g. substrate and gate dielectric) its intrinsic mobility severely degrades. This is due to scattering caused by either charged impurities located near graphene interfaces, so called Coulomb scattering [63, 64] or by surface optical phonons of the adjacent materials [65, 66]. At low temperatures (T < 300 K), depending on the impurity level, the scattering is dominated either by remote surface phonon scattering [67] or by Coulomb scattering [37]. In the latter case, the carrier mobility is constant at low

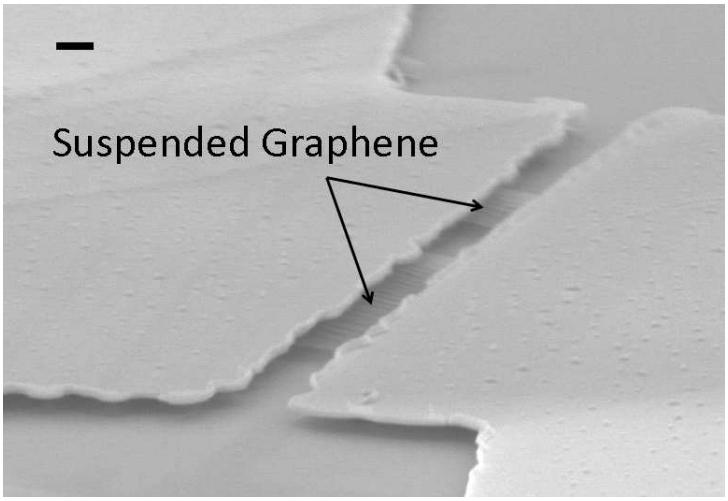

Figure 2.5: A SEM image of a suspended graphene film, scale bar 1 μm [62].

temperatures. However, at high temperatures the remote surface phonon scattering becomes dominant and the carrier mobility decays with increasing temperature [66].

It is theoretically shown that a high-κ dielectric can screen the charged impurities [65]. However, high-κ dielectrics generally have low surface phonon energies which can couple with electrons. In this case, only the scattering mechanism switches to phonon-electron scattering. Planar h-BN is another candidate which has been explored to obtain a high room temperature mobility of 10,000-40,000 cm^2/Vs [68, 69]. This is due to the strong in-plane ionic bonding which makes h-BN relatively inert and is expected to be free of surface charge traps as well as having a high surface phonon energy (100 meV). In summary, the extrinsic carrier mobility of graphene varies from few thousands [37, 70] to tens of thousands cm^2/Vs [71, 68, 69] and the mean free path which strongly depends on the carrier density typically ranges between 10-500 nm [72].

Moreover, unlike the conventional semiconductors, the electron and hole mobilities in graphene are very close to each other, see table 2.1. In suspended graphene they are equal [29] while in substrate supported graphene, due to the different type of impurities, they are within the same orders [70, 37].

2.4.2 Carrier saturation velocity in graphene

At high fields the saturation velocity becomes an important measure of the carrier transport. Figure 2.6 depicts the electron velocity versus the electric field for conventional semiconductors and simulated curves for large-area graphene having different deformation fields and potentials [73]. It is seen that the velocity saturation starts at relatively low electric fields due to the high carrier mobility in graphene. The saturation velocity is mainly limited by the optical phonon scattering of the substrate, and it has been shown that within sufficient accuracy this scattering phenomenon can be described by a single phonon energy ($\hbar\omega_{OP}$) [31]. Therefore, the saturation velocity depends on temperature as $1/(N_{OP}+1)$, where $N_{op} = 1/(exp(\hbar\omega_{OP}/k_BT) - 1)$ is

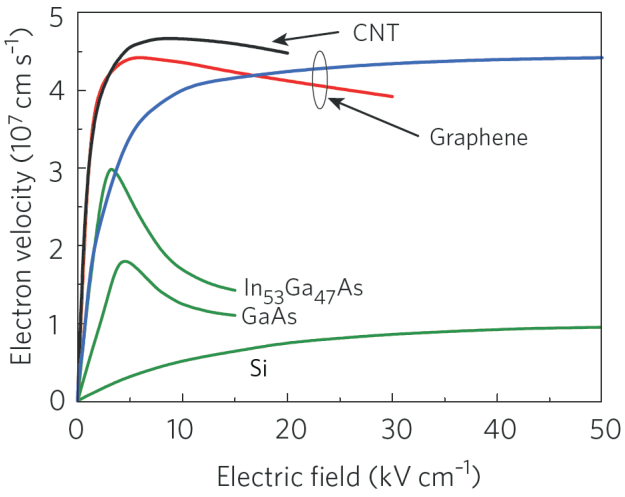

Figure 2.6: Electron drift velocity versus electric field [32].

the phonon occupation number [74].

CHAPTER

THREE

GRAPHENE FIELD EFFECT TRANSISTORS

This chapter introduces graphene field effect transistors (G-FETs). It discusses the physical structure of the metal-oxide-graphene stack which forms the heart of G-FETs. Finally, the device modelling, manufacturing and characterising are presented.

3.1 Field effect transistors

A field-effect transistor (FET) is a transistor that uses an electric field, induced capacitively via a gate voltage, to control the carrier density or the cross section area of the channel in order to alter the conductivity of its channel in between two electrodes, drain and source [5]. FETs are distinguished by the way the gate capacitor is formed [59]. In an insulated-gate FET, the gate capacitor is an insulator. In a metal semiconductor FET (MESFET) or a Junction FET (JFET), the capacitor is formed by a Schottky barrier or a depletion layer of a p-n junction, respectively. An insulating gate can be realised either by a dielectric layer in a metal oxide/insulator semiconductor FET (MOSFET/MISFET) or by a large bandgap semiconductor layer in a heterojunction FET (HFET) [6]. Moreover, FETs are unipolar and due to the higher electron mobility in traditional semiconductors (table 2.1) discrete FETs generally have n-type channels.

As it is shown in the previous chapter (Fig. 2.4), the carrier density of a graphene sheet can be controlled by changing its Fermi level. Hence graphene can be utilised as a channel in a MOSFET/MISFET structure. Fig. 3.1 shows the layer structures of graphene field effect transistors (G-FET) based on transferred graphene and sublimated SiC. Moreover, due to electron-hole duality in graphene, a G-FET can be operated as a p-type or n-type FET by only changing the gate voltage.

3.1.1 Metal-oxide-graphene structure

To understand the G-FET, the mechanism for controlling the carrier density of the channel has to be analysed. Importantly, the charge-control relation determining

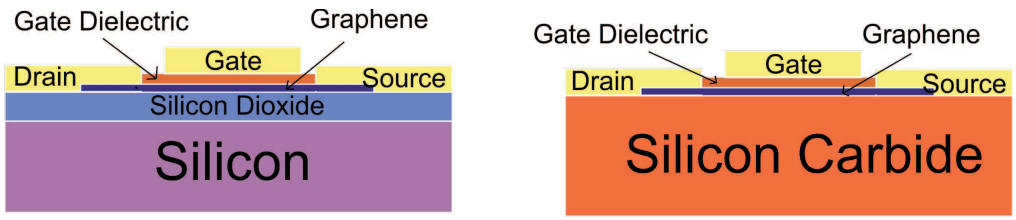

Figure 3.1: The layer structure of G-FETs based on, transferred graphene (left), and sublimation of SiC (right).

the channel charge density as a function of gate voltage should be obtained for the calculation of the drain-source current. As mentioned above, a G-FET is an insulated-gate FET. Among insulators, oxides are predominantly used as gate dielectrics and therefore metal-oxide-graphene structure plays an important role in G-FET technology. For example, as previously described, Coulomb scattering originating from charged impurities located near graphene/oxide interface can drastically degrade carrier mobility. In addition, the optical phonon scattering of gate oxides mainly determines the saturation velocity in G-FETs.

The energy-band diagram of a metal-oxide-graphene structure is shown in Fig. 3.2. In this structure drain and source are shorted. From electrostatics analysis, the total voltage drop, V_g, between the metal gate and the graphene layer can be written as

$$V_g = E_f/q + \Phi_{ms} - \frac{Q_s(E_f) + Q_f}{C_{ox}} \tag{3.1}$$

with Φ_{ms} being the difference in work function between the metal and the graphene layer. C_{ox} is the gate oxide capacitance and Q_f is the fixed charge sheet density representing any fixed charge near or at the graphene sheet/oxide interface. The term Φ_{ms} is just a voltage shift, so it can be embedded into the gate voltage. Fig. 3.3 shows E_f/q versus V_g with $C_{ox} = 0.25$ and $0.5\ \mu F cm^{-2}$ for ideal structure where $Q_f = 0$.

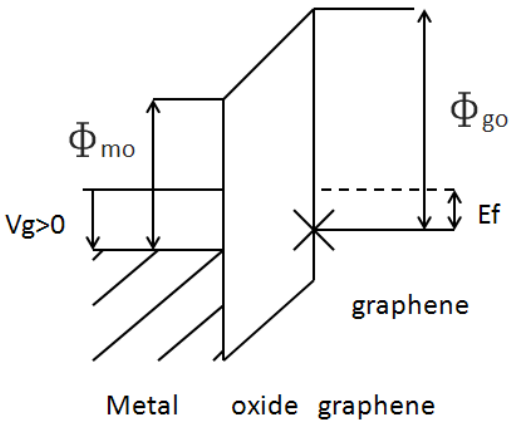

Figure 3.2: Band diagram of a metal-oxide-graphene structure.

In order to analyse the effect of Q_f, without losing generalisation, we assume it

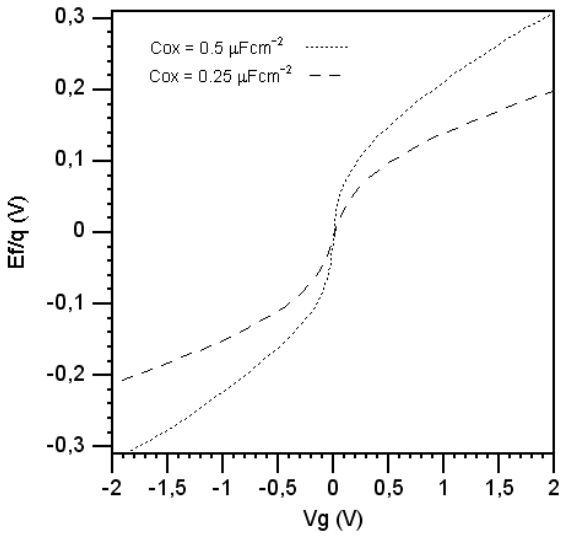

Figure 3.3: E_f/q versus gate voltage for an ideal metal-oxide-graphene contact with $C_{ox} = 0.25$ and 0.5 $\mu F cm^{-2}$.

has a distribution with a zero mean, since a nonzero mean only results in a gate voltage shift much the same as Φ_{ms}. The total voltage shift is generally referred to as the Dirac voltage, V_{dirac}.

Two extreme cases are examined. The first case $V_g \approx 0$

$$Q_f = \frac{E_f}{q} C_{ox} - Q_s(E_f); \tag{3.2}$$

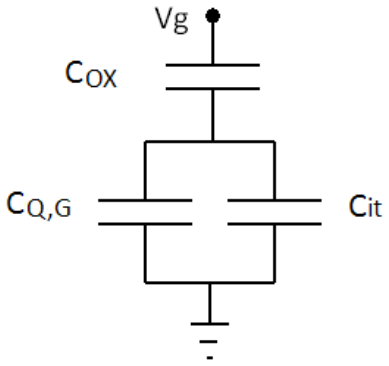

Figure 3.4: The metal-oxide-graphene capacitive network.

Although the average of Q_f is zero and the graphene sheet is neutral, the above equation shows that Q_f locally induces charges in the graphene sheet and creates electron or hole puddles [57]. These puddles increase the minimum conductance of a graphene sheet [56]. The above induced charge density differs from sample to sample, but it is mainly within $Q_0 = 4 - 12 \times 10^{-8}\ C/cm^2$. This corresponds to

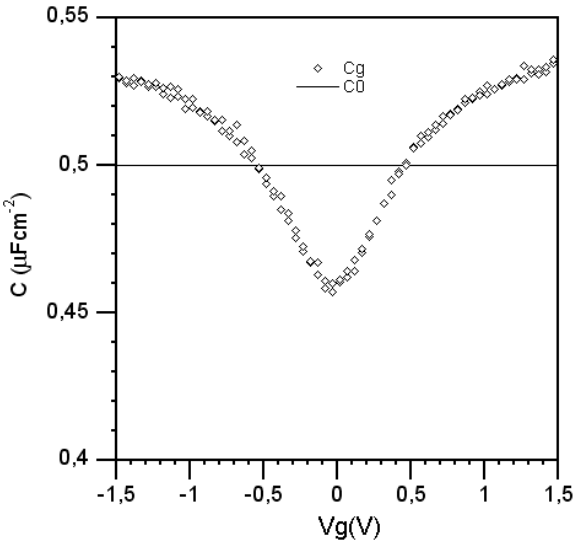

Figure 3.5: Measured CV for a metal-oxide-graphene capacitive network with 8 nm Al_2O_3 gate dielectric.

$\overline{|E_{f0}|} \approx 40 - 80$ meV, where $\overline{|E_{f0}|}$ is the mean value of $|\Delta E_f|$. Moreover, since $C_{Q,G}(E_f) = -dQ_s/d(E_f/q)$ the perturbation of E_f caused by Q_f can significantly increase the minimum $C_{Q,G}$ [58].

The second extreme case is where the potential drop on the graphene layer becomes very small, i.e. $V_g \gg E_f/q$. In this case the perturbation of E_f caused by Q_f can be ignored and therefore

$$-Q_s(E_f) = V_g C_{ox} \tag{3.3}$$

so in this region, the metal-oxide-graphene contact behaves like a simple capacitor.

The metal-oxide-graphene capacitive network is shown in Fig. 3.4. The interfacial trap capacitance, C_{it}, comes from the interfacial traps that can interact, via charge-discharge, with the channel. At microwave frequencies, traps do not have time to exchange charge so this term can be neglected. Moreover, as long as $C_{ox} \ll C_{Q,G}$, the variation of C_G ($C_{ox} \parallel C_{Q,G}$) can be ignored. The theoretical minimum value of $C_{Q,G}$ is about $1\mu Fcm^{-2}$ at room temperature. However, as described above, due to Q_f the minimum value is generally several times higher. So in many practical cases, except for ultra thin gate dielectrics, the above condition is valid. A typical C-V characteristic of G-FETs developed in this is shown in Fig. 3.5 It can be seen that by selecting the average value, C_0, the error will be less than 6%.

3.2 Device modelling

Device models can be divided in two major groups: physical models and empirical models. Physical models are based on first-principles describing the carrier transport. These models are imperative in the early stages of the device development

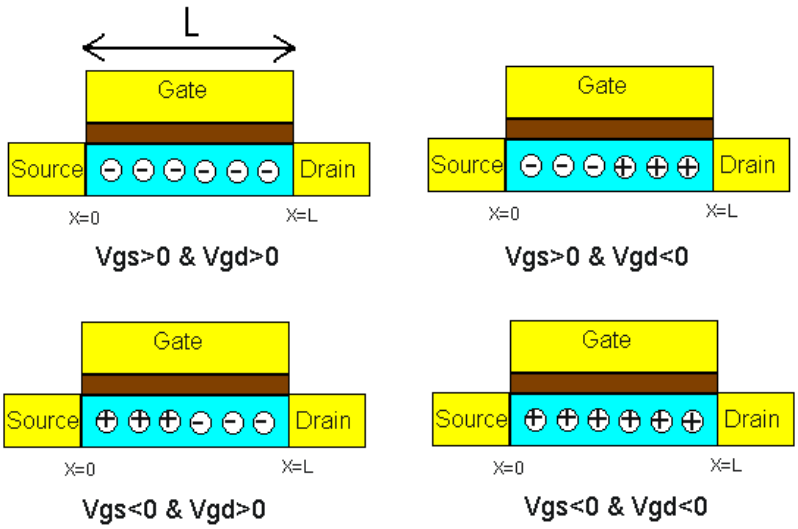

Figure 3.6: Carrier type in a G-FET channel at 4 different quadrants of the V_{gs}-V_{gd} plane.

and they can be used for process optimisation. Moreover, they give a better understanding of the physics behind the device behaviour. Several physical models for predicting the behaviour of G-FETs have been proposed [75, 76]. However, they are usually too complex for circuit modelling, i.e. they don't allow fast calculation and cannot be easily implemented in Electronic Design Automation (EDA) tools.

Empirical models, on the other hand, are based upon curve fitting in order to describe transistor operation and can provide acceptable accuracy. Although an empirical model needs preceding measurements on devices, it is still preferred for circuit simulation due to utilising simple equations which leads to fast and accurate enough simulations. For that reason, the large signal model is preferably of closed form and covers the entire operating range.

Due to the lack of a band gap and electron-hole duality characteristic in G-FETs, the conventional empirical FET models such as those proposed in [77, 78] are not applicable for G-FET modelling. A model based on a semiempirical square-root charge-voltage relation is presented in [31, 79]. In [80] an empirical charge-voltage relation in short-channel Si MOSFETs is utilised to model G-FETs. These models allow the calculation of I-V characteristics and the latter can distinguish between electron and hole charges. However, all developed models use the same carrier mobility for electrons and holes as well as the same contact resistance for p- and n-channels. Therefore the asymmetric behaviour of G-FETs [53, 81] cannot be predicted.

3.2.1 A symmetrical closed form G-FET model

As can be seen in Fig. 2.4, by deviating from the Dirac point one type of carrier becomes dominant, which means that the minority carrier can be ignored. The type

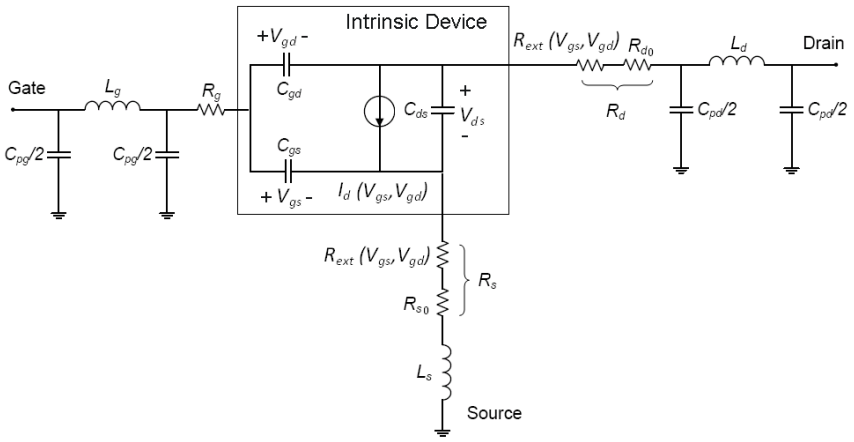

Figure 3.7: Equivalent circuit of a G-FET device.

of majority carrier is determined depending on in which quadrant of the $V_{gs} - V_{gd}$ plane the device bias is (Fig. 3.6). The current in the channel can be expressed as

$$I_{ds} = q\frac{W_g}{L_g}\int_0^{L_g} n(x)v_{drift}(x)dx \tag{3.4}$$

where $n(x)$, $v_{drift}(x)$, L_g and W_g are the carrier density, the carrier velocity, the channel length and the channel width respectively. As described in the previous section, the carrier density close to V_{dirac} approaches to the minimum value of n_0 and away from V_{dirac}, it can be calculated by CV/q. In [37] a semiempirical model is used to describe this behaviour and it is formulated as

$$n(V) = \sqrt{n_0^2 + (CV/q)^2} \tag{3.5}$$

In paper A, by using above relation and ignoring the quantum capacitance, at each quadrant $I_{ds}(V_{gs}, V_{gd})$ is calculated based on a combination of the following closed form expression

$$f(x,y) = \frac{x\sqrt{1+x^2} - y\sqrt{1+y^2}}{2} + \frac{1}{2}\ln\frac{\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y} \tag{3.6}$$

with $x = 0$ or CV_{gs}/qn_0 and $y = 0$ or CV_{gd}/qn_0 depending on the G-FET operating region (Fig. 3.6). Due to the symmetric structure of the G-FETs and since the drain and source are interchangeable, V_{gs} and V_{gd} are selected as independent variables like the model in [82]. In addition, for the calculation of v_{drift}, the model accepts different carrier mobilities for electrons and holes.

The complete equivalent circuit is shown in Fig. 3.7. In order to model carrier-type-dependent contact resistance in G-FETs, a variable term is added to the drain and source resistances. This new term is a function of V_{gs} and V_{gd}, and introduces an extra resistance when the channel majority carriers changes from holes to electrons. The fitting parameters can be extracted by the method described in paper A. However, occasionally some parameters should be manipulated to enhance better

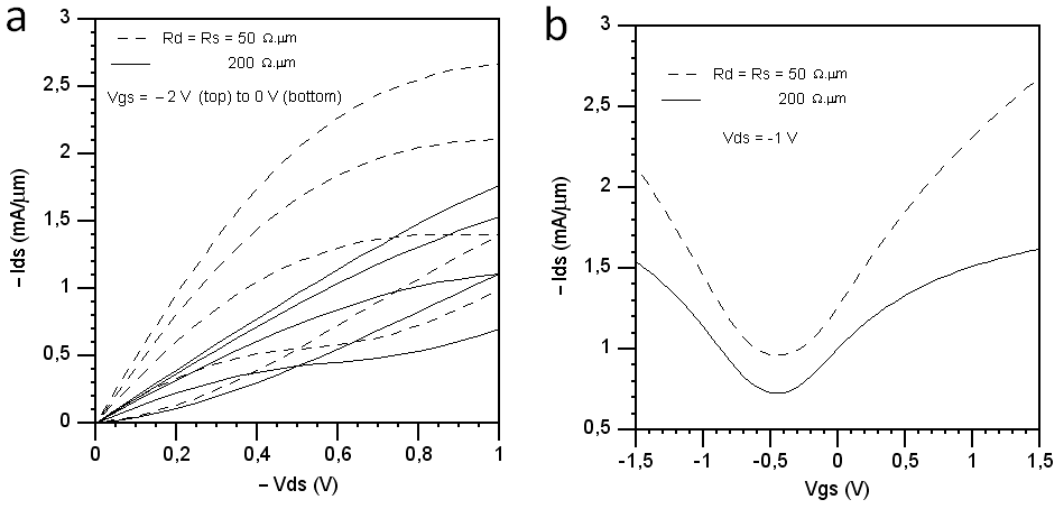

Figure 3.8: a) Simulated I_{ds}-V_{ds}, V_{gs} = -2 V (top) to V_{gs} = 0 V (bottom), b) simulated I_{ds}-V_{gs} at V_{ds} = -1 V, with $R_d = R_s$ = 50 and 200 $\Omega.\mu m$, L_g = 0.5 μm, and $\mu = 5,000\ cm^2/Vs$.

fitting. The model can be implemented in any standard circuit simulation software and in this work it is implemented in Agilent's Advanced Design System (ADS).

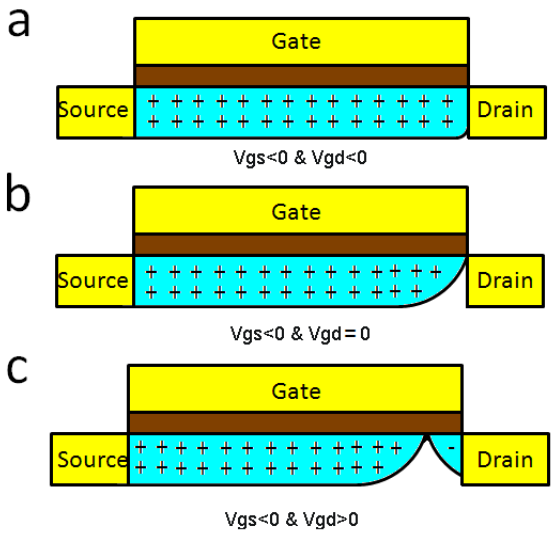

Figure 3.9: a) p-type channel b) channel pinch-off c) bipolar channel.

A simulated output characteristics, I_{ds}-V_{ds}, as well as the corresponding transfer function, I_{ds}-V_{gs} of a G-FET with contact resistances of 50 and 200 $\Omega.\mu m$ is plotted in Fig. 3.8 ($L_g = 0.5\ \mu m$, $\mu = 5,000\ cm^2/Vs$). As can be seen the contact resistance can severely affect the output characteristics. For both curves at V_{gs} = - 0.5 V, the G-FET shows a partial current saturation around V_{ds} = - 0.5 V. The partial current saturation happens at the drain voltage where the carrier type in the channel

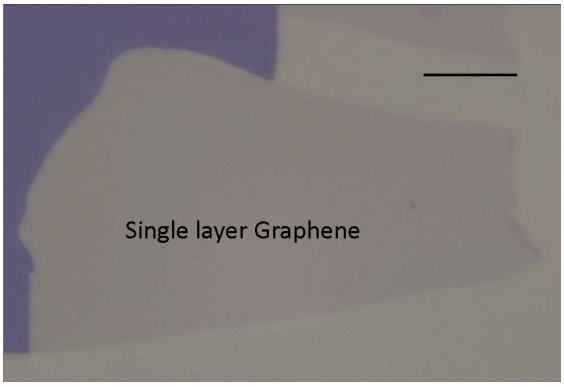

Figure 3.10: A single layer graphene on SiO_2/Si, scale bar 10 μm .

starts changing (Fig. 3.9). For a given V_{gs}, by assuming no unintentional charging, the partial current saturation occurs at the V_{ds} where the output characteristics of the G-FET crosses the line $V_{ds} = R_d I_{ds} + V_{gs}$. Hence, it becomes evident at a lower V_{ds} as R_d decreases (Fig. 3.8a, V_{gs} = -1 V). Besides carrier depletion effect, current saturation can be achieved due to the velocity saturation phenomenon at high fields. For example at V_{ds} = - 1 V and V_{gs} = -1.5 V, since the voltage drop in the device with a lower contact resistance is mainly on the G-FET channel, the carriers' velocity approaches the saturation velocity. Finally, the gate voltage of minimum conductivity, $V_{g,min}$, can be found at $V_{g,min} \simeq V_{dirac} + V_{ds}/2$.

3.3 Device fabrication

Graphene can be produced by several techniques, of which three are commonly used. Micromechanical exfoliation of graphite was the initial method for graphene production [14]. In this method, the graphite crystal is cleaved several times using the tape and then pressed against the desired substrate. Another method is based on the sublimation of silicon carbide substrates at high temperatures in vacuum [26]. This type of graphene is generally referred to as epitaxial graphene. Finally, graphene can be produced via CVD processes [25, 83]. In this method, a metallic substrate is exposed to several precursor gases including a carbon-containing gas which is decomposed at a high temperature ($> 1000°C$). The metal substrate is used as a catalyst in this process, since sp^2 bonds are formed at much higher temperature than that of the CVD process.

In this work, G-FETs are based on exfoliated graphene (Fig. 3.10) yielding high quality films. Nevertheless, fabrication process and design methods developed in this work can be applied to all types of graphene. Especially in [83], it has been shown that CVD graphene can be produced with the same electrical quality as exfoliated graphene. The single-layer character of the graphene sheets can be verified with Raman spectroscopy [84]. For graphene on a 300 nm silicon oxide film, however, it can also be confirmed by measuring the changes in the reflectance of green light [85] and in this work the latter method mainly is used.

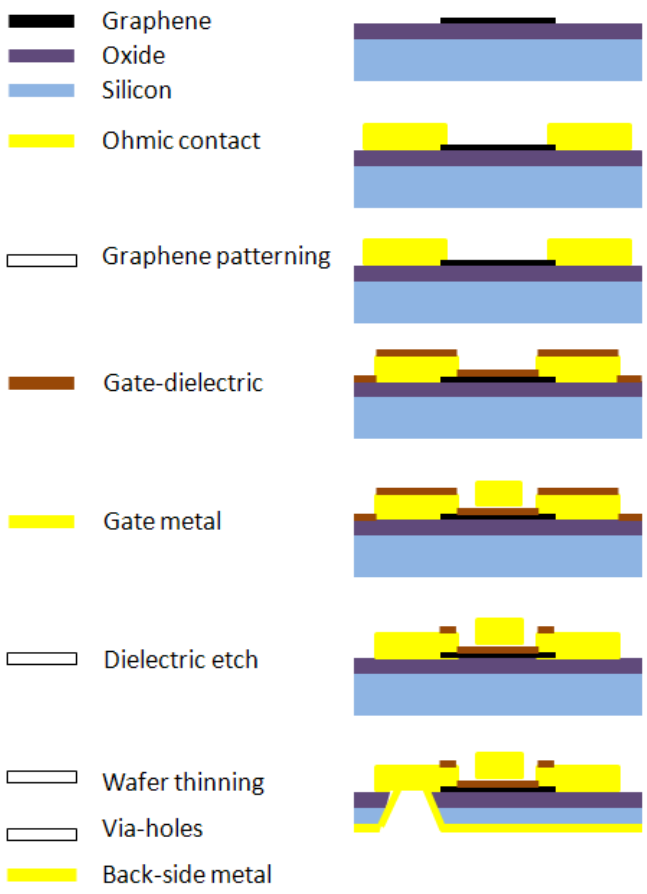

Figure 3.11: Fabrication process sequence.

For microwave applications an insulating substrate is needed and for this, high resistivity silicon ($\rho \geq 10$ kΩ.cm) is used. The fabrication process steps are schematically illustrated in Fig. 3.11. Electron-beam lithography is used for all lift-off processes. The G-FET fabrication sequence includes ohmic contact formation, patterning graphene if needed [paper F], gate dielectric deposition, gate pad formation and finally dielectric etching for defining the drain and source pads. When a circuit is required to be realised in coplanar waveguide (CPW) technology, the complete circuit is fabricated together with the ohmic contact and gate pad formation steps (paper D). However, in microstrip technology, backside processing steps including wafer thinning, etching of via holes and backside metallisation is applied as well (paper F).

3.3.1 Ohmic contact

A metal/graphene contact is more similar to a metal/metal contact than a metal/semiconductor contact, because of the lack of a band gap. By forming a metal/graphene contact there will be a charge transfer at the Metal/Graphene interface due to the difference between the work functions. Since graphene has a low DOS around

the Dirac point (Fig. 2.3b), the charge transfer region appears not only beneath the metal contacts but also far from the contacts into the G-FET channel. The transferred charge significantly shifts E_f, ~ 0.3 eV, underneath the metal contacts [53, 86, 54]. Although graphene-metal interaction charges the graphene layer in the contact area, its sheet resistivity is still high, resulting in a short transfer length, $\approx$ 0.2-1 μm [86, 87]. Therefore carriers are injected into the channel at the edge of the graphene-metal contact. In other words, the contact resistance depends on the contact width rather than the contact area [53].

The choice of contact metal [53], graphene interface quality [40] and the background pressure in evaporators [88] are all factors that affect the contact resistance. Therefore different values have been reported for the same metallisation. Among the reported values, Ni and Ti/Pd/Au (very thin Ti $\approx$ 1 nm) contacts show the best results with contact resistances of $\sim$ 500 $\Omega.\mu m$ [53] and $\sim$ 200 $\Omega.\mu m$ [40], respectively.

In this work the ohmic contact metallisation is based on the stack of Ti(1 nm)/Pd(30 nm)/Au(60 nm) and all devices have a 100 nm access length. So, the reported contact resistance includes the access resistance as well. In order to have a better graphene interface quality prior to the metal deposition for the ohmic contacts, the e-beam lithography process is used rather than the photolithography process. This is because the developing of e-beam resist leaves less polymer residue. In conventional semiconductor processing, oxygen plasma is commonly used to remove polymer residues but this can not be used since it will etch graphene.

There is also a clear correlation between the evaporator background pressure and the resulting contact resistance in fabricated devices. Using an evaporator which has a lower background pressure, $\sim 4 \times 10^{-8}$ mbar, results in contact resistances of $\sim$ 350-550 $\Omega.\mu m$, while utilising an evaporator with much higher background pressure, $\sim 2 \times 10^{-6}$ mbar, leads to roughly twice as high values. Possible reasons could be the reduction of adsorbent molecules on top of graphene and/or prevention of oxidation of the Ti layer during its deposition at lower pressures.

As described above due to the low DOS in graphene, the charge transfer region extends into the device channel. Therefore, when the carrier type in the channel is the opposite of the transferred charge, a p-n junction is formed. Due to the band-to-band tunneling, Klein tunneling, a graphene p-n junction does not have rectifying properties [89, 90]. However, the creation of a p-n junction adds an extra resistance. Hence an asymmetrical behaviour can be seen in G-FETs transfer characteristics. When the charge transfer length is longer than the channel length ($L_g \leq$ 100-150 nm), the polarity of the channel is mainly controlled by the transferred charge [91, 47]. The type of metallic contact influences the asymmetrical behaviour differently. For the case of Ti/Au contacts, this effect is clearly observed. On the other hand, for Cr/Au contacts no asymmetry is observed [53].

3.3.2 Gate dielectric

The gate dielectric formation process can severely degrade the transport properties of graphene [36]. Different methods have been reported to overcome this problem.

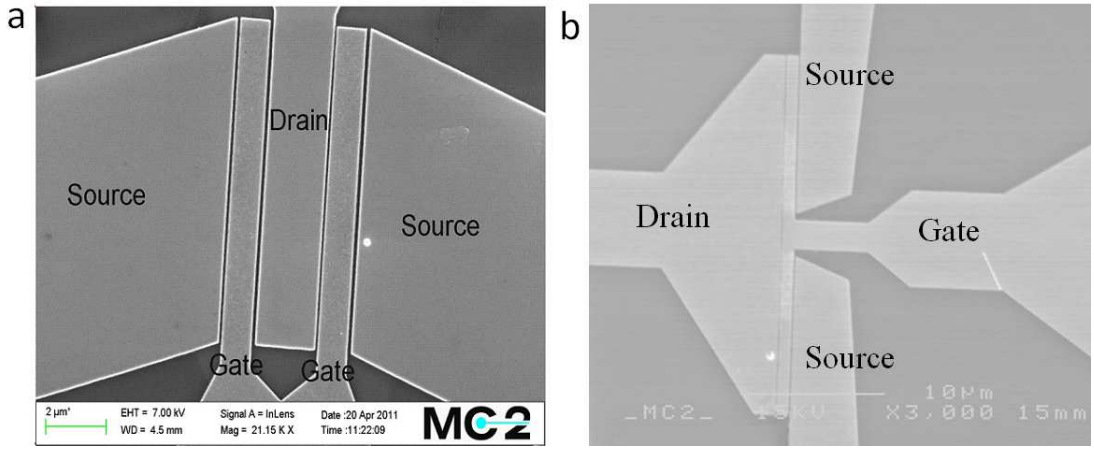

Figure 3.12: a) a G-FET with Al_2O_3 gate dielectric $L_g = 1$ μm, $W_g = 20$ μm, b) a G-FET with silicon nitride gate dielectric, $L_g = 1$ μm, $W_g = 15$ μm.

One approach is to use atomic layer deposition (ALD) of high-k oxides, which is performed at low temperature. Surface pretreatments are generally necessary to avoid discontinuous film growth. For example, as a seed layer, a polymer buffer layer and a 2 nm naturally oxidised Al are used for the ALD of HfO_2 and Al_2O_3 respectively [67, 37]. In addition, a stepwise natural oxidation of evaporated Al can be also used for Al_2O_3 [92]. With above methods only carrier mobility of a few thousands have been achieved. In order to take full advantage of the intrinsic graphene carrier mobility a better gate dielectric as well as substrate is needed. In [93] it is shown that by utilising h-BN as a substrate and gate dielectric the carrier mobility exceeds 15,000 cm^2/Vs. However, a deposition technique for h-BN needs to be developed in order to utilise h-BN.

In this work mainly Al_2O_3 is used as the gate dielectric, obtained by three times natural oxidation of evaporated Al. Moreover, in order to remove resist residues and other adsorbents from G-FETs' channel, devices are annealed in argon gas and then, they are immediately taken to the evaporator chamber. As a result, As a result, the fabricated devices generally has V_{dirac} around zero volt and exhibit carrier mobility of 1000-3000 cm^2/Vs. Besides Al_2O_3 gate dielectric, a method for direct deposition of silicon nitride has been developed in paper B. This method unintentionally charges graphene heavily with electrons and shifts V_{min} to large negative voltages. Consequently, for applications in which gate voltage is needed to be biased at minimum conductivity [paper C], this method of gate dielectric deposition is not suitable. Fig. 3.12 shows typical fabricated G-FETs in this work.

3.4 Device characterisation

The DC characteristics provide a first indication of a G-FET high frequency performance. Transconductance and output conductance are the most important parameters that can be extracted from DC measurement. Transconductance is a quantity

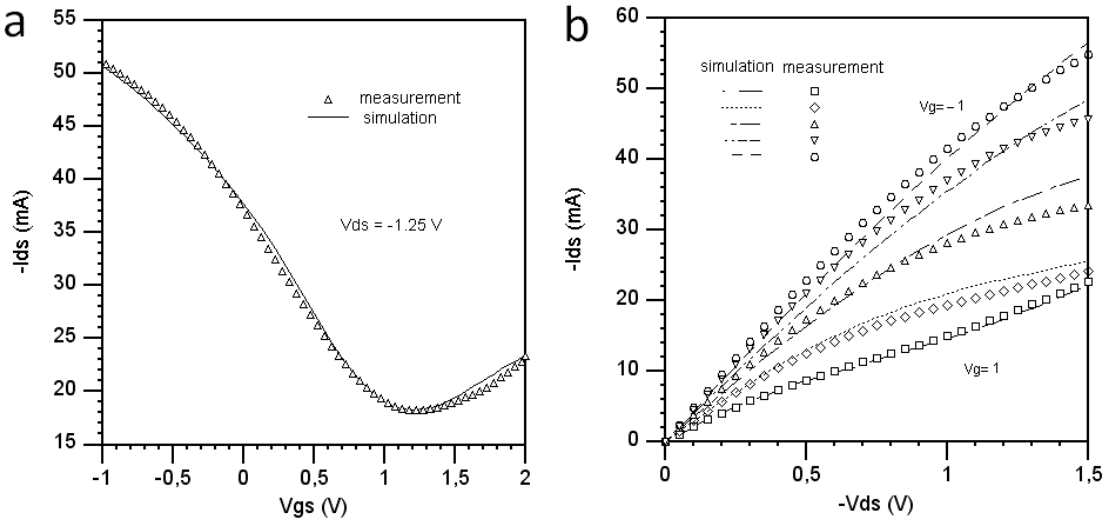

Figure 3.13: a) Transfer function at V_{ds} = -1.25 V, b) output characteristics at V_{gs} = 1 V (top) to V_{gs} = -1 V (bottom), $L_g = 1\ \mu m$ $W_g = 60\ \mu m$.

reflecting the strength of the gate voltage in controlling the channel current and is defined as

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds}=cst} \tag{3.7}$$

and the output conductance represents the inverse of the output resistance of the transistor which is defined as

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}|_{V_{gs}=cst} \tag{3.8}$$

Due to the high contact and access resistances in G-FETs, there is a considerable difference between the intrinsic and extrinsic g_m and g_d. For intrinsic parameters, $g_{m,in}$ and $g_{d,in}$, the above derivatives are based on intrinsic voltages and they are extracted via small signal models while the extrinsic values, $g_{m,ex}$ and $g_{d,ex}$, include parasitics effect and can be found via the DC characterisation.

A high transconductance is beneficial to high-frequency performance. Due to the high contact and access resistances, short gate-length devices, $L_g \leq 200$ nm, generally exhibit a lower $g_{m,ex}$ than do G-FETs with a longer gate length, $\sim$ 1-2 μm. For example in [94], for a G-FET with $L_g = 2.5\ \mu m$ and $W_g = 1\ \mu m$, a $g_{m,ex}$ of 2 $mS/\mu m$ at $V_{ds} = 2.2$ V is reported. However, because of the nonuniformity of the CVD and epitaxial graphene, in general wider G-FETs have a lower $g_{m,ex}$ per channel width. For instance, for long gate length devices, $g_{m,ex}$ on the order of 0.6-1 $mS/\mu m$ [95, 96] while for short gate length G-FETs, $g_{m,ex}$ on the order of 0.05-0.15 $mS/\mu m$ [97, 91] are reported. For high-speed applications, G-FETs should respond quickly to gate variations. In other words, high frequency operation relies on short gate length devices. Therefore, it is necessary to enhance $g_{m,ex}$ for short gate length devices.

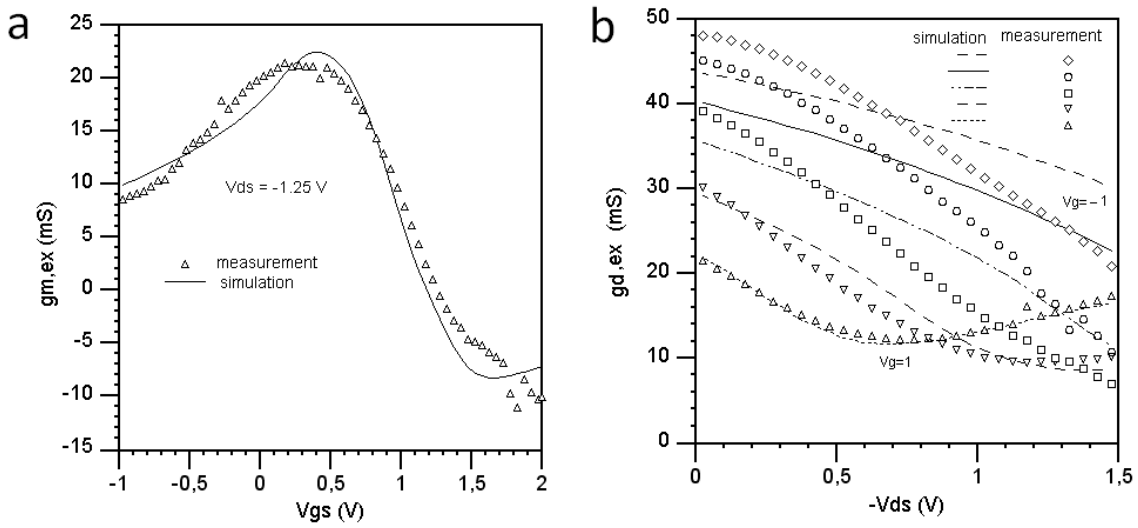

Figure 3.14: a) Device transconductance, b) output conductance.

A low output conductance is essential for voltage and power gain in FETs and can be obtained by achieving a current saturation behavior at the output. Due to the lack of bandgap, G-FETs generally exhibit high output conductances [97, 91, 92, 98]. A small bandgap can be created in G-FETs by moving from zero-bandgap graphene to bilayer graphene or nanostructures. However, this method can result in mobility degradation [32]. In [99] it is shown that by introducing a vertical field in a bilayer G-FET, a $g_{d,ex}$ as low as 2 $\mu S/\mu m$ can be obtained. In addition, as previously described, a partial current saturation can be achieved in gapless G-FETs and a $g_{d,ex}$ on the order of 0.1 $mS/\mu m$ has been reported [96].

Fig. 3.13 shows the transfer function and output characteristics of a G-FET presented in paper D. The device has a $L_g = 1\ \mu m$ and $W_g = 60\ \mu m$. We can see that the device transfer characteristic is asymmetric around the minimum conductivity voltage. The device transconductance and output conductance are depicted in Fig. 3.14. The device has a maximum $g_{m,ex}$ of 0.36 $mS/\mu m$ and a minimum $g_{d,ex}$ of 0.1 $mS/\mu m$. In addition, since the model parameters are extracted from the transfer characteristics, it has a better fit than the output characteristics.

3.4.1 Microwave characterisation

The high frequency capability of transistors is mainly benchmarked by two main figures-of-merits, the cutoff frequency, f_T, and the maximum frequency of oscillation, f_{MAX}.

The cutoff frequency is defined as the frequency at which the short-circuit current gain, h_{21}, is unity. The current gain can be calculated based on the s-parameters as

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{3.9}$$

In [59] an analytical expression for f_T is derived as

$$f_T = \frac{g_{m,in}}{2\pi((C_{gs}+C_{gd})(1+g_{d,in}(R_d+R_s)R_{ds})+C_{gd}g_{m,in}(R_d+R_s)+C_{pg})} \tag{3.10}$$

For the ideal case where the parasitic elements can be ignored, the above expression can be simplified as

$$f_T = \frac{g_{m,in}}{2\pi(C_{gs}+C_{gd})} \tag{3.11}$$

The f_{MAX} is the maximum frequency at which the device can provide unilateral (Mason's gain, [100]) power gain. The Mason's gain, U, can be calculated as

$$U = \frac{|S_{21}-S_{12}|^2}{det(I-SS^*)} \tag{3.12}$$

There is an analytical expression to estimate f_{MAX}, relative to f_T, in [59] as

$$f_{MAX} = \frac{f_T}{2\sqrt{g_{d,in}(R_g+R_s+R_i)+2\pi R_g C_{gd} f_T}} \tag{3.13}$$

To increase f_{MAX} it is important to reduce the gate resistance as well as to have current saturation at the output. It should be noted that for most applications, a high f_T is undoubtedly desirable, but high power gain and f_{MAX} are more important than f_T.

Due to the parasitic elements, especially the high contact and access resistances, generally there is a huge discrepancy between the intrinsic and extrinsic f_T and f_{MAX} for short gate length devices. For example the state-of-the-art intrinsic f_T is 350 GHz, achieved with an epitaxial G-FET at $L_g = 40$ nm, while its extrinsic f_T is about 10 GHz [46]. The low carrier mobility, $\sim$ 1000-2000 cm^2/Vs, in the demonstrated short gate length devices is the main reason for the low intrinsic f_T. The highest reported extrinsic f_T is 55 GHz achieved using CVD grown graphene and nanowire gate [98]. Due to the lack of current saturation in short gate length devices, f_{MAX} generally has a lower value than f_T [91, 92, 97, 98]. The state-of-the-art intrinsic and extrinsic f_{MAX} are 35 GHz and 28 GHz obtained from a SiC G-FET for a gate length of $L_g = 550$ nm [94].

In this work the main focus is the realisation of a microwave amplifier and subharmonic resistive mixer. In the former case, as will be described in Sec. 4.1, a wide device as well as a relatively long gate length, 1 μm, is required for efficient gate modulation. Therefore, the extrinsic f_{MAX} and f_T of these fabricated devices are $\sim$ 5-10 GHz while the intrinsic values are $\sim$ 15-20 GHz. In subharmonic resistive mixers since the device is biased at $V_{ds} = 0$ and a large signal is applied to the gate, f_T and f_{MAX} are not applicable and the operating frequency of the FET mixer is limited by the switching time. This can be estimated by the RC time constant of the device [101]. Hence, besides enhancing the current on-off ratio, it is necessary to decrease the on-state resistance and total capacitance.

CHAPTER

FOUR

GRAPHENE FET MICROWAVE CIRCUITS

In order to realise a complete microwave system by means of G-FETs, different types of circuit building blocks are needed. This includes amplifiers, mixers, frequency multipliers, detectors and oscillators. This chapter presents and analyses the demonstrated circuits with focus on a small signal amplifier and a novel subharmonic resistive mixer.

4.1 Small signal amplifiers

Small-signal amplifiers are among the most common circuits found in any microwave system. Hence, realisation of a G-FET amplifier is an essential step in order to achieve a complete G-FET microwave system.

A single-stage microwave transistor amplifier is shown in Fig. 4.1 where a matching network is used on both sides of the transistor to transform the input and output impedance Z_0 to the desired source and load impedances. There are several definitions of power gain that might be used for an amplifier. The most commonly used definition of power gain is the so-called transducer gain G_T defined as

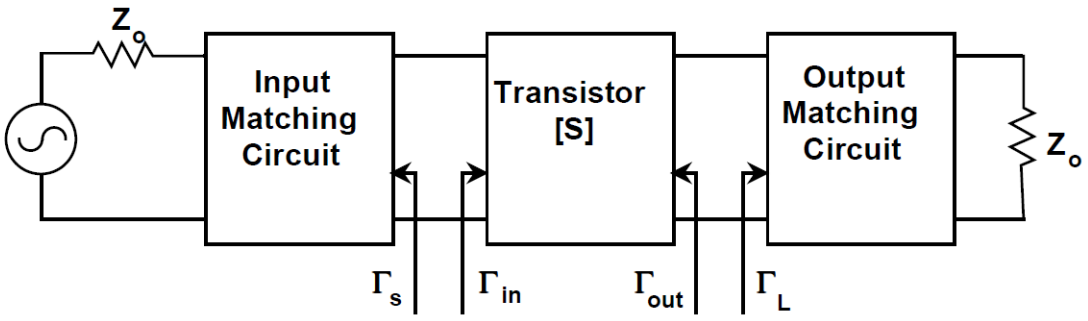

Figure 4.1: A single-stage microwave transistor amplifier diagram.

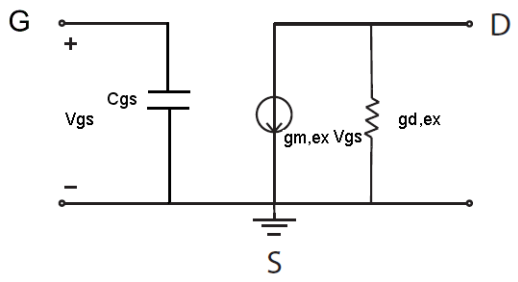

Figure 4.2: A simplified small-signal model of a FET.

$$G_T = \frac{P_{load}}{P_{av}} = \frac{|S_{21}|^2(1-\Gamma_S^2)(1-\Gamma_L^2)}{|1-\Gamma_S\Gamma_{IN}|^2|1-S_{22}\Gamma_L|^2} \tag{4.1}$$

where Γ_L and Γ_S are the load and source reflection coefficient respectively and [S] are the transistor S-parameters at a certain bias point. From Eq. 4.1, it can be seen that $|S_{21}| > 1$ is a sufficient condition in order to have $G_T > 1$ (e.g. with $\Gamma_L = \Gamma_S = 0$).

Fig. 4.2 shows a simplified small signal model of a transistor based on extrinsic transconductance, $g_{m,ex}$, and output conductance, $g_{d,ex}$, which can be found via the DC characterisation. In this case S_{21} can be calculated as

$$S_{21} = \frac{-2Z_0 g_{m,ex}}{1+Z_0 g_{d,ex}} \times \frac{1}{1+j\omega C_{gs} Z_0} \tag{4.2}$$

In order to have a better understanding of the S_{21} behaviour based on the G-FET size and its carrier transport properties, the influence of the device parameters on $g_{m,ex}$ and $g_{d,ex}$ is examined.

Up to now, long gate length G-FETs exhibit a higher $g_{m,ex}$ than do short gate length devices [91, 102]. This is due to the relatively high contact and access resistances, R_c, in G-FETs. Since $g_{m,ex} = \mathrm{d}(Vds/[R_c + R_{ch}(Vgs)])/\mathrm{d}Vgs|_{Vds=cst}$, scaling down the gate length without minimising the series resistances, i.e. $R_{ch}(Vgs) \gg R_c$, will result in devices exhibiting a low $g_{m,ex}$ [91, 92]. Hence, reduction of the contact and access resistance is required in order to utilise a short gate length device. Moreover, as mentioned in paper A, G-FETs generally have different contact resistances depending on the carrier type in the channel. Therefore, the device should be operated by the carrier type resulting in a lower contact resistance. Finally, a higher carrier mobility and capacitance per area results in a higher $g_{m,ex}$.

Current saturation in the output characteristics of the G-FET is needed in order to get a low $g_{d,ex}$. It occurs either by the velocity saturation or by the channel pinch-off effect. The velocity saturation phenomenon in G-FETs can be seen mainly in high mobility ($\approx$10,000 cm^2/Vs) devices [69]. Due to the lack of a band gap in graphene, G-FETs generally do not show a saturation region like conventional FETs. However, as shown before, partial current saturation can be achieved at the drain voltage where the carrier type starts changing (Fig. 3.9). By using Eq. 3.6 the

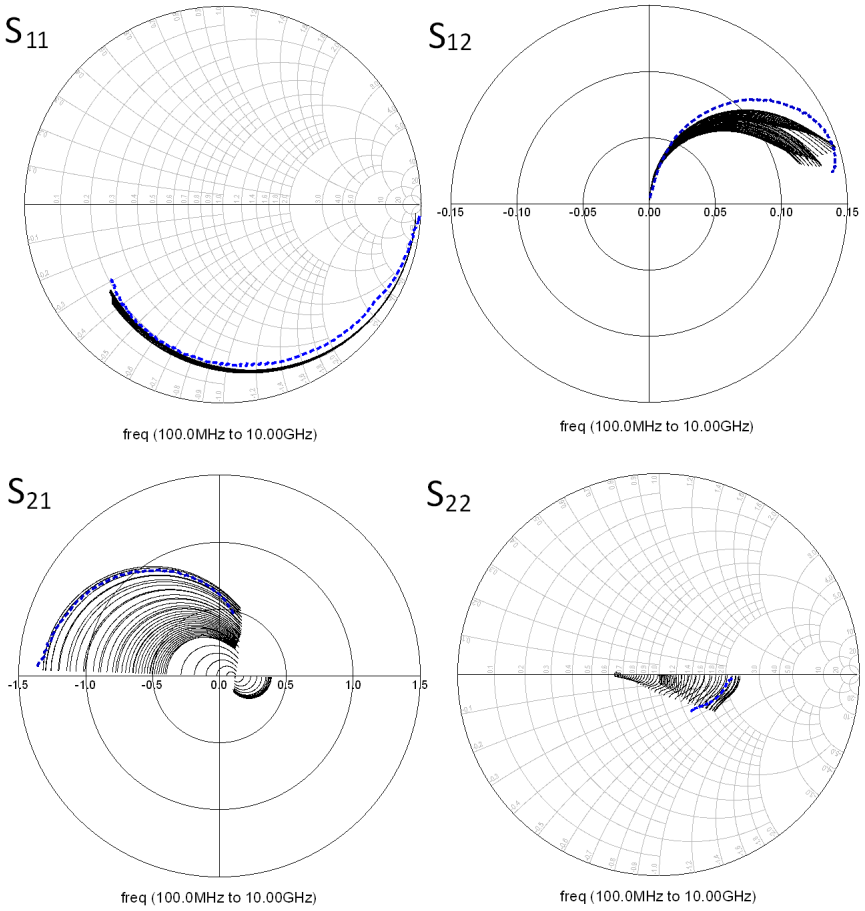

Figure 4.3: Simulated S-parameters versus gate voltage ∈ [-1 V, 2 V] and measured values (dotted line) at V_{gs} = 0.3 V for V_{ds} = -1.25 V.

corresponding $g_{d,ex}$ for $\mu|V_{ds}|/(L_g v_{sat}) < 1$ can be calculated as

$$g_{d,ex} \approx \frac{a}{1 + aR_c/2(\sqrt{1 + (CV_{gs}/Q_0)^2} - 1)} \tag{4.3}$$

where $a = \mu V_0 Q_0 / \sqrt[m]{1 + (\frac{\mu|V_{ds}|}{L_g v_{sat}})^m} \times \frac{W_g}{L_g}$ [paper A]. It is seen that a low $g_{d,ex}$ can be achieved with a higher capacitance per area, C, as well as a higher V_{gs}. The current saturation can be enhanced by adding a back-gate [74, 99], although, for high frequency operation it is preferred to avoid back gated device.

There are several reported G-FET voltage amplifiers [96, 103]. However, the first microwave G-FET amplifier providing power gain is demonstrated in paper D. The design frequency was set to 1 GHz and the gate length was kept at $L_g = 1$ μm for efficient gate modulation because of remaining high contact resistances in G-FETs (400-550 $\Omega.\mu m$) and carrier mobilities in the range of 1500-2500 cm^2/Vs. As discussed above, a higher capacitance per area results in a higher $g_{m,ex}$ and a lower $g_{d,ex}$ at the saturation point and therefore $C \approx 0.5$ $\mu F cm^{-2}$ was selected. Since $g_{m,ex}$ and $g_{d,ex}$ are proportional to the gate width, W_g, the first term in Eq.

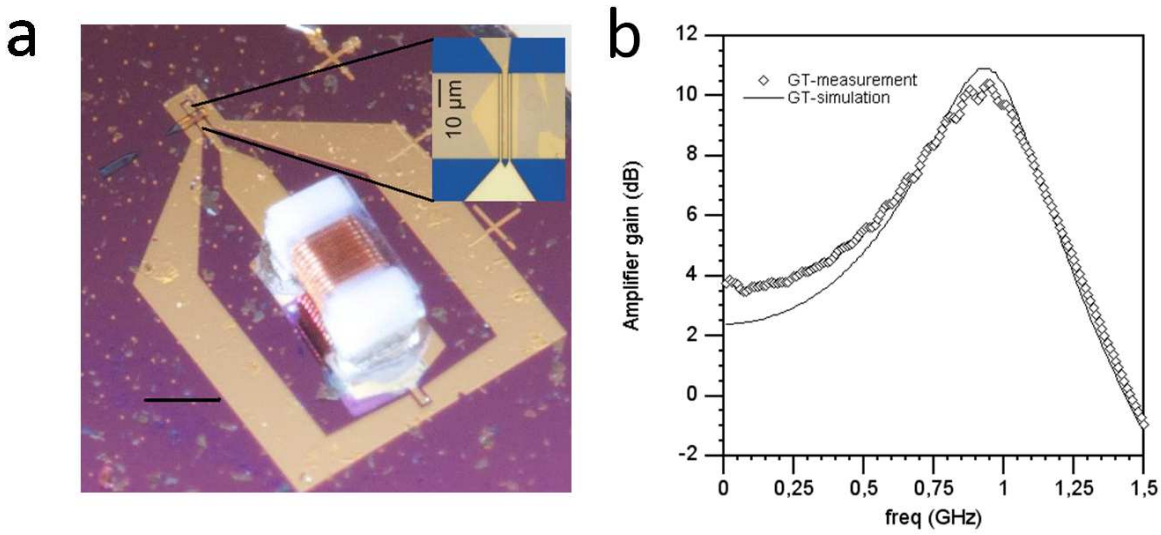

Figure 4.4: a) G-FET amplifier, b) Amplifier gain at V_{gs} = 0.3 V, V_{ds} = -1.25 V

4.2 monotonically increases by increasing the gate width. However, since C_{gs} in the second term of Eq. 4.2 is proportional to W_g, W_g should be selected so that at the operating frequency $\omega C_{gs} Z_0 \ll 1$. For that reason, W_g was selected to be 60 μm. Using the large signal model presented in paper A with the device parameters as stated above, DC and S-parameters simulations were conducted in order to verify the small-signal behaviour, especially $|S_{21}| > 1$.

The measured and simulated $g_{m,ex}$ and $g_{d,ex}$ are shown in Fig. 3.14. As can be seen the simulated $g_{m,ex}$ agrees well with the measurement, but there are deviations for $g_{d,ex}$ at high currents. Due to the unintentional charging in the channel, V_{dirac} = 1.5 V and therefore the partial current saturation occurs at $V_{gs} \approx V_{ds}+V_{dirac}$ = 0.25 V.

By inserting $g_{m,ex} \approx$ 20 mS and $g_{m,ex} \approx$ 12 ms and using together with Eq. 4.2 we can get $|S_{21}| \approx 1.25 > 1$. Fig. 4.3 shows the simulated S-parameters versus gate voltage at V_{ds}=-1.25 V as well as measured value at V_{gs}=0.3 V. The device shows power gain up to 3.3 GHz at the specific bias point and it exhibits f_T = 5 GHz and an f_{MAX} = 7 GHz, without de-embedding. In addition, $|S_{21}| > 1$ for 0.2 V < V_{gs} < 0.6 V at 1 GHz.

The amplifier design was conducted by drawing available power gain circles obtained from the device S-parameters at the design frequency. The maximum available power gain was located on the $r = 1$ circle in the Γ_S plane, therefore a series inductor was utilised to match the input and enhance the gain substantially. The output matching was ignored since it can provide only 0.5 dB higher gain. Fig. 4.4 depicts the fabricated amplifier and its power gain, G_T, versus frequency.

In order to enhance the operating frequency of the G-FET amplifiers, a higher $|S_{21}|$, e.g. $|S_{21}| \geq 4$, is required at low frequencies in combination with a lower gate capacitance and parasitic elements. For that reason, a higher $g_{m,ex}$ and a lower $g_{d,ex}$ should be achieved. The following equations relate the $g_{m,ex}$ and $g_{d,ex}$ to intrinsic counterparts and parasitic resistances

$$g_{m,ex} = \frac{g_{m,in}}{1 + g_{m,in}R_s + g_{d,in}(R_s + R_d)} \tag{4.4}$$

$$g_{d,ex} = \frac{g_{d,in}}{1 + g_{m,in}R_s + g_{d,in}(R_s + R_d)} \tag{4.5}$$

It can be seen that the reduction of the R_s and R_d as well as increasing the device mobility (higher $g_{m,in}$) can essentially increase $g_{m,ex}$. However, in order to reduce $g_{d,ex}$ a more effective current saturation mechanism is needed. As will be described in Sec. 4.2.3, it is possible to decrease R_s and R_d by having a wider contact and access area than the channel width. For reducing $g_{d,in}$, one possible way is to create a small bandgap. Another way is to utilise the velocity saturation phenomenon to induce current saturation which can be achieved by simultaneously enhancing the carrier mobility and reduction of contact and access resistance (Fig. 3.8a, [69]).

4.2 Subharmonic resistive mixers

A frequency mixer converts power from one frequency to another frequency while keeping the signal information mostly intact. For a down-converting mixer the input high frequency RF signal is down-converted to a low frequency IF signal. For passive mixers, the conversion loss is the ratio of input RF and output IF power, CL = P_{RF}/P_{IF}, while active mixers may have conversion gain, CG = 1/CL.

Frequency conversion obeys the superposition principle and it may be performed in a nonlinear or linear system. The former can be nonlinear two terminal devices such as diodes [104]. In the latter case, the linear system must be time-variant in order to generate new frequency components [105].

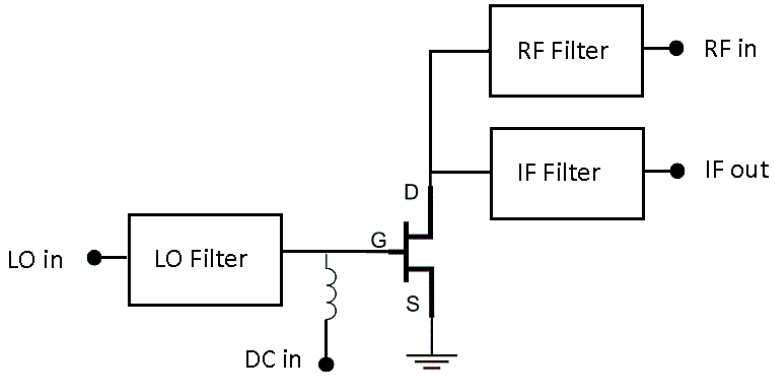

Figure 4.5: General topology for a down-converting single-ended resistive FET mixer.

A linear mixer can be implemented with a variable resistor which is commonly referred to as a *resistive mixer* [106]. The channel of a FET is a good approximation of a linear resistor at low drain-source voltages. In addition, the value of the channel resistance can be varied by the gate voltage. Therefore a resistive mixer can be

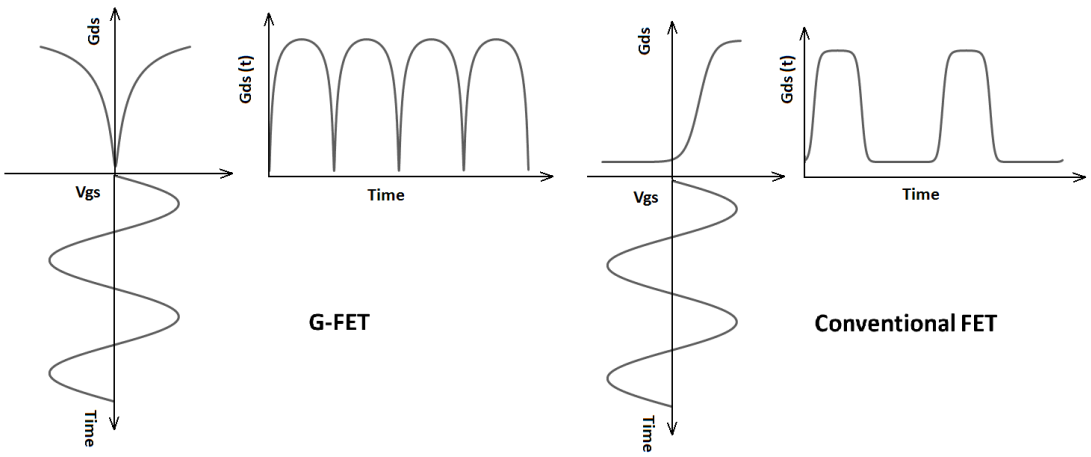

Figure 4.6: The channel conductance and the corresponding conduction wave for a G-FET and a conventional FET.

implemented with a FET channel and it is referred to as a *FET resistive mixer* [107]. Unlike frequency mixing in nonlinear devices, this form of mixer can cause relatively low levels of intermodulation distortion. Moreover, its noise is entirely thermal in origin, so it is not subject to shot-noise degradation. A general topology of a single-ended resistive mixer is shown in Fig. 4.5. In this structure the drain current is the product of the applied RF voltage and the modulated drain-source conductance. An appropriate filtering is required to separate the RF from the IF. Filtering is also necessary to prevent LO leakage from being coupled to the drain.

The channel conductance and the corresponding conduction waveform for a G-FET and a conventional FET is depicted in Fig 4.6. Since G-FETs can conduct current in both n-channel and p-channel modes, due to the electron-hole duality, the frequency of $G_{ds}(t)$ varies as twice the f_{LO}. This property is unique among all types of FETs. Consequently a single-ended G-FET resistive mixer is a subharmonic ($\times 2$) mixer. This feature is attractive, especially at millimeter and submillimeter wavelengths where there is a lack of compact sources providing sufficient power. The conventional subharmonic resistive FET mixers require two FETs in a parallel configuration, including a balun for feeding the two out of phase LO signals [108, 109]. As opposed, the G-FET subharmonic resistive mixer does not need a balun at the LO port.

4.2.1 Analysis of the mixer conversion loss

In this section the conversion loss of the mixer is investigated by means of the wave analysis described in [110, 111]. Although this method does not have the accuracy of methods based on more complex EDA software, it is able to estimate the mixer performance with simple calculations. Moreover, it provides insight into the mixer operation.

A number of simplifications need to be implemented for the wave analysis. The G-FET device is considered to be purely resistive. All mixing terms generated in

the mixer are terminated with the same impedance Z_0 (Fig. 4.7). Furthermore, it is assumed that the RF signal is small enough not to change $R_{ds}(t)$.

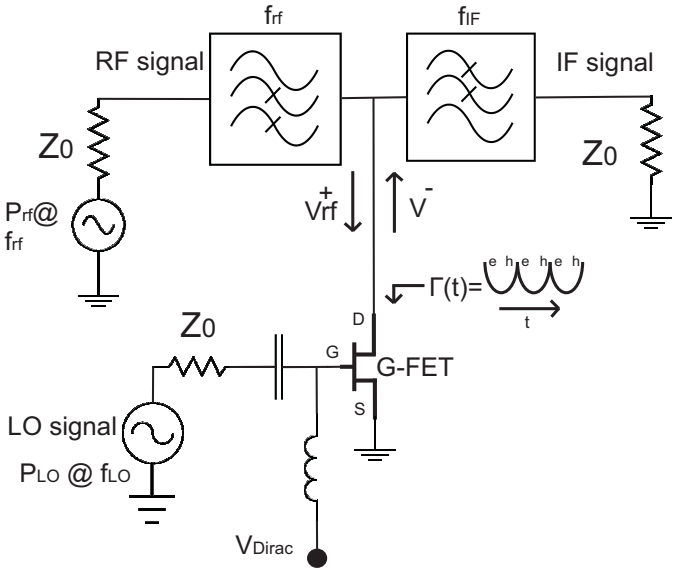

Figure 4.7: The circuit structure of the subharmonic resistive G-FET mixer.

Using the above assumption the reflection coefficient seen from the drain of the G-FET can be obtained as

$$\Gamma(t) = (R_{ds}(V_{LO}(t)) - Z_0)/(R_{ds}(V_{LO}(t)) + Z_0) \tag{4.6}$$

By choosing an appropriate time reference, $\Gamma(t)$ can be defined as an even function without losing generalisation and expressed by

$$\Gamma(t) = \Gamma_0 + \sum \Gamma_n cos(2n\omega_{_{LO}}t)dt \tag{4.7}$$

By applying the RF signal, $V^+_{RF}(t)$ to drain of the G-FET, a reflected voltage $V^-(t) = \Gamma(t)V^+_{RF}(t)$ is generated. The IF component with $f_{IF} = |f_{RF} - 2 \times f_{LO}|$, is extracted via a lowpass filter with a CL of

$$CL = \frac{4}{\Gamma_1^2} = \frac{4}{(2/T\int_0^T \Gamma(t)cos(2\omega_{_{LO}}t)\mathrm{d}t)^2} \tag{4.8}$$

where $T = 2\pi/(2\omega_{_{LO}})$. This simple expression for conversion loss can be directly used to explore the influence on conversion loss from different $\Gamma(t)$ waveforms. The drain-source resistance, R_{ds} can be written as

$$R_{ds} = R_{min} + \frac{R_{max} - R_{min}}{\sqrt{1 + \beta_0(V_{gs} - V_{dirac})^2}}, \tag{4.9}$$

with $\beta_0 = (C/qn_0)^2$ where C, n_0 and q are the gate capacitance per area, residual carrier density [37] and the electron charge respectively. For the sake of simple calculation, the same carrier mobility and the same contact resistance are selected

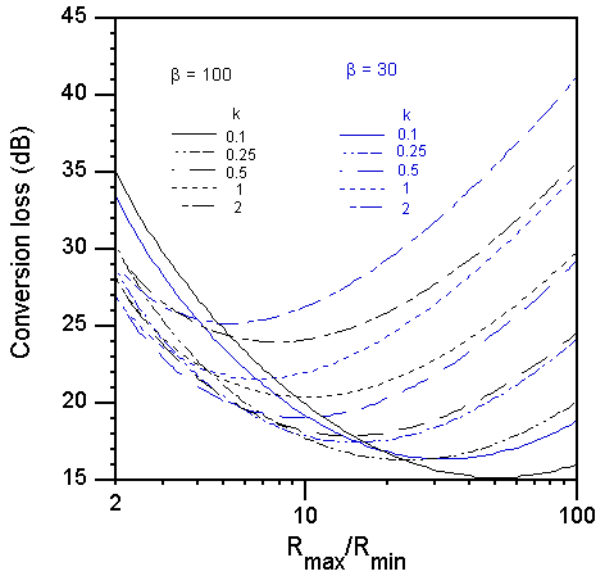

Figure 4.8: CL versus R_{max}/R_{min} for fixed $k = R_{min}/Z_0$ for $\beta = 30$ and 100. All mixing terms generated in the mixer are terminated with the same impedance, Z_0.

independent of the carrier type in the channel. In Eq. 4.9 the second term, $(R_{max} - R_{min})/\sqrt{1+\beta_0(V_g - V_{dirac})^2}$, is referred to as R_{ch}.

Assuming $V_{gs} = V_{LO}\ cos(\omega_{LO}t) + V_{dirac}$, the CL can be calculated as a function of R_{max}/R_{min}, R_{min}/Z_0 and $\beta = \beta_0 V_{LO}^2 = (CV_{LO}/qn_0)^2$. The parameter β contains device properties as well as the LO swing voltage and shows how well the channel resistance can be varied. Hence, it can be used as a figure of merit for the mixer performance. Based on the practical values for the device parameters β can be as high as 100. Fig. 4.8 shows the conversion efficiency versus R_{max}/R_{min} with a fixed $k = R_{min}/Z_0$ for $\beta = 30$ and 100. As can be seen, for a given $k = R_{min}/Z_0$ and β there is an optimum value for R_{max}/R_{min} ratio in order to minimise CL. Moreover, a higher β gives a lower overall CL, and the lowest CL can be achieved when simultaneously having a high R_{max}/R_{min} ratio and a low k. It can be seen that even for high R_{max}/R_{min} ratios, when the embedding impedance is far from R_{min}, i.e. $k = R_{min}/Z_0 > 1$, the CL increases drastically. This shows the importance of having proper impedance levels for G-FETs in the resistive mixer application. In order to reach a CL of 17 dB, $R_{max}/R_{min} \simeq 10$ and $k \simeq 0.3$ are required. It should be noted that since $R_{ch-ON} \sim R_{min}$, R_{max}/R_{min} is higher than the current on-off ratio, $R_{max}/(R_{min} + R_{ch-ON})$.

Further simulation shows that by increasing β and R_{max}/R_{min} as well as selecting proper embedding impedances, the CL decreases and approaches 14.2 dB. For this type of mixer, the lowest expected conversion loss is about 8 dB higher than in conventional subharmonic resistive FET mixers [108] and this is due to the difference in the waveforms of the $\Gamma(t)$. In conventional resistive FET mixers, the $\Gamma(t)$ exhibits a sharp transition between Γ_{max} and Γ_{min} and both on and off states have the same duty cycle. In contrast, a G-FET subharmonic resistive mixer has a smooth

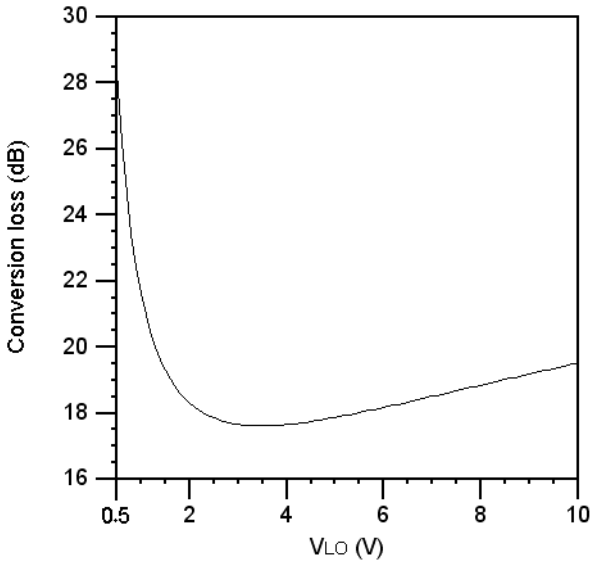

Figure 4.9: CL versus gate V_{LO} for $\beta_0 = 5\ V^{-2}$, $R_{max}/R_{min} = 10$ and $k = R_{min}/Z_0 = 0.5$. All mixing terms generated in the mixer are terminated with the same impedance, Z_0.

transition between Γ_{max} and Γ_{min} and the off state time is shorter than the on state time (Fig. 4.6).

Moreover, in the G-FET resistive subharmonic mixer there is an optimum value for the LO power (gate voltage swing), beyond which the CL increases (Fig. 4.9). This is due to the fact that higher gate voltage swing in G-FETs results in more uneven on and off state in the duty cycle.

The first demonstration of the subharmonic resistive G-FET mixer is presented in paper C. In this mixer $\beta \approx 30$, $R_{min}/Z_0 \approx 1$ and $R_{max}/R_{min} \approx 3.4$. The mixer has a CL of 24 dB which corresponds well with the CL achieved from Fig.4.8. Moreover, Fig. 4.10 shows the experimental spectrum of the $V^-(t)$ waveform, the reflected signal from the drain of the G-FET (Fig. 4.7). Low levels of odd harmonics are observed, which are attributed to a non perfect symmetry of R_{ds}.

4.2.2 Mixer based on a multi-channel G-FET

As can be seen in Fig. 4.8 a higher current on-off ratio is needed in order to decrease the CL. In addition, as shown in paper E the mixer noise is entirely thermal, i.e. $F_{mixer,SSB} \approx$ CL. Therefore the noise properties of the mixer can be enhanced by decreasing the CL. Due to the lack of bandgap in large area graphene, G-FETs generally have a low current on-off ratio. Moreover, since the contact and access resistances in G-FETs are relatively high, the low current on-off ratio becomes more critical as the gate-length decreases. Therefore, the structure of G-FETs should be modified in such a way as to have a higher $R_{channel-OFF}/R_{channel-ON}$ ratio as well as increase $R_{channel}/(R_{channel} + R_{contact} + R_{access})$ ratio.

Using graphene nanoconstrictions not only increases the channel resistance on-

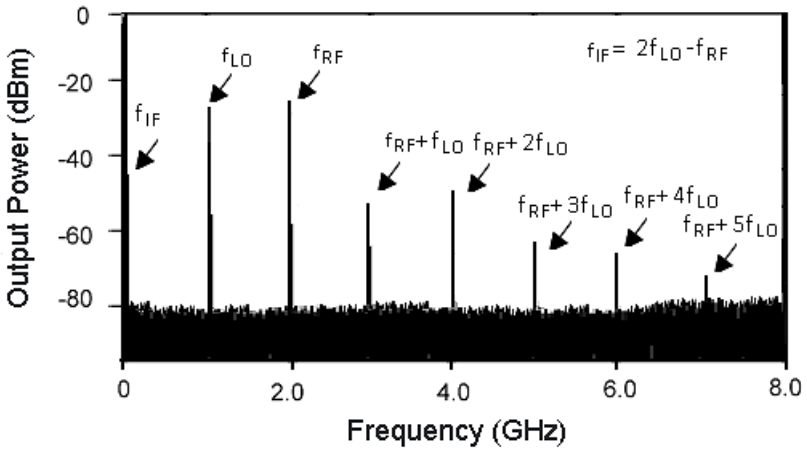

Figure 4.10: Spectrum of the reflected signal, $V^{-}(t)$ and the LO leakage (P_{LO} = 15 dBm, P_{RF} = -20 dBm, f_{RF} = 2 GHz, f_{LO} = 1.01 GHz).

off ratio, it also leads to a higher contribution of the channel resistance to the total drain-source resistance [43]. The latter is due to having a wider contact and access area compared with the channel width (Fig. 4.11a). A G-FET with a narrower constriction gives a higher on-off ratio. However, this may result in G-FETs with a strong asymmetrical transfer characteristic, due to edge effects, which is not suitable for the mixer. In paper F a constriction width of 100-150 nm is selected. Due to the high impedance level of the on-state in this structure, an array of these structures is used to lower the impedance level (Fig. 4.11b). In addition, because of removing about half of the graphene in the channels, the total gate capacitance is decreased approximately by a factor of two. This improves the high frequency performance of the G-FET.

The width of nanoconstrictions formed in paper F is not narrow enough to exhibit quantum effects ($\gg$ 20-30 nm) and can, as a consequence, still be modelled by the equations presented in paper A (Fig. 4.12). The device has a gate length of 0.5 μm and in order to fit the measured data, the gate width should be set to 15 μm, while the device has a contact width of 70 μm (Fig. 4.11c). A wider contact and access area reduces the on-state resistance while the narrower effective channel width increases the off-state resistance. The extracted mobilities are $\mu_h \approx 3300\ cm^2/Vs$ and $\mu_e \approx 2900\ cm^2/Vs$. It should be noted that without having constrictions in the channel, a G-FET with a gate length of 0.5 μm and a gate width of 70 μm has a current on-off ratio less than 3. Although increasing R_{max}/R_{min} from 3 to about 10 is a modest improvement, for this specific application it results in about 6 dB lower CL (Fig. 4.8).

The wave analysis is capable of estimating the mixer performance. However, at higher frequencies where the effect of the G-FET capacitors can no longer be ignored, a more complex method is needed for the mixer design. In paper F, harmonic-balance load-pull simulations were carried out in a standard circuit simulator (Agilent ADS) to estimate the optimum embedding impedances at f_{RF} =

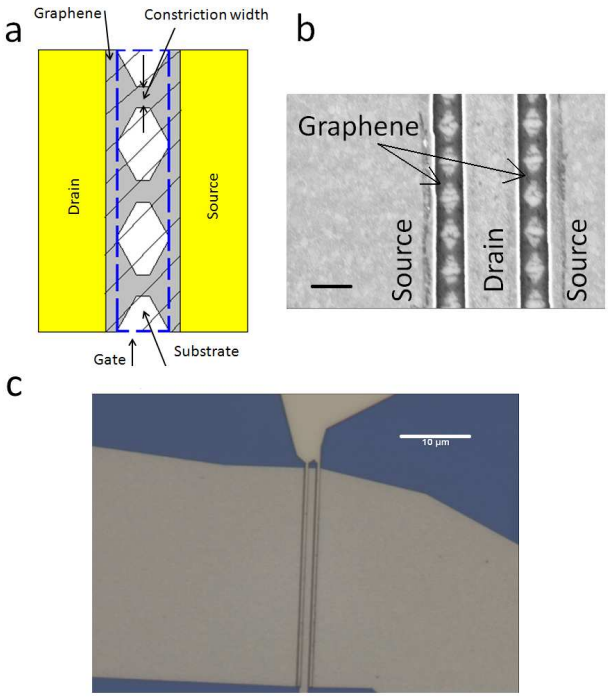

Figure 4.11: a) A schematic of the G-FET with the nanoconstriction channels. The hatched lines indicate the gate dielectric and the dashed line is the gate area. NB! Figure is not to scale. b) SEM image of graphene nanoconstrictions in the G-FET channel before gate-dielectric deposition, scale bar 1 μm. c) Complete G-FET, scale bar 10 μm.

30 GHz. In this simulation, the inductive and capacitive parasitic elements were set to the values obtained from measurement of the open and short structures as described in paper A. The ground inductance of the via holes was calculated by an equation presented in [112]. Fig. 4.13 shows the corresponding contour plots and the chosen embedding impedances. The optimum LO impedance is the impedance at which the gate voltage swing is maximised. However, a simpler LO circuit can be implemented by choosing an LO impedance corresponding to $CL = CL_{min}$ +0.5 dB.

Fig. 4.14 shows the fabricated integrated mixer which is presented in paper F. In this design distributed elements are utilised for the sake of fabrication simplicity. The LO and RF coupled line filters were used to obtain a high RF and LO isolation as well as facilitate an impedance transformation.

The main results are shown in Fig. 4.15. The mixer was characterised between 20 and 35 GHz. A conversion loss (CL) of 19 $\pm$ 1 dB over the frequency range of 24 to 31 GHz is obtained with an LO to RF isolation better than 20 dB at an LO power of 10 dBm. As can be seen from Fig. 4.14 about half of the circuit area is dedicated to the bias circuitry. By developing the fabrication process in a way to reduce the unintentional charging, i.e. $|V_{dirac}| < 0.1$ V, the mixer operates unbiased and requires no bias circuitry. This feature, together with the reduction of the filter

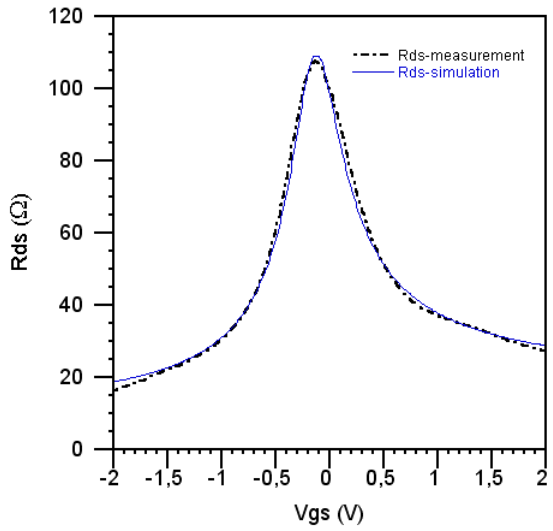

Figure 4.12: Measured and simulated R_{ds} versus gate bias voltage obtained at V_{ds} = 0.1 V.

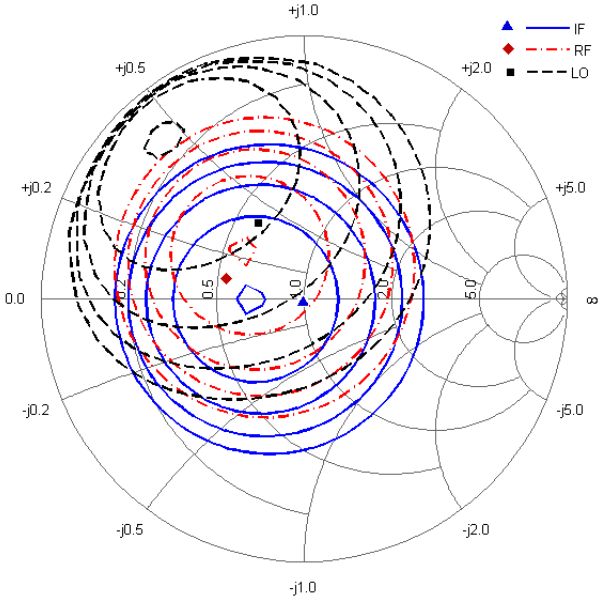

Figure 4.13: Simulated CL contour plots for LO, RF and IF embedding impedances. The inner contour is for CL ≈ 17 dB and the outer contour is for CL ≈ 19 dB (0.5-dB step), P_{LO} = 10 dBm and all other mixing terms are terminated with 50 Ω. The RF, LO and IF selected embedding impedances for the designed circuit are also depicted.

sizes at higher frequencies (f_{RF} > 100 GHz), makes G-FET subharmonic mixers a potential candidate for compact heterodyne array detectors.

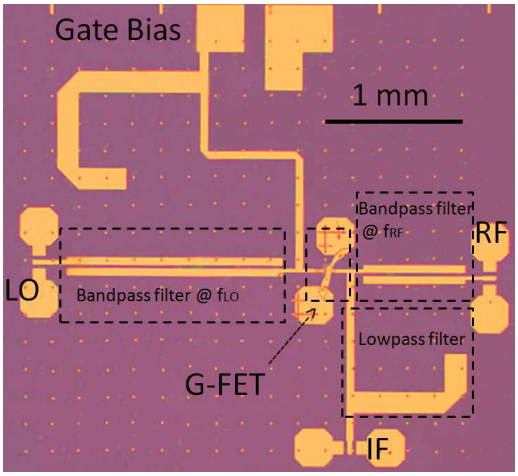

Figure 4.14: Photomicrograph of the fabricated subharmonic mixer on high resistivity silicon substrate. The chip measures 3.4 ×3.2 mm^2.

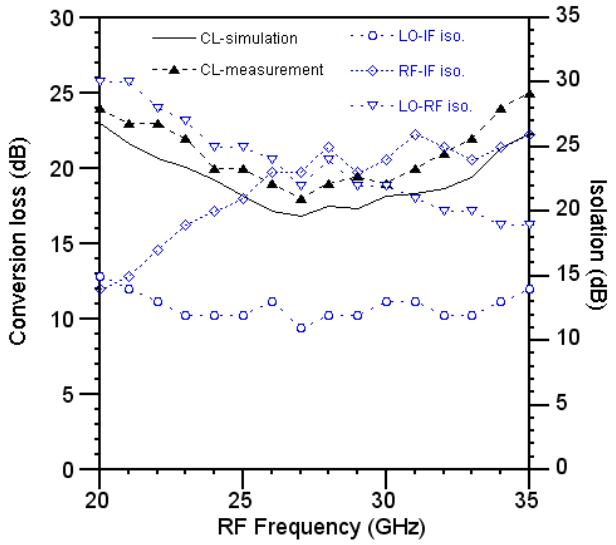

Figure 4.15: Conversion loss and port isolations versus frequency at 10 dBm LO-power with $f_{IF} = 100$ MHz, $f_{LO} = (f_{RF} - f_{IF})/2$.

4.2.3 Mixer linearity measurements

As previously described, a FET in a resistive mixer operates as a variable resistance controlled by the gate voltage. In order to have a linear mixer, the output characteristics of the FET should be linear for all gate voltages. Fig. 4.16 shows I_{ds}-V_{ds} of the G-FET presented in paper F. The zoomed part depicts how the G-FET behaves linearly at low V_{ds} during the entire gate voltage swing.

In order to assess the mixer linearity quantitatively, the well-established two-tone measurement principle [105] is used for the IMD measurement in paper E and F. The two equal-power RF signals are chosen to be at closely spaced frequencies separated by 20 MHz. The linear and third order response of the mixer at $P_{LO} =$

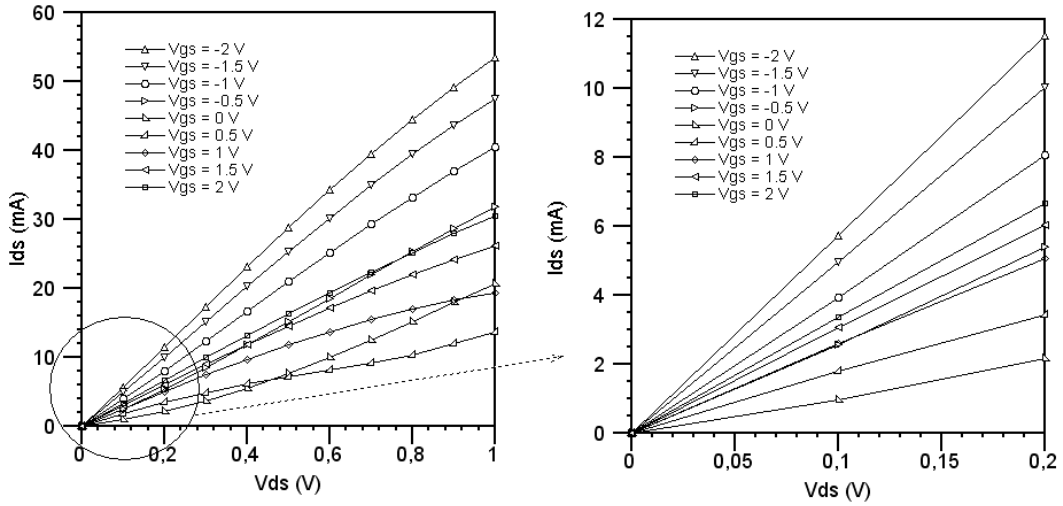

Figure 4.16: Measured DC output characteristics of the G-FET at different gate bias voltages where the linear transport region is identified.

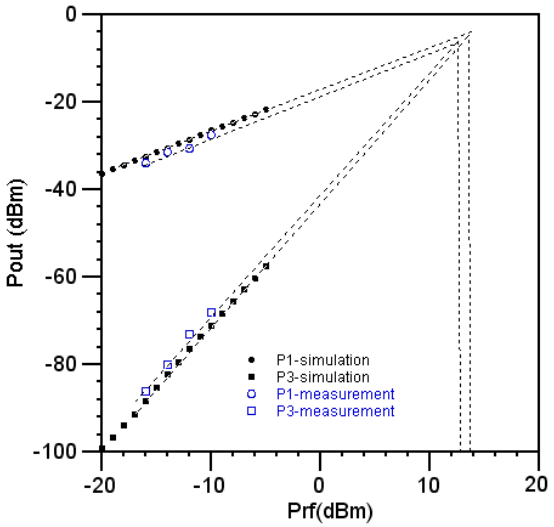

Figure 4.17: Measured and modelled linear and third order response. P_{LO} = 15 dBm.

15 dBm is shown in Fig. 4.17 (paper F). In this measurement f_{IF1} = 110 MHz, f_{IF2} = 90 MHz and the corresponding third order IMD responses were at $2f_{IF1}$-f_{IF2} = 130 MHz and $2f_{IF2}$-f_{IF1} = 70 MHz. The mixer has an IIP3 of 12.8 dBm which is fairly linear. However this value is more than 10 dB lower than IIP3 of GaAs/SiC MESFET single-ended resistive mixers [107],[113].

The mixer linearity is scrutinised by the method described in [114]. The output conductance, G_{ds}, and its derivatives, G_{d2} and G_{d3}, play the main role for the device's IMD behavior in a resistive mixer. As explained in [114], there is a strong correlation between a higher IIP3 and a lower G_{d3} at $V_{ds} \approx 0$. Fig. 4.18 depicts the simulated G_{ds}, G_{d2} and G_{d3} versus V_{gs} for the G-FET presented in paper F. For this device,

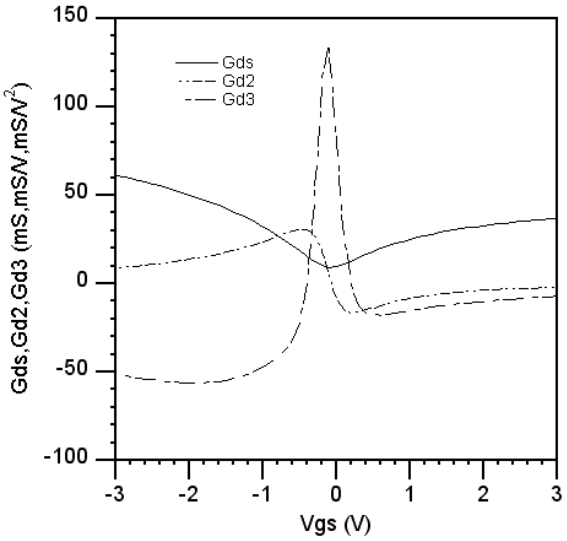

Figure 4.18: Simulated G_{ds}, G_{d2} and G_{d3} versus V_{gs} at $V_{ds} \approx 0$.

the G_{d3} has relatively high values compared with the MESFET in [114]. Moreover, the G_{d3} has lower values at positive gate voltages where the device has a higher contact resistance. This agrees with the result in paper E, where it is shown that by increasing the contact resistance, G-FET resistive mixers become more linear and a higher IIP3 can be achieved. In addition, it leads to a higher CL.

4.3 Fundamental mixers

Frequency mixing by transistors can be performed in the active mode as well. The main advantage of the active FET mixers is that they are able to provide conversion gain, CG. Fig. 4.19 shows a diagram of a single-FET active mixer. In this type of mixer, both RF and LO signals are applied to the gate and the IF signal is extracted from the drain of the FET. The mixer has RF, LO, and IF matching circuits that provide filtering and port-to-port isolation as well.

The mixer operates with the LO signal on the gate generating a time-varying transconductance, $g_{m,ex}(t)$, to which the RF signal is applied. Consequently the mixing terms are generated in the drain current, $g_{m,ex}(t)v_{RF}(t)$, and the IF signal is extracted by a lowpass filter. These mixers are sometimes called transconductance mixers.

Since the time-varying transconductance, $g_{m,ex}(t)$ is the primary contributor to mixing, it is important to maximise its range of variation [115]. G-FETs can generally have a fairly symmetrical transfer characteristic around $V_{g,min}$. Therefore by biasing at this point, the variation range of $g_{m,ex}(t)$ is maximised (Fig. 4.20). In addition the intermodulation distortions are significantly suppressed and a high IIP3 can be obtained. For example in [116] an IIP3 of 13.8 dBm is reported. On the other hand, if the device has an asymmetric transfer characteristics (Fig. 3.14a) the bias point should be selected slightly away from $V_{g,min}$, in order to get a maximum

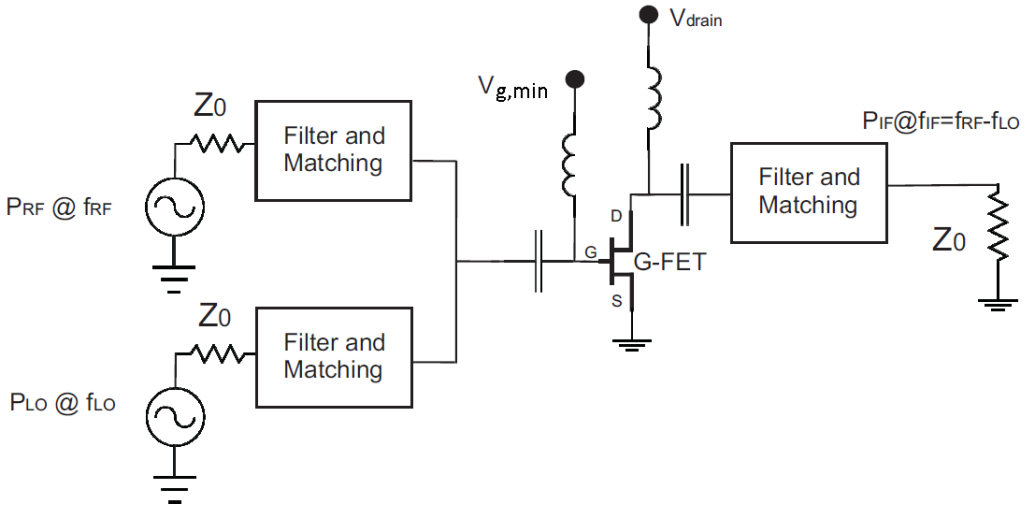

Figure 4.19: a G-FET fundamental mixer.

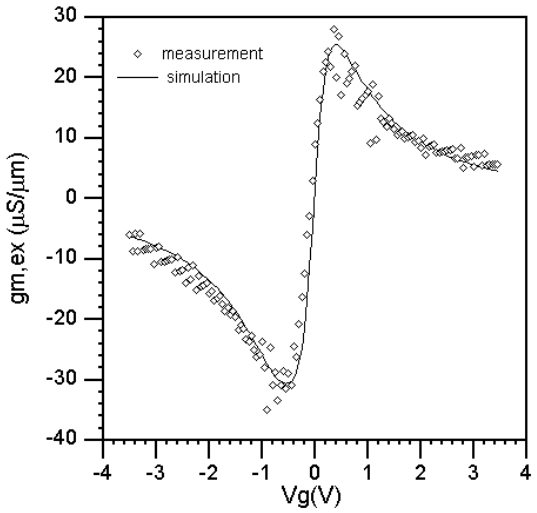

Figure 4.20: A typical G-FET transconductance $V_{DS} = 0.1$ V [paper A].

variation range for $g_{m,ex}(t)$.

In conventional single-FET active mixers, the transconductance waveform has an average (dc) value, which allows the FET to amplify as well as mix the RF signal. Amplification should be minimised to prevent spurious effects [115]. However, for the G-FETs, the average of the transconductance waveform is approximately zero, thereby reducing spurious effects.

The active FET mixer can provide a maximum conversion gain expressed with its small-signal circuit elements and g_1 as

$$CG = \frac{g_1^2 r_{ds}}{4\omega_{RF}^2 C_{gs}^2 (R_g + R_s + R_i)} \tag{4.10}$$

where g_1 is the first order coefficient of the Fourier series of $g_{m,ex}(t)$ [117]. From Fig.

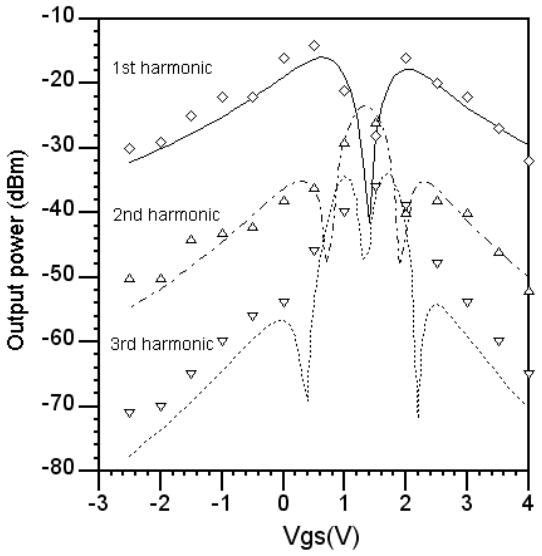

Figure 4.21: Measured and modelled power spectrum, $P_{in} = 0$ dBm, $V_{ds} = 0.5$ V [paper A].

4.20, it can be seen that for a G-FET with a fairly symmetrical transfer function, $g_1 \approx \max(g_{m,ex})$. Due to the currently low transconductance levels and lack of clear current saturation in G-FETs, the reported G-FET active mixers do not show CG, but on the contrary, they have a mainly high CL (≥ 30 dB) [116, 98]. From the above equation it can be seen that by improving the amplifying behaviour of the G-FET, the performance of the transconductance mixer will be substantially enhanced.

4.4 Frequency multipliers

A harmonic frequency multiplier generates a signal whose output frequency is an integer multiple of its input frequency. Frequency multipliers are important especially at millimetre and submillimetre wavelengths where there is a lack of compact sources providing enough power [118].

In all frequency multipliers, a nonlinear element is utilised to convert the pure sinusoidal input signal into a waveform containing more frequency components. Traditionally, nonlinear conductance of varistors [119, 120, 121] and nonlinear capacitance of varactors [119, 122, 123] have been used.

A frequency multiplier can be implemented with a transistor. This enables the integration of the frequency multiplier and the other circuits such as the amplifiers and mixers. This type of frequency multiplier uses the nonlinear transconductance characteristic of the transistor to shape the drain current waveform. Since the transistor uses a DC voltage to generate the channel current, such frequency multipliers have the potential to provide conversion gain.

The signal level and bias voltage applied to the gate determine the shape of the channel current and consequently the harmonic power levels. The power spectrum,

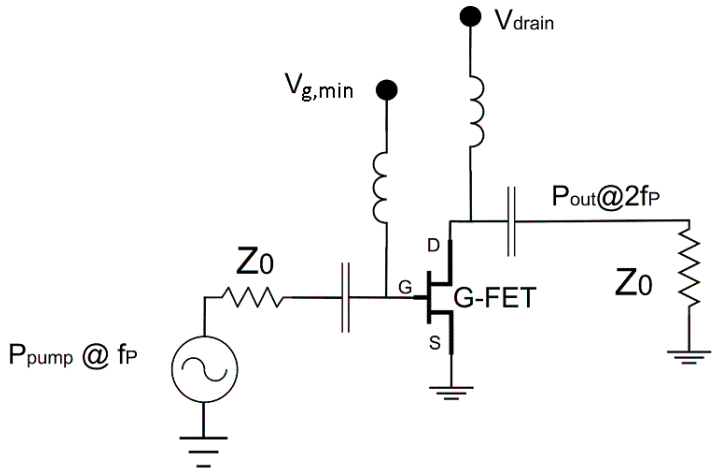

Figure 4.22: Circuit structure of a G-FET frequency doubler.

from simulation or measurement, can be used to find the bias point and input power level. Fig. 4.21 shows the G-FET's ability to generate higher order harmonics. It is seen that by biasing at $V_{gs} = V_{g,min}$, the second harmonic reaches its peak value while the other harmonics drastically decay. As opposed to the conventional single FET frequency doublers [124], the fundamental mode is substantially attenuated [125]. Therefore high spectral purity can be achieved without any filtering element. The circuit structure of a G-FET frequency doubler is depicted in Fig. 4.22.

There are several demonstrations of G-FET frequency doublers [126, 98, 127]. However, the reported CL is relatively high (≥ 25 dB). Like the subharmonic mixers, a higher current on-off ratio is needed to improve the frequency doubler CL which can be achieved by using a multi-channel G-FET as described in Sec. 4.2.2. Moreover, biasing at higher drain voltage can also decrease the CL.

4.5 Oscillators

RF and microwave oscillators are found in all communication systems to provide signal sources for frequency conversion and carrier generation. Generally there are two approaches to the realisation of the oscillators, known as feedback and negative-resistance methods [115].

In a feedback oscillator, an amplifier circuit can be forced to oscillate by feeding some of its output energy back to the input. In [128], a G-FET RF feedback oscillator is demonstrated at 72 MHz. However, due to the phase shift in the long connection from the amplifier to resonator, feedback oscillators are difficult to design at high frequencies.

High frequency oscillators are usually designed by means of a negative differential resistance. Due to physical processes in certain two-terminal devices such as tunnel and Gunn diodes, a negative differential resistance can be achieved [59]. It is however preferable that oscillators be implemented with a transistor for integra-

tion with other circuits. In a transistor oscillator, a negative resistance is created by terminating a potentially unstable transistor with an impedance which puts the device in an unstable region. Generally a FET with a high $|S_{21}|$ value is potentially unstable. The G-FET presented in paper D is unconditionally stable and cannot be used in an oscillator. It is necessary to increase $|S_{21}|$ in order to realise high frequency G-FET oscillators.

CHAPTER

FIVE

CONCLUSIONS AND FUTURE OUTLOOK

5.1 Conclusions

In this thesis the G-FET technology has been studied. The presented work was mostly focused on the development of a novel subharmonic single-ended resistive G-FET mixer. It has involved various aspects of device and circuit fabrication, modelling, design and characterisation.

The developed mixer utilises the unique electron-hole duality characteristic of graphene for subharmonic mixing. As a consequence, the mixer is implemented using only one transistor and no balun is required. Furthermore, by improving the fabrication process in a way so that unintentional charging is reduced, no bias circuitry is needed. These features make G-FET subharmonic mixers a potential candidate for compact high frequency heterodyne array receivers. A 30 GHz mixer is developed in microstrip technology. The mixer exhibits a conversion loss (CL) of 19 ± 1 dB in the frequency range of 24 to 31 GHz. This is the first demonstration of a G-FET based integrated circuit in microstrip technology.

In addition, a semiempirical large signal model has been developed for simulation of G-FETs. The model can be easily implemented in standard EDAs allowing device-circuit co-design. In this way, the effect of process uncertainty on the final circuit performance can be estimated as well. By utilising the model, based on the device size and carrier transport parameters, the amplifying behaviour of the developed G-FETs together with matching networks is analysed. By using the simulation results, the first G-FET microwave amplifier is designed, fabricated and measured. The amplifier has a small-signal power gain of 10 dB at 1 GHz.

5.2 Future outlook

Further development of G-FETs is required in order to compete with the much more mature technology of FETs (HEMT, Si MOSFET). The quality of graphene grown by scalable methods should be enhanced for achieving waferscale high performance devices. In addition, creating a bandgap in the G-FET channel and reducing the

contact and access resistances are two major steps to improve G-FET performance. A solution could be to utilise an array of graphene nanoconstrictions as a G-FET channel. Nanoconstrictions create a band gap more effectively than nanoribbons. For example, it has been shown that by utilising a 20 nm constriction a current on-off ratio of 100-200 is achievable [43]. Although this range of values is not suitable for logic circuits, it is sufficient for RF applications. In addition, due to having a wide contact and access area in nanoconstrictions, lower contact and access resistances can be obtained. Furthermore, in a nanconstriction the width of a small portion of the graphene is reduced to nanoscale, and therefore the carrier mobility is not degraded as for nanoribbons.

The mobility degradation caused by the substrate and gate-dielectric indicates the importance of choosing proper materials for the substrate and gate-dielectric. As shown in [48], with a carrier mobility of 14,000 cm^2/Vs, an intrinsic f_T of 1 THz is achievable. Although, by using a single crystal h-BN the mobility degradation effect can be essentially reduced and the above value can be fulfilled, still a deposition technique for h-BN needs to be developed for utilising thin film h-BN as the substrate and gate-dielectric.

Providing solutions to the above issues enables us to have a silicon compatible technology opening new niches for the development of complete sub-THz/THz system-on-chips.

Finally, besides G-FETs, several graphene based photonic and plasmonic devices capable of radiating THz waves are proposed theoretically [129, 130]. However, the realisation of these devices requires a high carrier mean-free-path in graphene, $>$ 1 μm, which can be achieved only in suspended graphene. Nevertheless, exploring such devices may result in new graphene based technologies operating at extremely high frequencies.

CHAPTER

SIX

SUMMARY OF APPENDED PAPERS

The thesis includes six appended papers for more in depth discussion and detailed presentation of the results. The papers are outlined below.

Paper A

In this paper, a semiempirical G-FET model for analysis and design of G-FET circuits is presented. The model can be implemented in any standard EDAs and it can predict the asymmetrical behaviour of G-FETs. The model is verified by DC, RF and power spectrum characterisation and good agreement between the simulated and the experimental data is achieved.
My contributions: I derived and proposed the symmetrical model, collected all the data, implemented the model in ADS, performed the simulations, and wrote the paper.

Paper B

The influence of a silicon nitride gate dielectric formed by a PECVD method on G-FETs is investigated in this letter. It is found that the high pressure process is more suitable. Since at high pressure, the mean free path of radicals in the plasma decreases and therefore less radicals react with the graphene surface.
My contributions: I developed the process, performed the device fabrication, characterisation, and wrote the letter.

Paper C

A novel subharmonic G-FET mixer is presented in this letter. The mixer takes advantage of the unique electron-hole duality characteristic in graphene. Unlike conventional subharmonic resistive FET mixers, this type of mixer does not need balun at the LO port which makes it more compact.

My contributions: I performed the design, fabrication and characterisation of the mixer, and wrote the letter. This is the first G-FET subharmonic mixer.

Paper D

The realisation of a G-FET microwave amplifier operating at 1 GHz is presented in this letter. The design is optimised for maximum gain and the amplifier exhibits a small-signal power gain of 10 dB. For matching, a lumped inductor is used on the gate yielding a return loss of 20 dB.
My contributions: I participated in the design, fabrication and measurement. This is the first matched graphene amplifier providing power gain at microwave frequencies.

Paper E

In this paper, a complete RF characterisation of subharmonic G-FET mixers including CL, noise figure and intermodulation distortion is presented at f_{RF} = 2-5 GHz. In addition, by using the developed model, the possible future performance of the mixer is analysed.
My contributions: I participated in the measurements, simulations and analysis.

Paper F

A 30 GHz integrated subharmonic resistive G-FET mixer is presented in this paper. The circuit is realised in microstrip technology on 250 μm high resistivity silicon. For enhancing the current on-off ratio and getting proper impedance levels, the G-FET utilises a channel consisting of an array of bow-tie structured graphene. A CL of 19 $\pm$ 1 dB over the frequency range of 24 to 31 GHz is obtained with an LO to RF isolation better than 20 dB.
My contributions: I came up with the idea of utilising a channel consisting of an array of bow-tie structured graphene in order to simultaneously have proper impedance levels and a suitable on-off ratio. In addition, I performed the design, fabrication, characterisation of the mixer and wrote the paper. This is the first millimetre wave graphene FET mixer circuit.

ACKNOWLEDGMENTS

I would like to express my gratitude to all people who helped me during this thesis. In particular I would like to sincerely thank my examiner and supervisor Prof. Jan Stake for his support, guidance and advice during this work. I would also like to thank my co-supervisor Dr. Josip Vukusic for his advisory role and helpful hints. Special thanks to Prof. Olof Engström for fruitful discussions regarding gate dielectric processing and for his support and encouragement. I would like to thank Prof. Erik Kollberg for his valuable discussions and comments on my papers and this work. Thanks to Dr. Sergey Cherednichenko and Vladimir Drakinsky for support and help during this thesis. In addition, a thank you to Prof. Mikael Fogelström for all his support. Thank you Klas Yhland for the discussions on the resistive mixers and your comments on the papers. Thank you Michael Andersson for valuable discussions, your assistance with measurements and proof reading. A thank you to Johanna Hanning for proof reading. I would like to sincerely thank Nanofabrication Laboratory staff especially Henrik Frederiksen, Mats Hagberg, Bengt Nilsson and Mahdad Sadeghi for help in the cleanroom.

Finally, I would like to acknowledge the financing institution. This work has been supported by the Swedish Foundation of Strategic Research (SSF).

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