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Design of a Two Stage Ku-Band Power Amplifier Based on GaN-HEMT Technology

Master's Thesis in Microtechnology and Nanoscience

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THESIS FOR THE DEGREE OF MASTER OF SCIENCE

Design of a Two Stage Ku-Band Power Amplifier Based on GaN-HEMT Technology

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Abstract

This thesis investigates the possibility to design a power amplifier at Ku-band using hybrid design technology. The investigation is based on design, simulation and measurement of a two stage hybrid power amplifier. The device technology used throughout the project is 0.25 um GaN-HEMT obtained from TriQuint Semiconductor. The two stage power amplifier consists of a gain stage and a power stage where balanced topology is employed by means of a 3-dB Branch-Line-Coupler (BLC). The required source and load impedance values are obtained from the source and load pull simulations.

The ADS schematic simulation results show that the amplifier delivers 43.2 dBm output power at P_{1dB}, 19.2 dB gain and 42 % power added efficiency at 15 GHz. For an input power of 24 dBm, the gain stage delivers 10.9 dB gain while the power stage delivers 8.9 dB gain. The momentum simulations, conducted at 15 GHz, provide 40.4 dBm output power, 12.5 dB gain with 21 % of power added efficiency. After tuning with copper foils, small signal measurements provided 14.09 GHz to be the frequency where the maximum gain is obtained. Large signal measurements were only performed for the fabricated and tuned gain stage of the power amplifier. Large signal measurements, conducted at 14.09 GHz, indicate that the gain stage of the power amplifier provides 4.08 dB maximum gain and more than 13 % drain efficiency.

According to the obtained results from both simulations and measurements, Ku-band hybrid power amplifier designs based on GaN-HEMT technology are highly sensitive. This sensitivity is the natural result of the devices instability. Since the GaN-HEMT devices are instable, the required stability network can be complex. Therefore it is essential to maintain the stability network simple with the similar size components. On the other hand, the optimum source and load impedances are highly capacitive. Hence, it makes difficult to design wideband matching networks, which also limits the performance. However, it can be concluded that power amplifier designs at Ku-band based on hybrid technology can provide acceptable performance results.

Acknowledgements

First of all I would like to thank my parents and friends for their support and love.

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List of Abbreviations

Abbreviation	Description
ADS	Advanced Design System
BLC	Branch Line Coupler
CW	Continuous Wave
DUT	Device Under Test
DE	Drain Efficiency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HIC	Hybrid Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
PAE	Power Added Efficiency
RF	Radio Frequency
S2P	Touchstone file format for 2 port S-parameters
SOLT	Short-Open-Load-Through
TRL	Thru-Reflect-Line

1. Introduction

1.1 Background

RF power amplifiers are one of the most critical components in almost all types of wireless applications. Each application has different requirements depending on frequency and type of input signal etc. This leads to the fact that, different power amplifiers have to be designed for each specific purpose. For each of specific purpose, they are expected to provide suitable output power and gain while achieving acceptable efficiency under application-specific linearity considerations. For example, in mobile communication systems, high efficiency and linearity are very important while for military radars high output power is of first concern.

Power amplifiers designed with GaAs device technology have been in use for a long time for both MMICs and HICs, especially for mobile and satellite communications. However, due to comparatively low operation voltage, GaAs device technology is limited to produce high output power levels at high input power. Therefore, wide bandgap devices, such as GaN-HEMT, are more suitable for high power operation due to their high breakdown voltage. Therefore, GaAs devices can act as a driver stage for the GaN-HEMT which can be used in the power stage. However, this approach is only applicable for HIC since MMIC does not allow different semiconductor technology such as GaAs and GaN to be present on the same board.

In HIC amplifiers lumped components and distributed elements are used. However, in some cases, the frequency of operation can be higher than the resonance frequencies of the lumped element values. This situation is therefore becomes a limitation in the HIC design.

1.2 Technical Specification

The aim of this thesis is to design a hybrid power amplifier using GaN device technology. The design specification of the power amplifier is presented in Table 1. The PA is designed based the nonlinear model of the device provided by Modelithics. On the other hand, load-pull measurements are also performed in order to verify the simulated impedances values.

Ku-band Power Amplifier

Parameter	*Specification*
Frequency	Ku-band (12 GHz - 18 GHz)
Output Power	> 40 dBm
Gain	>10 dB
PAE	>10 %

Table 1 Design specifications for Ku-band PA

1.3 Thesis Outline

The different classes of operation of a PA, like Class-A, Class-B, Class-AB and balanced amplifier topology are described in Chapter 2.

Chapter 3 discusses the load-pull measurement set-up, method and its results. The chapter continues with the topics related to the design and simulation of the power amplifier; In particular, stability and bias networks, source-/load-pull simulations, matching networks design and simulation results.

In Chapter 4, the measurement setup and the measurement results of the manufactured PAs are presented and discussed.

Finally, Chapter 5 summarizes the measured results and the differences with the ADS simulations. Proposals for future work are also stated in this chapter.

2. Theory

Power amplifiers are designed depending on the requirements specified by the application. These requirements can be high gain, high power or high efficiency. For example linearity and efficiency are more important in mobile communications, even though there is a trade-off between them. Therefore, it is important to decide the amplifier class and the topology prior to the design.

2.1 Classes of Operations

2.1.1 Class-A

A transistor can be biased in such way that the output current is always present. In other words, transistor has a conduction angle of 360° for the input signal. Therefore, Class-A amplifiers have the highest linearity and gain among all the amplifier classes. However, theoretical efficiency is 50 %, which is considered the lowest efficiency among other amplifier classes.

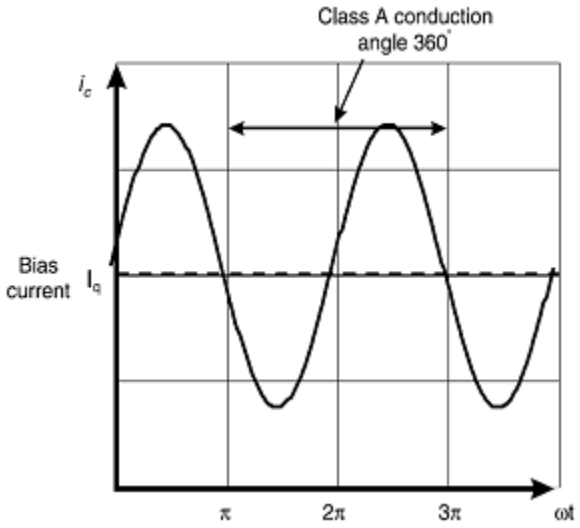


Figure 1 Class-A conduction angle

As a result, Class-A amplifiers are generally used in applications where high gain and linearity are more important than efficiency.

2.1.2 Class-B

Class-B amplifiers conduct half of the input signal cycle. Therefore, the efficiency of Class B amplifiers is higher than the one of compared to the Class-A. The ideal efficiency of a class B amplifier is 78.5 % [1].

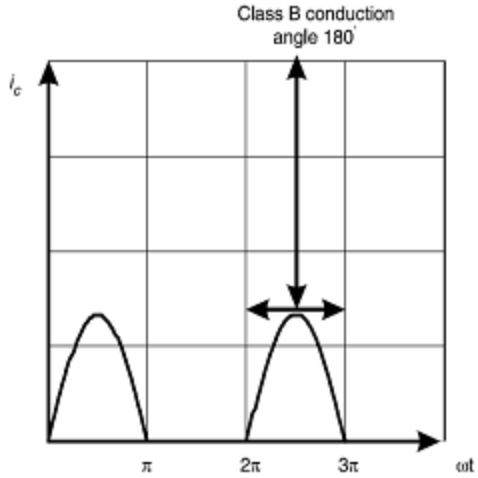


Figure 2 Class-B conduction angle

2.1.3 Class-AB

Class-AB amplifiers are biased between the cut-off point and Class-A. This also means that the bias point is in between Class-A and Class-B. Therefore Class-AB amplifiers have the blend of qualities of both classes in terms of linearity and efficiency. The conduction angle and the theoretical efficiency is between 180° - 360° and 50 % - 78.5 % respectively.

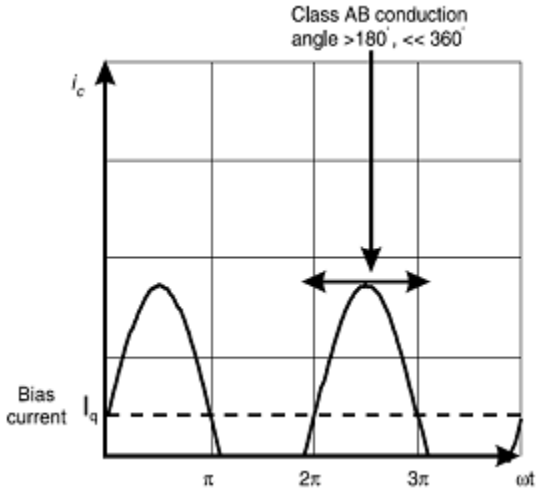


Figure 3 Class-AB conduction angle

2.2 Balanced Amplifier Topology

Figure 4 presents a balanced amplifier topology structure. Balanced amplifier topologies have two identical amplifiers that run in parallel. This structure improves the power characteristics of conventional single ended power amplifiers. The amplifiers in the figure operate out of phase, meaning there is a 90° phase difference between the fed input signals; when the input signal power is divided equally with a 90° power divider. After the separate amplification of each signal at each branch, it is combined with a 90°

power combiner. Thus the in-phase port would have 3 dB more output power and the out-of-phase ports would have no power, which improves the input and the output return losses.

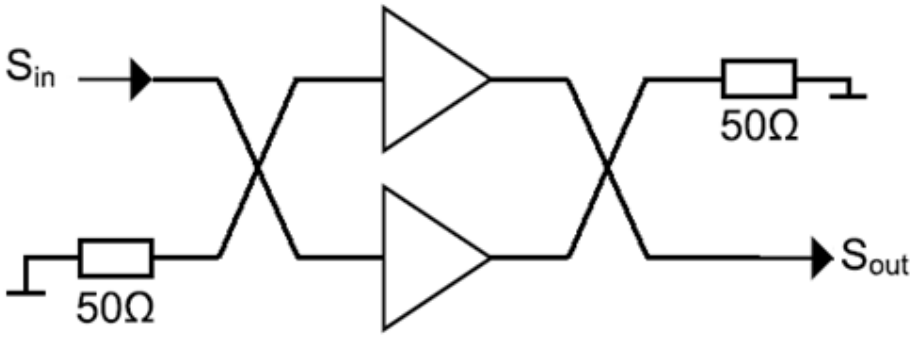


Figure 4 Balanced amplifier structure with a BLC

Different dividers or combiners, such as branch line coupler, Lange coupler etc. can be used for this purpose. Usually for hybrid designs a branch line coupler is more suitable because of its straight forward design and reliability. Therefore a 3 dB branch line coupler can be used as a divider or a combiner for balanced topology purposes. On the other hand Lange coupler is preferred for MMIC designs because of its compact size. In some cases Wilkinson power divider/combiner is used along with a phase shifter. However, resistor used in the Wilkinson power divider/combiner may increase the insertion loss when the there is a mismatch caused by the load impedances.

3. Power Amplifier Design and Simulation

3.1 Bias Point

According to the design specifications, the power amplifier should provide more than 10 dB gain and 10 % of PAE. This allows wide variety choices in terms of bias point. Therefore Class-AB is chosen so that both advantages of Class-A and Class-B are applicable, in terms of efficiency and gain. Therefore, the first step in the design is to choose the appropriate bias voltages for gate and drain.

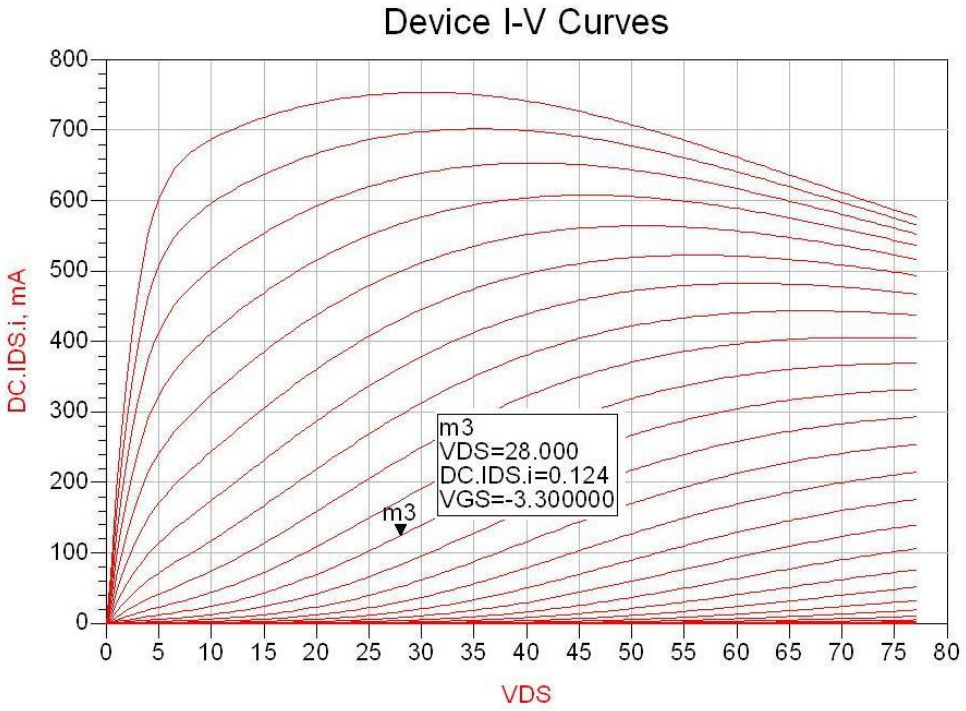


Figure 5 I-V characteristics of GaN HEMT device

Figure 5 shows the I-V characteristics of the GaN device. It gives information on how the drain current is controlled through drain and gate bias voltages. Since class AB is biased between cut-off and Class-A, drain to source voltage and gate to source voltages are selected to be $V_{Drain} = 28\ V$ and $V_{Gate} = -3.3\ V$.

3.2 Device Characterization

According to maximum power transfer rule, the load impedance has to be equal to the conjugate of the output impedance for delivering maximum power. The optimum source and load impedances have to be found in order to obtain the maximum output power. Therefore a procedure called load-pull technique is used.

In the load-pull measurement, the performance of the device is tracked through varying source and/or load impedances. Impedance values are varied by the means of either manual or automatic tuners which are controlled by a computer. The computer then fits the measured performance parameters on a gamma source or gamma load plane. Appropriate impedances for source and load are then determined so that the matching networks can be designed.

Load-pull measurement setup in this project is intended to measure the optimum source and load impedances, so that the input and output matching networks for gain and power stages can be designed. Detailed illustration of the load-pull setup and the actual setup can be seen in Figure 6 and Figure 7 respectively.

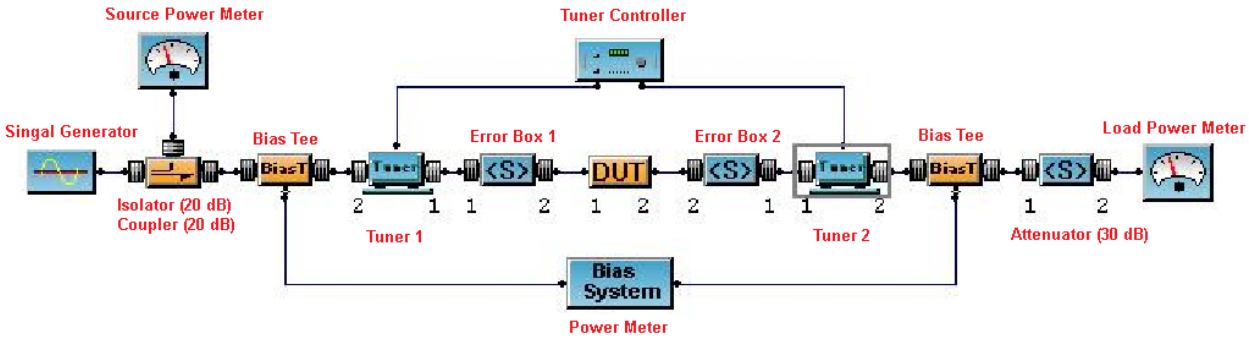


Figure 6 Load-Pull Block Diagram

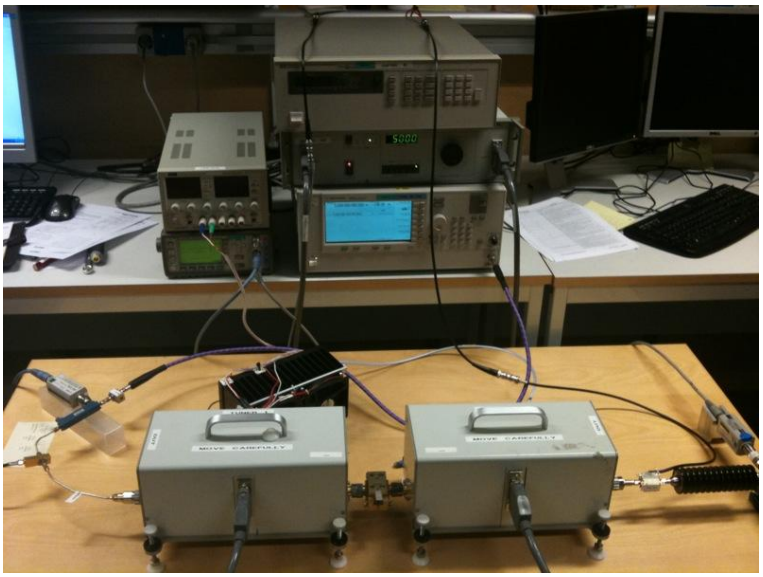


Figure 7 Load-Pull Measurement Setup

All the setup components are connected to a computer via GPIB cables. So that, the Maury Microwave ATS300 SNPW control software can monitor and perform automatic tuning of the mechanical tuners. The software plots power, available gain and power

added efficiency as output on a smith chart. However, in order to achieve accurate results some calibrations have to be done prior to the measurement. These include Tuner calibration, fixture calibration and overall system calibration.

3.2.1 Tuner Calibration

Tuner must be calibrated for each frequency of operation. In this project they are calibrated at 15 GHz. First step to the calibration is that auxiliary equipment such as the VNA has to be properly calibrated. It is also important to maintain the alignment in order to ensure the placement of the tuners in the measurement. Since 15 GHz can be considered high frequency, compared to the 18 GHz of maximum frequency of operation, tuners should be physically leveled to the used cables. This mitigates additional inaccuracies that can be introduced by flexed cables. Therefore tuners are leveled with respect to VNA using a bubble level.

There are different ways to calibrate the tuners. The available methods were step reflection and step position. Step reflection method selects the positions that are generated based on the entered parameters such as separation of magnitude and phase which specifies the density of the measured points. Then the tuner is characterized according to reflection coefficient at each point. Step position on the other hand moves the tuners over ranges of positions and measures the impedance values. In this project selected tuning method is step reflection because more uniform coverage was possible with step reflection method [3].

3.2.2 Fixture Calibration

At higher frequencies fixtures have considerably high loss. This would cause magnitude and phase shift which would lead to false input and output impedance values. Therefore some calibration is needed for the fixture. There are several methods of calibrations such as SOLT, TRL etc. These methods generates 12-term error correction model. These 12-terms represents forward and reverse error stimulus. This error model then are used to generate the input and output error boxes in order to de-embed inaccuracies brought by the fixture that the device is mounted on.

First step to generate these boxes is to calibrate the VNA properly with the same cables that will be used in the fixture calibration. It is also important to choose the method of calibration for the fixture calibration. From the different types of methods as explained earlier, TRL method is used in this project. The reason for this is that, TRL calibration determines the reflection coefficient and the transmission factor along with the S-parameters of the error boxes by only assuming the characteristic impedance and lengths are known. The calibration continues by measuring different length of transmission lines (1 mm, 3 mm, 5.5 mm and 30 mm). Lastly thru connection was measured where input and output ports of the fixture are connected directly together. This is done in order to define the “thru” error model.

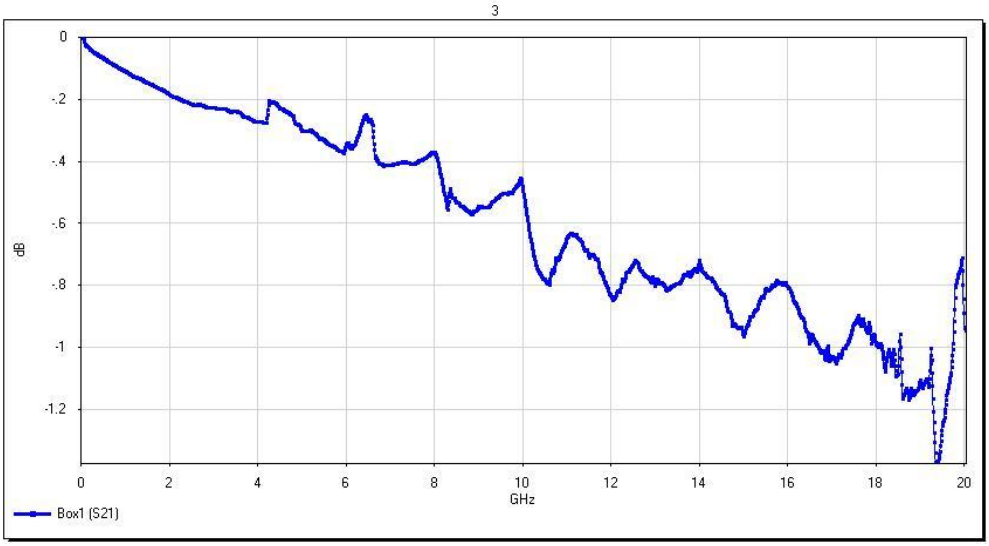


Figure 8 Error Terms for the input of the high power fixture

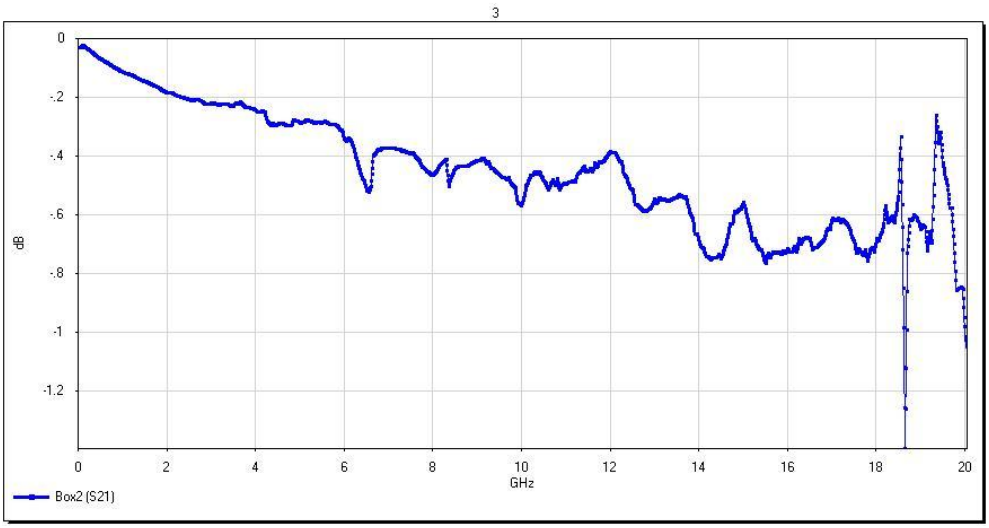


Figure 9 Error Terms for the output of the high power fixture

3.2.3 Overall System Calibration

In the setup there are other error sources that should be defined for accurate measurement of the optimum impedance values. This step is necessary towards accurate measurement since the frequency of operation is high and at high frequencies, RF components may have different behavior from low frequencies. Therefore 30 dB attenuator that is used to protect the output power meter is characterized along with the bias tee so the software can de-embed the S-parameter from the measured data. Prior to running the load-pull measurement the control software also requires system thru

calibration at 15 GHz which is done by removing the fixture and directly connecting the input and output tuners.

3.2.4 Load-Pull Results

After the calibration procedures, the load-pull measurement is carried out. According to the device s2p file provided by TriQuint Semiconductors, the S-parameters of the device at 15 GHz are close to edge of the Smith Chart. Therefore in order for the tuners to find the optimum impedances on the gamma plane, they should cover a magnitude of 0.95 over all the phase angles at 15 GHz.

However, the results were not as expected. As it can be seen from Figure 10, the tuners were only able to cover up to a magnitude level of 0.77, which was not enough.

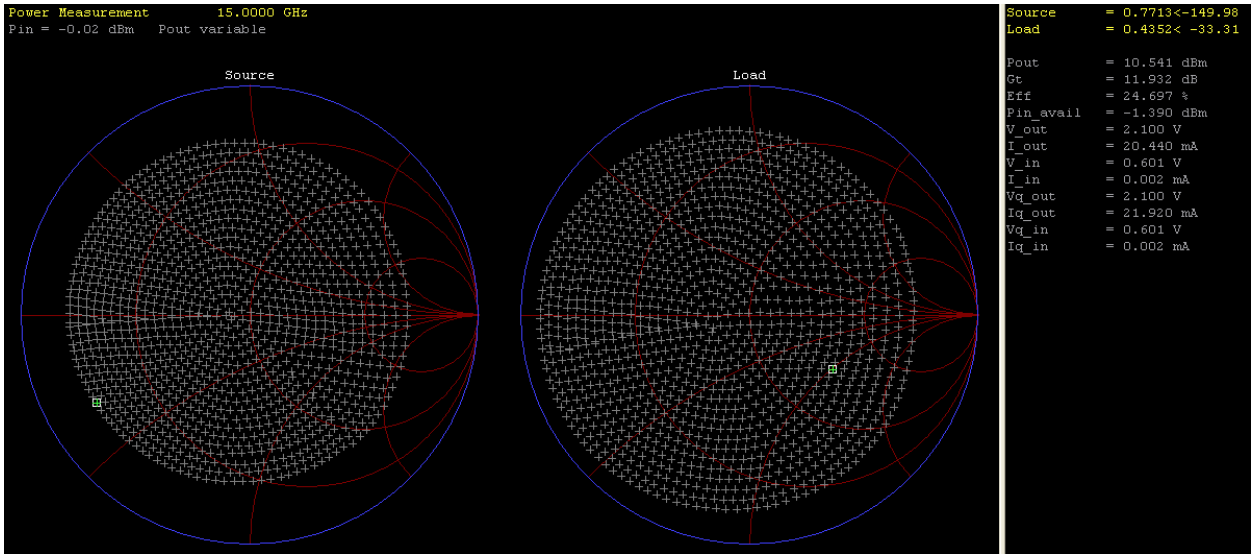


Figure 10 Tuner coverage during load-pull measurement

There were some other measurements carried out with different fixture and transistor. The device used is a low noise GaAs FET obtained by Mitsubishi Semiconductor. Same calibrations were also performed. According to the datasheet of the device tuners had to cover the magnitude of approximately 0.5 to obtain data.

After the load-pull measurements results were as expected. The device was able to provide 3 dB to 4 dB gain at 15 GHz when biased at $V_{DS} = 3\,V, I_D = 10\,mA$. This measurement verifies the reliability of the set-up as well as the software used to run the load-pull measurements. However, the tuners were not capable of delivering enough coverage for GaN-HEMT at 15 GHz. Therefore, the design of the power amplifier is continued based on model for the device provided by Modelithics Inc.

3.3 Stability Network

An amplifier should satisfy sufficient stability conditions to avoid oscillations. These conditions are stability factor ("$K > 1$") and stability measure ("$|\Delta| > 0$") [5]. Based on these conditions, if an amplifier is unstable, a stability network has to be designed to ensure the unconditional stability of the PA.

In this project, the stability network is designed with a capacitor in parallel with a series resistance and a series resistor at the gate bias network. Theoretically, this circuit should attenuate lower frequencies without affecting the gain at higher frequencies. However, slight reduction in the gain can be expected depending on the tolerances of the components that are used in the fabricated PA. The series resistor also improves the return loss as well as providing overall gain flatness.

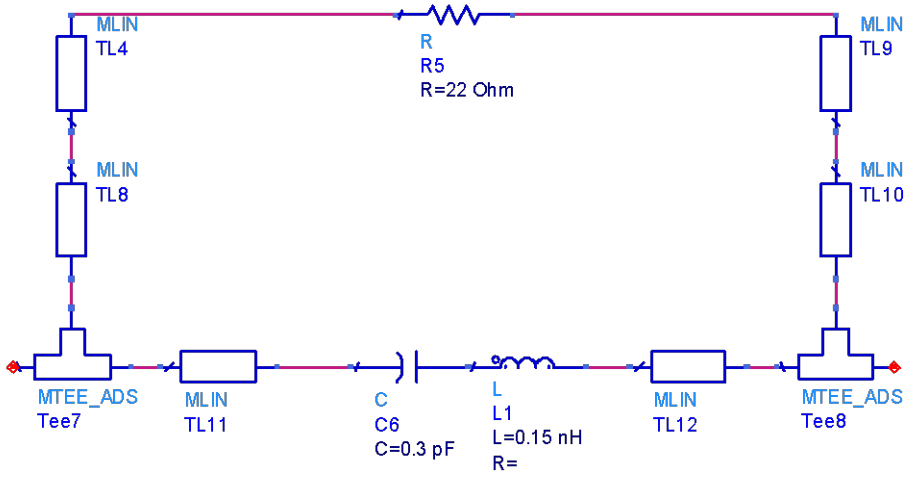
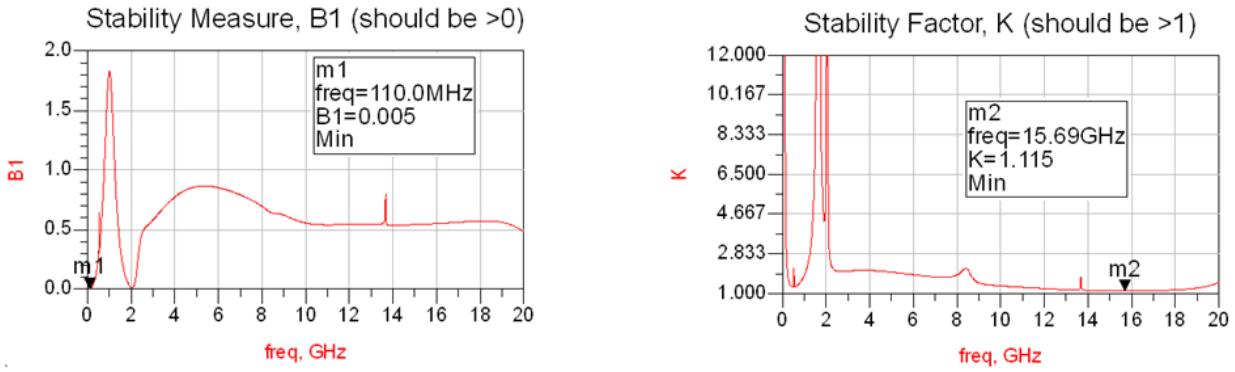


Figure 11 Stability network schematic

The resistor, parallel to the gate series capacitor has a resistance value of $22\ \Omega$ and the resistor at the gate bias network has a resistance value of $100\ \Omega$. Both of these resistances are considered to be standard film resistors at the fabrication of the PA. The capacitor is on the other hand is a single layer capacitor with a value of $0.3\ pF$. In order to attach the single layer capacitor to the distributed element golden bonding wires have to be used. Therefore the inductor seen in the Figure 11 represents the rough estimation of the inductance that is introduced by the bonding wires. In bonding wire process 5 or 6 parallel wires are used to reduce the total inductance.

In order to test the stability of the amplifier, stability network is simulated in series with the device. Since there is a trade-off between stability and gain, stability network is designed, so that stability factor "K" is close to "1" (one) as possible while maintaining stability measure "|Δ|" above "0" (zero). The results can be seen in Figure 12



(a) (b)

Figure 12 Stability Measure "|Δ|" (a) and Stability Factor "K" (b)

3.4 Bias Network

The role of the bias network is to block unwanted DC and RF from either sources (signal source and DC source) whereas both DC and RF have to be present at the device. The frequency of operation in this project is 15 GHz; therefore special attention has to be paid in blocking this frequency. In order to block DC, $1\ pF$ capacitor is used at the input and output.

In order to ensure open circuit condition at the operating frequency, an open radial stub together with a quarter wave transmission line are used. In order to electromagnetically define the open radial stub, a short transmission line between open radial stub and the tee is used. The principal behind this design is that the open radial stub is transformed into short circuit at the tee. The $90°$ transmission line then transforms short circuit to open circuit at the gate of the device. This ensures that at the frequency of operation, the bias network is seen as an open circuit, but at low frequencies other methods of RF block has to be employed. Therefore, towards the DC source various capacitors are added to short circuit these frequencies. These capacitors are also called decoupling capacitors. Bias network can be seen in Figure 13.

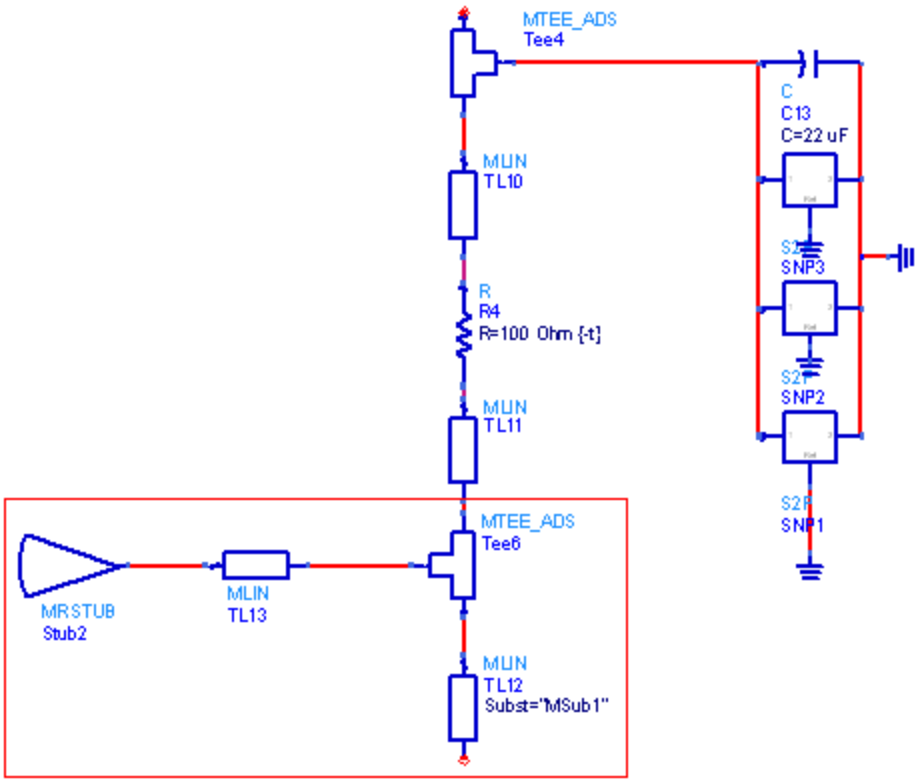


Figure 13 Bias network schematic

3.5 Matching Networks

Matching networks provide transformation from "Z_{source}" and "Z_{load}" to standard $50\ \Omega$ termination at a limited bandwidth. These "Z_{source}" and "Z_{load}" values are required in order to provide desired max power, gain or PAE. Therefore it is important to find these optimum values through source-load pull measurements or simulations. In this project optimum source and load impedances are obtained through source-load pull simulations using the device model. These values are then used to design the input and output matching networks with distributed components.

3.5.1 Gain Stage

The first stage of the PA is designed to drive the power stage. This stage is designed to provide most of the overall RF gain. Therefore, source-pull and load-pull simulations performed for high gain. From these simulations different impedance values for input and output matching network is obtained. The values for different input power levels at 15 GHz can be seen in Table 2.

Ku-band Power Amplifier
Gain Stage

$P_{Avaliable}$	P_{output}	$Gain$	PAE	Z_{Source}	Z_{Load}
21	32.94	11.94	21.45 %	0.906 - j*63.382	5.228 - j*47.492
22	34.00	12.00	24.32 %	0.906 - j*63.382	5.228 - j*47.492
23	35.04	12.04	27.46 %	0.906 - j*63.382	5.228 - j*47.492
24	36.04	12.04	30.90 %	0.906 - j*63.382	5.228 - j*47.492
25	36.98	11.98	34.52 %	0.906 - j*63.382	5.228 - j*47.492
26	37.82	11.82	38.05 %	0.906 - j*63.382	5.228 - j*47.492
27	38.44	11.44	40.52 %	0.906 - j*63.382	5.228 - j*47.492

Table 2 Gain stage input and output impedance values

The input matching network for the gain stage is designed to transform 50 Ω transmission line impedance to the source impedance ($\mathrm{Z_{Source}} = 0.906 - \mathrm{j} * 63.382$). The output matching network for the gain stage is designed to transform load impedance ($\mathrm{Z_{Load}} = 5.228 - \mathrm{j} * 47.492$) to 50 Ω transmission line impedance. In the output matching network, an open radial stub is used to achieve wider bandwidth. With the use of proper input and output matching networks approximately 12 dB gain is expected from the gain stage of the power amplifier.

3.5.2 Power Stage

Power stage of PA is designed to provide high power rather than high gain. Therefore same matching network that is used in the gain stage may not be used. The values for different input power levels at 15 GHz can be seen in Table 3.

Ku-band Power Amplifier
Power Stage

$P_{Avaliable}$	P_{output}	$Gain$	PAE	Z_{Source}	Z_{Load}
30 dBm	39.77 dBm	9.77 dB	42.85 %	0.906 - j*63.382	9.639 - j*52.293
31 dBm	40.62 dBm	9.62 dB	48.52 %	0.906 - j*63.382	9.639 - j*52.293
32 dBm	41.21 dBm	9.21 dB	49.79 %	0.906 - j*63.382	9.639 - j*52.293
33 dBm	41.71 dBm	8.71 dB	49.57 %	0.906 - j*63.382	9.639 - j*52.293
34 dBm	41.58 dBm	7.58 dB	49.90 %	0.906 - j*63.382	9.639 - j*52.293
35 dBm	41.24 dBm	6.24 dB	49.64 %	0.906 - j*63.382	9.639 - j*52.293
36 dBm	40.92 dBm	4.92 dB	45.22 %	0.906 - j*63.382	9.639 - j*52.293

Table 3 Power stage input and output impedance values

The input matching network for the power stage is designed to transform 50 Ω transmission line impedance to the source impedance ($\mathrm{Z_{Source}} = 0.906 - \mathrm{j} * 63.382$).

The output matching network for the power stage is designed to transform load impedance ($Z_{Load} = 9.639 - j * 52.293$) to 50 Ω transmission line impedance. With the use of proper input and output matching networks approximately 8 dB gain is expected from the power stage of the power amplifier.

3.6 Branch Line Coupler

The power stage of the power amplifier circuit is composed of two parallel identical amplifiers. This approach is used to achieve $3\,dB$ more power at the output when compared to a single power stage amplifier circuit. This topology is called balanced topology; see Figure 4 in Chapter 2. The input power to the power stage is divided by the means of a $3\,dB$ coupler, amplified and then combined again by a second coupler [6]. The BLC schematic and electromagnetic simulation results are presented Figure 14 and Figure 15 respectively.

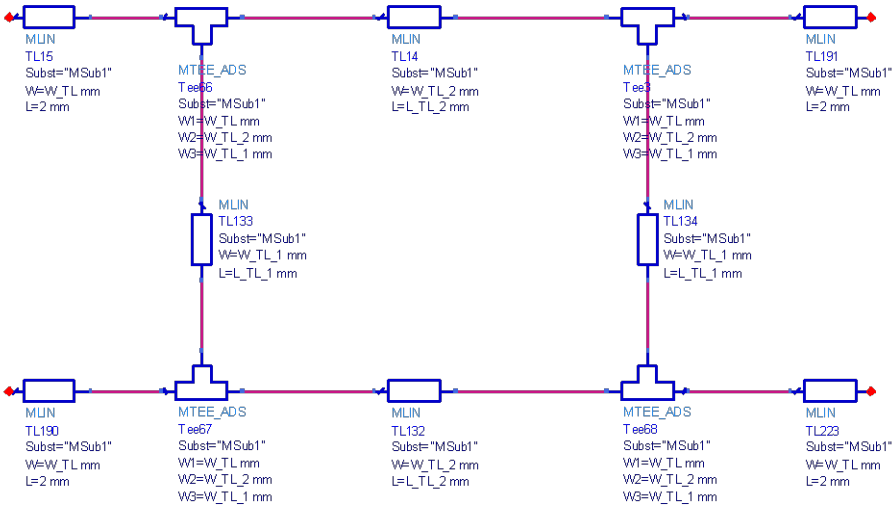


Figure 14 3-dB Branch-Line-Coupler

Ku-band Power Amplifier
Branch Line Coupler

Parameter	*Value*
W_TL_1	1.17 mm
L_TL_1	3.38 mm
W_TL_2	1.65 mm
L_TL_2	2.37 mm

Table 4 3-dB Branch-Line-Coupler transmission line values

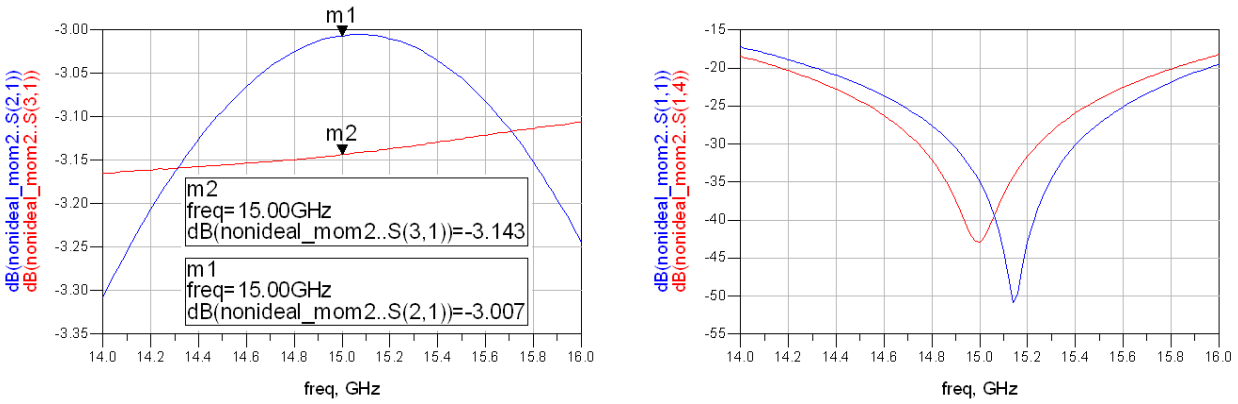


Figure 15 Electromagnetic simulation of designed BLC

Electromagnetic simulations show that, the designed BLC provides acceptable 3-dB coupling throughout 14 GHz to 16 GHz bandwidth. Isolated ports, terminated with $50\ \Omega$, provides more than 15 dB rejection throughout 14 GHz to 16 GHz bandwidth and more than 30 dB rejection around the frequency of operation. Therefore, the designed BLC is suitable for dividing and combining power for the balanced topology.

3.7 Simulation Results

As mentioned earlier, the PA is designed using a computer aided design tool called ADS. ADS provides two different simulation opportunities. These, can be referred to as schematic simulation and electromagnetic simulation called Momentum. Simulations using both procedures are performed on the PA. Illustration of the designed PA which shows the gain stage and the balanced power stage can be seen in Figure 16.

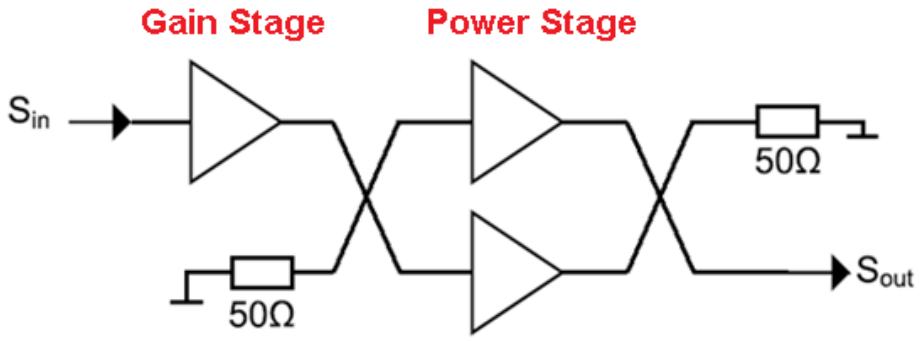


Figure 16 Illustration of the designed PA

3.7.1 Schematic Simulation Results

Although each stage is designed individually to meet the expectations, final simulation is still needed to be carried out in order to verify the schematic design. Therefore each stage is put together with the designed BLC.

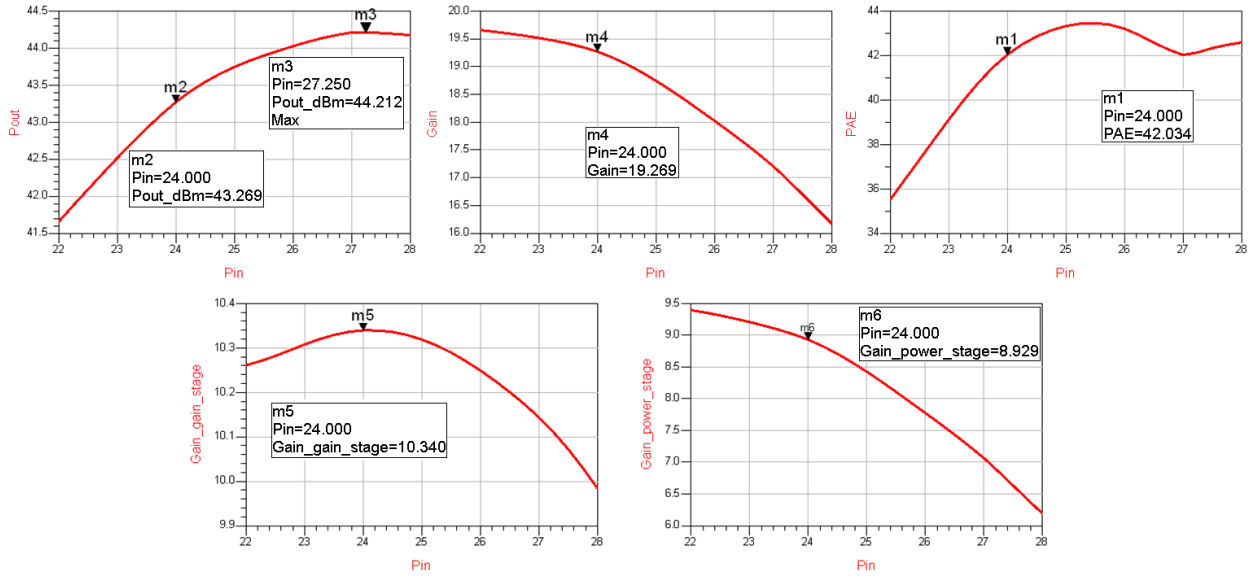


Figure 17 PA schematic simulation results at 15 GHz

Schematic simulation results indicate that, at 15 GHz the maximum output power of the PA is 44.2 dBm. 1 dB compression point occurs approximately at 24 dBm of input power. At this point, the PA provides 19.2 dB gain and 42 % of PAE. It can also be noticed that the gain stage provides more gain than the power stage which is also expected due to the matching circuit configurations.

3.7.2 Monte-Carlo Simulation Result

Each component, lumped element or distributed transmission line, has manufacturing tolerances that affect the overall PA results. In the Monte-Carlo Simulations provided by the ADS, it is possible to investigate the affects of the circuit component tolerances. Table 5 presents the Gaussian deviation used in the Monte-Carlo simulation and Figure 18 presents the Monte-Carlo simulation results with 50 iterations over varied P_{in} from 21 dBm to 31 dBm.

Ku-band Power Amplifier
Monte-Carlo Simulation

Parameter	*Gaussian Deviation*
Transmission Line Widths	$\pm 0.01\ mm$
Open Stub Widths	$\pm 0.01\ mm$
Open Stub Lengths	$\pm 0.01\ mm$
Open Radial Stub Widths	$\pm 0.01\ mm$
Capacitor Values	$\pm 0.0025\ nF$
Resistance Values	$\pm 1\ \Omega$

Table 5 PA Monte-Carlo Simulation results

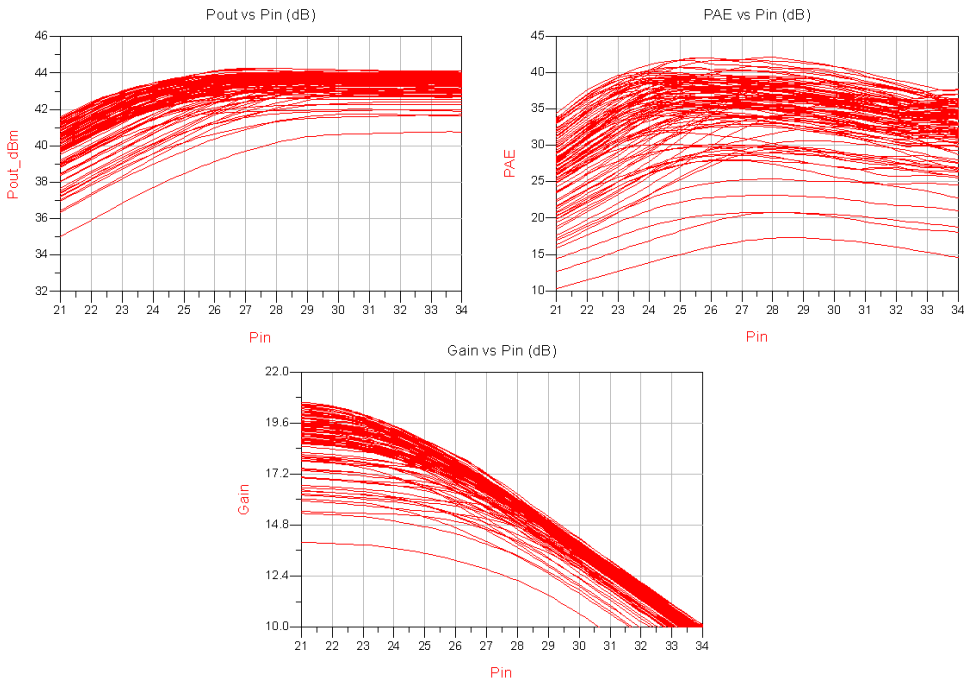


Figure 18 Monte-Carlo Simulations with input power sweep

Monte-Carlo simulations indicate that even in the schematic simulation environment, the performance of the designed PA is very sensitive to component tolerances. In some cases the variations of the component values degrade the gain down to 13 dB which is 6 dB less than the schematic simulation results.

3.7.1 Electromagnetic Simulation Results

Momentum simulation require continuous metallic layer in order to perform the simulation. Therefore whole circuit layout is divided into six parts which are all composed of distributed transmission lines. These six parts can be seen in Figure 19.

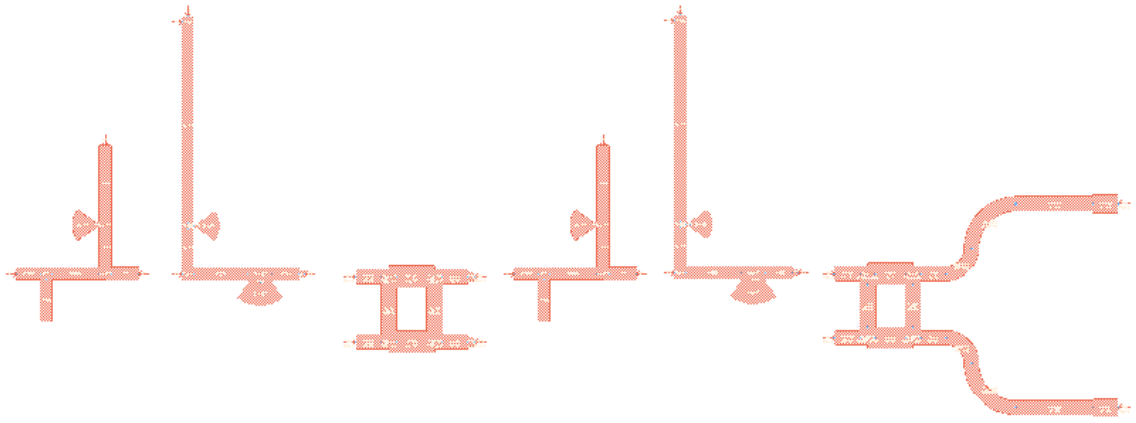


Figure 19 Simulated layout components of the PA circuitry

Each distributed transmission lines are simulated and tuned in order to match its corresponding schematic equivalent circuit. After reaching to the tuning limits, each simulation “s2p” files are added to the schematic design (which is originally used for schematic simulation) as data files while keeping the lumped elements and other circuitry. The Momentum simulation results are presented in Figure 20.

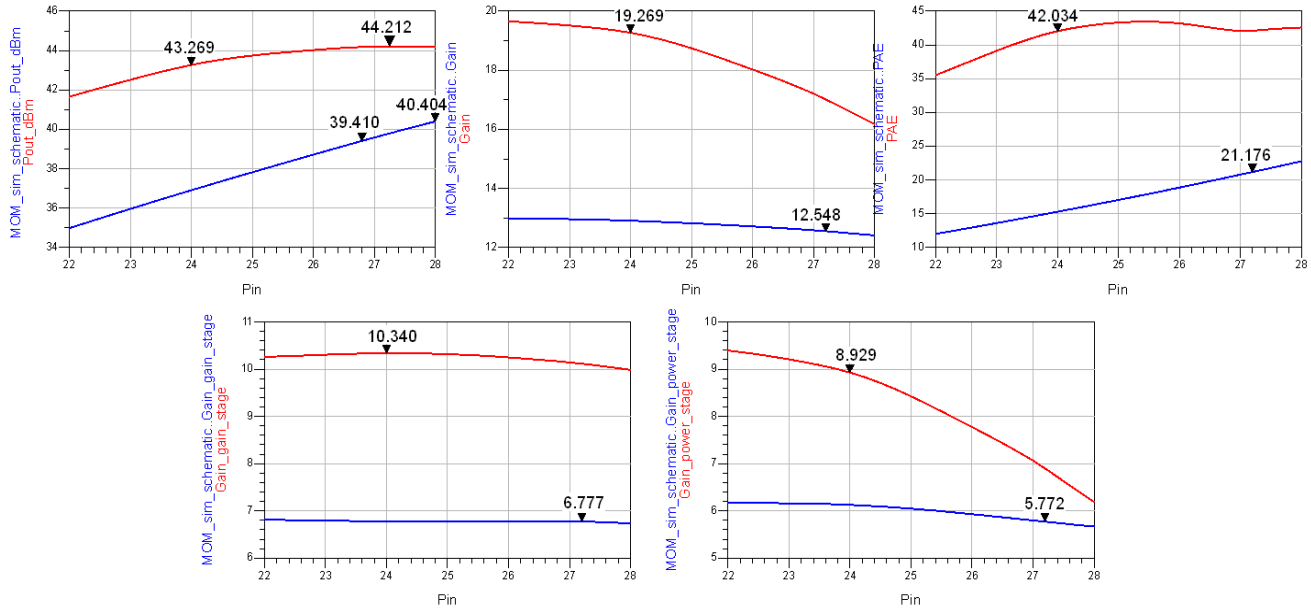


Figure 20 Schematic and Momentum simulation results

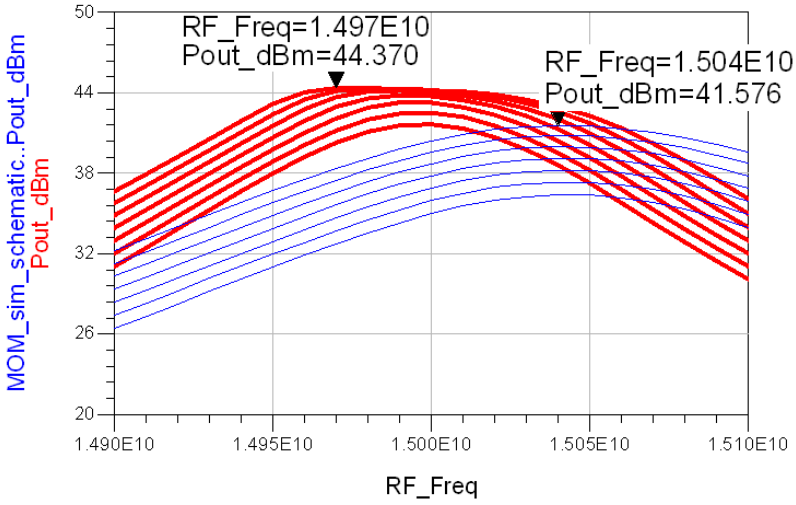


Figure 21 Frequency sweep with input power varying from 22 dBm to 28 dBm

Momentum simulation results indicate that, at 15 GHz the maximum output power of the PA is decreased more than 3 dB. In addition, gain has also decreased 7 dB at 15 GHz. Contributions to the total gain from the gain stage and power stage is 6.77 dB and 5.77 dB. In order to investigate the frequency shift a frequency sweep simulation is also

performed from 14.90 GHz to 15.10 GHz with varying input power from 22 dBm to 28 dBm. The frequency sweep simulation results are presented in Figure 21.

The large difference between schematic simulation and the electromagnetic simulation presented in Figure 20 and the results of the Monte-Carlo simulations clearly indicate that the fabricated PA is very sensitive.

3.8 Layout

The designed power amplifier is composed of 2 stages. First stage is the gain stage where it is designed for high gain to drive the power stage. Power stage is designed using balanced topology by the means of a $3\,dB$ branch line coupler which is described in section 3.7. The used stabilization and bias network are described in section 3.4 and section 3.5 respectively. In addition matching networks that are included in the layout for both gain and the power stages are described in section 3.6.

The final layout of the 15 GHz power amplifier is shown in Figure 22. . The size of the final layout is 74.5 mm x 94.5 mm.

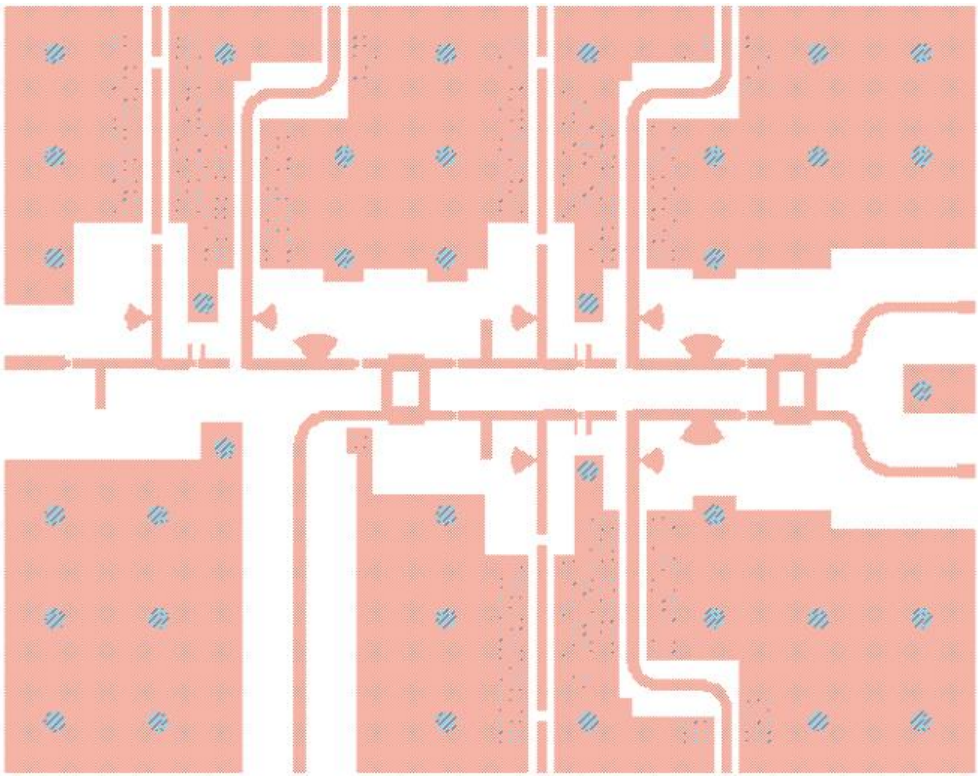


Figure 22 The layout of the PA

Apart from the PA layout, where both gain and power stages are present, a separate layout with only gain stage has also been manufactured. Layout of the gain stage of the PA is depicted in Figure 23. The size of the gain stage layout is 63.5 mm x 43 mm. This separate PA is used for assessing the performance of the gain stage separately from the whole PA board, which can be considered more complex than single stage amplifier.

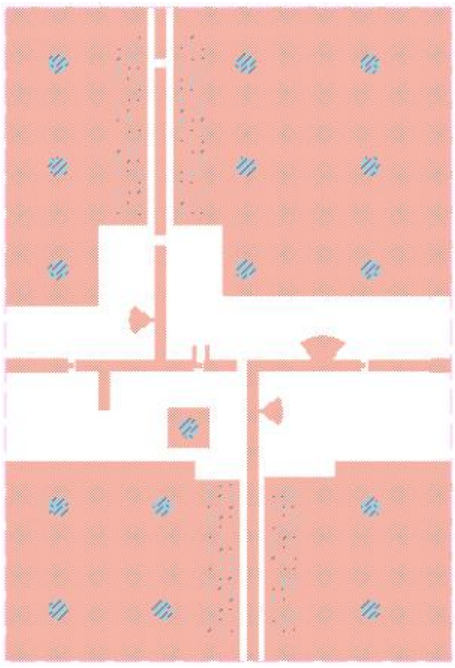


Figure 23 The layout of the gain stage of the PA

4. Implementation and Measurements

4.1 Implementation of the power amplifiers

The PA and gain stage PA are both implemented on Rogers 5870 substrate with ε=2.33 and thickness of 0.381 mm. In order to mitigate the effects of the transistor parasitics, a bare-die mounting approach of the GaN-HEMT transistor is used.

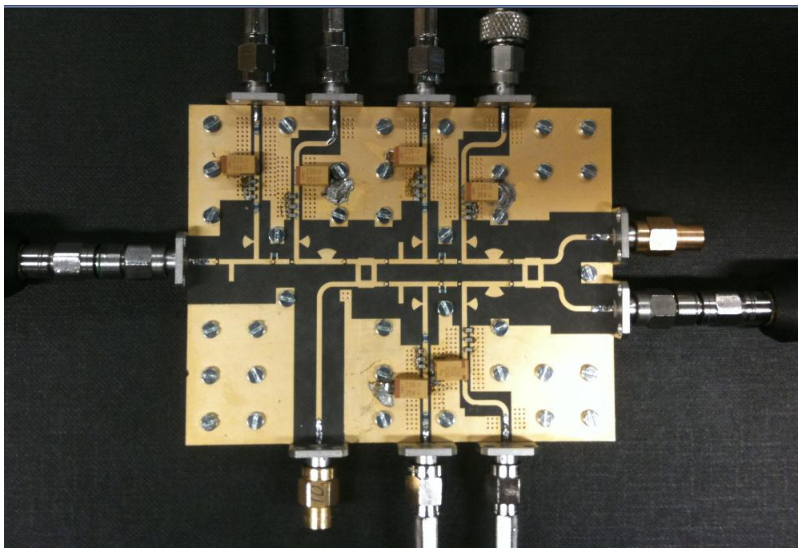


Figure 24 Photo of the manufactured PA

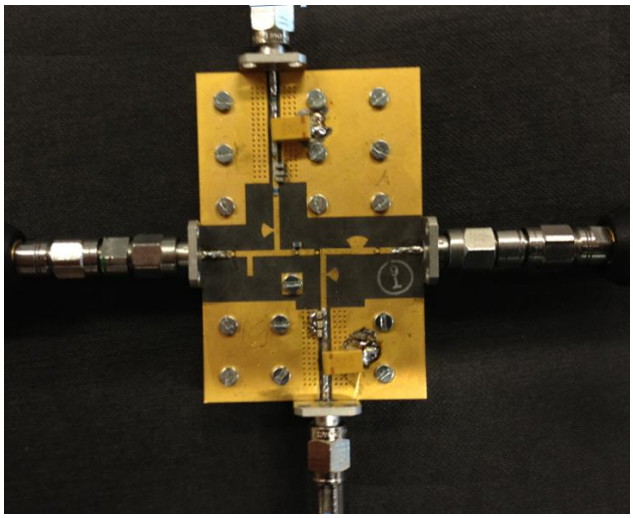


Figure 25 Photo of the manufactured gain stage of the PA

The bare-die transistors are mounted on a ridge of 0.32 mm thickness on brass fixture. The transistor chips are then attached to the PCBs using gold wire bonding [7]. Manufactured PAs are presented in Figure 24 and Figure 25 respectively.

4.2 Small Signal Measurements

In order to characterize the manufactured PAs, small signal (S-parameter) measurements have been performed using vector network analyzer and a dc source for biasing the devices. Thus the possible frequency shift can be analyzed prior to the large signal measurement.

The drain voltage of $V_{DS} = 28\,V$ is applied to both PAs. Gate voltage is tuned to obtain drain current of $I_D = 150\,mA$. The measured and simulated S-parameters of the gain stage of the PA are reported in Figure 26. Results indicate the disagreement between the two s-parameter results from ADS simulation and S-parameter measurement of the gain stage of the PA, both in frequency shift and amplitude.

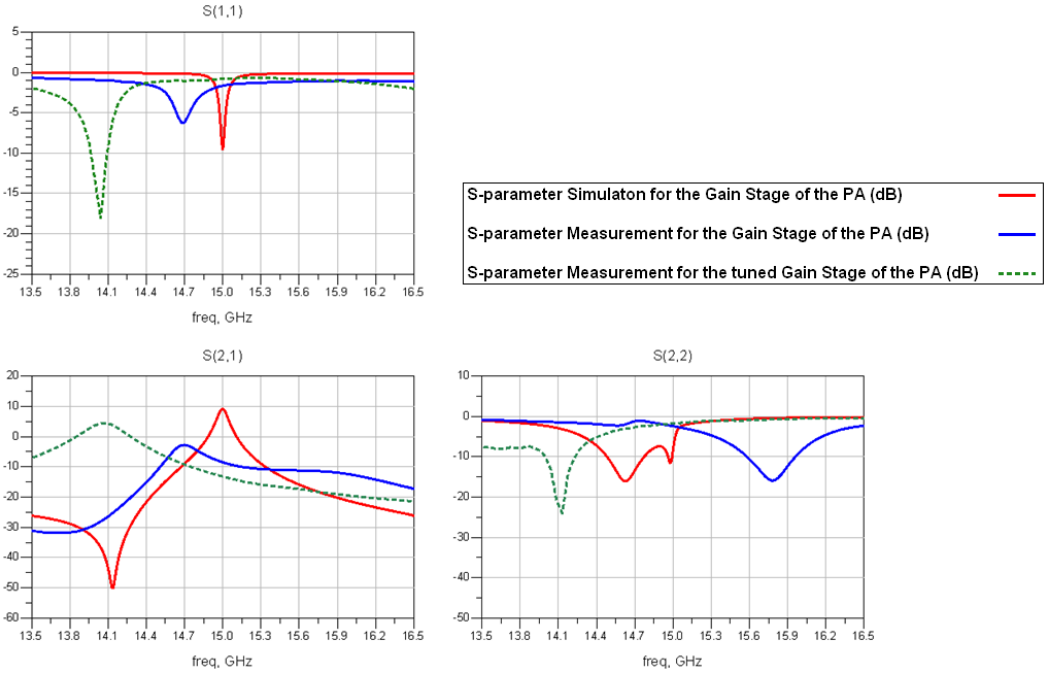


Figure 26 S-parameter simulation and measurement results for the gain stage PA

This result is expected due to the PA dependency on component and manufacturing tolerance, as presented in section 3.7.3 Monte-Carlo simulation results. The PA is designed to operate at frequency of 15 GHz. However, according to the measured results the frequency shift for S(1,1) is 0.3 GHz and for S(2,2) is 0.7 GHz. This disagreement in frequency shift results in degradation in S(2,1).

Therefore, the gain stage of the PA requires tuning in order to match the small signal measurement to the S-parameter simulation values. This is performed using copper foil. Both input and output matching network elements, such as open stubs and transmission lines, are tuned with copper foil. The result of this operation is presented in Figure 26 via dotted green lines. The results indicate that the frequency is matched at 14.09 GHz. The total frequency shift is more than 1 GHz. On the other hand, the adjustment of the matching networks improved both S(1,1) and S(2,2) which resulted in improvement of S(2,1), which is measured 4.4 dB.

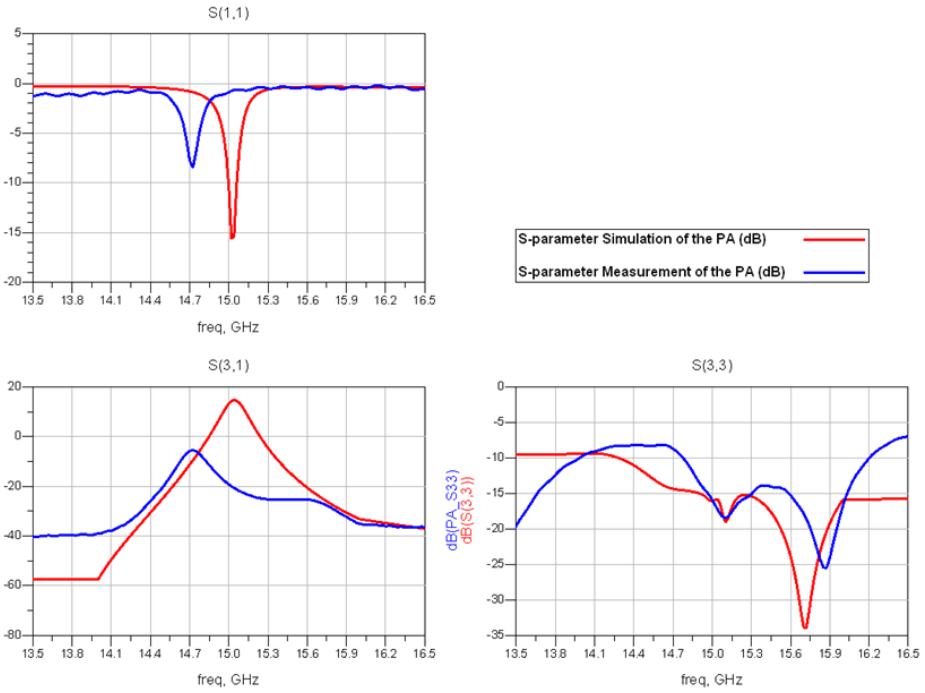


Figure 27 S-parameter simulation and measurement results for the PA

Figure 27 shows, small signal simulation and measurements where the red line depicts the S-parameter simulation and blue line depicts S-parameter measurement of the PA. Obtained results are worse than expected for the PA since the S-parameter simulation and measurement results for the gain stage of the PA show that the gain stage does not provide enough gain to for the power stage. Results show that there is both shift in frequency and decrease in amplitude for S(1,1) and S(3,1). Return loss, S(3,3), in this case has better performance compared to the return loss, S(2,2), of the gain stage. This is due to the wide bandwidth of the designed 3-dB BLC.

4.3 Large Signal Measurement

In order to measure the performance of the PA in terms of output power, gain and efficiency, large signal measurement is performed. The CW is generated by a vector signal generator to simulate the signal at different frequencies and the output power of

the PA is measured by a power meter. The measurement set up is illustrated in Figure 28.

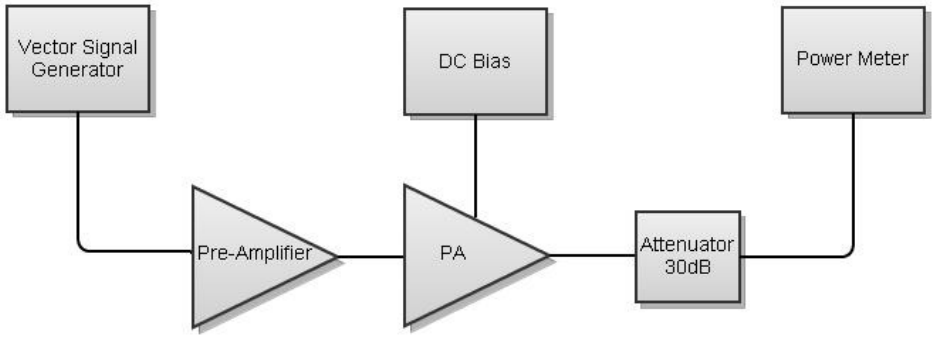


Figure 28 Large measurement set up illustration

The pre-amplifier is used to increase the power of the CW signal generated in the vector signal generator, allowing enough input power to drive the gain stage of the PA. The pre-amplifier has 48 dB gain from 12 GHz to 18 GHz. 30 dB attenuator is used to protect the power meter sensor from high power. A picture of the set up is presented in Figure 29.

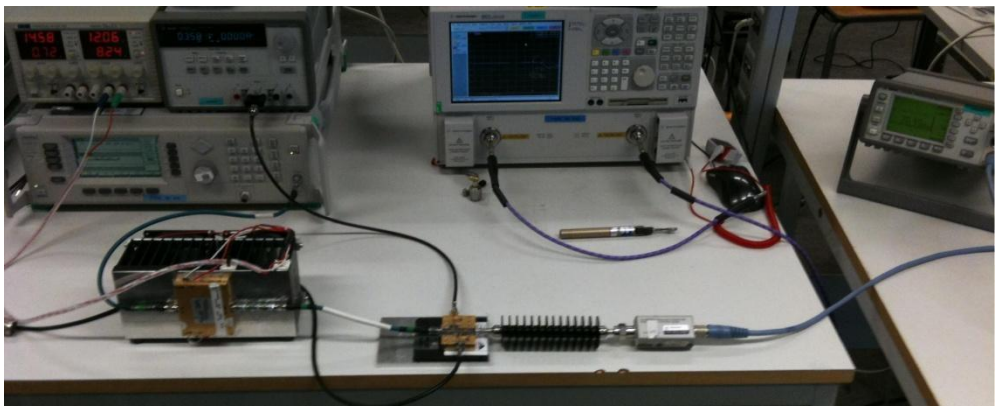


Figure 29 Large signal measurement set up

Pre-amplifier and the attenuator have different responses versus frequency. Therefore a calibration process is performed for input power sweep and frequency sweep measurements separately. For input power sweep required calibration is done by calculating the offset values so that during measurement, actual input power at the PA can be set from 10 dBm to 25 dBm with steps of 1 dB from 10 dBm to 20 dBm and 0.5 dB from 20.5 dBm to 25 dBm. Similar calibration procedure is performed for frequency sweep measurement. However in this case, frequency response of the set up is measured to calculate the offset values required so that the actual input power at the PA can be 24 dBm for each frequency of concern. The calibration is performed with different frequency steps so that obtained values are more precise. The frequency steps

are 20 MHz from 13.80 GHz to 14 GHz, 10 MHz from 14 GHz to 14.1 GHz and 20 MHz 14.12 GHz to 14.30 GHz.

Both measurements are performed only for the gain stage of the PA because it is tuned with copper foils during the small signal measurements. Applied drain bias voltage for the gain stage of the PA is $V_{DS} = 28\,V$ and the gate voltage is tuned to $V_{GS} = -3.616\,V$ to obtain drain current of $I_D = 100\,mA$.

According to the small signal measurement the highest power is obtained is at 14.09 GHz. Therefore in order to verify the obtained frequency value, frequency sweep measurement is performed. Measurement results are depicted in Figure 30. The results presents the PAE, drain efficiency (DE) and gain response of the gain stage versus frequency. The measurement results show that the maximum gain and efficiency occurs at 14.09 GHz. The gain stage of the PA provides approximately 3.5 dB gain at 14.09 GHz. It also provides more than 3 dB gain between 14 GHz to 15.2 GHz with gain flatness of 0.5 dB. Figure 30 also shows that the drain efficiency of the gain stage of the power amplifier is around 13%. Although measured values are less than the initial simulation results presented in Chapter 3.7, it provides that some gain at Ku-band for the designed hybrid integrated circuit power amplifier.

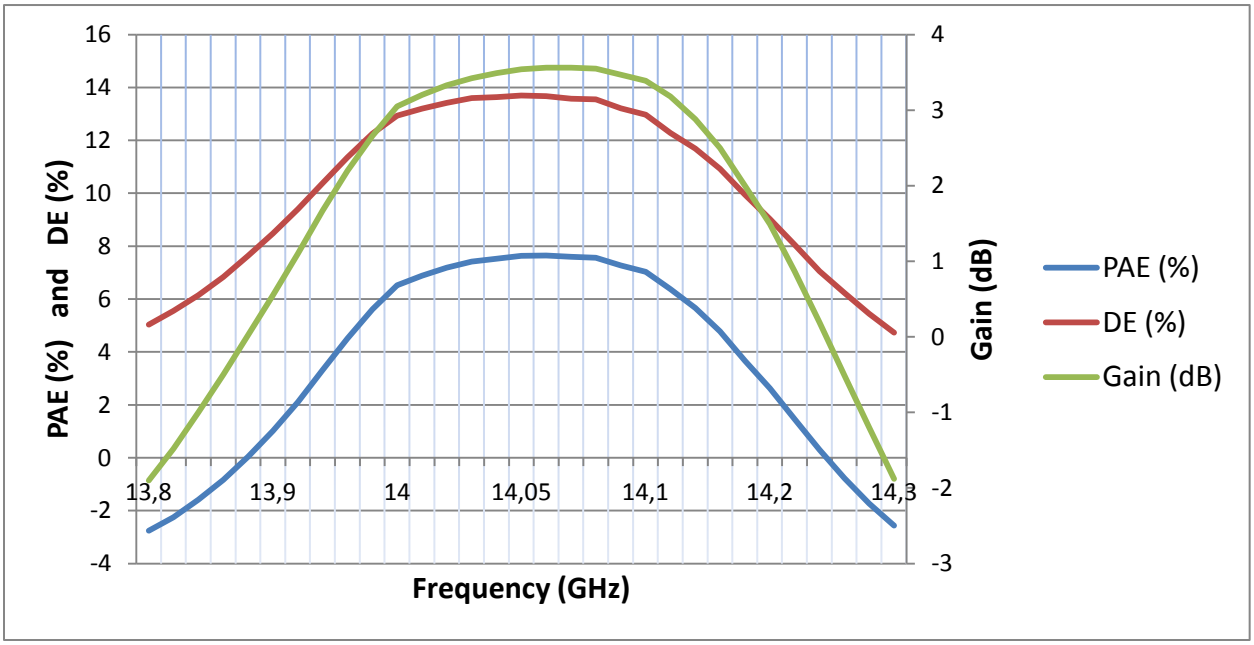


Figure 30 Measured gain and PAE vs. frequency for the gain stage of the PA

The other measurement that is performed is the power sweep measurement. According to the small signal and frequency sweep measurements maximum gain is obtained at 14.09 GHz. Obtained results are presented in Figure 31.

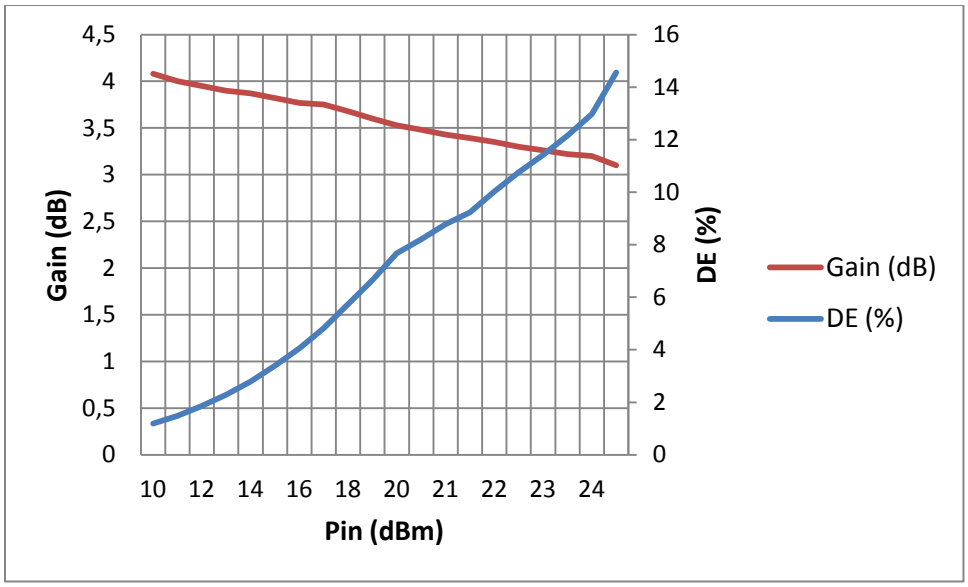


Figure 31 Measured gain and PAE vs. input power for the gain stage of the PA

The maximum measured gain at 14.09 GHz is 4.08 dB at 10 dBm of input power and at 24 dBm of input power measured gain is 3.2 dB. Measured gain values when compared to the electromagnetic simulation results show that there is around 3 dB difference. On the other hand measured DE is less than expected. However, it can be noticed that the DE is not saturated. This means that the gain stage of the PA can be tuned further to provide more gain.

4.3 Discussion

Implementation of the power amplifiers were done with single layer capacitors, since standard film capacitors did not resonate around 15 GHz. This resulted different lumped component technologies to be present on the same board. This inconsistency also affected the physical design of the power amplifier. For example, as it can be seen in Figure 11 single layer capacitor used in the stability network has a dimension of 0.685 mm in length and width while the thick film resistor used in the same network has a dimension of 1.6 mm in length and 0.8 mm in width. Therefore some extra microstrip transmission lines are used to combine these two elements. This approach may be useful in lower frequencies such as L-band, but at Ku-band transmission line width differences may have caused some mismatch. This mismatch could have caused degradation in performance. Therefore if single layer resistors were also used, the stability network could have been mounted on the $50\,\Omega$ transmission line, without the need for extra transmission lines.

The small signal measurement showed that the S11 and S22 have unexpectedly been shifted to opposite directions. This may depend on the manufacturing tolerances of the distributed and lumped elements. On the other hand, it also made the tuning more

diffucult apart from the process itself, considering the size of the board limited the space to place the copper foils. That is the reason why after tuning, the gain stage resulted around 14 GHz.

According to the datasheet of the used GaN-HEMT, device provides 6.6 dB gain and 41 % PAE at 14 GHz. Therefore the fabricated gain stage large signal measurement results are acceptable. However during the schematic simulations obtained gain was around 19 dB with 43 dBm of output power. This also indicates, that the used model is not very accurate.

The obtained results compared to published papers on power amplifiers at Ku-band is circled in Figure 33. However, it should be noticed that all of these power amplifiers are designed with MMIC technology. Moreover, if the power stage can be tuned to provide enough gain, the designed PA can be comparable to the published power amplifiers.

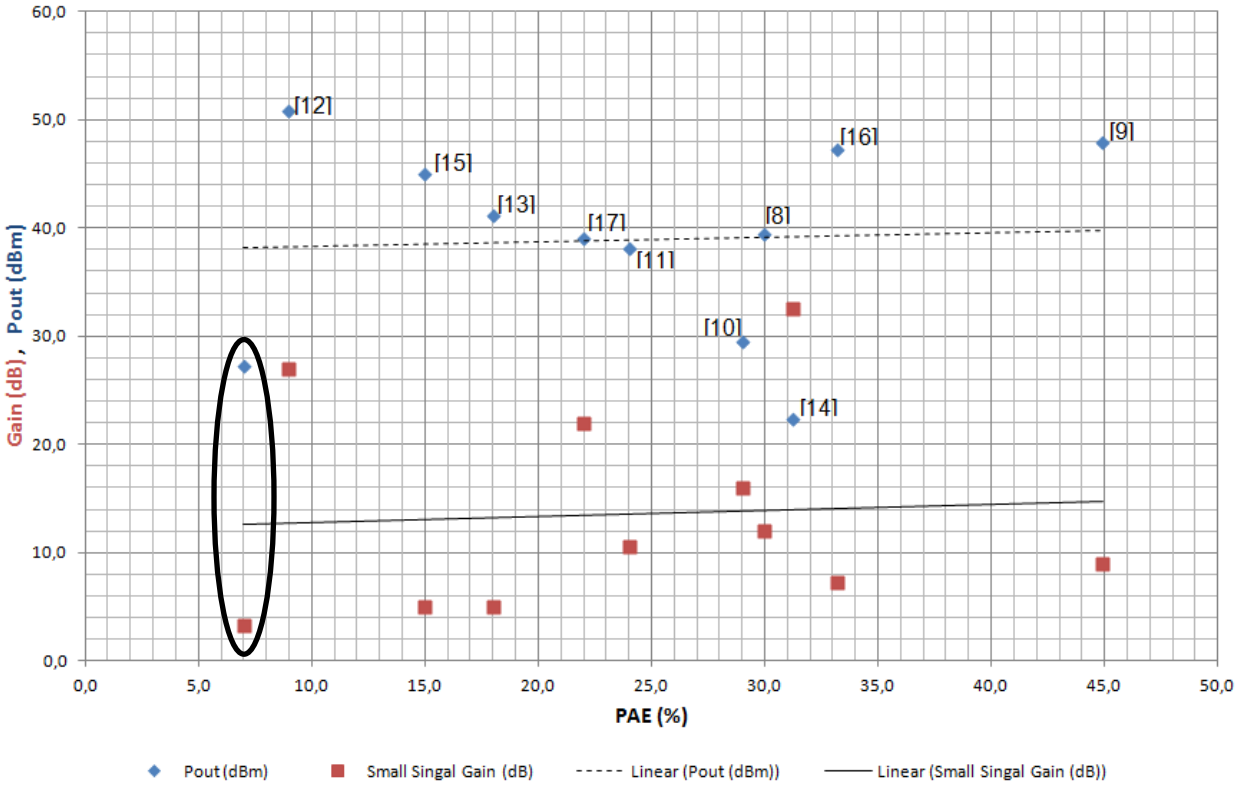


Figure 32 Published Ku-band power amplifiers

5. Conclusions and Future Work

Bare die GaN-HEMT and obtained transistor model is used to the design a two stage Ku band power amplifier. The design approach is based balanced topology drived by a gain stage using the same device.

Load-pull measurement has been performed in order to obtain source and load impedance values. However, due to the limitation of the tuners, no results were obtained. Therefore a transistor model is used throughout schematic design.

The design approach used in the stability network with parallel resistors and capacitor also provided reliable stability during the small signal and large signal measurements. However, since the used lumped element models in the schematic design were ideal, actual components affected the performance of the fabricated power amplifiers more than anticipated. On the other hand the circuitry used to connect the parallel film resistor should have been simpler; especially after the sensitivity of the PA from the Monte-Carlo simulations were observed.

Both schematic and electromagnetic simulations are used to provide estimation towards the actual measurement of the PA. The difference between both simulations indicated that the PA is very sensitive. This is also related to the difficulty in designing matching networks. The required source impedance is highly capacitive where 50 ohm has to be transformed to highly capacitive impedance. Therefore a slight change in matching networks decreased the performance of the PA. This conclusion was more obvious after performing the small signal measurement where the PA required tuning with copper foils. Therefore, using another GaN-HEMT device for future PA designs can be a solution to improve the performance of the PA.

However, the obtained values after tuning the gain stage of the PA can be considered acceptable. The maximum gain was 4 dB at low input power. If a rough estimation is made so that the power stage could be tuned to provide more than 3 dB, the total gain will be more than 7 dB at 14 GHz. This can be regarded as a high gain for hybrid integrated circuit power amplifier design at Ku-band. Therefore for future work both the gain stage of the PA and the power stage of the PA can be tuned to provide high gain at proper input power levels. On the other hand, the PA circuitry can be re-designed with a GaAs device that can act as a driver stage for the GaN-HEMT power stage according to proposed solutions

References

[1] I.D. Robertson, S. Lucyszyn, “RFIC and MMIC Design and Technology”, Institution of Engineering and Technology, February 2001.

[2] Mike Golio, “RF and Microwave Circuits, Measurements and Modeling”, 2nd ed., Jan 2008.

[3] Maury Microwave Corporation, “Automated Tuner System: PC Based Application Software”, Operating Manual, http://www.maurymw.com/.

[4] J. Stenarson, K. Yhland, “Automatic root selection for the unknown thru algorithm”, SP Swedish National Testing and Research Institute, Borås, Sweden, June 2006.

[5] G. Gonzales, “Microwave Transistor Amplifiers: Analysis and Design”, 2nd ed., 1997.

[6] M. Muraguchi, T. Yukitake, Y. Naito, “ Optimum Design of 3-dB Branch-Line Coupler Using Microstrip Lines”, IEEE Transactions on Microwave Theory and Techniques, vol. MTT-31, no. 8, August 1983.

[7] Paul Saad, Hossein Mashad Nemati, Kristoffer Andersson, Christian Fager, “Highly Efficient GaN-HEMT Power Amplifiers at 3.5 GHz and 5.5 GHz”, GigaHertz Centre, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden.

[8] C. H. Lin; H. Z. Liu; C. K. Chu; H. K. Huang; Y. H. Wang; C. C. Liu; C. H. Chang; C. L. Wu; C. S. Chang; , "A Fully Matched Ku-band 9W PHEMT MMIC High Power Amplifier," *Compound Semiconductor Integrated Circuit Symposium, 2006. CSIC 2006. IEEE* , vol., no., pp.165-168, Nov. 2006

[9] Yamauchi, Kazuhisa; Noto, Hifumi; Nonomura, Hiroyuki; Kunugi, Satoshi; Nakayama, Masatoshi; Hirano, Yoshihito; , "A 45% power added efficiency, Ku-band 60W GaN power amplifier," *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International* , vol., no., pp.1-4, 5-10 June 2011

[10] Noh, Y.S.; Yom, I.B.; , "Ku-band MMIC power amplifier with on-chip compensation gate bias circuit," *Microwave Conference, 2008. APMC 2008. Asia-Pacific* , vol., no., pp.1-4, 16-20 Dec. 2008

[11] Lin, C.-H.; Liu, H.-Z.; Chu, C.-K.; Huang, H.-K.; Liu, C.-C.; Chang, C.-H.; Wu, C.-L.; Chang, C.-S.; Wang, Y.-H.; , "A Compact 6.5-W PHEMT MMIC Power Amplifier for Ku-Band Applications," *Microwave and Wireless Components Letters, IEEE* , vol.17, no.2, pp.154-156, Feb. 2007

[12] Sumi, H.; Takahashi, H.; Soejima, T.; Mochizuki, R.; , "Ku-band, 120-W power amplifier using gallium nitride FETs," *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International* , vol., no., pp.1389-1392, 7-12 June 2009

[13] Masuda, S.; Akasegawa, A.; Ohki, T.; Makiyama, K.; Okamoto, N.; Imanishi, K.; Kikkawa, T.; Shigematsu, H.; , "Over 10W C-Ku band GaN MMIC non-uniform

distributed power amplifier with broadband couplers," *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International* , vol., no., pp.1388-1391, 23-28 May 2010

[14] Rasidah, S.; Rasmi, A.; Siti Maisurah, M.H.; Rahim, A.I.A.; Yahya, M.R.; , "3-stage 15 GHz p-HEMT power amplifier design for MMIC applications," *Electron Devices and Solid-State Circuits (EDSSC), 2010 IEEE International Conference of* , vol., no., pp.1-4, 15-17 Dec. 2010

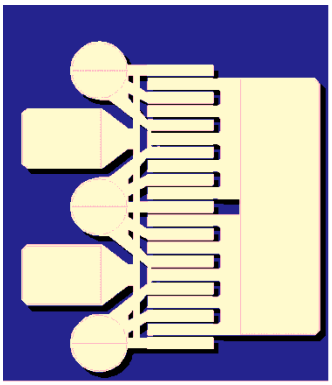
[15] Takagi, K.; Kashiwabara, Y.; Masuda, K.; Matsushita, K.; Sakurai, H.; Onodera, K.; Kawasaki, H.; Takada, Y.; Tsuda, K.; , "Ku-band AlGaN/GaN HEMT with over 30W," *Microwave Integrated Circuit Conference, 2007. EuMIC 2007. European* , vol., no., pp.169-172, 8-10 Oct. 2007

[16] Takagi, K.; Takatsuka, S.; Kashiwabara, Y.; Teramoto, S.; Matsushita, K.; Sakurai, H.; Onodera, K.; Kawasaki, H.; Takada, Y.; Tsuda, K.; , "Ku-band AlGaN/GaN-HEMT with over 30% of PAE," *Microwave Symposium Digest, 2009. MTT '09. IEEE MTT-S International* , vol., no., pp.457-460, 7-12 June 2009

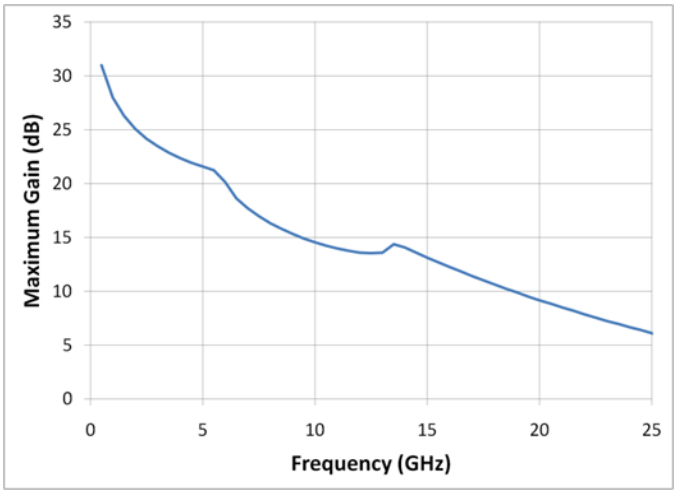
[17] Qi Zhang; Brown, S.A.; , "Fully monolithic 8 watt Ku-band high power amplifier," *Microwave Symposium Digest, 2004 IEEE MTT-S International* , vol.2, no., pp. 1161- 1164 Vol.2, 6-11 June 2004

Appendix A: TriQuint GaN- HEMT transistor data sheet

12 Watt Discrete Power GaN on SiC HEMT



Bias conditions: Vd = 28 V, Idq = 250 mA, Vg = -3.6 V Typical



Key Features

- Frequency Range: DC - 18 GHz
- 41 dBm Nominal Psat at 3 GHz
- 58% Maximum PAE
- 18 dB Nominal Power Gain
- Bias: Vd = 28 - 32 V, Idq = 250 mA, Vg = -3.6 V Typical
- Technology: 0.25 um Power GaN on SiC
- Chip Dimensions: 0.82 x 0.92 x 0.10 mm

Primary Applications

- Defense & Aerospace
- Broadband Wireless

Product Description

The TriQuint TGF2023-02 is a discrete 2.5 mm GaN on SiC HEMT which operates from DC-18 GHz. The TGF2023-02 is designed using TriQuint's proven 0.25um GaN production process. This process features advanced field plate techniques to optimize microwave power and efficiency at high drain bias operating conditions.

The TGF2023-02 typically provides 41 dBm of saturated output power with power gain of 18dB at 3 GHz. The maximum power added efficiency is 58% which makes the TGF2023-02 appropriate for high efficiency applications.

Lead-free and RoHS compliant

.

Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd	Drain Voltage	40 V	2/
Vg	Gate Voltage Range	-50 to 0 V	
Vdg	Drain-Gate Voltage	80 V	
Id	Drain Current	2.5 A	2/
Ig	Gate Current	14 mA	
Pin	Input Continuous Wave Power	34 dBm	2/
Tch	Channel Temperature	200 °C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter	Value
Vd	Drain Voltage	28 - 32 V
Idq	Drain Current	250 mA
Id_Drive	Drain Current under RF Drive	750 mA
Vg	Gate Voltage	-3.6 V

Table III
RF Characterization Table 1/

Bias: Vd = 28 V, Idq = 250 mA, Vg = -3.6V Typical

SYMBOL	PARAMETER	3 GHz	6 GHz	10 GHz	14 GHz	UNITS
Power Tuned:						
Psat	Saturated Output Power	41	40.3	40.2	38.8	dBm
PAE	Power Added Efficiency	58	56	50	41	%
Gain	Power Gain	18.1	12.3	9.9	6.6	dB
Efficiency Tuned:						
Psat	Saturated Output Power	39.7	38.6	39.9	38.8	dBm
PAE	Power Added Efficiency	64	64	52	42	%
Gain	Power Gain	17.4	12.9	10.2	6.5	dB

SYMBOL	PARAMETER	3 GHz	6 GHz	10 GHz	14 GHz	UNITS
Power Tuned:						
Rp 2/	Parallel Resistance	79.3	81.9	61.5	49.9	Ω·mm
Cp 2/	Parallel Capacitance	0.524	0.348	0.426	0.432	pF/mm
Efficiency Tuned:						
Rp 2/	Parallel Resistance	153	171	72.1	53.1	Ω·mm
Cp 2/	Parallel Capacitance	0.426	0.372	0.414	0.472	pF/mm

1/ Values in this table are engineering estimates scaled from measurements on the 1.25 mm GaN/SiC unit cell (see TGF2023-01 datasheet)

2/ Large signal equivalent output network (normalized) (see figure, pg 7)

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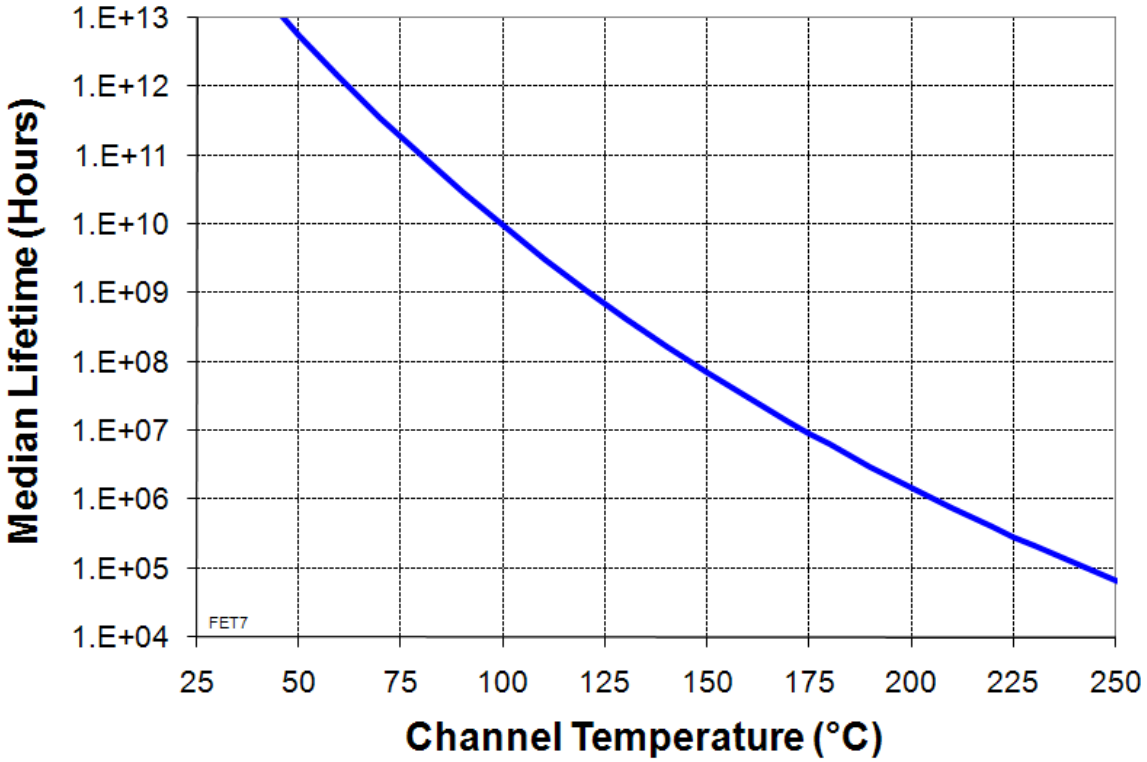
Table IV
Power Dissipation and Thermal Properties 1/

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 70 ºC	Pd = 16.2 W Tchannel = 200 ºC Tm = 1.5E+6 Hrs	2/
Thermal Resistance, θjc	Vd = 28 V Id = 250 mA Pd = 7 W Tbaseplate = 70 ºC	θjc = 8.0 (ºC/W) Tchannel = 126 ºC Tm = 6.4E+8 Hrs	
Thermal Resistance, θjc Under RF Drive	Vd = 28 V Id = 763 mA Pout = 41 dBm Pd = 9.0 W Tbaseplate = 70 ºC	θjc = 8.0 (ºC/W) Tchannel = 142 ºC Tm = 1.5E+8 Hrs	
Mounting Temperature	30 Seconds	320 ºC	
Storage Temperature		-65 to 150 ºC	

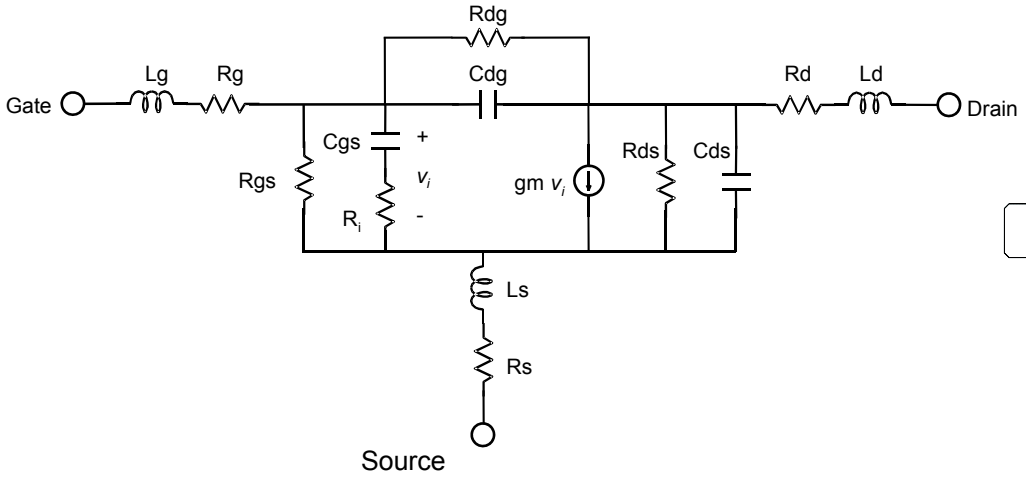
1/ Assumes eutectic attach using 1mil thick 80/20 AuSn mounted to a 10mil CuMo Carrier Plate

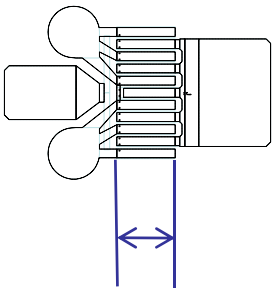
2/ Channel operating temperature will directly affect the device median lifetime. For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

Median Lifetime vs Channel Temperature



Linear Model for 1.25 mm Unit GaN Cell (UGC)



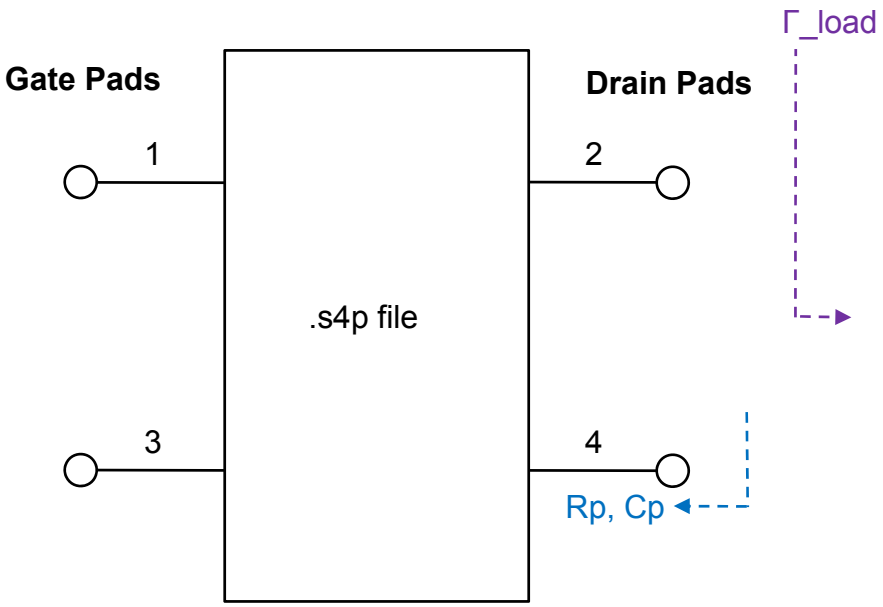


Unit GaN cell (UGC)
Reference Plane

MODEL PARAMETER	Vd=28V Idq=125mA	UNITS
Rg	0.78	Ω
Rs	0.13	Ω
Rd	1.28	Ω
gm	0.270	S
Cgs	1.79	pF
Ri	0.26	Ω
Cds	0.308	pF
Rds	123.6	Ω
Cgd	0.064	pF
Tau	2.78	pS
Ls	0.0058	nH
Lg	-0.013	nH
Ld	0.018	nH
Rgs	8900	Ω
Rgd	1730000	Ω

Complete 2.5mm GaN HEMT Linear Model

Includes 2 UGC, 3 vias, and 4 bonding pads



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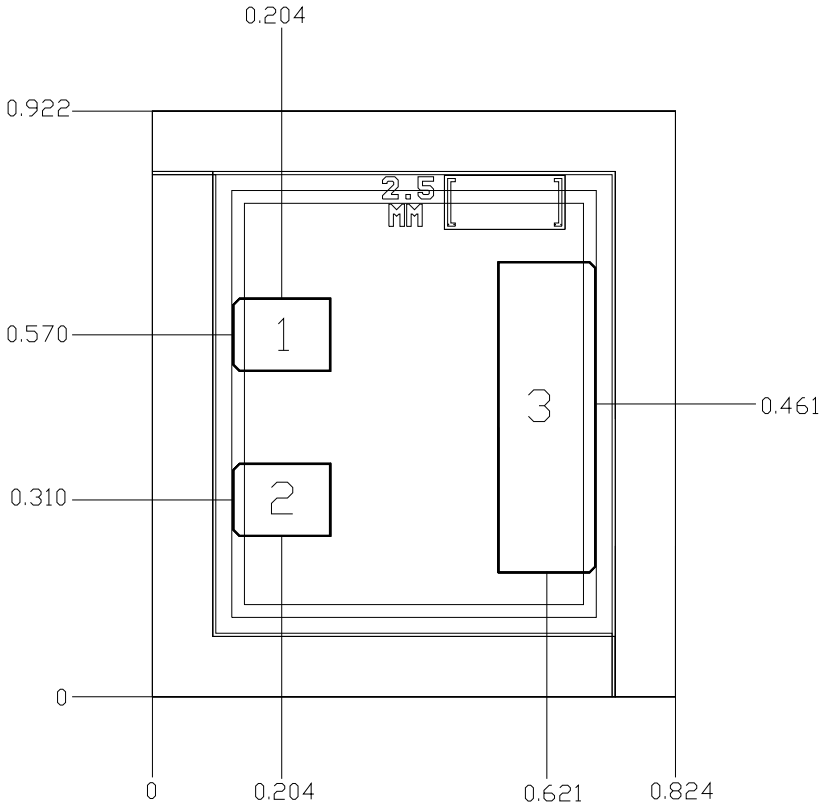
Mechanical Drawing



Units: millimeters

Thickness: 0.100

Die x,y size tolerance: +/- 0.050

Chip edge to bond pad dimensions are shown to center of pad

Ground is backside of die

Bond Pad #1, #2	Vg	0.154 x 0.115
Bond Pad #3	Vd	0.154 x 0.490

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Ball bonding is the preferred interconnect technique, except where noted on the assembly diagram.
- Force, time, and ultrasonics are critical bonding parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Ordering Information

Part	ECCN	Package Style
TGF2023-02	EAR99	GaN on SiC Die

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