THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Control of Voltage Source Converters for Voltage Dip Mitigation in Shunt and Series Configurations

MASSIMO BONGIORNO

Department of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
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MASSIMO BONGIORNO

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Department of Electric Power Engineering
Chalmers University of Technology
SE–412 96 Göteborg
Sweden
Telephone +46 (0)31–772 1000

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To my uncle and friend Filippo

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MASSIMO BONGIORNO
Department of Electric Power Engineering
Chalmers University of Technology

Abstract

Custom Power is the application of power electronics to improve the quality of power distribution for sensitive industrial plants. Industries reporting production stops due to voltage disturbances, like short interruptions and voltage dips, include paper mills, semiconductors facilities and other industries with fully automated production. Voltage dips are sudden drops in voltage, with duration between half a cycle and some seconds, mostly caused by clearing of short-circuit faults in the power system. Power electronic converters connected in shunt or series with the grid and equipped with energy storage can provide protection of sensitive processes against voltage dips. This thesis focuses on the control of Voltage Source Converter (VSC) connected in series or in shunt with the grid for mitigation of voltage dips. In both configurations, the core of the controller is the current controller. Since most voltage dips are unbalanced and have short duration, decisive factors for successful compensation are high speed of response and capability of handling unbalances. Three different algorithms for current control of VSC under unbalanced voltage conditions are presented and analyzed in detail. These algorithms include time delay compensation and reference voltage limitation with feedback, to improve the current control during overmodulation. Stability analysis of all three controllers is carried out. Different methods for sequence component detection are presented and compared, based on their transient performance. Simulations and experimental results on a 69-kVA prototype are presented and discussed for all three controllers. For use in a series-connected VSC, the three current controllers are completed with an outer voltage loop, thus realizing three cascade controllers that are presented and analyzed in detail. For all three controllers, stability analysis and simulation results with balanced and unbalanced voltage dips are also presented. The three controllers have been tested on a prototype series compensator and experimental results are presented in this thesis. Design and testing of the protection system for the series-connected VSC is also described in detail. Experimental results with non-linear load (diode rectifier) are shown. Finally, a similar cascade controller for voltage dip compensation with shunt-connected VSC is presented and tested via simulations. To improve the performance, a modified configuration including an LCL-filter between the VSC and the grid is proposed. It is also shown that by adding an active damping term in the inner current controller, undesired resonances between the filter components can be overcome and satisfactory mitigation of voltage dips can be achieved. A drawback is the high amount of injected current required if the grid is strong at the point of connection of the VSC.

Index Terms: Power Electronics, Power Quality, Current Controller, Voltage Dip (Sag), Voltage Source Converter (VSC).

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Massimo Bongiorno
Gothenburg, Sweden
November, 2004

Contents

Chapter 1

Introduction

1.1 Background and motivation

Since some years, novel power electronic controllers, called *Custom Power devices*, have been introduced to improve the quality of power distribution in industrial plants [23], in response to growing demand from industries reporting production stops due to voltage disturbances, like short interruptions and voltage dips. These power quality phenomena are normally caused by clearing short-circuit faults in the power system and, despite their very short duration, can impact the operation of low-power electronic devices, motor contactors, and drive systems [33][15][57][14]. Among the most sensitive industries are paper mills [11], semiconductors facilities [17] and other industries with fully automated production, where the sensitivity of electronic equipment to voltage disturbances can cause the stoppage of the whole facility. To solve this problem, several different custom power devices have been proposed, many of which have at their heart a Voltage Source Converter (VSC) connected to the grid. Voltage dips can be mitigated by injecting a voltage into the grid with a series-connected VSC. The injected voltage adds up to the supply voltage during the dip. This device, known with the commercial name of Dynamic Voltage Restorer (DVR), has been applied successfully in a number of facilities around the world, e.g. a yarn manufacture [60], semiconductor plants [62][16], a food plant in Australia [61], and a large paper mill in Scotland [11]. Alternatively, the VSC can be connected to the grid in shunt. This device, called distribution STATCOM or D-STATCOM, injects a controllable current in the grid. By injecting a current in the point of connection, a shunt-connected VSC can also boost the voltage in that point during a voltage dip.

In both cases, the VSC must be controlled properly to inject the necessary voltage (in series connection) or current (in shunt connection) into the grid in order to compensate for the voltage dip. Since some sensitive loads can shut down because of a dip that lasts some hundreds of ms, the speed of response of the device is a decisive factor for successful compensation. Moreover, most voltage dips are unbalanced, and therefore another requirement for successful dip compensation is a fast detection of the grid voltage unbalance and a high-performance control of the VSC.

A high-performance vector current controller (VCC) for the VSC, such as the one presented in

[41], can control the active and reactive currents of the VSC independently with a high bandwidth. As a result, the currents are sinusoidal, free from low-order harmonics, and the reactive power can be controlled, e.g. to maintain a desired power factor. However, the VCC designed as in [41] by only considering positive-sequence components can provide high performance during normal operating conditions of the grid, but will not perform well under unbalance conditions [19]. Different current controllers have been proposed, which use sequence components to deal with unbalanced grid conditions. In reference [44], positive and negative sequence components are separated, but only the positive sequence is controlled by the VCC. However, the method to detect the sequence components is not described, and no discussion is included on the impact of the sequence detection method on the overall performance of the controller. Reference [50] uses two separate VCCs for the two sequence components, but the performance is shown only under steady state unbalance of the grid.

Control of the series-connected VSC for voltage dip mitigation has been treated, among others, in [6] and [39]. Reference [6] develops a cascade controller, with an inner current control loop and an outer voltage control loop, which is capable of mitigating unbalanced voltage dips. However, the emphasis is more on system aspects than on a detailed analysis of the controllers. Reference [39] presents the design and control of a full-size series compensator for medium voltage applications. With the configuration adopted, based on three H-bridges sharing the same DC link, individual control of each phase is possible and therefore separation and independent control of sequence components is not necessary. The drawback is that double the amount of valves are required.

1.2 Aim and outline of this thesis

The aim of this thesis is to improve, analyze and test, both via simulation and experiments, different control algorithms for VSC, which are suitable for mitigation of unbalanced voltage dips for both series- and shunt-connected configurations of the VSC. Chapter 2 of the thesis gives an overview of voltage dips, of their causes and effects, and of possible mitigation methods. Three different algorithms for current control of VSC under unbalanced voltage conditions are presented and analyzed in detail in Chapter 3. These algorithms include time delay compensation and reference voltage limitation with feedback, to improve the current control during overmodulation. Stability analysis of all three controllers is included. A few different methods for sequence component detection are presented and compared based on their transient performance, which is obviously of utmost importance since the target application is to detect unbalanced voltage dips. Chapter 3 also includes simulation results of all three controllers. Experimental results of all three controllers, obtained on a prototype built in the Power System Laboratory of Chalmers University of Technology, are presented in Chapter 4. The three current controllers presented in Chapter 3 are completed with an outer voltage loop for use in series-connected configuration, thus realizing three cascade controllers presented and analyzed in detail in Chapter 5. Simulation results for all three controllers are also presented, together with stability analysis of the three controllers. The three cascade controllers have been tested on a prototype series compensator built in the Power System Laboratory. This included also

design and testing of a protection system for the series-connected VSC. Experimental results are reported in Chapter 6. In Chapter 7, a controller for voltage dip compensation with shunt-connected VSC is presented and tested via simulations. A modified configuration including an LCL-filter between the VSC and grid is proposed to improve the performance. Conclusions and suggestions for future work are given in Chapter 8.

Chapter 2

Voltage dips and mitigation methods

2.1 Introduction

The utilities' aim is to continuously provide their customers with an ideal sinusoidal voltage waveform, i.e. a voltage with constant magnitude at the required level and with a constant frequency. In case of three-phase operation, the voltages should be symmetric.

Unfortunately, due to power system variations under normal operation and to unavoidable events like short-circuit faults, the supply voltage never complies with the above mentioned requirements. On the other hand, utilities require that the customers draw sinusoidal current from the main supply.

The term "power quality" has arisen trying to clarify duties of utilities and customers versus each other. The interest in power quality has increased in the latest years, especially due to the increased number of electronic devices in industrial plants.

This chapter will present an overview of the power quality problems and especially of voltage dips, which are generally considered the most severe issue for electronic-based equipments [33]. Moreover, different solutions for voltage dip mitigation, like power system improvements, improvement of the load immunity and installation of mitigation devices will be treated.

2.2 Voltage dips

According to IEEE Std.1159-1995 [25], a voltage dip is defined as a decrease between 0.1 to 0.9 pu in the RMS voltage at the power frequency with duration from 0.5 cycles to 1 minute. A voltage dip can be caused by different events that can occur in the power system like transformer energizing, switching of capacitor banks, starting of large induction motors and short-circuit faults in the transmission and distribution system. In this report, only voltage dips due to short-circuits will be considered.

To quantify the magnitude and the phase of a voltage dip in a radial system, due to a three-phase fault, the simplified voltage divider model shown in Fig.2.1 can be used [9]. In this system,

two impedances are connected to the point of common coupling (PCC): the grid impedance, denoted with $\overline{Z}_{\mathrm{g}}$, which includes everything above the PCC, and the fault impedance $\overline{Z}_{\mathrm{f}}$, which represents the impedance between the fault and the PCC. The load is connected to the PCC through a transformer and its voltage is denoted as $\overline{E}_{\mathrm{l}}$. The source voltage is denoted by $\overline{E}_{\mathrm{s}}$. The voltage $\overline{E}_{\mathrm{g}}$ at the PCC during the fault is given by [9]

$$\overline{E}_{\mathrm{g}} = \frac{\overline{Z}_{\mathrm{f}}}{\overline{Z}_{\mathrm{f}} + \overline{Z}_{\mathrm{g}}} \overline{E}_{\mathrm{s}} \tag{2.1}$$

From Eq.(2.1) it is possible to observe that the voltage dip magnitude depends on the fault location (since the impedance $\overline{Z}_{\mathrm{f}}$ depends on the distance between the point in the power system where the fault occurs and the PCC) and the grid impedance. The argument of the voltage vector $\overline{E}_{\mathrm{g}}$ during the voltage dip, called phase-angle jump, depends on the X/R ratio between the grid and the fault impedance and is given by

$$\psi = \arg(\overline{E}_{\mathrm{g}}) = \arctan\left(\frac{X_{\mathrm{f}}}{R_{\mathrm{f}}}\right) - \arctan\left(\frac{X_{\mathrm{g}} + X_{\mathrm{f}}}{R_{\mathrm{g}} + R_{\mathrm{f}}}\right) \tag{2.2}$$

Equation (2.1) also shows that, in the ideal case of infinitely strong grid, where $\overline{Z}_{\mathrm{g}}$ is equal to zero, the voltage at the PCC will always be constant and independent on the fault location.

The duration of the dip is related to the tripping time of the protection device which controls the circuit breaker, denoted as CB in Fig.2.1. When the CB installed in the feeder where the fault occurs clears the fault, the voltage is restored for the rest of the system. This results in very short dips for faults in the transmission system (50-100 ms clearing time to avoid stability problems) and much longer ones for faults in the distribution system, where protections are delayed to ensure selectivity [9].

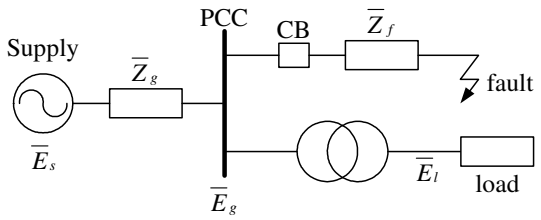


Fig. 2.1 Single-line diagram to display voltage division during voltage dips.

Often, it is preferable to characterize a voltage dip with the distance between the fault point and the PCC. In this case, the voltage $\overline{E}_{\mathrm{g}}$ during the fault can be expressed as

$$\overline{E}_{\mathrm{g}} = \frac{\lambda e^{\mathrm{j}\alpha}}{1 + \lambda e^{\mathrm{j}\alpha}} \tag{2.3}$$

where λ denotes the "electrical distance" between the faulted point and the PCC and α, called impedance angle, is the angle between grid and fault impedance

$$\alpha = \arctan\left(\frac{X_{\mathrm{f}}}{R_{\mathrm{f}}}\right) - \arctan\left(\frac{X_{\mathrm{g}}}{R_{\mathrm{g}}}\right) \tag{2.4}$$

Typically, the impedance angle α varies between $0°$ and $-60°$ [9].

An extended analysis of voltage dips and their classification is carried out in [64]. Depending on the type of fault (three-phase, phase-to-phase with or without ground involved, single-phase to ground), the resulting voltage dip at the PCC can be one of six types reported in Fig.2.2.

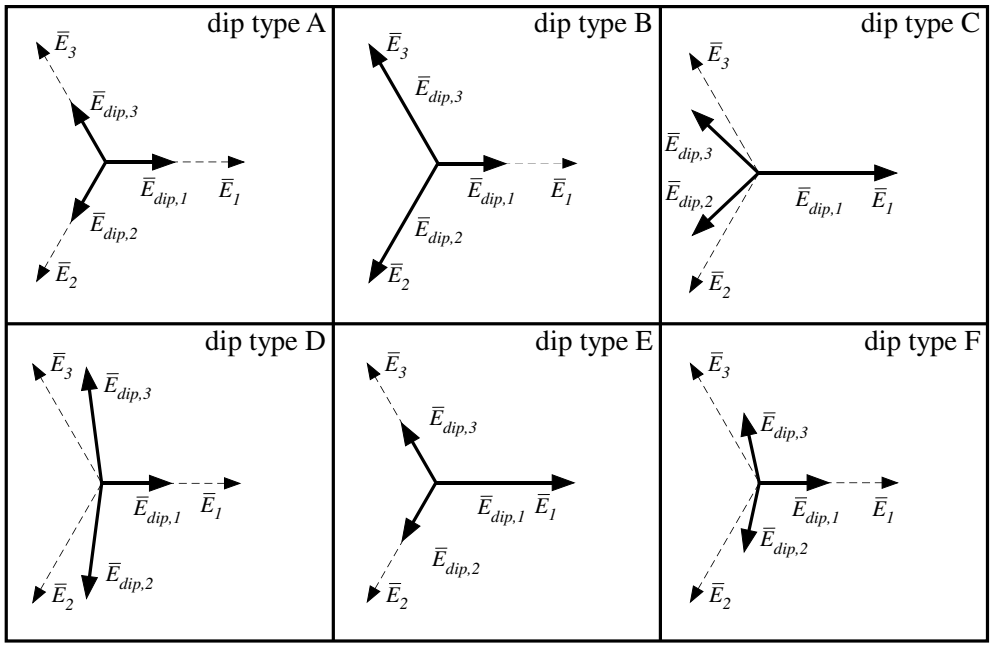


Fig. 2.2 Voltage dip classification "A" to "F". Phasors of three-phase voltage before (dotted) and during fault (solid) are displayed.

The load is usually supplied through a distribution transformer, connected in Δ/Y. The transformer swaps the phases and removes the zero-sequence component because of the delta connection, where no connection to ground exist. This results in a transformation of the dip characteristic as listed in Table.2.1 (right column). This dip classification is further extended in [63], where it is shown that type F is in fact a particular case of type C and D. It can be concluded that voltage dips that affect the load downstream a Δ/Y-transformer can only be of type A, C and D. The voltage dip type A is a drop in voltage in all three phases (balanced dip). The voltage dip type C is characterized by a drop in two phases with the third phase voltage almost undisturbed. Finally, the voltage dip type D is characterized by a larger drop in one phase and smaller drops in the other two phases. However, in some applications, such as control of VSC connected to the grid, it can be preferable to characterize the voltage dip in terms of the remaining positive-sequence voltage and the unbalance, expressed as magnitude of negative-sequence voltage in percentage of the pre-fault voltage [46].

TABLE 2.1. VOLTAGE DIP CLASSIFICATION AND PROPAGATION THROUGH Δ/Y-TRANSFORMERS.

Fault	Dip seen at PCC	Dip seen by the load
3-phase fault	type A	type A
1-phase fault	type B	type C
2-phase to ground	type E	type F
phase-to-phase	type C	type D

2.3 Voltage dip mitigation

The main problem related to voltage dips is that they can cause tripping of sensitive industrial equipment causing relatively high economical losses. As shown in Fig.2.3, different ways to reduce the number of voltage dips experienced by the load can be adopted [9]. The possibilities are to improve the power system, improve the immunity to voltage deviations of the end-user equipment and finally to use a mitigation device at the user interface. In the following, a brief description of these solutions will be carried out.

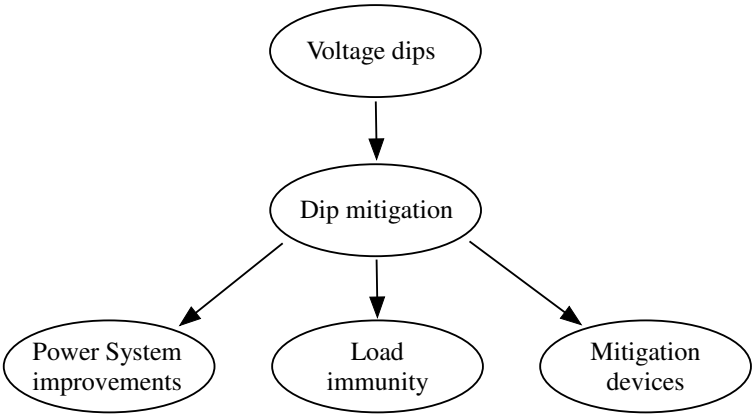


Fig. 2.3 Mitigation methods against voltage dips.

2.3.1 Power system improvement

A way to reduce the number of voltage dips experienced by the load is to improve the reliability of the power system. This can be done in three different ways:

- Improve the network design and operation;
- Reduce the number of faults per year;
- Use faster protection systems.

An extended analysis of these solutions is carried out in [9]; the following is a brief summary.

Improve network design and operation

By improving the power system design, the number and severity of the voltage quality phenomena experienced by the load is drastically reduced. The mitigation method against short interruptions and voltage dips is mainly the installation of redundant components, like feeders, generators or more substations to feed the bus where the sensitive load is connected. The problem related to this solution is that the costs for these improvements, especially at the transmission and subtransmission level, can be very high and, thus, this solution is not often economically feasible.

Reduce number of faults

Since the majority of voltage dips experienced in the power system are related to short-circuit faults, an obvious way to deal with the problem is to reduce the number of faults. The problem is that, since a fault represents an economical loss not only for the customer but also for the utility (a fault can damage the utility equipment or plant), most of the utilities have already reduced the fault frequency to a minimum. Improvements that reduce the number of faults per year include replacing the overhead lines with underground cables, increasing the insulation level and increasing the maintenance.

Faster protection system

By reducing the fault clearing time, the number of voltage dips experienced by the load will not be affected, but the duration of the dip will be reduced. A possible solution to reduce the clearing time of the fault is to use current-limiting fuses or modern static circuit breakers, which are able to clear the fault within one half-cycle [9]. However, some caution has to be taken when applying these new protection devices in existing distribution systems. If only some of the protective devices are replaced with static breakers (on incoming transformer circuits or feeder circuits, for instance), due to their extremely fast operation it would not be possible to co-ordinate them with previously existing downstream protective devices. Therefore, if faster fault clearing time is required, the whole system has to be re-designed and all protective devices have to be replaced with faster ones. This would greatly reduce the fault-clearing time. The drawback, of course, of these modifications in the power system is that this will result in an increase of the costs.

2.3.2 Load immunity

An increase of the load immunity against voltage dips can appear as the most suitable solution to avoid load tripping. The tolerance of the equipment is intended as the capability of the device to work properly during voltage variations. In order to evaluate the compatibility between power system and equipment, the so-called voltage-tolerance curve has been introduced in IEEE Std.1346-1998 [26]. This curve, reported in Fig.2.4, represents the maximum duration,

expressed in seconds, for which a piece of equipment can withstand dips of any magnitude (denoted in the figure as max Δt) and the maximum dip magnitude, expressed in per unit of the rated voltage, that the equipment can withstand regardless the duration of the dip (denoted as max ΔV). The knee of the curve is defined by the maximum duration and the minimum voltage and represents the tolerance of the equipment.

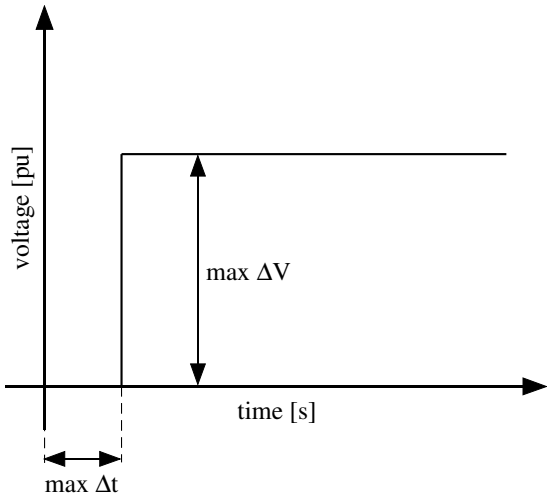


Fig. 2.4 Typical voltage-tolerance curve for sensitive equipment.

The main problem related to the immunity of the sensitive loads is that often the customer is not well aware of equipment sensitivity and will find out the problem only after the equipment has been installed. Moreover, since the customer is usually not in direct contact with the manufacturer, it is very hard to acquire information about the immunity of the device or to affect its specifications. Only for large industrial equipment, such as large drive systems, where usually the customer can require certain specification, the immunity of the equipment against power quality phenomena can be decided ad hoc.

2.3.3 Mitigation devices

The most commonly applied method for voltage dip mitigation is the installation of an additional device at the power system interface. The installation of these devices is getting more and more popular among industrial customers due to the fact that it is the only place where the customer has control over the situation. As explained in the previous section, both changes in the supply and changes in the characteristics of the equipment are outside the control of the end-user.

It is possible to divide the mitigation devices in two main groups:

- Passive mitigation devices, based on mature technology devices such as transformers or rotating machines;
- Power electronic based mitigation devices.

Motor-generator sets

Motor-generator sets store energy in a flywheel, as shown in Fig.2.5 [47]. They consist of a motor (can be an induction or a synchronous machine) supplied by the plant power system, a synchronous generator feeding the sensitive load and a flywheel, all connected to a common mechanical axis. The rotational energy stored in the flywheel can be used to perform steady-state voltage regulation and to support the voltage during disturbances. In case of voltage dips, the system can be disconnected from the mains by opening the contactor located upstream the motor and the sensitive load can be supplied through the generator. The mitigation capability of this device is related to the inertia and to the rotational speed of the flywheel.

This system has high efficiency, low initial costs and enables long-duration ride through (several seconds) but can only be used in industrial environment, due to its size, noise and maintenance requirements.

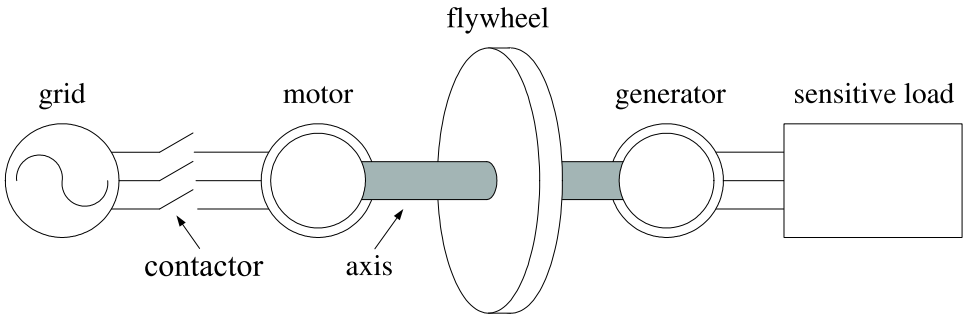


Fig. 2.5 Three-phase diagram of motor-generator set with flywheel to mitigate voltage dips.

Transformer-based mitigation devices

A constant voltage, or ferro-resonant, transformer works in a similar manner to a transformer with 1:1 turns ratio which is excited at a high point on its saturation curve, thus providing an output voltage that is not affected by input voltage variations. In the actual design, as shown in Fig.2.6, a capacitor, connected to the secondary winding, is needed to set the operating point above the knee of the saturation curve. This solution is suitable for low-power (less than 5 kVA [34]), constant loads: variable loads can cause problems, due to the presence of this tuned circuit on the output. Electronic tap changers (Fig.2.7) can be mounted on a dedicated transformer for the sensitive load, in order to change its turns ratio according to changes in the input voltage. They can be connected in series on the distribution feeder and be placed between the supply and the load. Part of the secondary winding supplying the load is divided into a number of sections, which are connected or disconnected by fast static switches, thus allowing regulation of the secondary voltage in steps. This should allow the output voltage to be brought back to a level above 90% of nominal value, even for severe voltage dips. If thyristor-based switches are used, they can only be turned on once per cycle and therefore the compensation is accomplished with a time delay of at least one half-cycle. An additional problem is that the current in the primary winding increases when the secondary voltage is increased to compensate for the dip in the grid voltage. Therefore, only small steps on the secondary side of the transformer are allowed.

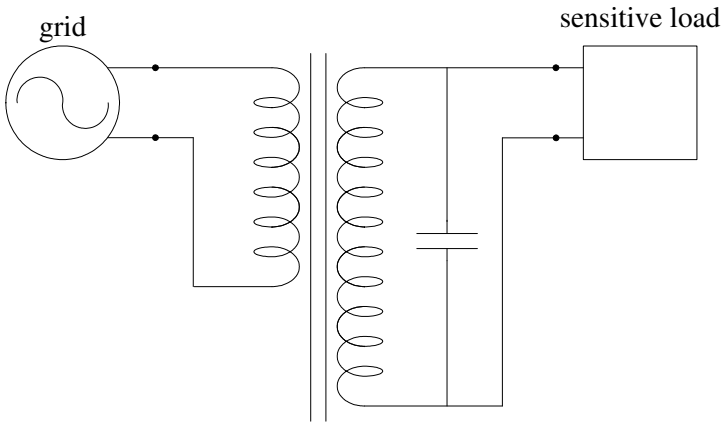


Fig. 2.6 Single-line diagram of ferro-resonant transformer.

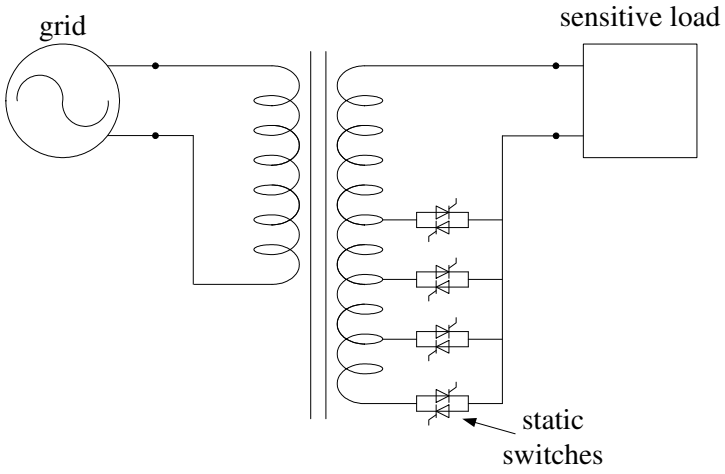


Fig. 2.7 Single-line diagram of transformer with electronic tap changers.

Static Transfer Switch

The Static Transfer Switch (STS) consists of two three-phase static switches, each constituted in turn of two antiparallel thyristors per phase, as shown in Fig.2.8, where the single-line diagram of an STS is displayed [45]. The aim of this device is to transfer the load from a primary source to a secondary one automatically and rapidly when reduced voltage is established in the primary source and while the secondary meets certain quality requirements. During normal operation, the primary source feeds the load through the thyristors of switch 1, while the secondary source is disconnected (switch 2 open). In case of voltage dips or interruptions in the primary source, the load will be transferred from the primary to the alternative source. Different control strategies in order to obtain instantaneous transfer of the load can be adopted. However, paralleling between the two sources during the transfer must be avoided. For this reason, the transfer time can take up to one half-cycle [49]. This means that the load will still be affected by the dip, but its duration will be reduced to the time necessary to transfer the load from the primary to the secondary source. The shortcoming of the STS is that it cannot mitigate voltage dips originated

by faults in the transmission system, since these type of dips usually affect both the primary and the secondary source. Moreover, it continuously conduct the load current, which leads to considerable conduction losses.

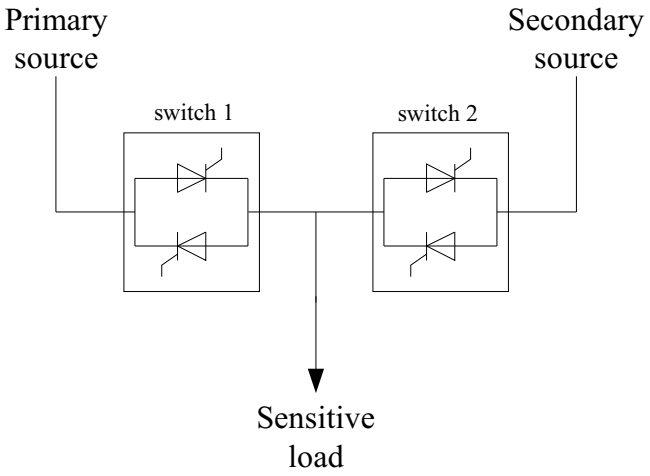


Fig. 2.8 Single-line diagram of Static Transfer Switch (STS).

Uninterruptible Power Supply

An Uninterruptible Power Supply (UPS) consists of a diode rectifier followed by an inverter, as shown in Fig.2.9 [47]. The energy storage is usually a battery connected to the DC link. During normal operation, the power coming from the AC supply is rectified and then inverted to fed the load. The battery remains in standby mode and only keeps the DC-bus voltage constant. During a voltage dip or an interruption, the energy released by the battery keeps the voltage at the DC bus constant. Depending on the storage capacity of the battery, it can supply the load for minutes or even hours. Low cost, simple operation and control have made the UPS the standard solution for low-power, single phase equipment, like computers. For higher-power loads the costs associated with losses due to the two conversions and maintenance of the batteries become too high and, therefore, a three-phase, high power UPS is not economically feasible.

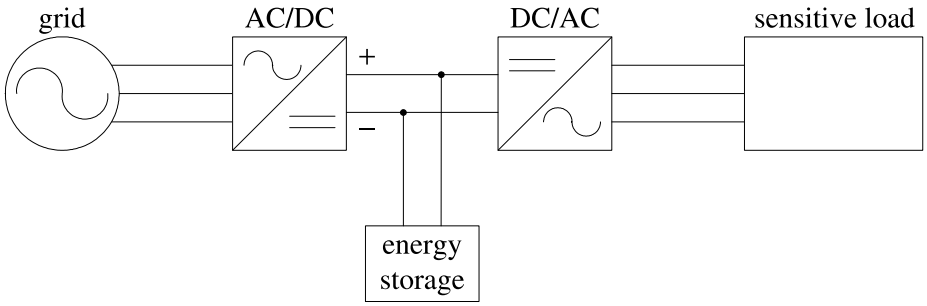


Fig. 2.9 Three-phase diagram of UPS.

Shunt-connected VSC

The basic idea of the shunt-connected VSC is to dynamically inject a current $\underline{i}_{\mathrm{r}}(t)$ of desired amplitude, frequency and phase into the grid. The typical configuration of a shunt-connected VSC is shown in Fig.2.10. The device consists of a VSC, an injection transformer, an AC filter and a DC-link capacitor. An energy storage can also be mounted on the DC link to allow active power injection into the AC grid.

The line impedance has a resistance R_{g} and inductance L_{g}. The grid voltage and current are denoted by $\underline{e}_{\mathrm{s}}(t)$ and $\underline{i}_{\mathrm{g}}(t)$, respectively. The voltage at the point of common coupling (PCC), which is also equal to the load voltage, is denoted by $\underline{e}_{\mathrm{g}}(t)$ and the load current by $\underline{i}_{\mathrm{l}}(t)$. The inductance and resistance of the AC-filter reactor are denoted by R_{r} and L_{r}, respectively.

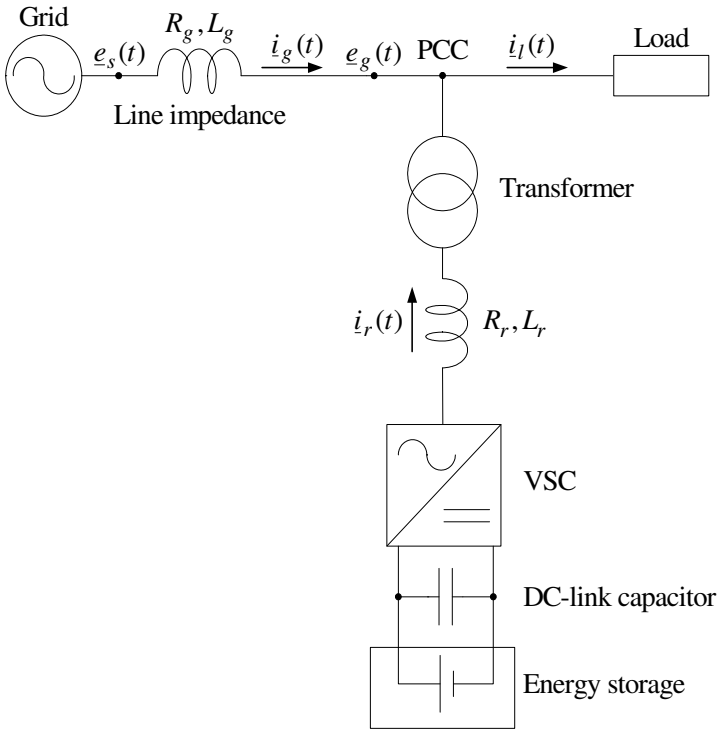


Fig. 2.10 Single-line diagram of shunt-connected VSC.

Figure 2.11 shows a simplified single-line diagram, where the VSC is represented as a current source. Amplitude, frequency and phase of the current $\underline{i}_{\mathrm{r}}(t)$ can be controlled.

By injecting a controllable current, the shunt-connected VSC can limit voltage fluctuation leading to flicker [53] and cancel harmonic currents absorbed by the load, thus operating as an active filter [1]. In both cases, the principle is to inject a current with same amplitude and opposite phase as the undesired components in the load current, so that they are cancelled in the grid current. These mitigation actions can be accomplished by only injecting reactive power.

A shunt-connected VSC can also be used for voltage dip mitigation. In this case, the device has to inject a current in the grid which results in an increased voltage amplitude at the PCC, as shown in the phasor diagram in Fig.2.12. The voltage phasor at PCC is denoted by $\overline{E}_{\mathrm{g}}$, $\overline{Z}_{\mathrm{g}}$ is the

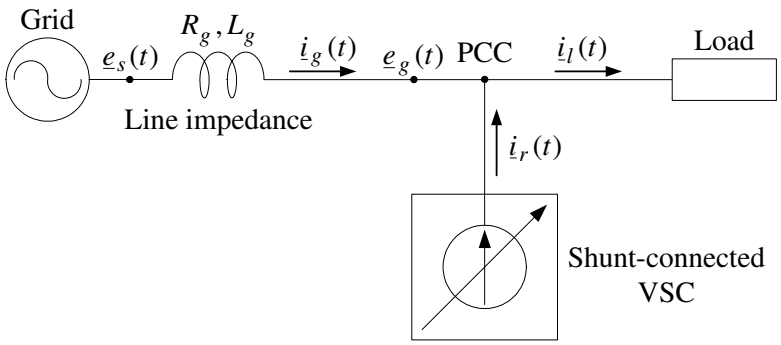


Fig. 2.11 Simplified single-line diagram of shunt-connected VSC.

line impedance, $\overline{E}_{\text{s,dip}}$ is the grid voltage phasor during the dip and ψ is the phase-angle jump of the dip.

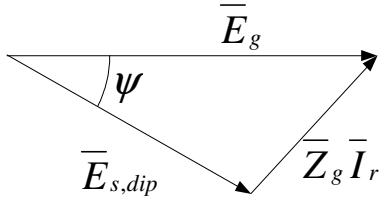


Fig. 2.12 Mitigation of voltage dips using shunt-connected VSC.

From the diagram it is possible to understand that when the shunt-connected VSC is used to mitigate voltage dips, it is necessary to provide an energy storage for injection of active power in order to avoid phase-angle jumps of the load voltage. If only reactive power is injected, it is possible to maintain the load voltage amplitude E_{g} to the pre-fault conditions but not its phase. Therefore, the voltage dip mitigation capability of a shunt-connected VSC depends on the rating of the energy storage and on the rating in current of the VSC. To restore the load voltage to the pre-fault conditions (without introducing phase-jump), the following condition must be fulfilled

$$\overline{E}_{\text{g}} = \overline{E}_{\text{s,dip}} + \overline{Z}_{\text{g}}\overline{I}_{\text{r}} \tag{2.5}$$

Active and the reactive power injected by the device can be calculated in per unit as

$$P_{\text{inj}} = \frac{\cos\varphi_{\text{l}}}{Z_{\text{l}}} - \frac{E_{\text{s}}(E_{\text{s,dip}}\cos(\varphi_{\text{g}} - \varphi_{\text{s}}) - \cos(\varphi_{\text{g}} - \varphi_{\text{s}} + \psi))}{E_{\text{s,dip}}Z_{\text{g}}} \tag{2.6}$$

$$Q_{\text{inj}} = -\frac{\sin\varphi_{\text{l}}}{Z_{\text{l}}} + \frac{E_{\text{s}}(E_{\text{s,dip}}\sin(\varphi_{\text{g}} - \varphi_{\text{s}}) - \sin(\varphi_{\text{g}} - \varphi_{\text{s}} + \psi))}{E_{\text{s,dip}}Z_{\text{g}}} \tag{2.7}$$

where the source voltage, the line impedance and the load impedance are expressed as $\overline{E}_{\text{s}} = E_{\text{s}}e^{\text{j}\varphi_{\text{s}}}$, $\overline{Z}_{\text{l}} = Z_{\text{l}}e^{\text{j}\varphi_{\text{l}}}$ and $\overline{Z}_{\text{g}} = Z_{\text{g}}e^{\text{j}\varphi_{\text{g}}}$, respectively.

Figures 2.13 and 2.14 show the amount of active and reactive power, respectively, injected by the shunt-connected VSC to maintain the voltage at its pre-fault value, considering the practical

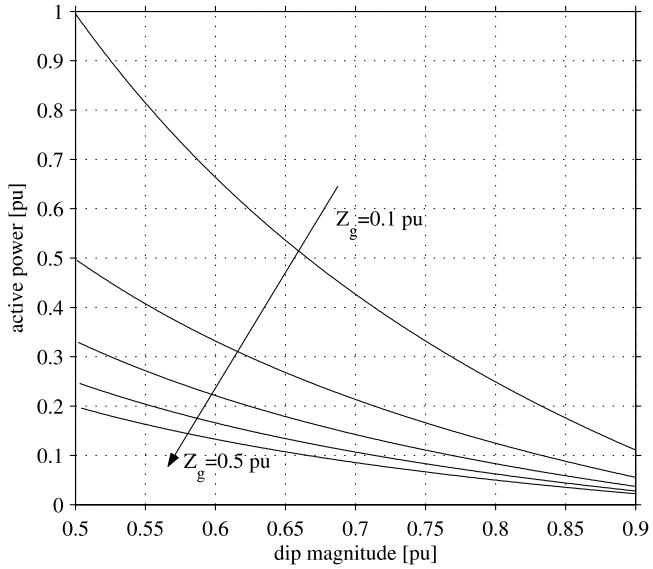


Fig. 2.13 Active power injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances $\overline{Z}_{\mathrm{g}}$ when injecting both active and reactive power.

case of mitigation of voltage dips with magnitude higher than 50% (i.e., the remaining voltage is equal or higher than 50% of the rated voltage). The load impedance $\overline{Z}_{\mathrm{l}}$ has been set to 1 pu with power factor of 0.8, while different values for the line impedance $\overline{Z}_{\mathrm{g}}$ (from 0.1 pu to 0.5 pu in steps of 0.1 pu) have been considered. For the grid impedance, it has been assumed that $X_{\mathrm{g}} = 0.995 Z_{\mathrm{g}}$ and $R_{\mathrm{g}} = 0.1 X_{\mathrm{g}}$ [12], which results in an impedance angle of $84.29°$. It is interesting to observe that, since the line impedance is mainly reactive ($R_{\mathrm{g}} < X_{\mathrm{g}}$), the amount of active power injected is significantly smaller than the reactive power. Moreover, the injected power increases for smaller values of the line impedance. This is not surprising, since smaller line impedance means a stronger grid. Thus, it will be necessary to inject a larger amount of current to increase the voltage at the PCC. Figure 2.15 shows the amplitude of the injected current versus the voltage dip magnitude when the line impedance is varying. From the figure it is possible to determine the biggest disadvantage when using a shunt-connected converter for voltage dip mitigation, i.e. the necessity of rating the device for large current.

If the VSC is designed for reactive power injection only, to find the expression of the required reactive power needed to keep the load voltage amplitude, the circuit diagram displayed in Fig.2.16 can be used, where $\underline{i}_{\mathrm{s}}(t)$ is the grid current upstream the fault point, $\underline{i}_{\mathrm{f}}(t)$ the fault current and $\overline{Z}_{\mathrm{l}}$ the load impedance.

Applying Thevenin to the circuit to the left of points A and B yields

$$\overline{E}'_{\mathrm{s}} = E'_{\mathrm{s}} e^{\mathrm{j}\varphi'_{\mathrm{s}}} = \overline{E}_{\mathrm{s}} \frac{\overline{Z}_{\mathrm{f}}}{\overline{Z}_{\mathrm{g}} + \overline{Z}_{\mathrm{f}}} \tag{2.8}$$

$$\overline{Z}'_{\mathrm{g}} = Z'_{\mathrm{g}} e^{\mathrm{j}\varphi'_{\mathrm{g}}} = \frac{\overline{Z}_{\mathrm{f}} \overline{Z}_{\mathrm{g}}}{\overline{Z}_{\mathrm{g}} + \overline{Z}_{\mathrm{f}}} \tag{2.9}$$

which are the Thevenin equivalent voltage and equivalent impedance, respectively.

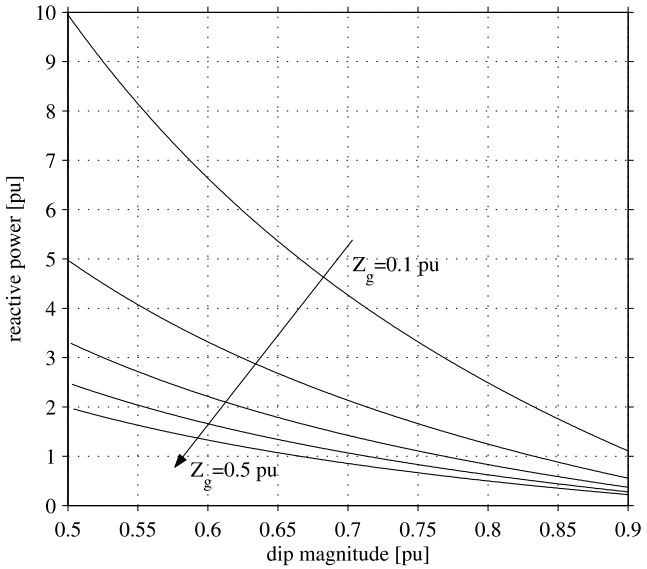


Fig. 2.14 Reactive power injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances $\overline{Z}_{\mathrm{g}}$ when injecting both active and reactive power.

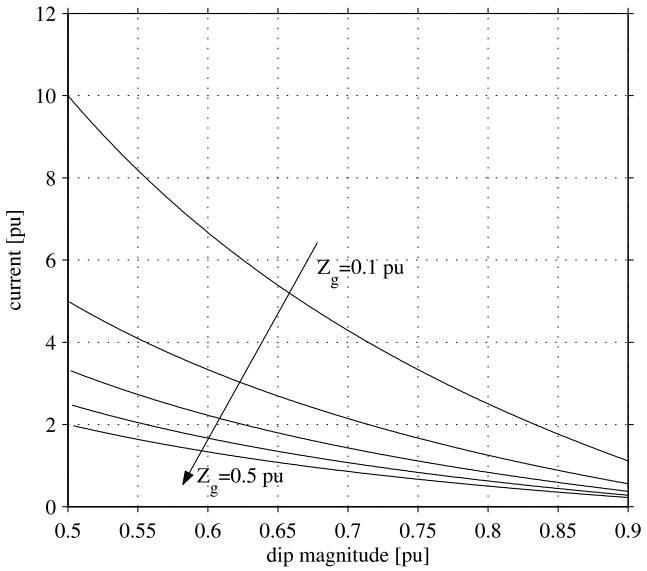


Fig. 2.15 Current injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances $\overline{Z}_{\mathrm{g}}$ when injecting both active and reactive power.

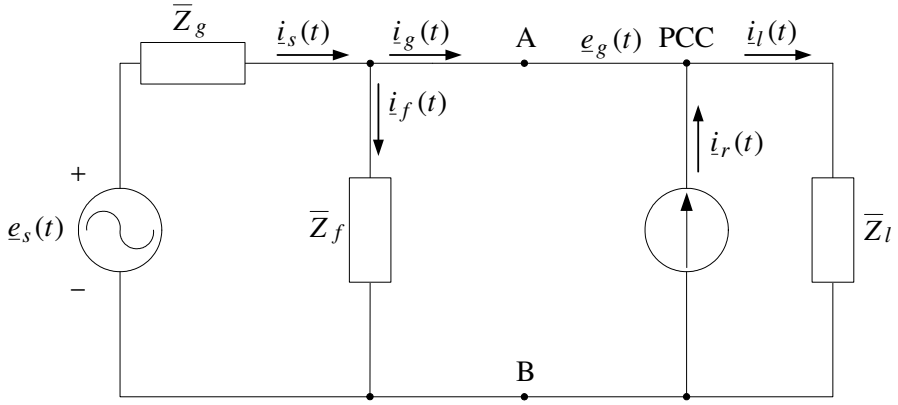


Fig. 2.16 Principle of operation of the shunt-connected VSC using simplified single-line diagram.

The injected reactive power can thus be found

$$Q_{\text{inj}} = \frac{E'_{\text{s}}}{Z'_{\text{g}}}\sin(\varphi'_{\text{s}} - \psi - \varphi'_{\text{g}}) + \frac{1}{Z'_{\text{g}}}\sin\varphi'_{\text{g}} + \frac{1}{Z_{\text{l}}}\sin\varphi_{\text{l}} \tag{2.10}$$

Figures 2.17 and 2.18 show the reactive power injected by the VSC and the load voltage phase shift when voltage dip mitigation with only reactive power injection is performed. The power injected in the grid is almost the same as in Fig.2.14 but the load voltage is affected by a phase deviation that increases with the magnitude of the dip and with the grid impedance $\overline{Z}_{\text{g}}$.

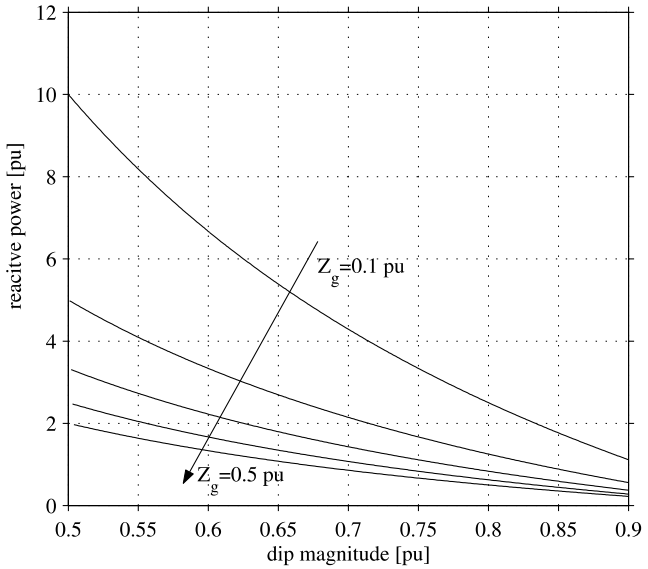


Fig. 2.17 Reactive power injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances Z_{g}. Reactive power injection only.

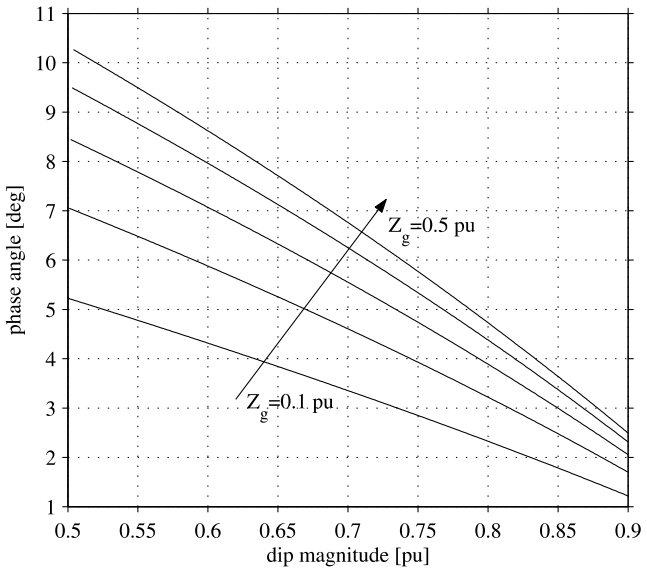


Fig. 2.18 Load voltage phase deviation as function of voltage dip magnitude for different line impedances Z_{g}. Reactive power injection only.

Series-connected VSC

In this section, the principle of operation of the series-connected VSC (also called static series compensator, SSC) will be described. The basic idea is to inject a voltage $\underline{e}_{\mathrm{c}}(t)$ of desired amplitude, frequency and phase between the PCC and the load in series with the grid voltage. A typical configuration of the SSC is shown in Fig.2.19: the main components of the SSC are the VSC, the filter, the injection transformer and the energy storage.

Figure 2.20 shows a simplified single-line diagram of the system with SSC. Differently from the shunt-connected VSC, the SSC can be represented as a voltage source with controllable amplitude, phase and frequency.

The SSC is mainly used for voltage dip mitigation. The device maintains the load voltage $\underline{e}_{\mathrm{l}}(t)$ to the pre-fault condition by injecting a voltage of appropriate amplitude and phase. Figure 2.21 shows the phasor diagram of the series injection principle during voltage dip mitigation, where $\overline{E}_c$ is the phasor of the voltage injected by the compensator, $\overline{I}_{\mathrm{l}}$ is the phasor of the load current and where φ is the angle displacement between load voltage and current.

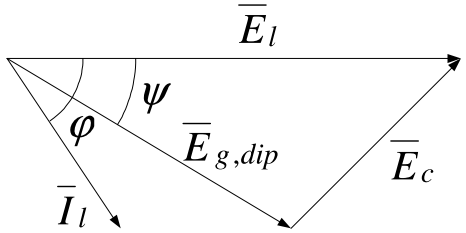


Fig. 2.21 Mitigation of voltage dips using SSC.

In order to be able to restore both magnitude and phase of the load voltage to the pre-fault

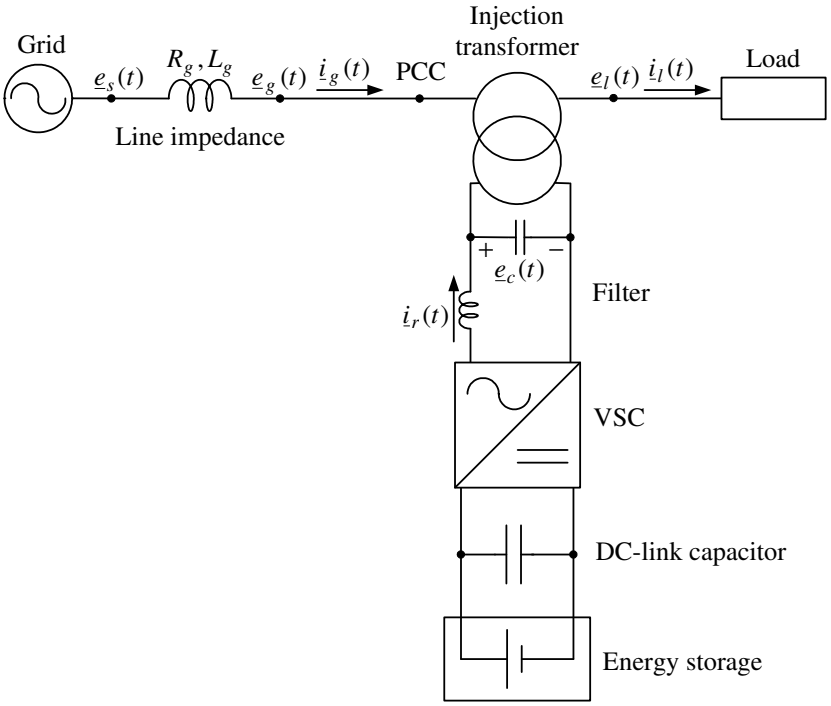


Fig. 2.19 Single-line diagram of SSC.

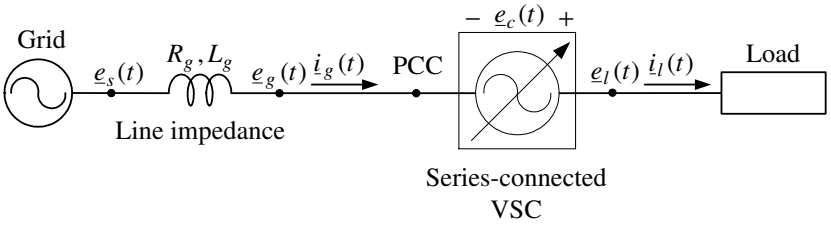


Fig. 2.20 Simplified single-line diagram of system with SSC.

conditions, the SSC has to inject both active and reactive power [10]. Assuming that the load voltage and current in pre-fault conditions are both equal to 1 pu, the power injected by the device during voltage dip mitigation is equal to

$$\begin{aligned}\overline{S}_{\text{inj}} &= \overline{E}_{\text{c}}\overline{I}_{\text{l}}^{*} = (\overline{E}_{\text{l}} - \overline{E}_{\text{g,dip}})\overline{I}_{\text{l}}^{*} = (1 - E_{\text{g,dip}}e^{\text{j}\psi})e^{\text{j}\varphi} = \\ &= \cos\varphi + \text{j}\sin\varphi - (E_{\text{g,dip}}\cos(\varphi+\psi) + \text{j}E_{\text{g,dip}}\sin(\varphi+\psi))\end{aligned} \tag{2.11}$$

Observe that the power absorbed by the load is given by

$$\overline{S}_{\text{load}} = P_{\text{load}} + \text{j}Q_{\text{load}} = \overline{E}_{\text{l}}\overline{I}_{\text{l}}^{*} = e^{\text{j}\varphi} = \cos\varphi + \text{j}\sin\varphi \tag{2.12}$$

Therefore, the active and the reactive power injected by the SSC are given by

$$P_{\text{inj}} = \left[\ 1 - \frac{E_{\text{g,dip}}\cos(\varphi+\psi)}{\cos\varphi}\ \right] P_{\text{load}} \tag{2.13}$$

$$Q_{\text{inj}} = \left[1 - \frac{E_{\text{g,dip}} \sin(\varphi + \psi)}{\sin\varphi} \right] Q_{\text{load}} \tag{2.14}$$

Figures 2.22 and 2.23 display the active and reactive power injected by the SSC during voltage dip mitigation for different impedance angles ($0°$, $-20°$, $-40°$, $-60°$) under the assumption of load impedance $\overline{Z}_1$ equal to 1 pu with power factor 0.8 inductive. It can be observed that lower active power is normally required as the phase-angle jump of the dip increases, while the required reactive power increases. Moreover, it is possible to notice that, in general, compared with the shunt-connected VSC (Fig.2.13), the SSC requires a larger energy storage to restore the load voltage to the pre-fault condition.

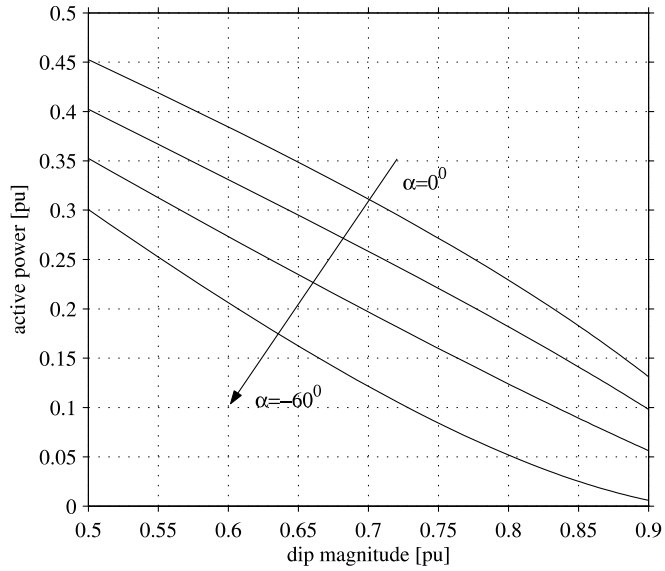


Fig. 2.22 Active power injected by SSC vs. dip magnitude during voltage dip mitigation for different impedance angles α when injecting both active and reactive power.

This is therefore the drawback when using the SSC for voltage dip mitigation and that still limits the commercial exploitation of the device, since the energy storage usually represents the most expensive component of the device [34]. Different compensation strategies, in order to minimize the active power injection during voltage dip mitigation, have been discussed in [6], but still require further investigation.

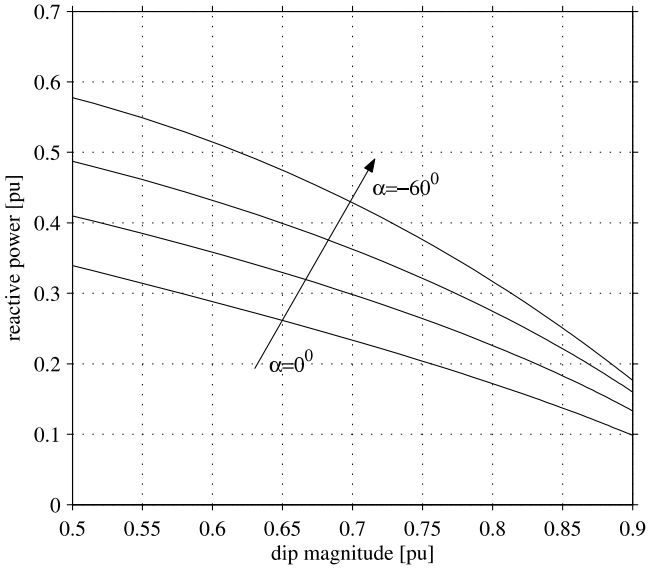


Fig. 2.23 Reactive power injected by SSC vs. dip magnitude during voltage dip mitigation for different impedance angles α when injecting both active and reactive power.

2.4 Conclusions

In this chapter, a brief overview of voltage dips, with their origin and classification has been given. Different methods for voltage dip mitigation have been described. Among all methods, the installation of a mitigation device seems to be the only solution for customers to protect themselves from voltage dips. Different mitigation devices, based on passive devices and based on power electronics, have been described. Particular emphasis has been given to the shunt-connected VSC and to the Static Series Compensator (SSC), which are the core of this report. In the next chapters, these two devices, and especially their control system, will be described in detail.

Chapter 3

Vector current-controller for shunt-connected VSC

3.1 Introduction

Grid-connected forced-commutated VSCs are becoming more and more common at distribution level for applications such as wind power plants, active front-end for adjustable speed drives and custom power devices. Also VSCs for transmission level are introduced in HVDCs. Benefits of using VSCs are sinusoidal currents, high current bandwidth, controllable reactive power to regulate power factor or bus-voltage level and to minimize resonances between the grid and the converter. These characteristics, which are highly desirable in grid-connected applications, can be obtained by using a high-performance current controller for the VSC.

This chapter consists of two parts. The first part deals with the development and the analysis of the deadbeat current-controller, designed to track the reference current in two samples. An extended analysis of the control system, its problems and possible solutions will be carried out. Improvements of a standard current controller in order to control positive and negative sequences of the line-filter current will be presented. In total, three different current-controllers will be investigated: the vector current-controller type 1 (denoted as VCC1), the vector current-controller type 2 (denoted as VCC2) and the dual vector current-controller, denoted as DVCC. The second part of the chapter presents simulation results for these vector current-controllers.

3.2 Vector Current-controller Type 1 (VCC1)

To obtain a high performance system, it is important to maximize the current bandwidth of the VSC. In a vector current-control system, the active and reactive currents (as well as the active and reactive powers) can be controlled independently. As a result, a high-bandwidth controller with a low cross-coupling between the reference currents and the line-filter currents can be achieved [13][55].

The VSC is the most important element in the design of the investigated system. Figure 3.1 shows the main circuit scheme of a three-phase VSC. The VSC is connected to a symmetric three-phase load with impedance $R_\mathrm{l} + \mathrm{j}\omega L_\mathrm{l}$ and back emfs $e_\mathrm{a}(t)$, $e_\mathrm{b}(t)$ and $e_\mathrm{c}(t)$. The phase potential, phase voltages and the potential of the floating-star load are denoted by $v_\mathrm{a}(t)$, $v_\mathrm{b}(t)$, $v_\mathrm{c}(t)$, $u_\mathrm{a}(t)$, $u_\mathrm{b}(t)$, $u_\mathrm{c}(t)$ and $v_0(t)$ respectively. The load currents in the three phases are denoted by $i_\mathrm{ra}(t)$, $i_\mathrm{rb}(t)$, $i_\mathrm{rc}(t)$ respectively. The valves in the phase-legs of the VSC (usually insulated gate bipolar transistors, IGBTs) are controlled by the switching signals $sw_\mathrm{a}(t)$, $sw_\mathrm{b}(t)$ and $sw_\mathrm{c}(t)$. The DC-link voltage is denoted by $u_\mathrm{dc}(t)$. The switching signal can be equal to ± 1. When $sw_\mathrm{a}(t)$ is equal to 1, the upper valve in the phase a is turned on while the lower valve in the same leg is off. Therefore, the potential $v_\mathrm{a}(t)$ is equal to half of the DC-link voltage ($u_\mathrm{dc}(t)/2$). Vice versa, when the switching signal is equal to -1, the upper valve is off and the lower one is on and, thus, $v_\mathrm{a}(t)$ is equal to $-u_\mathrm{dc}(t)/2$. The potential $v_0(t)$ can be written as

$$v_0(t) = \frac{1}{3}(v_\mathrm{a}(t) + v_\mathrm{b}(t) + v_\mathrm{c}(t)) \tag{3.1}$$

assuming that the load is symmetrical. The phase voltages become

$$u_\mathrm{a}(t) = v_\mathrm{a}(t) - v_0(t) \tag{3.2}$$
$$u_\mathrm{b}(t) = v_\mathrm{b}(t) - v_0(t) \tag{3.3}$$
$$u_\mathrm{c}(t) = v_\mathrm{c}(t) - v_0(t) \tag{3.4}$$

To obtain the switching signals for the VSC, Pulse Width Modulation technique (PWM) has been adopted [24]. To avoid short-circuit of the VSC phase-legs, blanking time must be applied [36]. Assuming that the switching frequency is very high, during steady-state operation the VSC can be modelled as an ideal three-phase voltage source. Therefore, the output voltages of the VSC can be considered sinusoidal and equal to the reference voltages to the modulator, given by

$$u^*_\mathrm{a}(t) = \sqrt{\frac{2}{3}} U^* \sin(\omega^* t + \phi^*) \tag{3.5}$$
$$u^*_\mathrm{b}(t) = \sqrt{\frac{2}{3}} U^* \sin(\omega^* t + \phi^* - \frac{2}{3}\pi) \tag{3.6}$$
$$u^*_\mathrm{c}(t) = \sqrt{\frac{2}{3}} U^* \sin(\omega^* t + \phi^* - \frac{4}{3}\pi) \tag{3.7}$$

where U^*, ω^* and ϕ^* are the reference value of the phase-to-phase RMS voltage, the reference angular frequency and the reference phase-shift respectively.

In the three-phase diagram of the VSC system displayed in Fig.3.2, the grid voltages at the PCC are denoted by $e_\mathrm{g,a}(t)$, $e_\mathrm{g,b}(t)$ and $e_\mathrm{g,c}(t)$. The currents through the filter reactor are $i_\mathrm{r,a}(t)$, $i_\mathrm{r,b}(t)$ and $i_\mathrm{r,c}(t)$ and the phase voltages out of the VSC are denoted by $u_\mathrm{a}(t)$, $u_\mathrm{b}(t)$ and $u_\mathrm{c}(t)$. The resistance and the inductance of the filter reactor are denoted by R_r and L_r, respectively.

Applying Kirchhoff's voltage law (KVL), the following differential equations for the three phases can be obtained

$$u_\mathrm{a}(t) - e_\mathrm{g,a}(t) - R_\mathrm{r} i_\mathrm{r,a}(t) - L_\mathrm{r} \frac{\mathrm{d}}{\mathrm{d}t} i_\mathrm{r,a}(t) = 0 \tag{3.8}$$

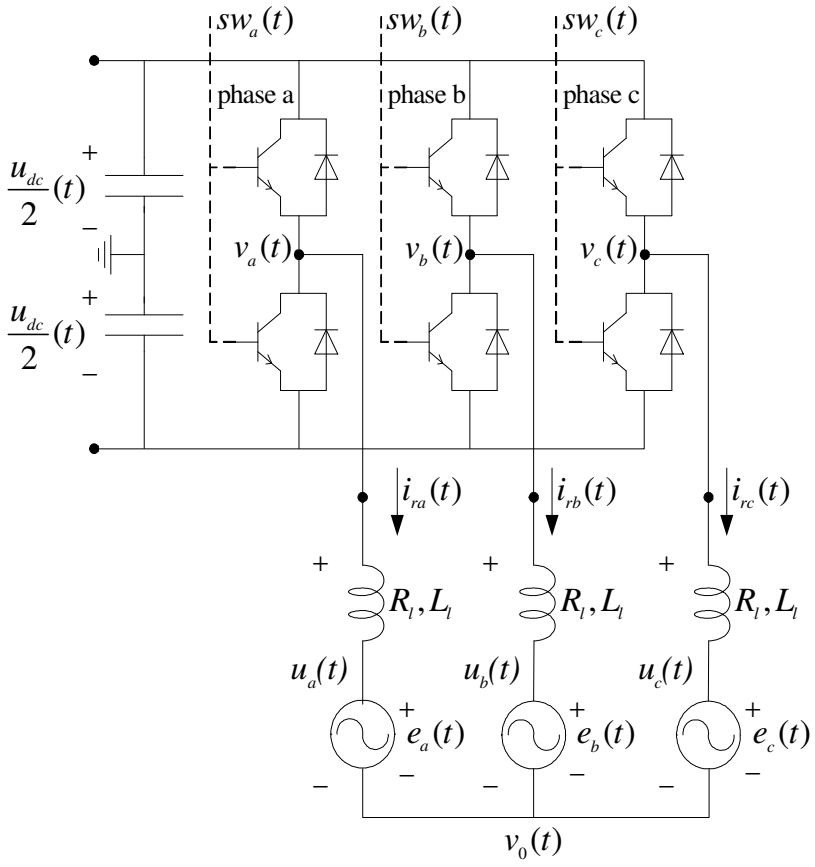


Fig. 3.1 Main circuit of three-phase VSC and load consisting of impedance and voltage sources.

$$u_{\mathrm{b}}(t) - e_{\mathrm{g,b}}(t) - R_{\mathrm{r}} i_{\mathrm{r,b}}(t) - L_{\mathrm{r}} \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{r,b}}(t) = 0 \tag{3.9}$$

$$u_{\mathrm{c}}(t) - e_{\mathrm{g,c}}(t) - R_{\mathrm{r}} i_{\mathrm{r,c}}(t) - L_{\mathrm{r}} \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{r,c}}(t) = 0 \tag{3.10}$$

By applying Clarke's transformation, Eqs.(3.8) to (3.10) can be written in the fixed $\alpha\beta$-coordinate system as

$$\underline{u}^{(\alpha\beta)}(t) - \underline{e}_{\mathrm{g}}^{(\alpha\beta)}(t) - R_{\mathrm{r}} \underline{i}_{\mathrm{r}}^{(\alpha\beta)}(t) - L_{\mathrm{r}} \frac{\mathrm{d}}{\mathrm{d}t} \underline{i}_{\mathrm{r}}^{(\alpha\beta)}(t) = 0 \tag{3.11}$$

The $\alpha\beta$- to dq-transformation (in Appendix A) is applied. The phase-locked loop (PLL) [22][6] is synchronized with the grid voltage vector $\underline{e}_{\mathrm{g}}^{(\alpha\beta)}(t)$ and the transformation angle is denoted by θ, and is equal to the grid voltage angle in steady state. The VSC voltages and the grid voltages and currents in the rotating dq-coordinate system are equal to

$$\underline{u}^{(dq)}(t) = e^{-\mathrm{j}\theta(t)} \underline{u}^{(\alpha\beta)}(t) \tag{3.12}$$

$$\underline{e}_{\mathrm{g}}^{(dq)}(t) = e^{-\mathrm{j}\theta(t)} \underline{e}_{\mathrm{g}}^{(\alpha\beta)}(t) \tag{3.13}$$

$$\underline{i}_{\mathrm{r}}^{(dq)}(t) = e^{-\mathrm{j}\theta(t)} \underline{i}_{\mathrm{r}}^{(\alpha\beta)}(t) \tag{3.14}$$

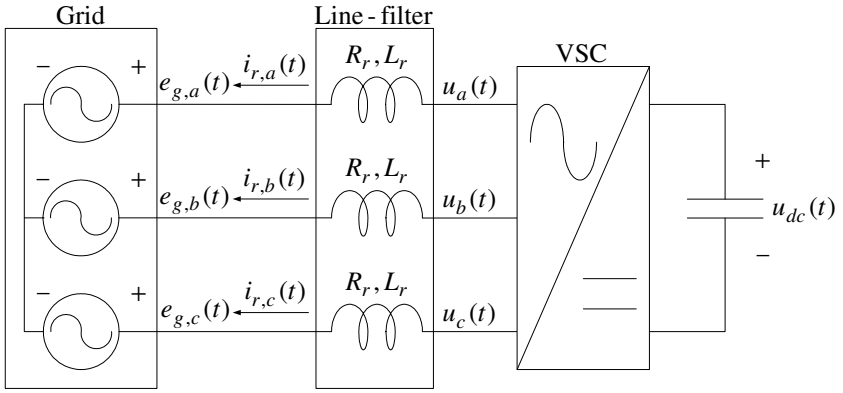


Fig. 3.2 Three-phase diagram of grid-connected VSC system.

Equation (3.11) can thus be transformed into

$$\underline{u}^{(dq)}(t) - \underline{e}_{\mathrm{g}}^{(dq)}(t) - R_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dq)}(t) - L_{\mathrm{r}}\frac{\mathrm{d}}{\mathrm{d}t}\underline{i}_{\mathrm{r}}^{(dq)}(t) - \mathrm{j}\omega L_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dq)}(t) = 0 \tag{3.15}$$

which can be split up into two equations representing the d- and the q- components separately

$$u_d(t) - e_{\mathrm{g}d}(t) - R_{\mathrm{r}} \cdot i_{\mathrm{r}d}(t) - L_{\mathrm{r}}\frac{\mathrm{d}}{\mathrm{d}t}i_{\mathrm{r}d}(t) + \omega L_{\mathrm{r}} i_{\mathrm{r}q}(t) = 0 \tag{3.16}$$

$$u_q(t) - e_{\mathrm{g}q}(t) - R_{\mathrm{r}} \cdot i_{\mathrm{r}q}(t) - L_{\mathrm{r}}\frac{\mathrm{d}}{\mathrm{d}t}i_{\mathrm{r}q}(t) - \omega L_{\mathrm{r}} i_{\mathrm{r}d}(t) = 0 \tag{3.17}$$

With the chosen PLL [22], the voltage vector is aligned with the direction of the d-axis during steady state. The grid voltage component in the d-direction is equal to its RMS-value (when using power-invariant transformation, Appendix A) and the q-component of the grid voltage is equal to zero. Thus, the d-component of the current vector (in steady state parallel to the grid voltage vector) becomes the active current component (d-current) and the q-component of the current vector becomes the reactive current component (q-current).

3.2.1 Proportional Controller

In this section, the proportional controller will be derived for the vector current-controller.

Considering that the control system has to be implemented in a digital controller and that it will operate in discrete time, it is necessary to discretize Eqs.(3.16) and (3.17). By integrating these equations over one sample period T_{s} (from time kT_{s} to time $(k+1)T_{\mathrm{s}}$) and then dividing by the sample time T_{s}, the following equations can be obtained

$$\begin{aligned} u_d(k,k+1) = {} & e_{\mathrm{g}d}(k,k+1) + R_{\mathrm{r}} i_{\mathrm{r}d}(k,k+1) - \omega L_{\mathrm{r}} i_{\mathrm{r}q}(k,k+1) + \\ & + \frac{L_{\mathrm{r}}}{T_{\mathrm{s}}}(i_{\mathrm{r}d}(k+1) - i_{\mathrm{r}d}(k)) \end{aligned} \tag{3.18}$$

$$u_q(k,k+1) = e_{gq}(k,k+1) + R_r i_{rq}(k,k+1) + \omega L_r i_{rd}(k,k+1) + \\ + \frac{L_r}{T_s}(i_{rq}(k+1) - i_{rq}(k)) \tag{3.19}$$

where $u_d(k,k+1)$ denotes the average value of the voltage component u_d from sample k to sample $k+1$ (and analogously for the other quantities) [5]. If a proportional regulator with deadbeat gain is used, the controller will track the reference currents with one sample delay [2]. Thus, the current reference value at the sample instant k must be equal to the current value at the sample $k+1$, i.e.

$$\underline{i}_r^{(dq)}(k+1) = \underline{i}_r^{(dq)*}(k) \tag{3.20}$$

The following assumptions can be made in order to derive the controller:

- The grid voltage changes slowly and can be considered constant over one sample period

$$\underline{e}_g^{(dq)}(k,k+1) = \underline{e}_g^{(dq)}(k) \tag{3.21}$$

- The current variations are linear

$$\underline{i}_r^{(dq)}(k,k+1) = \frac{1}{2}\left[\ \underline{i}_r^{(dq)}(k) + \underline{i}_r^{(dq)}(k+1)\ \right] = \frac{1}{2}\left[\ \underline{i}_r^{(dq)}(k) + \underline{i}_r^{(dq)*}(k)\ \right] \tag{3.22}$$

- The average value of the VSC voltage over a sample period is equal to the reference value

$$\underline{u}^{(dq)}(k,k+1) = \underline{u}^{(dq)*}(k) \tag{3.23}$$

Under these assumptions, the proportional controller can be rewritten as follows [54]

$$u_d^*(k) = e_{gd}(k) + R_r i_{rd}(k) - \frac{\omega L_r}{2}(i_{rq}(k) + i_{rq}^*(k)) + \\ + \left(\ \frac{L_r}{T_s} + \frac{R_r}{2}\ \right)(i_{rd}^*(k) - i_{rd}(k)) = u_{ffd}(k) + k_p(i_{rd}^*(k) - i_{rd}(k)) \tag{3.24}$$

$$u_q^*(k) = e_{gq}(k) + R_r i_{rq}(k) + \frac{\omega L_r}{2}(i_{rd}(k) + i_{rd}^*(k)) + \\ + \left(\ \frac{L_r}{T_s} + \frac{R_r}{2}\ \right)(i_{rq}^*(k) - i_{rq}(k)) = u_{ffq}(k) + k_p(i_{rq}^*(k) - i_{rq}(k)) \tag{3.25}$$

where $u_{ffd}(k)$ and $u_{ffq}(k)$ are the feed-forward voltage terms for the d- and for the q-component at sample k, respectively, while

$$k_p = \frac{L_r}{T_s} + \frac{R_r}{2} \tag{3.26}$$

is the proportional gain of the controller to obtain deadbeat.

3.2.2 Proportional-Integral controller

In order to remove static errors caused by non-linearities, noise in the measurements and non-ideal components, an integral part is introduced in the controller [43]. The controller using PI-regulator can be formulated as

$$u_d^*(k) = u_{\mathrm{ff}d}(k) + k_p(i_{\mathrm{r}d}^*(k) - i_{\mathrm{r}d}(k)) + \Delta u_{\mathrm{i}d}(k) \tag{3.27}$$

$$u_q^*(k) = u_{\mathrm{ff}q}(k) + k_p(i_{\mathrm{r}q}^*(k) - i_{\mathrm{r}q}(k)) + \Delta u_{\mathrm{i}q}(k) \tag{3.28}$$

where $\Delta u_{\mathrm{i}d}(k)$ and $\Delta u_{\mathrm{i}q}(k)$ are the integral terms for the d- and for the q-component at sample k, respectively. These terms are written as

$$\Delta u_{\mathrm{i}d}(k+1) = \Delta u_{\mathrm{i}d}(k) + k_i(i_{\mathrm{r}d}^*(k) - i_{\mathrm{r}d}(k)) \tag{3.29}$$

$$\Delta u_{\mathrm{i}q}(k+1) = \Delta u_{\mathrm{i}q}(k) + k_i(i_{\mathrm{r}q}^*(k) - i_{\mathrm{r}q}(k)) \tag{3.30}$$

where the integral gain k_i can be written as

$$k_i = k_p \frac{T_{\mathrm{s}}}{T_i} \tag{3.31}$$

with T_i the integration time constant. After some algebraic manipulation of Eqs.(3.27) and (3.28) [2], the latter is found as

$$T_i = \frac{L_{\mathrm{r}}}{R_{\mathrm{r}}} + \frac{T_{\mathrm{s}}}{2} \approx \frac{L_{\mathrm{r}}}{R_{\mathrm{r}}} \tag{3.32}$$

to obtain deadbeat. From Eqs.(3.26) and (3.32) it is possible to notice that the parameters of the PI-controller are directly related to the filter parameters R_{r} and L_{r}. This represents a useful tool when analyzing the sensitivity of the control system to system variations. Moreover, it is demonstrated in [2] that this is an optimal choice to obtain a discrete deadbeat controller.

In Fig.3.3, the block scheme of the vector current-controller is displayed. The algorithm of the vector current-controller can be summarized as follows:

1. Measure grid voltages and filter currents and sample them with sampling frequency f_s;
2. Transform all quantities from the three-phase coordinate system to the fixed $\alpha\beta$-coordinate system and then to the rotating dq-coordinate system, using the transformation angle $\theta(k)$, obtained from the PLL;
3. Calculate the reference voltage $\underline{u}^{(dq)*}(k)$;
4. Convert the reference voltage from the rotating dq-coordinate system to the three-phase coordinate system by using the transformation angle $\theta(k) + \Delta\theta$, where $\Delta\theta = 0.5\omega T_{\mathrm{s}}$ is a compensation angle to take into account the delay introduced by the discretization of the measured quantities [54];
5. Calculate the duty-cycles [36] in the PWM block and send the switching pulses to the VSC valves.

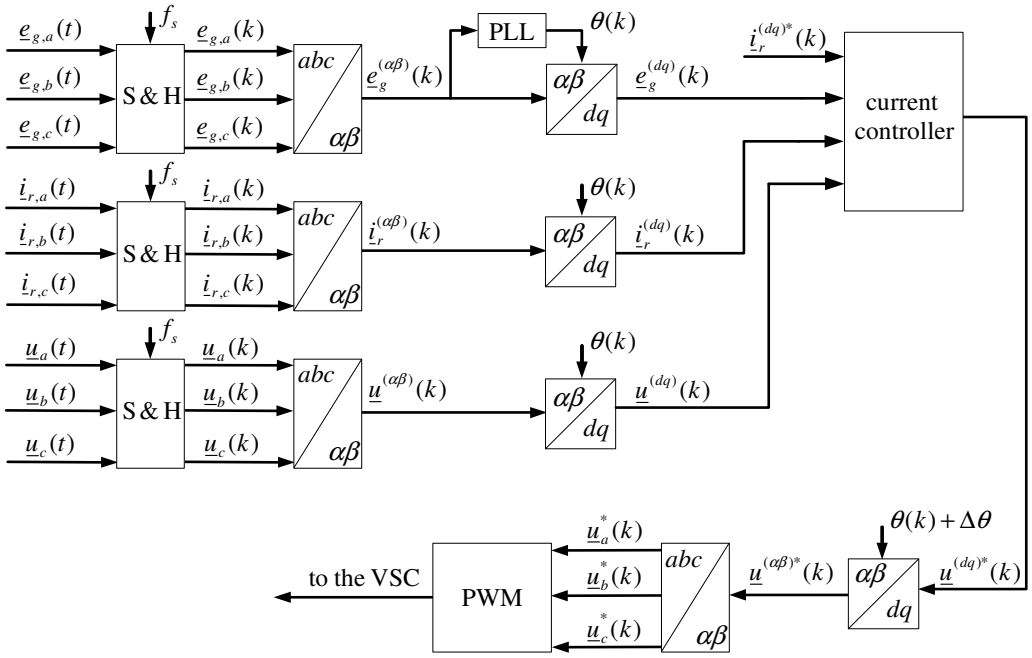


Fig. 3.3 Block scheme of implemented vector current-controller.

In order to improve the controller derived for ideal conditions, it is necessary to take into account some problems that occur in a real system. In particular, it is important to consider that the amplitude of the output voltage of the VSC is not infinite, but limited and proportional to the DC-link voltage level. Moreover, all calculations are affected by the delay due to the computational time of the control computer. For this reason, some improvements have been made to the described vector current-controller:

- Smith predictor using a state observer for the computational time delay compensation [4] [41];
- Limitation of the reference voltage vector and anti-windup function to prevent integrator windup [4] [41].

3.2.3 One-sample delay compensation

In a real system, the reference voltage used in the PWM modulator $\underline{u}^{(dq)*}(k)$ is delayed one sampling period due to the computational time in the control computer. If a control system with high proportional gain is used, this delay will affect the performance of the system and large oscillations in the output current can be experienced [7]. To avoid this problem and be able to use a high proportional gain, it is necessary compensate for this delay.

In this work, a Smith predictor has been used for this purpose [42]. The main advantage by using a Smith predictor is that the current controller can be treated as in the ideal case without any time delay. The basic idea of the Smith predictor is to predict the output current one sample ahead

by using a state observer and feed the predicted current back into the current controller. Thus, the delay of one sample has been eliminated. In order to feedback the real current to the current controller, the predicted current one sample delayed is subtracted from the feedback signal. The block scheme of the current controller with the computational time delay, the Smith predictor and the process (equal to the VSC system shown in Fig.3.2) is displayed in Fig.3.4. The output of the Smith predictor is the difference between the estimated filter current at sample k, $\underline{\hat{i}}_{\mathrm{r}}^{(dq)}(k)$ and the same signal at sample $k-1$, $\underline{\hat{i}}_{\mathrm{r}}^{(dq)}(k-1)$. If at sample k a step in the reference current is applied, at sample $k+1$ the reference voltage $\underline{u}^{(dq)*}$ output of the current controller will vary. Therefore, the output signal of the Smith predictor will not be equal to zero and will adjust the current error. At sample $k+2$ the difference between the predicted current and the delayed one will be zero again. Thus, the Smith predictor will not affect the current error. Therefore, the Smith predictor will affect the performance of the controller only during transients, but not during steady state.

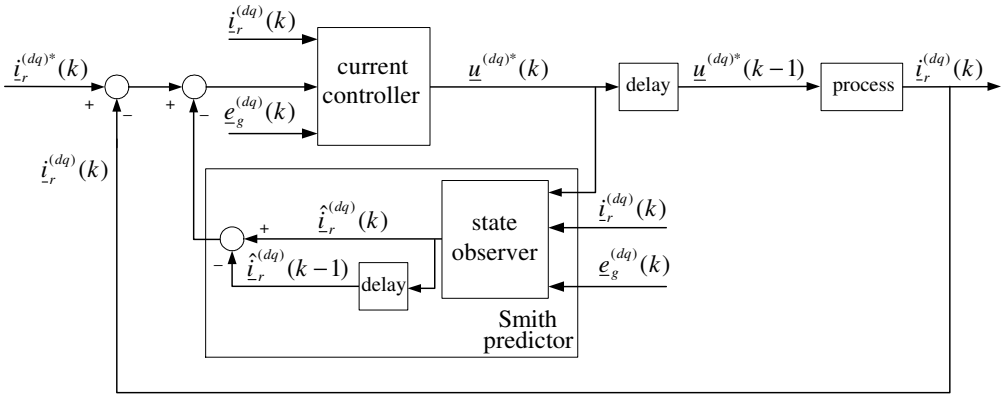


Fig. 3.4 Block scheme of vector current-controller with Smith predictor and process.

For a correct estimation of the grid current, the state observer has to be designed in order to reproduce the process. Applying KVL to the circuit shown in Fig.3.5, the following equation in the $\alpha\beta$-coordinate system can be written

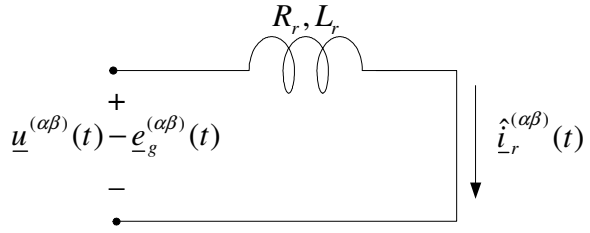


Fig. 3.5 Single-line diagram of circuit representation of state observer.

$$\underline{u}^{(\alpha\beta)}(t) - \underline{e}_{\mathrm{g}}^{(\alpha\beta)}(t) = R_{\mathrm{r}}\underline{\hat{i}}_{\mathrm{r}}^{(\alpha\beta)}(t) + L_{\mathrm{r}}\frac{\mathrm{d}}{\mathrm{d}t}\underline{\hat{i}}_{\mathrm{r}}^{(\alpha\beta)}(t) \tag{3.33}$$

In the dq-coordinate system, Eq.(3.33) becomes

$$\underline{u}^{(dq)}(t) - \underline{e}_{\mathrm{g}}^{(dq)}(t) = R_{\mathrm{r}}\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(t) + \mathrm{j}\omega L_{\mathrm{r}}\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(t) + L_{\mathrm{r}}\frac{\mathrm{d}}{\mathrm{d}t}\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(t) \tag{3.34}$$

which can be discretized using the forward Euler method. The grid voltage changes slowly compared with the sampling time, so it can be considered constant over one sampling period. The average values of the VSC voltages over one sample period are equal to the reference values. Equation (3.34) can therefore be rewritten in the discrete time domain as

$$\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k+1) = \left(1 - \frac{R_{\mathrm{r}}T_{\mathrm{s}}}{L_{\mathrm{r}}} - \mathrm{j}\omega T_{\mathrm{s}} \right)\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k) + \frac{T_{\mathrm{s}}}{L_{\mathrm{r}}}(\underline{u}^{(dq)*}(k) - \underline{e}_{\mathrm{g}}^{(dq)}(k)) \tag{3.35}$$

The measured current $\underline{i}_{\mathrm{r}}^{(dq)}(k)$ and the predicted current $\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k)$ are equal in an ideal system, but in a real system, due to non linearities and noise in the measurements, this relation is not valid. Therefore, an additional term is included to take into account this error in the estimation, giving the final equation for the state observer as

$$\begin{aligned}\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k+1) = &\left(1 - \frac{R_{\mathrm{r}}T_{\mathrm{s}}}{L_{\mathrm{r}}} - \mathrm{j}\omega T_{\mathrm{s}} \right)\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k) + \frac{T_{\mathrm{s}}}{L_{\mathrm{r}}}(\underline{u}^{(dq)*}(k) - \underline{e}_{\mathrm{g}}^{(dq)}(k)) + \\ &+ k_{\mathrm{psp}}(\underline{i}_{\mathrm{r}}^{(dq)}(k) - \widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k))\end{aligned} \tag{3.36}$$

where k_{psp} denotes the observer gain. Thus, if k_{psp} is large, the observer does not trust the process model. If k_{psp} is small, the observer believes in the process model.

To obtain the reference phase voltages, the reference voltage vector $\underline{u}^{(dq)*}$ in the dq-coordinate system is transformed in the fixed $\alpha\beta$-coordinate system, as shown earlier in Fig.3.3. The one-sample delay due to the computational time affects also the compensation angle $\Delta\theta$. For a correct transformation, the reference voltage vector in the $\alpha\beta$-plane is given by

$$\underline{u}^{(\alpha\beta)*} = \underline{u}^{(dq)*}e^{\mathrm{j}(\theta+\Delta\theta)} = \underline{u}^{(dq)*}e^{\mathrm{j}(\theta+\frac{3}{2}\omega T_{\mathrm{s}})} \tag{3.37}$$

3.2.4 Saturation and Integrator Anti-windup

In this section, the problem with saturation of the VSC and different solutions (stopping the integration during saturation and use of back-calculation) to avoid integrator windup will be treated.

In Section 3.2, the principle of operation of the VSC has been treated. As explained in [29], the three switching signals sw_{a}, sw_{b} and sw_{c} can be combined in eight ways. The resulting voltage vectors for these combinations draw a hexagon in the fixed $\alpha\beta$-coordinate system. Figure 3.6 shows the eight realizable voltage vectors, their switching combinations and the relative sectors for the two-level VSC. A vector $\underline{u}(sw_{\mathrm{a}}, sw_{\mathrm{b}}, sw_{\mathrm{c}})$ with switching states $sw_{\mathrm{a}} = 1$, $sw_{\mathrm{b}} = -1$ and $sw_{\mathrm{c}} = 1$ is represented as $\underline{u}(1, -1, 1)$.

The VSC is capable to deliver voltages within this hexagon. Linear modulation is possible up to the radius of the maximum circle that can be inscribed inside the hexagon. This is equal to

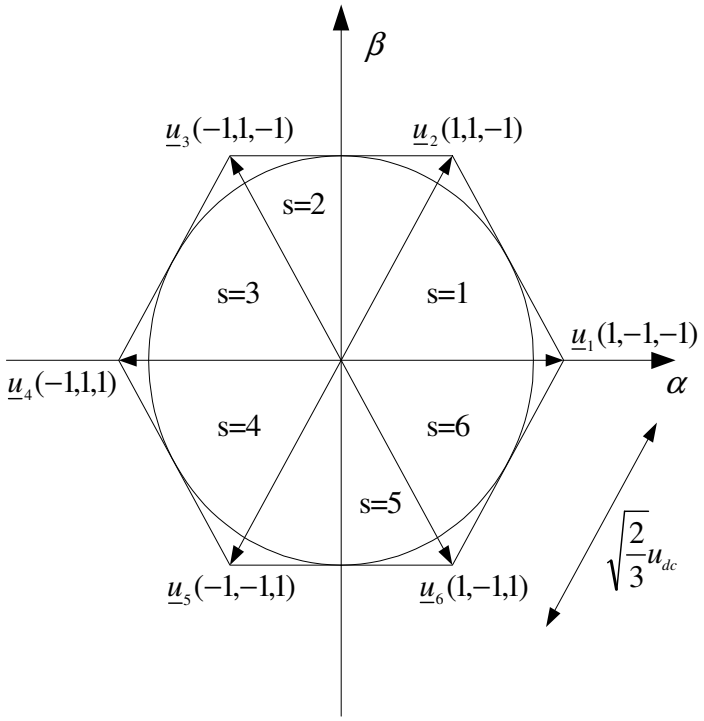


Fig. 3.6 Hexagon including the eight realizable voltage vectors for VSC.

$u_{dc}/\sqrt{2}$ if power-invariant transformation is used. During transients, it is also possible to control the PWM voltage outside this circle but within the hexagon, in order to improve the dynamic performance of the control system.

If saturation occurs (i.e. if the reference voltage vector exceeds the boundary of the hexagon), the VSC will not be able to deliver the demanded voltage and reduced performance of the system will be obtained. For this reason, in case of saturation it is necessary to reduce the demanded voltage within the boundary of the hexagon.

In [41], an extended description of the saturation problem and possible solutions for the limitation of the reference voltages for the PWM modulator are reported. Here, the method used is the Minimum Amplitude Error limitation method (MAE). According to MAE, the limited voltage vector $\underline{u}_{\mathrm{r}}^{(\alpha\beta)*}$ is chosen on the hexagon boundary nearest the original reference vector $\underline{u}^{(\alpha\beta)*}$. Thus, MAE minimizes the voltage amplitude error. As shown in Fig.3.7, using the auxiliary xy-coordinate system, the components of the limited reference voltage vector become

$$u_{\mathrm{r}x}^{*} = \frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{3.38}$$

$$u_{\mathrm{r}y}^{*} = \begin{cases} u_y^* & |u_y^*| \le u_{\mathrm{dc}}/\sqrt{6} \\ \mathrm{sgn}(u_y^*)\dfrac{u_{\mathrm{dc}}}{\sqrt{6}} & |u_y^*| > u_{\mathrm{dc}}/\sqrt{6} \end{cases} \tag{3.39}$$

The transformation angle θ_{xy} is the angle between the α-axis and the x-axis and is defined as

$$\theta_{xy} = (1 + 2(\mathrm{s} - 1))\pi/6 \tag{3.40}$$

where s is the hexagon sector where the voltage vector $\underline{u}^{(\alpha\beta)*}$ is located.

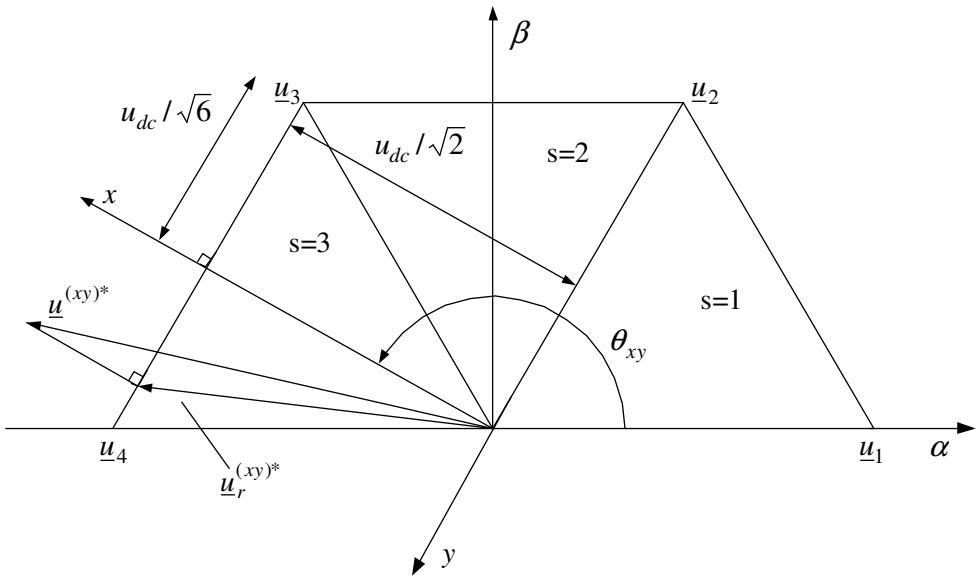


Fig. 3.7 Principle of MAE method to limit reference voltage vector to hexagon boundary.

If saturation occurs, the output voltage of the current controller will be limited to the boundary of the hexagon and the output voltage will be smaller compared with the demanded one. In this case, if a controller with an integral part is used, the current error will be integrated and, as a consequence, the integration term can become very large because the output voltage cannot be increased, thus reducing the current error. This phenomenon is called "integrator windup" [4]. Figure 3.8 shows the dynamic performance of the deadbeat vector current-controller with VSC voltage limitation and with no integrator anti-windup. At time $t = 0.1$ s a step in the d-component of the reference current from -0.5 pu to 1 pu has been applied. The q-component of the reference current (not shown for clarity) is constant to 0 pu. The signal "sat" indicates VSC saturation. As shown, the transient behavior of the control system is rather sluggish and after the step, the actual current is affected by a steady-state error that decreases slowly down to zero. The error is caused by windup of the integrator.

A countermeasure to avoid integrator windup is to inhibit the integration whenever the output of the VSC saturates. Another solution is to use a back-calculation of the current error in order to limit the demanded current during saturation [22]. In this case, if saturation occurs, the integrated current error will be modified in order to take into account the limited VSC control voltage. The back-calculated error is given by [22]

$$\underline{i}_{\mathrm{er}}^{(dq)}(k) = \frac{1}{k_{\mathrm{p}}}[\underline{u}_{\mathrm{r}}^{(dq)*}(k) - \underline{u}_{\mathrm{ff}}^{(dq)}(k) - \Delta\underline{u}_{\mathrm{i}}^{(dq)}(k)] \tag{3.41}$$

where k_{p} is the proportional gain of the controller, $\underline{u}_{\mathrm{r}}^{(dq)*}$ is the limited reference voltage vector, $\underline{u}_{\mathrm{ff}}^{(dq)}$ is the feed-forward voltage term and $\Delta\underline{u}_{\mathrm{i}}^{(dq)}$ is the integral term of the controller.

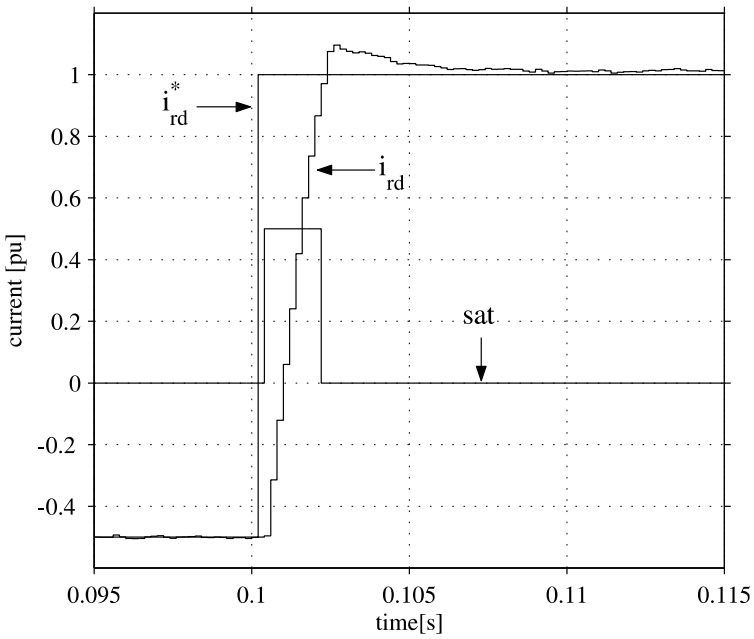


Fig. 3.8 Simulated active current response to reference active current step during VSC saturation for deadbeat current controller with no integrator anti-windup.

Figures 3.9 and 3.10 show the step response of the deadbeat vector current-controller with integrator stop and back-calculation, respectively. The two methods are practically equivalent: the advantage of using back-calculation is that if saturation occurs the integrator is not freezed, but is dynamically adjusted. Due to the presence of the integral part in the controller even during saturation, the back-calculation results slightly faster as compared with the integrator stop.

The complete block scheme of the vector current controller with all modifications mentioned is shown in Fig.3.11. From this point on, this will be referred to as vector current-controller type 1, VCC1.

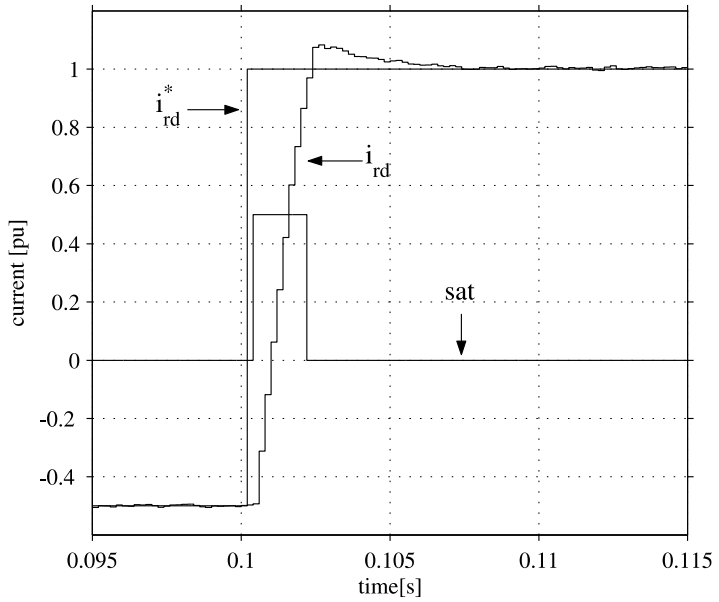


Fig. 3.9 Simulated active current response to reference active current step during VSC saturation for deadbeat current controller with integrator stop.

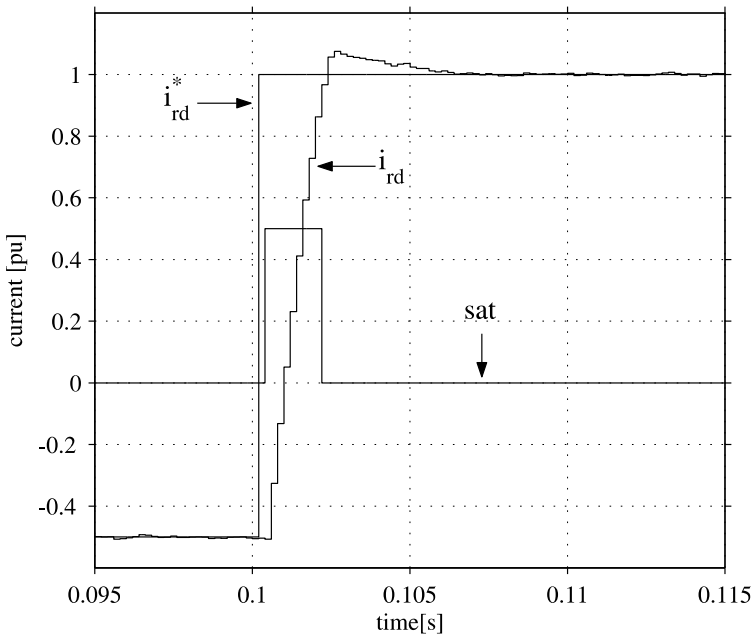


Fig. 3.10 Simulated active current response to reference active current step during VSC saturation for deadbeat current controller with back-calculation.

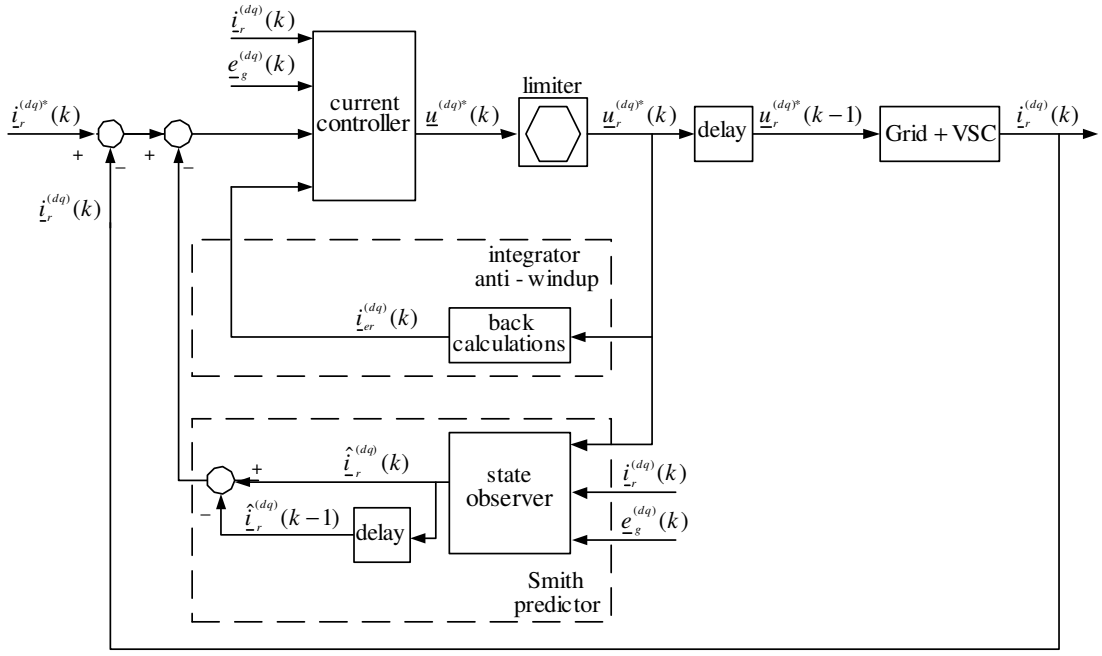


Fig. 3.11 Block scheme of the improved control system denoted by vector current-controller type 1 (VCC1).

3.2.5 Stability analysis

The performance of the entire system depends on the setting of the controller parameters. Therefore, a stability analysis is important to determine the stability margin and of course the performance.

To ensure stability and a good damping of the system, the poles of the closed-loop system should be located in the gray area shown in Fig.3.12(a) in the continuous time domain. For a discrete system, they should be located within the gray region inside a unit circle, as shown in Fig.3.12(b) [5].

In this section, the analysis of VCC1 in case of accurate knowledge of the system parameters will be carried out. The pole location for the deadbeat VCC1 when varying the observer gain k_{psp} will be analyzed. The step response and the frequency analysis of the closed-loop system for different values of the observer gain will be shown. Furthermore, the case of inaccurate knowledge of the model parameters will be considered. The effect of an inaccurate estimation of the system parameters (and especially of the filter inductance L_{r}) on the dynamic performance of the closed-loop system will be investigated.

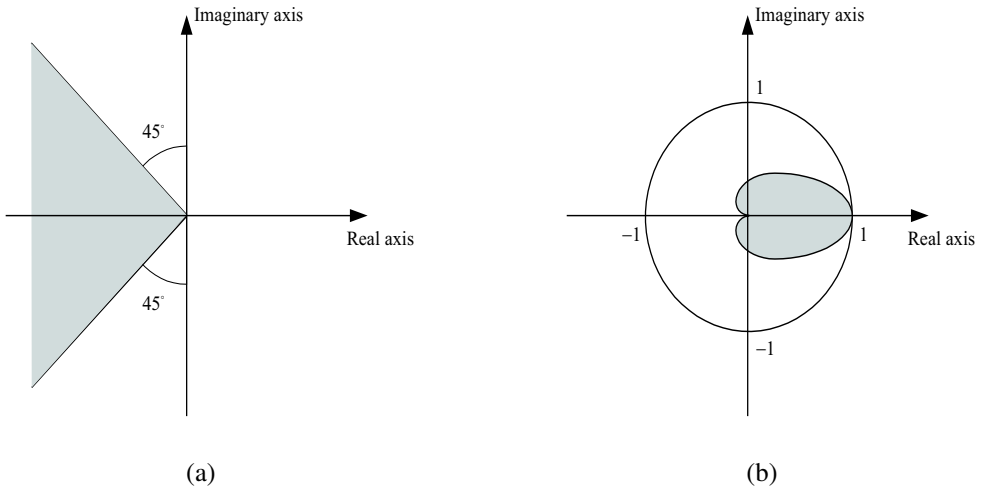


Fig. 3.12 Desired poles locus in continuous time domain, plot (a), and in discrete time domain, plot (b).

Accurate knowledge of model parameters

When the model parameters are known exactly, the current controller in Eqs.(3.27) and (3.28) contains the exact values for the filter parameters and the state observer in Eq.(3.36) is the exact reproduction of the system. The measured current $\underline{i}_{\mathrm{r}}(k)$ and the estimated current $\widehat{\underline{i}}_{\mathrm{r}}(k)$ should then be equal and the observer gain k_{psp} can be equal to zero. However, in a real system, due to non linearities and noise in the measurements, the above mentioned relation will not be true and for this reason it is necessary to introduce a non-zero gain in the state observer. Of course, this will affect the stability and the performance of the closed-loop system.

Figure 3.13 shows the pole placement of the investigated two-sample delayed system when k_{psp} varies from 0 to 0.5, under the assumption that the vector current-controller is operating at deadbeat. As shown, when increasing the observer gain, the poles move far from the real axis and the imaginary part of the complex-conjugate poles increases. It can be observed that, for observer gain equal to zero, two poles have a real part bigger than 1 and therefore are located outside the circle boundary. If the observer gain is set equal to 0.1, the control system is stable and the poles are well damped, while for 0.3 the system is still stable, but the poles are not well damped. Finally, if the state observer gain is set to 0.5 the system gets unstable.

Figures 3.14(a) to 3.14(d) show the step response of the analyzed two-sample deadbeat current controller for $k_{\mathrm{psp}} = 0$, $k_{\mathrm{psp}} = 0.1$, $k_{\mathrm{psp}} = 0.3$, and $k_{\mathrm{psp}} = 0.5$, respectively. A unity step in the d-component of the reference current has been applied at $t = 0$ and the response of the transfer function from reference d-current to actual d-current is shown. The sampling time is $T_{\mathrm{s}} = 0.2$ ms. As expected, when the observer gain is set to 0 and 0.5 the closed-loop system is unstable while for $k_{\mathrm{psp}} = 0.1$ and $k_{\mathrm{psp}} = 0.3$ the system is stable. As shown in Fig.3.14(a), when $k_{\mathrm{psp}} = 0$, since two poles are located outside (but very close to) the unit circle, the oscillation is slowly increasing. If the observer gain is instead set to 0.5 (Fig.3.14(d)), two poles are located outside the unit circle and farther from the circle boundary compared with the previous case, therefore the transfer function quickly goes into instability. For $k_{\mathrm{psp}} = 0.1$ (Fig.3.14(b))

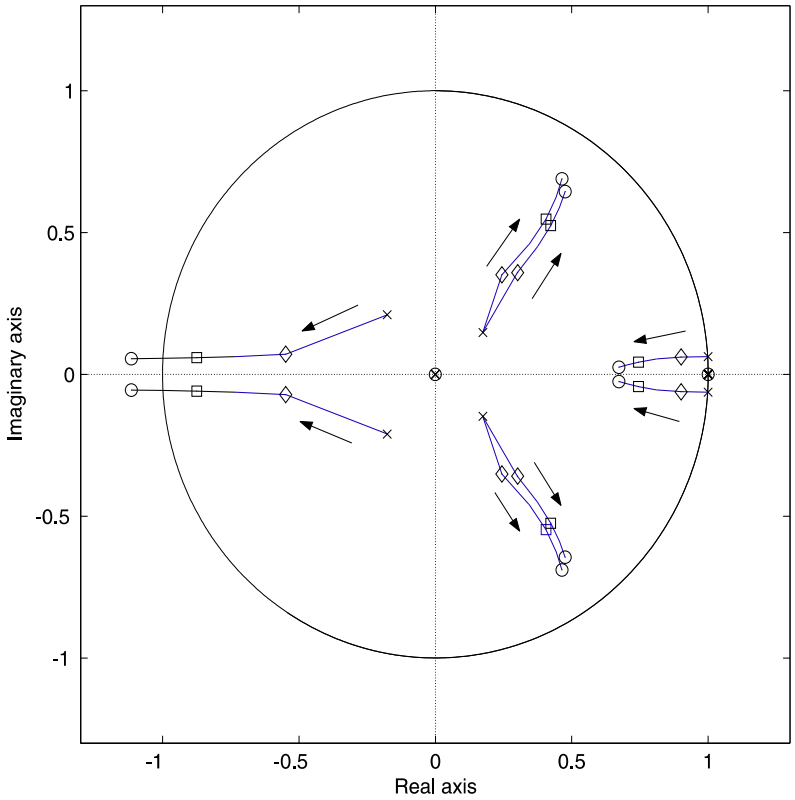


Fig. 3.13 Pole placement for accurate knowledge of system parameters at variation of observer gain. Marker "×" denotes $k_{\text{psp}} = 0$, marker "◇" denotes $k_{\text{psp}} = 0.1$, marker "□" denotes $k_{\text{psp}} = 0.3$, marker "○" denotes $k_{\text{psp}} = 0.5$.

it can be seen that at $t = 0.4$ ms, after two samples, the actual current tracks the reference, as expected for a two-sample deadbeat controller. However, the actual current is affected by a 0.1 pu overshoot, due to the cross-coupling term in the controller. If the observer gain is set to 0.3 (Fig.3.14(c)), two couples of complex and conjugate poles are outside the shadowed area shown in Fig.3.12(b), and the closed-loop system presents a stable oscillatory response with an overshoot of 0.3 pu.

Frequency analysis

As mentioned in Section 3.2, the greatest advantage when using a vector current-controller is to control the active and the reactive currents independently. Therefore, it is of interest to analyze the frequency response of the direct- and cross-coupling current of the investigated closed-loop system.

Figure 3.15 shows the Bode diagram of the transfer function from the d-component of the reference current to the d-component of the actual current for different values of the state observer gain k_{psp}. As shown, for $k_{\text{psp}} = 0$ and $k_{\text{psp}} = 0.1$ the gain is approximately one. For $k_{\text{psp}} = 0.5$, at high frequencies the gain variation is higher compared with the other two cases and presents two peaks at 750 Hz (5.5 dB) and 1.7 kHz (-6 dB). Moreover, the phase-shift is higher when k_{psp} increases for frequencies up to 1.8 kHz. The same characteristic can be obtained for the trans-

fer function from the q-component of the reference current to the q-component of the actual current.

The Bode diagram of the transfer function from the d-component of the reference current to the q-component of the actual current is displayed in Fig.3.16. The gain is in general very small. For $k_{\text{psp}} = 0.5$, the gain variation is higher compared with the other two cases. The phase presents a similar trend as in Fig.3.15, but is almost double.

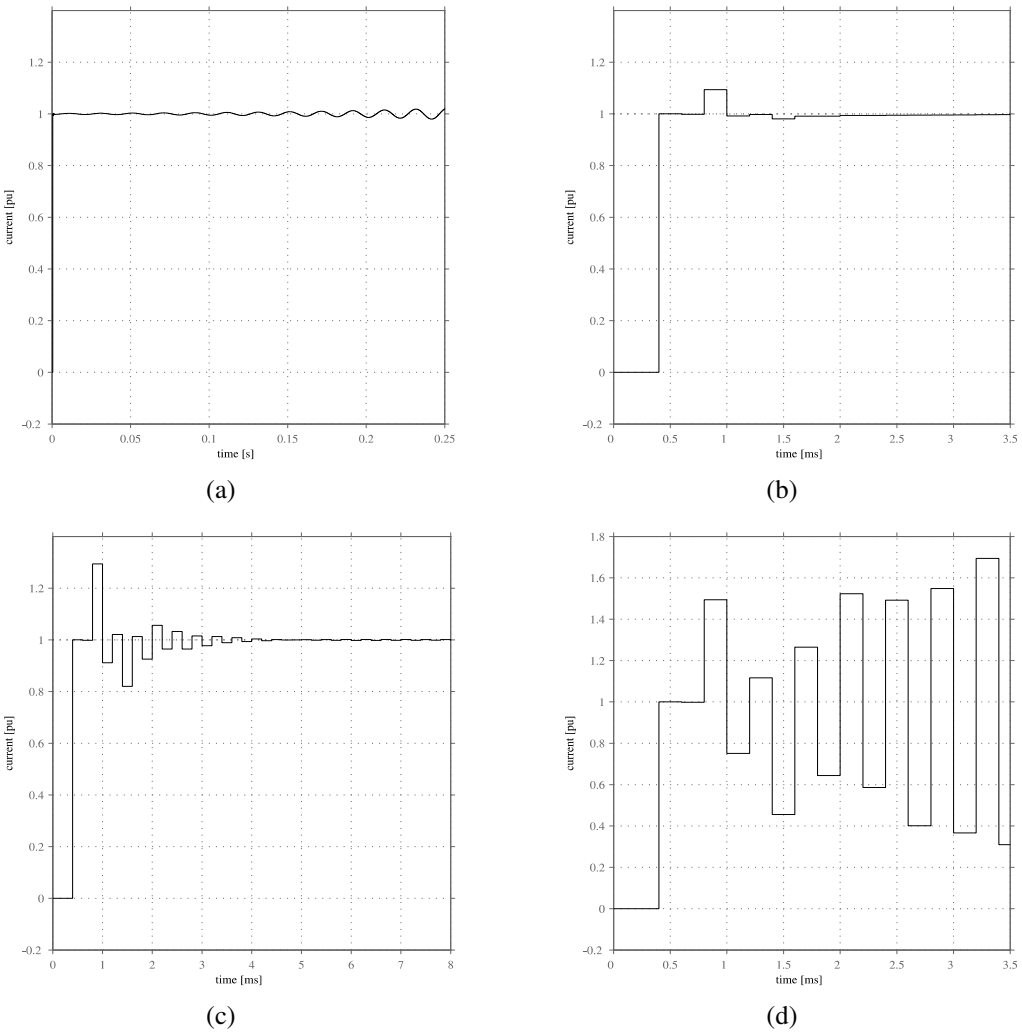


Fig. 3.14 Simulated active current step response of the VCC1 for accurate knowledge of system parameters for $k_{\text{psp}} = 0$, plot (a), $k_{\text{psp}} = 0.1$, plot (b), $k_{\text{psp}} = 0.3$, plot (c), $k_{\text{psp}} = 0.5$, plot (d).

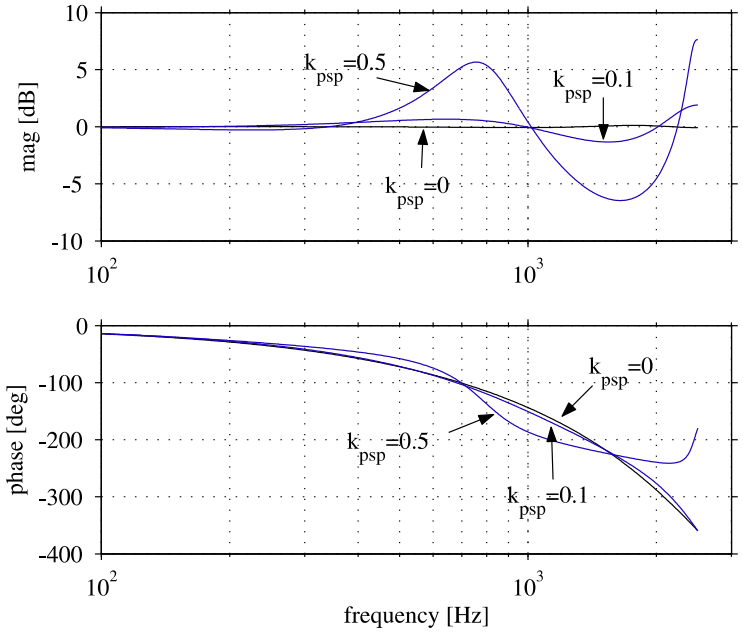


Fig. 3.15 Bode diagram from reference value of d-current Δi^*_{rd} to d-current Δi_{rd} for accurate knowledge of system parameters at variation of the observer gain.

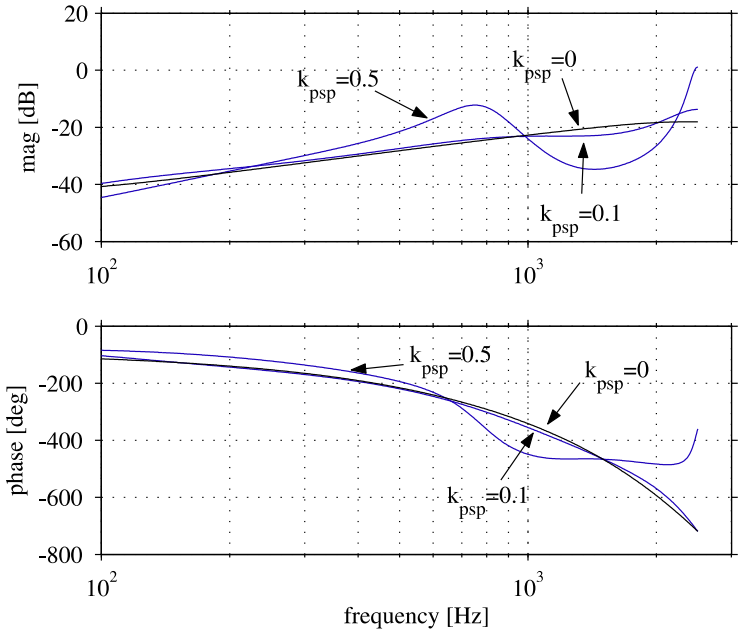


Fig. 3.16 Bode diagram from reference value of the d-current Δi^*_{rd} to q-current Δi_{rq} for accurate knowledge of system parameters at variation of the observer gain.

The harmonic content of the grid voltage will affect the output current of the VSC. Figures 3.17 and 3.18 show the Bode diagram of the transfer function from the d-component of the grid voltage to the d- and q-component of the actual current, respectively, for different k_{psp}. In all three cases, the gain of the direct-coupling increases with the frequency. As shown in Fig.3.17, for $k_{\mathrm{psp}} = 0.5$ the gain is lowest for low frequencies but increases more rapidly with a peak of 7 dB at 800 Hz. After 1.1 Hz, the gain decreases rapidly for all three cases. The cross-coupling,

instead, presents always an attenuation. Again, for $k_{\text{psp}} = 0.5$ the gain presents a higher slope with a peak of -10 dB at 800 Hz.

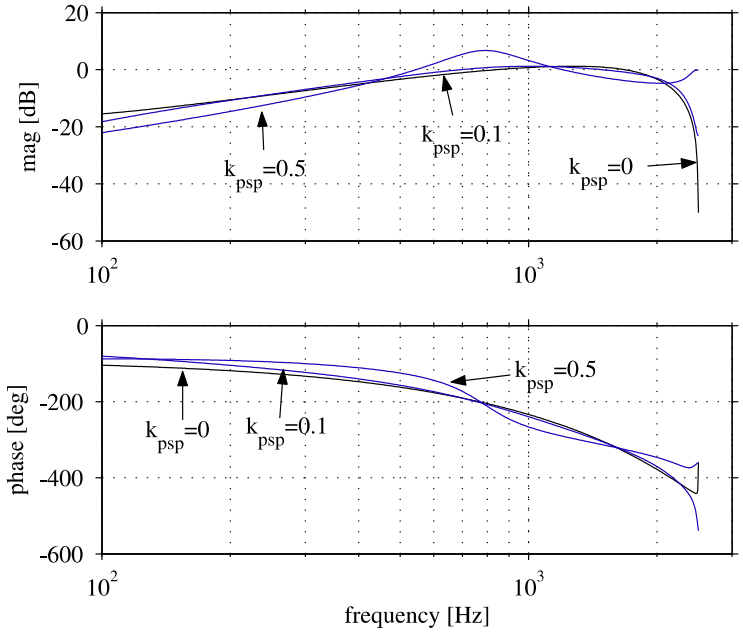


Fig. 3.17 Bode diagram from d-grid voltage Δe_{gd} to d-current Δi_{rd} for accurate knowledge of system parameters at variation of the observer gain.

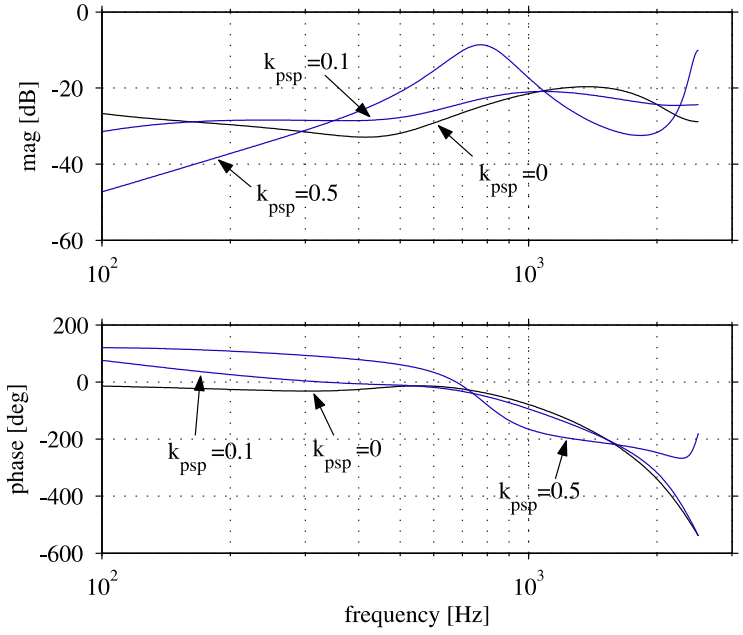


Fig. 3.18 Bode diagram from d-grid voltage Δe_{gd} to q-current Δi_{rq} for accurate knowledge of system parameters at variation of the observer gain.

Inaccurate knowledge of model parameters

For a real system, the values of the parameters are not known exactly. Moreover, some of the parameter values change during operation, due to aging or to temperature changes. Therefore, both the equation of the current controller and the equation of the state observer can be re-written considering the estimated values of the filter parameters and of the grid frequency, denoted by the superscript $\widehat{\ }$. Calling $\underline{\varepsilon}_{\mathrm{i}}^{(dq)}$ the current error, given by

$$\underline{\varepsilon}_{\mathrm{i}}^{(dq)}(k) = \underline{i}_{\mathrm{r}}^{(dq)*}(k) - \underline{i}_{\mathrm{r}}^{(dq)}(k) - \widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k) + \widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k-1) \tag{3.42}$$

the equations for the current controller and for the state observer become

$$\begin{aligned} \underline{u}^{(dq)*}(k) = \underline{e}_{\mathrm{g}}^{(dq)*}(k) + \widehat{R}_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dq)}(k) + \mathrm{j}\frac{\widehat{\omega}\widehat{L}_{\mathrm{r}}}{2}(\underline{i}_{\mathrm{r}}^{(dq)*}(k) + \underline{i}_{\mathrm{r}}^{(dq)}(k)) + \\ + k_p\underline{\varepsilon}_{\mathrm{i}}^{(dq)}(k) + \sum_{n=1}^{k} k_i\underline{\varepsilon}_{\mathrm{i}}^{(dq)}(n-1) \end{aligned} \tag{3.43}$$

$$\begin{aligned} \widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k+1) = (1 - \frac{\widehat{R}_{\mathrm{r}}T_{\mathrm{s}}}{\widehat{L}_{\mathrm{r}}} - \mathrm{j}\widehat{\omega}T_{\mathrm{s}})\widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k) + \frac{T_{\mathrm{s}}}{\widehat{L}_{\mathrm{r}}}(\underline{u}^{(dq)*}(k) - \underline{e}_{\mathrm{g}}^{(dq)}(k)) + \\ + k_{\mathrm{psp}}(\underline{i}_{\mathrm{r}}^{(dq)}(k) - \widehat{\underline{i}}_{\mathrm{r}}^{(dq)}(k)) \end{aligned} \tag{3.44}$$

where the proportional and the integral gain of the current controller are now equal to

$$k_p = \frac{\widehat{L}_{\mathrm{r}}}{T_{\mathrm{s}}} + \frac{\widehat{R}_{\mathrm{r}}}{2} \tag{3.45}$$

$$k_i = k_p\frac{T_{\mathrm{s}}}{T_i} \tag{3.46}$$

and the time constant T_i is equal to

$$T_i = \frac{\widehat{L}_{\mathrm{r}}}{\widehat{R}_{\mathrm{r}}} \tag{3.47}$$

Under these conditions, the state observer will not be able to reproduce the actual filter current. Therefore, a non-zero observer gain has to be introduced. From the results obtained in the previous analysis, an observer gain equal to 0.1 has been chosen.

Since the filter resistance is usually negligible compared with its reactance, the response of the closed-loop system is insensitive to its variation. The system is instead sensitive to variations of the filter inductance. Figures 3.19(a) to 3.19(c) show the pole placement of the closed-loop system when the estimated filter inductance $\widehat{L}_{\mathrm{r}}$ varies from 60% to 140% of the actual filter inductance L_{r}, for $k_{\mathrm{psp}} = 0.1$. The trajectory of some poles has been plotted separately for

clarity. From this figure, it is possible to observe that an underestimation of L_{r} results in a well-damped closed-loop system, while when the estimated inductance increases, the poles move far from the real axis. Therefore, it can be concluded that, in order to obtain a well-damped system, it is better to underestimate the filter inductance $\widehat{L}_{\mathrm{r}}$. According with the analysis carried out, the inductance has to be underestimated by 90% ($\widehat{L}_{\mathrm{r}}$=0.1L_{r}) for the system to go into instability, which in practice means that it will never happen.

To validate these results, the step response of VCC1 when $\widehat{L}_{\mathrm{r}} = 0.6L_{\mathrm{r}}$ and when $\widehat{L}_{\mathrm{r}} = 1.4L_{\mathrm{r}}$ has been analyzed and is shown in Figs.3.20(a) and 3.20(b), respectively. As expected, when the filter inductance is underestimated the system is well damped, while the overestimated filter inductance provides an oscillatory step response with an initial overshoot of 0.4 pu.

Finally, the sensitivity of the closed-loop system to variations of the grid frequency has been investigated. The estimated grid frequency has been varied by $\pm 10\%$ of the nominal frequency (50 Hz). The pole locus of the deadbeat VCC1 for $k_{\mathrm{psp}} = 0.1$, shown in Fig.3.21, when the estimated grid frequency $\widehat{f}$ is varied, shows that the system can be considered insensitive to normal variations of the grid frequency. This is due to the fact that the estimated frequency affects only the cross-coupling term of the current controller (see Eq.(3.43)).

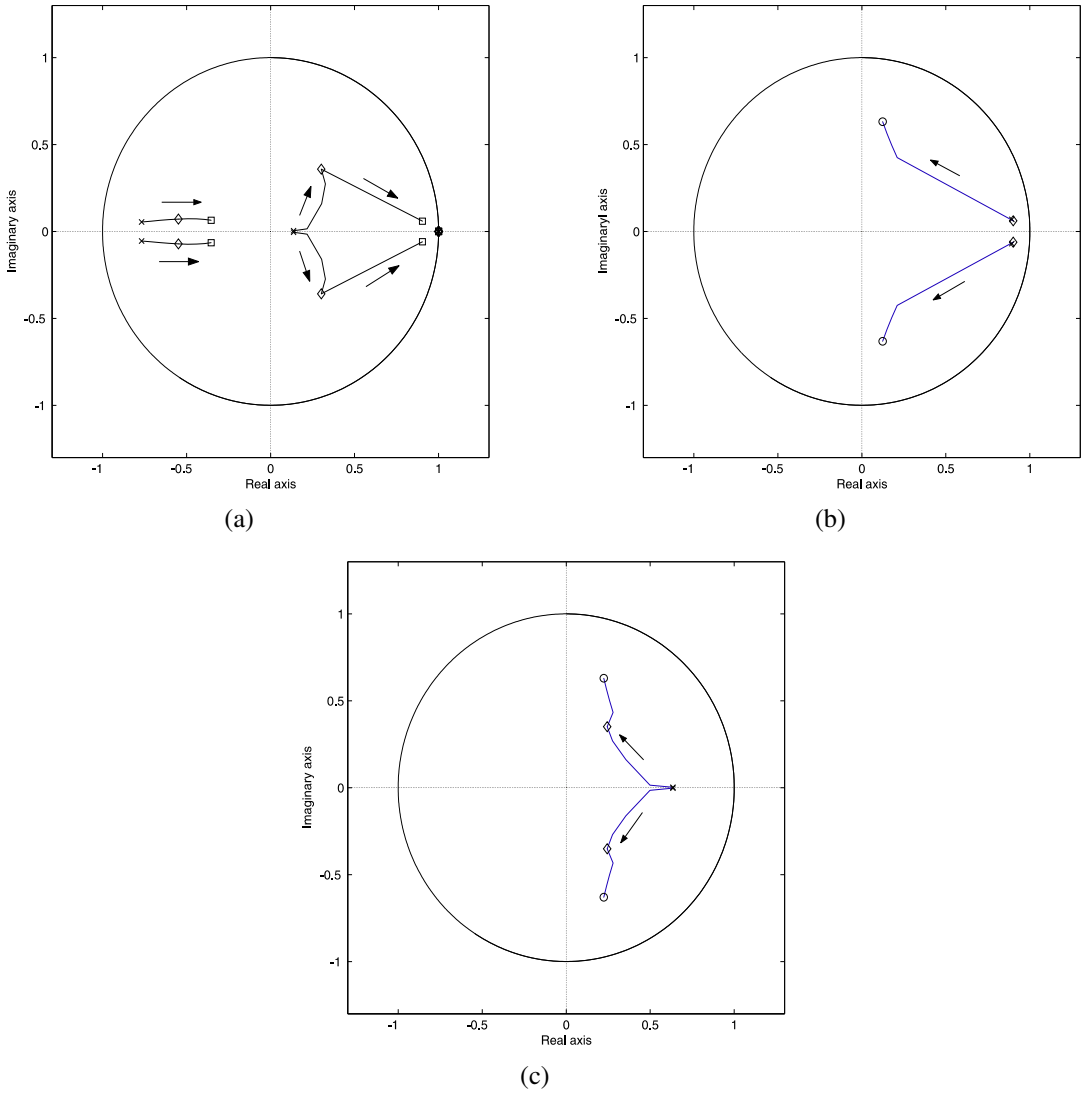
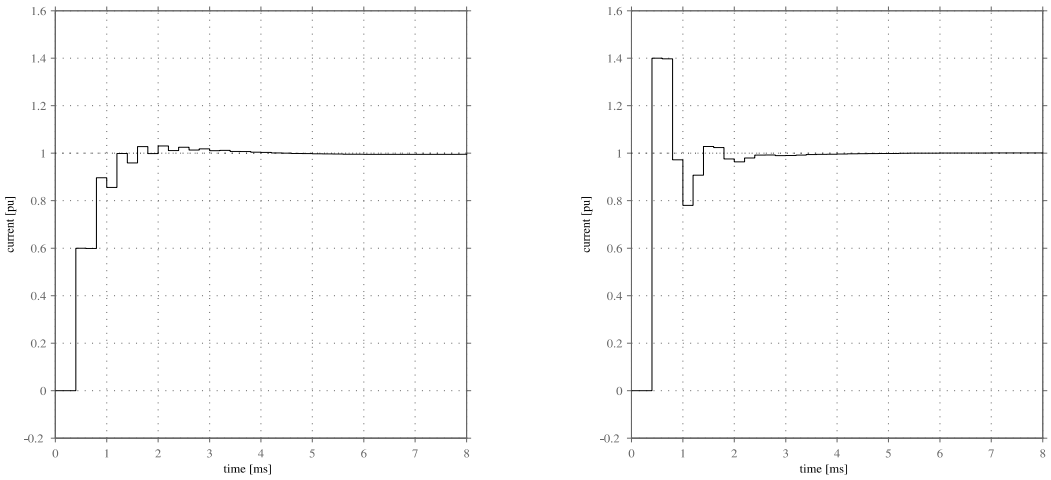


Fig. 3.19 Pole placement for inaccurate knowledge of the system parameters for $k_{\mathrm{psp}} = 0.1$ at the variation of the estimated filter inductance. Marker "$\times$" denotes $\widehat{L}_{\mathrm{r}} = 0.6L_{\mathrm{r}}$, marker "$\diamond$" denotes $\widehat{L}_{\mathrm{r}} = L_{\mathrm{r}}$, marker "$\circ$" denotes $\widehat{L}_{\mathrm{r}} = 1.4L_{\mathrm{r}}$.



(a) (b)

Fig. 3.20 Simulated active current step response of the VCC1 for $k_{\mathrm{psp}} = 0.1$ and for $\widehat{L}_{\mathrm{r}} = 0.6L_{\mathrm{r}}$, plot (a), and $\widehat{L}_{\mathrm{r}} = 1.4L_{\mathrm{r}}$, plot (b).

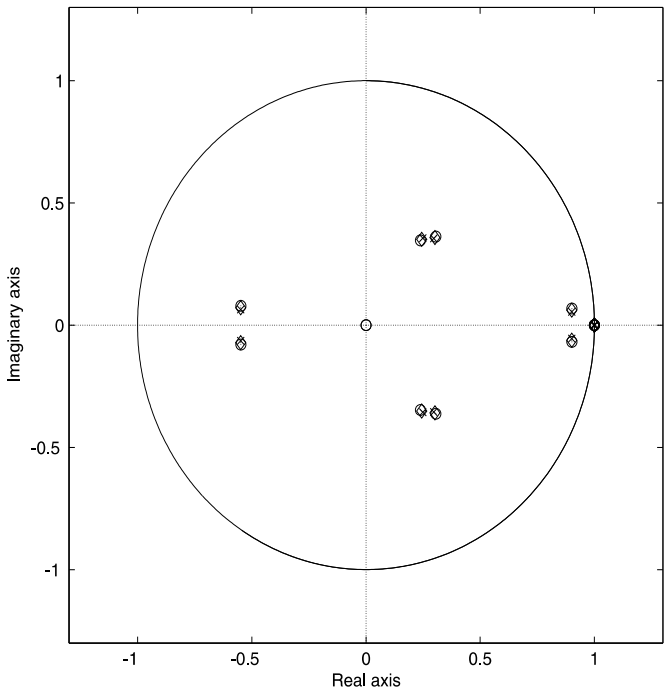


Fig. 3.21 Pole placement for inaccurate knowledge of the system parameters for $k_{\mathrm{psp}} = 0.1$ at the variation of the estimated grid frequency. Marker "$\times$" denotes $\widehat{f} = 40$Hz, marker "$\diamond$" denotes $\widehat{f} = 50$Hz, marker "$\circ$" denotes $\widehat{f} = 60$Hz.

Frequency analysis

In this section, the frequency response of the investigated closed-loop system will be investigated. From previous analysis, the system results insensitive to normal variations of the grid frequency, therefore only the frequency response of the system when varying the estimated filter inductance will be presented.

Figures 3.22 to 3.25 show the Bode diagram of the transfer function from $\Delta i^*_{\mathrm{r}d}$ to $\Delta i_{\mathrm{r}d}$, from $\Delta i^*_{\mathrm{r}d}$ to $\Delta i_{\mathrm{r}q}$, from $\Delta e_{\mathrm{g}d}$ to $\Delta i_{\mathrm{r}d}$ and from $\Delta e_{\mathrm{g}d}$ to $\Delta i_{\mathrm{r}q}$ when the ratio between the estimated and the actual filter inductance $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}}$ is equal to 1 (denoted in the figure by $L_{1.0}$), 0.6 (denoted in the figure by $L_{0.6}$) and 1.4 (denoted in the figure by $L_{1.4}$), respectively. As shown, the gain changes ± 3 dB at 300 Hz and equals the gain for $\widehat{L}_{\mathrm{r}} = L_{\mathrm{r}}$ between 500 Hz and 600 Hz for the transfer function $\Delta e_{\mathrm{g}d}$ to $\Delta i_{\mathrm{r}d}$. When the inductance is overestimated, the gain has a peak of 5 dB at 1 kHz. Further, the Bode diagram of the transfer function from $\Delta e_{\mathrm{g}d}$ to $\Delta i_{\mathrm{r}q}$ shows that for low frequencies the gain is higher when underestimating the filter inductance, while for frequencies higher that 700 Hz the gain for overestimated inductance increases rapidly with a peak of -12 dB at 1.1 kHz. For the transfer function from $\Delta i^*_{\mathrm{r}d}$ to $\Delta i_{\mathrm{r}d}$ the gain fluctuation is ± 7 dB when going from $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}} = 0.6$ to $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}} = 1.4$, while the transfer function of the cross-coupling term, from $\Delta i^*_{\mathrm{r}d}$ to $\Delta i_{\mathrm{r}q}$, is similar to the cross-coupling term from $\Delta e_{\mathrm{g}d}$ to $\Delta i_{\mathrm{r}q}$: the gain is highest for $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}} = 0.6$ for frequencies lower that 370 Hz, for $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}} = 1.4$ otherwise.

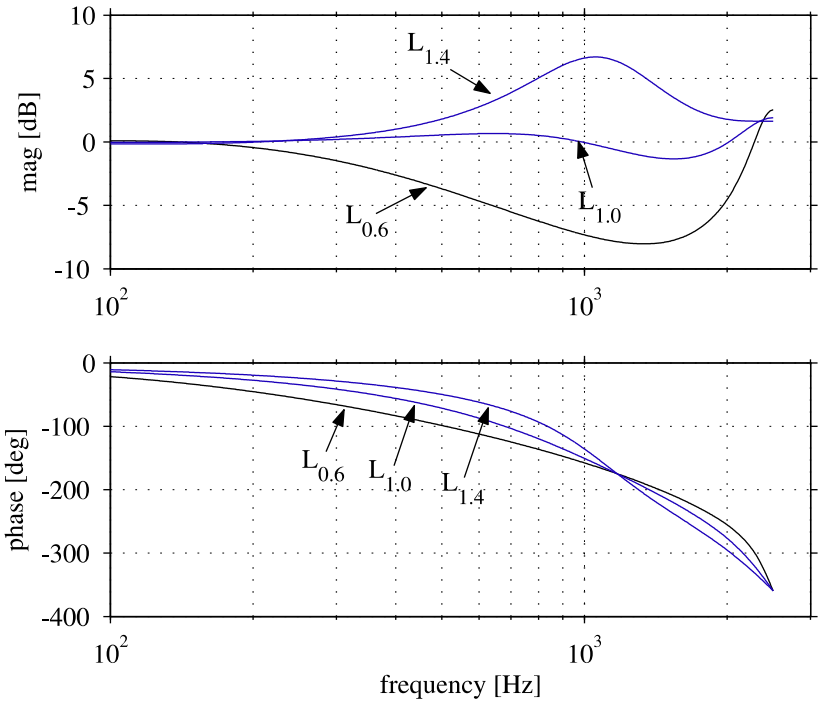


Fig. 3.22 Bode diagram from reference value of d-current $\Delta i^*_{\mathrm{r}d}$ to d-current $\Delta i_{\mathrm{r}d}$ for inaccurate knowledge of filter inductance.

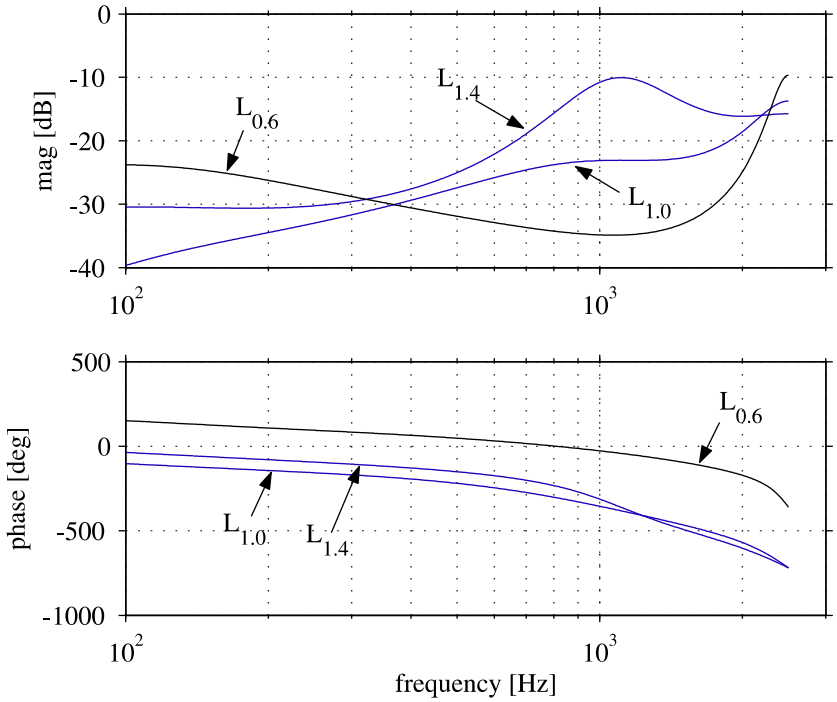


Fig. 3.23 Bode diagram from reference value of d-current Δi^*_{rd} to q-current Δi_{rq} for inaccurate knowledge of filter inductance.

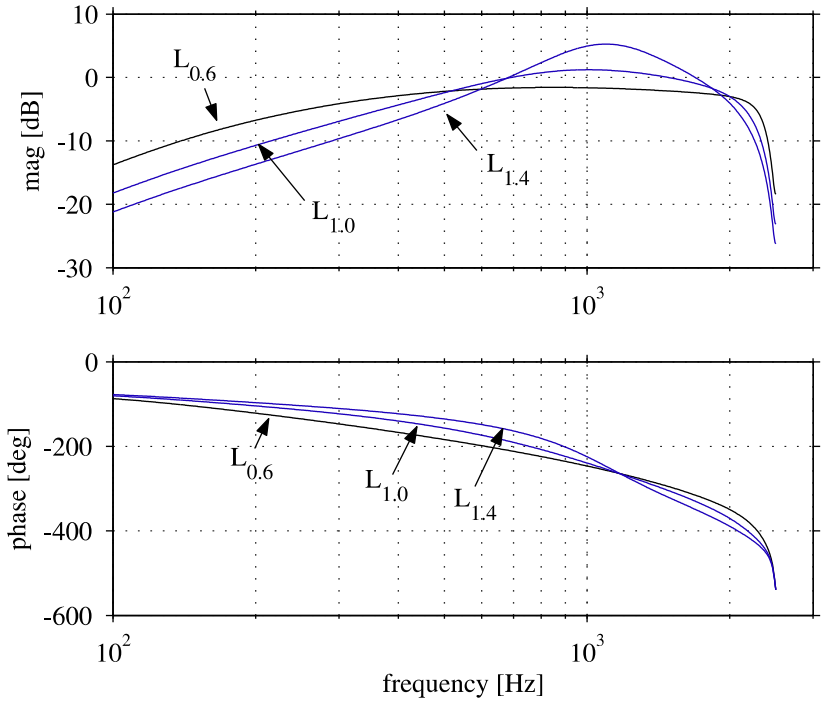


Fig. 3.24 Bode diagram from d-grid voltage Δe_{gd} to d-current Δi_{rd} for inaccurate knowledge of filter inductance.

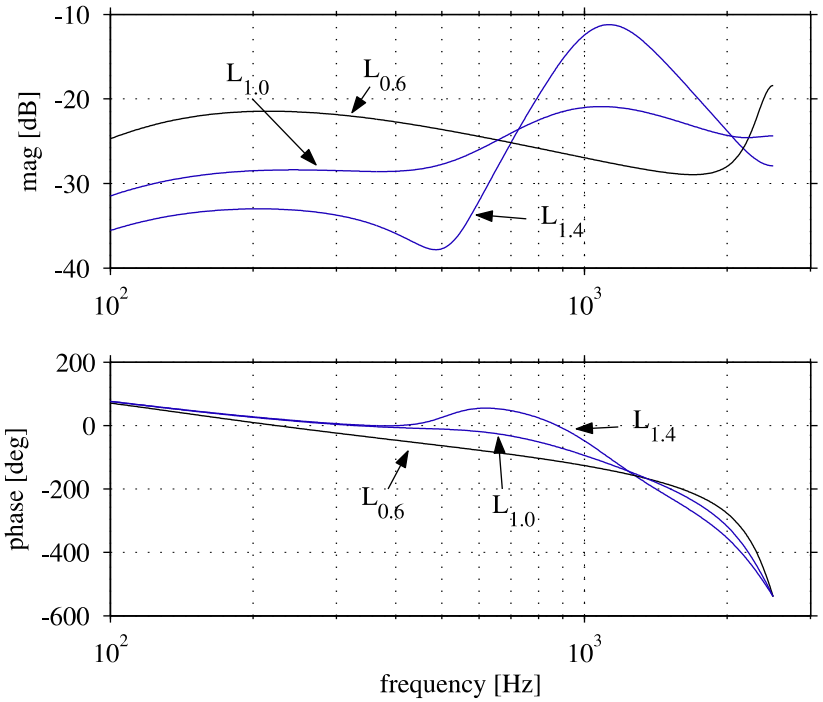


Fig. 3.25 Bode diagram from d-grid voltage Δe_{gd} to q-current Δi_{rq} for inaccurate knowledge of filter inductance.

3.2.6 Simulation results using VCC1

In this section, simulation results for the shunt-connected VSC with VCC1 will be presented. Simulations have been carried out by using the simulation program PSCAD/EMTDC by Manitoba and the complete discrete control system has been implemented in discrete-time domain by using Fortran 90 language [27].

The transient performance of VCC1 has been tested by applying steps in the active and reactive reference current under balanced and unbalanced conditions of the grid voltage. The control system has also been tested under symmetrical and unsymmetrical voltage dips.

The model reproduces a prototype of the shunt-connected VSC that has been built in the Power System Laboratory at the Department of Electric Power Engineering of Chalmers University. System parameters are reported in Table 3.1 and controller parameters for VCC1 are reported in Table 3.2. In applications where the VSC in connected to a grid, the PLL must keep track

TABLE 3.1. SYSTEM PARAMETERS FOR VCC1.

Grid voltage	E = 400 V = 1 pu	Grid current	I = 40 A = 1 pu
Grid frequency	f = 50 Hz	DC-link voltage	U_{dc} = 600 V = 1.5 pu
Filter resistance	R_{r} = 24.8 mΩ = 0.0025 pu	Filter inductance	L_{r} = 2 mH = 0.0628 pu

of the fundamental component of the grid voltage, but it must be insensitive to its harmonics. For this reason, the bandwidth of the PLL must be very low [40]. However, this will result in

TABLE 3.2. CONTROLLER PARAMETERS FOR VCC1.

Sampling frequency	f_{s} = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Proportional gain	k_{p} = 10.01 (deadbeat)	Integrator time constant	T_{i} = 0.0806 s
Observer gain	k_{psp} = 0.1		

long time for tracking. For this reason, in these simulations, an instantaneous PLL, based on the following equation, has been used

$$\theta(k) = \mathrm{atan2}(e_{\mathrm{g}\beta}(k), e_{\mathrm{g}\alpha}(k)) \tag{3.48}$$

Simulations with balanced grid voltage

Simulated grid voltages in the three-phase coordinate system plotted in Fig.3.26 are sinusoidal and with constant amplitude equal to 1 pu. The grid voltages are constant in the dq-coordinate system, as displayed in Fig.3.27. After 0.02 s, a step of 0.375 pu in the active current $i_{\mathrm{r}d}$ with duration 0.04 s is applied. The reactive current $i_{\mathrm{r}q}$ is constant and equal to 0.25 pu. Due to the variation of the demanded power, the q-component of the reference voltage for the VSC steps up from 0 pu to 0.035 pu, while the d-component remains constant at 1 pu (see Fig.3.28). Figure 3.29 shows the current response to the step. The actual current tracks the reference current in two samples (0.4 ms), as displayed in Fig.3.30, which shows a detail of the transient response of VCC1. It can be noticed that there is a small cross-coupling between the d- and the q-component of the current at the beginning and at the end of the step.

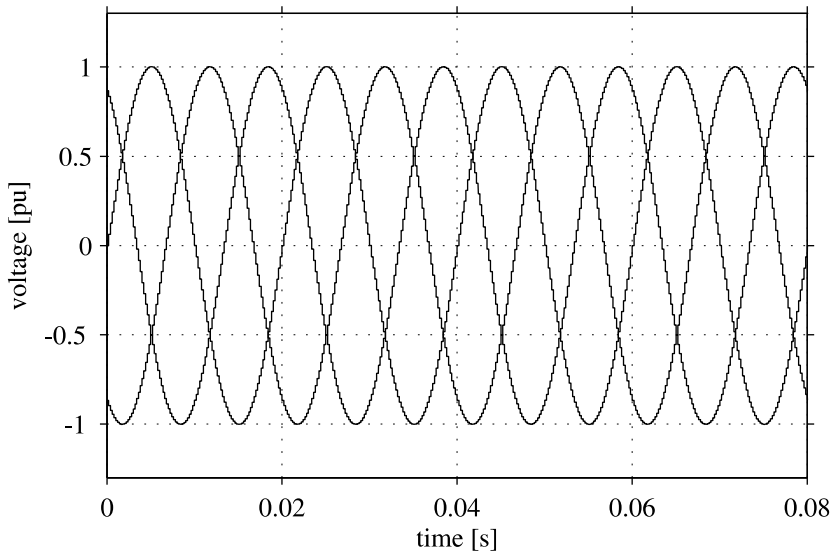


Fig. 3.26 Simulated three-phase balanced grid voltages.

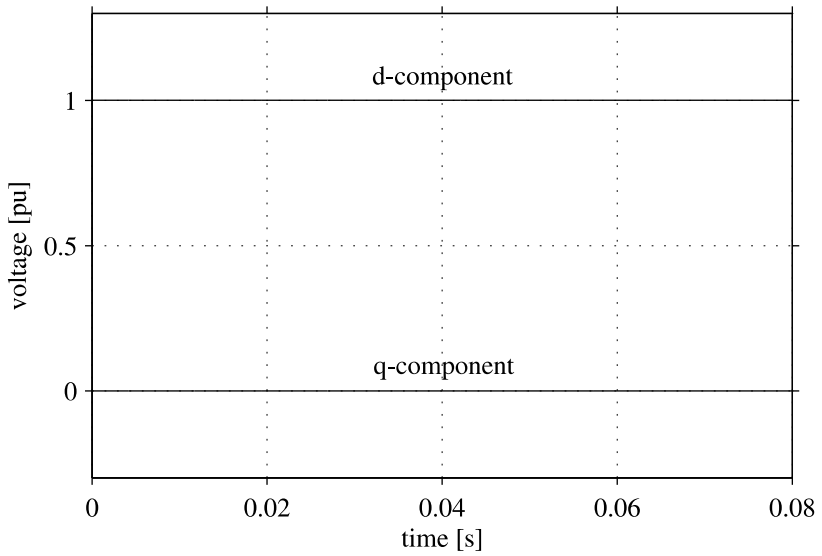


Fig. 3.27 Simulated balanced grid voltages in dq-coordinate system.

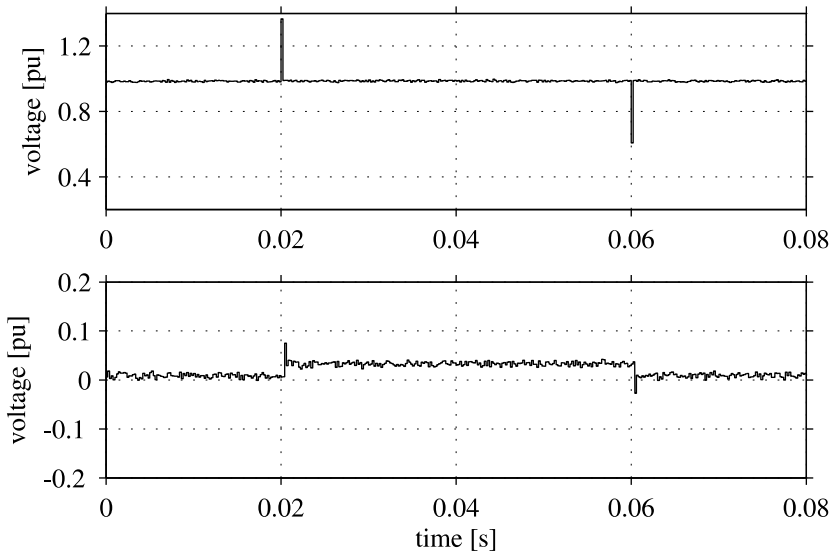


Fig. 3.28 Simulated reference voltages for VSC due to reference active current step. VCC1 and balanced grid voltage are used. Top: d-component; bottom: q-component.

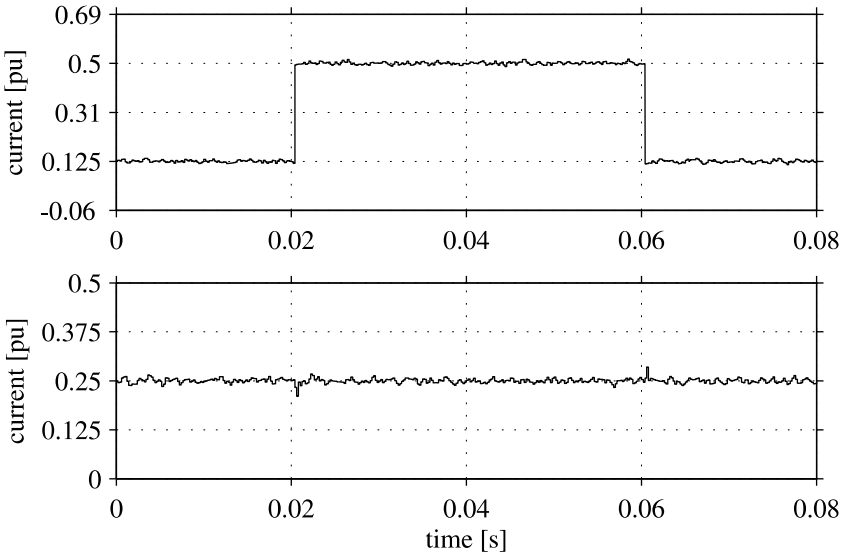


Fig. 3.29 Simulated active and reactive current response to reference active current step. VCC1 and balanced grid voltage are used. Top: d-component; bottom: q-component.

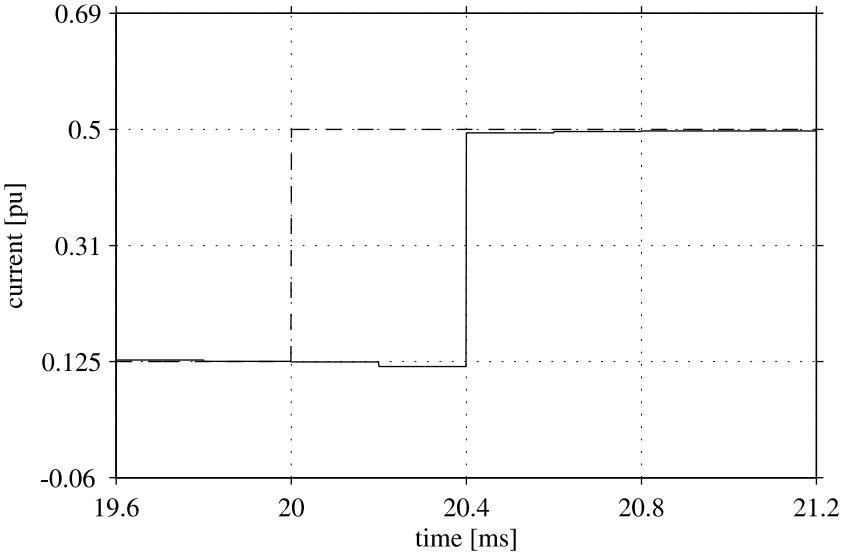


Fig. 3.30 Simulated active current response to reference active current step. VCC1 and balanced grid voltage are used. Dashed: $i^*_{\mathrm{r}d}$; solid: $i_{\mathrm{r}d}$.

The step response of active and reactive current due to a step in the reference reactive current is shown in Fig.3.31. The operating point is $i_{\mathrm{r}d} = 0.25$ pu and $i_{\mathrm{r}q} = 0.125$ pu. After 0.02 s, the reference reactive current makes a step with amplitude 0.375 pu and duration 0.04 s. Once more, the control system works properly and manages to track the current references with a delay of two samples, as displayed in Fig.3.32.

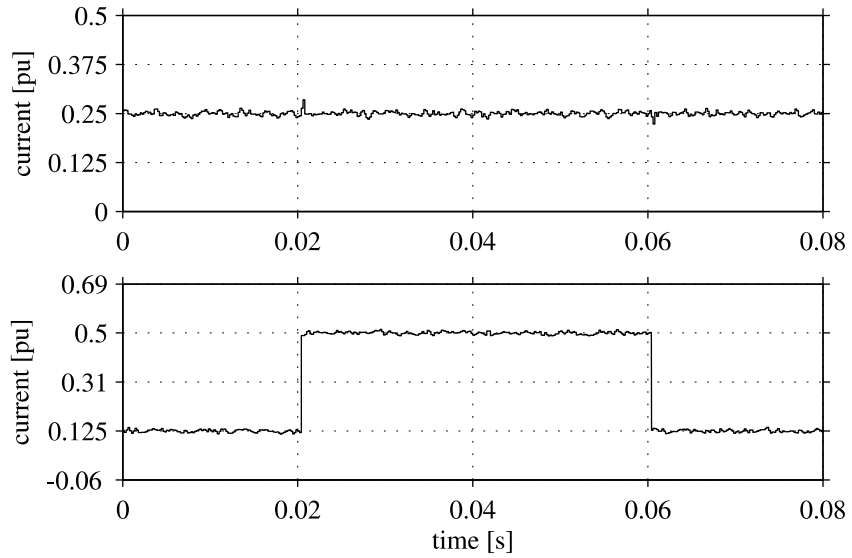


Fig. 3.31 Simulated active and reactive current response to reference reactive current step. VCC1 and balanced grid voltage are used. Top: d-component; bottom: q-component.

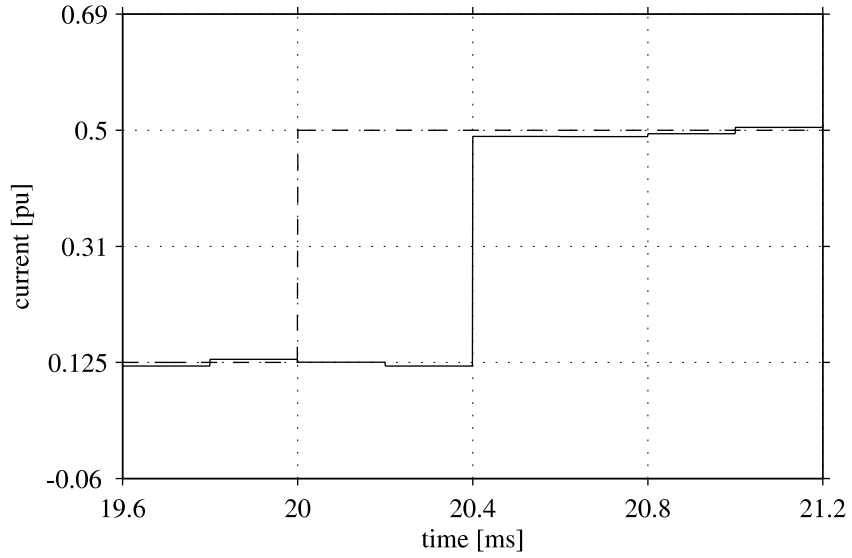


Fig. 3.32 Simulated reactive current response to reference reactive current step. VCC1 and balanced grid voltage are used. Dashed: $i_{\mathrm{r}q}^{*}$; solid: $i_{\mathrm{r}q}$.

Simulations with unbalanced grid voltage

The controller has been tested under unbalanced grid voltage by applying the same steps in active and reactive current as in the previous section. Simulated phase-voltages of the grid are shown in Fig.3.33. The amplitude of the phase voltage is equal to 1 pu for one phase and to 0.71 pu for the other two phases. The voltages in the dq-coordinate system, shown in Fig.3.34, are affected by a 100 Hz oscillation due to the grid unbalance. The amplitude of this oscillation is equal to the negative-sequence component, as explained in Appendix A. The active and reactive currents in the dq-coordinate system, shown in Fig.3.35 and Fig.3.36, respectively, during steps in active and reactive power, are also affected by a 100 Hz oscillation of 0.06 pu (peak-to peak) around the steady-state value. It has been proven via simulation, by varying one parameter at the time, that the amplitude of these oscillations, which is constant before, during and after the step, depends on the grid voltage level at the PCC, on the percentage of unbalance and on the size of the filter reactor (see Fig.3.37(a)). Moreover, it depends on the sampling frequency (Fig.3.37(b)), but is not dependent on the settings of the PI-regulator. Note that when varying the filter inductance and the sampling frequency, the other parameters of the system have been maintained constant as in Table 3.1. The relative controller gains are the same for all cases.

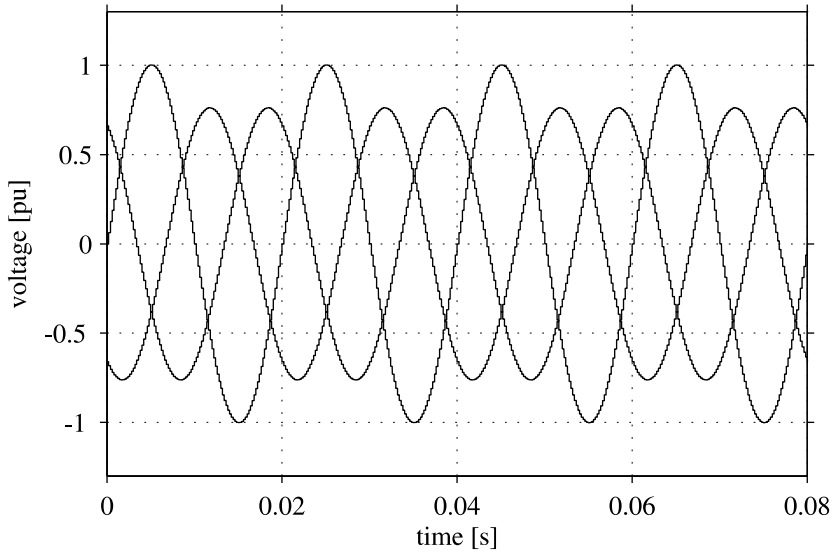


Fig. 3.33 Simulated three-phase unbalanced grid voltages.

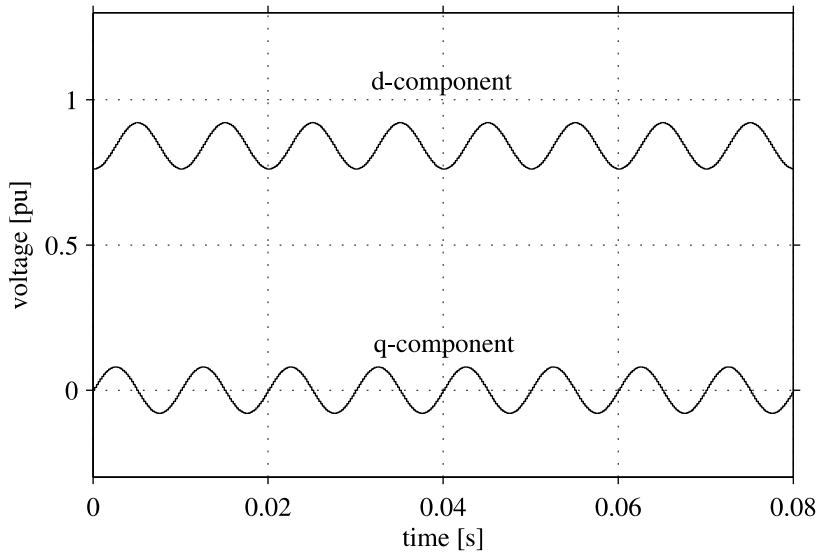


Fig. 3.34 Simulated unbalanced grid voltages in dq-coordinate system.

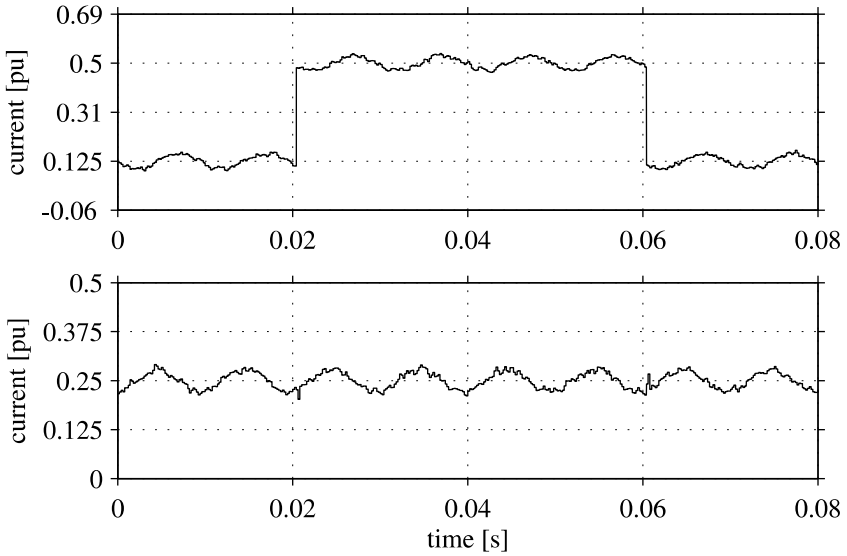


Fig. 3.35 Simulated active and reactive current response to active current step. VCC1 and unbalanced grid are used. Top: d-component; bottom: q-component.

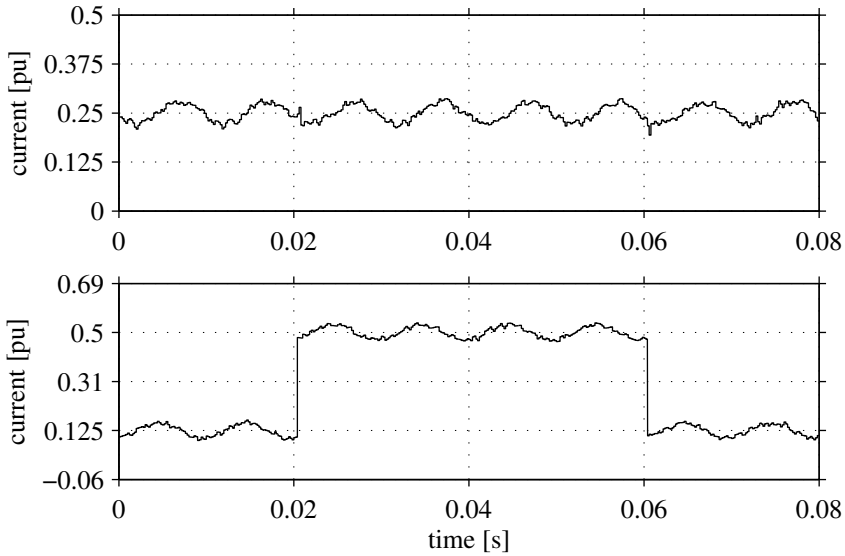


Fig. 3.36 Simulated active and reactive current response to reactive current step. VCC1 and unbalanced grid are used. Top: d-component; bottom: q-component.

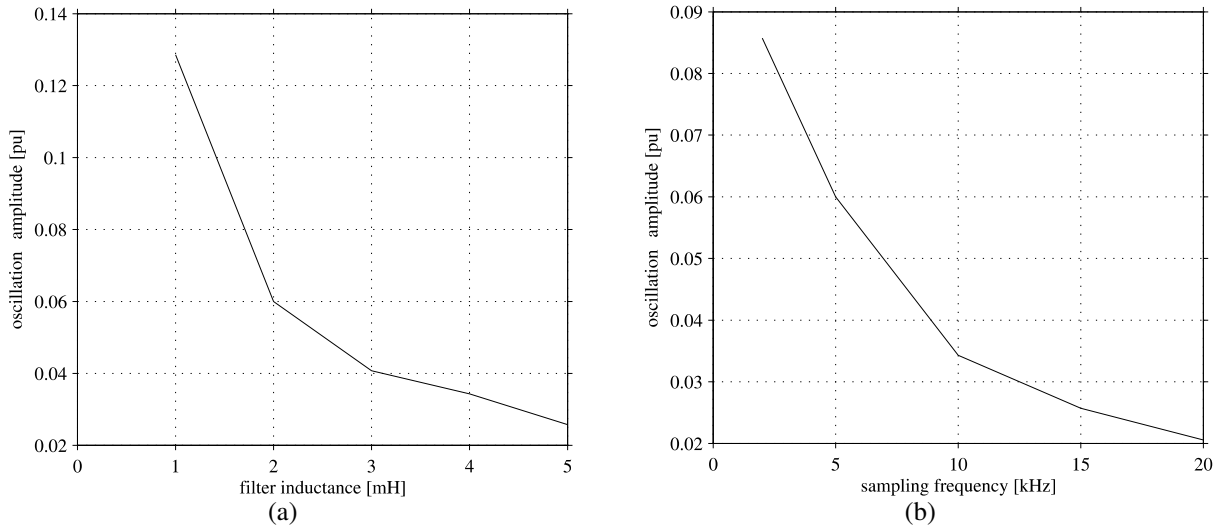


Fig. 3.37 Amplitude of 100 Hz current oscillations under unbalanced conditions of grid voltage. Oscillation amplitude vs. filter inductance: plot (a); oscillation amplitude vs. sampling frequency: plot (b).

Voltage dip response

Finally, the VCC1 has been tested under voltage dips. A 70% three-phase balanced voltage dip with duration of 300 ms has been applied at $t = 0.03$ s. Figure 3.38 shows the three-phase grid voltage at PCC, while the grid voltages in the dq-coordinate system are in Fig.3.39. The operating point is $i_{\mathrm{rd}} = 0.125$ pu and $i_{\mathrm{rq}} = 0.25$ pu, as displayed in Fig.3.40. Despite the sudden voltage drop, the control system manages to keep the current constant to the pre-fault values. However, there is an overshoot of 0.6 pu with duration of 1 ms in the active current, which is due to the rapid variation of the grid voltage. A similar transient can be observed at the end of the dip (not shown in the figure for clarity). Different countermeasures to reduce the amplitude and duration of this overshoot can be adopted.

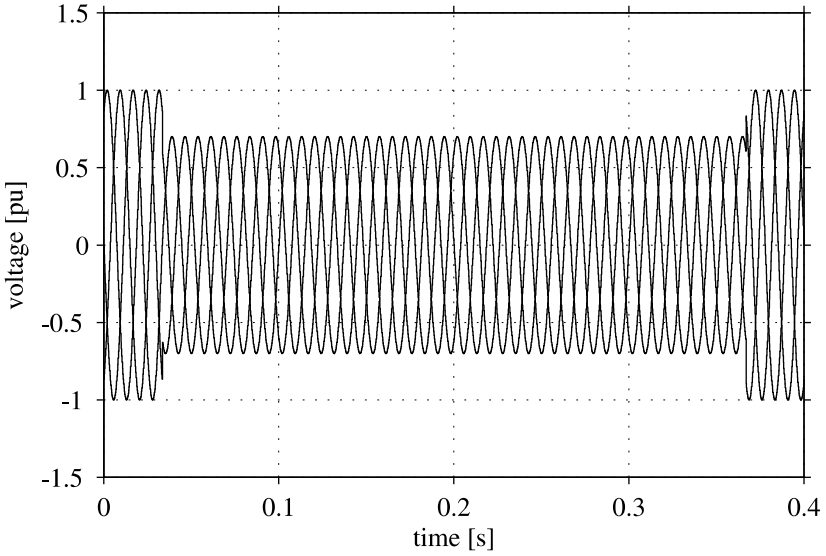


Fig. 3.38 Simulated three-phase grid voltages system during 70% balanced voltage dip.

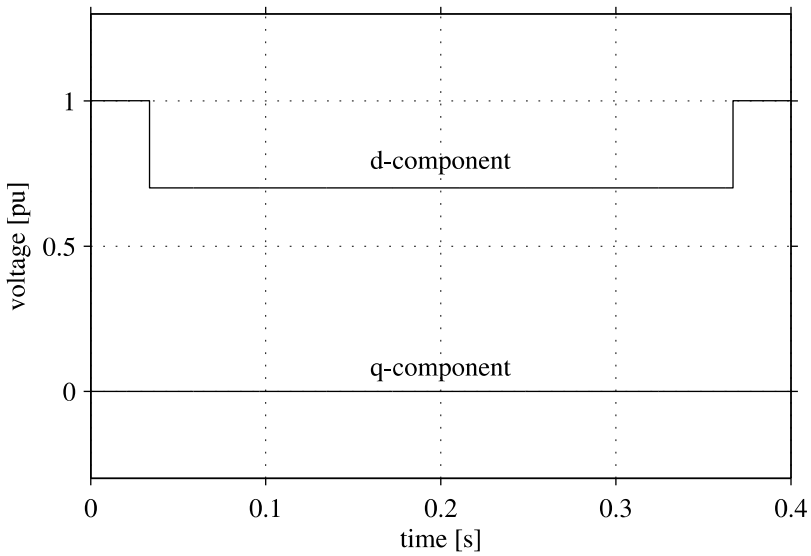


Fig. 3.39 Simulated grid voltages in dq-coordinate system during 70% balanced voltage dip.

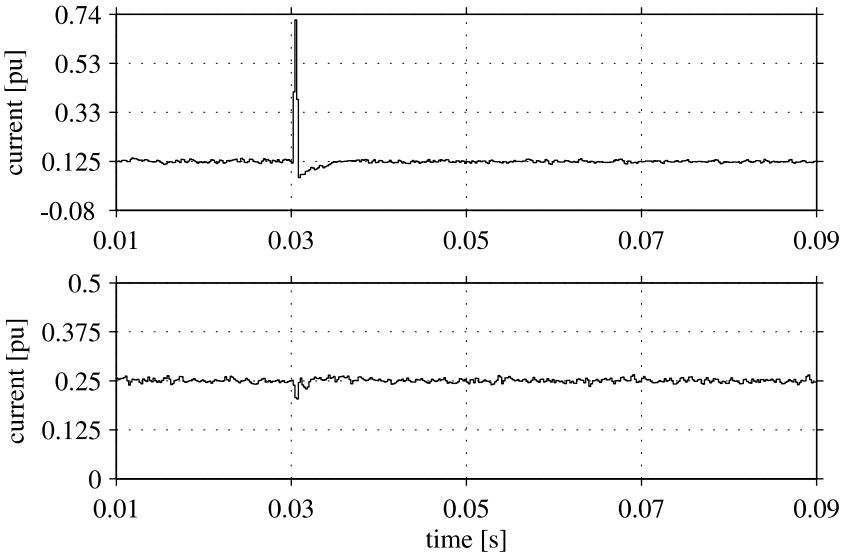


Fig. 3.40 Simulated active and reactive current response of VCC1 to 70% balanced voltage dip. Top: d-component; bottom: q-component.

The current variation depends on the voltage level at the PCC, on the magnitude of the voltage dip and on the grid impedance. For example, by increasing the capacitance in the grid, the voltage variation will be slower, resulting in a smaller overshoot. However, normally it is not possible to change the grid parameters, but only the parameters of the device and of the control system.

In Fig.3.41, details of the current spike due to the voltage dip for different values of the filter parameters are displayed. As shown, when increasing the size of the filter reactor, both amplitude and duration of the overshoot at the beginning of the dip are reduced.

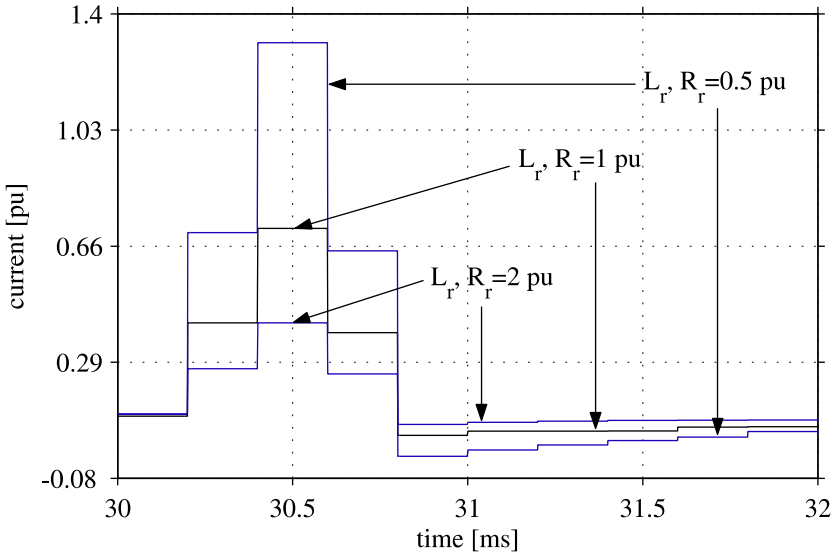


Fig. 3.41 Simulated active current at beginning of balanced voltage dip with VCC1 and different values of filter parameters L_r and R_r.

If only modifications in the controller parameters are possible, a way to reduce the overshoot is to increase the sampling frequency f_s of the control system. Figure 3.42 shows the current spike at the beginning of the dip when the sampling frequency is set to 10 kHz, 5 kHz and 2.5 kHz. As expected, when increasing the sampling frequency both the amplitude and the duration of the overshoot will be reduced. It is of interest to observe that, by changing the parameters of the PI-regulator, the amplitude of the overshoot will be constant but its duration is reduced when fast controllers are used, as displayed in Fig.3.43.

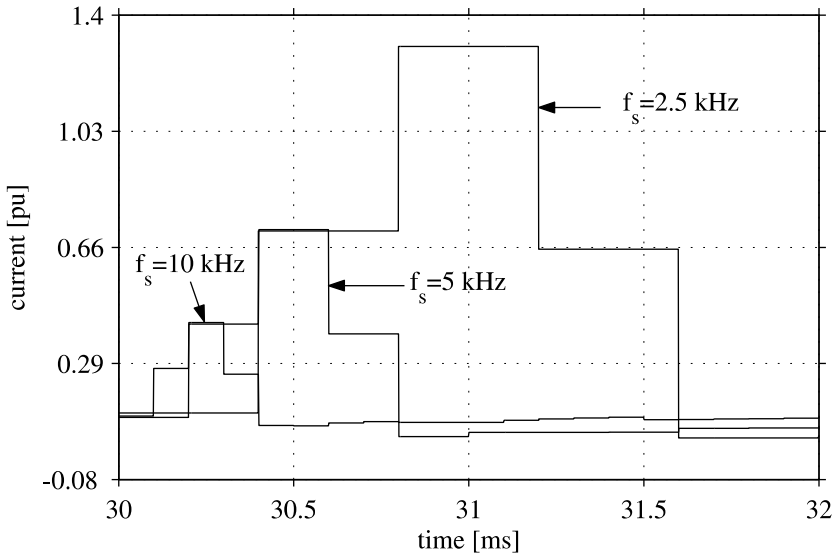


Fig. 3.42 Simulated active current at beginning of balanced voltage dip with VCC1 and different values of sampling frequency f_s.

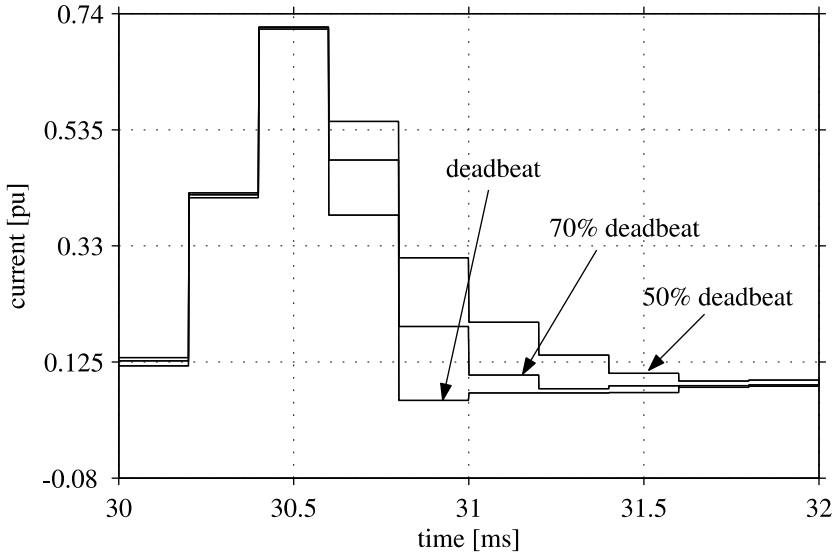


Fig. 3.43 Simulated active current at beginning of balanced voltage dip with VCC1 and different values of PI-parameters.

The control system has also been tested under unbalanced voltage dips. As shown in Fig.3.44, at $t = 0.03$ s an unbalanced 80% voltage dip with unbalance of 10.9% and duration of 300 ms has been applied to the grid voltage. Due to the presence of a negative-sequence component during the dip, the grid voltages in the dq-coordinate system are affected by a 100 Hz oscillation, as shown in Fig.3.45.

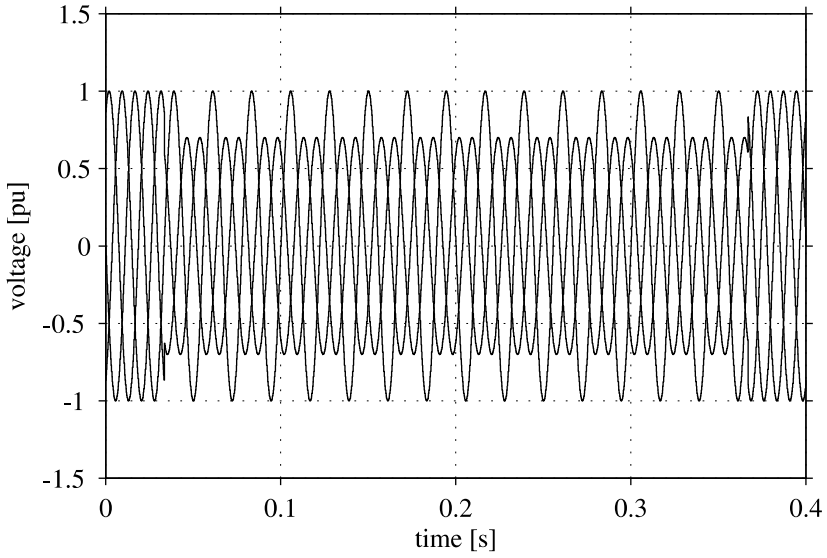


Fig. 3.44 Simulated three-phase grid voltages during 80% voltage dip with unbalance of 10.9%.

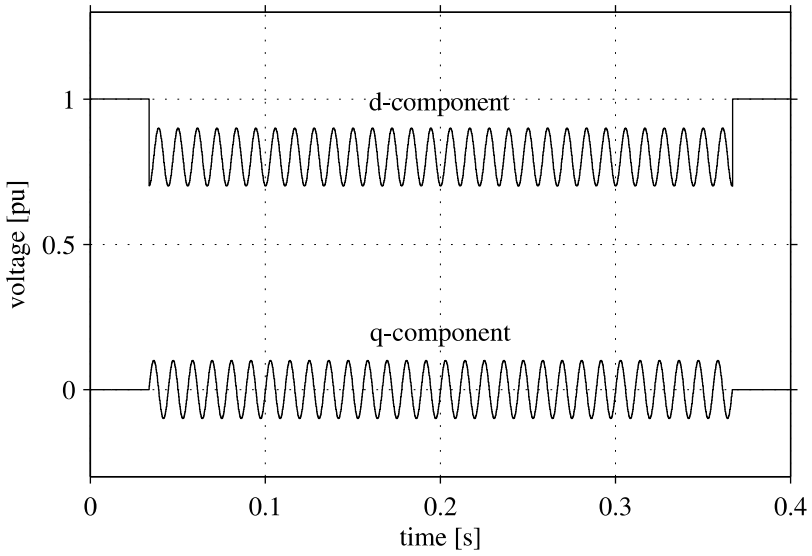


Fig. 3.45 Simulated grid voltages in dq-coordinate system during 80% voltage dip with unbalance of 10.9%.

As expected, during an unbalanced voltage dip the control system cannot keep the pre-fault conditions for the current, as shown in Fig.3.46. Besides the 100 Hz oscillation observed with unbalanced grid voltages (Figs.3.35 and 3.36), there is also an overshoot at the beginning of the dip, as in the case of balanced dip.

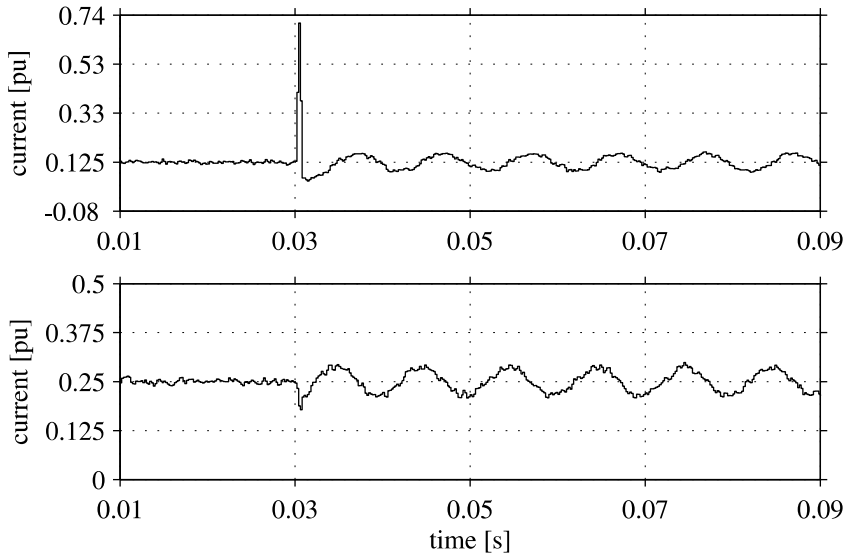


Fig. 3.46 Simulated active and reactive current response of VCC1 to 80% voltage dip with unbalance of 10.9%. Top: d-component; bottom: q-component.

3.2.7 Summary

In this section, the vector current-controller for shunt-connected VSC has been presented. Different problems related to this controller and possible solutions have been discussed. The improved vector current-controller, VCC1, has been tested via simulations under balanced and unbalanced conditions of the grid voltage by applying steps in the active and reactive current. Moreover, the transient performance of the VCC1 under balanced and unbalanced voltage dips has been investigated. The transient overshoot in the current due to the fast voltage variation at the beginning of the dip has been proven to depend on the filter parameters and on the sampling frequency. Moreover, it has been proven that variations in the parameters of the PI-regulator will affect the duration of this overshoot, but not its amplitude.

Simulation results show that the VCC1 operates properly only under balanced conditions of the grid voltage but presents unsatisfactory performance under unbalanced conditions. For this reason, improvements in the control system in order to be able to control the current even during unbalanced conditions of the grid voltage are needed.

3.3 Sequence separation method (SSM)

To be able to control the current also during unbalanced conditions of the grid voltage, an algorithm for detection of positive- and negative-sequence components is needed. This algorithm is here called sequence separation method (SSM). When applied to a control system, the SSM has to fulfill specific requirements of speed and robustness in order to ensure a satisfactory performance of the system. Moreover, the SSM has to be insensitive to harmonics in the measured signal.

According with Fortescue's theorem [20], a set of three unbalanced phasors $\overline{V}_\mathrm{a}$, $\overline{V}_\mathrm{b}$ and $\overline{V}_\mathrm{c}$ can always be resolved into three balanced systems of phasors:

- Positive phase-sequence component system, formed by three phasors of equal magnitude V_p and displaced 120° counterclockwise from each other;
- Negative phase-sequence components system, formed by three phasors of equal magnitude V_n and displaced 120° clockwise from each other;
- Zero phase-sequence components system, formed by three phasors of equal magnitude V_0 and equal phase.

The sequence components can be calculated by

$$\overline{V}_p = \frac{1}{3}(\overline{V}_\mathrm{a} + \alpha\overline{V}_\mathrm{b} + \alpha^2\overline{V}_\mathrm{c}) \tag{3.49}$$

$$\overline{V}_n = \frac{1}{3}(\overline{V}_\mathrm{a} + \alpha^2\overline{V}_\mathrm{b} + \alpha\overline{V}_\mathrm{c}) \tag{3.50}$$

$$\overline{V}_0 = \frac{1}{3}(\overline{V}_\mathrm{a} + \overline{V}_\mathrm{b} + \overline{V}_\mathrm{c}) \tag{3.51}$$

$$\tag{3.52}$$

where $\alpha = \mathrm{e}^{\mathrm{j}2\pi/3}$ gives a phase shift of 120°.

The drawback of this traditional method, based on phasors, is that it results slow, due to the calculation time required for the calculation of the RMS value. For this reason, when using SSM for fast control system, techniques based on vector control must be used. In the following, different techniques for the detection of the positive- and negative-sequence components will be treated. It is important to stress that, since a two-level, three legs VSC is used, the system cannot inject zero-sequence component into the mains, thus it can be discarded in the control system.

3.3.1 Delayed signal cancellation technique (DSC)

In the general case of unbalanced grid voltages, the grid voltage vector $\underline{e}^{(\alpha\beta)}(t)$ in the $\alpha\beta$-coordinate system can be written as

$$\begin{aligned}\underline{e}^{(\alpha\beta)}(t) &= \underline{e}_\mathrm{p}^{(\alpha\beta)}(t) + \underline{e}_\mathrm{n}^{(\alpha\beta)}(t) = \\ &= E_\mathrm{p}^{\mathrm{j}(\omega t+\varphi_\mathrm{p})}(t) + E_\mathrm{n}^{-\mathrm{j}(\omega t+\varphi_\mathrm{n})}(t)\end{aligned} \tag{3.53}$$

where $\underline{e}_{\mathrm{p}}^{(\alpha\beta)}(t)$ and $\underline{e}_{\mathrm{n}}^{(\alpha\beta)}(t)$ are the voltage vectors of the positive and negative phase-sequence of the grid voltage. E_{p} and E_{n} are the amplitudes of positive and negative phase-sequence voltage, while φ_{p} and φ_{n} are their phase displacements. The delayed signal cancellation (DSC) method for sequence detection is defined by [45] [28]

$$\widehat{\underline{e}}_{\mathrm{p}}^{(\alpha\beta)}(t) = \frac{1}{2}\left(\underline{e}^{(\alpha\beta)}(t) + \mathrm{j}\underline{e}^{(\alpha\beta)}(t - \frac{T}{4}) \right) \tag{3.54}$$

$$\widehat{\underline{e}}_{\mathrm{n}}^{(\alpha\beta)}(t) = \frac{1}{2}\left(\underline{e}^{(\alpha\beta)}(t) - \mathrm{j}\underline{e}^{(\alpha\beta)}(t - \frac{T}{4}) \right) \tag{3.55}$$

where $\widehat{\underline{e}}_{\mathrm{p}}^{(\alpha\beta)}(t)$ and $\widehat{\underline{e}}_{\mathrm{n}}^{(\alpha\beta)}(t)$ are the estimated positive- and negative-sequence components of the grid voltage, and T is the period of the grid voltage.

The principle of the DSC technique can be understood by using the vector diagram shown in Fig.3.47. In the fixed $\alpha\beta$-coordinate system, the positive phase-sequence vector rotates with the grid frequency counterclockwise, while the negative rotates with the same frequency clockwise. Delaying the grid voltage vector $\underline{e}^{(\alpha\beta)}(t)$ by a quarter of period yields

$$\underline{e}_{\mathrm{p}}^{(\alpha\beta)}(t) = \mathrm{j}\underline{e}_{\mathrm{p}}^{(\alpha\beta)}\left(t - \frac{T}{4} \right) \tag{3.56}$$

$$\underline{e}_{\mathrm{n}}^{(\alpha\beta)}(t) = -\mathrm{j}\underline{e}_{\mathrm{n}}^{(\alpha\beta)}\left(t - \frac{T}{4} \right) \tag{3.57}$$

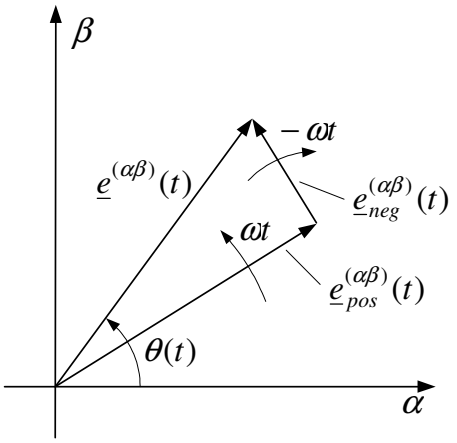


Fig. 3.47 Vector diagram describing principle of DSC technique.

The sequence components can then be estimated by Eqs.(3.54) and (3.55). Applying Eqs.(3.54) and (3.55) corresponds to averaging the input signal over a quarter of period, which gives a robust response. The drawback of this detection method is that it requires a quarter of cycle at the fundamental frequency for estimation.

Figure 3.48 displays the block diagram of DSC applied in discrete time. The term "dqp" denotes a dq-plane that rotates counterclockwise with the angular frequency of the system, while the

term "dqn" denotes a dq-plane that rotates clockwise with the angular frequency. These two planes can also be called positive and negative synchronous reference frames (SRFs).

When using a discrete controller, the measured signal $\underline{e}^{(\alpha\beta)}(k)$ has to be delayed of $f_s/4f_g$ samples. This number should be an integer, which means that for a perfect estimation, good knowledge of the grid frequency and ad-hoc selection of the sampling frequency are necessary. This is a limitation of using this method.

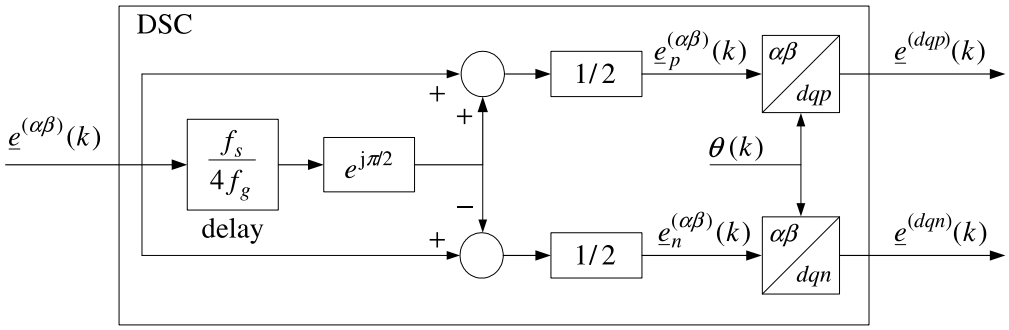


Fig. 3.48 Block diagram of DSC technique implemented in discrete-time domain.

Figures 3.49 and 3.50 show positive- and negative-sequence components of the grid voltage, respectively, during an 80% voltage dip with an unbalance of 10.9% when using DSC. As shown, this SSM requires 5 ms (one quarter of cycle at the grid frequency) for the estimation of the sequence components. During this time, both positive and negative sequence are affected by cross-coupling, due to the error in the estimation.

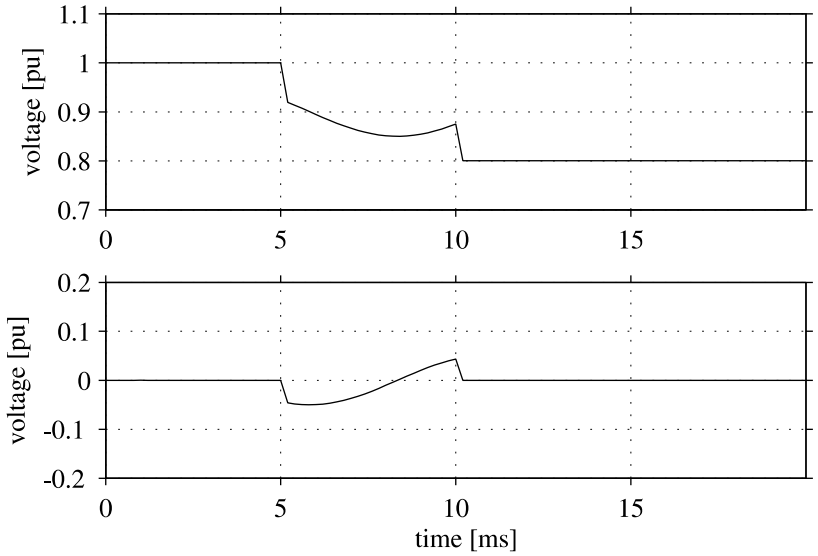


Fig. 3.49 Transient performance of DSC during 80% voltage dip with 10.9% unbalance. Positive-sequence components in positive SRF. Top: d-component; bottom: q-component.

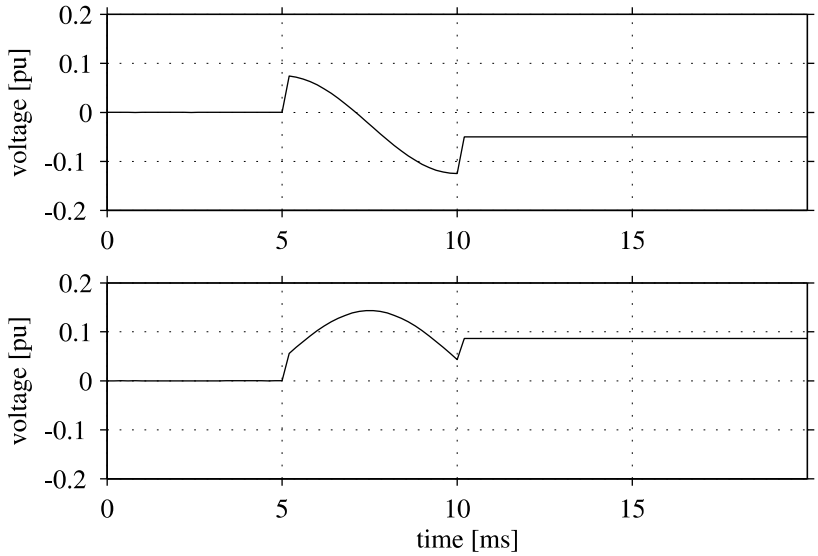


Fig. 3.50 Transient performance of DSC during 80% voltage dip with 10.9% unbalance. Negative-sequence components in negative SRF. Top: d-component; bottom: q-component.

3.3.2 Favor Positive Sequence technique (FPS)

As shown in the previous section, DSC requires a fourth of the line period for detection of positive- and negative-sequence components of the grid voltage. This occurs also when the disturbance involves only a positive-sequence components. However, in normal operation, it would be preferable to estimate the positive sequence as fast as possible. The DSC can then be used to detect the negative-sequence component only, $\underline{e}_{\text{g,n}}^{(\alpha\beta)}(k)$. The positive-sequence component, $\underline{e}_{\text{g,p}}^{(\alpha\beta)}(k)$, can then be estimated by subtracting this signal from $\underline{e}_{\text{g}}^{(\alpha\beta)}(k)$. This modified DSC is here denoted as Favor Positive Sequence (FPS) technique (Fig.3.51). Since the measured signal is always affected by harmonics and noise, the signal $\underline{e}_{\text{g},n}^{(\alpha\beta)}(k)$ has to be filtered. To ensure a good estimation of the positive-sequence component, not affected by the harmonics present in the measured grid voltage, the filter can be a second order Butterworth low-pass filter (LP-filter) with a maximum cut-off frequency of 100 Hz. To avoid the phase-shift introduced by the filter, the signal $\underline{e}_{\text{g,n}}^{(\alpha\beta)}(k)$ is transformed from the $\alpha\beta$- to the dqn-coordinate system and the obtained signal $\underline{e}_{\text{g}}^{(dqn)}(k)$ is then passed through the LP-filter. The filtered signal $\underline{e}_{\text{g,lp}}^{(dqn)}(k)$ is then transformed back to the $\alpha\beta$-coordinate system and subtracted from $\underline{e}_{\text{g}}^{(\alpha\beta)}(k)$ to obtain $\underline{e}_{\text{gf,p}}^{(\alpha\beta)}(k)$, which is finally transformed into $\underline{e}_{\text{gf}}^{(dqp)}(k)$ in the dq-coordinate system. As a consequence, the detection of the positive-sequence component will be faster compared with the DSC, while the detection of the negative-sequence component will result slower. Using FPS, the transient will be fed directly to the current controller and a faster transient performance can be obtained.

Of course, the transient performance of FPS depends on the cut-off frequency of the LP-filter. Figures 3.52 and 3.53 show positive and negative voltage components, respectively, when a voltage dip of 80% with an unbalance of 10.9% occurs in the grid for different cut-off frequencies of the LP-filter. As shown, when using a cut-off frequency lower than 100 Hz ($f_{\text{cut}} = 50$ Hz and $f_{\text{cut}} = 25$ Hz), due to the delay introduced by the LP-filter, the positive-sequence component

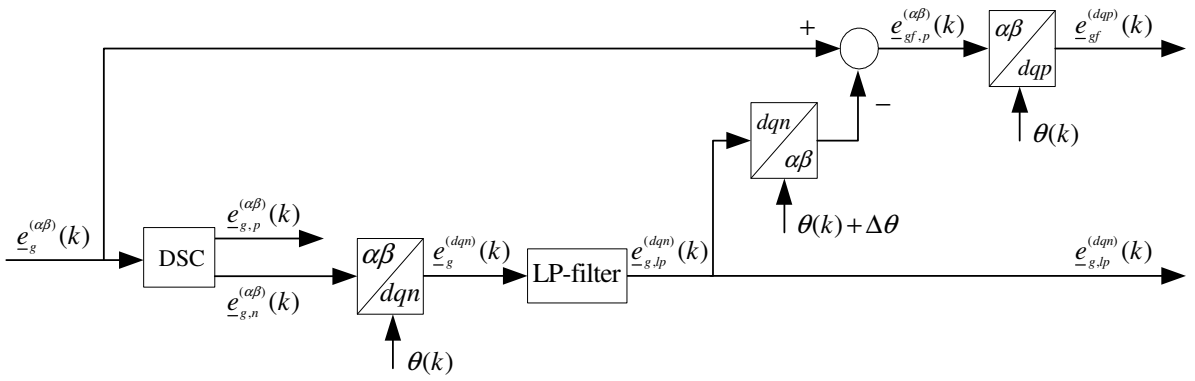


Fig. 3.51 Block scheme of Favor Positive Sequence (FPS) SSM.

of the grid voltage in the dq-coordinate system is affected by oscillations that increase when decreasing the cut-off frequency of the LP-filter.

As shown through simulation results, the main advantage of using FPS is that when a voltage dip occurs at the mains, the response of the positive-sequence component of the grid voltage can be considered instantaneous. However, the drawback when using this SSM is that both positive- and negative-sequence components will be affected by oscillations before reaching the new steady state value, due to the presence of the LP-filter.

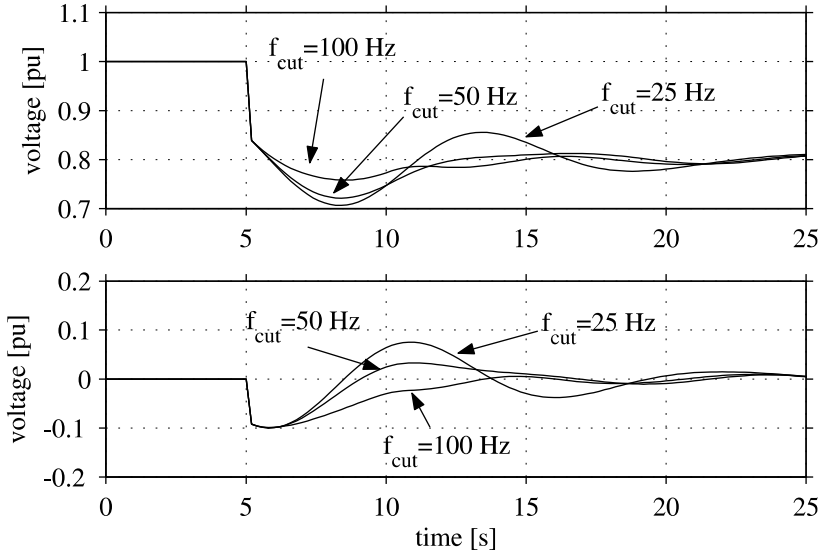


Fig. 3.52 Transient performance of FPS for different cut-off frequencies of Butterworth filter during an 80% voltage dip with unbalance of 10.9%. Positive-sequence components in positive SRF. Top: d-component; bottom: q-component.

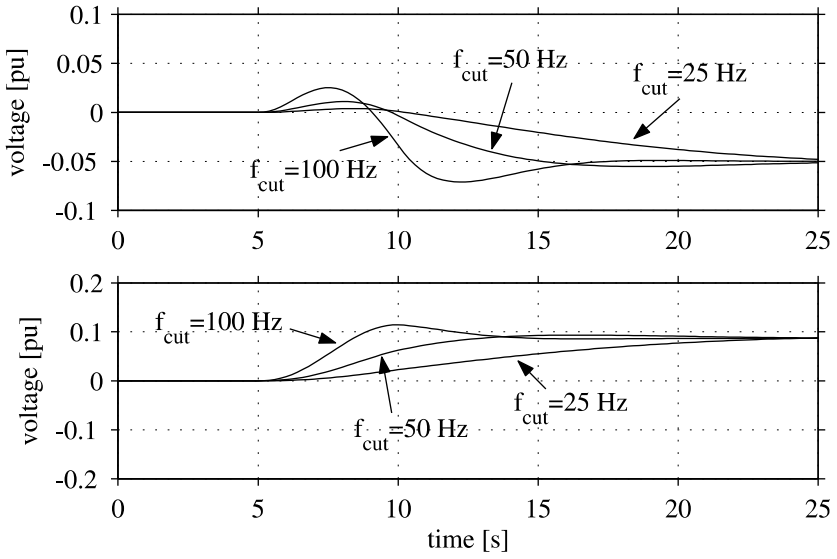


Fig. 3.53 Transient performance of FPS for different cut-off frequencies of Butterworth filter during an 80% voltage dip with unbalance of 10.9%. Negative-sequence components in negative SRF. Top: d-component; bottom: q-component.

3.3.3 Recursive Least Square technique (RLS)

Equation (3.53), giving the grid voltage vector in the fixed $\alpha\beta$-frame can be written in matrix form as

$$\begin{bmatrix} e_\alpha(t) \\ e_\beta(t) \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & \cos(\omega t) & \sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} E_{d\mathrm{p}}(t) \\ E_{q\mathrm{p}}(t) \\ E_{d\mathrm{n}}(t) \\ -E_{q\mathrm{n}}(t) \end{bmatrix} \tag{3.58}$$

where $E_{d\mathrm{p}}$ and $E_{q\mathrm{p}}$ are the real and the imaginary part of the vector $E_{\mathrm{p}}^{\mathrm{j}\varphi_p}$, respectively, and analogously for $E_{d\mathrm{n}}$ and $E_{q\mathrm{n}}$. Equation (3.58) can be expressed in discrete-time domain, with sampling time T_{s}, as follows

$$Y(k) = \mathbf{R}(k)\Theta(k) \tag{3.59}$$

with

$$Y(k) = \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} \tag{3.60}$$

$$\mathbf{R}(k) = \begin{bmatrix} \cos(\omega k T_{\mathrm{s}}) & -\sin(\omega k T_{\mathrm{s}}) & \cos(\omega k T_{\mathrm{s}}) & \sin(\omega k T_{\mathrm{s}}) \\ \sin(\omega k T_{\mathrm{s}}) & \cos(\omega k T_{\mathrm{s}}) & -\sin(\omega k T_{\mathrm{s}}) & \cos(\omega k T_{\mathrm{s}}) \end{bmatrix} \tag{3.61}$$

$$\Theta(k) = \begin{bmatrix} E_{d\mathrm{p}}(k) \\ E_{q\mathrm{p}}(k) \\ E_{d\mathrm{n}}(k) \\ -E_{q\mathrm{n}}(k) \end{bmatrix} \tag{3.62}$$

To estimate the sequence components of the voltage vector $\underline{e}^{(\alpha\beta)}$, four variables should be determined, but the transformation matrix is only 2×4. Assuming that $E_{d\mathrm{p}}$, $E_{q\mathrm{p}}$, $E_{d\mathrm{n}}$ and $E_{q\mathrm{n}}$

change slowly and can be considered constant over two samples, the following expression can be obtained

$$\begin{bmatrix} Y(k-1) \\ Y(k) \end{bmatrix} = \begin{bmatrix} \mathbf{R}(k-1) \\ \mathbf{R}(k) \end{bmatrix} \Theta(k) \tag{3.63}$$

thus, the state vector $\Theta(k)$ is equal to

$$\Theta(k) = \begin{bmatrix} \mathbf{R}(k-1) \\ \mathbf{R}(k) \end{bmatrix}^{-1} \begin{bmatrix} Y(k-1) \\ Y(k) \end{bmatrix} \tag{3.64}$$

Therefore, by using Eq.(3.63) it is possible to estimate the sequence components within two samples. However, this method results very sensitive to noise in the measurements. It is possible to increase the robustness of the algorithm by considering more samples. Thus, the SSM will be less sensitive to noise, but, of course, this will lower the bandwidth of the algorithm. Assuming that γ samples are considered, the expression becomes

$$\begin{bmatrix} Y(k-\gamma) \\ \vdots \\ Y(k) \end{bmatrix} = \begin{bmatrix} \mathbf{R}(k-\gamma) \\ \vdots \\ \mathbf{R}(k) \end{bmatrix} \Theta(k) \tag{3.65}$$

and the state vector is equal to

$$\Theta(k) = \left[\begin{bmatrix} \mathbf{R}(k-\gamma) \\ \vdots \\ \mathbf{R}(k) \end{bmatrix}^{\mathrm{T}} \begin{bmatrix} \mathbf{R}(k-\gamma) \\ \vdots \\ \mathbf{R}(k) \end{bmatrix} \right]^{-1} \begin{bmatrix} \mathbf{R}(k-\gamma) \\ \vdots \\ \mathbf{R}(k) \end{bmatrix}^{\mathrm{T}} \begin{bmatrix} Y(k-\gamma) \\ \vdots \\ Y(k) \end{bmatrix} \tag{3.66}$$

The problem with this method is that the transformation matrix increases with the increased number of stored samples, thus large amount of memory in the control computer is required. To overcome this problem, recursive least-square estimation (RLS) can be adopted. The objective with the RLS algorithm is to estimate the state vector $\Theta(k)$ from the measurement $Y(k)$ and the observation matrix $\mathbf{R}(k)$ [51]. To achieve this goal, the estimated state vector can be written as

$$\widehat{\Theta}(k) = \widehat{\Theta}(k-1) + \mathbf{K}(k)(Y(k) - \mathbf{R}(k)\widehat{\Theta}(k-1)) \tag{3.67}$$

where $\mathbf{K}(k)$ is a gain matrix given by

$$\mathbf{K}(k) = \mathbf{P}(k-1)\mathbf{R}^{\mathrm{T}}(k)(\lambda\mathbf{I} + \mathbf{R}(k)\mathbf{P}(t-1)\mathbf{R}^{\mathrm{T}}(k))^{-1} \tag{3.68}$$

with $\mathbf{P}(k)$ the error covariance matrix, given by

$$\mathbf{P}(k) = (\mathbf{I} - \mathbf{K}(k)\mathbf{R}(k))\mathbf{P}(k-1)\frac{1}{\lambda} \tag{3.69}$$

where λ is the forgetting factor, which can vary between zero and one. The transient performance of the RLS method depends on this factor λ: increasing λ enhances the averaging effect in the estimation and increases the noise immunity of the estimator. Typically, a value of $\lambda = 0.99$ is used [51].

An advantage of the RLS over the DSC is that it is independent of the relation between grid frequency and sampling frequency, therefore it is always possible to perform an accurate estimation of the sequence components.

Comparison between different SSM

Figures 3.54 and 3.55 show the positive and the negative sequence components, respectively, of the grid voltage using the explained detection methods when a dip of 80% with an unbalance of 10% occurs in the grid. As shown, using FPS the sequence detection is instantaneous but the positive sequence is affected by an oscillation and takes 10 ms to reach the steady state. Using RLS the controller takes 3 ms for the detection, while DSC requires 5 ms.

The FPS technique provides a faster response in the positive sequence estimation compared with the other two methods. However, the estimation of the negative-sequence components is slower and both positive- and negative-sequence components are affected by oscillations due to the presence of the low-pass filter. Moreover, the drawback with this SSM is that the harmonic content of the measured signal is directly fed to the estimated positive-sequence component. The RLS shows faster response compared with DSC. However, it has been tested via simulation that when this method is applied in a feedback loop, the control system can easily get into instability. For these reasons, even if DSC is the slowest within the methods analyzed, it is the method of choice for detection of sequence components in this work, because of its robustness.

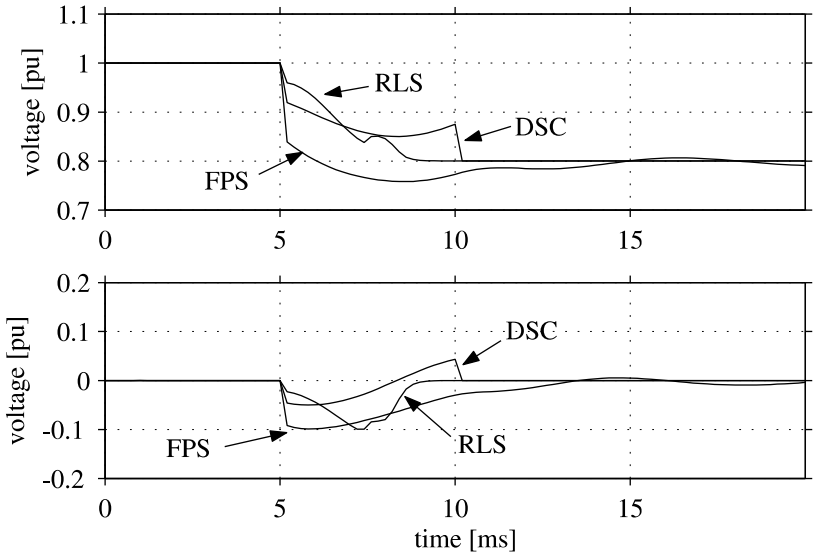


Fig. 3.54 Voltage response to simulated unbalanced voltage dip when using DSC, FPS and RLS. Top: d-component, positive sequence; bottom: q-component, positive sequence.

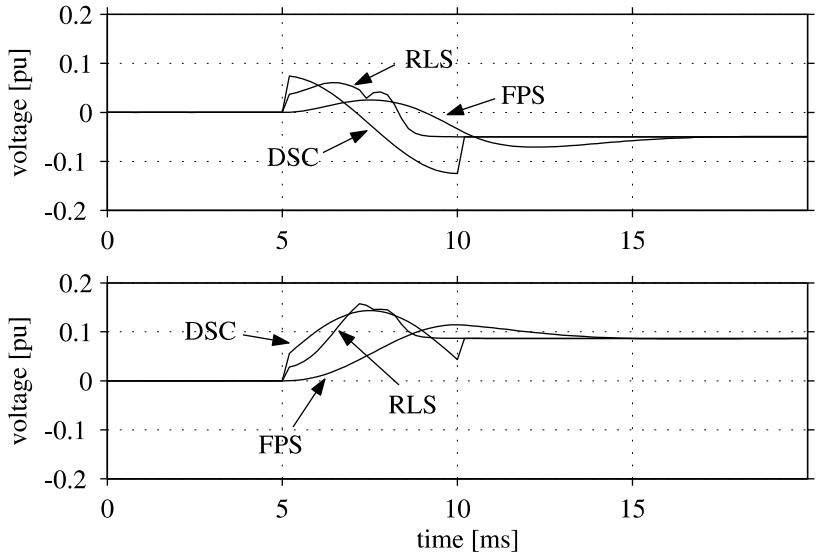


Fig. 3.55 Voltage response to simulated unbalanced voltage dip when using DSC, FPS and RLS. Top: d-component, negative sequence; bottom: q-component, negative sequence.

3.4 Vector Current-controller Type 2 (VCC2)

The problems encountered using VCC1 under unbalanced conditions of the grid voltage are due to the presence of a negative sequence voltage. An obvious way of dealing with the problem is to separate the positive and negative sequence voltage components of the grid voltage and only send the positive sequence voltage to the vector current-control. The negative sequence voltage is instead directly added to the reference voltage out from the current controller [44]. The block scheme of the improved vector current-controller, here called vector current-controller type 2 (VCC2), is displayed in Fig.3.56.

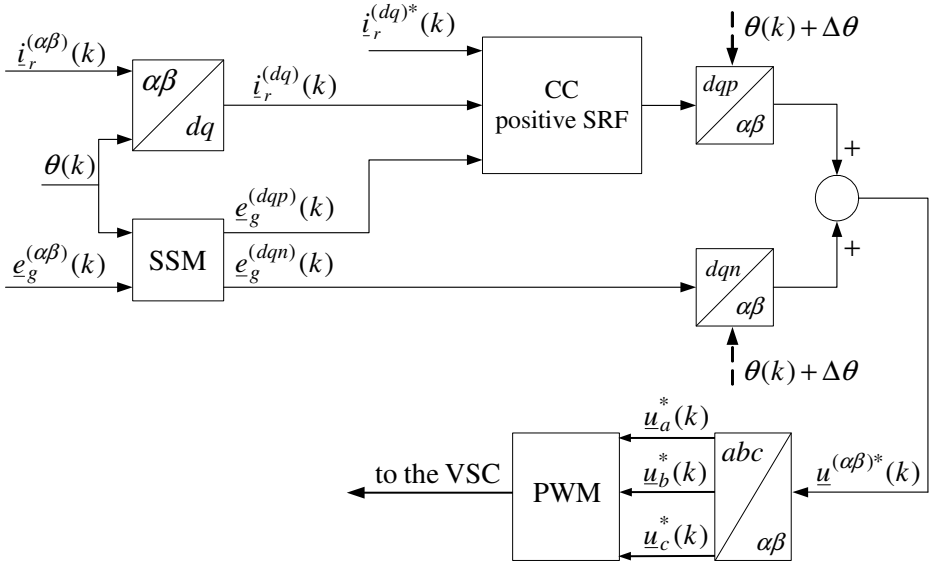


Fig. 3.56 Block scheme of vector current-controller type 2 (VCC2).

3.4.1 Simulation results using VCC2

The VCC2 has been simulated both under balanced and unbalanced conditions of the grid voltage. The parameters used for VCC2 are reported in Table 3.2. Since the objective of using VCC2 is to improve the performance of the system under unbalanced conditions, only simulations results for unbalanced grid voltages and unbalanced voltage dips will be presented.

Simulations with unbalanced grid voltage

In order to compare the performance of VCC1 and VCC2, the latter has been tested under the same unbalanced conditions as in Section 3.2.6. Three-phase unbalanced grid voltages affected by unbalance of 10.9% are displayed in Fig.3.33. In the control system, positive and negative sequence voltage components are separated by the SSM and transformed into the positive and negative SRFs, respectively, where they appear as DC-quantities, as shown in Fig.3.57.

The control system has been tested applying steps in the active and reactive current as in Section 3.2.6. As displayed in Fig.3.58 and Fig.3.59, the actual current tracks the reference in two samples and is free of oscillations, despite the unbalance of the grid voltage.

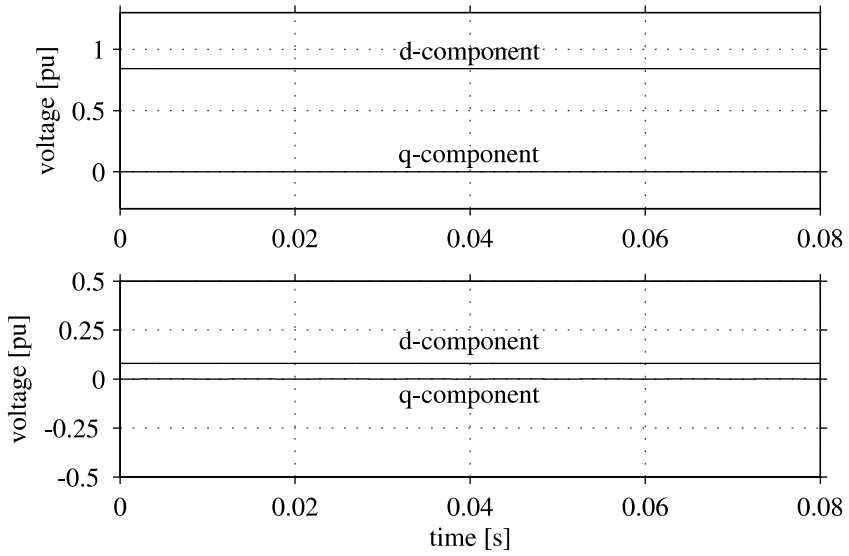


Fig. 3.57 Simulated unbalanced grid voltages in dq-coordinate system with DSC. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

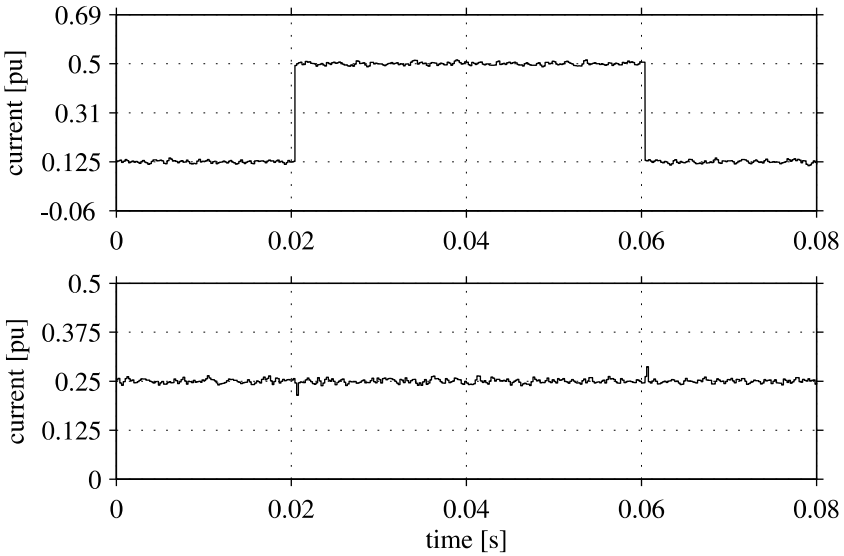


Fig. 3.58 Simulated active and reactive current response to reference active current step with VCC2 and unbalanced grid voltage. Top: d-component; bottom: q-component.

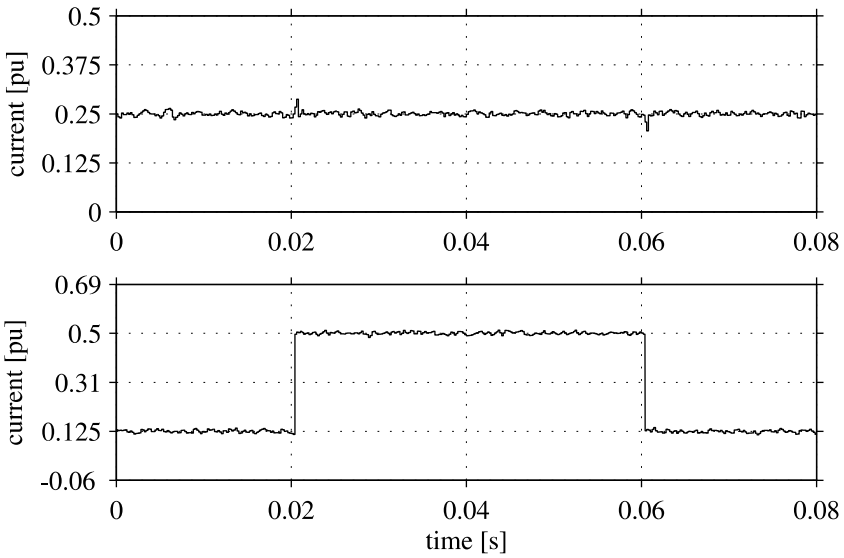


Fig. 3.59 Simulated active and reactive current response to reference reactive current step with VCC2 and unbalanced grid voltage. Top: d-component; bottom: q-component.

Voltage dip response

To test the speed of response of the VCC2 during transients, the system has also been tested under unsymmetrical voltage dip. Three-phase grid voltages during an 80% voltage dip with unbalance of 10.9% are shown in Fig.3.44. The sequence components of the grid voltage, detected by the SSM, will appear as DC-quantities in the corresponding SRFs, as displayed in Fig.3.60. During the dip, the d-component of the positive sequence voltage goes from 1 pu to 0.8 pu, while the d-component of the negative sequence voltage steps from 0 pu to 0.1 pu. The small transient at the beginning and at the end of the dip, which lasts for 5 ms (one fourth of period at 50 Hz) is due to the adopted DSC.

The control system operates properly and the actual current maintains the pre-fault value during the dip, as shown in Fig.3.61. It can be noticed that, as in Section 3.2.6, the actual current is affected by a 0.6 pu overshoot but, due to the delay introduced by the sequence detection in the grid voltage, it takes 5 ms to reach the steady state value.

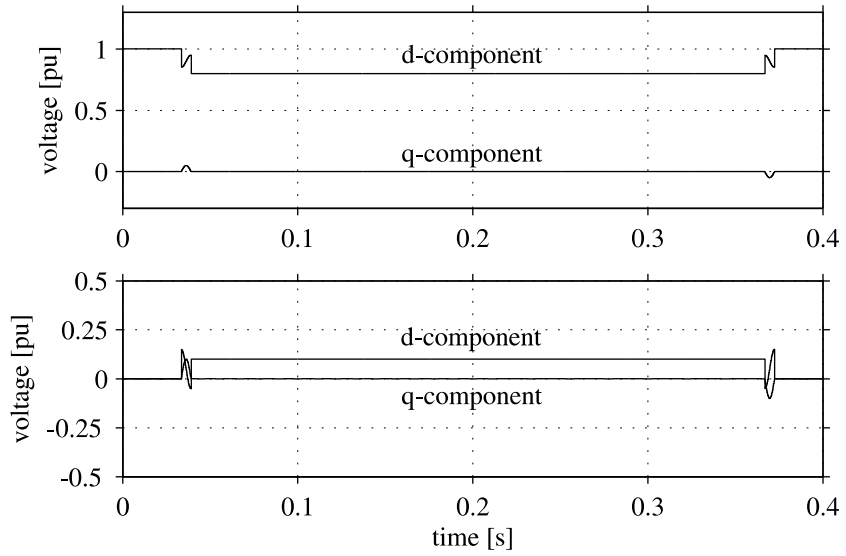


Fig. 3.60 Simulated grid voltages in dq-coordinates during 80% voltage dip with unbalance of 10.9%. VCC2 and unbalanced voltage dip are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

3.4.2 Summary

In this section, the modified vector current-controller, VCC2, obtained by only feeding the positive sequence of the grid voltage to the control system, has been presented. Different sequence separation methods (SSMs) to separate the positive and the negative sequence voltage components have been explained and compared. Simulation results show that the VCC2 operates properly also under unbalanced grid voltages.

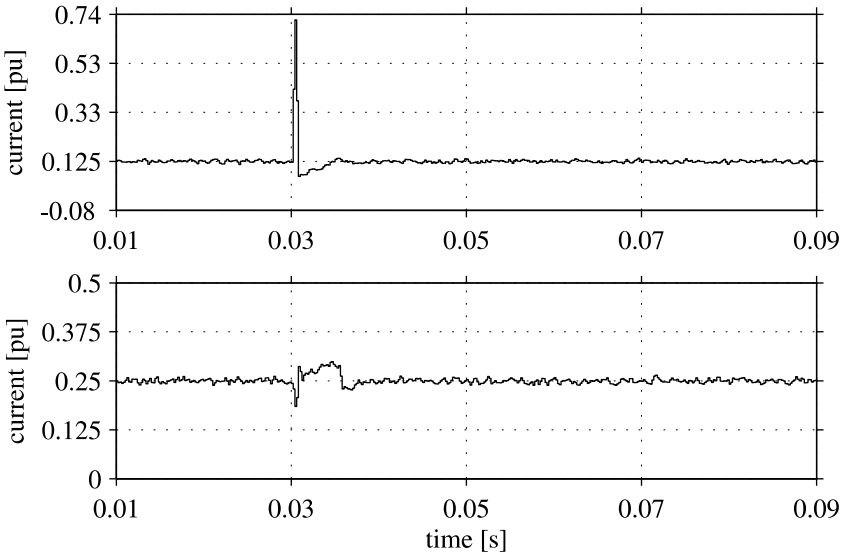


Fig. 3.61 Simulated active and reactive current response in dq-coordinates during 80% voltage dip with unbalance of 10.9%. VCC2 and unbalanced voltage dip are used. Top: d-component; bottom: q-component.

3.5 Dual Vector Current-controller (DVCC)

In some cases, the vector current-controller must control both the positive- and the negative-sequence components of the filter current. This is the case in applications where the current controller is used to regulate the DC-link voltage to a constant value through a DC-voltage controller in unbalanced conditions [32], or where positive and negative reference currents are provided separately by an outer loop, for instance, in the cascade controller proposed in [6]. To achieve this goal, a dual vector current-controller (DVCC) can be used.

The DVCC is constituted by two separate controllers implemented in the positive and in the negative SRF, respectively, as shown in Fig.3.62 [50]. Both grid voltage and current are separated into positive- and negative-sequence components and the controller tracks positive- and negative-sequence reference currents. The positive-sequence current controller in the positive SRF is given by

$$\begin{aligned}\underline{u}^{(dqp)*}(k) = \underline{e}_{\mathrm{g}}^{(dqp)}(k) + R_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dqp)}(k) + \mathrm{j}\frac{\omega L_{\mathrm{r}}}{2}(\underline{i}_{\mathrm{r}}^{(dqp)*}(k) + \underline{i}_{\mathrm{r}}^{(dqp)}(k)) + \\ + k_p\underline{\varepsilon}_{\mathrm{i}}^{(dqp)}(k) + \sum_{n-1}^{k} k_i\underline{\varepsilon}_{\mathrm{i}}^{(dqp)}(n-1)\end{aligned} \tag{3.70}$$

where the current error in the positive SRF is

$$\underline{\varepsilon}_{\mathrm{i}}^{(dqp)}(k) = \underline{i}_{\mathrm{r}}^{(dqp)*}(k) - \underline{i}_{\mathrm{r}}^{(dqp)}(k) - \widehat{\underline{i}}_{\mathrm{r}}^{(dqp)}(k) + \widehat{\underline{i}}_{\mathrm{r}}^{(dqp)}(k-1) \tag{3.71}$$

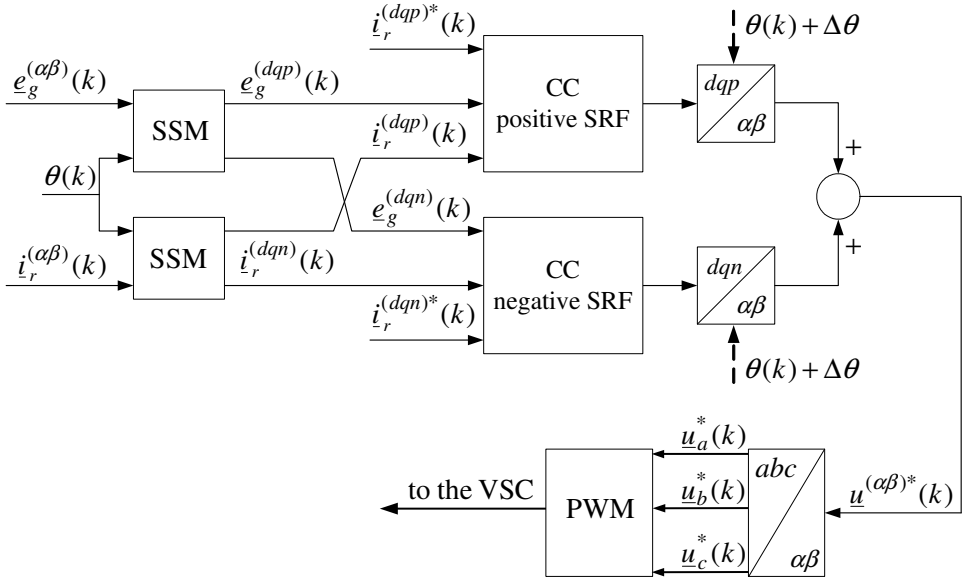


Fig. 3.62 Block scheme of dual vector current-controller (DVCC).

The corresponding state observer is given by

$$\begin{aligned}\underline{\hat{i}}_{\mathrm{r}}^{(dqp)}(k+1) = (1-\frac{R_{\mathrm{r}}}{L_{\mathrm{r}}}T_{\mathrm{s}}-\mathrm{j}\omega T_{\mathrm{s}})\underline{\hat{i}}_{\mathrm{r}}^{(dqp)}(k)+\frac{T_{\mathrm{s}}}{L_{\mathrm{r}}}(\underline{u}^{(dqp)*}(k)-\underline{e}_{\mathrm{g}}^{(dqp)}(k))+\\ +k_{\mathrm{psp}}(\underline{i}_{\mathrm{r}}^{(dqp)}(k)-\underline{\hat{i}}_{\mathrm{r}}^{(dqp)}(k))\end{aligned} \tag{3.72}$$

Similarly, the negative-sequence current controller in the negative SRF can be derived as

$$\begin{aligned}\underline{u}^{(dqn)*}(k) = \underline{e}_{\mathrm{g}}^{(dqn)}(k)+R_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dqn)}(k)-\mathrm{j}\frac{\omega L_{\mathrm{r}}}{2}(\underline{i}_{\mathrm{r}}^{(dqn)*}(k)+\underline{i}_{\mathrm{r}}^{(dqn)}(k))+\\ +k_p\underline{\varepsilon}_{\mathrm{i}}^{(dqn)}(k)+\sum_{n-1}^{k}k_i\underline{\varepsilon}_{\mathrm{i}}^{(dqn)}(n-1)\end{aligned} \tag{3.73}$$

where the current error in the negative SRF is

$$\underline{\varepsilon}_{\mathrm{i}}^{(dqn)}(k) = \underline{i}_{\mathrm{r}}^{(dqn)*}(k)-\underline{i}_{\mathrm{r}}^{(dqn)}(k)-\underline{\hat{i}}_{\mathrm{r}}^{(dqn)}(k)+\underline{\hat{i}}_{\mathrm{r}}^{(dqn)}(k-1) \tag{3.74}$$

and the corresponding state observer is given by

$$\begin{aligned}\underline{\hat{i}}_{\mathrm{r}}^{(dqn)}(k+1) = (1-\frac{R_{\mathrm{r}}}{L_{\mathrm{r}}}T_{\mathrm{s}}+\mathrm{j}\omega T_{\mathrm{s}})\underline{\hat{i}}_{\mathrm{r}}^{(dqn)}(k)+\frac{T_{\mathrm{s}}}{L_{\mathrm{r}}}(\underline{u}^{(dqn)*}(k)-\underline{e}_{\mathrm{g}}^{(dqn)}(k))+\\ +k_{\mathrm{psp}}(\underline{i}_{\mathrm{r}}^{(dqn)}(k)-\underline{\hat{i}}_{\mathrm{r}}^{(dqn)}(k))\end{aligned} \tag{3.75}$$

The DVCC outputs are positive- and negative-sequence components of the reference voltage for the PWM modulator in the two SRFs. By transforming them into the fixed $\alpha\beta$-coordinate system and then adding them up, the reference voltage vector $\underline{u}^{(\alpha\beta)*}$ is obtained.

3.5.1 Saturation strategies for DVCC

When using DVCC, one crucial point is the limitation of the reference voltage to the boundary of the hexagon, if saturation occurs. This limitation can be implemented on the reference voltage vector $\underline{u}^{(\alpha\beta)*}$, as explained in Section 3.2.4. However, this means that any information about the sequence components is lost. Thus, it is not possible to recalculate positive- and negative-sequence components of the voltage vector. As a consequence, during saturation of the VSC it is not possible to calculate the back-calculated error for each sequence component and to estimate the currents using the Smith predictor. In the following, different methods for the limitation of the reference voltage vector when using DVCC are proposed.

Equal priority scaling

In this section, two limitation methods for the reference voltage vector when using DVCC based on the equal scaling of the positive- and negative-sequence components will be presented.

If the reference voltage vector $\underline{u}^{(xy)*}(k)$ in the auxiliary xy-coordinate systems exceeds the boundary of the hexagon, one way of dealing with the problem is to limit its length to the boundary of the hexagon and then scaling its positive- and negative-sequence components, denoted by $\underline{u}_{\mathrm{p}}^{(xy)*}(k)$ and $\underline{u}_{\mathrm{n}}^{(xy)*}(k)$, respectively, in proportion. This limitation method is here called dual space vector limitation method (DSVL). The principle of DSVL is depicted in Fig.3.63.

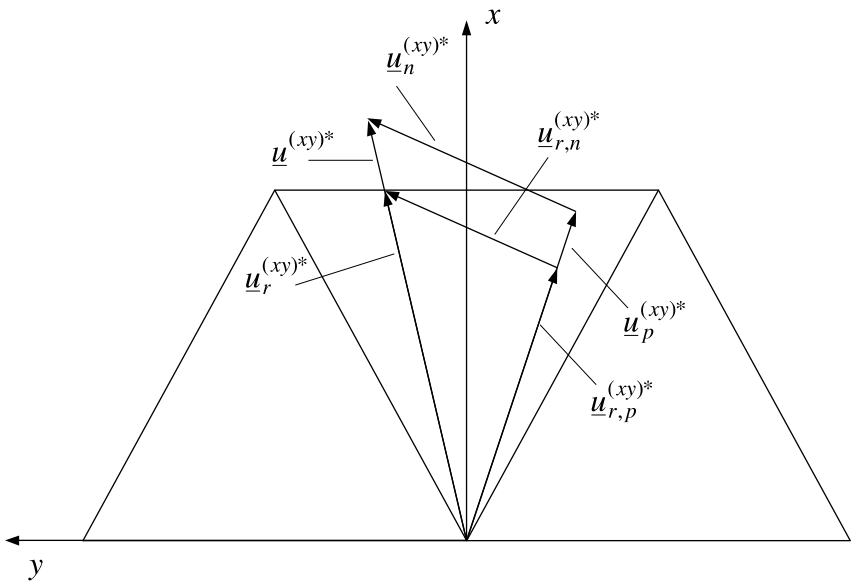


Fig. 3.63 Principle of DSVL method to avoid VSC saturation when DVCC is used.

Using this method, the reduced reference voltage vector $\underline{u}_{\mathrm{r}}^{(xy)*}$ has the same direction as the original reference voltage vector and its components $u_{x\mathrm{r}}^*$ and $u_{y\mathrm{r}}^*$ on the x- and y-axis, respectively, are equal to

$$u_{x\mathrm{r}}^* = \frac{u_{\mathrm{dc}}}{\sqrt{2}} \tag{3.76}$$

$$u_{y\mathrm{r}}^{*} = u_{y}^{*}\frac{u_{x\mathrm{r}}^{*}}{u_{x}^{*}} = u_{y}^{*}\gamma \tag{3.77}$$

where, similarly, u_x^* and u_y^* are the components of the non limited reference voltage vector in x- and y-axis, respectively, and γ is always smaller than 1.

By using simple geometry, the positive and negative sequence components of the limited voltage vector are thus equal to

$$\underline{u}_{\mathrm{r},p}^{(xy)*} = \gamma \underline{u}_{p}^{(xy)*} \tag{3.78}$$

$$\underline{u}_{\mathrm{r},n}^{(xy)*} = \gamma \underline{u}_{n}^{(xy)*} \tag{3.79}$$

To avoid integrator windup, back-calculation can be adopted, as in Section 3.2.4. The back-calculated current error for positive- and for negative-sequence components is given by

$$\underline{i}_{\mathrm{er}}^{(dqp)} = \frac{1}{k_{\mathrm{p}}}(\underline{u}_{\mathrm{r}}^{(dqp)*} - \underline{u}_{\mathrm{ff}}^{(dqp)} - \Delta\underline{u}_{\mathrm{i}}^{(dqp)}) \tag{3.80}$$

$$\underline{i}_{\mathrm{er}}^{(dqn)} = \frac{1}{k_{\mathrm{p}}}(\underline{u}_{\mathrm{r}}^{(dqn)*} - \underline{u}_{\mathrm{ff}}^{(dqn)} - \Delta\underline{u}_{\mathrm{i}}^{(dqn)}) \tag{3.81}$$

where

$$\underline{u}_{\mathrm{ff}}^{(dqp)}(k) = \underline{e}_{\mathrm{g}}^{(dqp)}(k) + R_{\mathrm{r}}\underline{i}_{\mathrm{r}}^{(dqp)}(k) + \mathrm{j}\frac{\omega L_{\mathrm{r}}}{2}(\underline{i}_{\mathrm{r}}^{(dqp)*}(k) + \underline{i}_{\mathrm{r}}^{(dqp)}(k)) \tag{3.82}$$

$$\Delta\underline{u}_{\mathrm{i}}^{(dqp)}(k+1) = \Delta\underline{u}_{\mathrm{i}}^{(dqp)}(k) + k_i\varepsilon_{\mathrm{i}}^{(dqp)}(k) \tag{3.83}$$

and analogously for the negative-sequence.

To test the effectiveness of DSVL, the DVCC has been tested by applying steps in the active reference current. The application of DSC introduces a delay of a quarter of period in the current measurement. To overcome system instability due to this delay, the bandwidth of both positive and negative current controllers has been reduced to 70% of deadbeat. Control system parameters are displayed in Table 3.3. Parameters of the simulated system are shown in Table 3.1. All simulations have been carried out under the assumption that the grid voltage is balanced and at nominal value. Figure 3.64 shows the simulation results of shunt-connected VSC with

TABLE 3.3. CONTROLLER PARAMETERS FOR DVCC.

Sampling frequency	f_{s} = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Proportional gain	k_{p} = 7.01	Integrator time constant	T_{i} = 0.0564 s
Observer gain	k_{psp} = 0.1		

DVCC and DSVL under balanced grid voltage when applying a step in the positive sequence d-current. The operating point is equal to -0.5 pu d-component and 0.25 pu q-component for both positive and negative sequence current. At $t = 20$ ms, the reference active current makes a step with amplitude 1 pu and the step lasts for 40 ms. Due to the large variation in the demanded

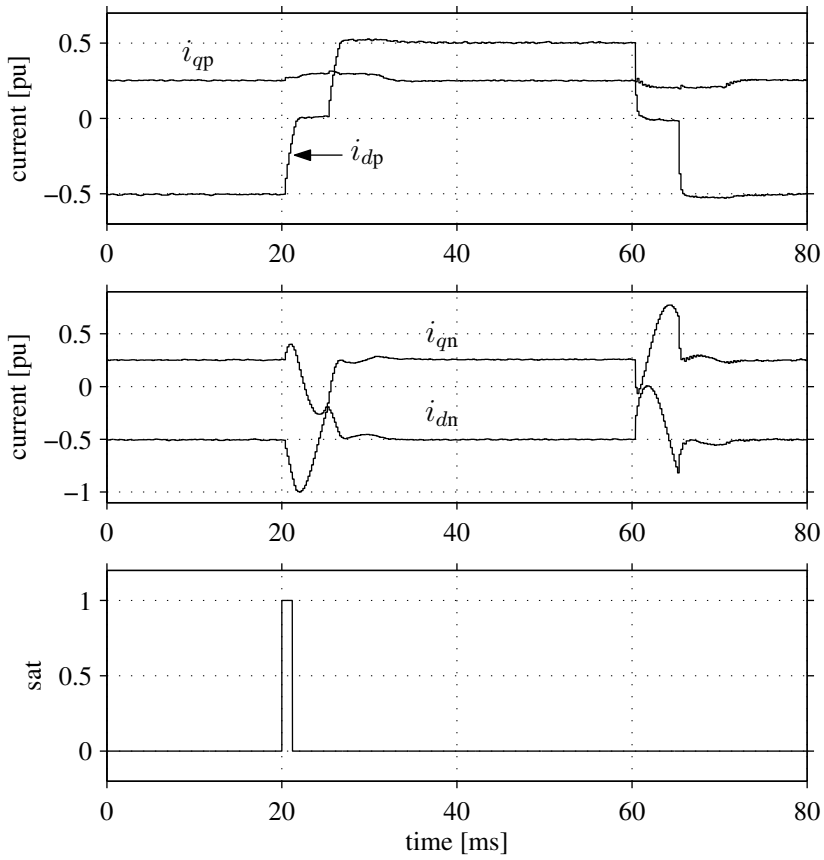


Fig. 3.64 Simulated current response to reference active current step. DVCC and DSVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

current, the VSC saturates. The signal "sat" in the figure denotes VSC saturation. Due to the saturation of the VSC, the positive flank of $i_{d\mathrm{p}}$ during the step is not as steep as the negative flank. However, thanks to the DSVL, even during saturation of the VSC the controller works properly and the actual current manages to track the reference.

An alternative way to limit the reference voltage vector is to consider that, when a step in the reference current is applied, the reference voltage vector can be considered the sum of the steady state reference voltage vector, defining the operating point and denoted as $\underline{u}_{\mathrm{ffi}}^{(xy)*}$, and a transient term, denoted as $\Delta\underline{u}^{(xy)*}$, due to the applied step. The reference voltage vector $\underline{u}_{\mathrm{ffi}}^{(xy)*}$ that defines the current operating point, can be split into its positive- and negative-sequence components

$$\underline{u}_{\mathrm{ffi}}^{(xy)*}(k) = \underline{u}_{\mathrm{ffi,p}}^{(xy)*}(k) + \underline{u}_{\mathrm{ffi,n}}^{(xy)*}(k) \tag{3.84}$$

where

$$\underline{u}_{\mathrm{ffi,p}}^{(xy)*}(k) = \underline{u}_{\mathrm{ff,p}}^{(xy)*}(k) + \sum_{n=1}^{k} k_i \underline{\varepsilon}_{i\mathrm{p}}^{(xy)}(n-1) \tag{3.85}$$

where $\underline{u}_{\mathrm{ff,p}}^{(xy)}$ and $\underline{\varepsilon}_{i\mathrm{p}}^{(xy)*}$ are the feed-forward voltage term and the current error for the positive sequence in the xy-coordinate system. An analogous relation can be written for the negative

sequence.

Similarly, the transient variation of the reference voltage $\Delta\underline{u}^{(xy)*}$ due to step, can be written as

$$\Delta\underline{u}^{(xy)*}(k) = \Delta\underline{u}_{\mathrm{p}}^{(xy)*}(k) + \Delta\underline{u}_{\mathrm{n}}^{(xy)*}(k) \tag{3.86}$$

where

$$\Delta\underline{u}_{\mathrm{p}}^{(xy)*}(k) = k_p\underline{\varepsilon}_{i\mathrm{p}}^{(xy)}(k) \tag{3.87}$$

In the dual dynamic vector limitation strategy (DDVL), displayed in Fig.3.65, only the transient term $\Delta\underline{u}^{(xy)*}$ is limited.

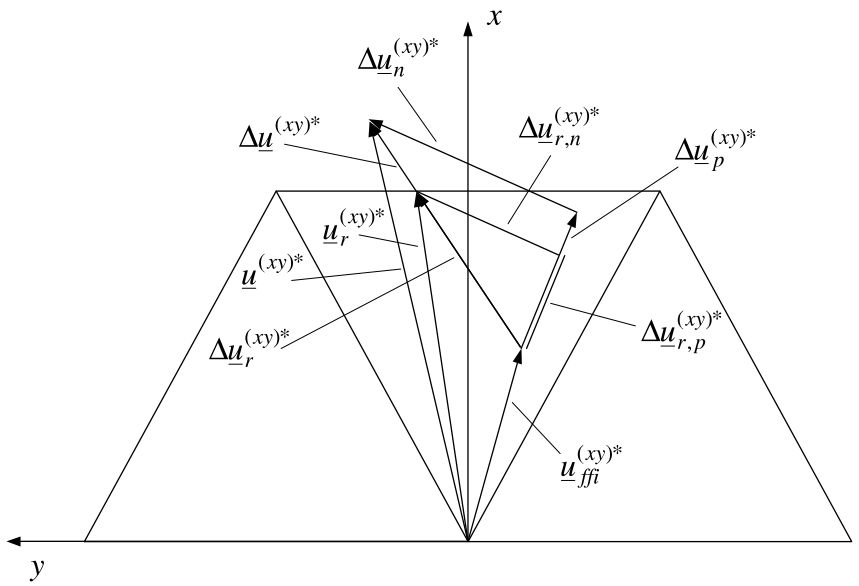


Fig. 3.65 Principle of DDVL method to avoid VSC saturation when DVCC is used.

If saturation occurs, $\Delta\underline{u}^{(xy)*}$ is reduced to the boundary of the hexagon, and the reduced transient voltage vector $\Delta\underline{u}_{\mathrm{r}}^{(xy)*}$ is

$$\Delta\underline{u}_{\mathrm{r}}^{(xy)*} = \gamma\Delta\underline{u}^{(xy)*} \tag{3.88}$$

where γ is a scaling factor. By substituting Eq.(3.86) into Eq.(3.88), the positive- and negative-sequence component of the transient term are equal to

$$\Delta\underline{u}_{\mathrm{r,p}}^{(xy)*} = \gamma\Delta\underline{u}_{\mathrm{p}}^{(xy)*} \tag{3.89}$$

$$\Delta\underline{u}_{\mathrm{r,n}}^{(xy)*} = \gamma\Delta\underline{u}_{\mathrm{n}}^{(xy)*} \tag{3.90}$$

In Fig.3.65, by using simple geometry, the scaling factor γ can be written

$$\gamma = \frac{\Delta u_x^* - u_x^* + u_{\mathrm{dc}}/\sqrt{2}}{\Delta u_x^*} \tag{3.91}$$

where Δu_x^* and u_x^* are the projections of the voltage vectors $\Delta\underline{u}^{(xy)*}$ and $\underline{u}^{(xy)*}$, respectively, on the x-axis.

The back-calculated current error for positive and negative sequences will be equal to

$$\underline{i}_{\text{er}}^{(dqp)} = \frac{\Delta \underline{u}_{\text{r}}^{(dqp)*}}{k_p} \tag{3.92}$$

$$\underline{i}_{\text{er}}^{(dqn)} = \frac{\Delta \underline{u}_{\text{r}}^{(dqn)*}}{k_p} \tag{3.93}$$

Figure 3.66 shows the simulation results of shunt-connected VSC with DVCC and DDVL under balanced grid voltage when applying the same step in the positive sequence d-current as in Fig.3.64. The transient performance of the DVCC during saturation when using DSVL and when using DDVL is identical.

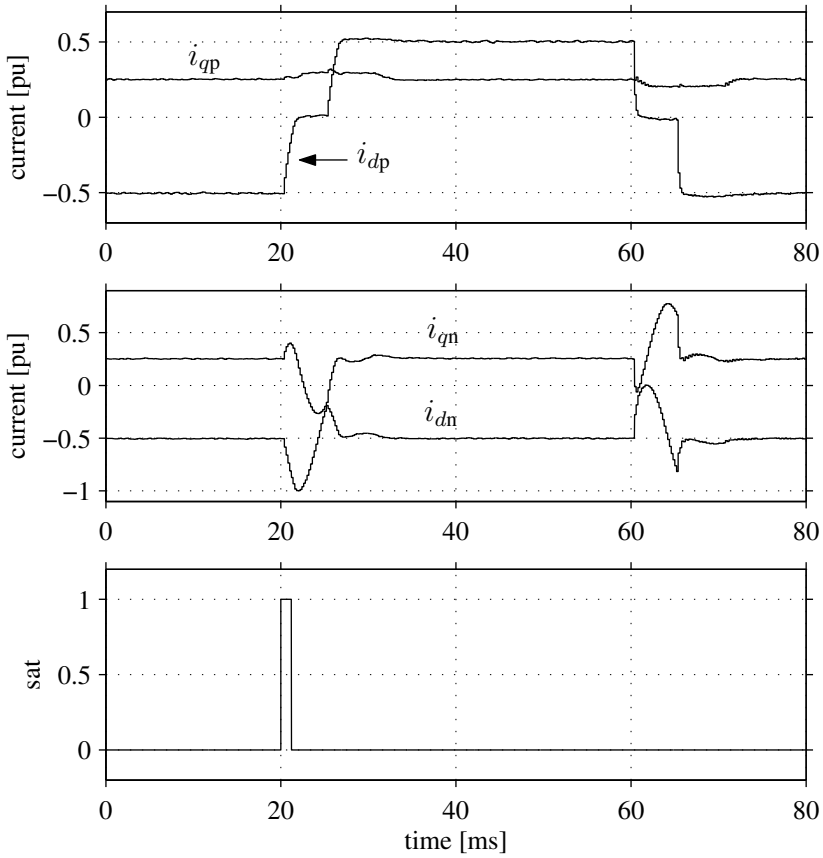


Fig. 3.66 Simulated current response to reference active current step. DVCC and DDVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

Dynamic positive vector limitation strategy (DPVL)

In many applications, it is important to maximize the injection of positive sequence into the grid, also during saturation. For this reason, the DDVL can be modified in order to favor the injection

of positive-sequence component over the injection of negative-sequence component. This limitation method is here called dynamic positive vector limitation strategy (DPVL). Two different scenarios can occur during saturation: the positive sequence voltage vector is located inside the hexagon, as in Fig.3.67(a), or the positive sequence voltage vector exceeds the hexagon boundary, as in Fig.3.67(b).

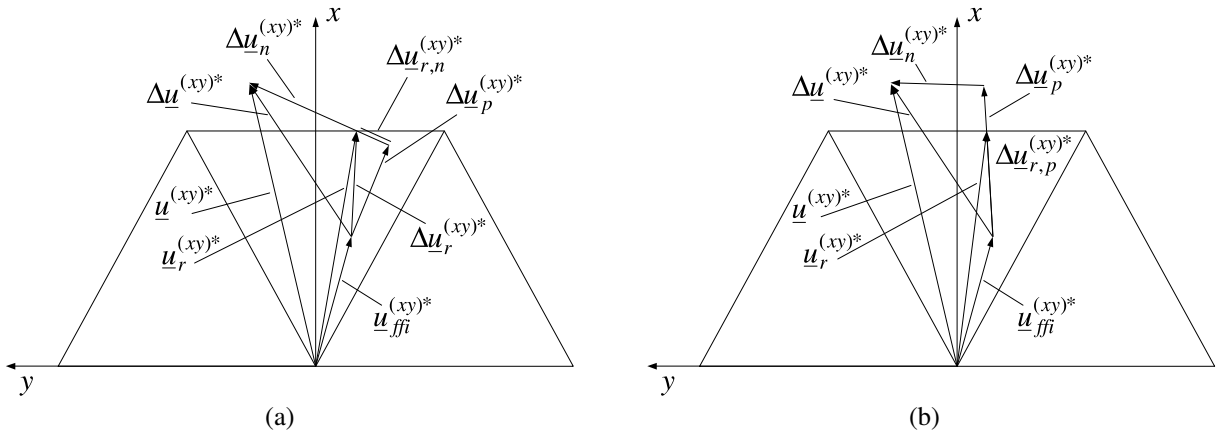


Fig. 3.67 Principle of DPVL method to avoid VSC saturation. Positive sequence reference voltage vector inside hexagon boundary (a); positive sequence voltage vector outside hexagon boundary (b).

When the positive sequence voltage vector is inside the hexagon, the saturation strategy consists in limiting the transient term of the negative sequence voltage vector $\Delta\underline{u}_{\mathrm{n}}^{(xy)*}$ in order to reduce the transient reference voltage $\Delta\underline{u}^{(xy)*}$ to the boundary of the hexagon, while the transient term of the positive sequence vector $\Delta\underline{u}_{\mathrm{p}}^{(xy)*}$ is maintained constant. The components of the reduced vector $\Delta\underline{u}_{\mathrm{r,n}}^{(xy)*}$ in the x- and y-direction can be written as

$$\Delta u_{x\mathrm{r,n}}^{*} = \frac{u_{\mathrm{dc}}}{\sqrt{2}} - u_{x\mathrm{ffi}}^{*} - \Delta u_{x\mathrm{p}}^{*} \tag{3.94}$$

$$\Delta u_{y\mathrm{r,n}}^{*} = \Delta u_{y\mathrm{n}}^{*} \frac{\Delta u_{x\mathrm{r,n}}^{*}}{\Delta u_{x\mathrm{n}}^{*}} \tag{3.95}$$

where $\Delta u_{x\mathrm{p}}^{*}$ is the projection of the transient voltage vector $\Delta\underline{u}_{\mathrm{p}}^{(xy)*}$ on the x-axis and analogously for the other vectors. In this case, only back-calculation of the negative sequence current error should be considered, which can be calculated using Eq.(3.93).

If the positive sequence of the reference voltage vector $\underline{u}_{\mathrm{p}}^{(xy)*}$ exceeds the boundary of the hexagon, as in Fig.3.67(b), its transient term will be scaled in order to reduce the transient reference voltage $\Delta\underline{u}^{(xy)*}$ to the boundary of the hexagon, while the transient term of the negative sequence $\Delta\underline{u}_{\mathrm{n}}^{(xy)*}$ will be set to zero. Therefore, the limited transient reference voltage vector $\Delta\underline{u}_{\mathrm{r}}^{(xy)*}$ will be equal to the limited transient positive-sequence voltage vector $\Delta\underline{u}_{\mathrm{r,p}}^{(xy)*}$. The components of the reduced transient vector $\Delta\underline{u}_{\mathrm{r,p}}^{(xy)*}$ in the x- and in the y-direction can be written as

$$\Delta u_{x\mathrm{r,p}}^{*} = \frac{u_{\mathrm{dc}}}{\sqrt{2}} - u_{x\mathrm{ffi}}^{*} \tag{3.96}$$

$$\Delta u^*_{yr,p} = \Delta u^*_{yp} \frac{\Delta u^*_{xr,p}}{\Delta u^*_{xp}} \tag{3.97}$$

The back-calculated error for the positive and the negative sequence of the current can be calculated by using Eqs.(3.92) and (3.93), respectively.

Figure 3.68 shows the simulation results of the shunt-connected VSC using DVCC and DPVL under balanced conditions of the grid voltage when applying a step in the positive sequence active current. The operating point is $i_{dp} = -0.5$ pu and $i_{qp} = 0.25$ pu. The negative-sequence d-current is equal to -0.5 pu, while the q-current is set to 0.25 pu. At $t = 20$ ms the reference active current makes a step with amplitude 1 pu and duration 40 ms. Due to the large variation in the demanded current the VSC saturates, as indicated by the signal "sat".

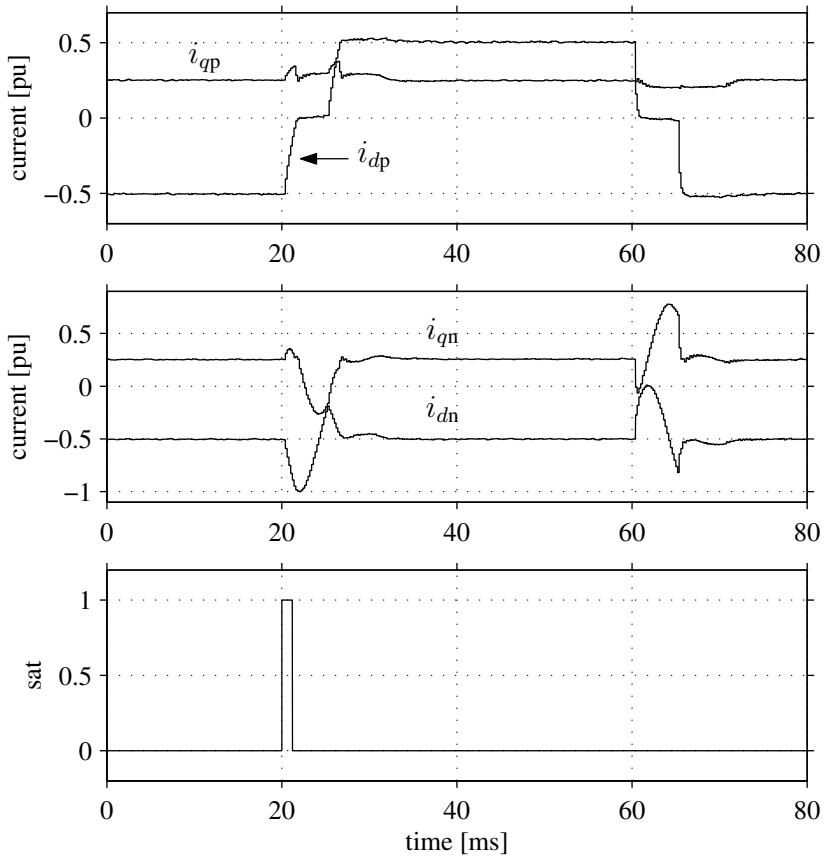


Fig. 3.68 Simulated current response to reference active current step during VSC saturation. DVCC and DPVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

Compared with DSVL and DDVL, the cross-coupling in the positive sequence q-current i_{qp} shows a small overshoot during the positive flank of i_{dp}. Moreover, the cross-coupling term in the negative-sequence d-current when the VSC saturates is slightly smaller as compared to using DDVL (Fig.3.66). This is due to the fact that since the voltage vector $\underline{u}^{(xy)*}_p$ exceeds the boundary of the hexagon due to the step, the transient term of the negative sequence voltage vector $\Delta\underline{u}^{(xy)*}_n$ is set to zero.

Figure 3.69 shows the transient performance of shunt-connected VSC with DVCC and DPVL during a step in the negative-sequence d-current. Starting from the same operating point as in the previous example of Fig.3.68, at $t = 20$ ms the reference current $i^*_{d\mathrm{n}}$ makes a step of amplitude 1 pu and duration 40 ms. The VSC does not go into saturation during the positive flank of the current step, but it saturates at the step down. In this case, the voltage vector $\underline{u}_{\mathrm{p}}^{(xy)*}$ remains inside the hexagon also during saturation, therefore the DPVL limits the transient term of the negative sequence component $\Delta\underline{u}_{\mathrm{n}}^{(xy)*}$, while $\Delta\underline{u}_{\mathrm{p}}^{(xy)*}$ is maintained constant. This was shown in the simulation by an additional signal, not shown in Fig.3.69 for clarity.

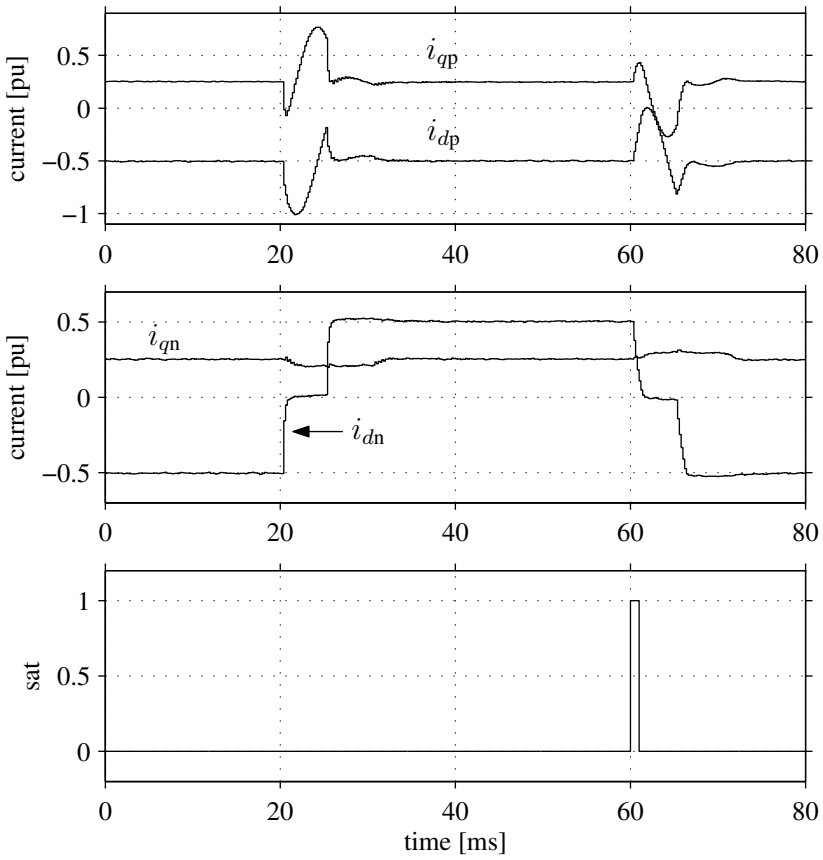


Fig. 3.69 Simulated current response to reference d-component negative sequence current step during VSC saturation. DVCC and DPVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

Dynamic negative vector limitation strategy (DNVL)

Finally, it might be desired to maximize the injection of negative sequence in the grid during saturation, by adopting a dynamic negative vector limitation strategy (DNVL). As for the DPVL, two different situation can occur during saturation: the negative sequence voltage vector is located inside the hexagon, as in Fig.3.70(a), or the negative sequence voltage vector exceeds the hexagon boundary, as in Fig.3.70(b).

If the negative sequence voltage vector is inside the hexagon, the transient term of the positive

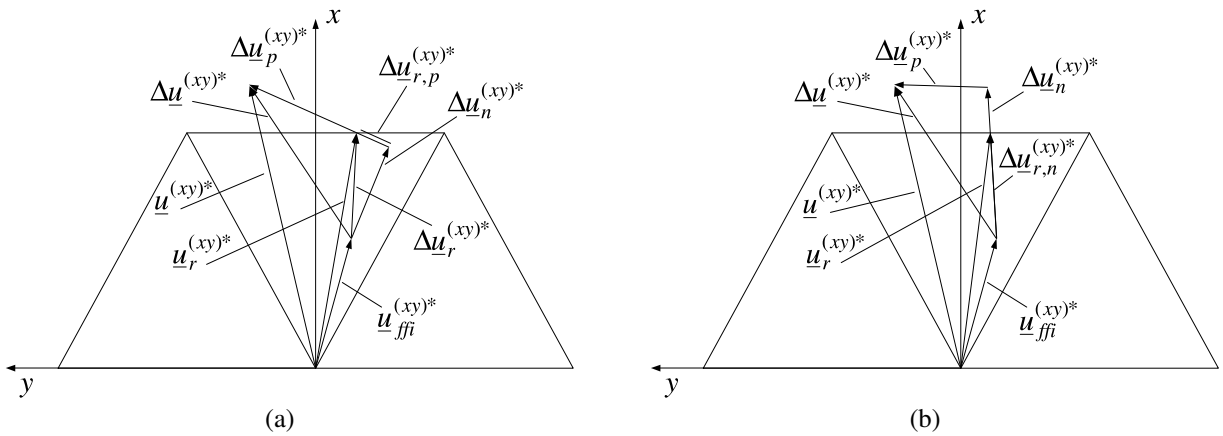


Fig. 3.70 Principle of DNVL method to avoid VSC saturation. Negative sequence reference voltage vector inside hexagon boundary, plot (a); negative sequence voltage vector outside hexagon boundary, plot (b).

sequence voltage vector $\Delta\underline{u}_{\mathrm{p}}^{(xy)*}$ is limited in order to reduce the transient reference voltage $\Delta\underline{u}_{\mathrm{r}}^{(xy)*}$ to the boundary of the hexagon, while the transient term of the negative sequence vector $\Delta\underline{u}_{\mathrm{n}}^{(xy)*}$ is maintained constant. The components of the reduced vector $\Delta\underline{u}_{\mathrm{r,p}}^{(xy)*}$ in the x- and in the y-direction obtained as

$$\Delta u_{x\mathrm{r,p}}^{*} = \frac{u_{\mathrm{dc}}}{\sqrt{2}} - u_{x\mathrm{ffi}}^{*} - \Delta u_{x\mathrm{n}}^{*} \tag{3.98}$$

$$\Delta u_{y\mathrm{r,p}}^{*} = \Delta u_{y\mathrm{p}}^{*} \frac{\Delta u_{x\mathrm{r,p}}^{*}}{\Delta u_{x\mathrm{p}}^{*}} \tag{3.99}$$

In this case, only back-calculation of the positive-sequence current error should be considered, which can be calculated by using Eq.(3.92).

If the negative sequence of the reference voltage vector $\underline{u}_{\mathrm{n}}^{(xy)*}$ exceeds the boundary of the hexagon, as in Fig.3.70(b), its transient term will be scaled in order to reduce the transient reference voltage $\Delta\underline{u}^{(xy)*}$ to the boundary of the hexagon, while the transient term of the positive sequence $\Delta\underline{u}_{\mathrm{p}}^{(xy)*}$ will be set to zero. Therefore, the limited reference transient voltage vector $\Delta\underline{u}_{\mathrm{r}}^{(xy)*}$ will be equal to the limited transient negative-sequence voltage vector $\Delta\underline{u}_{\mathrm{r,n}}^{(xy)*}$, whose components in the x- and in the y-direction can be written as

$$\Delta u_{x\mathrm{r,n}}^{*} = \frac{u_{\mathrm{dc}}}{\sqrt{2}} - u_{x\mathrm{ffi}}^{*} \tag{3.100}$$

$$\Delta u_{y\mathrm{r,n}}^{*} = \Delta u_{y\mathrm{n}}^{*} \frac{\Delta u_{x\mathrm{r,n}}^{*}}{\Delta u_{x\mathrm{n}}^{*}} \tag{3.101}$$

The back-calculated error for positive- and the negative-sequence current can be calculated by using Eqs.(3.92) and (3.93), respectively.

During normal operation, the grid voltage vector is mainly positive sequence, thus the negative-sequence reference voltage $\underline{u}_{n}^{(xy)*}$, if at all present, is very small compared with $\underline{u}_{p}^{(xy)*}$. Therefore, it is not realistic to consider that the VSC saturates due to a variation in the required

negative sequence current. However, for completeness also this case has been investigated. In order to have a large negative sequence component for the reference voltage vector also during steady state, the DVCC with DNVL has been tested under the grid voltage with 50% unbalance displayed in Fig.3.71. The operating point is $i_d = -0.5$ pu and $i_q = 0.25$ pu for both positive and negative sequence. Figure 3.72 shows the transient performance of the shunt-connected VSC using DVCC and DNVL during a step in the negative-sequence d-current. At $t = 20$ ms the reference current $i^*_{d\text{n}}$ makes a step with amplitude 1 pu and duration 40 ms. Despite the consistent magnitude of the current step, the direction of the corresponding reference voltage step is such that the VSC does not saturate during the step up, but it does at the step down. In this case, the voltage vector $\underline{u}_{\text{n}}^{(xy)*}$ remains inside the hexagon also during saturation, therefore the DNVL limits the transient term of the positive sequence component $\Delta\underline{u}_{\text{p}}^{(xy)*}$, while $\Delta\underline{u}_{\text{n}}^{(xy)*}$ is kept constant.

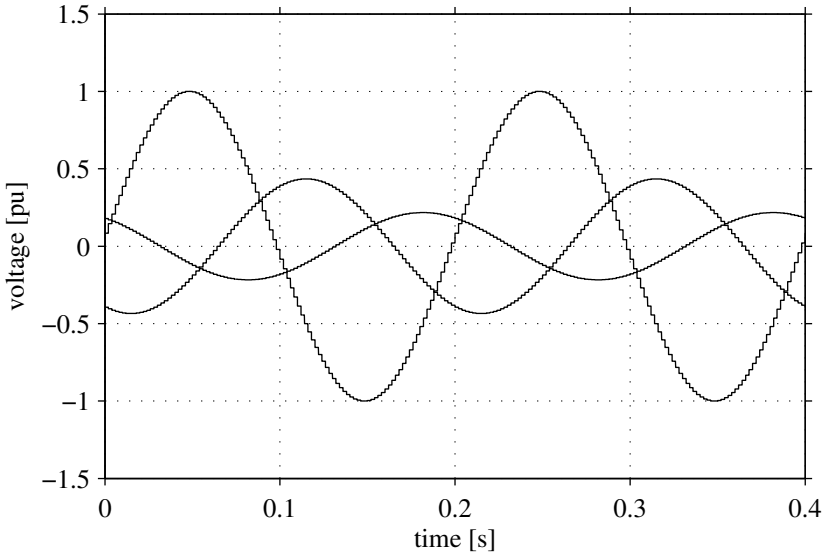


Fig. 3.71 Simulated unbalanced three-phase grid voltages.

Figure 3.73 shows the transient performance of shunt-connected VSC with DVCC and DNVL when the negative component of the reference voltage vector $\underline{u}_n^{(xy)*}$ exceeds the boundary of the hexagon. To achieve this case starting from the same operating point, a very large step of 2 pu has been applied to the reference current $i_{d\text{n}}^{(xy)*}$. During the positive flank of the step, the voltage vector $\underline{u}_{\text{n}}^{(xy)*}$ remains inside the hexagon also during saturation, therefore the DNVL limits the transient term of the positive sequence component $\Delta\underline{u}_{\text{p}}^{(xy)*}$, while $\Delta\underline{u}_{\text{n}}^{(xy)*}$ is maintained constant. During the step down, instead, the voltage vector $\underline{u}_{\text{n}}^{(xy)*}$ exceeds the boundary of the hexagon, therefore the DNVL limits the vector $\Delta\underline{u}_{\text{n}}^{(xy)*}$, while the transient term of the positive sequence voltage vector $\Delta\underline{u}_{\text{p}}^{(xy)*}$ is set to zero.

Summary

In this section, the problem of VSC saturation when using DVCC has been discussed. Different limitation strategies have been presented and tested via simulation. It has been shown that,

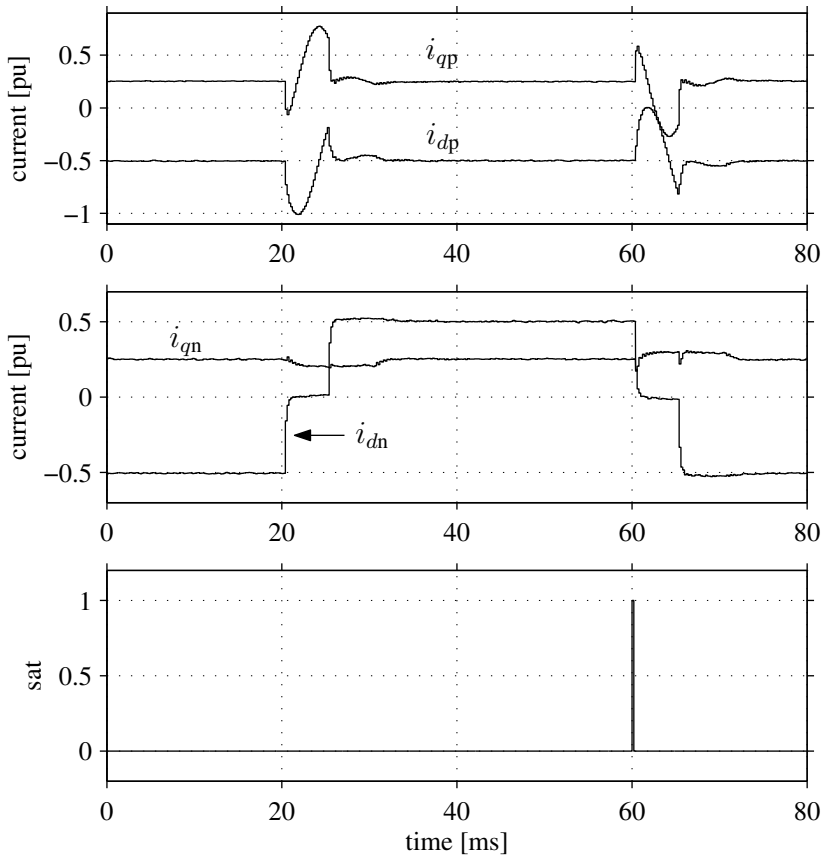


Fig. 3.72 Simulated current response to reference d-component negative sequence current step during VSC saturation. DVCC and DNVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

due to the delay introduced by the adopted SSM and due to the short overmodulation time, all three limitation methods present equivalent performance. The only exception is represented by DNVL, implemented to maximize the injection of negative-sequence component in the grid during saturation. It has been shown that this method is suitable when there is high percentage of unbalance in the grid voltage and large steps (2 pu) in the current have to be applied. Therefore, this method will be used very seldom in practice. In this thesis, the method adopted for limitation of the reference voltage vector when using DVCC is DDVL.

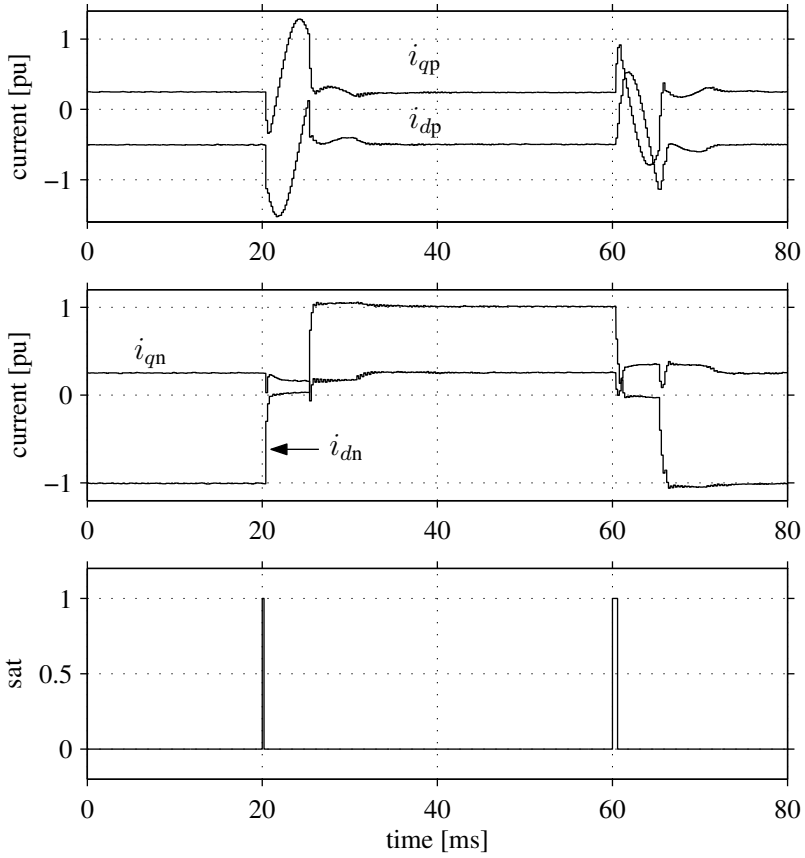


Fig. 3.73 Simulated current response to reference d-component negative sequence current step during VSC saturation. DVCC and DNVL are used. Top: positive sequence in positive SRF; middle: negative sequence in negative SRF; bottom: saturation signal.

3.5.2 Simulation results using DVCC

In this section, simulation results of shunt-connected VSC using DVCC will be presented. Control system parameters are displayed in Table 3.3. The dynamic performance of DVCC has been tested under the same unbalanced conditions of the grid voltage as the previous two vector current-controllers. Simulated unbalanced three-phase grid voltages are displayed in Fig.3.33 and in the dq-coordinate system in Fig.3.57. The operating point is equal to 0.125 pu active current and 0.25 pu reactive current for the positive sequence, while both d- and q-components of the negative-sequence current are equal to zero. The reference active current makes a step after 0.02 s with amplitude 0.375 pu and duration 0.04 s, as shown by the simulated positive-sequence current plotted in Fig.3.74. The actual current takes a quarter of the line period to track the reference current, due to the SSM. A small cross-coupling can be noticed in the q-current. The negative sequence dq-currents, displayed in Fig.3.75, show significant cross-coupling, due to the sequence detection.

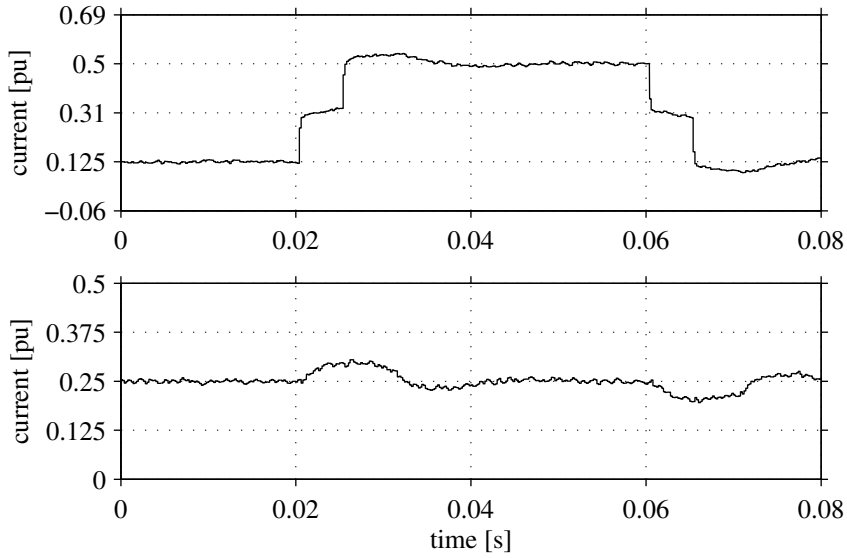


Fig. 3.74 Simulated positive-sequence current response to reference active current step. Positive-sequence components in positive SRF. DVCC and unbalanced grid are used. Top: d-component; bottom: q-component.

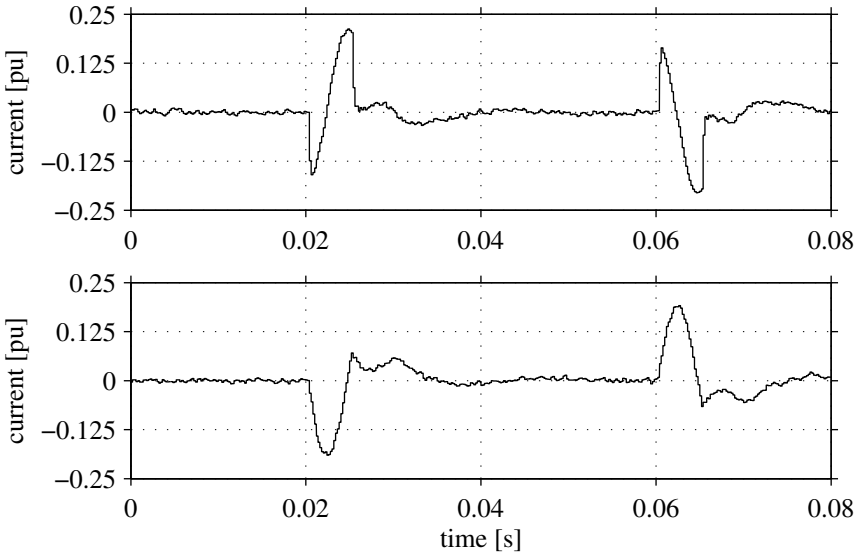


Fig. 3.75 Simulated negative-sequence current response to reference active current step. Negative-sequence components in negative SRF. DVCC and unbalanced grid are used. Top: d-component; bottom: q-component.

Voltage dip response

The delay introduced by the sequence detection in the current affects also the response to voltage dips. The DVCC has been tested with the same unbalanced voltage dip shown in Fig.3.44 (positive- and negative-sequence dq-voltages are shown in Fig.3.60). As shown in Fig.3.76 and

Fig.3.77, the measured d-currents for both sequences are affected by two identical transient spikes with 5 ms in between. It then takes 5 ms more to restore the current exactly to the steady-state value. The q-currents also show two identical subsequent transients, due to cross-coupling, in both sequences. This behavior is due to the use of DSC for sequence separation of both grid voltage and VSC current, differently from VCC2, where only the grid voltage is separated into sequence components and only one current spike can be observed in the currents (see Fig.3.61). The current spike in Fig.3.76 has smaller amplitude as compared to Fig.3.61, but a direct comparison is difficult as there is also a spike in the negative-sequence current.

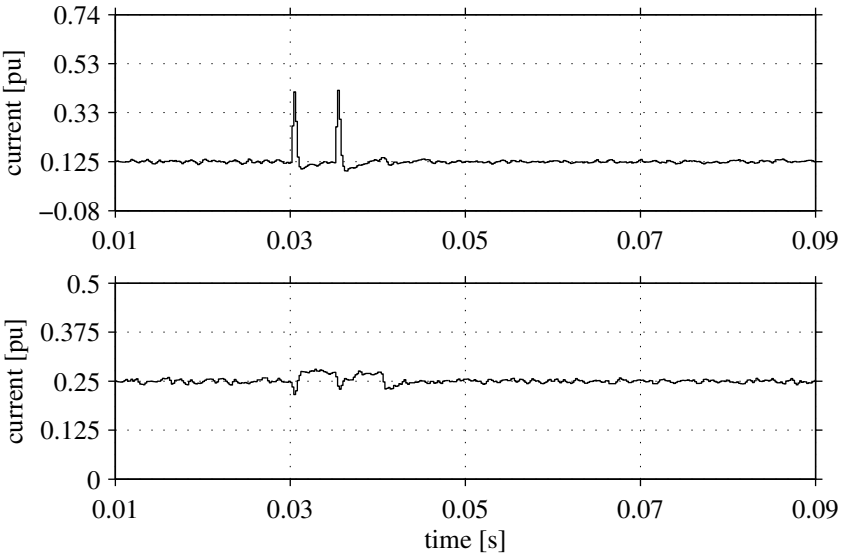


Fig. 3.76 Simulated positive-sequence current response to unbalanced voltage dip. DVCC is used. Top: d-component; bottom: q-component.

3.6 Conclusions

In this chapter, a comprehensive analysis of the vector current-controller for shunt-connected VSC has been presented. Three different current controllers have been investigated and compared under balanced and unbalanced conditions of the grid voltage and under symmetrical and unsymmetrical voltage dips. With a constant DC-link voltage, steps in the reference currents have been applied in order to test the dynamic performance of the system. It has been demonstrated that, using vector current-controller type 1 (VCC1), designed by only considering positive sequence components, the dq-currents under unbalanced grid voltage are affected by an oscillation at double the power frequency. By feeding the same controller only the positive-sequence component of the grid voltage in the vector current-controller type 2 (VCC2), the response is improved and the actual current tracks the reference current with almost no delay. The dual vector current-controller (DVCC), where both voltages and currents are separated into their sequence components and two separate current controllers are used, showed a slower response compared with VCC2 response, due to the delay introduced by the sequence separation.

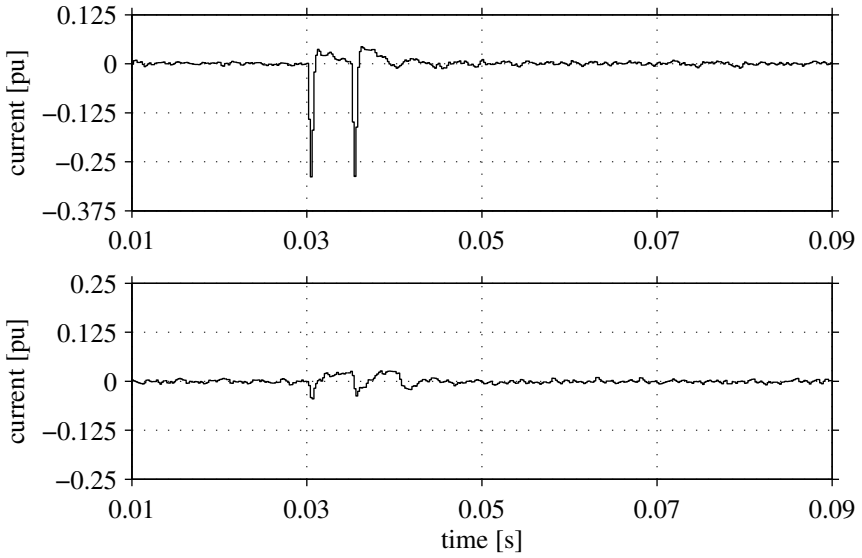


Fig. 3.77 Simulated negative-sequence current response to unbalanced voltage dip. DVCC is used. Top: d-component; bottom: q-component.

Since it presents a fast response and can operate properly both under balanced and unbalanced conditions of the grid voltage, the VCC2 seems to be the most suitable option for control of shunt-connected VSC. However, as it will be discussed in Chapter 5, in some applications where the current controller is used as inner loop of a cascade controller, control of both positive and negative sequences of the filter current might be needed, thus DVCC has to be used. In the next chapter, experimental verification of the vector current-controllers discussed here will be presented.

Chapter 4

Experimental results using shunt-connected VSC

4.1 Introduction

To validate the results obtained via simulation for the shunt-connected VSC, the three controllers have been tested experimentally under balanced and unbalanced conditions of the grid voltage and under symmetrical and unsymmetrical voltage dips. In this chapter, a description of the laboratory setup and of the components used will be given, and experimental results for the three different current controllers will be presented.

4.2 Laboratory setup

The single-line diagram of the experimental setup is given in Fig.4.1. The VSC has been connected through an L-filter to an analog model of a transmission line. System parameters are reported in Table 3.1. The load is a three-phase resistor of 8.8 Ω, corresponding to 18 kW. In order to absorb an unbalanced current from the mains, an additional resistance of 4.2 Ω can be connected between two phases closing contactor 3 in Fig.4.1.

All experiments have been carried out with a fixed DC-link voltage by using a DC machine rated 700 V, 60 A. Figure 4.2 is a picture of the actual setup in the Power System Laboratory. The main components of the laboratory setup are described in more detail in the following.

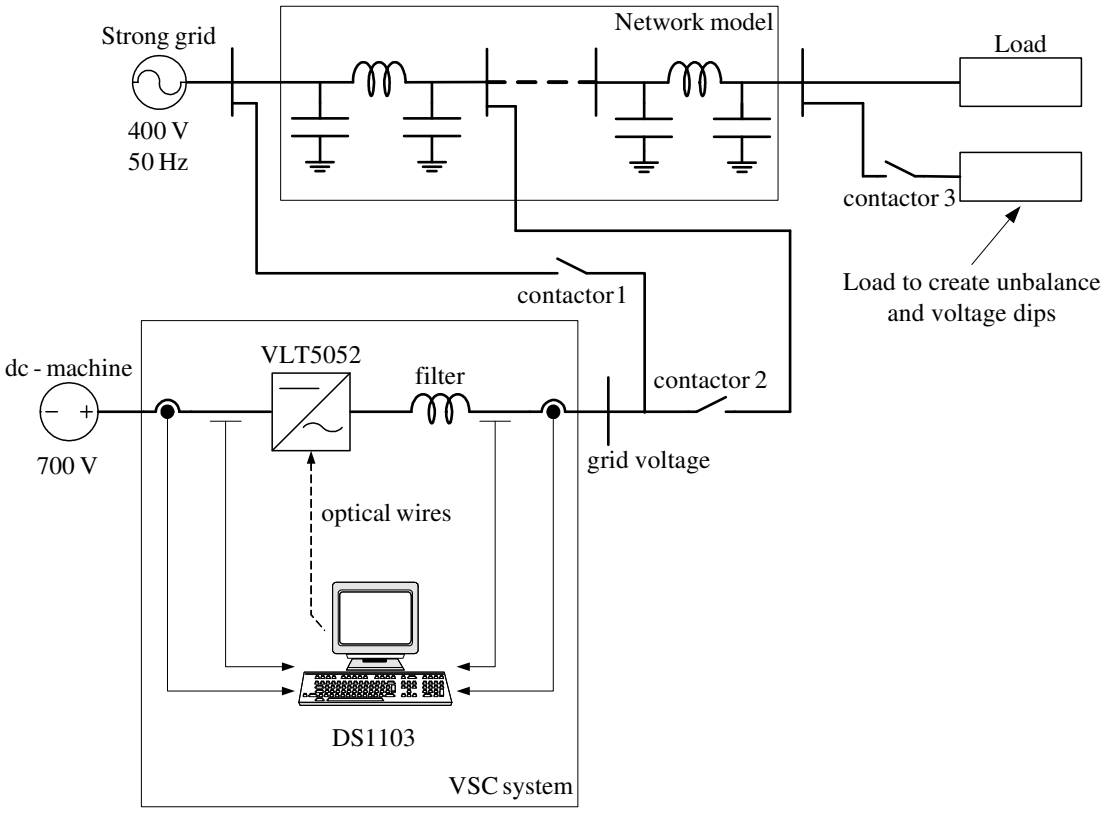


Fig. 4.1 Single-line diagram of laboratory setup.

Fig. 4.2 Photo of laboratory setup.

4.2.1 Network model

The network model is a three-phase model of a 400 kV transmission system. The entire model operates at 400 V, consequently the voltage scale is 1:1000 [21]. As shown in Fig.4.3, the network model can be supplied both using a 75 kVA synchronous generator (reproduction of the Harsprånget hydro power plant located by the Luleå river in the north of Sweden) or through a distribution transformer using the local distribution network, denoted in the figure as strong grid.

The transmission line model consists of six identical π-sections, each corresponding to 150 km of line at 400 kV. Each π-section of the model is constituted by series reactors (denoted in the figure by $R_{\mathrm{g,m}}$ and $L_{\mathrm{g,m}}$) and shunt capacitors (denoted by $C_{\mathrm{g,m}}$). The data for the real 150 km section of the 400 kV line are

$$X_{\mathrm{g}} = 50.4\ \Omega \tag{4.1}$$
$$R_{\mathrm{g}} = 4.17\ \Omega \tag{4.2}$$
$$C_{\mathrm{g}} = 0.065767\ \mu\mathrm{F} \tag{4.3}$$

while the scaled data of the 400 V network model are

$$X_{\mathrm{g,m}} = 0.644\ \Omega \tag{4.4}$$
$$R_{\mathrm{g,m}} = 0.05\ \Omega \tag{4.5}$$
$$C_{\mathrm{g,m}} = 46\ \mu\mathrm{F} \tag{4.6}$$

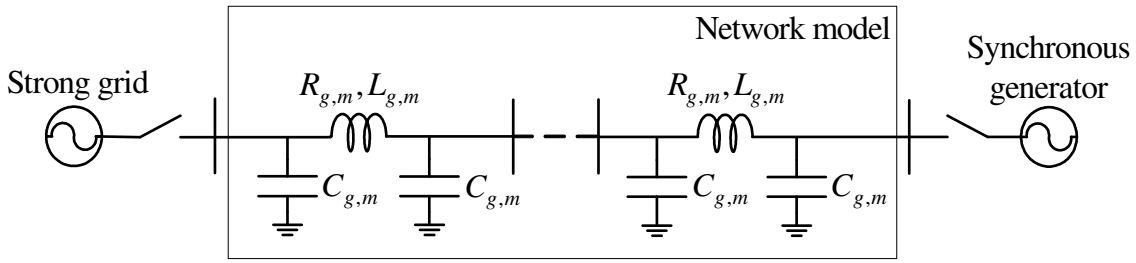


Fig. 4.3 Single-line diagram of network model.

All sections can be connected arbitrarily in series or in parallel. For these experiments the π-sections have been connected in series, as shown in Fig.4.3, and, in order to have a strong supply, the network model has been supplied using the strong grid.

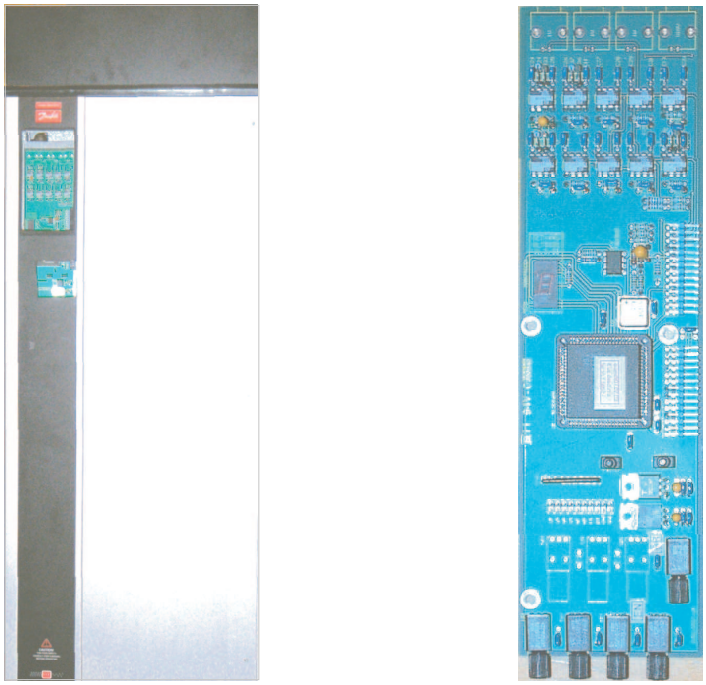
4.2.2 VSC and control card

The VSC used in this laboratory setup is a Danfoss VLT5052. The data of the VSC are reported in Table 4.1. To provide the firing pulses at the gate of the IGBTs, an interface and protection card (IPC) built by Aalborg University has been used. The IPC is a replacement for the original

TABLE 4.1. DATA FOR VSC.

rated power	64.7 kVA
rated voltage	420 V
rated current	90 A
DC-link capacitor	4.7 mF

card of the Danfoss VTL5052 with the purpose of providing external control over the IGBT gate drivers. Protection against short-circuit overcurrent, DC-overvoltage protection, inverter-leg shoot-through and overtemperature is provided. Moreover, the IPC card provides a 3-μs hardware blanking time for the switching signals. The Danfoss VLT5052 is shown in Fig.4.4(a) and the IPC card in Fig.4.4(b).



(a) (b)

Fig. 4.4 Photo of Danfoss VLT5052 (a), and of IPC card (b).

4.2.3 Control computer system

The control computer system consists of a PC with a DS1103 PPC controller board. The DS1103 can be programmed using C-code or using Matlab/Simulink [18]. The board is provided together with the software "Control Desk", which allows real-time management of the inputs and outputs by providing a virtual control panel with instruments and scopes and which allows to modify all controller parameters during the experiment. One important feature of

DS1103, which makes it very suitable for this application, is the high number of analog inputs. The board has four parallel A/D-converters with 16-bit resolution and 4 μs sampling time, which can be multiplexed to four channels each, and four parallel single-channel A/D-converters with 12-bit resolution and 800 ns sampling time. This gives a total of 20 analog inputs available. Moreover, the hardware interrupt signal can be controlled and the board itself has the capability of generating three-phase PWM pattern (in one single output) and four independent single-phase PWM outputs.

4.2.4 Dc-link protection

When a VSC is connected to the AC grid, one of the most critical problems is its protection against voltage swells. In fact, if an overvoltage occurs in the grid and the voltage on the AC side of the VSC becomes higher than the voltage on the DC side, the exceeding energy will be pumped from the grid to the DC link and (especially if the VSC is blocked) the IGBTs can be destroyed.

To prevent such problem, in applications where the VSC is operating connected to the grid, usually a voltage transducer and an overvoltage relay that disconnects the DC power supply in case of overvoltage can be used. If a rapid return to service is required, another option is to use a DC chopper connected in shunt between the DC supply and the DC side of the VSC (Fig. 4.5) in order to dissipate the energy in excess in a damping resistor, denoted in the figure by R_{chopper}.

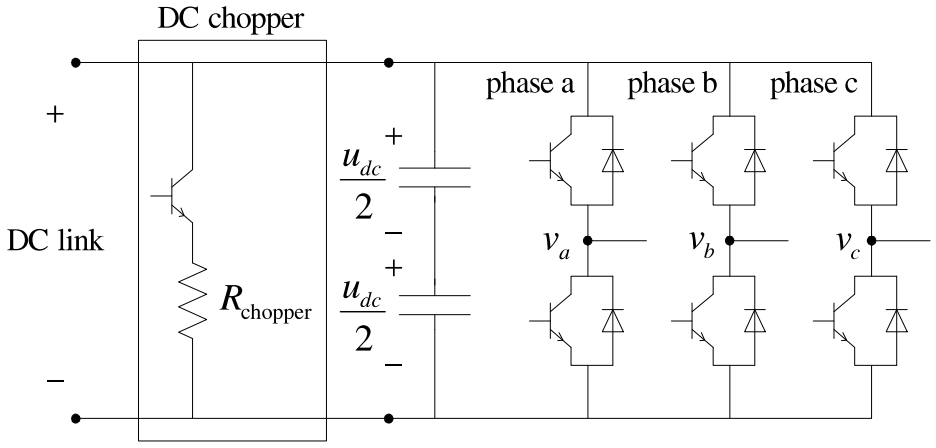
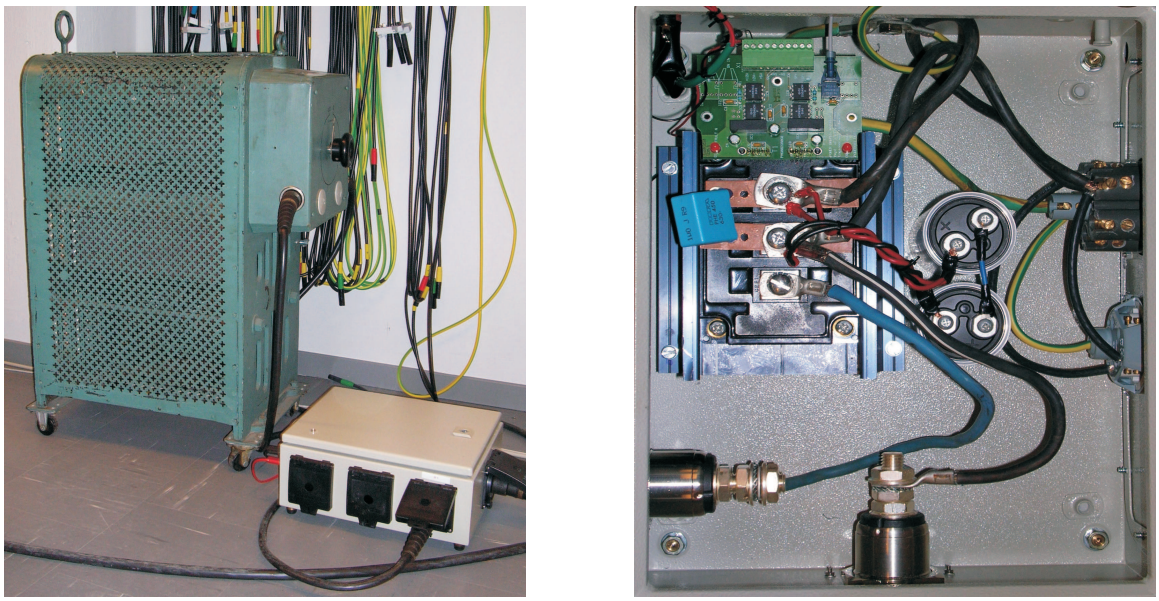


Fig. 4.5 Main circuit of VSC with DC chopper.

In the design of the DC chopper, and in particular of its resistor, the following requirements must be considered:

- The DC capacitors should discharge as fast as possible;
- The initial discharge current should not exceed the maximum current allowed through the IGBT of the chopper.

In this setup, a resistor of $12\,\Omega$, as suggested in the Danfoss Design Guide [59], has been chosen. A picture of the DC chopper if displayed in Fig.4.6(a), while a picture showing a detail of IGBT of the chopper with its snubber circuit is shown in Fig.4.6(b).



(a) (b)

Fig. 4.6 Photo of DC chopper (a), and detail of chopper's IGBT with snubber circuit (b).

4.3 Experimental results using VCC1

To validate the results obtained in Section 3.2.6, the VCC1 has been tested on the VSC system in the laboratory under balanced and unbalanced conditions of the grid voltage and during symmetrical and unsymmetrical voltage dips.

4.3.1 Balanced grid voltages

A first set of tests has been carried out with balanced grid voltage applied to the VSC. The controller parameters are the same used for the simulations and reported in Table 3.2. To ensure a correct estimation of the grid voltage angle without harmonic distortion, the bandwidth of the PLL has been set to 30 Hz. In order to have a stiff and symmetric AC voltage, the VSC has been connected directly to the strong grid by closing contactor 1 in Fig.4.1, while contactor 2 has been left open. Therefore, the grid voltage will not be affected by the current injected by the VSC. A simplified three-phase scheme of the system during this test is shown in Fig.4.7, where the block π denotes a π-section of the network model.

The measured three-phase grid voltages displayed in Fig.4.8 are sinusoidal and with constant amplitude equal to 1 pu. This can also be seen in Fig.4.9, which shows the grid voltages in

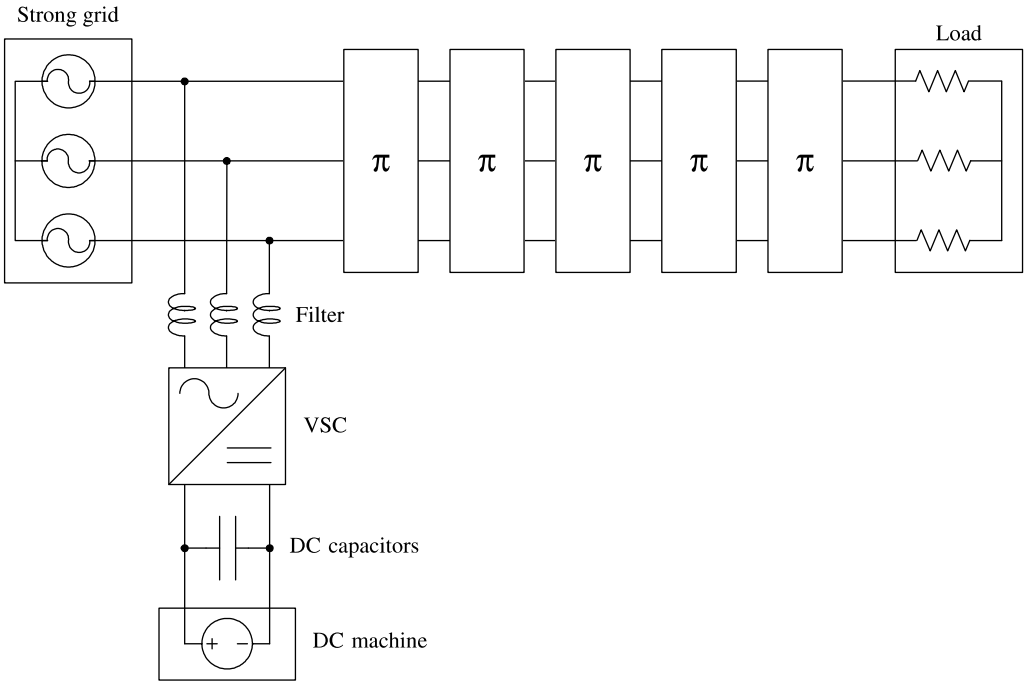


Fig. 4.7 Simplified three-phase scheme of laboratory setup to test VSC with balanced grid voltages.

the dq-coordinate system. It can be observed that the measured grid voltages are not purely sinusoidal but are affected by some harmonics, therefore they are not perfectly flat in the dq-coordinate system.

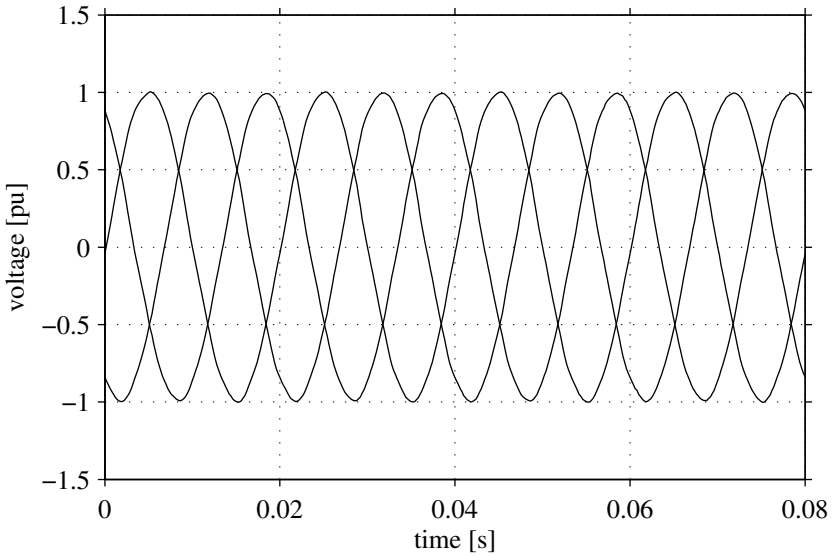


Fig. 4.8 Measured balanced three-phase grid voltages.

After 0.02 s a step from 0.125 to 0.5 pu with duration 0.04 s is applied to the reactive component of the current $i_{\mathrm{r}q}$. The active current $i_{\mathrm{r}d}$ is maintained constant and equal to 0.25 pu. As shown in

Fig.4.10, the control system works properly and the actual current tracks the reference current. Comparison with Fig.3.31 shows that the experimental results confirm the simulations.

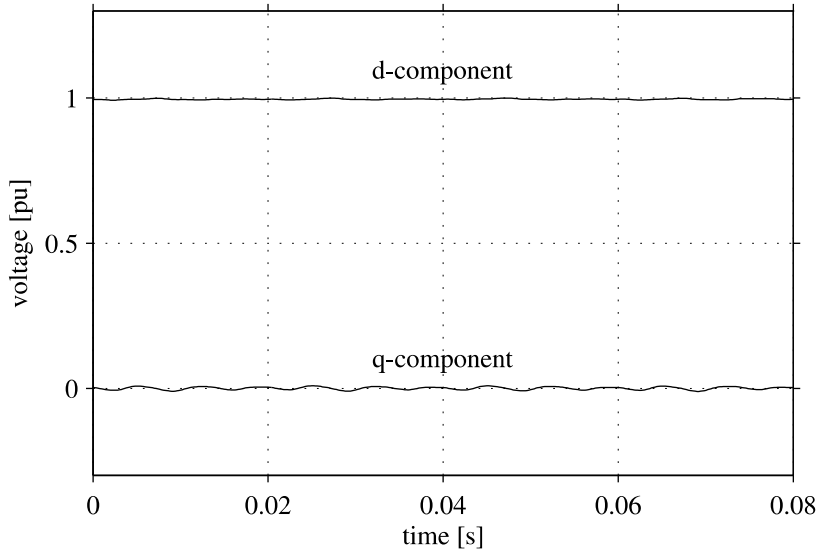


Fig. 4.9 Measured balanced grid voltage in dq-coordinate system.

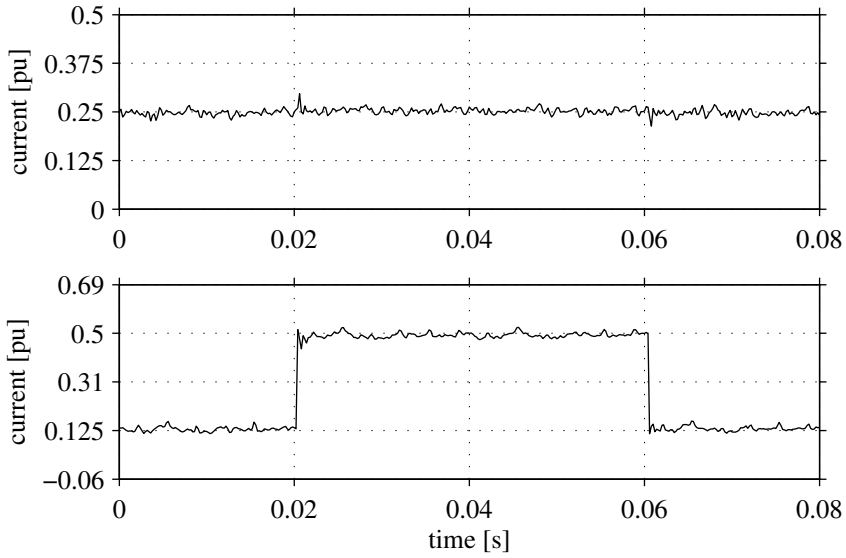


Fig. 4.10 Measured current response to reference reactive current step. VCC1 and balanced grid voltage are used. Top: d-component; bottom: q-component.

4.3.2 Unbalanced grid voltages

To create unbalance in the grid, the VSC has been connected after one π-section in the network model by opening contactor 1 and closing contactor 2 in Fig.4.1. Moreover, an additional resistor of 4.2 Ω has been connected between two phases by closing contactor 3. Figure 4.11 shows the three-phase scheme of the laboratory setup used for this experiment.

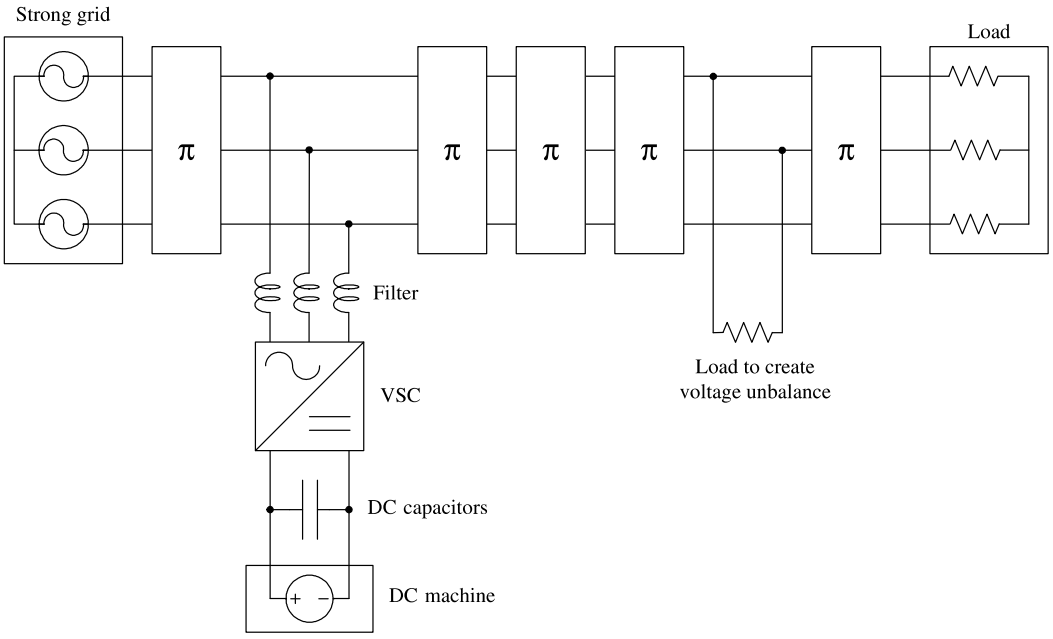


Fig. 4.11 Simplified three-phase scheme of laboratory setup to test VSC with unbalanced grid voltages.

When the VSC is connected to a weak grid, the control-system gain cannot be set to deadbeat. This is because of the assumption that the grid voltage components change slowly and can be considered constant over one sample, made when deriving the equations for vector current-controller in Section 3.2.1. Since in a weak grid the current injected by the VSC will affect the grid voltage, this assumption is not valid anymore and the speed of the controller has to be reduced to avoid instability. Therefore, the gain of the VCC1 has been set to 70% deadbeat. The parameters of the VCC1 are reported in Table 4.2. The unbalanced current circulating on

TABLE 4.2. CONTROLLER PARAMETERS FOR VCC1 WITH WEAK SUPPLY.

Sampling frequency	f_s = 5 kHz	Switching frequency	f_sw = 5 kHz
Proportional gain	k_p = 7.01	Integrator time constant	T_i = 0.0564 s
Observer gain	k_psp = 0.1		

the line inductance creates the three-phase voltage waveform shown in Fig.4.12 at the PCC. As shown, one phase voltage has an amplitude of 1 pu while the other two phases have an amplitude of 0.71 pu, resulting in a steady-state unbalance of 10.9%. Due to the unbalance, the grid voltage in the dq-coordinate system are affected by a 100 Hz oscillation with amplitude of 0.11 pu (peak-to-peak), as shown in Fig.4.13. Steps in the active power have been applied to the system. Due to the weak supply, the injection of power in the grid affects the grid voltage and this results in a ripple in the grid voltage, both at the beginning and at the end of the step.

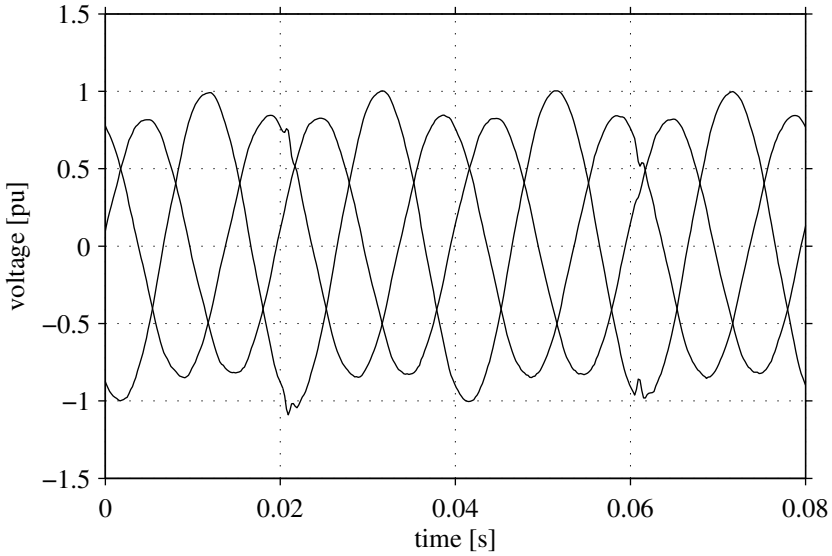


Fig. 4.12 Measured three-phase unbalanced grid voltages.

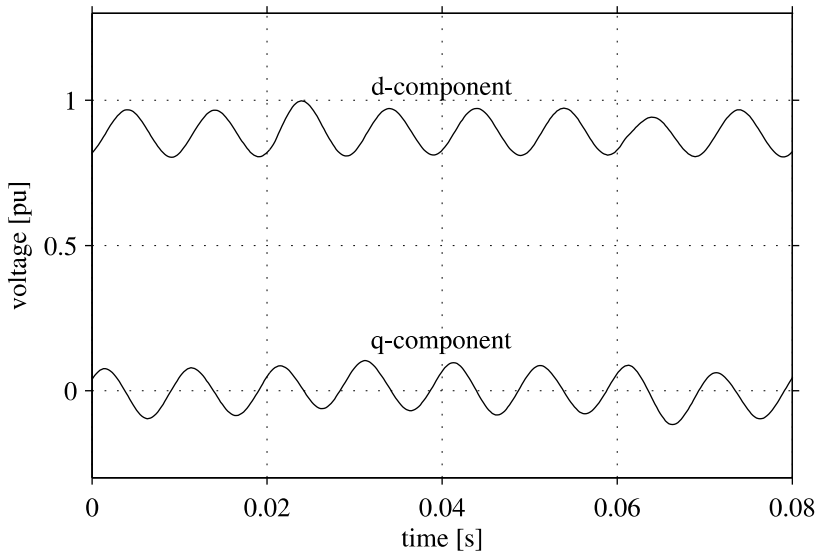


Fig. 4.13 Measured unbalanced grid voltages in dq-coordinate system.

Measured step response of active and reactive current due to a step in the reference active current is displayed in Fig.4.14. The operating point is equal to 0.25 pu reactive current and 0.125 pu active current. The reference active current makes a step after 0.02 s with amplitude 0.375 pu and duration 0.04 s. As expected from the simulation results shown in Section 3.2.6, the currents are also affected by a 100 Hz oscillation with amplitude of 0.4 pu (peak-to-peak) around the steady state value and during the step. The current flanks are not steep as in Fig.4.10 due to the reduced gain of the controller and show oscillations due to the weak grid voltage. The oscillations in the measured current are larger compared with the simulation displayed in Fig.3.35. Again, this is due to the weak supply, which was not included in the simulation model, and to the slow PLL.

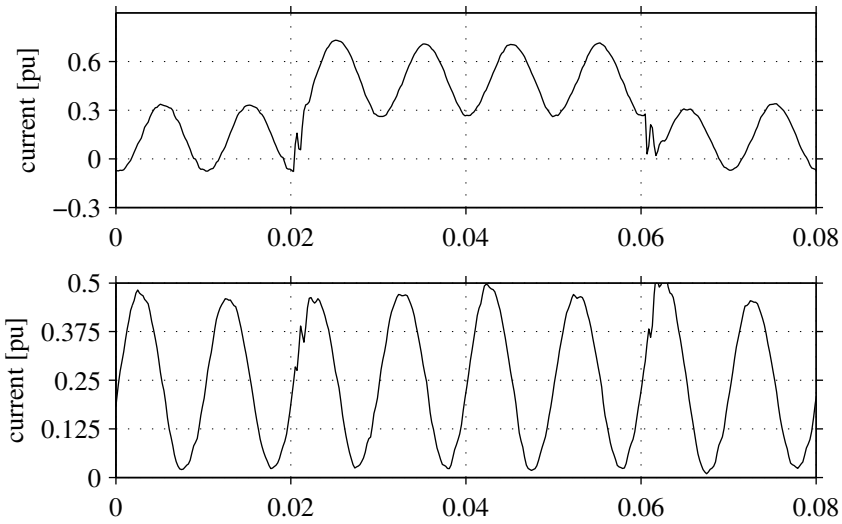


Fig. 4.14 Measured current response to reference active current step. VCC1 and unbalanced grid voltage are used. Top: d-component; bottom: q-component.

4.3.3 Voltage dip response

To test the VCC1 under balanced and unbalanced voltage dips, the VSC has been connected to the weak grid and three resistances of 2.1 Ω each have been inserted by closing contactor 3 shown in Fig.4.15 for 300 ms. The grid voltage was affected by a 71% symmetrical voltage dip, as shown in Fig.4.16 and in Fig.4.17 in dq-coordinate system.

As in the simulations shown in Section 3.2.6, the operating point is equal to $i_{\mathrm{r}d} = 0.125$ pu and $i_{\mathrm{r}q} = 0.25$ pu, as displayed in Fig.4.18. The controller manages to keep the actual current equal to the pre-fault value, despite a transient experienced at the beginning of the dip. This transient is smaller compared with the one obtained via simulation and its duration is longer compared to the simulation, shown in Fig.3.40. This is due to additional damping due to resistances in the actual system.

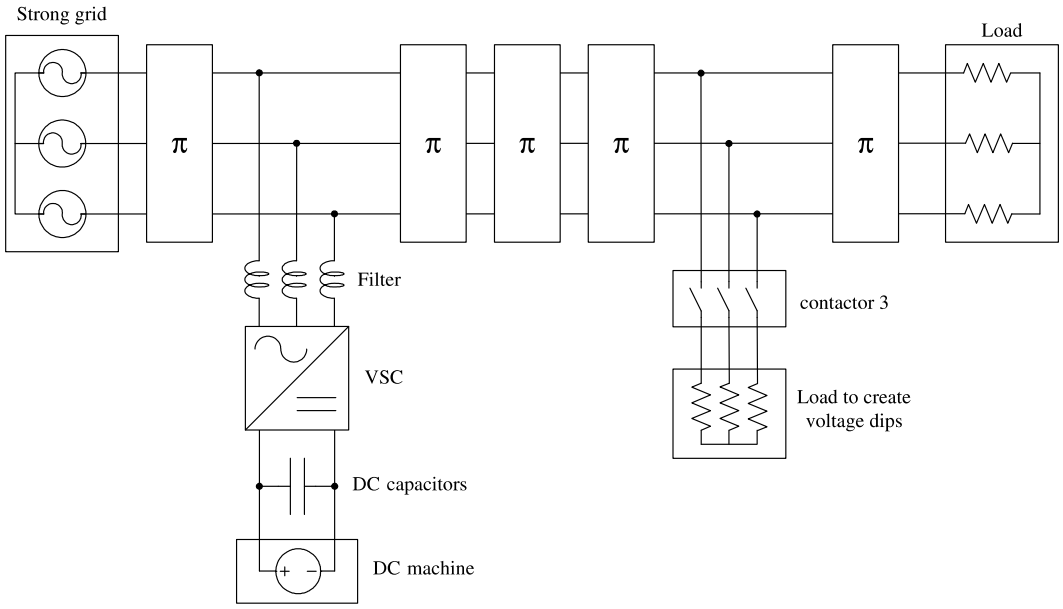


Fig. 4.15 Simplified three-phase scheme of laboratory setup to test VSC under balanced voltage dips.

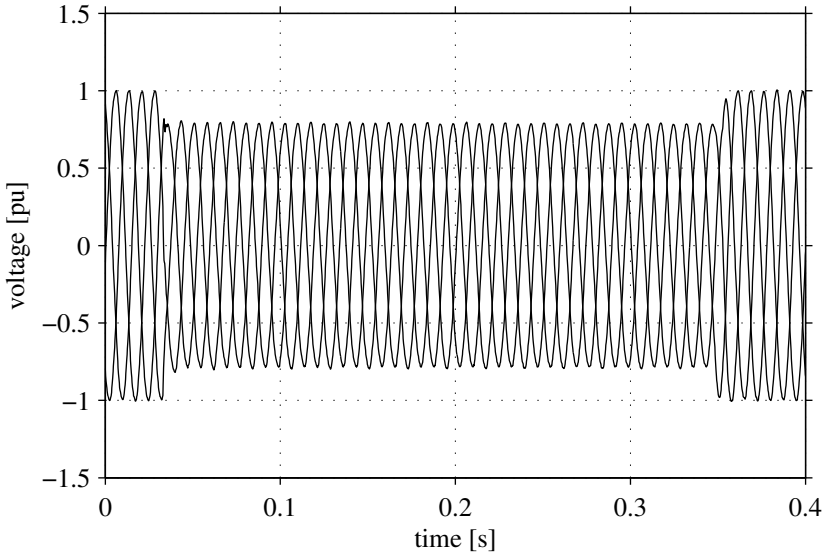


Fig. 4.16 Measured three-phase grid voltages during balanced voltage dip.

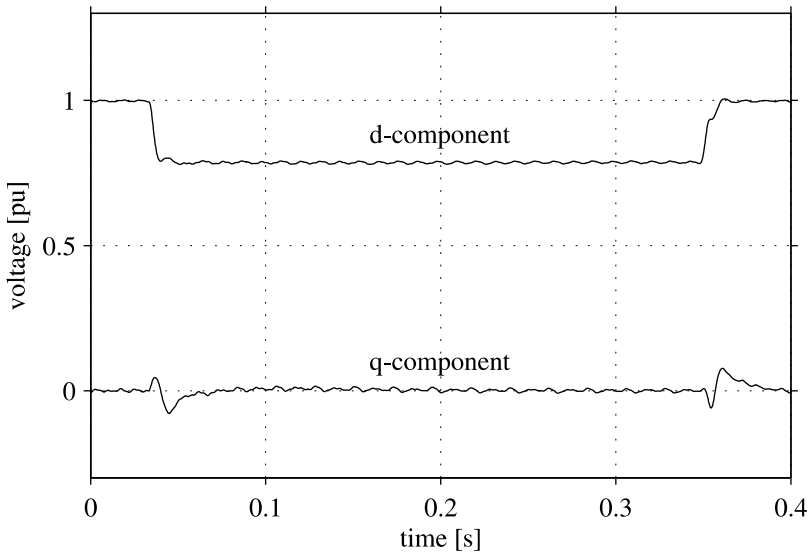


Fig. 4.17 Measured grid voltages in dq-coordinate system during balanced voltage dip.

Moreover, the shunt capacitors in the network model of will provide a smoother voltage variation at the VSC terminals. This can be seen in Fig.4.19, showing a detail of the grid voltage in the dq-coordinate system at the beginning of the dip. It is possible to observe that, due to the presence of the inductance of the π-section upstream of the PCC, a phase-angle jump of 9° is associated to the voltage dip. This can be noticed from Fig.4.17, where the q-component of the grid voltage is affected by a transient both at the beginning and at the end of the dip. From the figure it is possible to see that the PLL takes 0.03 s to track the grid voltage vector.

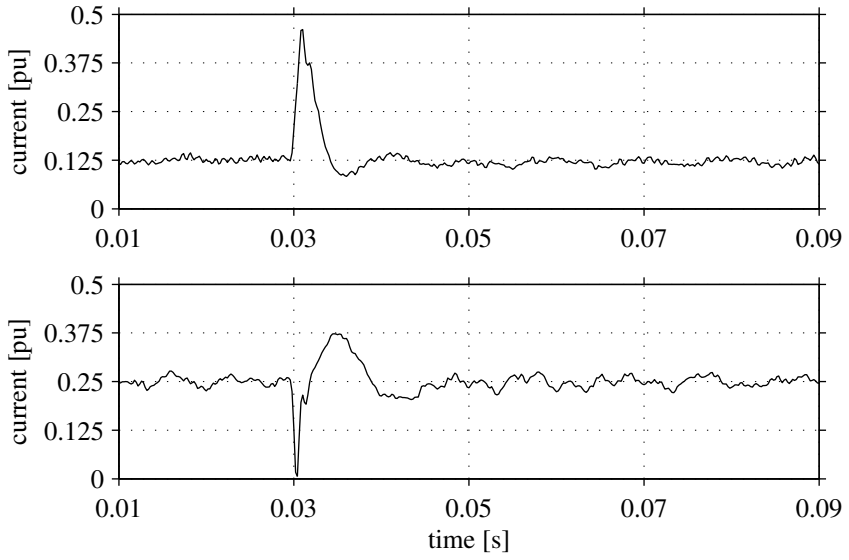


Fig. 4.18 Measured current response to balanced voltage dip. VCC1 is used. Top: d-component; bottom: q-component.

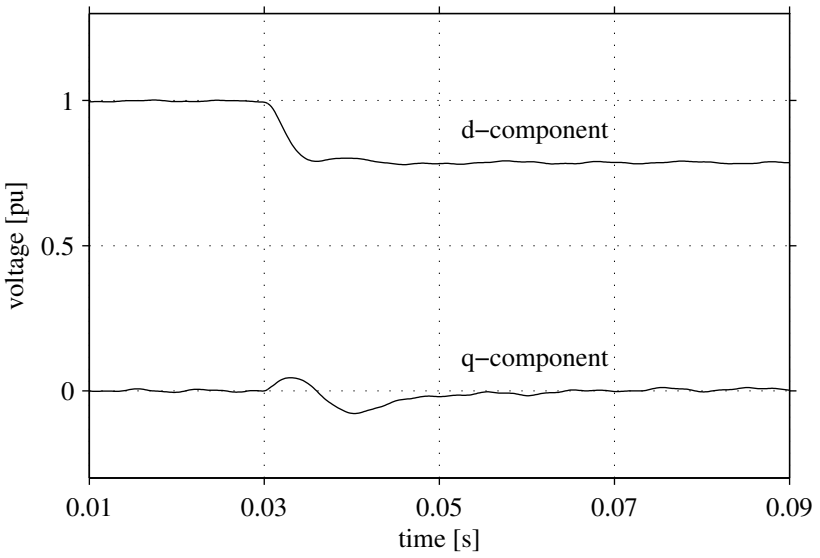


Fig. 4.19 Detail of measured grid voltages in dq-coordinate system during balanced voltage dip.

Finally, to test the VCC1 under unsymmetrical voltage dips, two phases were shorted through a 4.2 Ω resistor by closing contactor 3, as shown in Fig.4.20. As a result, the voltage waveforms shown in Fig.4.21 and Fig.4.22 (in the dq-coordinate system) have been obtained.

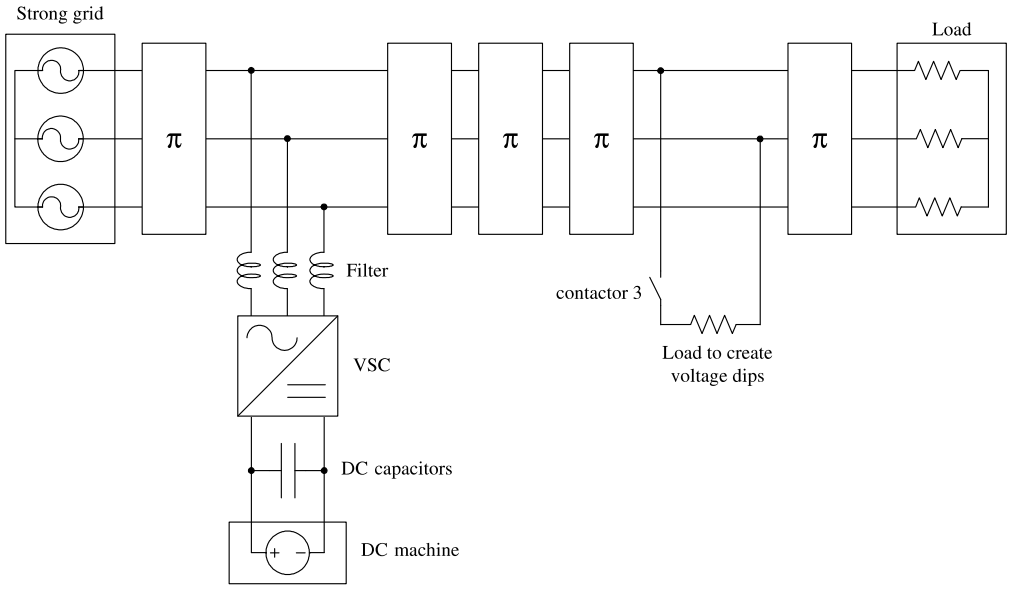


Fig. 4.20 Simplified three-phase scheme of laboratory setup to test VSC under unbalanced voltage dips.

As expected, the control system does not manage to keep the current constant at the pre-fault conditions and the measured line current is affected by a 100 Hz oscillation, as shown in Fig.4.23. Compared to the simulations shown in Fig.3.46, the behavior is the same, although the oscillations in the current are bigger during the dip, whereas the transient peak in the active current at the beginning of the dip is smaller.

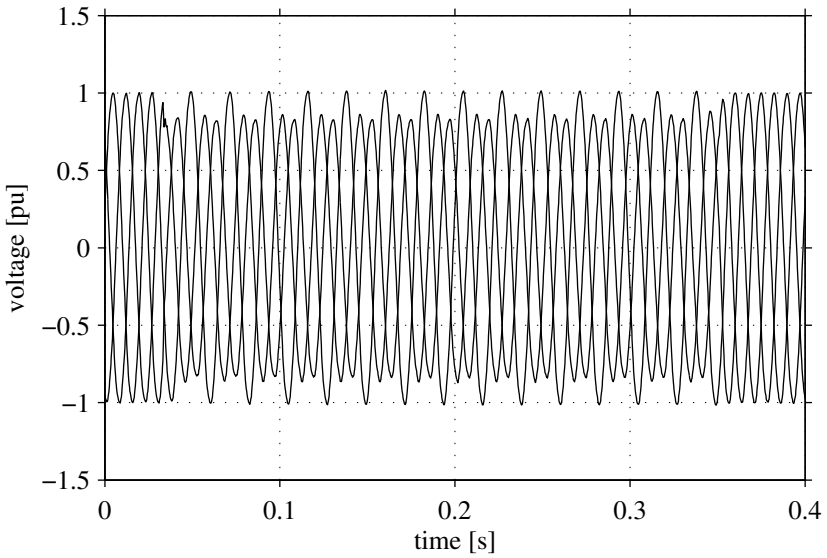


Fig. 4.21 Measured three-phase grid voltages during unbalanced voltage dip.

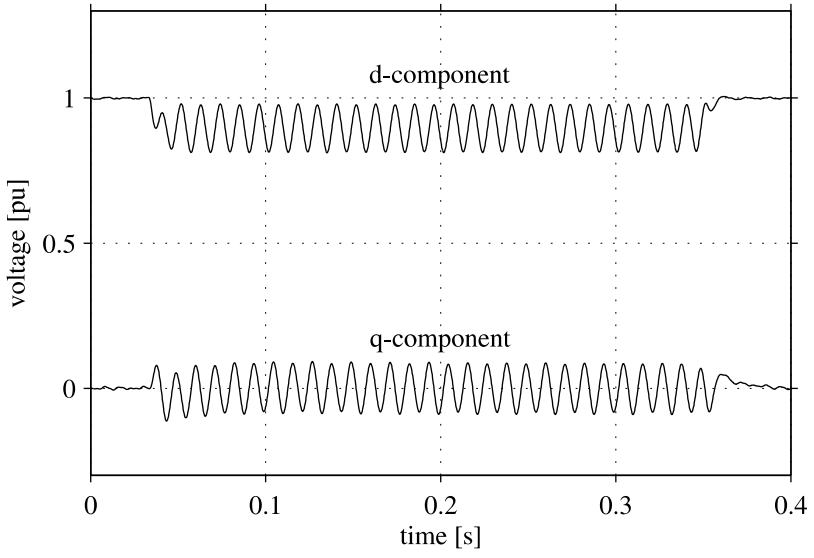


Fig. 4.22 Measured grid voltages in dq-coordinate system during unbalanced voltage dip.

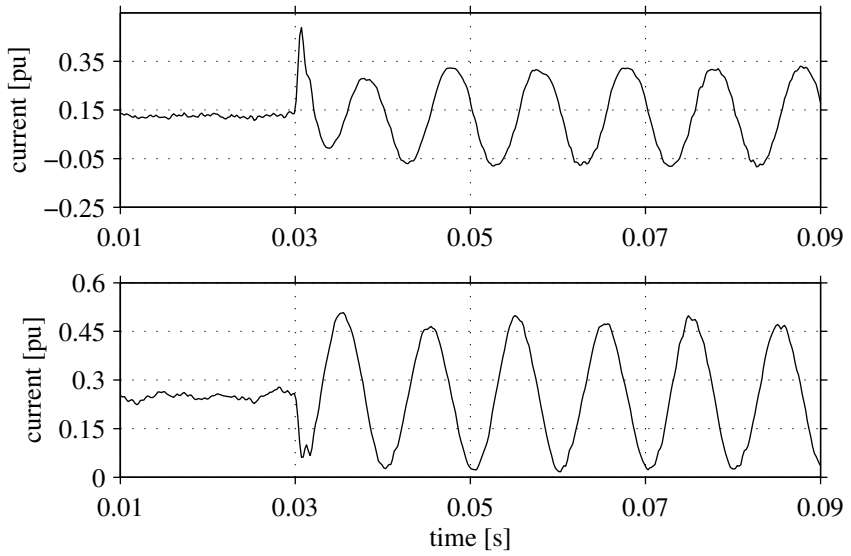


Fig. 4.23 Measured current response to unbalanced voltage dip. VCC1 is used. Top: d-component; bottom: q-component.

4.4 Experimental results using VCC2 and DVCC

Several tests have been carried out in the laboratory for VCC2 and DVCC under different conditions of the grid voltage. However, only experimental results with unbalanced grid voltage will be reported here. The VSC is connected to the weak grid. Parameters for VCC2 are reported in Table 4.2, while controller parameters for the DVCC are reported in Table 3.3.

4.4.1 Unbalanced grid voltages

To compare the performance of the controllers, they have been tested with the same unbalanced supply voltage affected by a steady-state unbalance of 10.9%, shown in Fig.4.24. The sequence components of the grid voltage separated by the SSM and transformed into the corresponding SRFs appear as DC-quantities, as shown in Fig.4.25. The characteristic 100 Hz oscillations denoting unbalance are not present in the dq-current obtained with the VCC2, shown in Fig.4.26 when applying a step change in the active current reference. However, the response is not fast as in Fig.4.10 due to the reduced controller gain. It is possible to notice an oscillation of the current during the positive and negative flanks due to the weak supply voltage, which is not present in the simulated currents displayed in Fig.3.58.

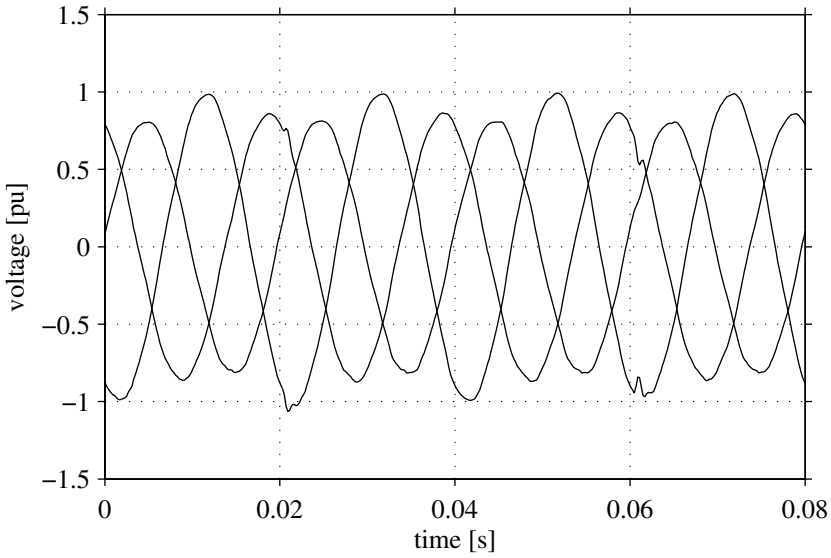


Fig. 4.24 Measured three-phase unbalanced grid voltages.

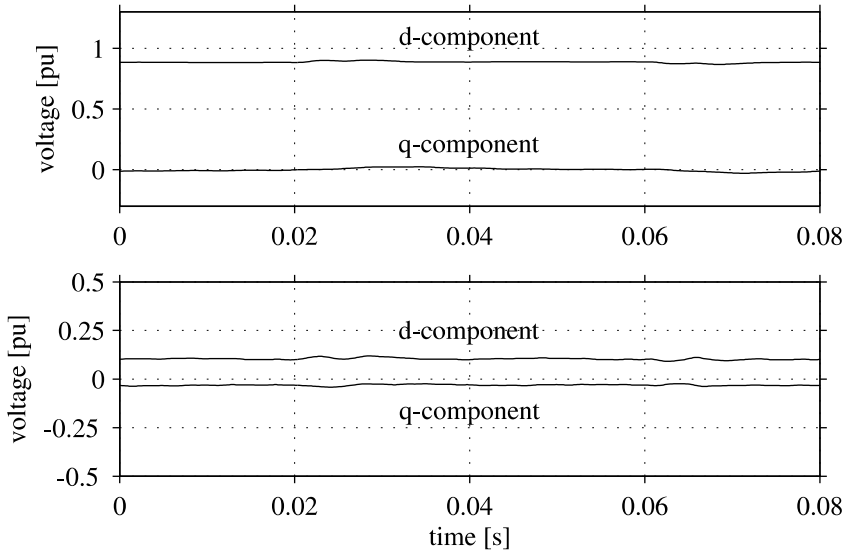


Fig. 4.25 Measured grid voltages in dq-coordinate system. DSC is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

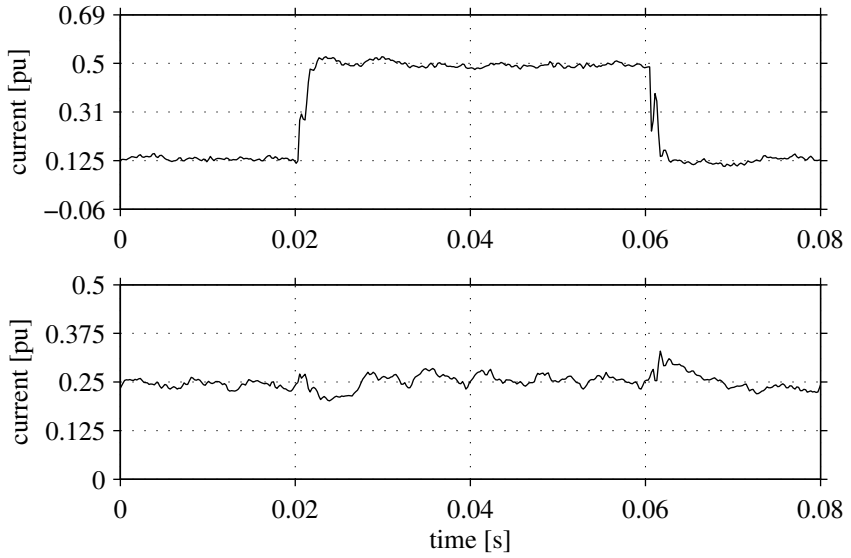


Fig. 4.26 Measured current response to reference active current step. VCC2 and unbalanced grid voltage are used. Top: d-component; bottom: q-component.

The DVCC has been tested under the same unbalanced grid voltage and with the same current step, applied to the positive-sequence d-current, starting from the same operating point. The negative-sequence components of the current have been set to zero. Positive and negative sequence of the measured current are reported in Fig.4.27 and Fig.4.28, respectively. As seen in the simulation results reported in Section 3.5.2, the transient performance of the control system is affected by the DSC in the current controller and the actual current takes 5 ms to respond to the step, in addition to the delay introduced by the current controller itself. Moreover, due to the sequence detection, there is a cross-coupling term between positive- and negative-sequence components both at the beginning and at the end of the step. Moreover, it is possible to observe a ripple in the measured current at the beginning and at the end of the step, not present in the simulated currents in Figs.3.74 and 3.75, which is due to the weak grid. However, due to the separate control of the sequence currents, the current ripple due to harmonics present in the supply has been reduced compared with VCC2.

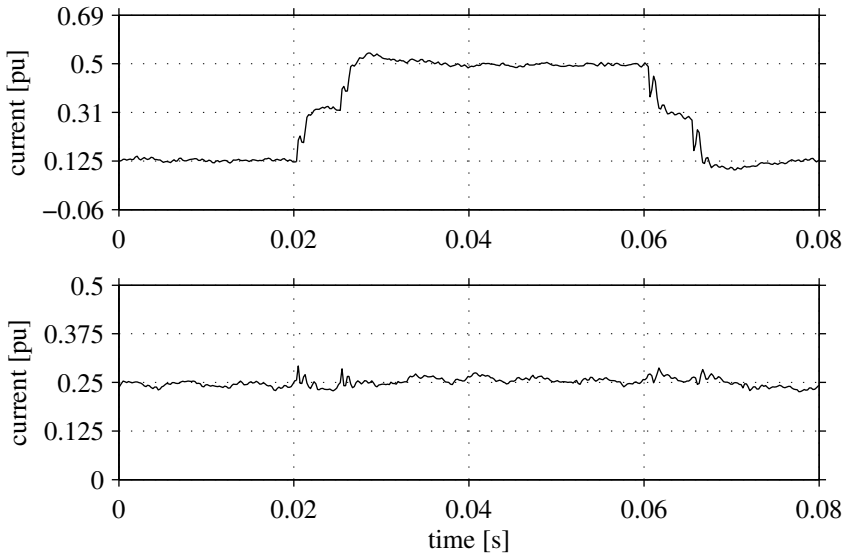


Fig. 4.27 Measured positive-sequence current response to reference active current step. DVCC and unbalanced grid voltage are used. Top: d-component; bottom: q-component.

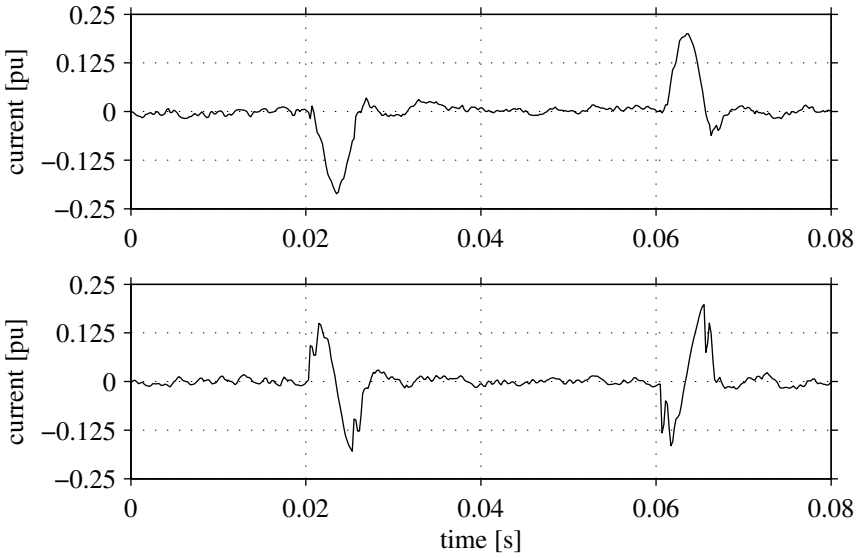


Fig. 4.28 Measured negative-sequence current response to reference active current step. DVCC and unbalanced grid voltage are used. Top: d-component; bottom: q-component.

4.4.2 Voltage dip response

The system has been tested with VCC2 and DVCC also under unbalanced voltage dips. Measured grid voltages during an 85% voltage dip with unbalance of 10.9% are shown in Fig.4.29 (three-phase waveforms) and Fig.4.30 (dq-coordinate system). As shown, during the dip the positive-sequence d-component goes down from 1 pu to 0.85 pu, while the negative-sequence d-component makes a step from 0 pu to 0.1 pu.

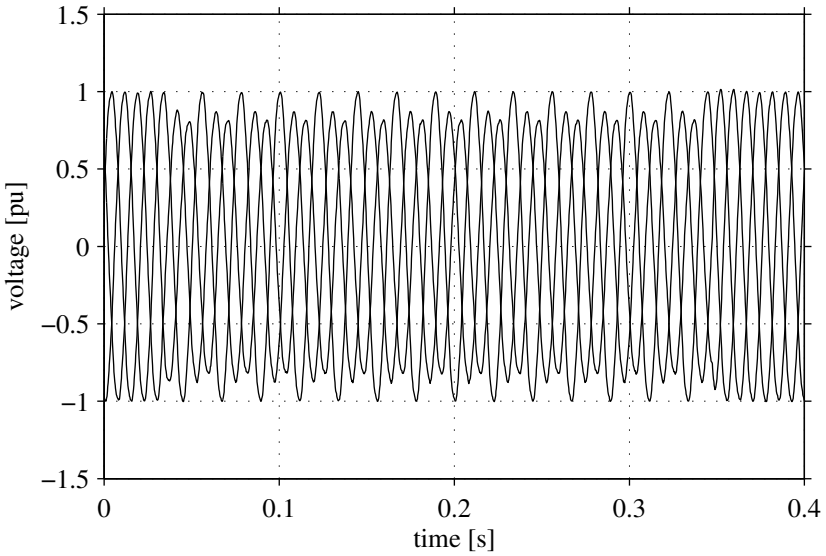


Fig. 4.29 Measured three-phase grid voltages during unbalanced voltage dip.

The operating point is again $i_{\mathrm{rd}} = 0.125$ pu and $i_{\mathrm{rq}} = 0.25$ pu. The control system operates properly and the actual current maintains the pre-fault values also during the dip, as shown by the measured dq-currents in Fig.4.31. The spike in the measured current at the beginning of the dip is 50% smaller compared with the simulation displayed in Fig.3.61, but it lasts for 15 ms, i.e. the control system takes 10 ms more than in the simulation to reach the steady-state. This is due to the capacitors present in the network model and to the time needed for the PLL to track the grid voltage vector, as mentioned in Section 4.3.3.

The positive- and the negative-sequence currents in the positive and negative SRFs for DVCC, respectively, are displayed in Fig.4.32 and Fig.4.33. The controller manages to keep the current to the pre-fault value. However, due to the delay introduced by the DSC, the DVCC presents a more sluggish response compared with VCC2. This confirms the simulation results shown in Section 3.5.2.

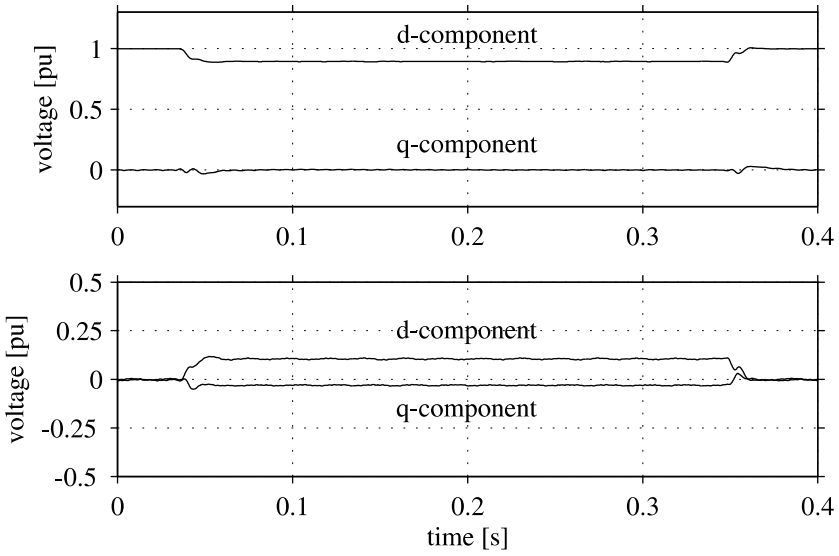


Fig. 4.30 Measured grid voltages in dq-coordinate system during unbalanced voltage dip. DSC is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

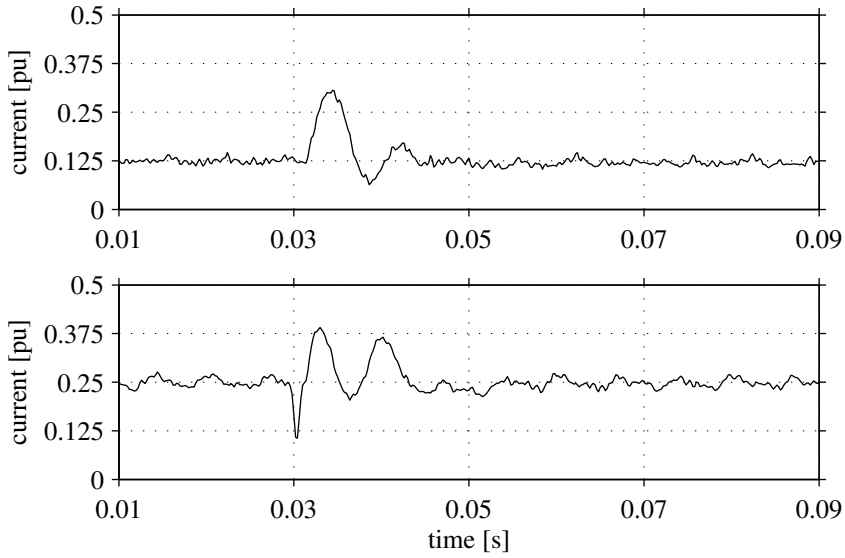


Fig. 4.31 Measured current response to unbalanced voltage dip. VCC2 is used. Top: d-component; bottom: q-component.

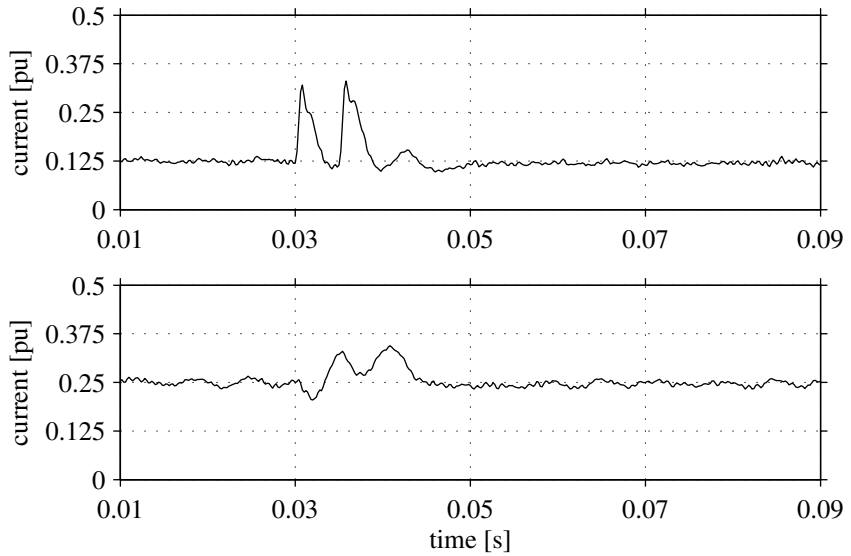


Fig. 4.32 Measured current response to unbalanced voltage dip. Positive sequence components in positive SRF. DVCC is used. Top: d-component; bottom: q-component.

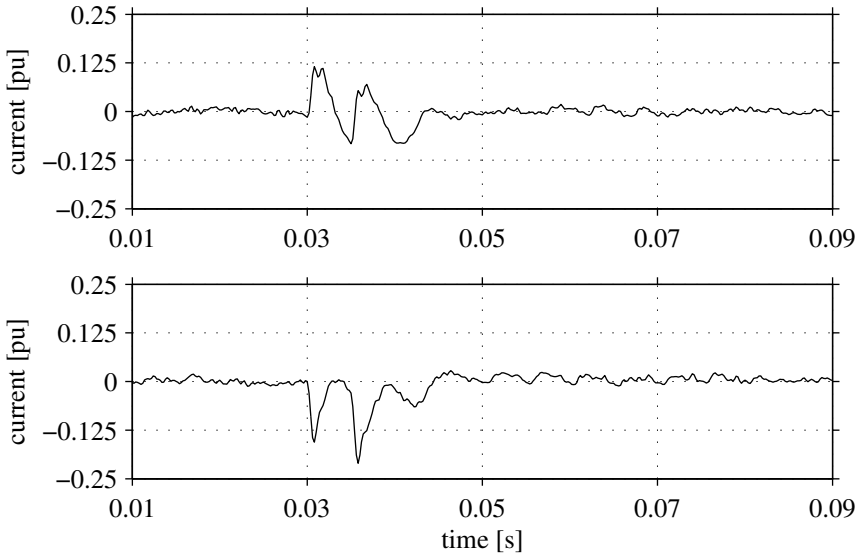


Fig. 4.33 Measured current response to unbalanced voltage dip. Negative sequence components in negative SRF. DVCC is used. Top: d-component; bottom: q-component.

4.5 Conclusions

In this chapter, experimental results for the three current controllers presented in the previous chapter have been shown. An extended description of the laboratory setup and the components used during these experiments has been carried out. With a constant DC-link voltage, steps in the reference currents under balanced and unbalanced conditions of the grid voltage have been applied. Moreover, the transient performance of the three current controllers has been tested by applying balanced and unbalanced voltage dips into the mains. It has been shown that the experimental results confirm the simulations very well. Moreover, it has been shown that, due to the additional damping introduced by the resistance present in an actual system and due to the shunt capacitors of the network model, the current transient experienced for all controllers during the voltage dip is lower compared with the transient experienced during simulations. However, the performance for all controllers under unbalanced grid conditions is lower compared with the simulations. This is due to the necessity in the laboratory setup, when creating unbalance and voltage dip, to connect the VSC to a weak grid and due to the low bandwidth of the PLL. As seen from the simulations, due to the fast response and to the capability of controlling the current under balanced and unbalanced grid conditions, the VCC2 is the best solution when controlling a VSC connected to the grid.

Chapter 5

Control of series-connected VSC

5.1 Introduction

In Chapter 2, the principle and typical configurations of the series-connected VSC for voltage dip mitigation, or SSC, have been reviewed. In this chapter, the derivation of a cascade controller to control the SSC to mitigate voltage dips will be presented. An extended analysis of the control system will be carried out. Three different types of cascade controller will be investigated: the dual vector-controller type 1 (denoted as DVC1), based on VCC1, the dual vector-controller type 2 (denoted as DVC2), based on VCC2 and the dual vector-controller type 3 (denoted as DVC3), based on DVCC. Simulation results of the SSC using the proposed cascade controllers under balanced and unbalanced voltage dips will be presented.

5.2 Layout of the SSC

The three-phase diagram of a grid with SSC is displayed in Fig.5.1. The three-phase voltages of the grid are denoted by $e_{\mathrm{s,a}}(t)$, $e_{\mathrm{s,b}}(t)$ and $e_{\mathrm{s,c}}(t)$, while the grid voltages at the PCC and the grid currents are denoted by $e_{\mathrm{g,a}}(t)$, $e_{\mathrm{g,b}}(t)$, $e_{\mathrm{g,c}}(t)$ and $i_{\mathrm{g,a}}(t)$, $i_{\mathrm{g,b}}(t)$ and $i_{\mathrm{g,c}}(t)$, respectively. The three-phase voltages and currents of the VSC are denoted by $u_{\mathrm{a}}(t)$, $u_{\mathrm{b}}(t)$, $u_{\mathrm{c}}(t)$ and $i_{\mathrm{r,a}}(t)$, $i_{\mathrm{r,b}}(t)$ and $i_{\mathrm{r,c}}(t)$, respectively. The filter capacitor voltages and currents are denoted by $e_{\mathrm{c,a}}(t)$, $e_{\mathrm{c,b}}(t)$, $e_{\mathrm{c,c}}(t)$ and $i_{\mathrm{c,a}}(t)$, $i_{\mathrm{c,b}}(t)$ and $i_{\mathrm{c,c}}(t)$, respectively. The voltages and currents injected by the SSC are denoted by $e_{\mathrm{inj,a}}(t)$, $e_{\mathrm{inj,b}}(t)$, $e_{\mathrm{inj,c}}(t)$ and $i_{\mathrm{inj,a}}(t)$, $i_{\mathrm{inj,b}}(t)$ and $i_{\mathrm{inj,c}}(t)$, respectively. The DC-link voltage is denoted by $u_{\mathrm{dc}}(t)$. Finally, the load voltages are denoted by $e_{\mathrm{l,a}}(t)$, $e_{\mathrm{l,b}}(t)$ and $e_{\mathrm{l,c}}(t)$.

It can be noticed that, as a difference compared with the shunt-connected VSC, in the SSC an LC-filter is mounted at the output of the VSC. This filter is installed in order to remove both current and voltage harmonics, thus reducing the harmonic pollution in the injected voltage. Moreover, this reduces the ripple present in the voltage applied to the windings of the injection transformer, which in turn lengthens the transformer lifetime. As for the L-filter used for the shunt-connected VSC, the inductance smoothes the current output of the VSC, thus reducing

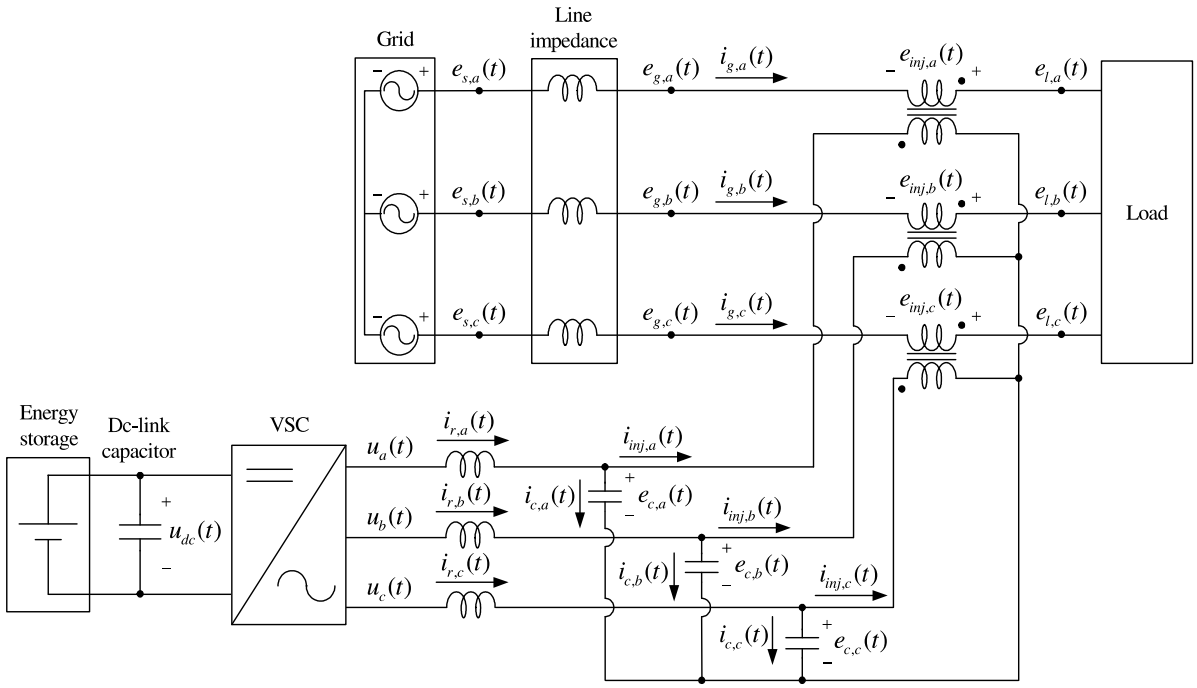


Fig. 5.1 Three-line diagram of grid with SSC.

the current ripple and therefore the stress on the valves of the VSC.

The cut-off frequency of the filter determines the amount of harmonics injected in the grid by the SSC and thereby the harmonic content of the load voltage. This should be considered if the load is particulary sensitive. A basic rule in the design of the filter is that its cut-off frequency should be much lower than the switching frequency of the VSC, thus eliminating the switching ripple in the output voltage. However, the filter should not affect the fundamental component of the injected voltage. Here, the cut-off frequency of the LC-filter has been set to 460 Hz.

The SSC injects the required missing load voltage into the grid through three single-phase transformers. The rated power of the injection transformers is dictated by the load current, which continuously flows on the winding that is connected to the feeder, and by the maximum voltage to be injected. Here, the injection transformers are designed for full-voltage injection.

System parameters reported in Table 5.1 are those of a SSC prototype built in the Power System Laboratory of the Department of Electric Power Engineering at Chalmers University.

5.3 Dual Vector-controller Type 1 (DVC1)

The control system of the SSC is constituted by two closed-loop controllers connected in cascade: an outer loop that controls the voltage across the filter capacitor $\underline{e}_c(t)$ and an inner controller that controls the current through the filter reactor $\underline{i}_r(t)$ [6]. The basic assumption is that the injected voltage is equal to the voltage across the capacitors of the VSC output filter, i.e. the

TABLE 5.1. SYSTEM PARAMETERS FOR SSC.

Grid parameters			
Grid voltage	E	400 V	1 pu
Grid current	I	40 A	1 pu
Grid frequency	f	50 Hz	
Load resistance	R_{l}	10 Ω	1 pu
Load inductance	L_{l}	23.9 mH	0.7508 pu
DC-link voltage	U_{dc}	600 V	1.5 pu
Filter parameters			
Filter resistance	R_{r}	24.8 mΩ	0.0025 pu
Filter inductance	L_{r}	2 mH	0.0628 pu
Filter capacitor	C	60 µF	0.18 pu
Transformer parameters			
Rated power	S_{n}	10 kVA	1.08 pu
Rated voltage	V_{n}	230 V	1 pu
Short-circuit power	P_{cc}	141 W	0.015 pu
Short-circuit voltage	V_{cc}	5.3 V	0.023 pu

injection transformer is considered ideal with a 1:1 turn ratio, therefore

$$e_{\mathrm{inj,a}}(t) = e_{\mathrm{c,a}}(t) \tag{5.1}$$

$$i_{\mathrm{inj,a}}(t) = i_{\mathrm{g,a}}(t) \tag{5.2}$$

and analogously for the other two phases. Under these assumptions, applying the Kirchhoff's current law to the LC-filter, the following differential equations for the three phases can be written

$$i_{\mathrm{r,a}}(t) = i_{\mathrm{c,a}}(t) + i_{\mathrm{g,a}}(t) = C\frac{\mathrm{d}}{\mathrm{d}t}e_{\mathrm{c,a}}(t) + i_{\mathrm{g,a}}(t) \tag{5.3}$$

$$i_{\mathrm{r,b}}(t) = i_{\mathrm{c,b}}(t) + i_{\mathrm{g,b}}(t) = C\frac{\mathrm{d}}{\mathrm{d}t}e_{\mathrm{c,b}}(t) + i_{\mathrm{g,b}}(t) \tag{5.4}$$

$$i_{\mathrm{r,c}}(t) = i_{\mathrm{c,c}}(t) + i_{\mathrm{g,c}}(t) = C\frac{\mathrm{d}}{\mathrm{d}t}e_{\mathrm{c,c}}(t) + i_{\mathrm{g,c}}(t) \tag{5.5}$$

By applying Clarke's transformation, Eqs.(5.3) to (5.5) can be written in the $\alpha\beta$-coordinate system as

$$\frac{\mathrm{d}}{\mathrm{d}t}\underline{e}_{\mathrm{c}}^{(\alpha\beta)}(t) = \frac{1}{C}\underline{i}_{\mathrm{r}}^{(\alpha\beta)}(t) - \frac{1}{C}\underline{i}_{\mathrm{g}}^{(\alpha\beta)}(t) \tag{5.6}$$

which, by using $\alpha\beta$- to dq-transformation with a PLL synchronized with the grid voltage vector, becomes

$$\frac{\mathrm{d}}{\mathrm{d}t}\underline{e}_{\mathrm{c}}^{(dq)}(t) = \frac{1}{C}\underline{i}_{\mathrm{r}}^{(dq)}(t) - \frac{1}{C}\underline{i}_{\mathrm{g}}^{(dq)}(t) - \mathrm{j}\omega\underline{e}_{\mathrm{c}}^{(dq)}(t) \tag{5.7}$$

5.3.1 Voltage controller

To derive the voltage controller to be implemented in a digital controller, it is necessary to discretize Eq.(5.7). This is done by integrating the equation over one sample period T_s and then dividing by T_s, thus obtaining

$$\begin{aligned}\frac{1}{T_\mathrm{s}}(\underline{e}_\mathrm{c}^{(dq)}(k+1)-\underline{e}_\mathrm{c}^{(dq)}(k)) = \frac{1}{C}\underline{i}_\mathrm{r}^{(dq)}(k,k+1)-\frac{1}{C}\underline{i}_\mathrm{g}^{(dq)}(k,k+1)+\\ -\mathrm{j}\omega\underline{e}_\mathrm{c}^{(dq)}(k,k+1)\end{aligned} \tag{5.8}$$

where $\underline{e}_\mathrm{c}^{(dq)}(k,k+1)$ denotes the average value of $\underline{e}_\mathrm{c}^{(dq)}(t)$ between sample k and sample $k+1$.

If a proportional controller with deadbeat gain is used, the controller will track the reference voltage with one sample delay, yielding

$$\underline{e}_\mathrm{c}^{(dq)}(k+1)=\underline{e}_\mathrm{c}^{(dq)*}(k) \tag{5.9}$$

The reference capacitor voltage is the voltage to be injected in the grid to restore the load voltage to the desired value

$$\underline{e}_\mathrm{c}^{(dq)}(k)=\underline{e}_\mathrm{l}^{(dq)*}(k)-\underline{e}_\mathrm{g}^{(dq)}(k) \tag{5.10}$$

where $\underline{e}_\mathrm{l}^{(dq)*}$ denotes the load reference voltage in the dq-coordinate system.

The following assumptions are made in order to formulate the voltage controller:

- The grid current components change slowly and are considered constant over one sample period

$$\underline{i}_\mathrm{g}^{(dq)}(k,k+1)=\underline{i}_\mathrm{g}^{(dq)}(k) \tag{5.11}$$

- The filter capacitor voltage changes linearly during one sample period

$$\underline{e}_\mathrm{c}^{(dq)}(k,k+1)=\frac{1}{2}\left[\ \underline{e}_\mathrm{c}^{(dq)}(k)+\underline{e}_\mathrm{c}^{(dq)}(k+1)\ \right]=\frac{1}{2}\left[\ \underline{e}_\mathrm{c}^{(dq)}(k)+\underline{e}_\mathrm{c}^{(dq)*}(k)\ \right] \tag{5.12}$$

- The average value of the filter current over one sample period is equal to the reference

$$\underline{i}_\mathrm{r}^{(dq)}(k,k+1)=\underline{i}_\mathrm{r}^{(dq)*}(k) \tag{5.13}$$

The proportional voltage controller can now be formulated as

$$\begin{aligned}\underline{i}_\mathrm{r}^{(dq)*}(k)=\underline{i}_\mathrm{g}^{(dq)}(k)+\mathrm{j}\frac{\omega C}{2}(\underline{e}_\mathrm{c}^{(dq)*}(k)+\underline{e}_\mathrm{c}^{(dq)}(k))+\\ +\frac{C}{T_\mathrm{s}}(\underline{e}_\mathrm{c}^{(dq)*}(k)-\underline{e}_\mathrm{c}^{(dq)}(k))\end{aligned} \tag{5.14}$$

which gives for the d- and the q-component of the reference current

$$\begin{aligned} i^*_{\mathrm{r}d}(k) &= i_{\mathrm{g}d}(k) - \frac{\omega C}{2}(e^*_{\mathrm{c}q}(k) + e_{\mathrm{c}q}(k)) + \frac{C}{T_\mathrm{s}}(e^*_{\mathrm{c}d}(k) - e_{\mathrm{c}d}(k)) = \\ &= i_{\mathrm{ff}d}(k) + k_{\mathrm{p,vc}}(e^*_{\mathrm{c}d}(k) - e_{\mathrm{c}d}(k)) \end{aligned} \tag{5.15}$$

$$\begin{aligned} i^*_{\mathrm{r}q}(k) &= i_{\mathrm{g}q}(k) + \frac{\omega C}{2}(e^*_{\mathrm{c}d}(k) + e_{\mathrm{c}d}(k)) + \frac{C}{T_\mathrm{s}}(e^*_{\mathrm{c}q}(k) - e_{\mathrm{c}q}(k)) = \\ &= i_{\mathrm{ff}q}(k) + k_{\mathrm{p,vc}}(e^*_{\mathrm{c}q}(k) - e_{\mathrm{c}q}(k)) \end{aligned} \tag{5.16}$$

where $i_{\mathrm{ff}d}(k)$ and $i_{\mathrm{ff}q}(k)$ are the feed-forward terms for the d- and q-component, respectively, and $k_{\mathrm{p,vc}}$ is the proportional gain of the voltage controller to obtain deadbeat and is equal to

$$k_{\mathrm{p,vc}} = \frac{C}{T_\mathrm{s}} \tag{5.17}$$

In order to remove static errors due to non linearities, such as noise in the measurements and non-ideal components, an integral part has to be introduced in the control system. The PI-controller can be formulated as

$$i^*_{\mathrm{r}d}(k) = i_{\mathrm{ff}d}(k) + k_{\mathrm{p,vc}}(e^*_{\mathrm{c}d}(k) - e_{\mathrm{c}d}(k)) + \Delta i_{\mathrm{i}d}(k) \tag{5.18}$$

$$i^*_{\mathrm{r}q}(k) = i_{\mathrm{ff}q}(k) + k_{\mathrm{p,vc}}(e^*_{\mathrm{c}q}(k) - e_{\mathrm{c}q}(k)) + \Delta i_{\mathrm{i}q}(k) \tag{5.19}$$

where $\Delta i_{\mathrm{i}d}(k)$ and $\Delta i_{\mathrm{i}q}(k)$ are the integral terms for the d- and q-components, respectively, which can be written as

$$\Delta i_{\mathrm{i}d}(k+1) = \Delta i_{\mathrm{i}d}(k) + k_{\mathrm{i,vc}}(e^*_{\mathrm{c}d}(k) - e_{\mathrm{c}d}(k)) \tag{5.20}$$

$$\Delta i_{\mathrm{i}q}(k+1) = \Delta i_{\mathrm{i}q}(k) + k_{\mathrm{i,vc}}(e^*_{\mathrm{c}q}(k) - e_{\mathrm{c}q}(k)) \tag{5.21}$$

where the integral gain of the voltage controller $k_{\mathrm{i,vc}}$ can be written as

$$k_{\mathrm{i,vc}} = k_{\mathrm{p,vc}}\frac{T_\mathrm{s}}{T_{\mathrm{i,vc}}} \tag{5.22}$$

and $T_{\mathrm{i,vc}}$ is the integration time constant.

The output of the voltage controller is the reference current $\underline{i}^{(dq)*}_\mathrm{r}$, which will be the input to the current controller in order to control the current through the filter reactor $\underline{i}^{(dq)}_\mathrm{r}$. The current controller used is VCC1, described in Section 3.2. Figure 5.2 shows the block scheme of the implemented cascade controller, constituted by the described voltage controller (denoted in the figure by VC) in series with VCC1. The algorithm of the implemented control system can be summarized as:

1. Measure and sample the grid voltages, grid currents, filter currents and capacitor voltages with sampling frequency f_s;

2. Transform all three-phase quantities to the $\alpha\beta$-coordinate system and then to the rotating dq-coordinate system, using the transformation angle θ, obtained from the PLL;

3. Calculation of the reference filter current $\underline{i}_r^{(dq)*}(k)$ using the VC block;

4. Calculation of the reference voltage $\underline{u}^{(dq)*}(k)$ using the VCC1 block;

5. Convert the reference voltages from the dq-coordinate system into three-phase voltages using the transformation angle $\theta(k) + \Delta\theta$, where $\Delta\theta = 3/2\ \omega T_\mathrm{s}$, as explained in Section 3.2.3;

6. Calculate the duty-cycles in the PWM block and send the switching signals to the VSC valves.

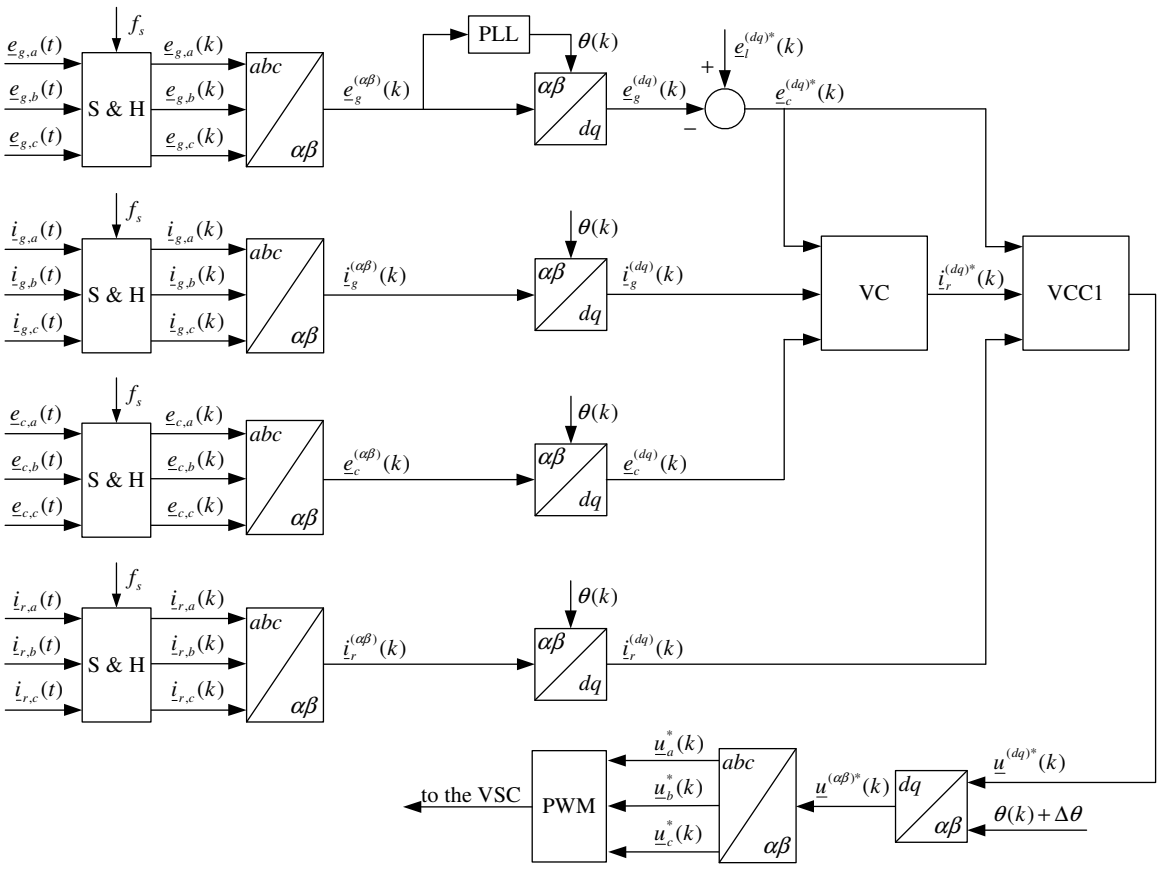


Fig. 5.2 Block-scheme of implemented cascade controller for voltage dip mitigation using SSC.

5.3.2 Transformer saturation

As shown in Fig.5.1, the SSC injects a voltage in series with the main supply through an injection transformer. When a voltage dip is detected, the SSC injects a voltage into the mains

by applying a voltage on the secondary side of the injection transformer. The flux Ψ in the transformer during dip mitigation can be expressed as

$$\Psi = \int_0^t E_{\text{inj}} \cos(\omega\tau + \varphi) d\tau = \frac{E_{\text{inj}}}{\omega}(\sin(\omega t + \varphi) - \sin(\varphi)) \tag{5.23}$$

where E_{inj} denotes the RMS value of the injected voltage and φ is the initial phase of the injected voltage. The voltage dip occurs at $t = 0$.

As shown in Eq.(5.23), the flux in the injection transformer is constituted by an AC term that varies with the grid frequency and a DC term that depends on the angle of the grid voltage at the beginning of the dip. If the initial phase of the injected voltage φ is equal to $\pi/2 + n\pi$, with n any integer, the transformer flux can reach up to twice the steady-state value. Therefore, if the transformer is not properly designed, saturation can occur and the magnetizing current can become very large. As a result, the VSC can be damaged due to overcurrent. To avoid saturation under all conditions, the transformer has to be sized to handle two times the normal steady-state flux requirement at maximum RMS injection voltage without saturating [35]. The drawback of this solution is that the increased size of the transformer will lead to a significant increase of the cost of the device.

Transformer-less SSC has been suggested as an alternative [31], however there are still a number of problems related to this system, such as absence of galvanic insulation between the grid and the VSC, protection of the VSC against fault currents to ground, necessity of designing the system for medium voltage level.

A possible countermeasure is to limit the $\mathrm{d}v/\mathrm{d}t$ applied to the windings of the transformer during the first instants of the injection. If the required voltage variation is such that it would saturate the transformer, the controller should act by limiting the rate of change of the capacitor voltage $\underline{e}_{\text{c}}^{(dq)}$ over one sample. Since the voltage across the capacitor is controlled through the VSC output current $\underline{i}_{\text{r}}^{(dq)}$, this can be achieved by limiting the variation of the reference current $\underline{i}_{\text{r}}^{(dq)*}$ at the VC output to keep the transformer away from saturation. This will of course affect the performance of the SSC in the first instants of the mitigation, but will contain the cost of the device.

If the voltage variation during voltage dip mitigation exceeds the saturation limits of the transformer, the reference current output of the VC will be limited by a current limiter. To avoid integrator windup in the VC, it is necessary to adjust the voltage error by using back-calculation, as explained in Section 3.2.4. The back-calculated error $\underline{e}_{\text{ec}}^{(dq)}$ is given by

$$\underline{e}_{\text{ec}}^{(dq)}(k) = \frac{1}{k_{\text{p,vc}}}[\underline{i}_{\text{r,lim}}^{(dq)*}(k) - \underline{i}_{\text{ff}}^{(dq)}(k) - \Delta\underline{i}_{\text{i}}^{(dq)}(k)] \tag{5.24}$$

where $\underline{i}_{\text{r,lim}}^{(dq)*}$ is the limited reference current vector, $\underline{i}_{\text{ff}}^{(dq)}$ is the feed-forward current term and $\Delta\underline{i}_{\text{i}}^{(dq)}$ is integral term of the VC.

Figure 5.3 shows the block scheme of the modified cascade controller (here called dual vector-controller type 1, DVC1). The block "current limiter" is added to avoid the risk of saturation of

the core of the transformer, as explained above. Moreover, this block sets a maximum limit to the reference current for the VCC1, and therefore the current through the filter inductor. This limit depends on the size of the injection transformer and on its capability to be overloaded. Here, the maximum current allowed through the filter inductor is set to 50 A (1.25 pu).

The saturation signal "sat", also shown in Fig.5.3, is instead added to stop the integral term of the VC if the demanded voltage exceeds the boundary of the hexagon and therefore cannot be generated by the VSC. VSC saturation has been explained in Section 3.2.4.

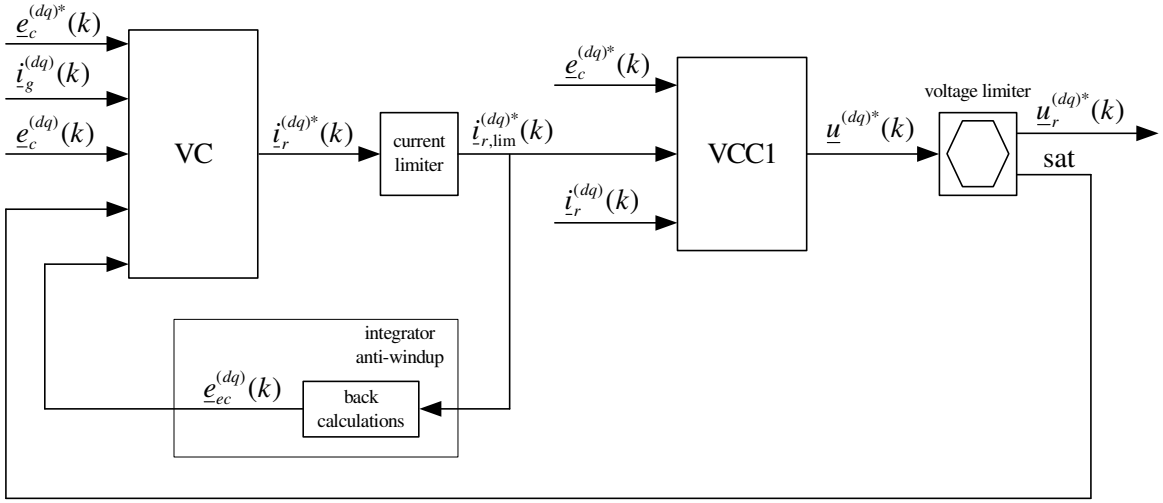


Fig. 5.3 Block-scheme of improved cascade controller, denoted by DVC1.

5.3.3 Stability analysis

In this section, the stability analysis of the entire system using DVC1 will be presented. The dynamic performance of the two closed-loop systems in both cases of accurate and inaccurate knowledge of the filter parameters will be investigated. System parameters are displayed in Table 5.1. A block diagram of the closed-loop system is depicted in Fig.5.4, where the VSC has been considered as an ideal amplifier. Note that the load dynamics are included in the scheme. An RL-load has been considered. Thus, the load current will change when the load voltage changes.

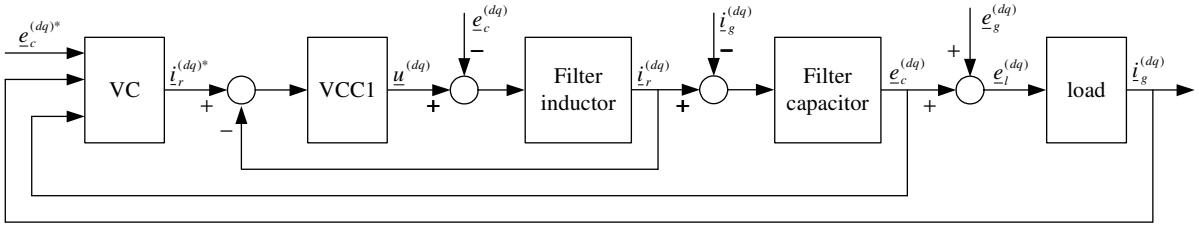


Fig. 5.4 Block diagram of closed-loop system constituted by DVC1, filter and load.

Accurate knowledge of filter parameters

In case of accurate knowledge of the filter parameters, both the equations of the voltage controller and of the current controller contain the exact values of the parameters. In this case, it is of interest to investigate the interaction between the two controllers. When a cascade controller is used, it is important to carefully select the bandwidth of the two controllers in order to ensure the stability of the entire system. Figure 5.5 shows the closed-loop poles placement of the SSC with DVC1 for different values of the voltage controller gain (denoted as α_{vc} and expressed in pu of the deadbeat gain of the voltage controller). The inner current controller is set to deadbeat. When increasing the gain of the outer controller, the poles move out from the real axis. It can be observed that, for α_{vc} equal to 0.1 and 0.3, the closed-loop system is stable, while for α_{vc} equal to 1 (i.e. both voltage controller and current controller at deadbeat) the closed-loop system is unstable. Stability of the system is achieved when the outer controller gain α_{vc} is set to 0.57 of deadbeat.

From this analysis it is possible to understand one of the basic rules for selecting the parameters of a cascade controller: the inner loop should be much faster than the outer one. Typically, the ratio between the bandwidth of the inner controller and that of the outer controller should be at least 5 [4].

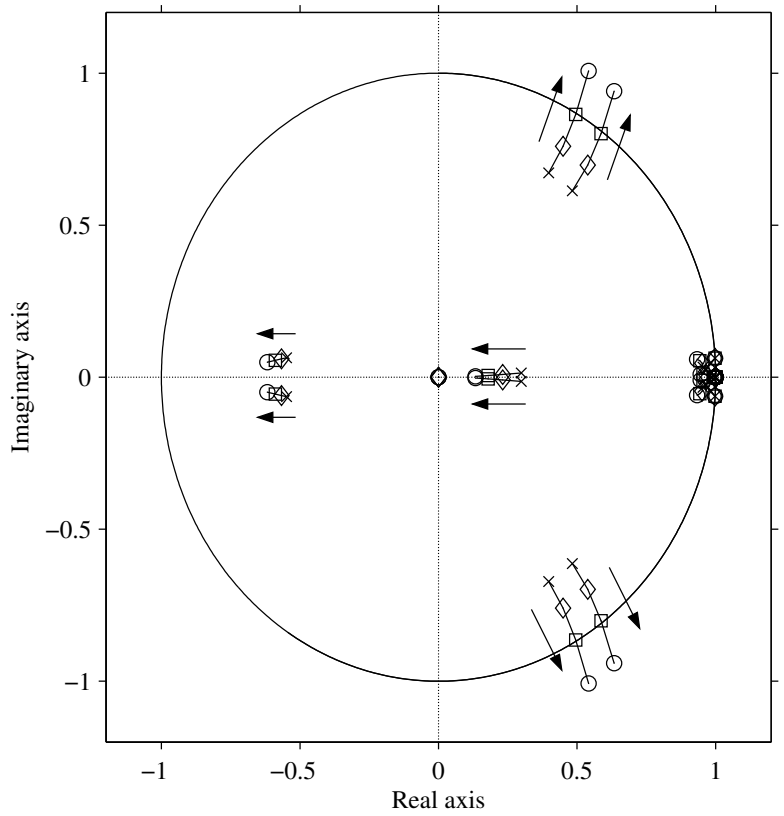


Fig. 5.5 Pole placement for accurate knowledge of filter parameters when varying voltage controller gain α_{vc}. Marker "$\times$" denotes $\alpha_{\text{vc}} = 10\%$ deadbeat, marker "$\diamond$" denotes $\alpha_{\text{vc}} = 30\%$ deadbeat, marker "$\square$" denotes $\alpha_{\text{vc}} = 57\%$ deadbeat, marker "$\circ$" denotes $\alpha_{\text{vc}} =$ deadbeat.

Frequency analysis

Figure 5.6 shows the Bode diagram of the transfer function from the d-component of the reference capacitor voltage Δe^*_{cd} to the d-component of the actual capacitor voltage Δe_{cd} for different values of the gain of the voltage controller α_{vc}. As shown, when α_{vc} is set to 0.3, the gain is constant and equal to 0 dB up to 800 Hz. This means that the controller will be able to track the reference value up to 800 Hz. For higher frequencies, the gain decreases and the phase shift increases. For α_{vc}=0.57 the gain is bigger compared with the previous case and presents two peaks at 750 Hz and 850 Hz (12 dB). The phase shift presents a variation at the same frequencies. Finally, if α_{vc}=1, the gain is equal to 0 dB up to 400 Hz, then it slowly increases with a peak at 800 Hz of 10 dB. The same characteristic can be obtained for the transfer function from the q-component of the reference voltage Δe^*_{cq} to the q-component of the actual capacitor voltage Δe_{cq} (not shown).

The frequency response of the transfer function from the reference d-voltage of the capacitor Δe^*_{cd} to the q-component of the actual capacitor voltage Δe_{cq} is displayed in Fig.5.7. As shown, for α_{vc}=0.3 the gain of the cross-coupling term is very small and can be neglected. For higher values of α_{vc}, the gain of the cross-coupling term increases with the frequency with a peak at 800 Hz (18 dB for α_{vc}=0.57 and 7 dB for α_{vc}=1, respectively).

As seen for the shunt-connected VSC, the harmonic content of the grid voltage might affect the capacitor voltage. Figures 5.8 and 5.9 show the Bode diagram of the transfer function from the d-component of the grid voltage Δe_{gd} to the d- and q-component of the capacitor voltage, respectively, for different values of α_{vc}. As shown, in all three cases both the direct and the cross-coupling term present a small gain and can be neglected. This is surprising, since it means that the control system results unsensitive to the harmonic content of the grid voltage. Here, the gain of the outer loop has been set to 30% of deadbeat, which represents a compromise between the speed of response of the control system and its damping.

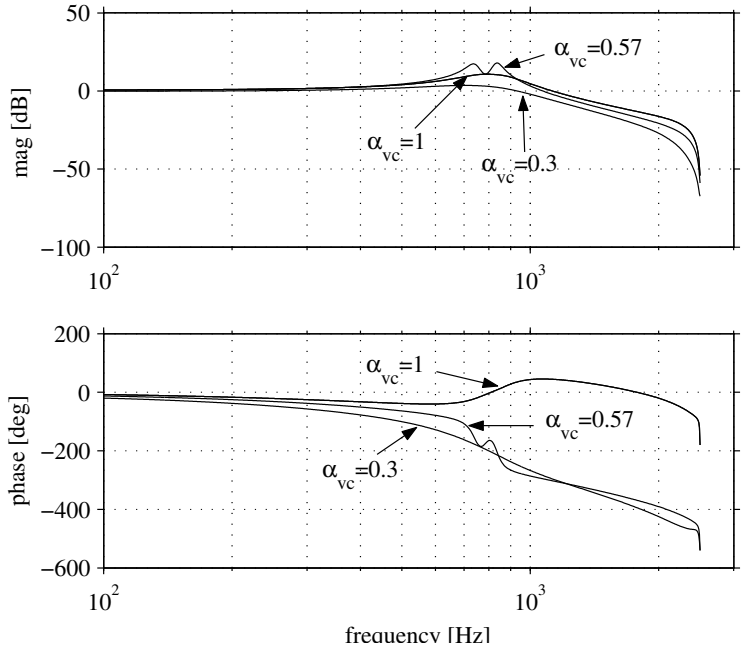


Fig. 5.6 Bode diagram from reference d-component of capacitor voltage Δe^*_{cd} to d-component of capacitor voltage Δe_{cd} for accurate knowledge of filter parameters when varying voltage controller gain α_{vc} (in pu of deadbeat gain).

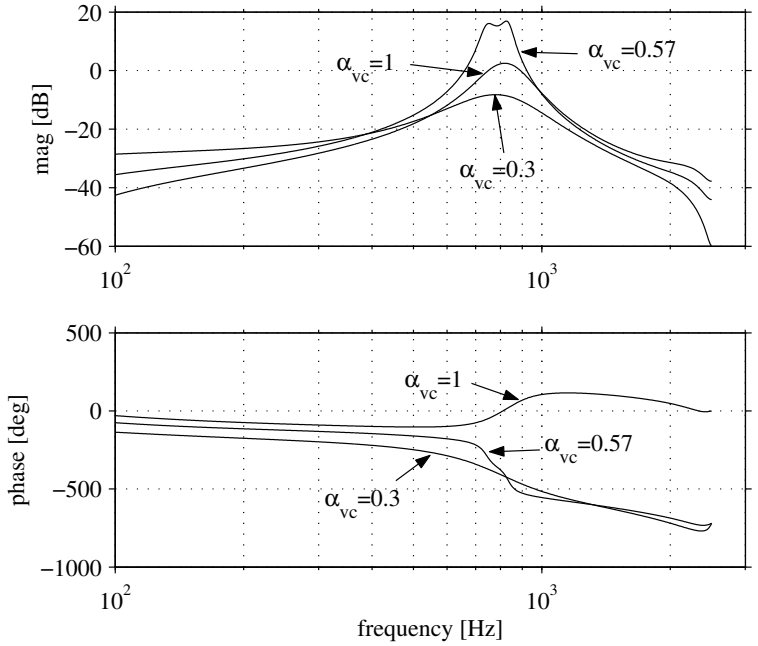


Fig. 5.7 Bode diagram from reference d-component of capacitor voltage Δe^*_{cd} to q-component of capacitor voltage Δe_{cq} for accurate knowledge of filter parameters when varying voltage controller gain α_{vc} (in pu of deadbeat gain).

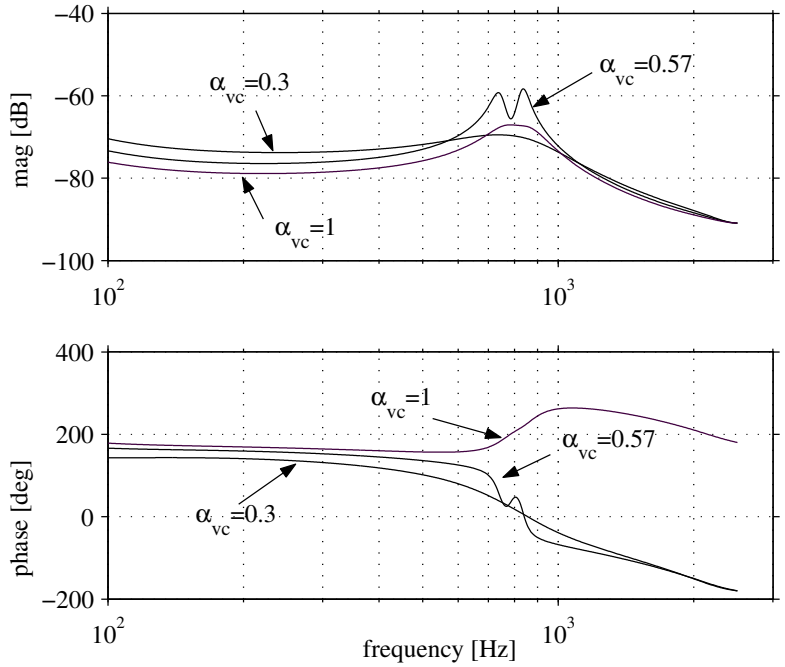


Fig. 5.8 Bode diagram from d-component of grid voltage Δe_{gd} to d-component of capacitor voltage Δe_{cd} for accurate knowledge of filter parameters when varying voltage controller gain α_{vc} (in pu of deadbeat gain).

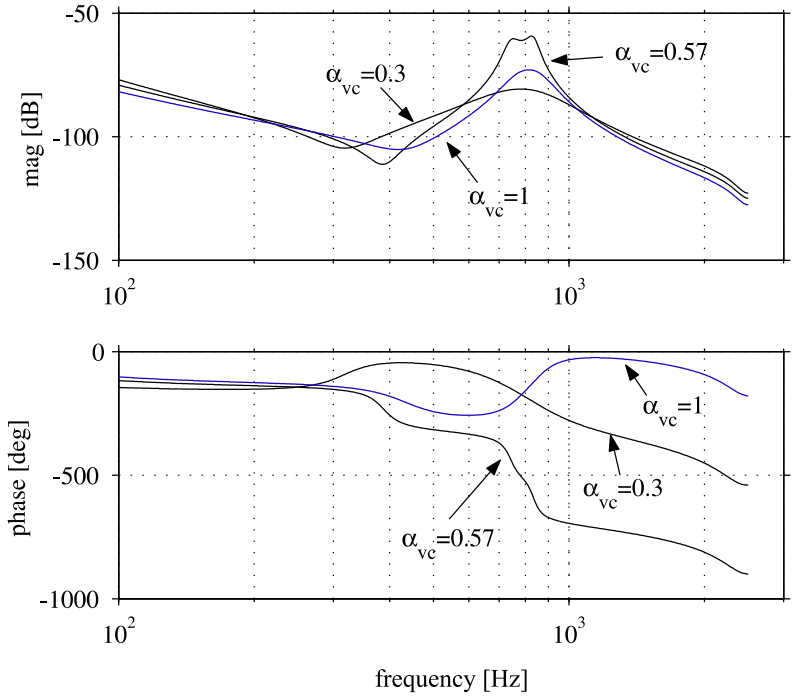


Fig. 5.9 Bode diagram from d-component of grid voltage Δe_{gd} to q-component of capacitor voltage Δe_{cq} for accurate knowledge of filter parameters when varying voltage controller gain α_{vc} (in pu of deadbeat gain).

Inaccurate knowledge of filter parameters

When the filter parameters are not known with accuracy, estimated values for the filter reactor ($\widehat{R}_\mathrm{r}$ and $\widehat{L}_\mathrm{r}$) and filter capacitor ($\widehat{C}$) are used in the equations of the current controller and of the voltage controller. From the results obtained in the previous analysis, α_vc has been set to 30% of deadbeat.

The reactor resistance is usually negligible compared with its reactance, therefore the response of the system can be considered insensitive to its variation. Figure 5.10 shows the closed-loop poles of the SSC with DVC1 when the estimated filter inductance $\widehat{L}_\mathrm{r}$ varies from 60% to 180% of the actual filter inductance L_r. The current controller is using deadbeat gain and the gain of the voltage controller is 30% of deadbeat gain. From this figure it is possible to observe that an underestimation of the filter inductance $\widehat{L}_\mathrm{r}$ results in a well damped system. When increasing $\widehat{L}_\mathrm{r}$, the poles move far from the real axis and for $\widehat{L}_\mathrm{r}$ equal to 180% of L_r the system gets unstable. Therefore, similarly to what found in Section 3.2.5, it can be concluded that it is better to underestimate the filter inductance from the stability point of view.

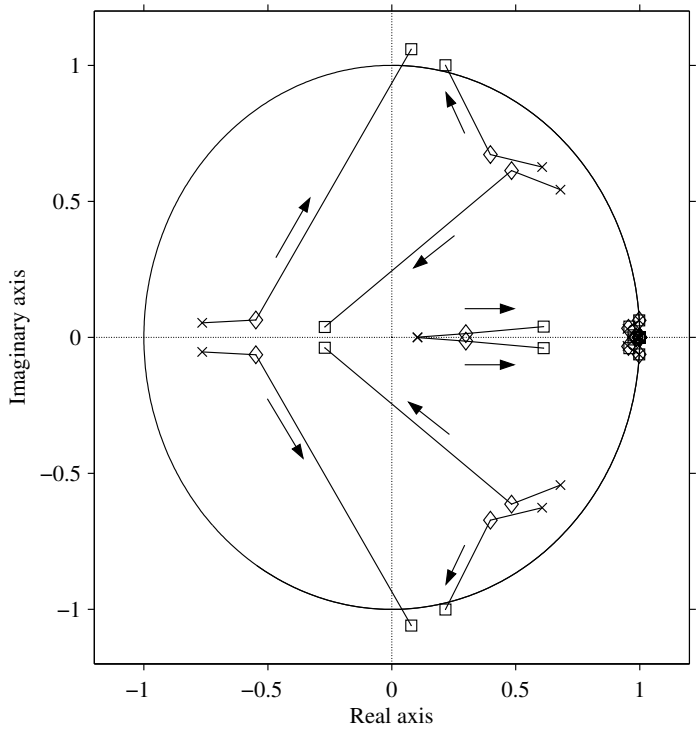


Fig. 5.10 Pole placement for inaccurate knowledge of filter parameters for $\alpha_\mathrm{vc} = 0.3$ when varying estimated filter inductance. Marker "×" denotes $\widehat{L}_\mathrm{r} = 0.6L_\mathrm{r}$, marker "◇" denotes $\widehat{L}_\mathrm{r} = L_\mathrm{r}$, marker "□"denotes $\widehat{L}_\mathrm{r} = 1.8L_\mathrm{r}$.

Figure 5.11 shows the closed-loop poles of the control system when the estimated filter capacitor $\widehat{C}$ varies from 60% to 180% of the actual filter capacitor C. As shown, the poles slowly move far from the real axis when increasing $\widehat{C}$, but always remain inside the unit circle. Therefore, it can be concluded that, when the filter capacitor is underestimated, the control system results

more damped than in case of overestimation, but in general it is less sensitive to variations of the filter capacitor C compared with variations of the filter inductor L_{r}.

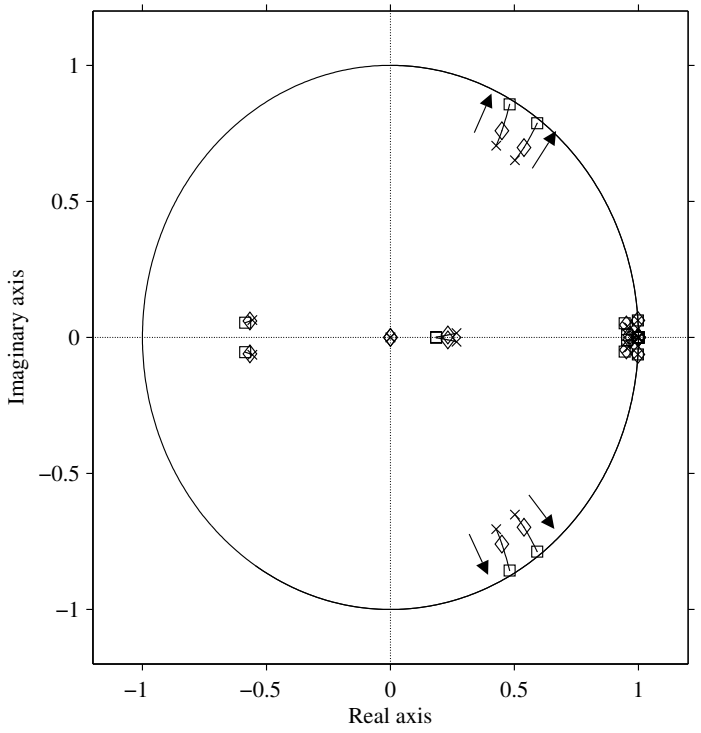


Fig. 5.11 Pole placement for inaccurate knowledge of filter parameters for $\alpha_{\mathrm{vc}} = 0.3$ at variation of estimated filter capacitor. Marker "$\times$" denotes $\widehat{C} = 0.6C$, marker "$\diamond$" denotes $\widehat{C} = C$, marker "$\square$"denotes $\widehat{C} = 1.8C$.

Frequency analysis

From the previous analysis, it is concluded that the system is insensitive to variations of R_{r} and to normal variations of C. Therefore, only the frequency analysis of the system when varying L_{r} will be carried out.

Figures 5.12 and 5.13 show the Bode diagram of the transfer function from Δe^*_{cd} to Δe_{cd} and from Δe^*_{cd} to Δe_{cq}, respectively. The ratio between estimated and actual filter inductance $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}}$ is equal to 1 (denoted as $L_{1.0}$), 0.6 (denoted as $L_{0.6}$) and 1.8 (denoted as $L_{1.8}$). In Fig.5.12, the gain fluctuation is $\pm$6 dB when going from $L_{0.6}$ to $L_{1.8}$. In Fig.5.13 the gain is highest for $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}}$=0.6 for frequencies lower than 750 Hz, for $\widehat{L}_{\mathrm{r}}/L_{\mathrm{r}}$=1.8 otherwise.

The controller results again insensitive to the harmonic content of the grid voltage, as indicated by the gain of the transfer function from Δe_{gd} to Δe_{cd} and from Δe_{gd} to Δe_{cq} displayed in Fig.5.14 and 5.15, respectively, which is always lower that 1.

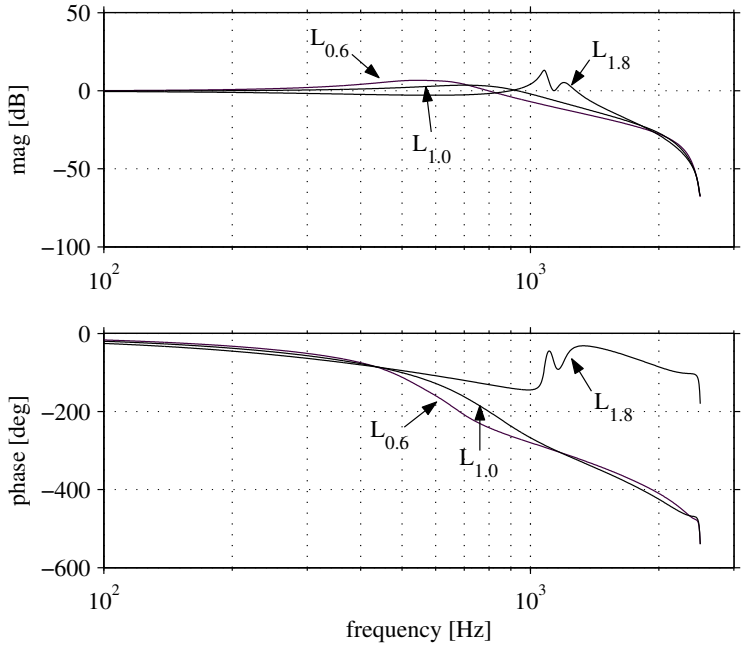


Fig. 5.12 Bode diagram from reference d-component of capacitor voltage Δe^*_{cd} to d-component of capacitor voltage Δe_{cd} for inaccurate knowledge of filter inductance L_r. $\alpha_\mathrm{vc} = 30\%$ deadbeat.

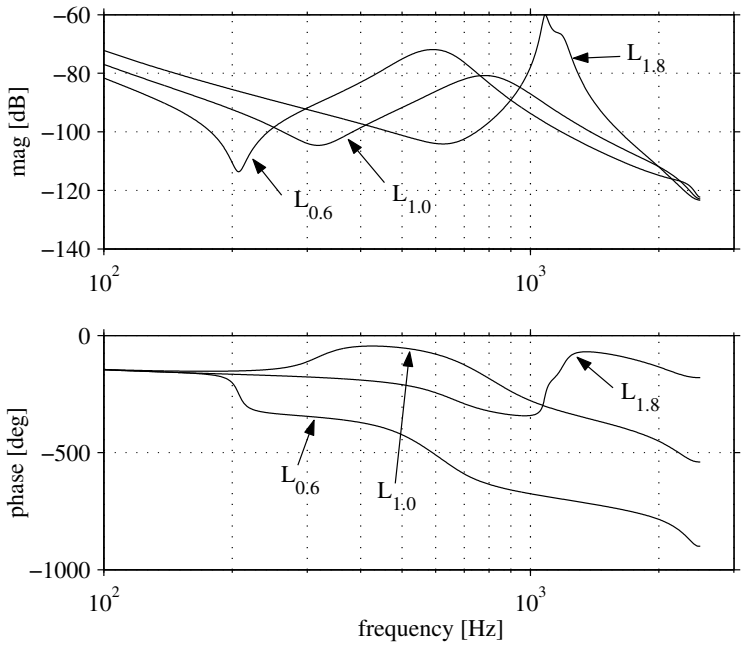


Fig. 5.15 Bode diagram from d-component of grid voltage Δe_{gd} to q-component of capacitor voltage Δe_{cq} for inaccurate knowledge of filter inductance L_r. $\alpha_\mathrm{vc} = 30\%$ deadbeat.

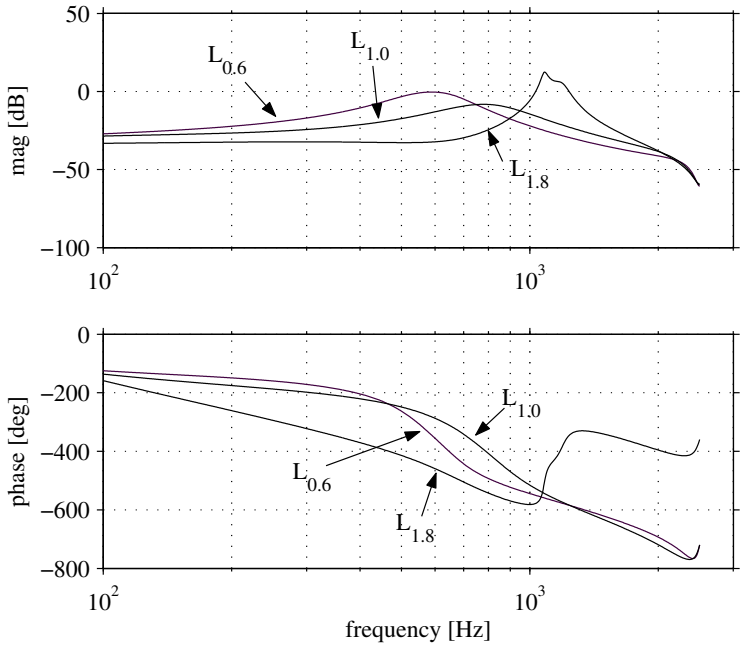


Fig. 5.13 Bode diagram from reference d-component of capacitor voltage Δe^*_{cd} to q-component of capacitor voltage Δe_{cq} for inaccurate knowledge of filter inductance L_r. $\alpha_{vc} = 30\%$ deadbeat.

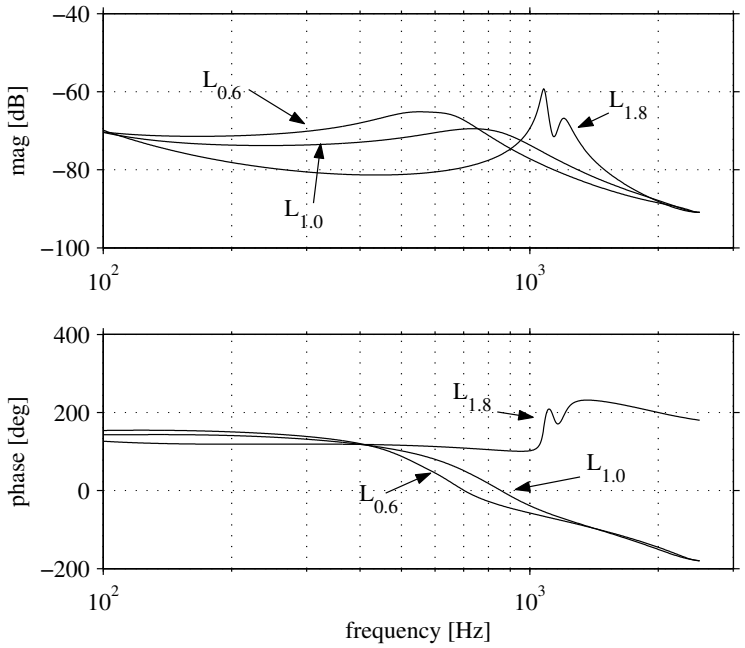


Fig. 5.14 Bode diagram from d-component of grid voltage Δe_{gd} to d-component of capacitor voltage Δe_{cd} for inaccurate knowledge of filter inductance L_r. $\alpha_{vc} = 30\%$ deadbeat.

5.3.4 Simulation results using DVC1

Simulation results obtained using PSCAD/EMTDC of the SSC using DVC1 will be presented in this section. The step response of the DVC1 during voltage dip mitigation has been tested under symmetrical and unsymmetrical voltage dips. System parameters are shown in Table 5.1. Controller parameters for the DVC1 are displayed in Table 5.2.

TABLE 5.2. CONTROLLER PARAMETERS FOR DVC1.

Sampling frequency	f_s = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Current controller parameters			
Proportional gain	$k_{p,cc}$	10.01	(deadbeat)
Integrator gain	$k_{i,cc}$	0	
Observer gain	k_{psp}	0.1	
Voltage controller parameters			
Proportional gain	$k_{p,vc}$	0.09	(30% deadbeat)
Integrator time constant	$T_{i,vc}$	0.03	

Balanced voltage dips

The three-phase grid voltages at the PCC are displayed in Fig.5.16. At $t = 0.03$ s a balanced voltage dip occurs and the grid voltage decreases from 1 pu to 0.7 pu for 100 ms. The grid voltages in the dq-coordinate system are displayed in Fig.5.17.

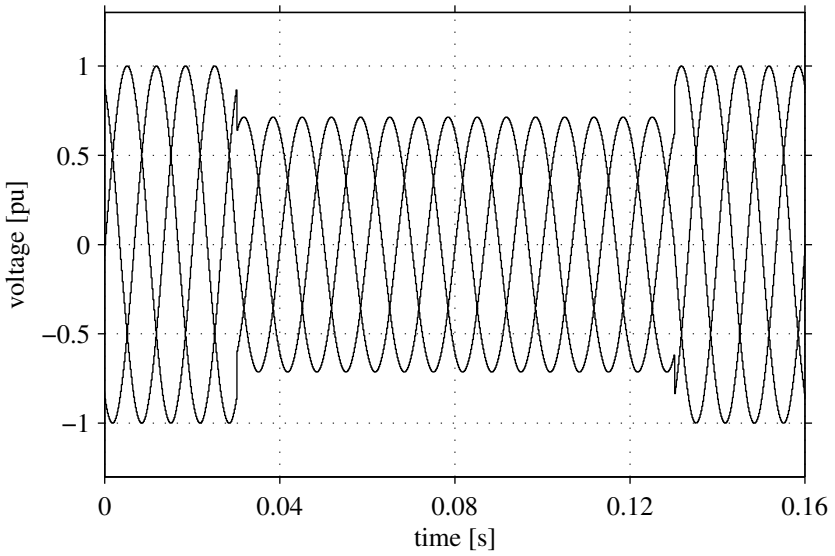


Fig. 5.16 Simulated three-phase grid voltages during 70% balanced voltage dip.

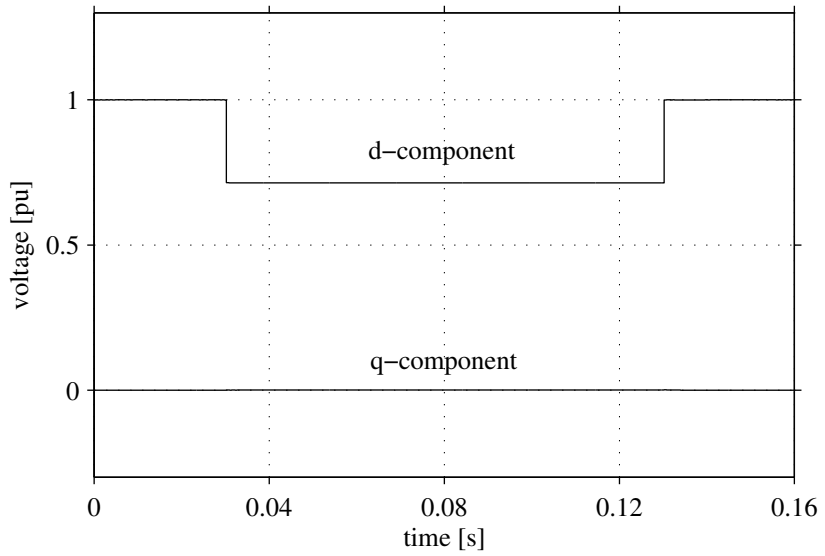


Fig. 5.17 Simulated grid voltages in dq-coordinate system during 70% balanced voltage dip.

Figure 5.18 shows the resulting capacitor voltage in the dq-coordinate system. As shown, before and after the dip, the voltage across the capacitor is approximately zero. When the voltage dip occurs, the d-component makes a step from 0 to 0.3 pu, responding to the reduced grid voltage. The q-component remains constant and is equal to zero. The capacitor voltage tracks its reference with a response time of 2 ms, as shown by the step response of the voltage controller in Fig.5.19. Due to the high bandwidth of the controller, the actual capacitor voltage is affected by an initial overshoot of 0.1 pu. This can be reduced by decreasing the gain $k_{p,vc}$ of the voltage controller. However, this will result in a slower response of the system.

The reactor current $\underline{i}_{\mathrm{r}}^{(dq)}$ is shown in Fig.5.20. As shown, the $i_{\mathrm{r}d}$ and $i_{\mathrm{r}q}$ are equal to 0.6 pu and 0.45 pu before and after the dip, respectively. When the voltage dip occurs, $i_{\mathrm{r}q}$ makes a step down of 0.05 pu, while $i_{\mathrm{r}d}$ remains constant. Both current components show an overshoot, both at the beginning and at the end of the dip. This is due to the sudden variation of the grid voltage.

The control system manages to keep the load voltage to the pre-fault value equal to 1 pu. This can be seen from the three-phase voltage waveforms displayed in Fig.5.21 or, even better, from the dq-voltage in Fig.5.22. The load voltage is affected by a transient both at the beginning and at the end of the voltage dip. This transient is due to the high speed of the control system and can be reduced by slowing down the outer controller. However, the variation of the grid voltage is not instantaneous in reality as in the simulation, thus the transient will be more damped in a real system.

It is of interest to observe the error in the load voltage magnitude in the $\alpha\beta$-coordinate system, calculated as the difference between the reference load voltage $\underline{e}_{\mathrm{l}}^{(\alpha\beta)*}$ and of the actual load voltage $\underline{e}_{\mathrm{l}}^{(\alpha\beta)}$. As displayed in Fig.5.23, the error is practically zero, except for the transients at the beginning and at the end of the voltage dip, where it reaches a peak of 0.17 pu.

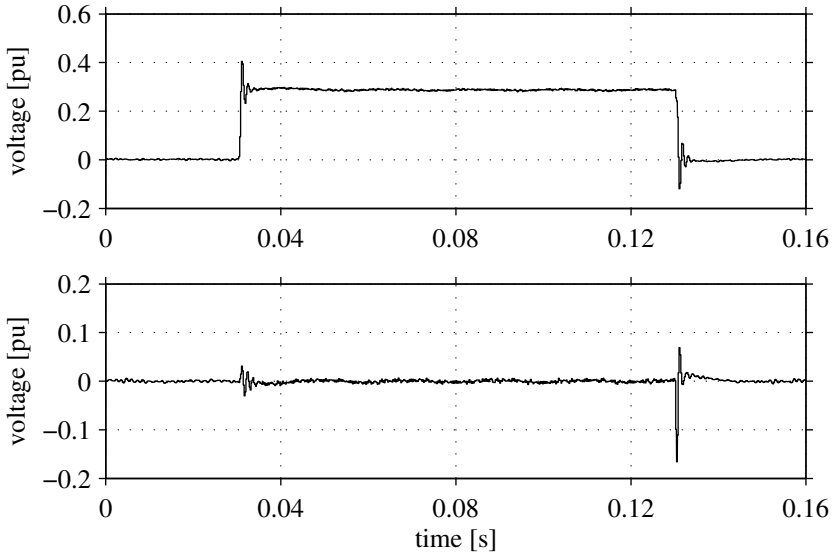


Fig. 5.18 Simulated response of capacitor voltage to balanced voltage dip. DVC1 is used. Top: d-component; bottom: q-component.

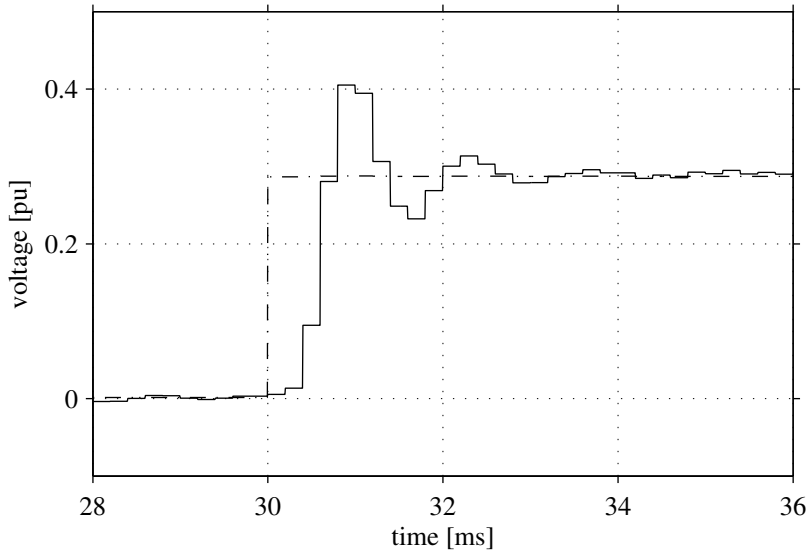


Fig. 5.19 Detail of step response of DVC1 during balanced voltage dip. e^*_{cq}: dashed, e_{cq}: solid.

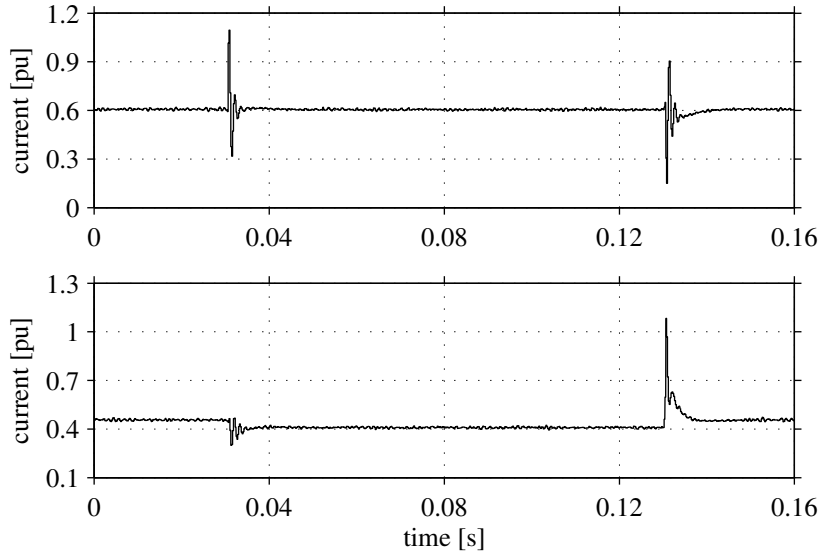


Fig. 5.20 Simulated response of filter reactor current to balanced voltage dip. DVC1 is used. Top: d-component; bottom: q-component.

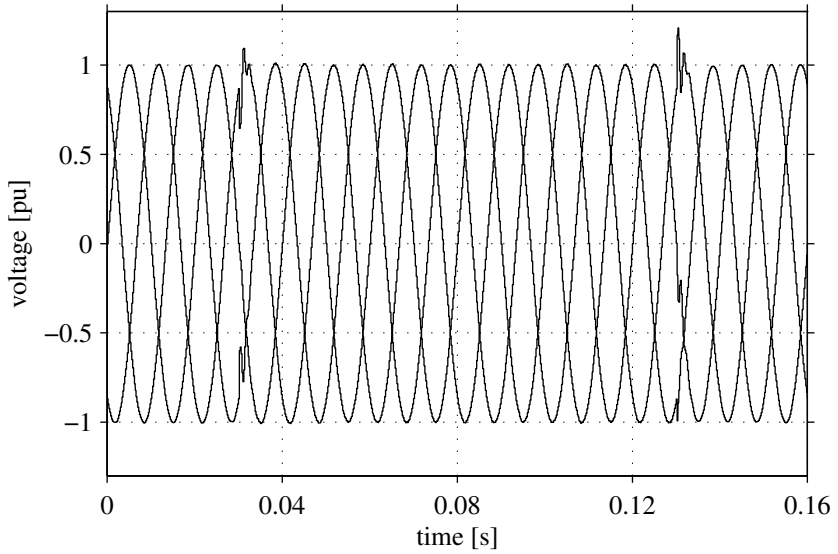


Fig. 5.21 Simulated three-phase load voltage. DVC1 and balanced voltage dip are used.

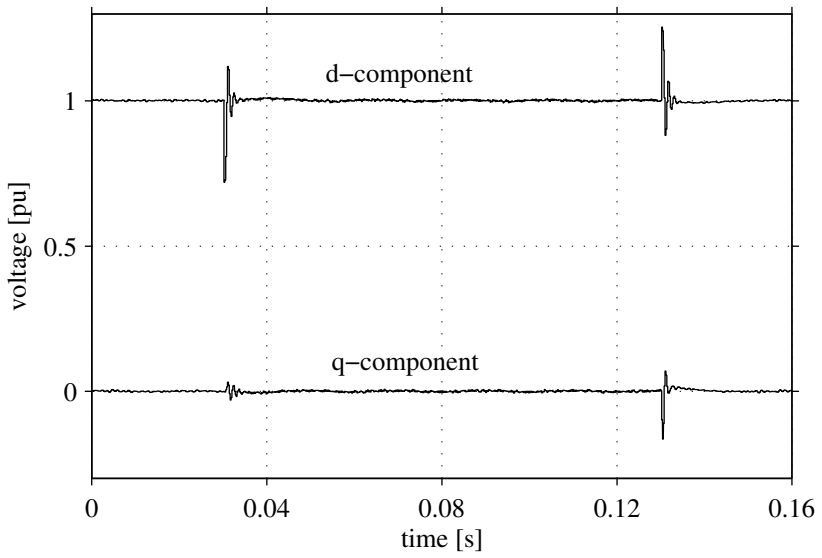


Fig. 5.22 Simulated load voltage in dq-coordinate system. DVC1 and balanced voltage dip are used.

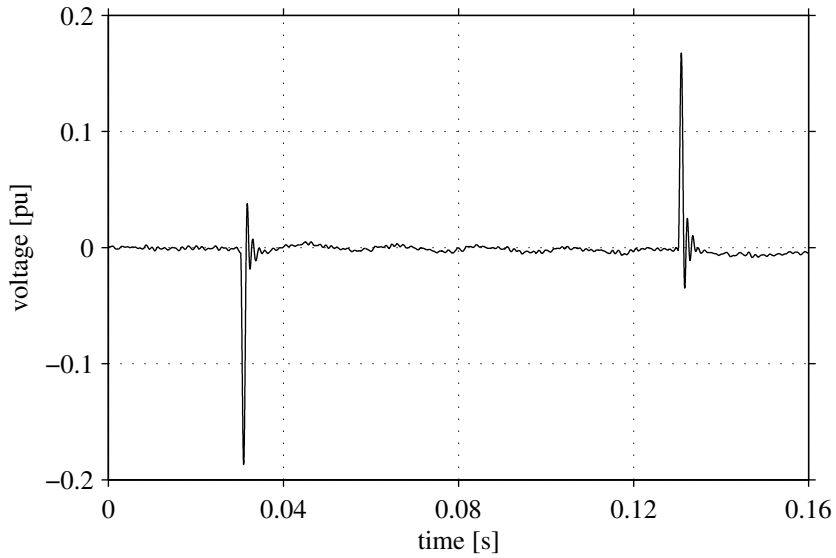


Fig. 5.23 Simulated error of load voltage magnitude. DVC1 and balanced voltage dip are used.

Unbalanced voltage dips

The step response of the implemented DVC1 has also been tested under unbalanced voltage dips. The three-phase grid voltages at PCC are displayed in Fig.5.24. At $t = 0.03$ s, a phase-to-phase fault occurs in the grid and lasts for 100 ms. As a result, phases a and b drop from 1 pu to 0.7 pu and 0.8 pu, respectively, while phase b remains constant and equal to 1 pu. Due to the unbalance, the grid voltages in the dq-coordinate system are affected by a 100 Hz oscillation with amplitude of 0.2 pu (peak-to-peak), as shown in Fig.5.25.

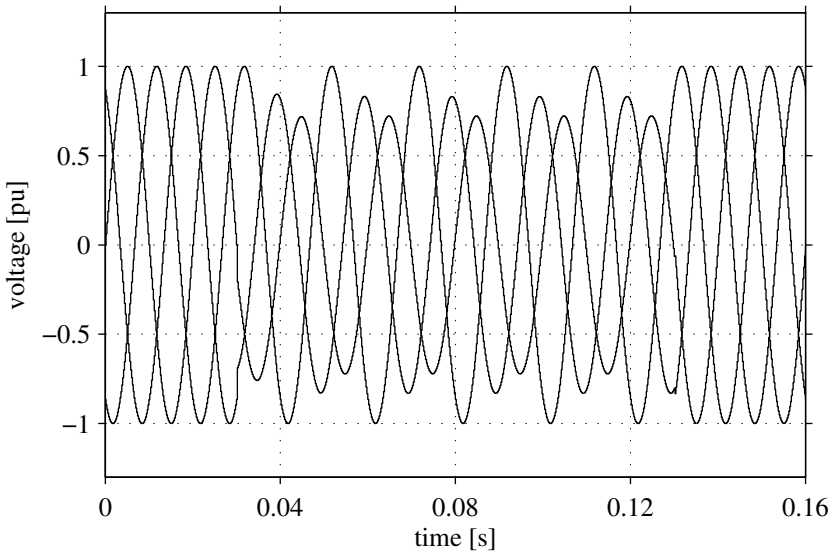


Fig. 5.24 Simulated three-phase grid voltages during unbalanced voltage dip.

The oscillations in the dq-components of the grid voltage during the voltage dip will also affect the capacitor voltage. As shown in Fig.5.26, at the beginning of the voltage dip the controller reacts by fast trying to restore the load voltage to the pre-fault value, but the injected voltage is also affected by 100 Hz oscillations.

As a consequence, the load voltage shown in Fig.5.27 will be only partially restored to the pre-fault value. During the voltage dip, the load voltages are unbalanced. This is more evident in Figs.5.28 and 5.29, where the load voltages in the dq-coordinate system and the error in the load voltage amplitude are oscillating with 100 Hz around the steady-state value during the dip. These oscillations, which have an amplitude of 0.04 pu (peak-to-peak), are proportional to the percentage of unbalance associated to the voltage dip. It has been proven via simulation, by varying one parameter at the time, that the amplitude of these oscillations can be reduced by increasing the size of the filter capacitor, as in Fig.5.30(a), or by increasing the sampling frequency of the control system (see Fig.5.30(b)). On the other hand, the size of the filter reactor and the gains of the inner and outer control loops have been proven to have no influence on the oscillations. Note that when varying the filter capacitor and the sampling frequency, the other parameters of the system have been maintained constant as in Table 5.1. The relative controller gains are the same for all cases.

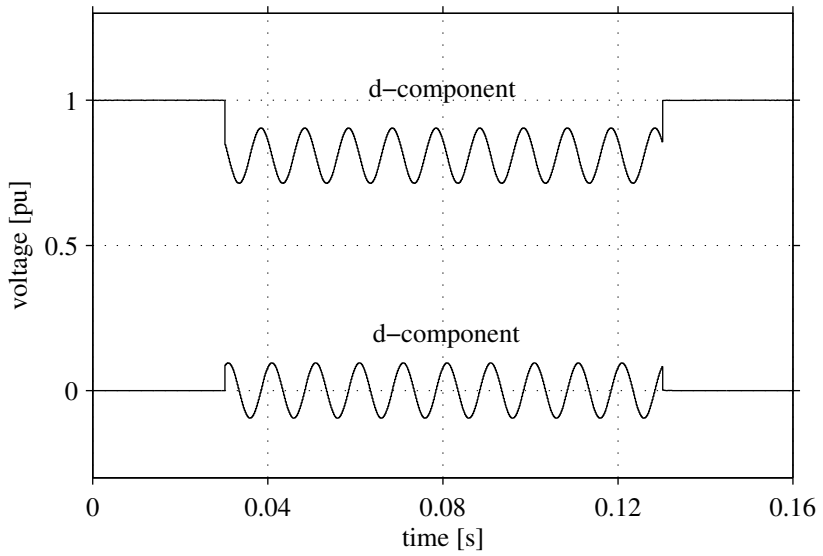


Fig. 5.25 Simulated grid voltages in dq-coordinate system during unbalanced voltage dip.

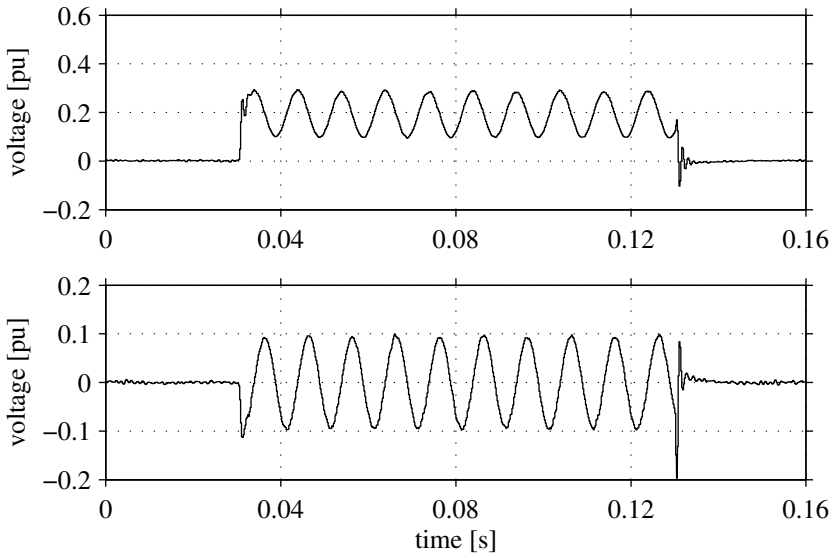


Fig. 5.26 Simulated response of capacitor voltage to unbalanced voltage dip. DVC1 is used. Top: d-component; bottom: q-component.

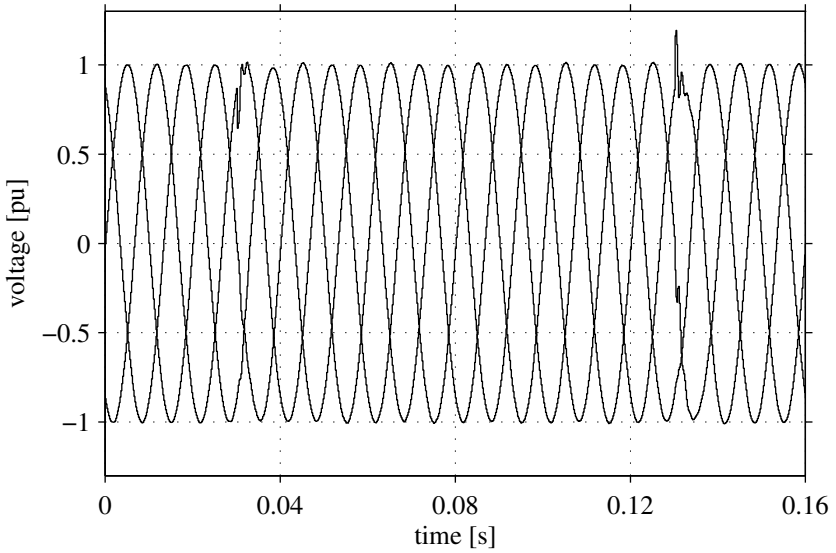


Fig. 5.27 Simulated three-phase load voltage. DVC1 and unbalanced voltage dip are used.

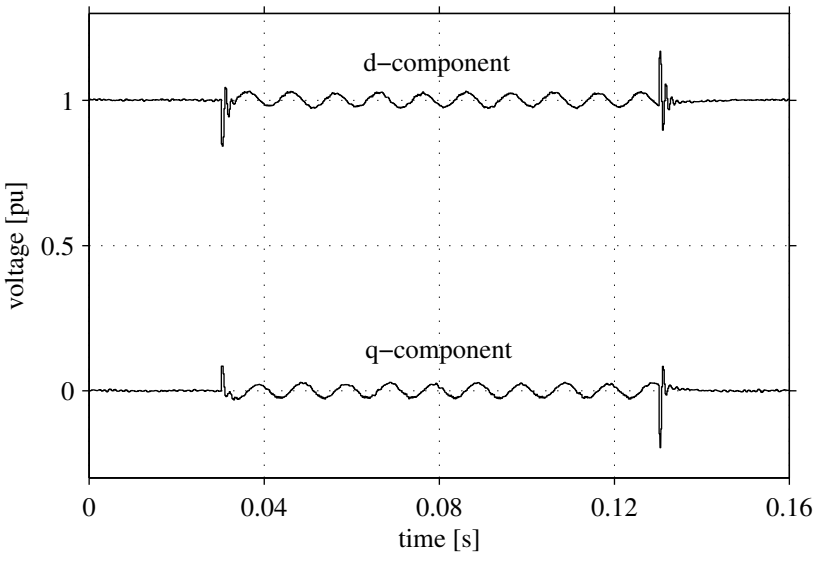


Fig. 5.28 Simulated load voltage in dq-coordinate system. DVC1 and unbalanced voltage dip are used.

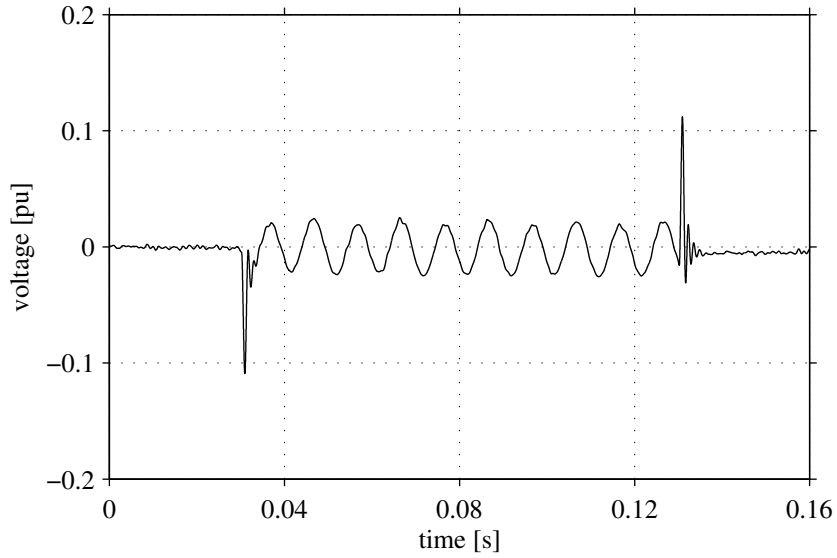


Fig. 5.29 Simulated error of load voltage magnitude. DVC1 and balanced voltage dip are used.

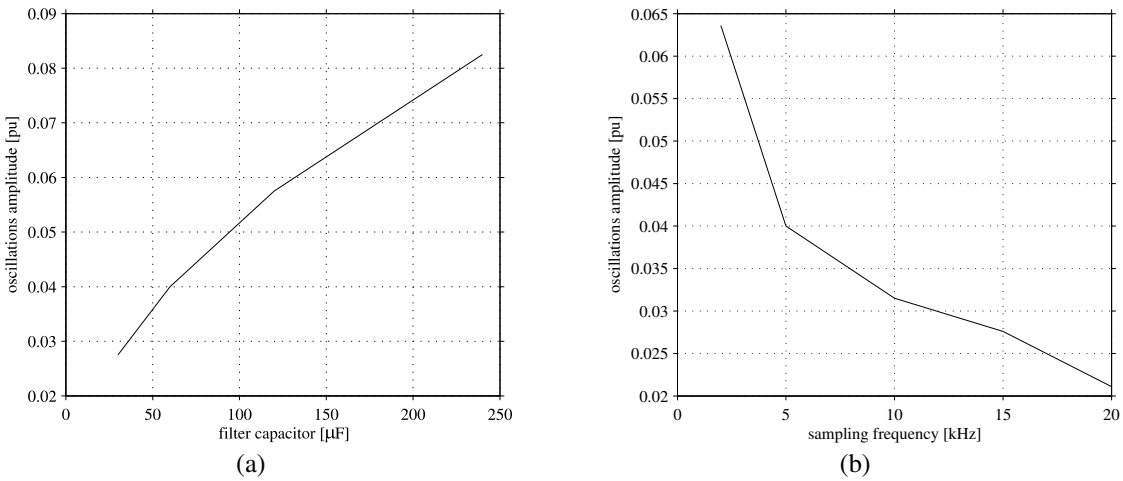


Fig. 5.30 Amplitude of 100 Hz voltage oscillations (peak-to-peak) during unbalanced voltage dip mitigation using DVC1. Oscillation amplitude vs. filter capacitor size: plot (a); oscillation amplitude vs. sampling frequency: plot (b).

5.3.5 Summary

In this section, the cascade controller for the SSC has been presented. The problem with the saturation of the injection transformer during voltage dip mitigation and several solutions have been discussed. The improved cascade controller, here called dual vector-controller type 1 (DVC1), has been tested via simulations under balanced and unbalanced voltage dips. Simulation results show that the DVC1 operates properly under balanced voltage dips and restores the load voltage to the rated value within 2 ms. Under unbalanced voltage dips, the controller is able to mitigate the dip but the load voltage results unbalanced. To improve the mitigation for unbalanced dip, the control system can be modified to inject also a negative sequence in the mains.

5.4 Dual Vector-controller Type 2 (DVC2)

To compensate unbalance dips, it is necessary to modify the DVC1 to inject also a negative sequence voltage. A way to deal with the problem is to detect the positive and the negative sequence components of the grid voltage and calculate separately the sequence components of the reference capacitor voltages. With the same principle used in Section 3.4, it is possible to send to the cascade controller only the positive sequence components of the capacitor voltage $\underline{e}_{\mathrm{c}}^{(dqp)}$ and of the reference voltage $\underline{e}_{\mathrm{c}}^{(dqp)*}$, while $\underline{e}_{\mathrm{c}}^{(dqn)*}$ is directly added to the reference voltage output of the current controller. The block scheme of the improved cascade controller, here called dual vector-controller type 2 (DVC2), is displayed in Fig.5.31. The method used for calculating the sequence components is the DSC, explained in Section 3.3.

5.4.1 Simulation results using DVC2

The DVC2 has been tested under unbalanced voltage dips for different filter capacitor sizes, with the controller parameters displayed in Table 5.2.

The step response of the DVC2 has been tested under the same unbalanced voltage dip displayed in Fig.5.24. The sequence components of the grid voltage are constant in the respective SRFs, as displayed in Fig.5.32. As shown, at $t = 0.03$ s the positive sequence d-component makes a step down from 1 pu to 0.8 pu, while, due to a 5° phase-angle jump, the q-component goes from 0 pu to -0.05 pu. The negative sequence components of the grid voltage are both equal to zero before and after the dip and go down to -0.11 pu during the dip.

Simulated positive and negative sequence of the capacitor voltage are displayed in Fig.5.33. Both are equal to zero before and after the dip. When the dip occurs, the positive sequence d-voltage makes a step from 0 pu to 0.17 pu, while the q-component, due to the presence of the phase-angle jump during the dip, goes from 0 pu to 0.05 pu. The uncontrolled negative sequence components go from 0 pu to 0.1 pu, i.e. the VSC reacts injecting into the mains a negative sequence voltage equal to the negative sequence of the grid voltage $e_{\mathrm{g}}^{(dqn)}$ but opposite in sign.

As a consequence, the voltage dip is mitigated and the load voltage is restored to 1 pu, as shown

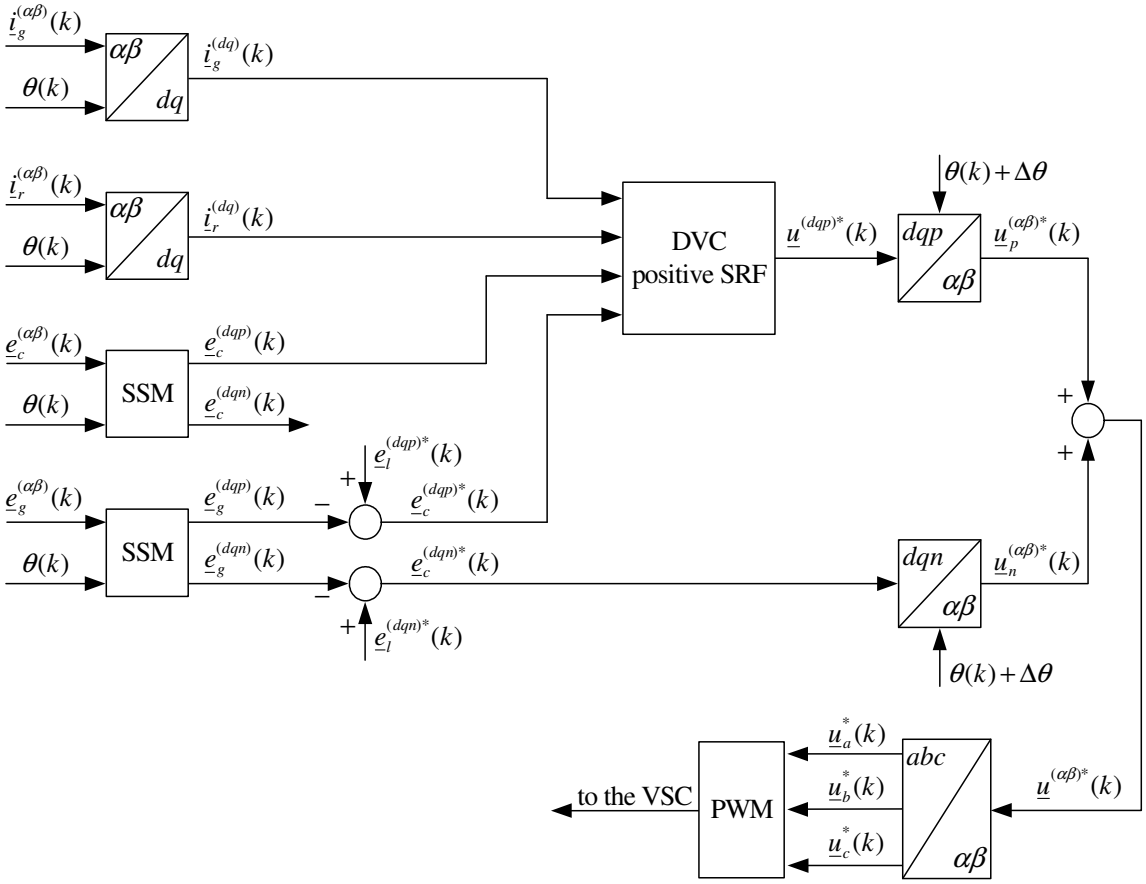


Fig. 5.31 Block-scheme of dual vector-controller type 2 (DVC2).

in Fig.5.34 and Fig.5.35, showing the three-phase load voltage and the corresponding voltage vector components in dq-coordinate system, respectively. Due to the uncontrolled injection of negative-sequence voltage by the SSC, the load voltage is still not perfectly balanced during the dip. Figure 5.36 shows the error in the load voltage magnitude in the $\alpha\beta$-coordinate system, which is still oscillating with twice the grid frequency and has amplitude of 0.03 pu (peak-to-peak).

To understand the reason why the load voltage is affected by this unbalance during the voltage dip, it is necessary to make a step back and consider the block-diagram of the DVC2 in Fig.5.31. The negative-sequence reference voltage is practically the opposite of the negative-sequence grid voltage, as the desired load voltage at negative sequence is normally zero. This voltage is reproduced at the output of the VSC. The actual injected voltage, however, which is the voltage across the filter capacitor, differs from the VSC output voltage by the voltage drop on the filter inductor. This gives an error in the injected negative-sequence voltage as compared with the desired value. The problem obviously does not arise for the positive sequence of the capacitor voltage, which is controlled with a feedback loop. Therefore, the error in the negative-sequence voltage injection will depend on the amount of negative-sequence current flowing on the filter reactor. For a given value of negative-sequence voltage and filter reactance, the amount of current depends on the capacitor size. The error will thus increase with increasing capacitor size, as a bigger capacitor draws higher current.

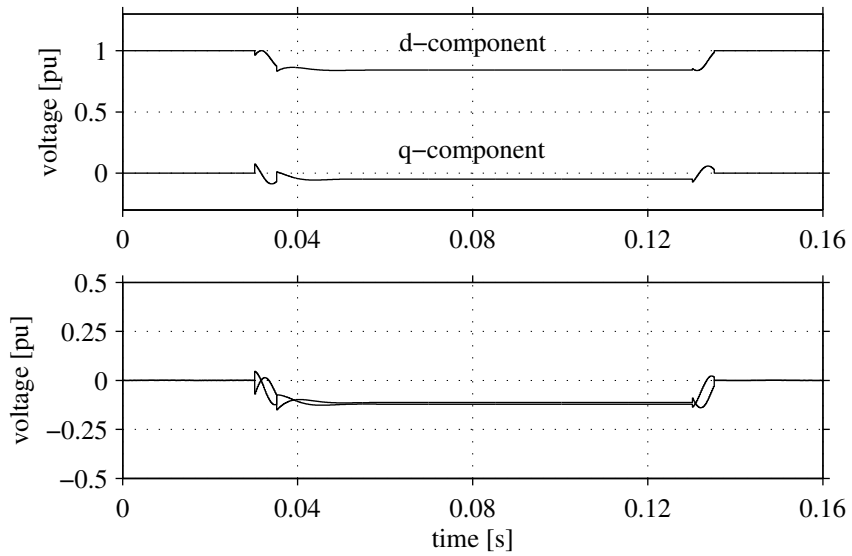


Fig. 5.32 Simulated grid voltages in dq-coordinate system during unbalanced voltage dip. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

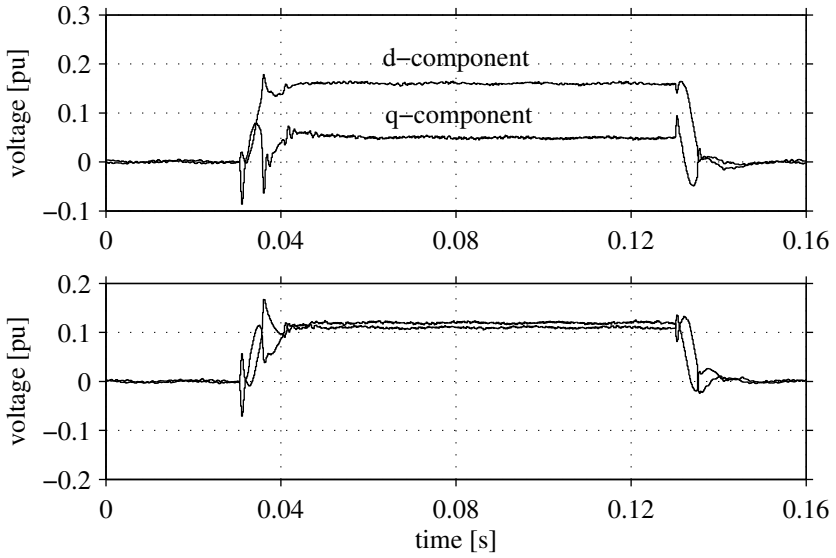


Fig. 5.33 Simulated response of capacitor voltage in dq-coordinate system to unbalanced voltage dip. DVC2 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

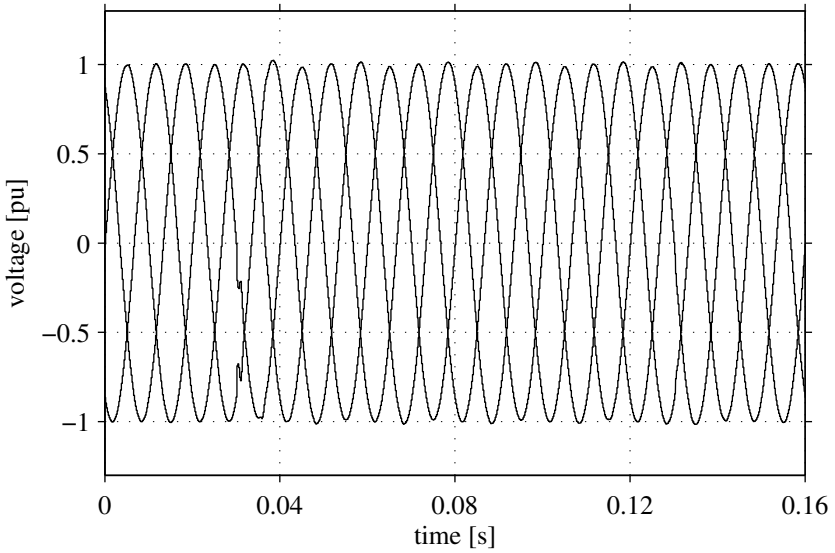


Fig. 5.34 Simulated three-phase load voltages during unbalanced voltage dip. DVC2 is used.

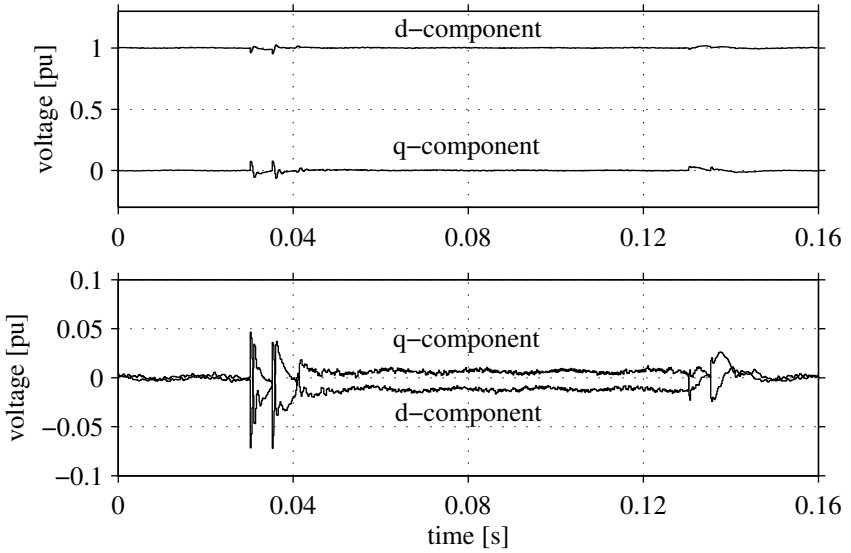


Fig. 5.35 Simulated load voltages in dq-coordinate system during unbalanced voltage dip. DVC2 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

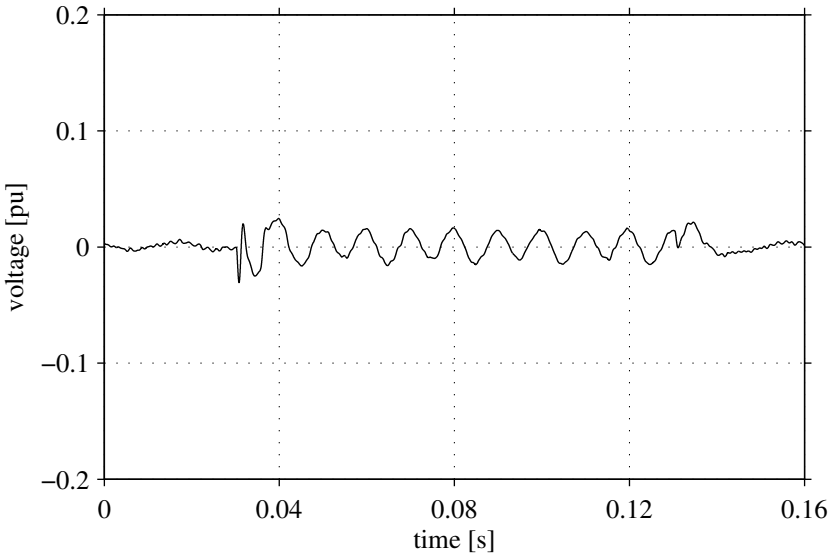


Fig. 5.36 Simulated error of load voltage magnitude during unbalanced voltage dip. DVC2 is used.

Figures 5.37 and 5.38 show the error in the load voltage magnitude when the grid voltage is affected by the voltage dip in Fig.5.24 for $C = 120$ μF and $C = 30$ μF, respectively. As shown, when increasing the capacitor size the error in the load voltage magnitude increases, while a reduced size of the filter capacitor results in lower voltage error. Therefore, when SSC with DVC2 is used, the design of the filter capacitor is a trade-off between the required cut-off frequency of the LC-filter and the necessity of creating a high-impedance path for the negative-sequence current at the VSC output. This can also be seen from Fig.5.39(a), where the amplitude of the oscillations as a function of the filter capacitor when using SSC with DVC2 is shown. As already mentioned in the previous section, the amplitude of these oscillations can also be reduced by increasing the sampling frequency of the control system, as in Fig.5.39(b). Note that when varying the filter capacitor and the sampling frequency, the other parameters of the system have been maintained constant as in Table 5.1. The relative controller gains are the same for all cases.

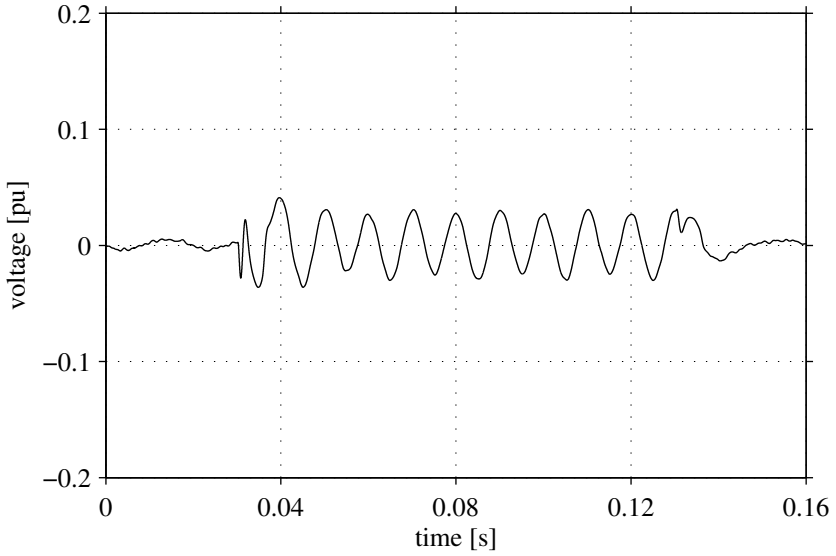


Fig. 5.37 Simulated error of load voltage magnitude during unbalanced voltage dip. DVC2 and filter capacitor $C = 120$ μF are used.

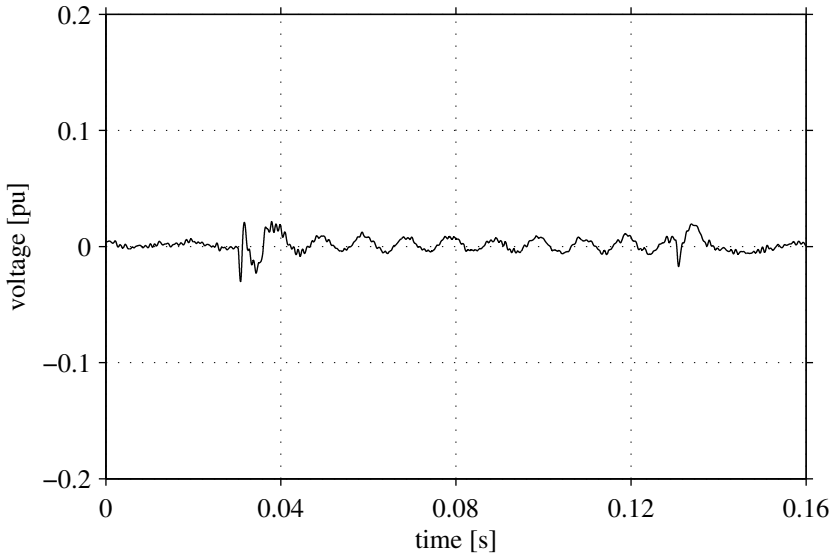
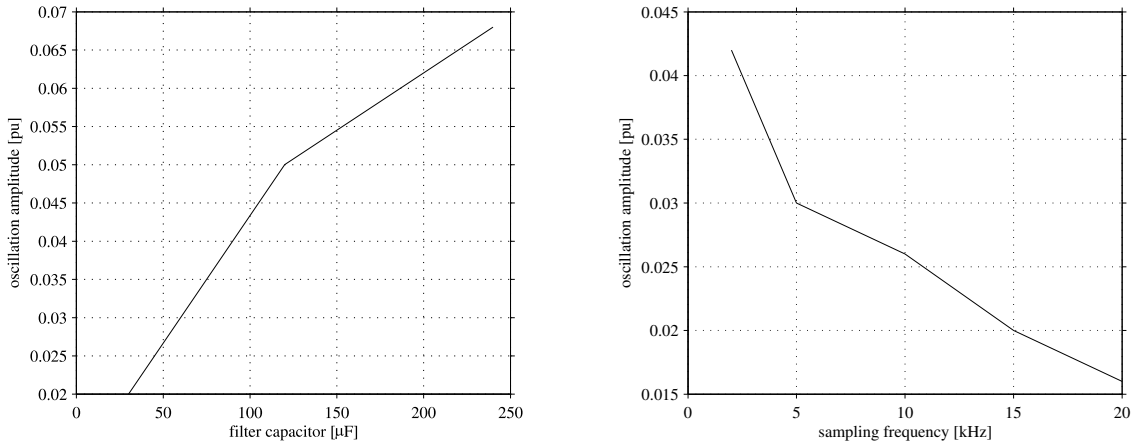


Fig. 5.38 Simulated error of load voltage magnitude during unbalanced voltage dip. DVC2 and filter capacitor $C = 30$ μF are used.



(a) (b)

Fig. 5.39 Amplitude of 100 Hz voltage oscillations (peak-to-peak) during unbalanced voltage dip mitigation using DVC2. Oscillation amplitude vs. filter capacitor size: plot (a); oscillation amplitude vs. sampling frequency: plot (b).

5.4.2 Summary

In this section, the modified cascade controller DVC2 has been presented. It has been shown that the performance of the DVC2, although improved as compared to DVC1, does not eliminate completely the unbalance in the load voltage. With a careful choice of the filter capacitor, the unbalance can be greatly reduced. However, to ensure complete cancellation of the unbalance in the load voltage, independently of the filter design, further modifications to the controller can be applied.

5.5 Dual Vector-controller Type 3 (DVC3)

In the dual vector-controller type 3 (DVC3), positive- and negative-sequence components of the VSC current $\underline{i}_{\mathrm{r}}^{(dq)}$ and filter capacitor voltage $\underline{e}_{\mathrm{c}}^{(dq)}$ are controlled independently by using two cascade controllers implemented in the positive and in negative SRFs, respectively, as displayed in Fig.5.40. The sequence detection is using the DSC algorithm. Positive- and negative-sequence components of the reference capacitor voltage are calculated as shown in Fig.5.31. The voltage controller used for the positive-sequence DVC is the one derived in Section 5.3.1. The voltage controller implemented in the negative SRF is obtained as

$$\begin{aligned}\underline{i}_{\mathrm{r}}^{(dqn)*}(k) = \underline{i}_{\mathrm{g}}^{(dqn)}(k) - \mathrm{j}\frac{\omega C}{2}(\underline{e}_{\mathrm{c}}^{(dqn)*}(k) + \underline{e}_{\mathrm{c}}^{(dqn)}(k)) + k_{\mathrm{p,vc}}(\underline{e}_{\mathrm{c}}^{(dqn)*}(k)+ \\ - \underline{e}_{\mathrm{c}}^{(dqn)}(k)) + \sum_{n-1}^{k} k_{\mathrm{i,vc}}(\underline{e}_{\mathrm{c}}^{(dqn)*}(n-1) - \underline{e}_{\mathrm{c}}^{(dqn)}(n-1))\end{aligned} \tag{5.25}$$

The current controllers are also separated for the two sequences as in the DVCC, explained in Section 3.5.

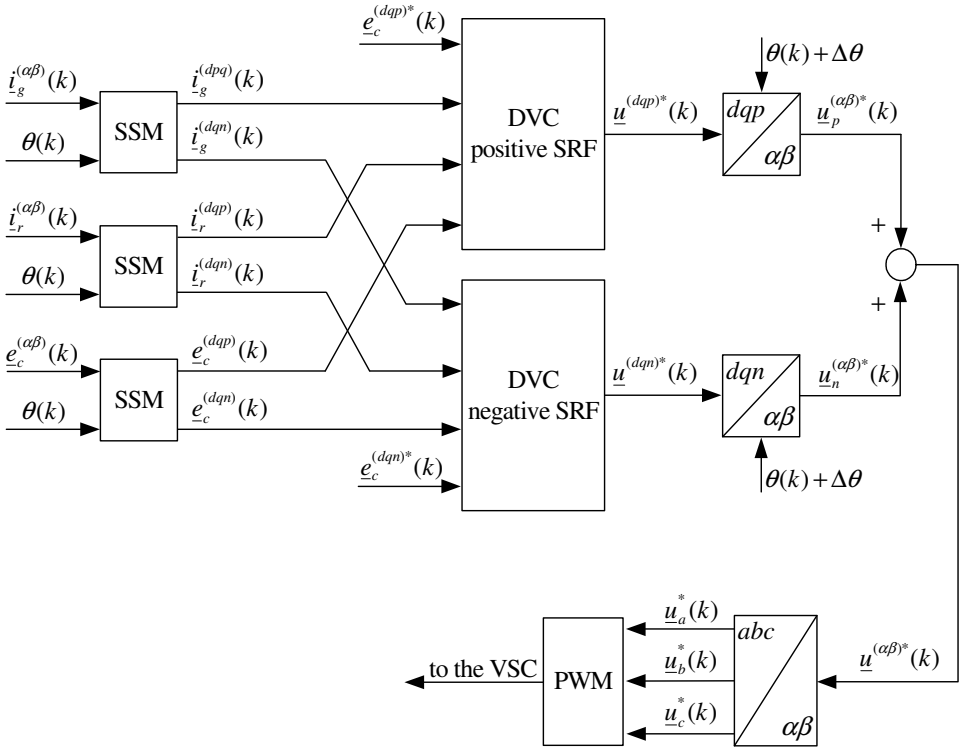


Fig. 5.40 Block-scheme of dual vector-controller type 3 (DVC3).

5.5.1 Simulation results using DVC3

In this section, simulation results for DVC3 will be presented. The control system has been tested under unbalanced voltage dips. Moreover, the dynamic performance of the controller when protecting different loads (diode rectifier, induction machine) will be shown.

As explained in Section 3.5.1, due to the delay introduced by the DSC, it is not possible to use a deadbeat current controller in DVCC due to instability. Therefore, the bandwidth of the current controller (and consequently of the voltage controller) has to be reduced. The parameters for the DVC3 are displayed in Table 5.3.

TABLE 5.3. CONTROLLER PARAMETERS FOR DVC3.

Sampling frequency	f_s = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Current controller parameters			
Proportional gain	$k_{p,cc}$	7.01	(70% deadbeat)
Integrator gain	$k_{i,cc}$	0	
Observer gain	k_{psp}	0.1	
Voltage controller parameters			
Proportional gain	$k_{p,vc}$	0.075	(25% deadbeat)
Integrator time constant	$T_{i,vc}$	0.03	

Unbalanced voltage dips

In this first set of simulation results, the DVC3 has been tested under unsymmetrical voltage dips when protecting a RL-load from voltage dips. The system parameters are displayed in Table 5.1.

To compare the performance of the DVC3 with the results obtained for the DVC2, the SSC has been tested for the same voltage dip as in Section 5.4.1. The three-phase grid voltages and the components of the corresponding voltage vector in the dq-coordinate system during an unbalance voltage dip are displayed in Figs.5.24 and 5.32, respectively.

Due to the variation in the grid voltage, the VSC current makes a step to charge the filter capacitor. As displayed in Fig.5.41, where the controlled positive- and the negative-sequence components of the VSC current in the corresponding dq-coordinate systems are displayed, the operating point is 0.6 pu d-component and 0.45 pu q-component for the positive sequence and 0 pu both for the d- and the q-component of the negative sequence. When the dip occurs, the d-component of the positive sequence makes a step down of 0.01 pu, while the q-component goes to 0.43 pu. Due to the unbalance, the negative sequence becomes -0.02 pu. It is possible to observe that, due to the scaling of the figure, the current ripple due to the PWM pattern, which was not visible in Fig.5.20, is now visible.

Figure 5.42 shows the step response of the positive and the negative sequence of the controlled filter capacitor voltage. In steady-state before and after the dip, all components are equal to zero. During the dip, the d- and q- components of the positive sequence go to 0.16 pu and -0.05 pu, respectively. The d-component of the negative sequence increases t 0.11 pu, while the q-component becomes -0.11 pu.

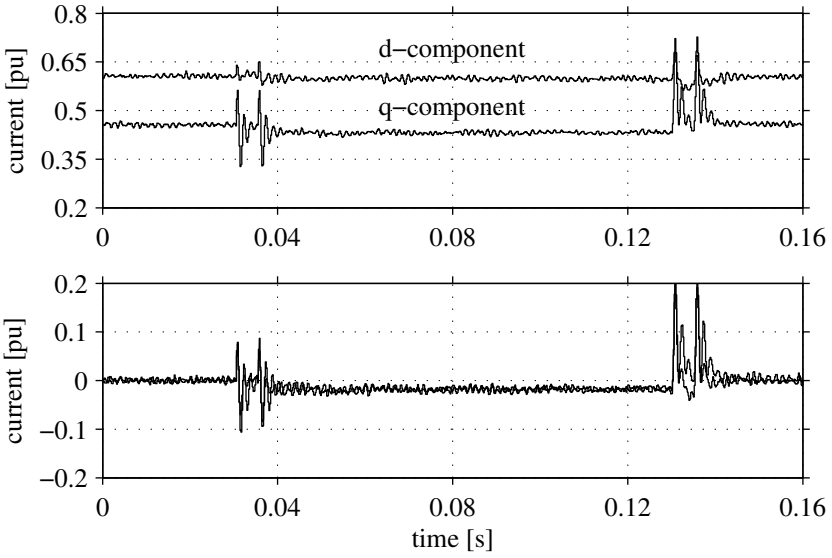


Fig. 5.41 Simulated response of d- and q-component of VSC current to unbalanced voltage dip. DVC3 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

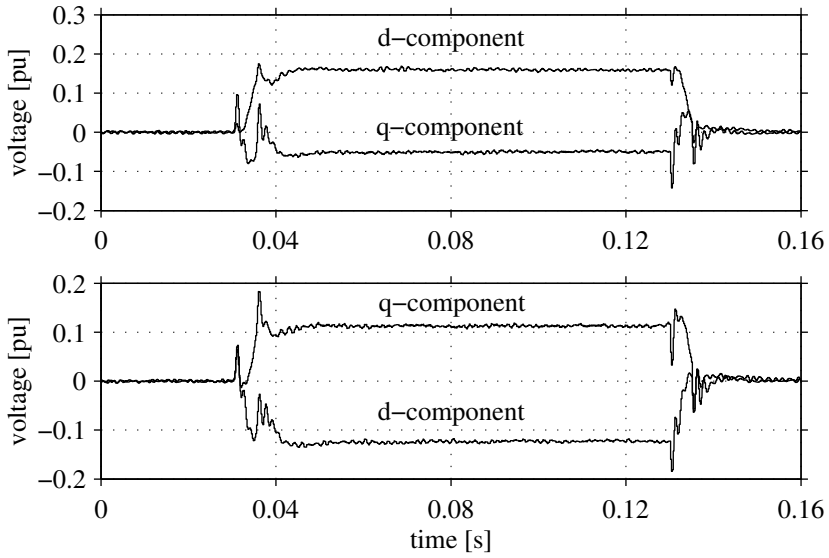


Fig. 5.42 Simulated response of d- and q-component of voltage capacitor to unbalanced voltage dip. DVC3 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

The three-phase load voltage is depicted in Fig.5.43. The load voltage is constant at 1 pu before, during and after the dip, apart from the transient at the beginning and at the end of the dip. The positive- and the negative-sequence components of the load voltage in the dq-coordinate system, shown in Fig.5.44, display that the load voltage is unaffected by the dip, except for small transients in the beginning and in the end of the dip.

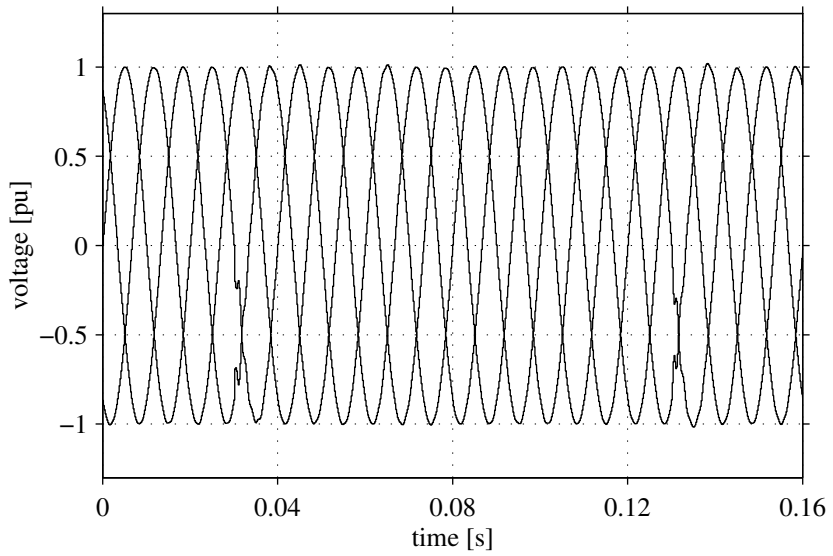


Fig. 5.43 Simulated three-phase load voltages during unbalanced voltage dip. DVC3 is used.

The performance of the DVC3 during unbalance voltage dips is satisfactory, as shown in Fig.5.45, where the error in the load voltage amplitude in the $\alpha\beta$-coordinate system is displayed. It is pos-

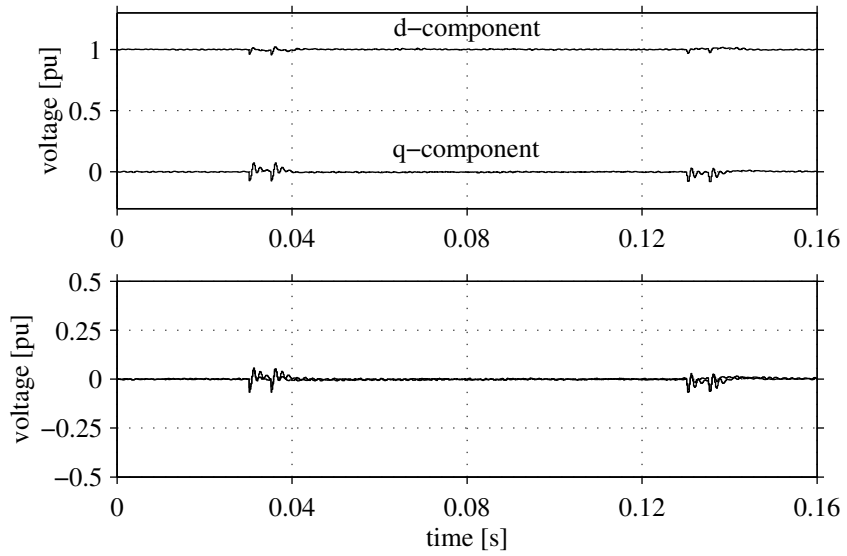


Fig. 5.44 Simulated load voltages in dq-coordinate system during unbalanced voltage dip. DVC3 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

sible to notice that, apart from the transient at the start and at the end of the dip, where the error has a maximum value of 0.025 pu due to the SSM, the error can always be considered zero.

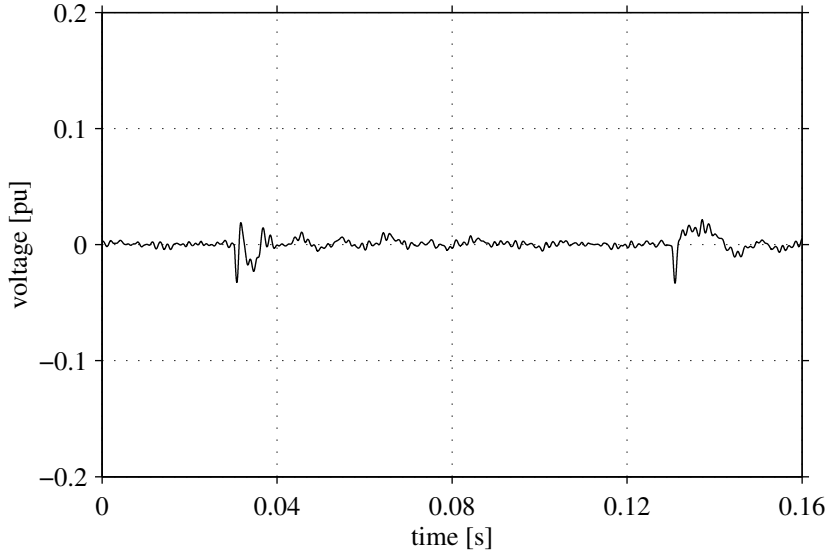


Fig. 5.45 Simulated error of load voltage magnitude during unbalanced voltage dip. DVC3 is used.

Diode rectifier load

In this section, the performance of the SSC with DVC3 when protecting a diode rectifier load will be shown. The use of three-phase diode rectifiers is widespread in industrial installations, since it represent a cost-effective way to convert AC to DC voltage. The main disadvantage when

using diode rectifiers is the highly distorted AC current. Therefore, in typical configurations, a smoothing inductance is mounted on the AC side. Moreover, to smooth the voltage ripple on the DC side of the diode rectifier, a DC capacitor can be used. The single-line diagram of the grid with the SSC that is installed to protect the diode rectifier load is shown in Fig.5.46. The smoothing inductance is denoted by L_c and is equal to 3 mH (0.1 pu), while the smoothing DC capacitor is equal to 300 μF. The load is constituted by a 10 Ω resistor.

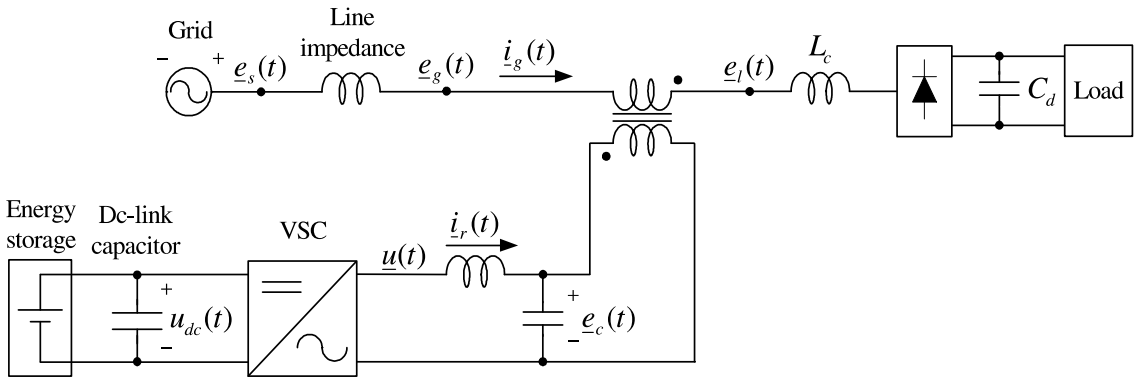


Fig. 5.46 Single-line diagram of grid with SSC and diode rectifier load.

The three-phase grid voltage and the dq-voltages of the grid are shown in Fig.5.47 and 5.48, respectively. At $t = 0.03$ s a three-phase voltage dip occurs in the grid and the voltage drop from 1 pu to 0.67 pu. From Fig.5.48 it is possible to notice that the d-component of the positive sequence goes from 1 pu to 0.7 pu, while the q-component increases from 0 pu to 0.1 pu, denoting that a $9°$ phase-angle jump is associated to the dip.

The grid current in the three-phase coordinate system is depicted in Fig.5.49. From the figure it is possible to notice that the current drawn by the diode rectifier is highly distorted: the current is affected by a 14.89% 5^{th} harmonic and by a 5.78% 7^{th} harmonic. The current THD is about 16%.

Also under these conditions, the DVC3 works properly and the SSC can mitigate the voltage dip and keep the load voltage to the pre-fault conditions. This is shown in Figs.5.50 to 5.52, where the three-phase load voltage and the corresponding dq-voltage together with the error of the load voltage magnitude are displayed. It can be noticed that due to the distorted current floating in the grid impedance, the load voltage is not purely sinusoidal, but is affected by low-order harmonics, resulting in a THD of 9.61%.

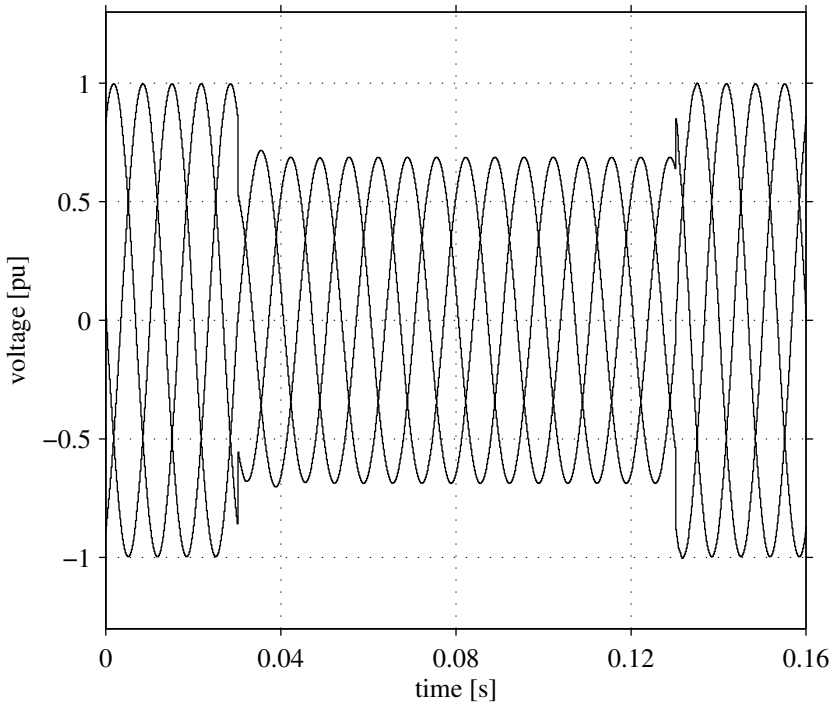


Fig. 5.47 Simulated three-phase grid voltages during balanced voltage dip.

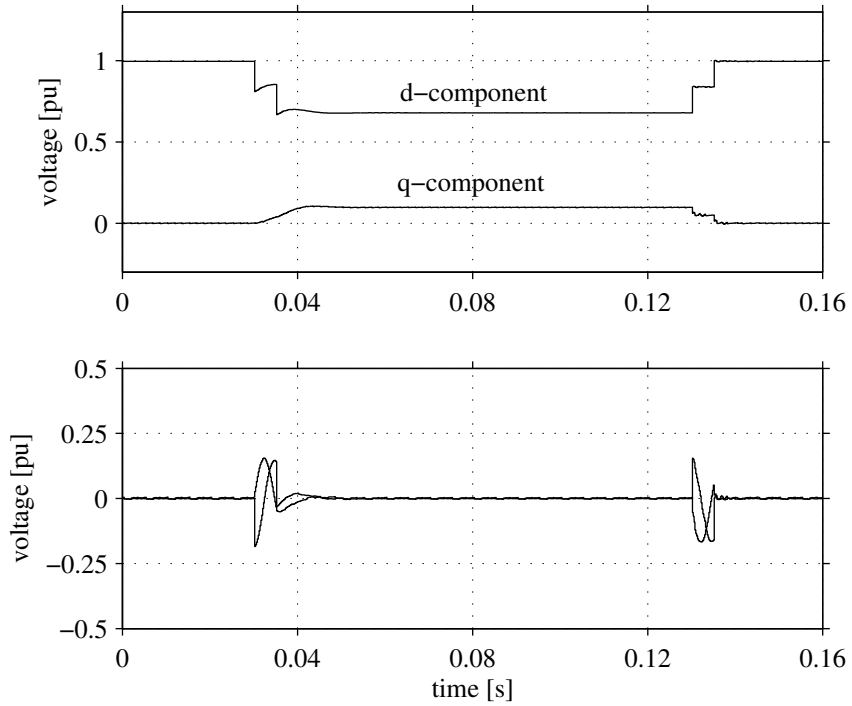


Fig. 5.48 Simulated grid voltages in dq-coordinate system during balanced voltage dip with 9° phase-angle jump. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

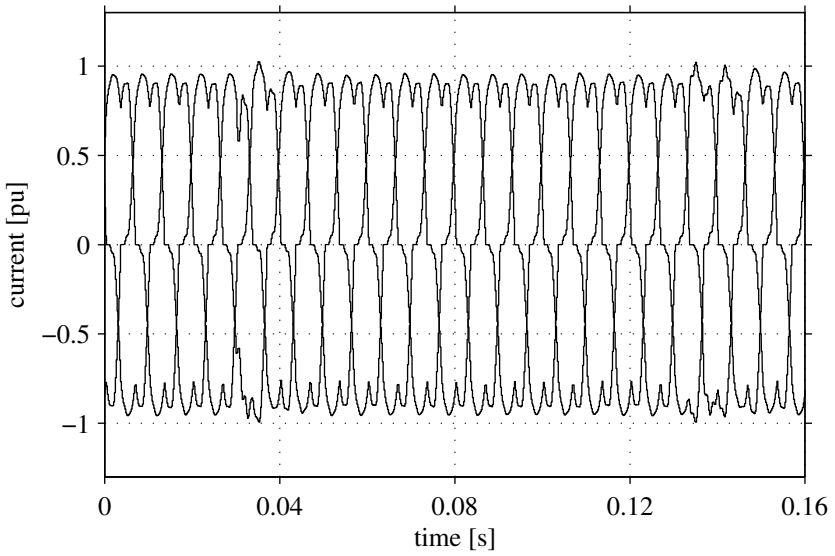


Fig. 5.49 Simulated three-phase grid currents during balanced voltage dip with 9° phase-angle jump in case of diode rectifier load.

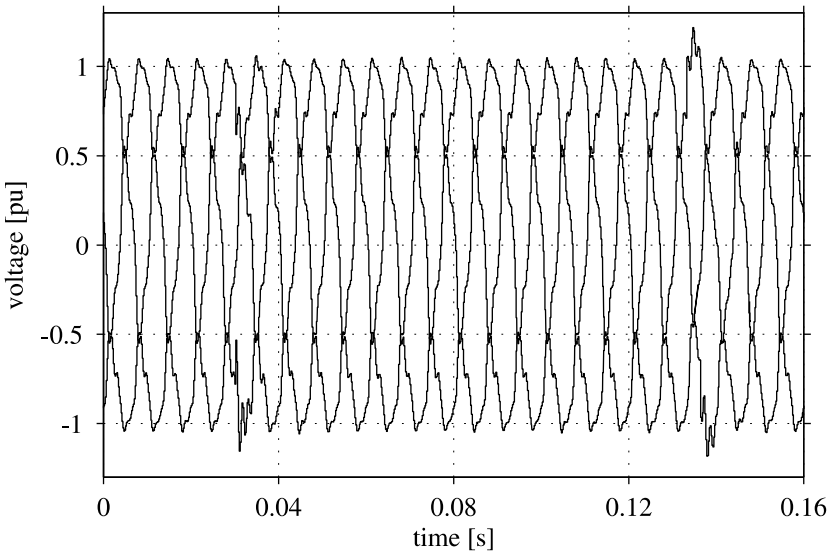


Fig. 5.50 Simulated three-phase load voltages during balanced voltage dip with 9° phase-angle jump. DVC3 and diode rectifier load are used.

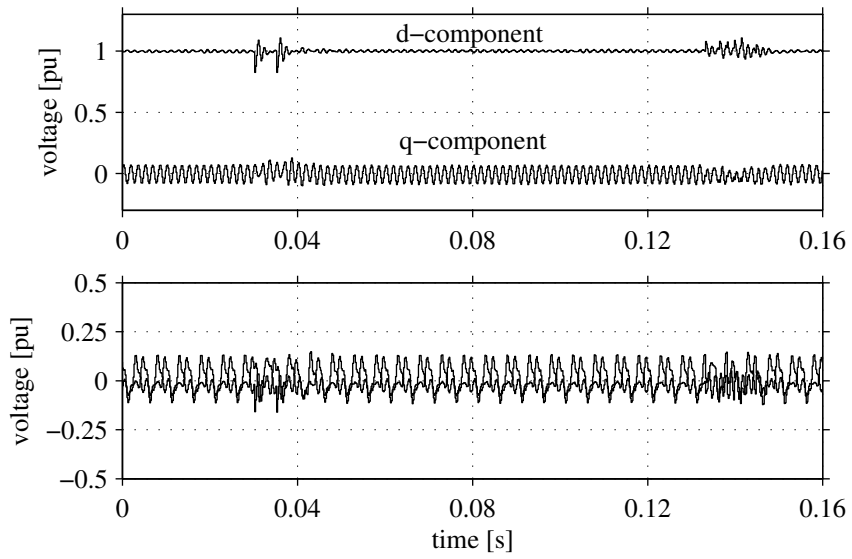


Fig. 5.51 Simulated load voltages in dq-coordinate system during unbalanced voltage dip with 9° phase-angle jump. DVC3 and diode rectifier load are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

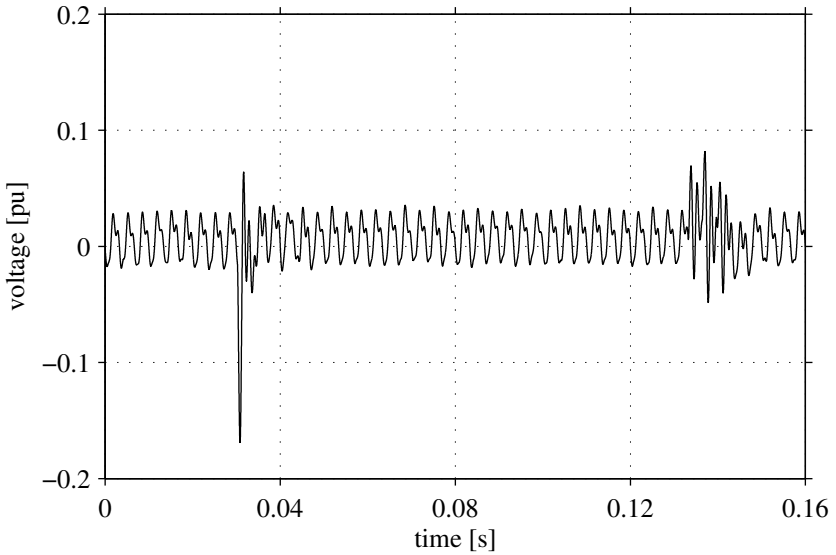


Fig. 5.52 Simulated error of load voltage magnitude during unbalanced voltage dip. DVC3 and diode rectifier load are used.

From the results above, it is of interest to analyze how the current harmonics propagate through the SSC when DVC3 is used. In the first case considered, the diode rectifier is supplied by the system without the SSC in between. The current of the diode rectifier has characteristic low-order odd harmonics, giving a current THD of 20.81%, shown in Fig.5.53(a). These harmonic currents, flowing through the small grid impedance, results in a harmonic distortion of the load voltage of 0.399% (Fig.5.53(b)). When the SSC is inserted in series with the line and with the VSC in idle mode, i.e. with the upper valves in the bridge always on and the other ones off, or vice versa, the VSC acts as a short circuit. Therefore, the whole SSC can be modelled as an impedance in series with the line. The SSC behaves as a passive filter, consisting of L_{r} and C in parallel and then in series with the leakage impedance of the transformer. This is schematically represented in Fig.5.54, where L_{tr} denotes the leakage inductance of the injection transformer.

The current drawn by the diode rectifier in this condition is smoothed by the increased inductance in between the rectifier and the grid, which results in a lower THD for the current (16.94%), see Fig.5.53(c). Still, the lower harmonic current results into a higher harmonic content of the load voltage (THD $= 23.42\%$), again because of the increased impedance between grid and load, as in Fig.5.53(d). Figures 5.53(e) and 5.53(f) are obtained when the SSC is on line and the grid voltage is balanced and at nominal value. The reference voltage for the SSC is then equal to zero for all components. However, the measured voltage will present a low-frequency ripple (THD $= 9.94\%$) due to the current harmonics (THD $= 16.62\%$) circulating in the grid impedance. The control system attempts at compensating this ripple by injecting a voltage containing low-frequency components, in addition to a small fundamental component that compensates the voltage drop on transformer and filter. However, the control system has been designed to compensate only the fundamental voltage and therefore the injected harmonic voltage components do not have the correct phase angle to obtain full compensation. For this reason, the resulting harmonic content of the load voltage is reduced as compared to with the SSC in idle mode, but still higher than without the SSC. In the more general case where the SSC protects a whole industrial facility with several loads, the harmonic voltage distortion created by non-linear loads could then create problems for other highly sensitive loads. With only some additional modifications in the controller, full compensation of harmonic voltage components can be achieved, thus utilizing the same device also as a series active filter [48][37][38].

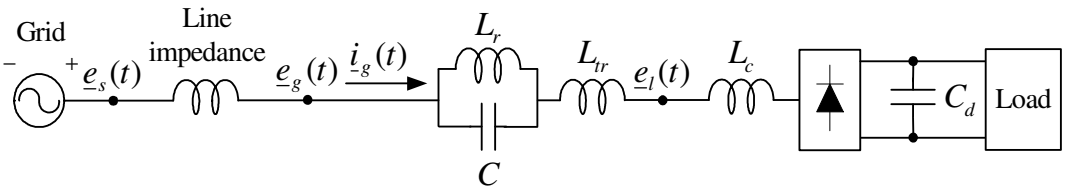


Fig. 5.54 Single-line diagram of grid with SSC and diode rectifier load. VSC in idle mode

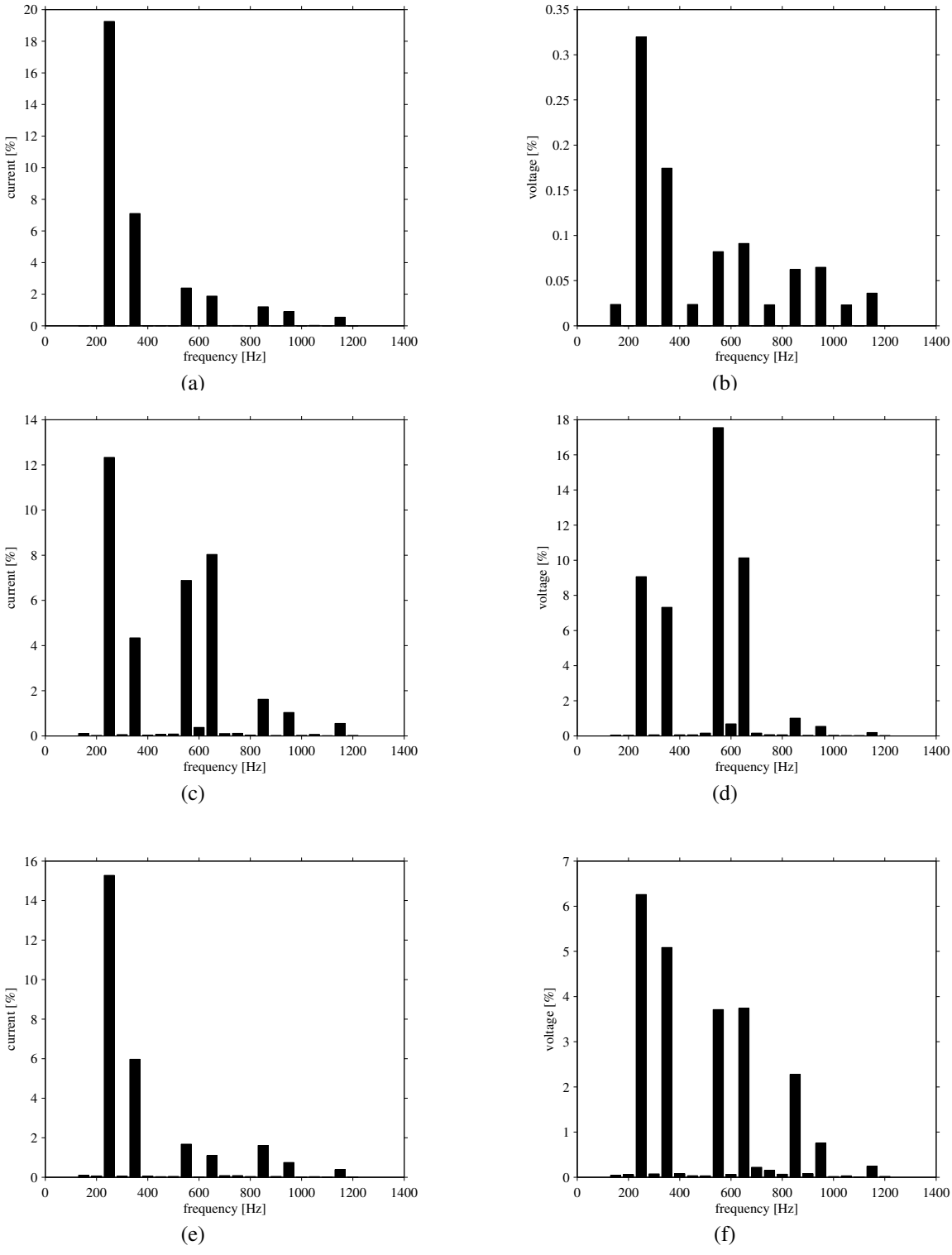


Fig. 5.53 Harmonic content of load current and voltage when using diode rectifier load. SSC disconnected: current (a), voltage (b); SSC idle: current (c), voltage (d); SSC online: current (e), voltage (f).

Induction machine load

Finally, the performance of the SSC with DVC3 has been tested for protection of an induction machine. The single-line diagram of the grid with the SSC installed to protect the induction machine is shown in Fig.5.55. Parameters of the simulated induction machine are displayed in Table 5.4. A constant torque, equal to 100 Nm has been applied to the rotor shaft, resulting in 0.45 pu load level.

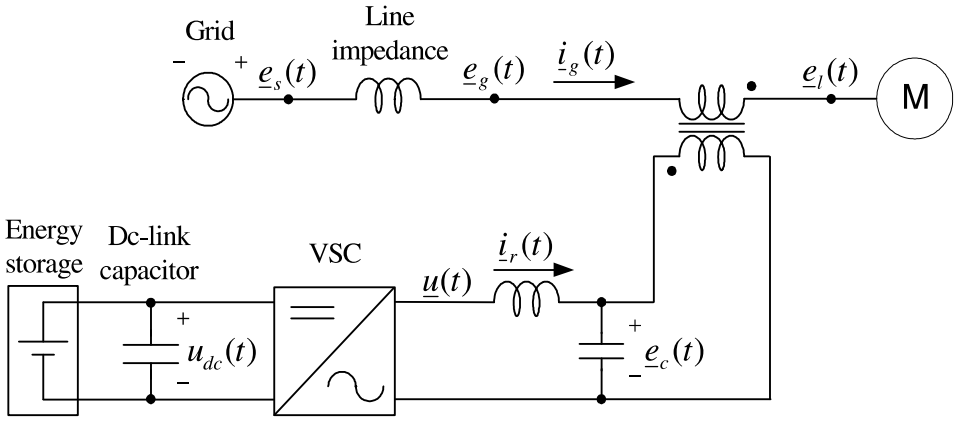


Fig. 5.55 Single-line diagram of grid with SSC and machine load.

TABLE 5.4. INDUCTION MACHINE PARAMETERS.

Rated power	22 kW
Rated voltage	400 V
Rated frequency	50 Hz
Number of poles	2
Rated speed	1430 rpm
Stator resistance	0.18 Ω
Rotor resistance	0.2256 Ω
Stator/rotor inductance	45.6 mH
Magnetizing inductance	4.9 mH
Inertia	0.785 kg · m^2

For this type of load, a three-phase voltage dip has been considered. Three-phase grid voltages are shown in Fig.5.56. The dip occurs after 0.03 s and lasts for 0.8 s. The sequence components of the grid voltage in the dq-coordinate system are shown in Fig.5.57. As shown, during the dip the d-component of the positive sequence decreases from 1 pu to 0.6 pu, while the q-component increases from 0 pu to 0.1 pu, denoting that the during the dip the grid voltage is affected by a 10° phase-angle jump. Since the voltage dip is balanced, the negative-sequence components of the grid voltage are always zero, except from the transient at the beginning and at the end of the dip, due to the used SSM.

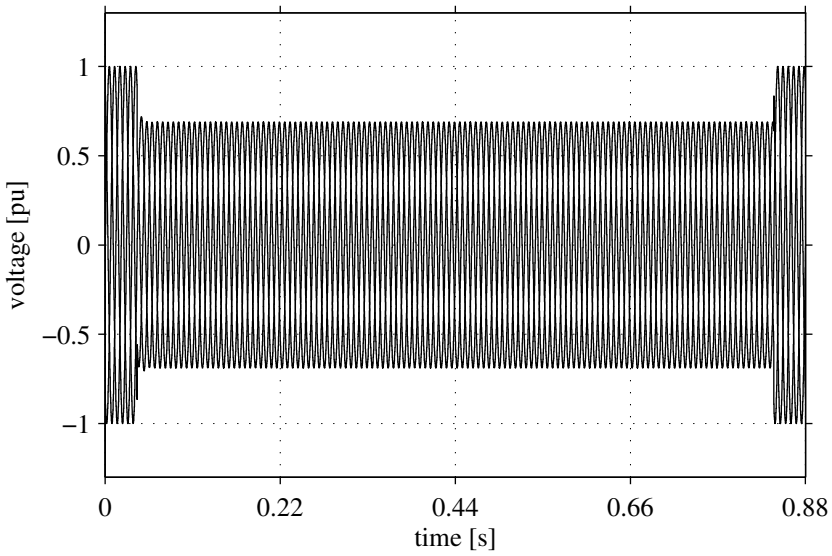


Fig. 5.56 Simulated three-phase grid voltages during balanced voltage dip with 10° phase-angle jump.

As shown in Fig.5.58, where the load voltage in the dq-coordinate system are displayed, the controller works properly and the load voltages are constant and equal to the pre-fault values in the positive and negative rotating coordinate system.

It is of interest to compare the current absorbed by the machine during the dip when the SSC is disconnected and when the SSC is online. Figure 5.59 displays the current observed by the induction machine during the voltage dip when the SSC is disconnected. As shown, when the dip starts, due to the back-emf of the machine and to the low leakage inductance, the machine starts to demand reactive power from the grid with a peak value of 1.8 pu at the end of the dip. Thus, the current absorbed by the machine decreases slowly to the rated value. When the SSC is on line, instead, (Fig.5.60), the load current remains constant at the pre-fault operating point (0.45 pu active power, 0.21 pu reactive power) also during the voltage dip. Only a small transient, due to the SSM, can be observed at the beginning and at the end of the dip.

Finally, it is possible to compare the speed of the machine when the SSC is online and when the compensator is disconnected from the mains. As shown in Fig.5.61, where the rotor speed in pu of the synchronous speed is depicted, when the machine is exposed to a voltage dip and the compensator is offline, the speed of the rotor decreases when reduced voltage is applied to its stator windings and then slowly goes back to the rated speed after that the fault has been cleared. If the SSC is online, the speed of the machine is instead constant and equal to 0.98 pu.

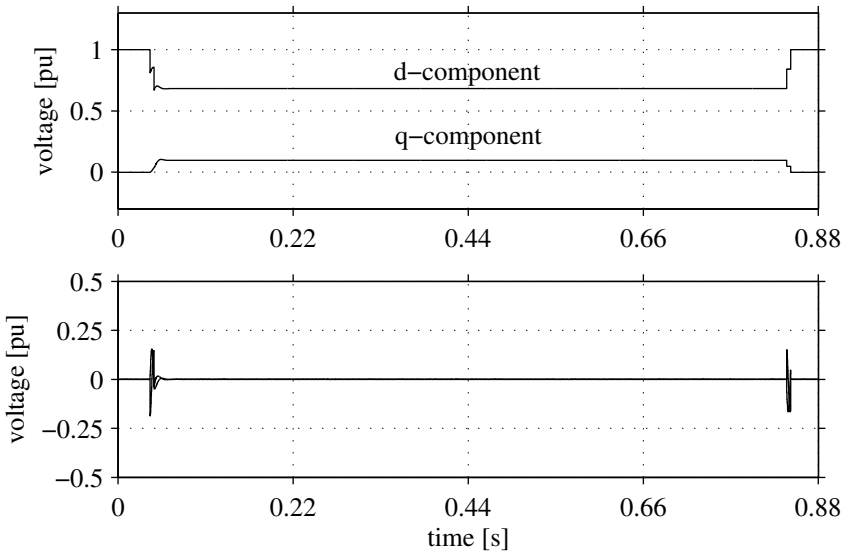


Fig. 5.57 Simulated grid voltages in dq-coordinate system during balanced voltage dip with 10° phase-angle jump. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

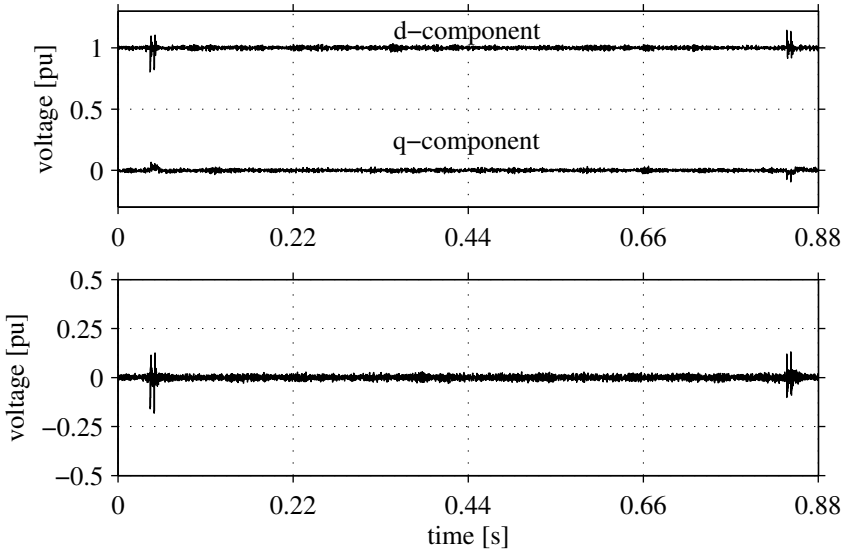


Fig. 5.58 Simulated load voltages in dq-coordinate system during balanced voltage dip with 10° phase-angle jump. DVC3 and induction machine load are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

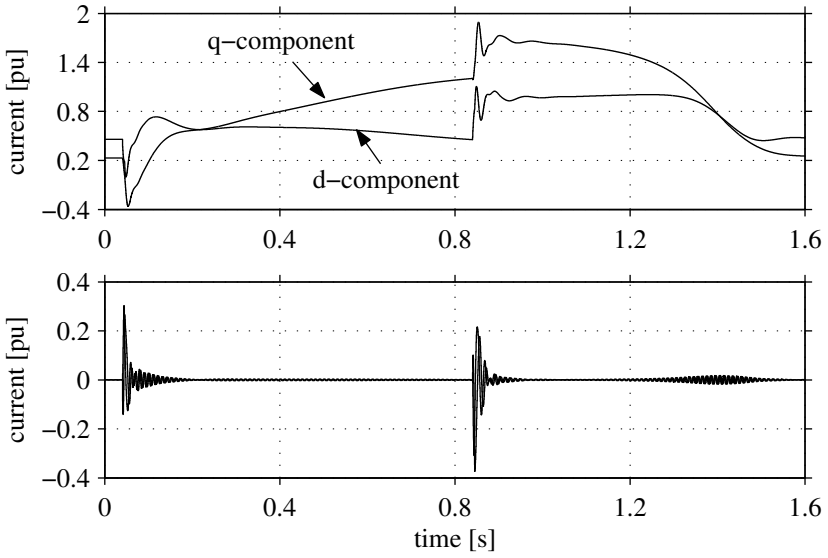


Fig. 5.59 Simulated load currents in dq-coordinate system during balanced voltage with 10° phase-angle jump. Induction machine load is used. SSC disconnected. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

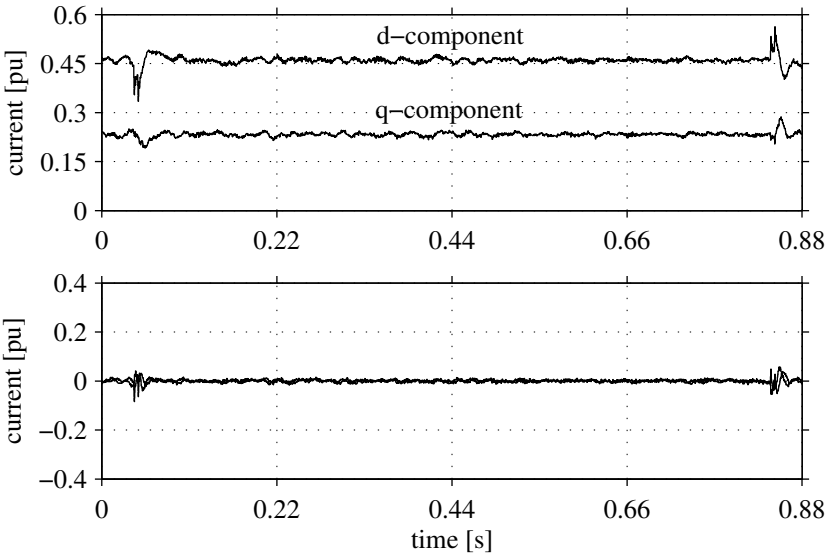


Fig. 5.60 Simulated load currents in dq-coordinate system during balanced voltage dip with 10° phase-angle jump. DVC3 and induction machine load are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

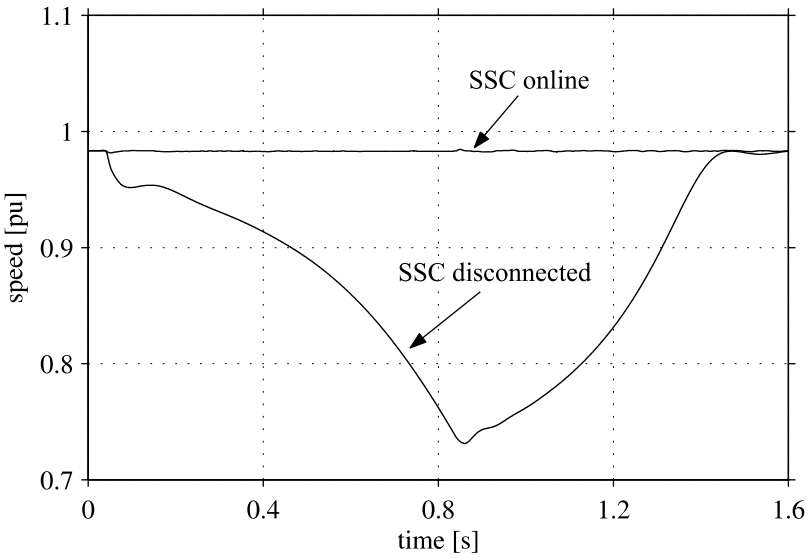


Fig. 5.61 Simulated machine speed response to balanced voltage dip with 10° phase-angle jump. DVC3 is used.

5.5.2 Summary

In this section, the principle of operation of the DVC3, based on two cascade controllers implemented in the positive and in the negative SRF, has been explained. It has been shown through simulations results that by controlling both the positive and the negative sequences of the filter current and of the capacitor voltage, a satisfactory performance of the control system when mitigating balanced and unbalanced voltage dips can be achieved. Simulations results show that the SSC presents high performance also when protecting different type of loads.

5.6 Conclusions

In this chapter, a cascade controller for SSC to mitigate voltage dips has been derived. An extended analysis of the control system and the interaction between the inner controller and the outer controller has been carried out. The problem with saturation of the injection transformer during voltage dip mitigation operations and several solutions have been discussed. Three different control systems for SSC have been investigated and compared under balanced and unbalanced voltage dips. It has been demonstrated that using dual vector-controller type 1 (DVC1), designed by only considering the positive-sequence components of the measured signals, the SSC is able to mitigate only balanced voltage dips. However, under unbalanced voltage dips, the controller is able to mitigate the dip but the load voltage results unbalanced. A way to deal with the problem of unbalanced voltage dips is to feed to the same controller only the positive-sequence components of the capacitor voltage and of the reference voltage, while the negative reference voltage is directly added to the reference voltage output of the current controller. By using this control system, called dual vector-controller type 2 (DVC2), it has been shown that

the SSC is able to mitigate also unbalanced voltage dips. However, the performance of the controller is related to the size of the filter capacitor. Since deadbeat gain for the current controller can be used, the DVC2 can be considered as a suitable solution for SSC when fast restoration of the load voltage is required and when the use of a small filter is allowed. Finally, the dual vector-controller type 3 (DVC3), based on two cascade controllers implemented in the positive and in the negative SRF, has been presented. It has been demonstrated that the DVC3 presents high performance when mitigating balanced and unbalanced voltage dips for different type of loads. Due to the use of DVCC, thus the necessity of reduce the bandwidth of the controller, the DVC3 presents a slower response compared with DVC2, however it ensures a good mitigation of the voltage dip, regardless of the size of the filter capacitor and of the percentage of unbalance of the dip.

Chapter 6

Experimental results using series-connected VSC

6.1 Introduction

To validate the results obtained via simulation in the previous chapter, the DVC1, DVC2 and DVC3 have been tested experimentally under balanced and unbalanced voltage dips. In this chapter, a description of the laboratory setup and of the protection system used for these tests will be carried out. Finally, experimental results for all three different control systems will be presented.

6.2 Laboratory setup

A single-line diagram of the laboratory setup of the SSC is displayed in Fig.6.1. The VSC has been connected to the network model, described in Section 4.2, through an LC-filter and three single-phase transformers, used to inject the required missing voltage in the mains during the dip. Parameters of the implemented system are displayed in Table 5.1. To avoid overvoltage due to Ferranti effect, the network model has been loaded using a three-phase resistor of 17.8 Ω, corresponding to 9 kW. In order to generate voltage dips in the grid, an additional variable resistance can be inserted in the network model by closing with a timer the contactor denoted in Fig.6.1 as contactor 3. The load protected by the SSC is a three-phase resistor of 8.8 Ω, corresponding to 18 kW. The protection system depicted in Fig.6.1 is further explained in Section 6.3.

As in Section 4.2, all experiments have been carried out with a fixed DC-link voltage by using a DC machine rated 700 V, 60 A. A picture of the actual laboratory setup in the Power System Laboratory is depicted in Fig.6.2.

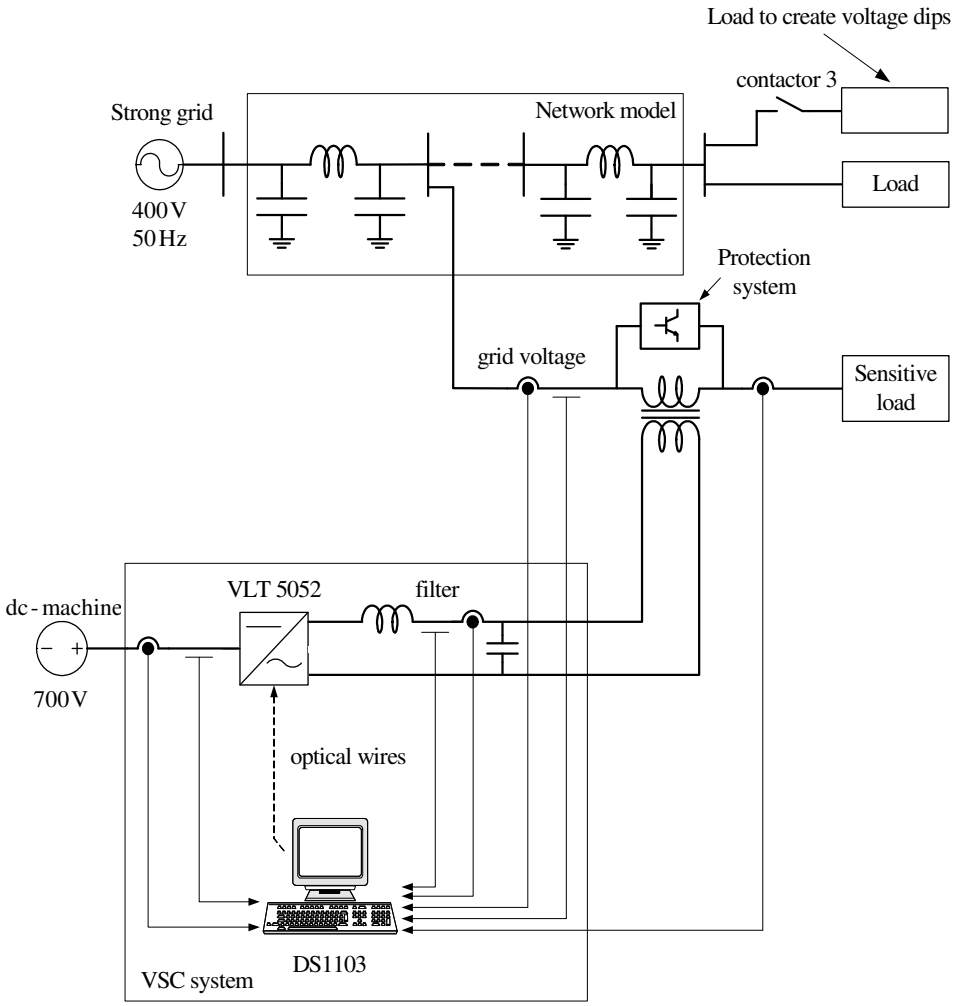


Fig. 6.1 Single-line diagram of laboratory setup of SSC.

Fig. 6.2 Photo of laboratory setup.

6.3 Protection system

In this section, the system for protection of the SSC against downstream fault is described. This system is also used for the start-up of the SSC.

The major complication for protection of the VSC in the series connection is that the fault current flowing in the primary winding of the injection transformer due to a downstream fault will be reflected to the secondary side with at least the same magnitude (in a real installation, where the transformer steps down the voltage, it will be even higher on the converter side). This overcurrent can break the valves of the VSC. Even though the VSC is blocked, the current will flow through the diodes and the DC-link voltage will quickly increase, destroying the valves of the VSC. The solution is to provide an alternative path to the fault current to avoid it to flow into the VSC. Also, the protection system should not disconnect the load during the fault, as the feeder protection should take care of this.

Figure 6.3 shows a single-line diagram of the SSC with the protection system, which consists of an IGBT-based crowbar that bypasses the injection transformers if overcurrent occurs in the grid.

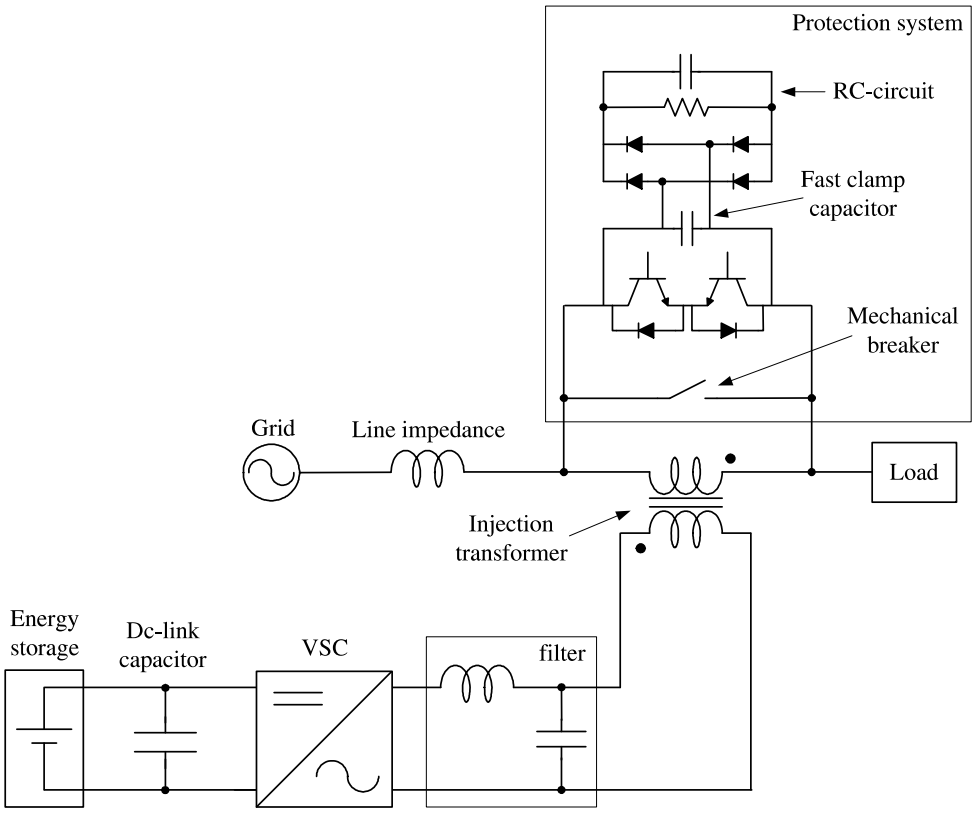


Fig. 6.3 Single-line scheme of grid, SSC and protection system.

If the grid current exceeds a pre-defined threshold, an analog logic commands the mechanical breaker to close. Since the breaker will not respond sufficiently quickly, the same signal is sent to close two IGBTs in series, connected in parallel with the breaker. The IGBTs close first but

provide a path of comparatively high resistance so that, when the breaker closes, it takes over most of the current, thus relieving the IGBTs of the high current and decreasing the cooling requirements. Moreover, the mechanical breakers provide an alternative path if the IGBTs fail to close. The closing time of the IGBTs has been set to 100 ns. At this high speed, the main risk during switching is represented by the inductance of the cables, causing an overvoltage due to the high $\mathrm{d}i/\mathrm{d}t$ during switching, which can destroy the IGBTs in the crowbar. The same problem arises when the IGBTs open. To overcome these overvoltages, a snubber circuit is needed. The first steep flank of the overvoltage is absorbed by a fast polypropylene clamp capacitor directly mounted across the IGBTs by using copper stripes to provide a low-inductance connection. This capacitor must be very small to present a high-reactance impedance path to normal operation currents. Lower-frequency overvoltages are taken care of by an RC-circuit connected to the IGBTs through a single-phase diode rectifier, to dissipate the exceeding energy. This is "trapped" in the capacitance and later released and dissipated in the parallel resistance. The diode rectifier ensures that the discharge current cannot flow back to the feeder.

To verify the effectiveness of the snubber, the crowbar has been connected to a DC-current source through a 1 m long cable. The current flowing through the IGBTs of the crowbar is equal to 0.2 pu. After 4 μs, the current has been interrupted by opening the IGBTs. Figures 6.4 and 6.5 show the current through the IGBTs and the voltage across them with and without snubber, respectively. Without snubber, due to the fast variation of the current in the cable inductances the voltage across the IGBTs is affected by a 0.6 pu overshoot lasting for 2 μs, while with the snubber in the crowbar the overvoltage is reduced to 0.04 pu. It is possible to observe that, after the first overshoot, due to the presence of capacitors in the snubber circuit the voltage takes 28 μs to reach the steady-state. A picture of the actual crowbar is shown in Fig.6.6.

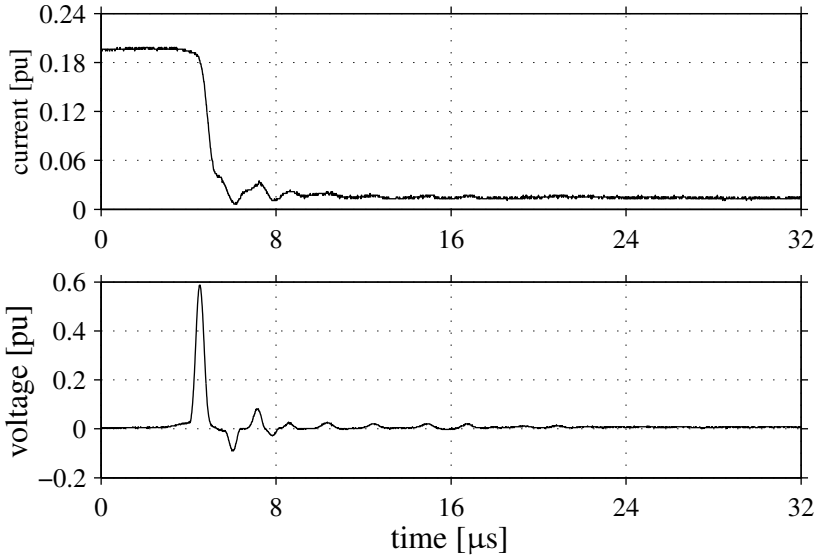


Fig. 6.4 Measured transient due to switching of IGBTs in crowbar without snubber. Top: current through IGBTs; bottom: IGBTs voltage.

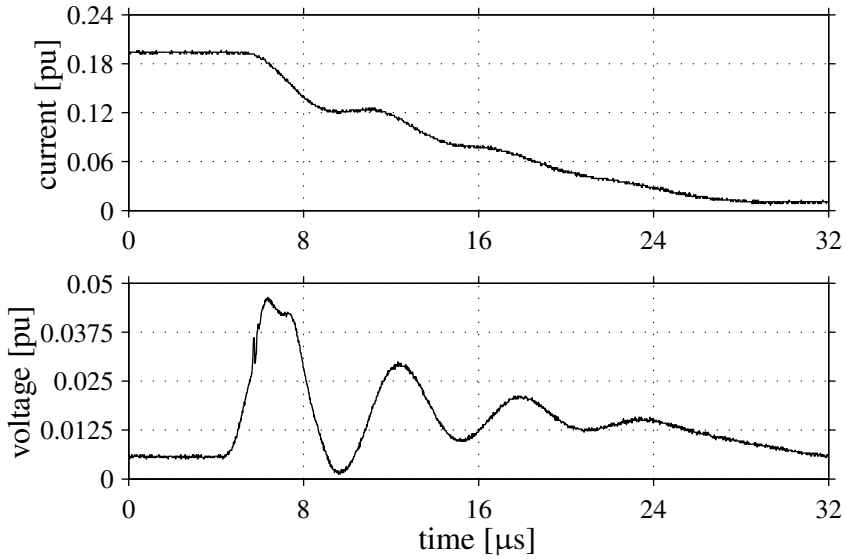


Fig. 6.5 Measured transient due to switching of IGBTs in crowbar with snubber. Top: current through IGBTs; bottom: IGBTs voltage.

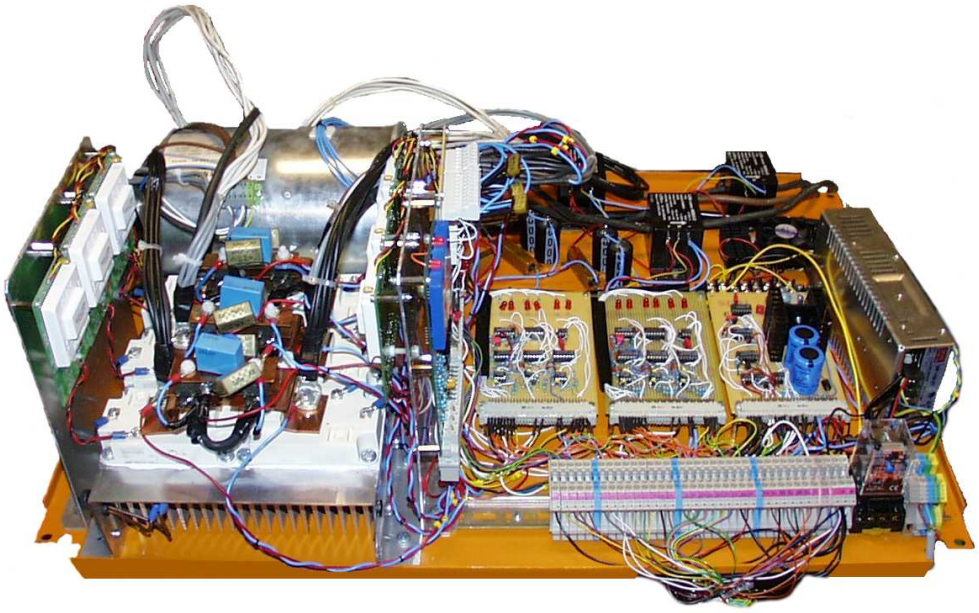


Fig. 6.6 Photo of crowbar for SSC protection.

6.4 Experimental results using DVC1

In order to validate the results obtained via simulation in Section 5.3.4, the DVC1 has been tested in the laboratory under balanced and unbalanced voltage dips. Controller parameters for the DVC1 are displayed in Table 5.2. In the following, the experimental results will be presented.

6.4.1 Balanced voltage dips

A first set of tests has been carried out when the grid voltage is affected by a balanced voltage dip. To generate a voltage dip in the mains, at $t = 0.03$ s three star-connected resistances of $2.1\,\Omega$ each have been connected to the network model by closing contactor 3 in Fig.6.1 for 300 ms. As a result, the grid voltage at PCC was affected by a 71% symmetrical voltage dip, as shown in Fig.6.7 (three-phase waveforms) and Fig.6.8 (dq-coordinate system). From the latter, it can be noticed that the q-component of the grid voltage is affected by a transient at the beginning and at the end of the dip. This is due to the phase-angle jump associated with the dip and to the response time of the PLL, which takes about 0.03 ms to lock into the new angle of the voltage vector, as explained in Chapter 4. However, after this transient, the q-component of the voltage is constant and equal to zero. The grid voltage in the dq-coordinate system is not perfectly flat, but shows a small ripple, due to the harmonics present in the grid voltage.

Figure 6.9 shows the measured capacitor voltage in the dq-coordinate system. Before and after the dip the capacitor voltage is approximately zero. When the voltage dip occurs, the d-component makes a step of 0.245 pu, while the q-components remains constant to zero, except for the transient at the beginning and at the end of the dip.

The current in the filter reactor is displayed in Fig.6.10. The operating point is 0.6 pu d-component and 0 pu q-component. At $t = 0.03$ s, the q-component makes a step up of 0.05 pu, while the d-component remains constant at the pre-fault value. The characteristic current overshoot at the beginning and at the end of the dip seen from the simulation results is also evident here.

The SSC mitigates the voltage dip and keeps the load voltage to the pre-fault value, as shown by the three-phase waveform of the load voltage in Fig.6.11 and by the dq-components of the load voltage shown in Fig.6.12. Only a small transient at the beginning and at the end of the voltage dip can be noticed, which is also evident in Fig.6.13, showing the error of the load voltage magnitude during the dip. Compared with the results obtained via simulation (see Figs.5.21 to 5.23), the transient at the beginning and at the end of the dip is 0.7 pu, i.e. it is reduced by 40% compared with the simulated value. As already explained in Section 4.3.3, this is due to the presence of capacitors in the network model, which provide a smoother variation of the grid voltage.

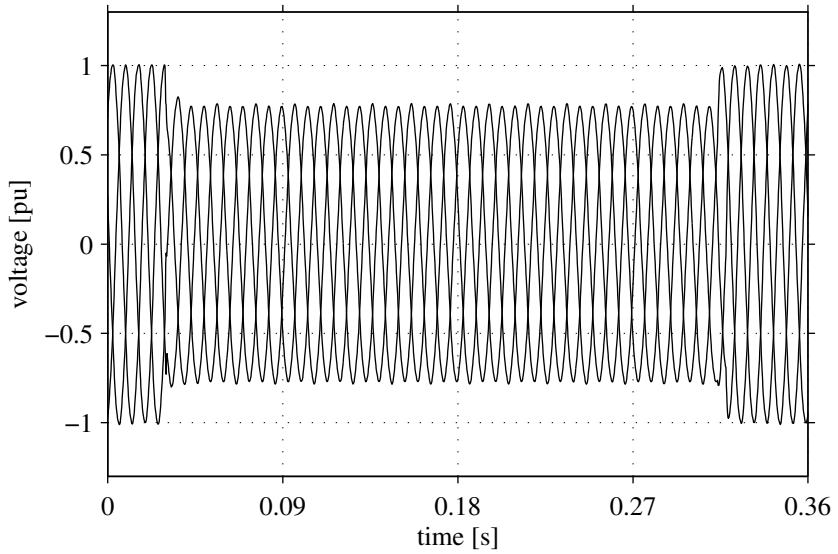


Fig. 6.7 Measured three-phase grid voltage during balanced voltage dip.

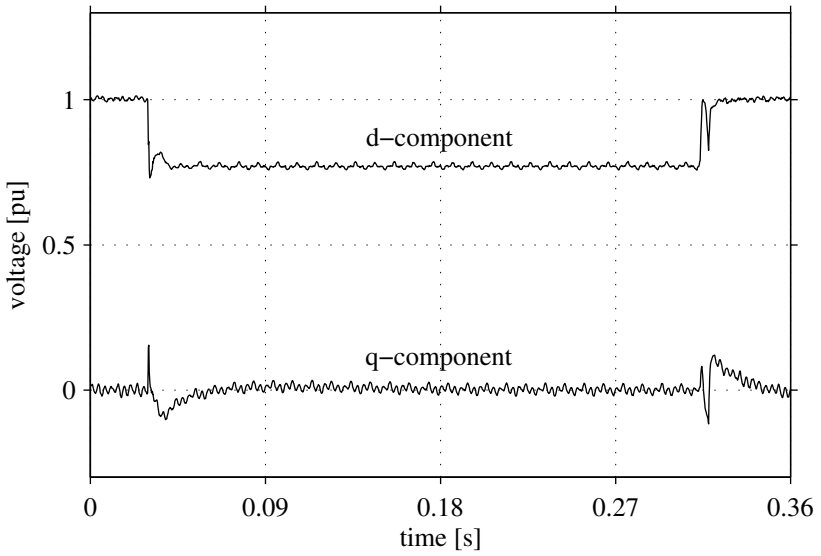


Fig. 6.8 Measured grid voltage in dq-coordinate system during balanced voltage dip. DVC1 is used.

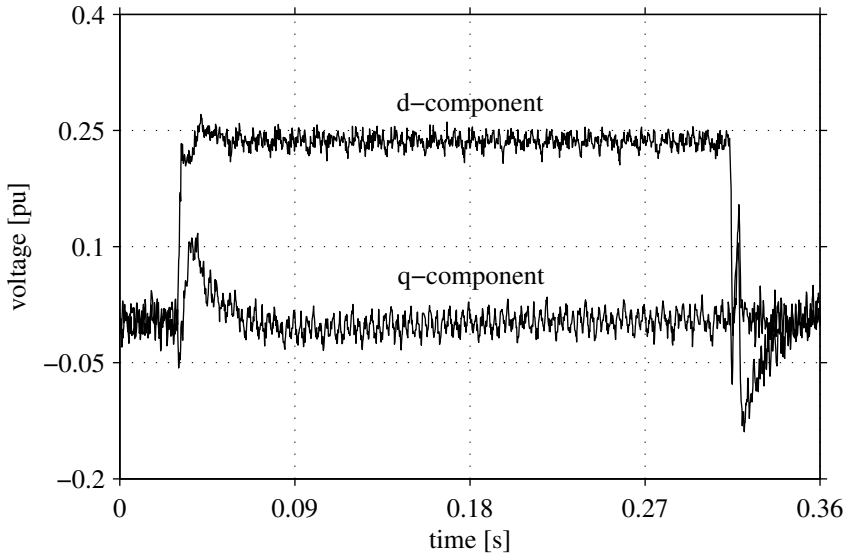


Fig. 6.9 Measured dq-components of capacitor voltage during balanced voltage dip. DVC1 is used.

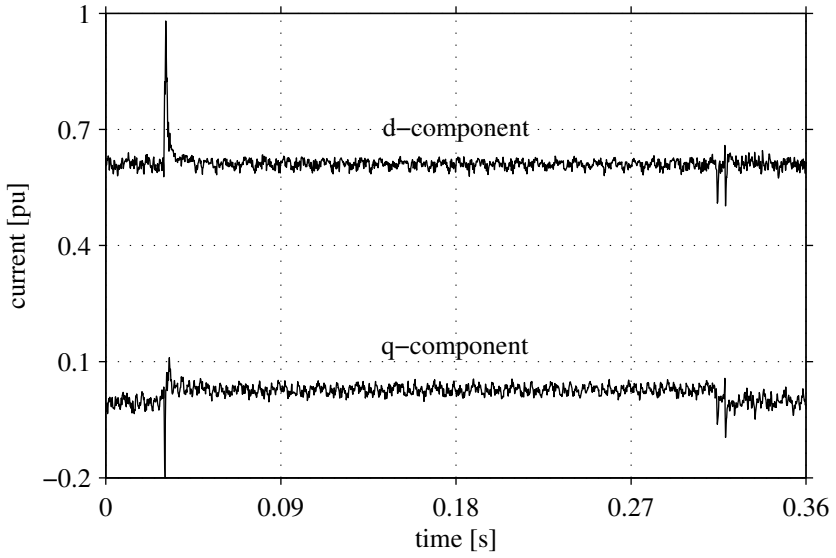


Fig. 6.10 Measured response of d- and q-component of filter reactor current to balanced voltage dip. DVC1 is used.

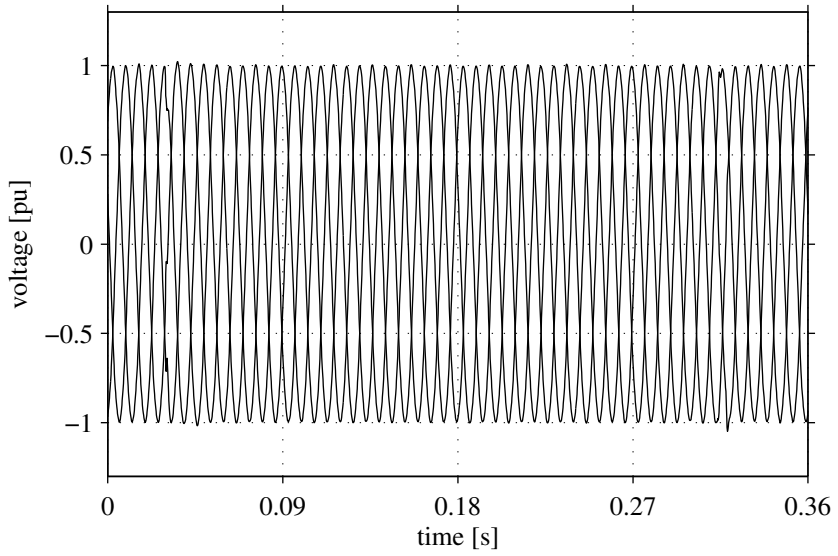


Fig. 6.11 Measured three-phase load voltage. DVC1 and balanced voltage dip are used.

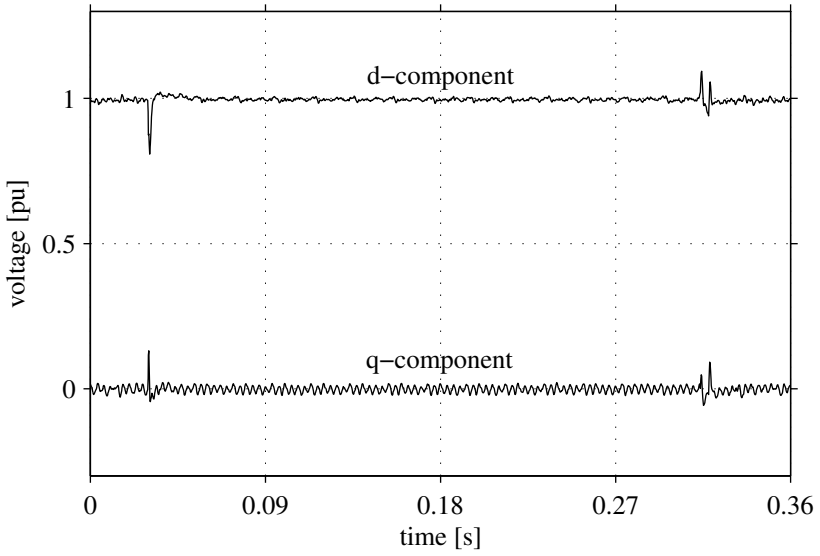


Fig. 6.12 Measured load voltage in dq-coordinate system. DVC1 and balanced voltage dip are used.

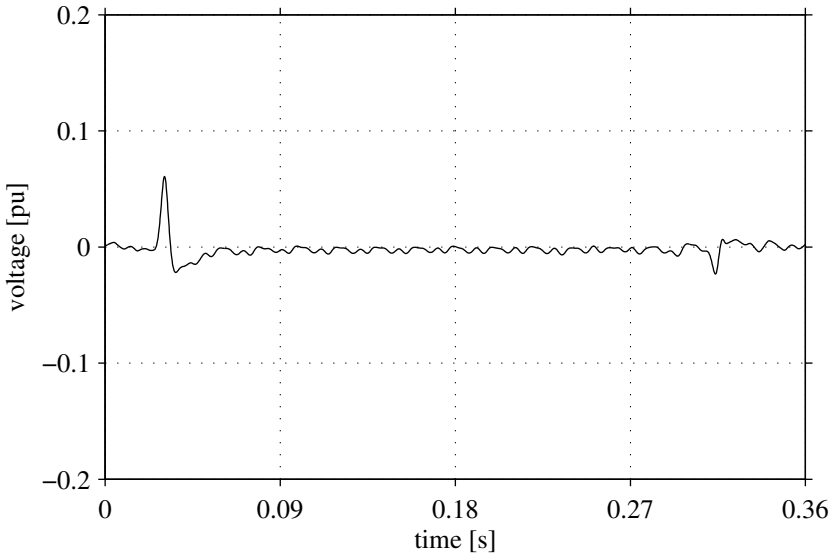


Fig. 6.13 Measured error of load voltage magnitude during balanced voltage dip. DVC1 is used.

6.4.2 Unbalanced voltage dips

The step response of the DVC1 has also been tested under unbalanced voltage dips. To generate an unsymmetrical dip in the mains, at $t = 0.03$ s an additional resistance of 4.2 Ω has been connected between phases b and c for 300 ms by closing contactor 3. The unbalanced current circulating in the first π-section of the network model in Fig.6.1 creates the three-phase voltage waveforms displayed in Fig.6.14. Phases b and c drop from 1 pu to 0.8 pu and 0.7 pu, respectively, while phase a remains constant to 1 pu. The retained positive-sequence voltage is 85% and the unbalance is 10.9%. Due to the unbalance, the grid voltages in the dq-coordinate system, shown in Fig.6.15, are affected by a 100 Hz oscillation with an amplitude of 0.2 pu (peak-to-peak).

The oscillations in the dq-components of the grid voltage during the dip will also affect the capacitor voltage. In agreement with the simulation results, the SSC tries to restore the load voltage by injecting a voltage into the mains but the capacitor voltage (and thus also the injected voltage) oscillates also with 100 Hz, as shown in Fig.6.16.

As a result, the load voltage is partially restored to the pre-fault value but is still unbalanced during the voltage dip, as shown by the three-phase waveforms in Fig.6.17 and by the corresponding dq-components in Fig.6.18. Figure 6.19 shows the error of the load voltage magnitude, which obviously oscillates with 100 Hz.

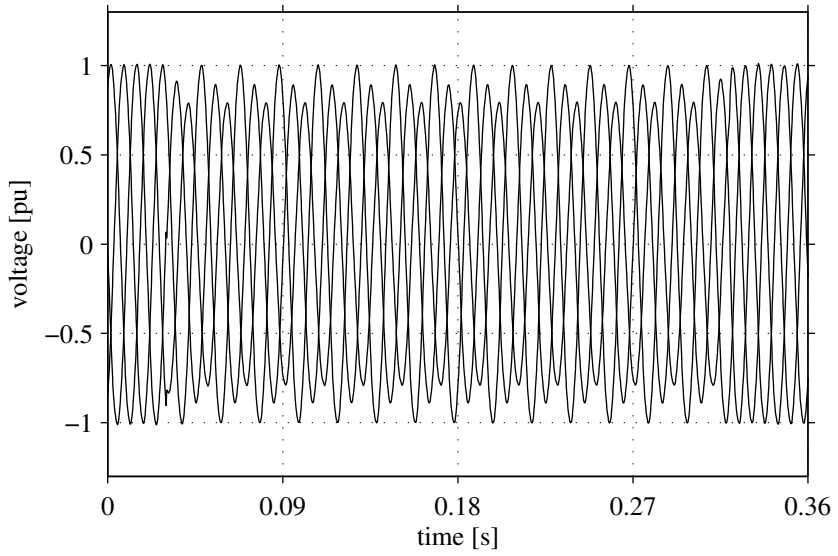


Fig. 6.14 Measured three-phase grid voltages during unbalanced voltage dip.

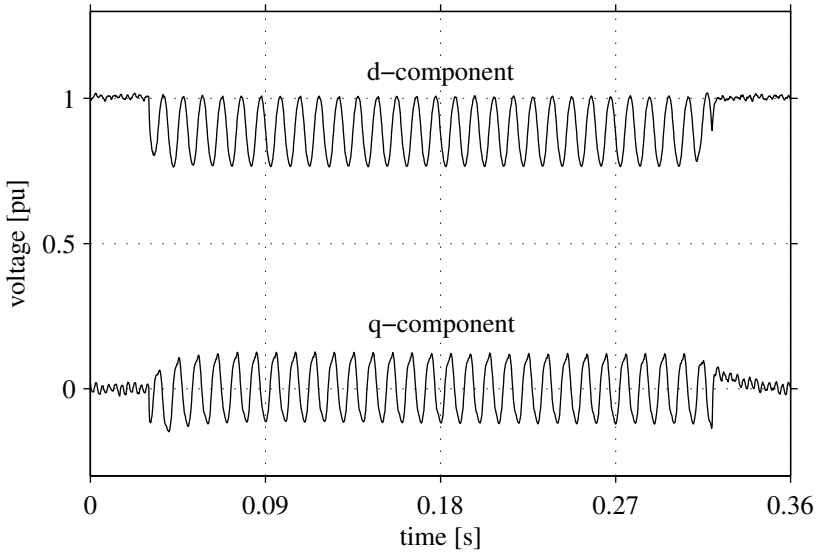


Fig. 6.15 Measured grid voltage in dq-coordinate system during unbalanced voltage dip. DVC1 is used.

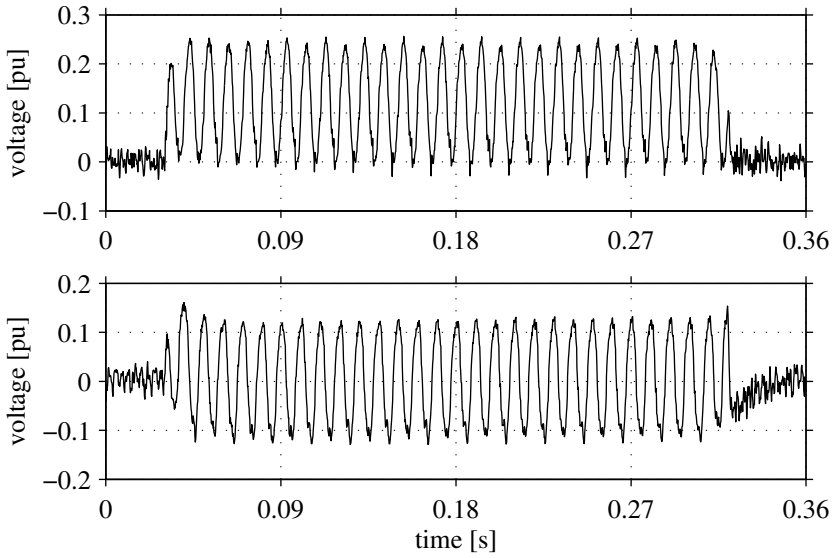


Fig. 6.16 Measured response of capacitor voltage to unbalanced voltage dip. DVC1 is used. Top: d-component; bottom: q-component.

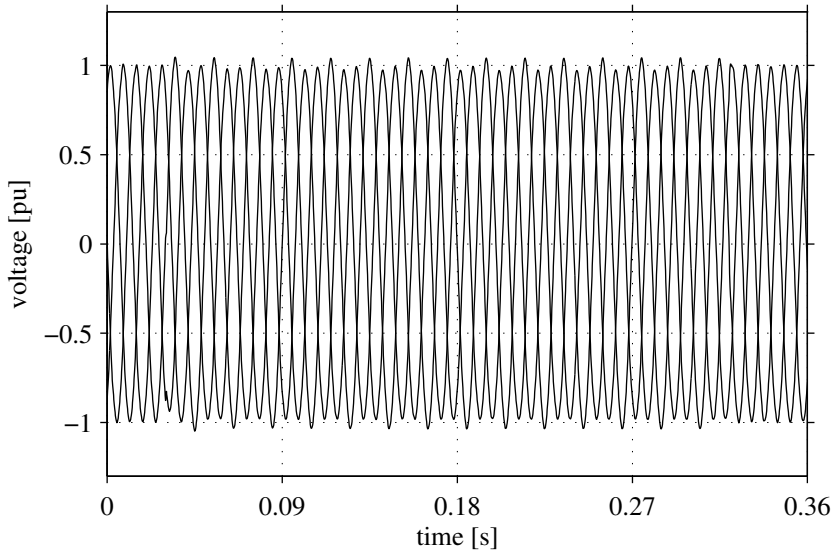


Fig. 6.17 Measured three-phase load voltage. DVC1 and unbalanced voltage dip are used.

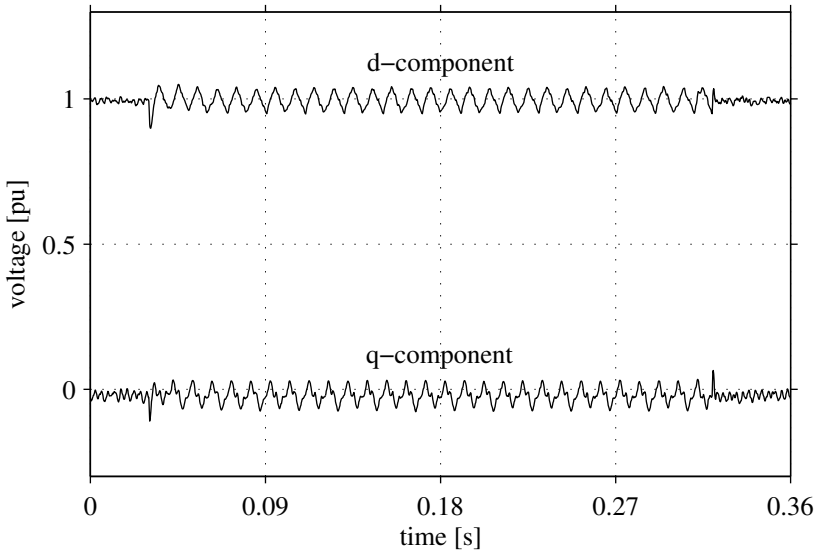


Fig. 6.18 Measured load voltage in dq-coordinate system. DVC1 and unbalanced voltage dip are used.

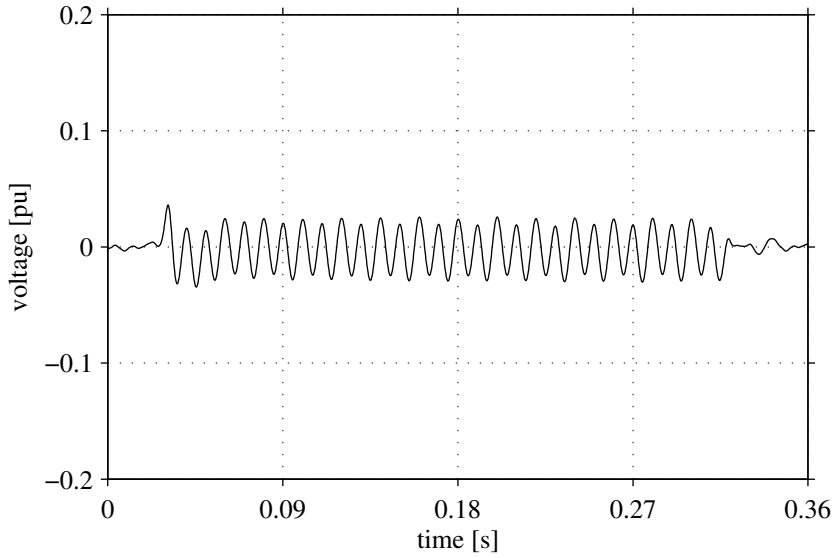


Fig. 6.19 Measured error of load voltage magnitude during unbalanced voltage dip. DVC1 is used.

6.5 Experimental results using DVC2

In this section, the experimental results for SSC with DVC2 under unbalanced voltage dips will be presented. Controller parameters for DVC2 are displayed in Table 5.2.

6.5.1 Unbalanced voltage dips

The dynamic performance of DVC2 has been tested with the same unbalanced voltage dip shown in Fig.6.14. The corresponding sequence components detected by the control system using DSC are shown in Fig.6.20 to be constant in the corresponding SRFs before the dip. When the dip occurs, the positive-sequence d-component makes a step down to 0.85 pu. The dq-components of the negative sequence are both equal to zero before and after the dip. They are equal to 0.11 pu and -0.05 pu, respectively, during the unbalanced voltage dip.

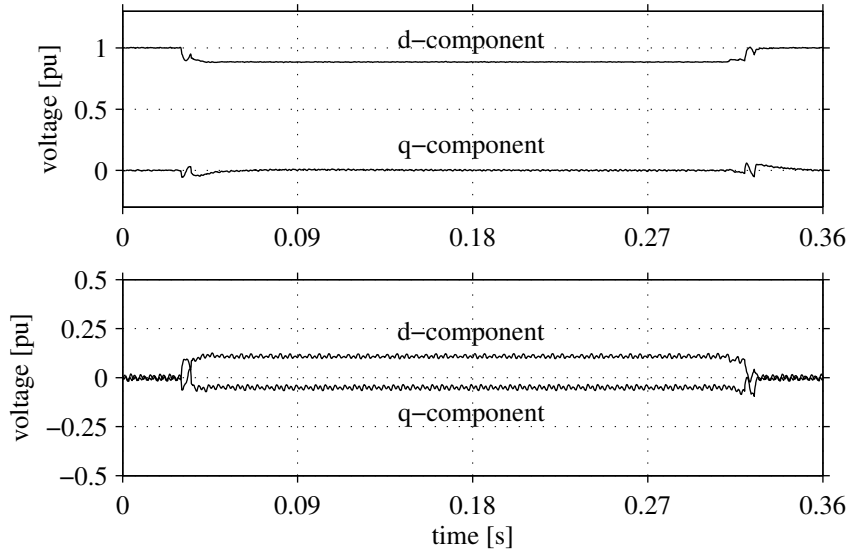


Fig. 6.20 Measured grid voltage in dq-coordinate system during unbalanced voltage dip. DVC2 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

Measured sequence components of the capacitor voltage are displayed in Fig.6.21. Both positive and negative sequence are equal to zero before and after the dip. When the dip occurs, the d-component of the positive sequence goes from 0 pu to 0.11 pu. The uncontrolled negative sequence components step to 0.05 pu q-component and -0.11 pu d-component, i.e. the control system reacts to the unbalanced grid voltage by trying to inject into the mains a negative sequence voltage equal to the negative sequence of the grid voltage but opposite in sign.

Figures 6.22 and 6.23 display the three-phase load voltages and its sequence components, respectively. As shown, the load voltage is restored to 1 pu but it is still slightly unbalanced due to the uncontrolled injection of negative-sequence voltage into the mains by the SSC. However, due to the small unbalance of the voltage dip, the error in the load voltage magnitude, displayed in Fig.6.24, is very small (0.01 pu, peak-to-peak), i.e. about one third of the error obtained via

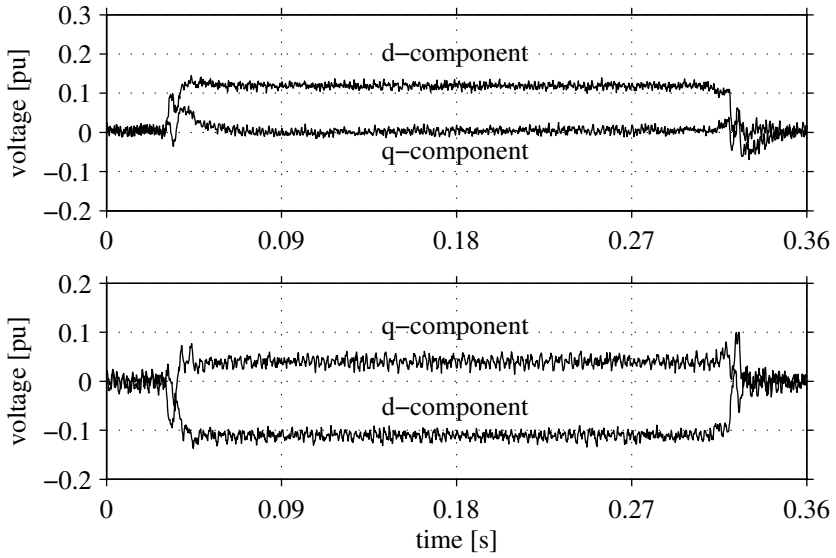


Fig. 6.21 Measured dq-components of capacitor voltage with unbalanced voltage dip. DVC2 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

simulation and displayed in Fig.5.36. This is due to the lower unbalance of the voltage dip, due to practical limitations in the laboratory.

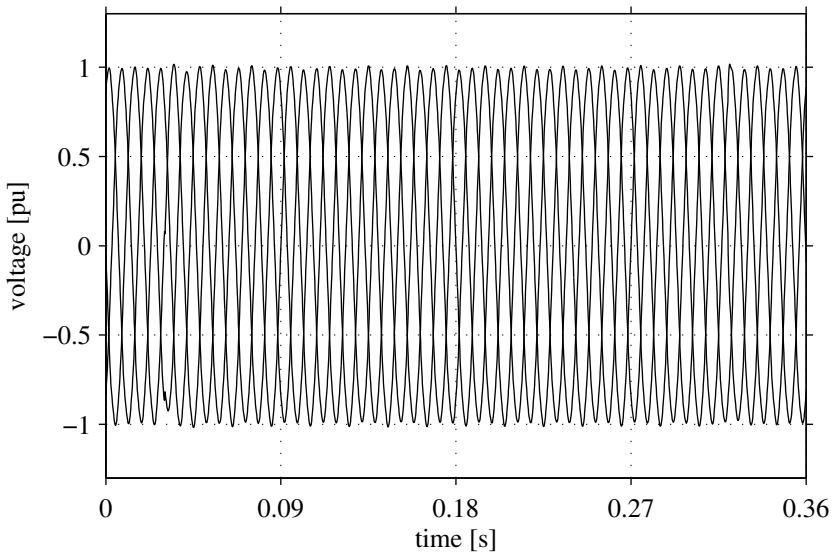


Fig. 6.22 Measured three-phase load voltage. DVC2 and balanced voltage dip are used.

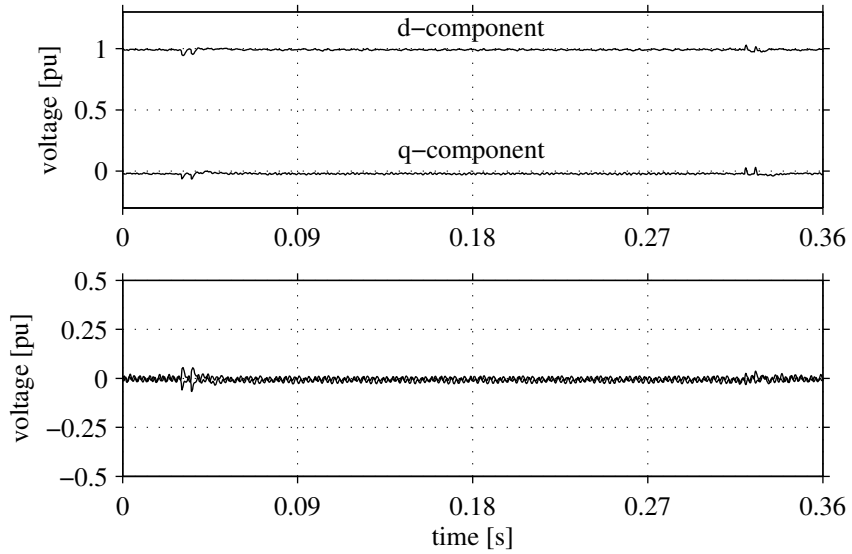


Fig. 6.23 Measured load voltage in dq-coordinate system. DVC2 and unbalanced voltage dip are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

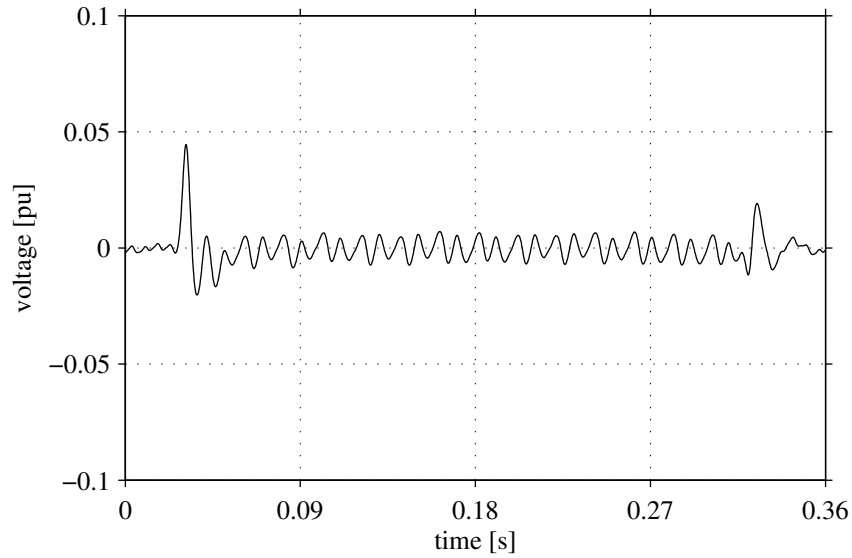


Fig. 6.24 Measured error of load voltage magnitude during unbalanced voltage dip. DVC2 is used.

6.6 Experimental results using DVC3

Finally, in this section experimental results for the SSC with DVC3 will be presented. The controller has been tested in the laboratory under unbalanced voltage dips. Moreover, the dynamic performance of the SSC with DVC3 when protecting a diode rectifier load will be shown. Controller parameters for DVC3 are displayed in Table 5.3.

6.6.1 Unbalanced voltage dips

In this first set of experimental results, the DVC3 has been tested under unbalanced voltage dips when protecting a pure resistive load. To compare the performance of DVC3 with DVC2, the system has been tested under the same unbalanced voltage dip (see Fig.6.14 and Fig.6.20).

As shown in Fig.6.25, the operating point for the filter current is 0.6 pu d-current and 0 pu q-current for the positive sequence, and 0 pu for both components of the negative sequence. When the dip occurs in the grid, due to the reduced voltage at the PCC, the VSC currents change to opportunely charge the filter capacitor. The positive-sequence q-current and the negative-sequence d-current make a small step up of 0.05 pu and 0.02 pu, respectively, while the other components remain constant at the pre-fault values.

Figure 6.26 shows the step response of positive and negative sequence of the capacitor voltage. In steady state, before and after the dip, all components are approximately equal to zero. During the dip, the d-component of the positive sequence goes to 0.12 pu, while the d- and q-component of the negative sequence go to -0.1 pu and 0.05 pu, respectively.

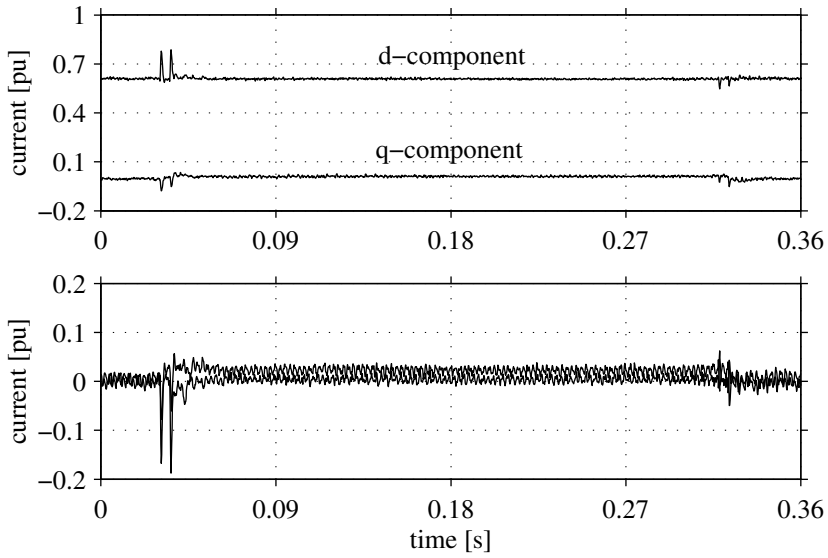


Fig. 6.25 Measured response of filter reactor current to unbalanced voltage dip. DVC3 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

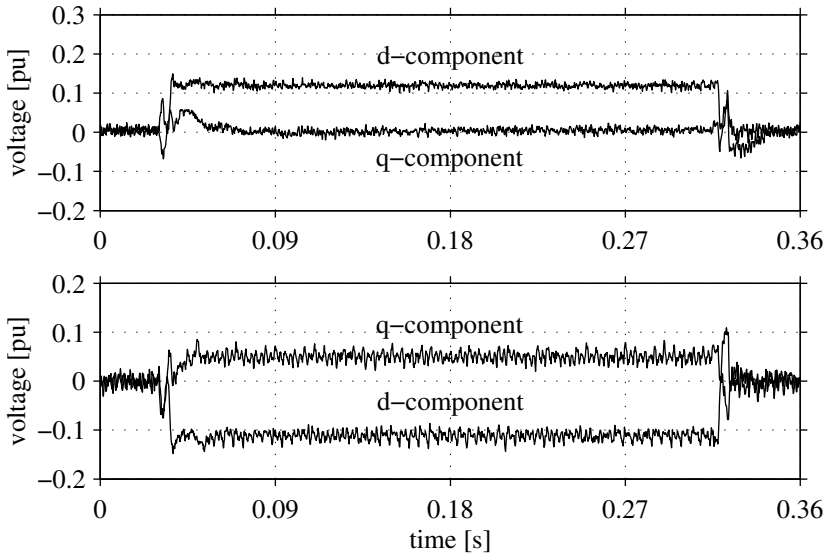


Fig. 6.26 Measured response of capacitor voltage to unbalanced voltage dip. DVC3 is used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

The load voltage is depicted in Fig.6.27 (three-phase waveforms) and Fig.6.28 (sequence components). The load voltage is restored to the pre-fault value with higher accuracy than DVC2, which can be seen in Fig.6.29, showing that the error of the load voltage magnitude is practically zero during mitigation. This confirms the results obtained via simulation and shown in Fig.5.45.

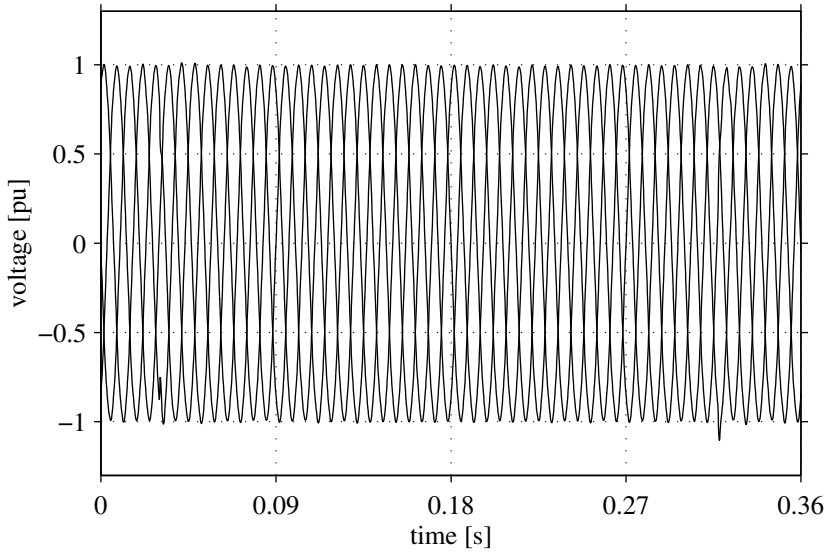


Fig. 6.27 Measured three-phase load voltage. DVC3 and unbalanced voltage dip are used.

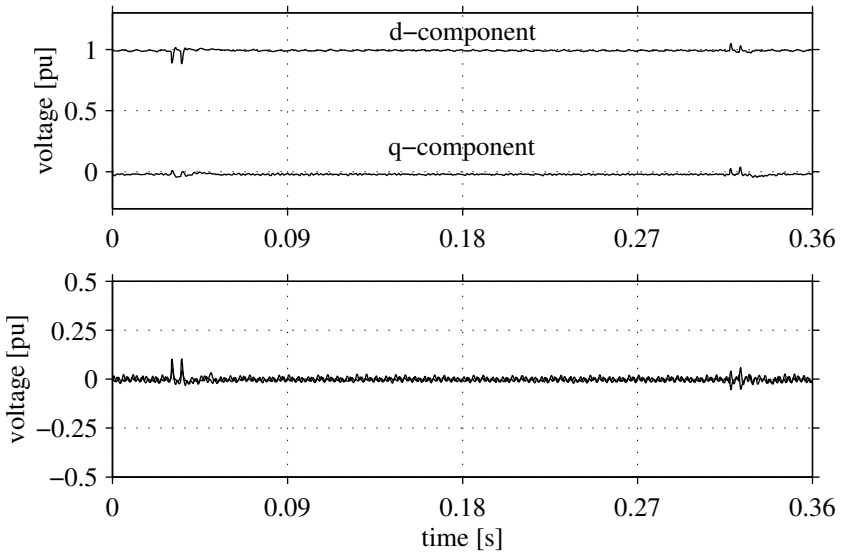


Fig. 6.28 Measured load voltage with DVC3 and unbalanced voltage dip are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

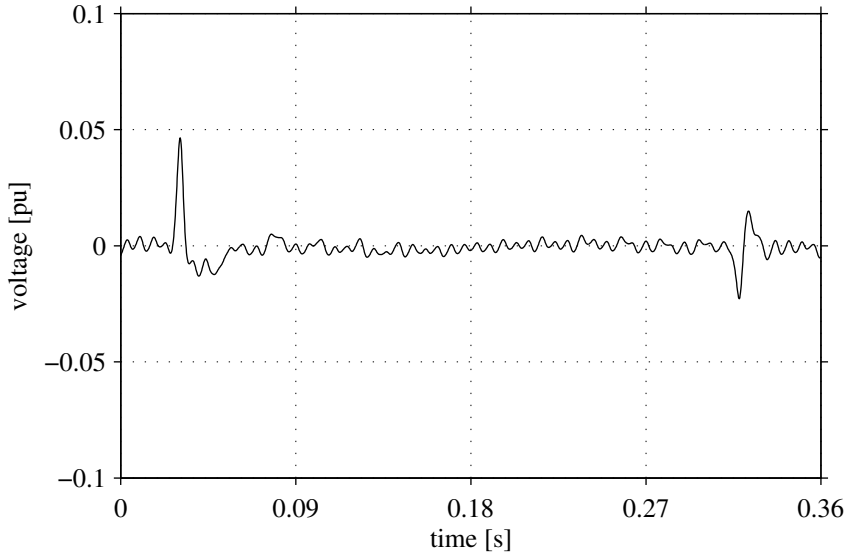


Fig. 6.29 Measured error of load voltage magnitude during unbalanced voltage dip. DVC3 is used.

6.6.2 Diode rectifier load

The DVC3 has also been tested under balanced voltage dips when protecting a diode rectifier load. As shown in Fig.5.46, the diode rectifier has been connected downstream the injection transformer through a smoothing inductance of 3 mH. To smooth the voltage on the DC side of the diode rectifier, a capacitor of 300 μF has been used.

The distorted current circulating in the first π-section of the network model creates the voltage waveforms displayed in Fig.6.30. At $t = 0.03$ s the contactor 3 is closed for 300 ms to connect

three star-connected resistances and, as a result, the grid voltage is affected by a 70% voltage dip, which can also be seen in Fig.6.31, showing the grid voltage in the dq-coordinate system.

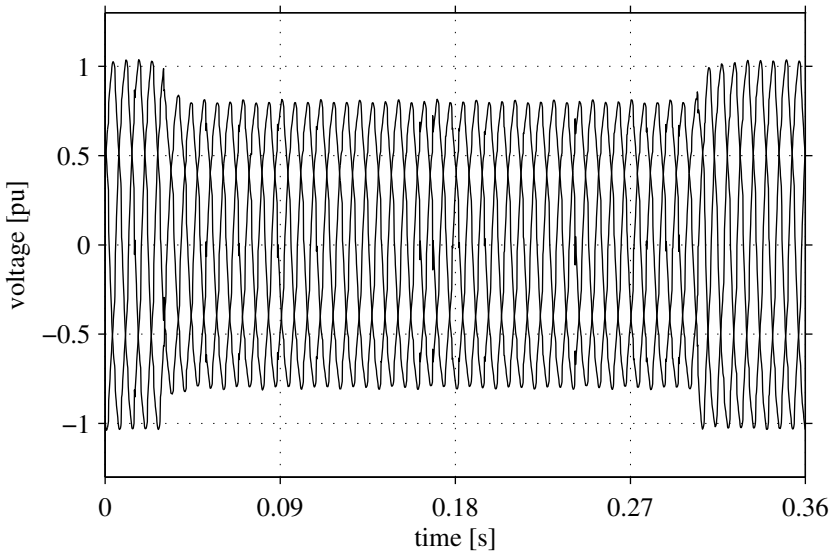


Fig. 6.30 Measured three-phase grid voltage during balanced voltage dip with diode rectifier load.

The three-phase grid current displayed in Fig.6.32 shows that the current drawn from the diode rectifier is highly distorted. The current THD is 26%.

Figure 6.33 shows the three-phase load voltage, which appears to be perfectly compensated. The dip can hardly be noticed as there is only one very short transient at the beginning and at the end of the dip. However, the load voltage is affected by low-order harmonics and has a THD of 6.7%. The distortion is also evident as a ripple of the sequence components shown in the respective dq-frames in Fig.6.34. However, the error of the load voltage magnitude, which is plotted in Fig.6.35, shows that the compensation is very accurate. Note that the error has been filtered to reduce harmonics and noise, because the main concern is to show the compensation capability for the fundamental voltage.

Figures 6.36(a) to 6.36(d) show the harmonic content of the load current and voltage with and without the SSC. In general, the harmonic content of the load voltage is lower when the SSC is disconnected, which is in agreement with the simulation results, although, the harmonic content is higher compared with the simulated case (see in Fig.5.53(b)), due to the larger grid impedance. However, the 5^{th} harmonic is slightly higher when the SSC is disconnected, which is in contrast with the simulation results. The larger grid impedance will also affect the harmonic content of the load current. It can be observed that the current distortion is slightly lower when the SSC is online, which also confirms the simulation results. However, the difference compared to when the SSC is disconnected is lower than in the simulated case.

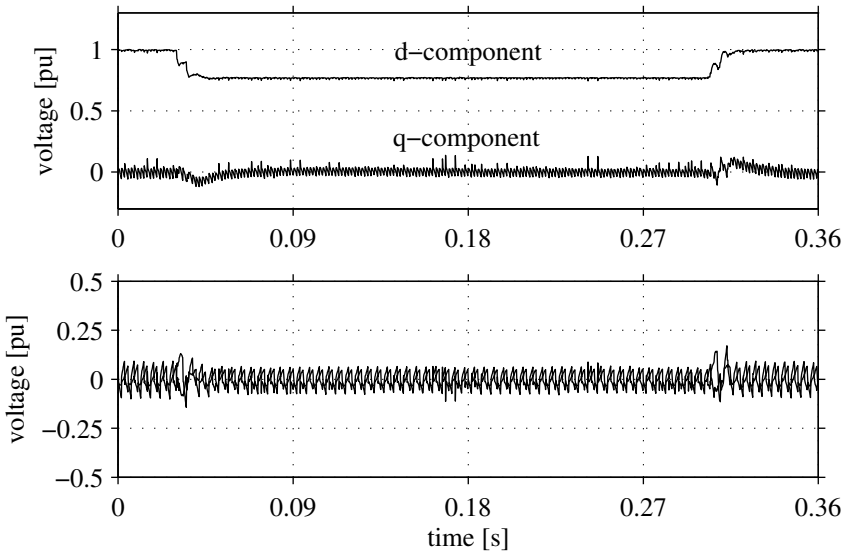


Fig. 6.31 Measured grid voltage in dq-coordinate system during balanced voltage dip. DVC3 and diode rectifier load are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

6.7 Conclusions

In this chapter, experimental results for SSC using DVC1, DVC2 and DVC3 have been presented. An extended description of the laboratory setup and of the protection system of the SSC against downstream short-circuits have been carried out. Experimental results for all three controllers confirm the results obtained via simulation. Due to practical limitations in the laboratory, the unbalance voltage dip tests had to be made with a limited unbalance. However, even in these conditions, it is clear that the mitigation capability is dramatically improved when choosing DVC2 or DVC3 as compared to DVC1. The difference between the other two controllers is harder to see when looking at the three-phase load voltage waveforms, which are in both cases very well compensated. However, the error of load voltage magnitude shows distinctly that there is a further improvement in the accuracy of the compensation when choosing DVC3. Finally, the results with DVC3 and diode rectifier load agree in general with the simulations presented in Chapter 5. Some minor differences are due to difficulties in modelling exactly the frequency characteristic of the grid impedance.

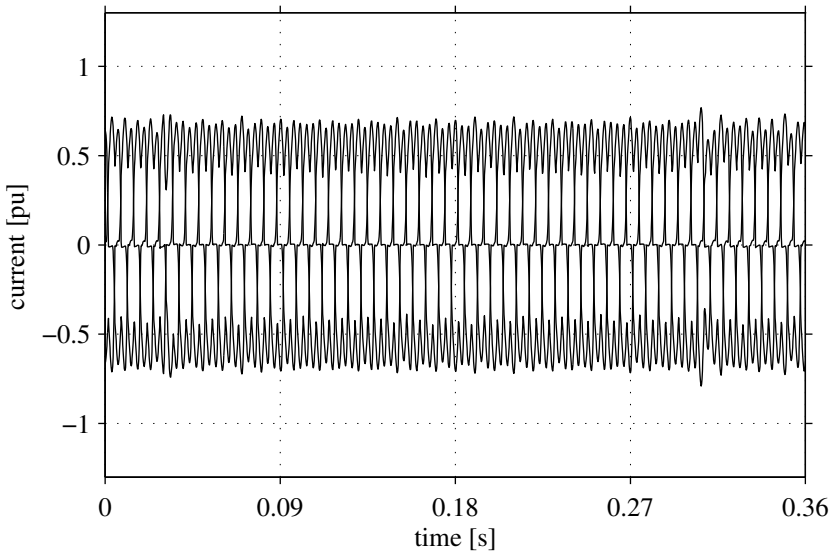


Fig. 6.32 Measured three-phase grid current during balanced voltage dip. DVC3 and diode rectifier load are used.

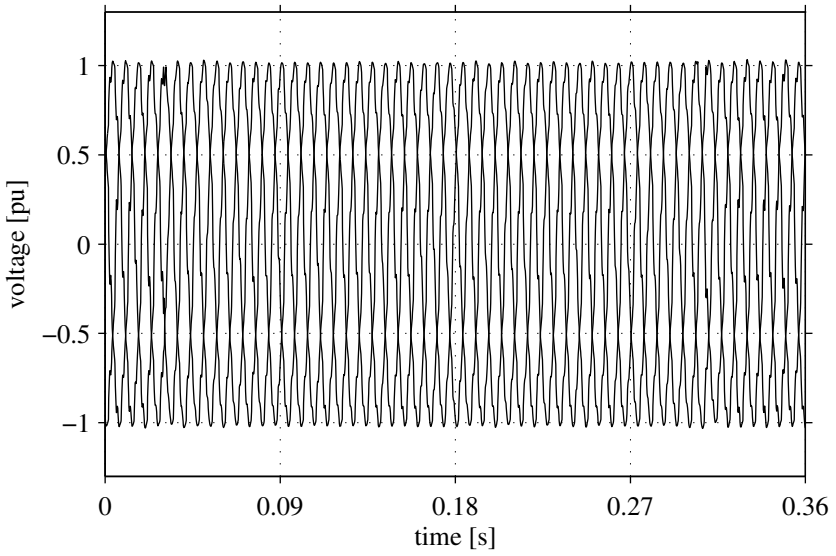


Fig. 6.33 Measured three-phase load voltage. DVC3 and diode rectifier load are used.

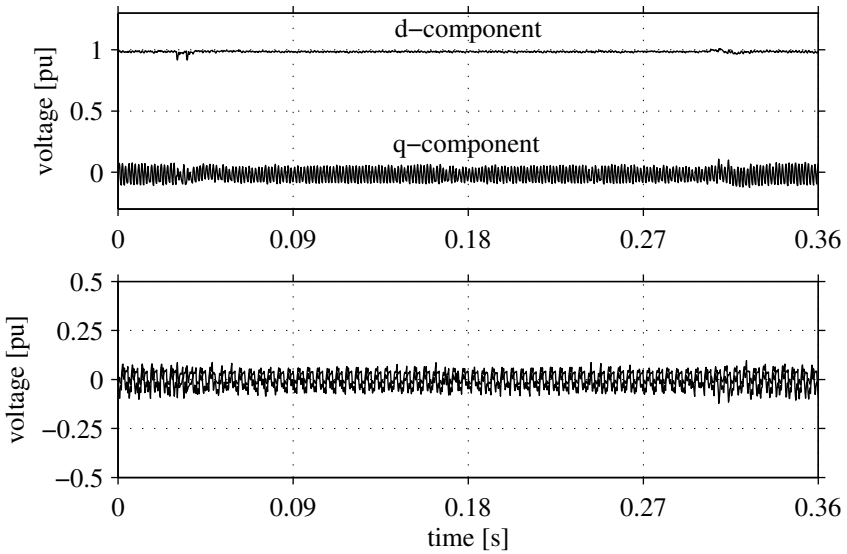


Fig. 6.34 Measured load voltage in dq-coordinate system. DVC3 and diode rectifier load are used. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

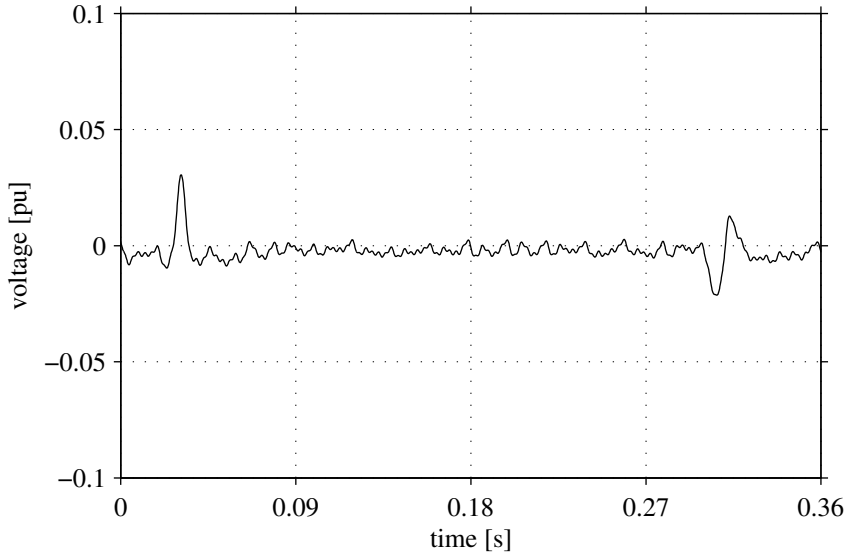


Fig. 6.35 Measured error of load voltage magnitude during unbalanced voltage dip. DVC3 and diode rectifier load are used.

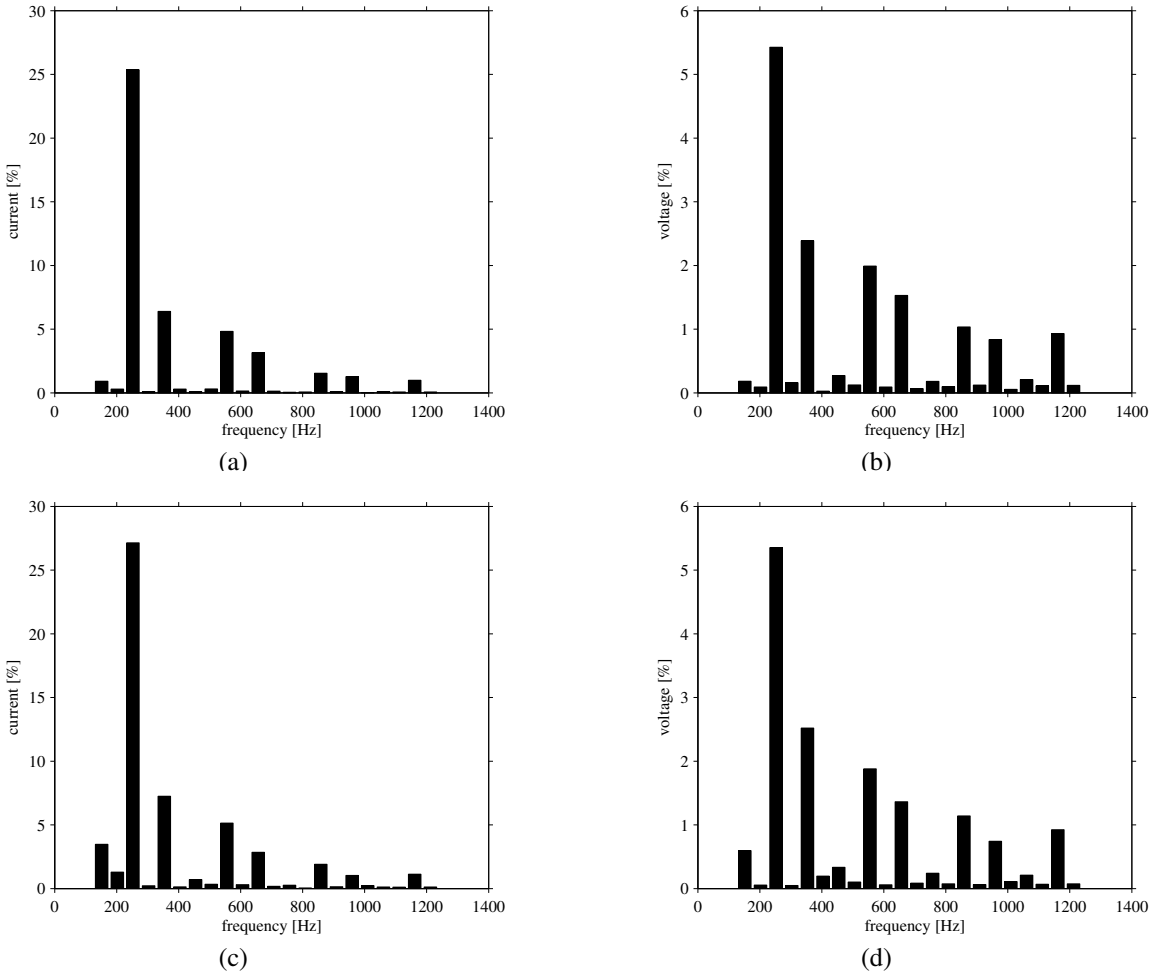


Fig. 6.36 Harmonic content of measured load current and voltage with diode rectifier load. Harmonic spectrum of load current when SSC offline: plot (a); harmonic spectrum of load voltage when SSC offline: plot (b); harmonic spectrum of load current when SSC online: plot (c); harmonic spectrum of load voltage when SSC online: plot (d).

Chapter 7

Voltage dip mitigation using shunt-connected VSC

7.1 Introduction

In the previous chapters, different current controllers for shunt-connected and series-connected VSCs have been presented. For the series-connected VSC, the current controller was completed with an outer voltage control loop that provides the appropriate current references in order to compensate for voltage dips. However, in Chapter 2 it was observed that voltage dip mitigation can be accomplished also by using a shunt-connected VSC.

This chapter will present the derivation of a controller for dip mitigation. Two different control strategies will be developed and compared and related simulation results will be shown. Unfortunately, experimental tests could not be carried out due to practical limitations in the laboratory setup.

7.2 Voltage dip mitigation using reactive power injection

The principle of voltage dip mitigation using shunt-connected VSC is to inject a current into the PCC in order to maintain a constant voltage at the PCC. This can be obtained by only injecting reactive current without energy storage on the DC side of the VSC. The resulting scheme of the system, shown in Fig.7.1, is thus the same as the one in Fig.2.10, except for the absence of the energy storage device connected to the DC link of the VSC. A DC-link capacitor is still necessary for proper commutation.

Chapter 2 demonstrated that the magnitude of the voltage can be restored, but not its phase angle, by injecting reactive current. As shown in Fig.7.2, where the block scheme of the implemented control system is displayed, the voltage magnitude error, given by the difference between the magnitude of the measured voltage at PCC and its reference, is passed through an AC-voltage controller constituted by a PI-regulator. The output of the AC-voltage controller is

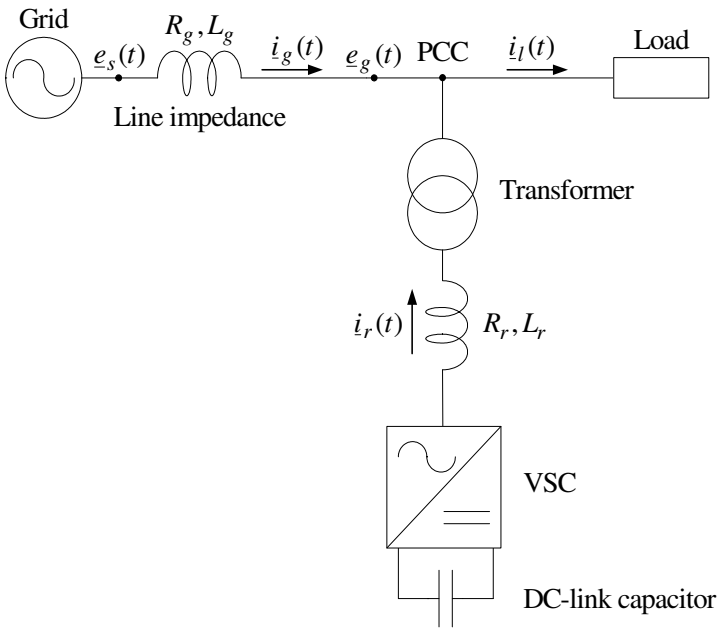


Fig. 7.1 Single-line diagram of shunt-connected VSC designed for reactive power injection only.

the reference reactive current, which is fed to the current controller, explained in Section 3.2. The reference active current is, instead, set to zero.

In a voltage-oriented system, the PLL sets the q-component of the grid voltage in the dq-coordinate system to zero. Thus, the capacitive reactive power injected by the VSC is given by

$$Q = e_{\mathrm{g}q} i_{\mathrm{r}d} - e_{\mathrm{g}d} i_{\mathrm{r}q} = -e_{\mathrm{g}d} i_{\mathrm{r}q} \tag{7.1}$$

Therefore, if the grid voltage is too low, capacitive reactive power should be injected and the current $i_{\mathrm{r}q}$ should be negative. The PI-regulator is given by

$$\begin{aligned} i^*_{\mathrm{r}q}(k) = &-k_{pQ}(|\underline{e}^{(dq)*}_{\mathrm{g}}(k)| - |\underline{e}^{(dq)}_{\mathrm{g}}(k)|)+ \\ &- \sum_{n=1}^{k} k_{iQ}(|\underline{e}^{(dq)*}_{\mathrm{g}}(n-1)| - |\underline{e}^{(dq)}_{\mathrm{g}}(n-1)|) \end{aligned} \tag{7.2}$$

The system has been tested via simulations by using the system configuration displayed in Fig.4.7. System and controller parameters are reported in Tables 7.1 and 7.2, respectively. The reactive power controller was tuned so the desired step response of the system was achieved. The bandwidth of the PLL is set to 30 Hz, as mentioned in Section 4.3.1.

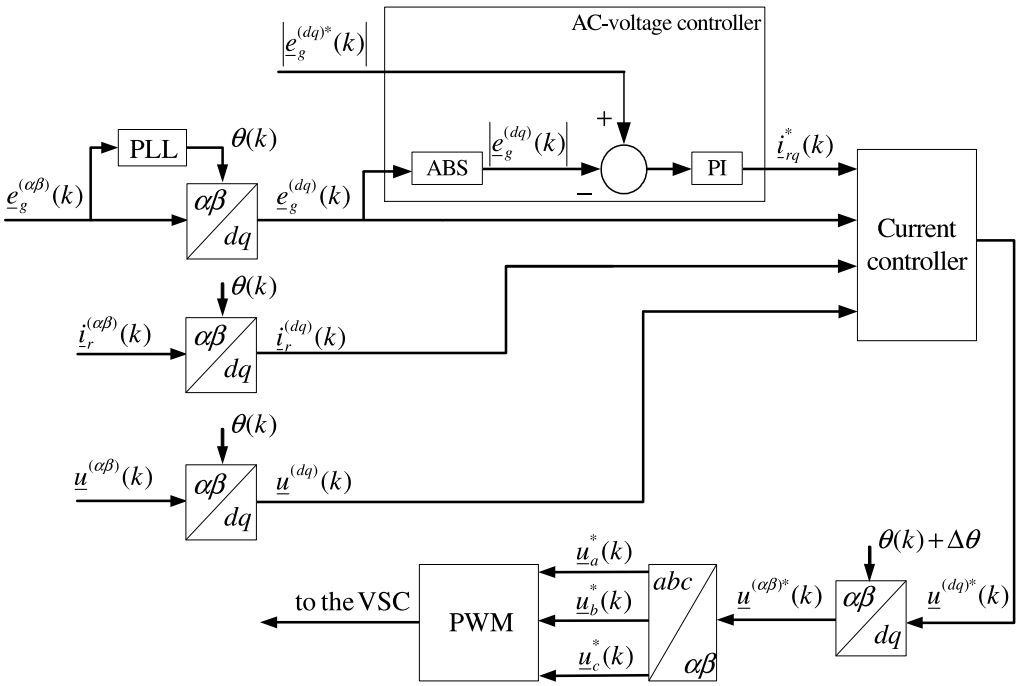


Fig. 7.2 Block scheme of reactive power control using shunt-connected VSC.

TABLE 7.1. SYSTEM PARAMETERS.

Grid voltage	E = 400 V = 1 pu	Grid current	I = 40 A = 1 pu
Grid frequency	f = 50 Hz	DC-link voltage	U_{dc} = 600 V = 1.5 pu
Grid inductance	L_{g} = 2.1 mH = 0.11 pu	Grid resistance	R_{g} = 0.05 Ω = 0.0087 pu
Load inductance	L_{l} = 23.9 mH = 1.3 pu	Load resistance	R_{l} = 10 Ω = 1.73 pu
Filter resistance	R_{r} = 24.8 mΩ = 0.0025 pu	Filter inductance	L_{r} = 2 mH = 0.0628 pu

TABLE 7.2. CONTROLLER PARAMETERS.

Sampling frequency	f_{s} = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Current controller parameters			
Proportional gain	$k_{\mathrm{p,cc}}$	7.01	(70% deadbeat)
Integrator gain	$k_{\mathrm{i,cc}}$	0	
Observer gain	k_{psp}	0.1	
Reactive power controller			
Proportional gain	$k_{p\mathrm{Q}}$	0.97	
Integrator time constant	$T_{i\mathrm{Q}}$	0.01	

Figure 7.3 shows the three-phase voltages at the PCC, which are affected by a voltage dip of 71% magnitude and with a phase-angle jump of 9°. The latter can be clearly appreciated from the dq-components of the voltage, shown in Fig.7.4. Figure 7.5 shows that during the voltage dip, the VSC responds by injecting a high amount of reactive current (1.15 pu), which in turn

keeps the voltage at the PCC constant at 1 pu. The voltages at PCC in the three-phase and in the dq-coordinate system are shown in Figs.7.6 and 7.7, respectively. However, the phase angle of the voltage varies by 25° during the dip, which can be seen clearly during the initial transient shown in Fig.7.8. At the end of the dip, a similar jump in phase angle will take place, as the phase voltage will come back to its pre-fault value. Note that the phase jump cannot be seen in the dq-components of the PCC voltage. However, during the transients at the beginning and end of the dip transients occur, because the PLL locks into the new phase angle, shown in Fig.7.7.

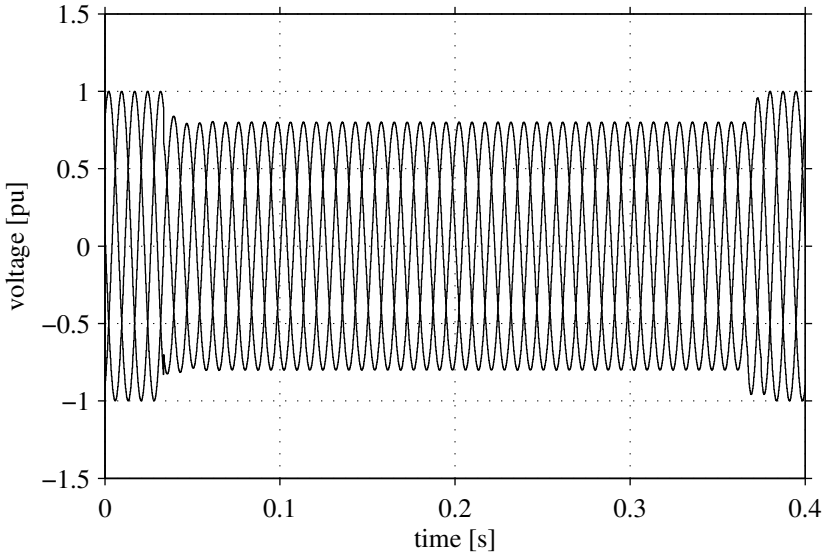


Fig. 7.3 Simulated three-phase grid voltages at PCC during balanced voltage dip. Dip mitigation is not active.

The simulation results prove that it is possible to mitigate voltage dips with the proposed controller, provided that the size of the VSC is such that it can handle the amount of reactive power needed. One disadvantage that has been pointed out in [58] is that the controller must be tuned for a specific value of the grid and load impedances, and it is very likely that the controller becomes unstable when either of the two parameters change. Simulations have shown that variations of $\pm 3\%$ in the grid impedance and of $\pm 2\%$ in the load impedance are allowed. However, for larger variations of these two parameters, the system becomes unstable. The grid and load parameters can increase without resulting in instability by slowing down the controller, but in most cases it will not be fast enough to compensate for voltage dips. A stable operation can be obtained for compensation of slower phenomena, such as voltage fluctuations leading to flicker [56][3] or voltage stability improvements [52]. However, if the grid configuration and the load are known and expected not to change, this controller can easily be implemented to add voltage dip compensation capability to existing or new shunt-connected VSC installations used for other purpose, such as STATCOM or active filters. To obtain high performance and a more robust controller, modifications of the VSC system are necessary. The modifications will be explained in the next section.

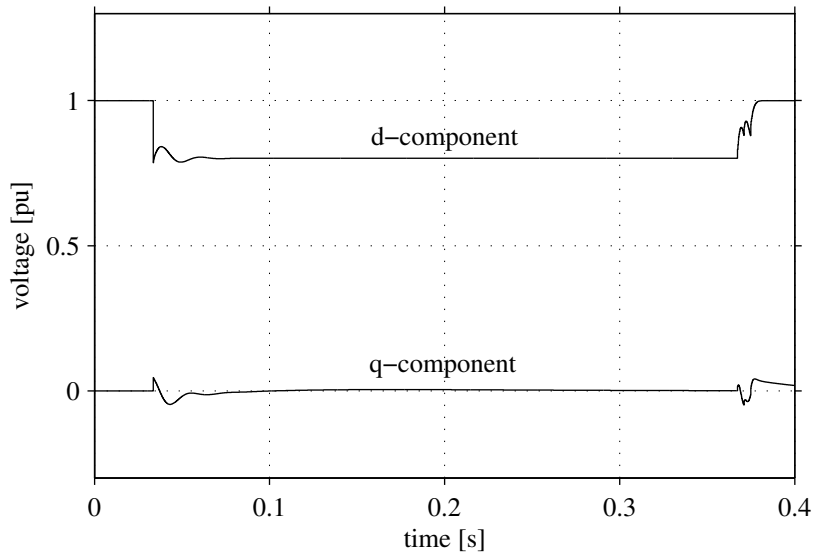


Fig. 7.4 Simulated grid voltages at PCC in dq-coordinate system during balanced voltage dip. Dip mitigation is not active.

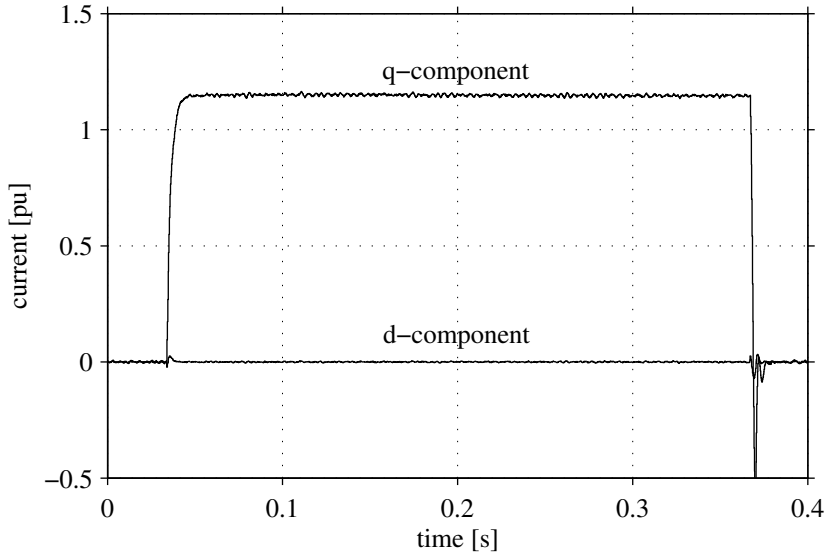


Fig. 7.5 Simulated response of d- and q-component of filter current due to 71% balanced voltage dip. Reactive power injection is used.

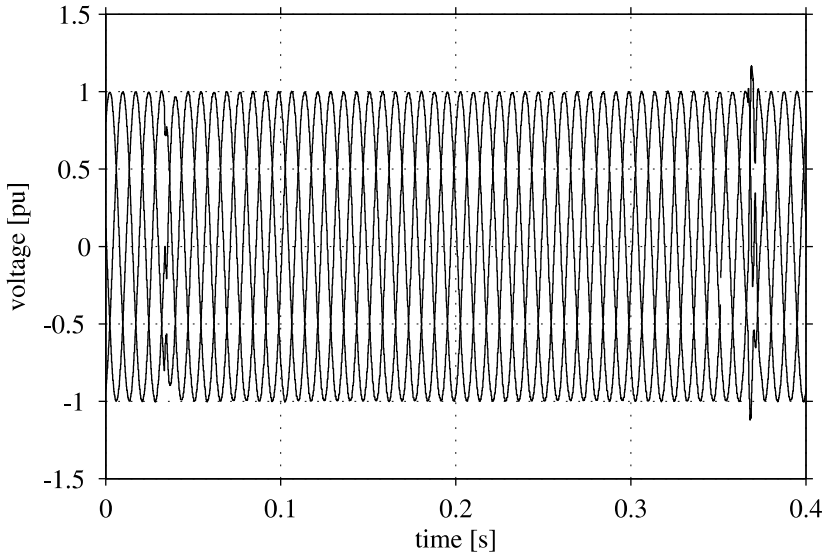


Fig. 7.6 Simulated compensated three-phase grid voltages at PCC. Reactive power injection is used.

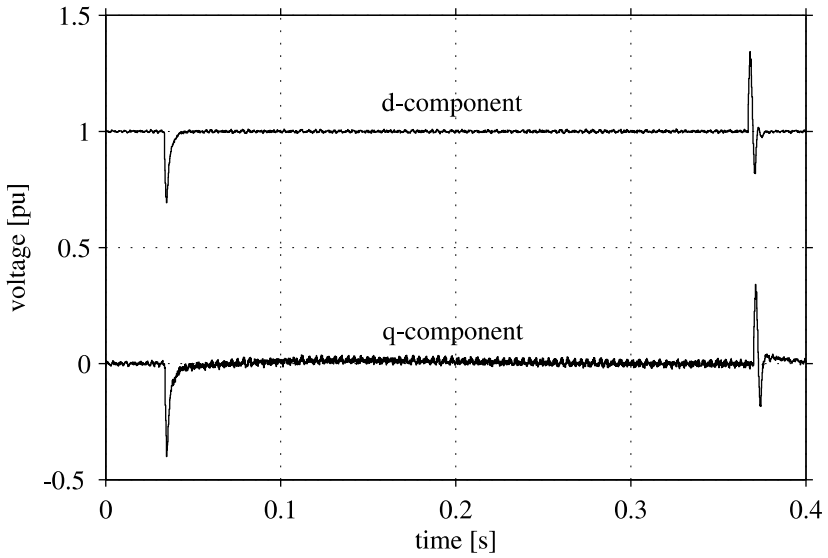


Fig. 7.7 Simulated compensated grid voltages at PCC in dq-coordinate system. Reactive power injection is used.

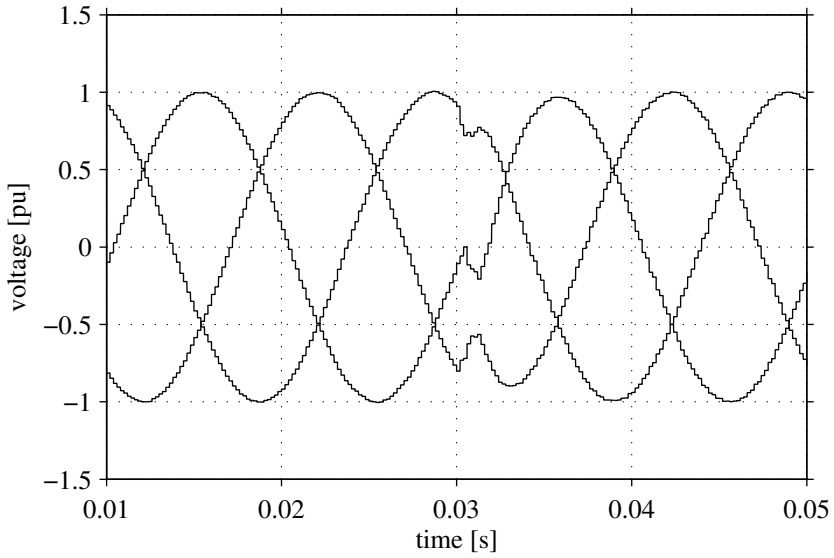


Fig. 7.8 Detail of phase deviation in compensated phase voltages at PCC at beginning of voltage dip. Reactive power injection is used.

7.3 Shunt-connected VSC using LCL-filter

The modified configuration of the shunt-connected VSC for voltage dip mitigation is shown in Fig.7.9. A capacitor is added in between the filter inductor at the VSC output and the transformer, with the twofold purpose of making the voltage at the PCC more stable and filtering the harmonic voltage components in the VSC output voltage. The VSC is then connected to the grid by an LCL-filter, where the grid-side inductor is obtained by the leakage reactance of the transformer. The leakage inductance and the series resistance of the transformer are denoted in the figure as L_{tr} and R_{tr}, respectively. System parameters are shown in Table 7.1. The filter capacitor is equal to 60 μF, while the transformer parameters L_{tr} and R_{tr} are equal to 1 mH and 31.4 mΩ, respectively.

The control objective is to maintain the voltage across the filter capacitor, and thereby the PCC voltage, constant. This only holds if the voltage drop over the transformer is negligible. A cascade controller, shown in Fig.7.10, that is similar to the one developed for the SSC (derived in Section 5.3), can be used for this purpose. The main differences compared to the series-connected VSC are that the grid current cannot be considered constant and that the reference value of the capacitor voltage is known and not calculated from the measured grid voltage. However, the PCC voltage is only measured and used as input to the PLL, in order to achieve proper control of the active and reactive power injected in the grid. Since only the PLL will use the PCC voltage, an inexpensive and simple voltage measurement can be used. The control system parameters are shown in Table 7.3.

One problem by using the LCL-filter is that unwanted resonances can arise between the filter components. The dq-currents during mitigation of the voltage dip shown in Fig.7.3 using the proposed cascade controller, are shown in Fig.7.11. The oscillations in the currents are clearly

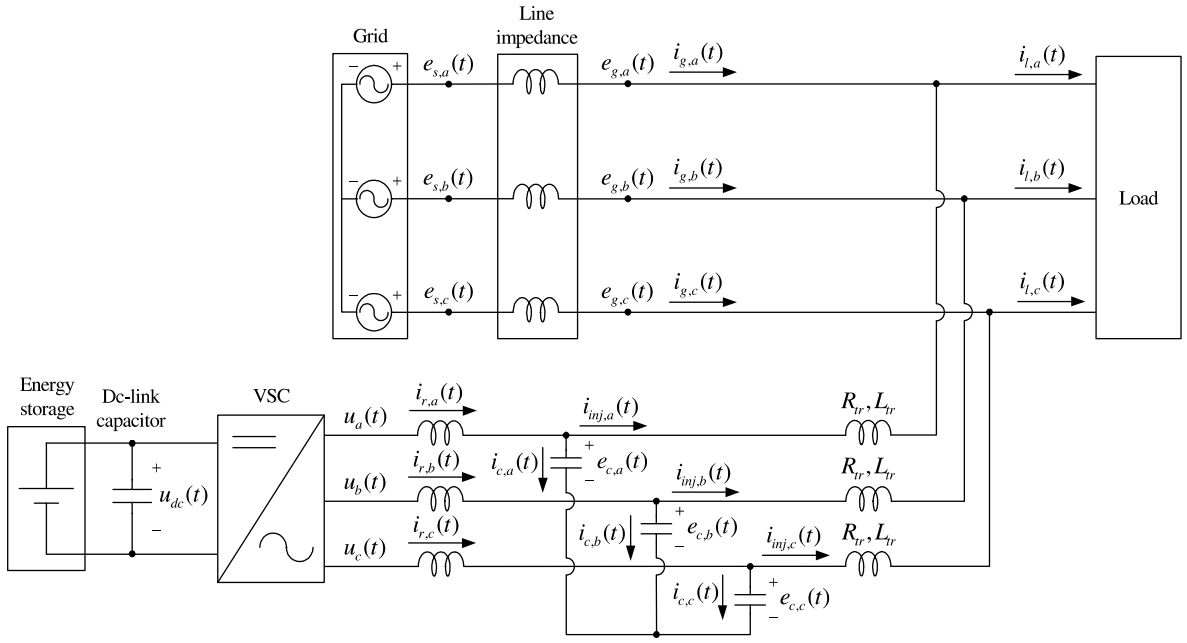


Fig. 7.9 Scheme of shunt-connected VSC using LCL-filter.

TABLE 7.3. CONTROLLER PARAMETERS.

Sampling frequency	f_s = 5 kHz	Switching frequency	f_{sw} = 5 kHz
Current controller parameters			
Proportional gain	$k_{p,cc}$	7.01	(70% deadbeat)
Integrator gain	$k_{i,cc}$	0	
Observer gain	k_{psp}	0.1	
Voltage controller parameters			
Proportional gain	$k_{p,vc}$	0.075	(25% deadbeat)
Integrator time constant	$T_{i,vc}$	0.03	

visible. This phenomenon can be avoided by adding a resistor in series with the filter capacitor, as proposed in [30]. However, the resistor causes losses in all operating conditions and increases the amount of active power during voltage dip mitigation. An alternative method [8][22] is to add a fictitious resistance R_d in the inner current controller that, calling $\underline{\varepsilon}_i^{(dq)}$ the current error as in Eq.(3.42), becomes

$$\begin{aligned}\underline{u}^{(dq)*}(k) = \underline{e}_g^{(dq)}(k) + R_r\underline{i}_r^{(dq)}(k) + j\frac{\omega L_r}{2}(i_r^{(dq)*}(k) + i_r^{(dq)}(k)) + \\ + k_p\underline{\varepsilon}_i^{(dq)}(k) + \sum_{n=1}^{k} k_i\underline{\varepsilon}_i^{(dq)}(n-1) - R_d\underline{i}_r^{(dq)}(k)\end{aligned} \tag{7.3}$$

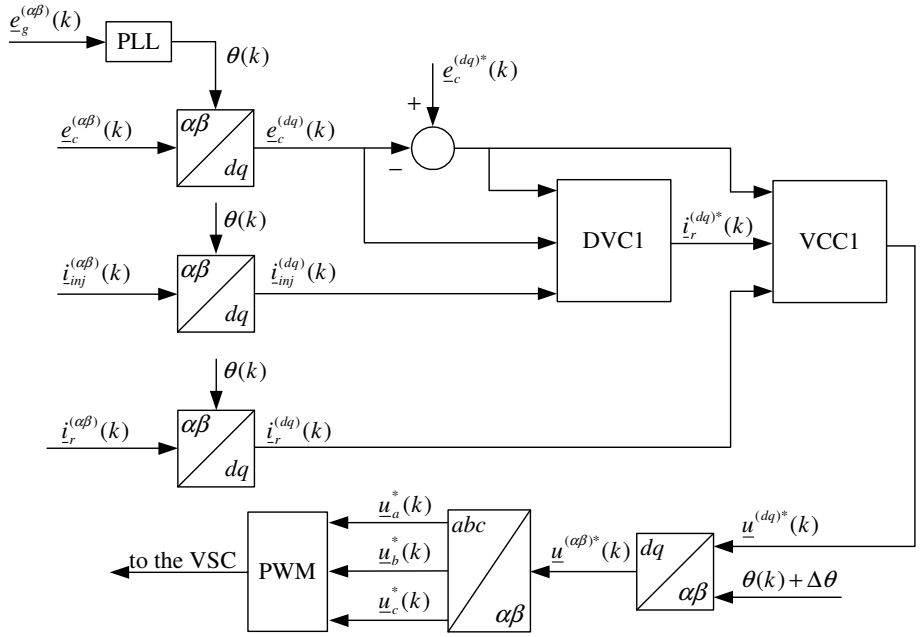


Fig. 7.10 Block scheme of control system for voltage dip mitigation using shunt-connected VSC and LCL-filter.

This is simplified to

$$\begin{aligned}\underline{u}^{(dq)*}(k) = \underline{e}_{\mathrm{g}}^{(dq)}(k) - (R_{\mathrm{d}} - R_{\mathrm{r}})\underline{i}_{\mathrm{r}}^{(dq)}(k) + \mathrm{j}\frac{\omega L_{\mathrm{r}}}{2}(i_{\mathrm{r}}^{(dq)*}(k) + i_{\mathrm{r}}^{(dq)}(k)) + \\ + k_p\underline{\varepsilon}_{\mathrm{i}}^{(dq)}(k) + \sum_{n=1}^{k} k_i\underline{\varepsilon}_{\mathrm{i}}^{(dq)}(n-1)\end{aligned} \tag{7.4}$$

This modification is effective in damping the oscillations, but it results in a slightly slower response of the controller. The size of the damping term R_{d} is thus a trade-off between the desired damping and the desired speed of response [8]. Here, the value of the damping term R_{d}, which has been determined by trial and error, is set to 0.5 Ω. Therefore, the resistive voltage drop in the current controller is negative. The dq-currents during mitigation of the voltage dip shown in Fig.7.3 using the proposed cascade controller and active damping in the inner loop are shown in Fig.7.12. As shown, the current is still affected by oscillation, but with a smaller amplitude and higher damping. However, also the response of the controller is slower. The injected reactive current during the dip under steady state is equal to 0.95 pu. It is possible to observe that the reactive current injected by the VSC is lower compared with the previous case. This is due to the voltage drop over the transformer and to the presence of the filter capacitor, which produces reactive power. Moreover, the steady state active current during the dip mitigation is zero. However, at the beginning and at the end of the dip, active current transients occur. These transients are due to the oscillations in the LCL-filter and to the required time for the PLL to track the new phase angle. Therefore, if the DC-link capacitor is big enough to handle the transients, no extra energy storage is needed. The PCC voltage, shown in Fig.7.13, is regulated to the desired value. Only very small oscillations of 0.01 pu at the beginning and at the end of the dip can be noticed in the dq-voltages in Fig.7.14.

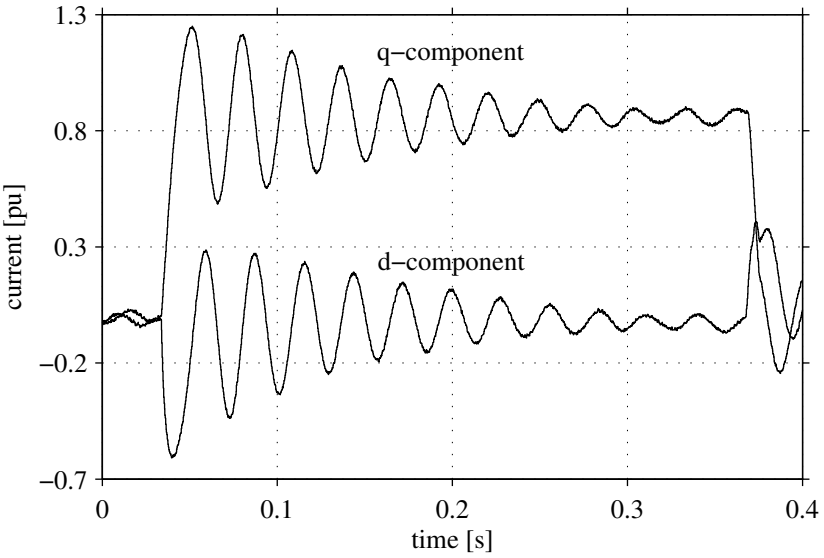


Fig. 7.11 Simulated response of d- and q-component of filter current to balanced voltage dip. VSC with LCL-filter is used.

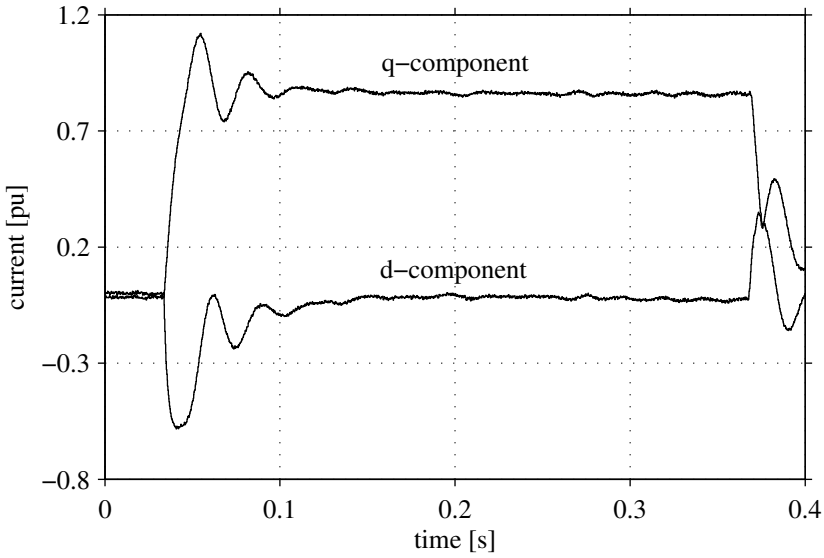


Fig. 7.12 Simulated response of d- and q-component of filter current to balanced voltage dip. VSC with LCL-filter is used. Controller has active damping.

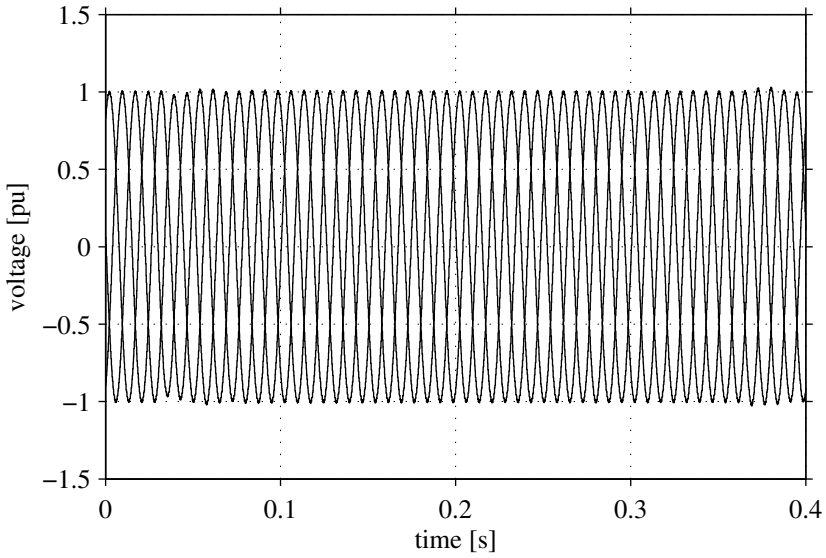


Fig. 7.13 Simulated compensated three-phase grid voltages at PCC. VSC with LCL-filter is used. Controller has active damping.

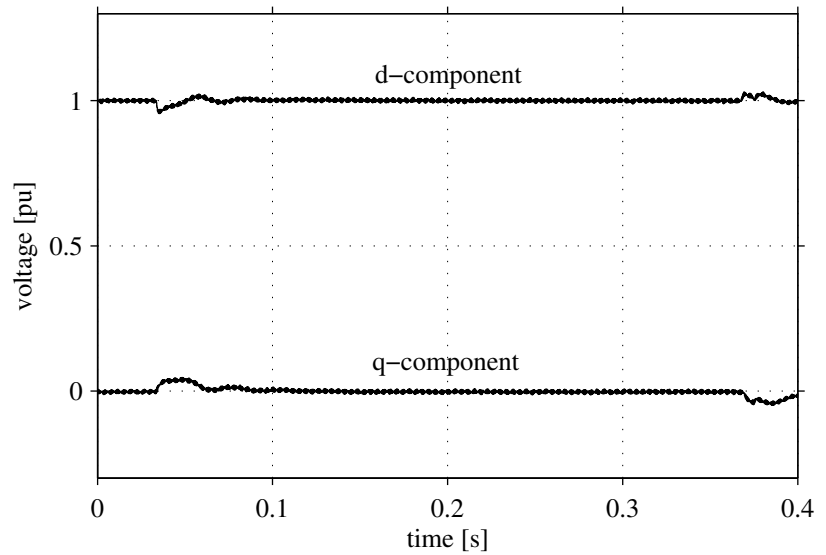


Fig. 7.14 Simulated compensated grid voltages at PCC in dq-coordinate system. VSC with LCL-filter is used. Controller has active damping.

The controller has also been tested under unbalanced voltage dips. Figures 7.15 and 7.16 display the PCC voltage in three-phase voltages and in dq-voltages without dip mitigation. For the same dip and mitigation active, the injected currents in Fig.7.17 are affected by a 100 Hz oscillation, as the controller is designed in the positive SRF. This results in unbalanced PCC voltages as shown in Fig.7.18 (three-phase) and Fig.7.19 (dq-coordinates). However, the average grid voltage amplitude is now at a correct level.

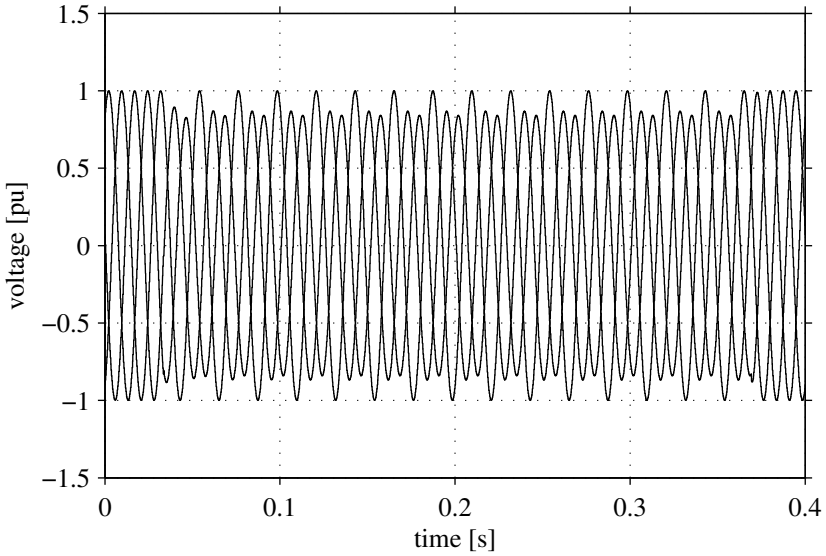


Fig. 7.15 Simulated three-phase grid voltages at PCC during unbalanced voltage dip.

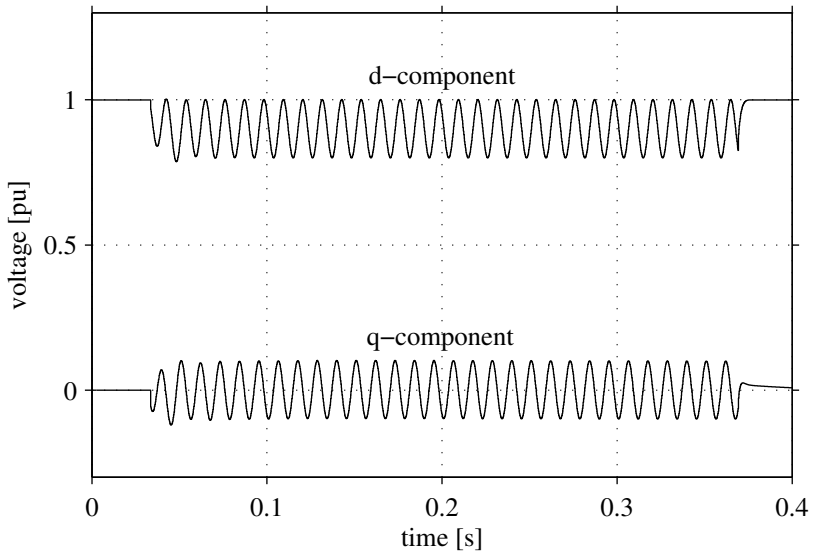


Fig. 7.16 Simulated grid voltages at PCC in dq-coordinate system during unbalanced voltage dip.

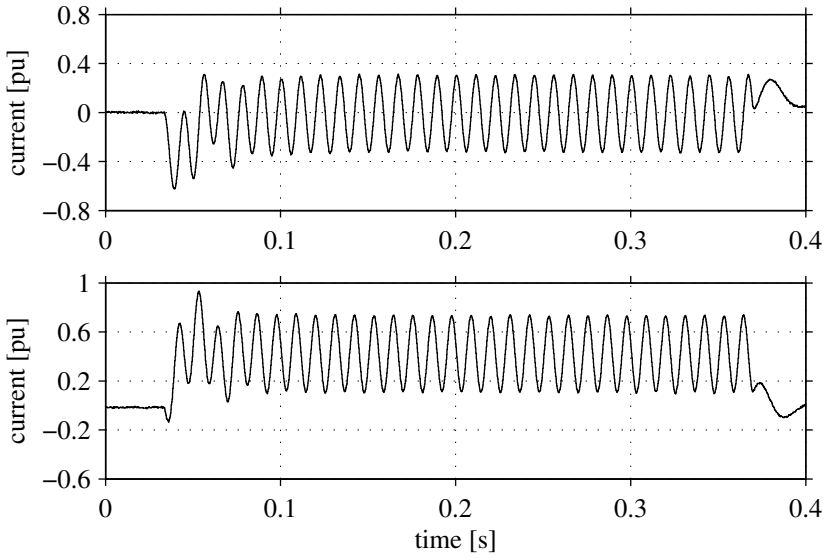


Fig. 7.17 Simulated response of d- and q-component of injected current due to unbalanced voltage dip. VSC with LCL-filter is used. Controller has active damping.

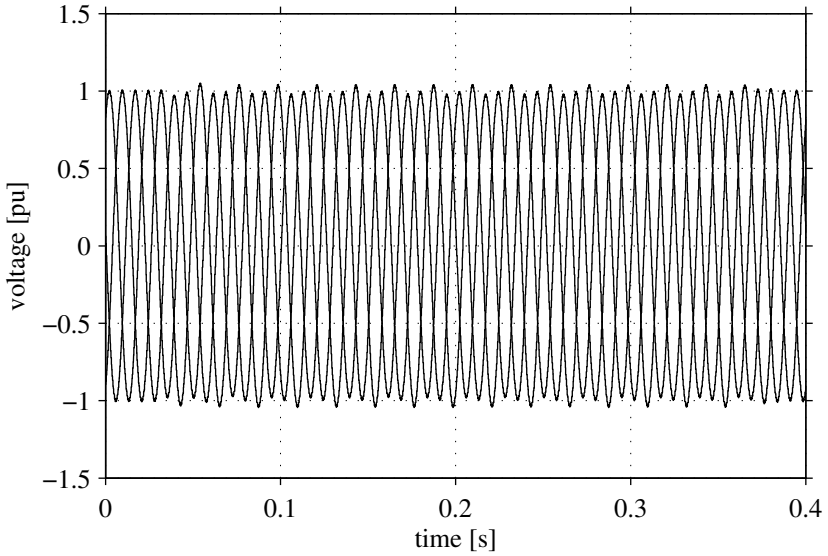


Fig. 7.18 Simulated compensated three-phase grid voltages at PCC. VSC with LCL-filter is used. Controller has active damping.

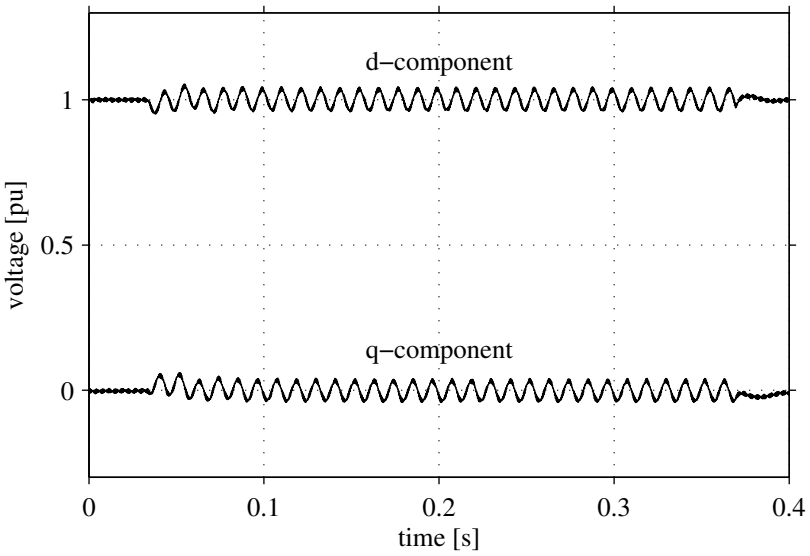


Fig. 7.19 Simulated compensated grid voltages at PCC in dq-coordinate system. VSC with LCL-filter is used. Controller has active damping.

To control the positive and the negative sequences separately, it is possible to implement two separate controllers in the positive and negative SRFs, respectively. This is similar to what was done for the series-connected configuration in Section 5.5. The corresponding block scheme is shown in Fig.7.20. The controller parameters are displayed in Table 7.3. The same active damping term as in Eq.(7.4) has been added in both the positive and negative current controllers.

Figures 7.21 to 7.23 show the sequence components in the corresponding SRFs for the uncompensated PCC voltage, the injected currents and the compensated PCC voltage, respectively. Successful compensation of the voltage dip is clearly visible also in the three phase voltages at the PCC, shown in Fig.7.24.

To test the robustness of the proposed control system, the shunt-connected VSC with LCL-filter has been tested under the same unbalanced voltage dip displayed in Fig.7.15 for a weaker grid. For this new set of simulations, the grid impedance has been set double compared with the previous case ($L_{\mathrm{g}} = 4.2$ mH, $R_{\mathrm{g}} = 0.1\ \Omega$). As shown in Fig.7.25, where the VSC currents in the positive and negative SRF are displayed, the controller maintains stable operation and, when the dip occurs, injects power into the mains to restore the voltage at PCC to the pre-fault conditions. It can be noticed that, due to the larger grid impedance, the amount of power injected by the VSC is lower compared with the previous case. Successful restoration of the grid voltage at PCC is achieved also in this case, as shown in Figs.7.27 and 7.26, where the the three-phase grid voltages and the grid voltage in the positive and negative SRF, respectively, are displayed.

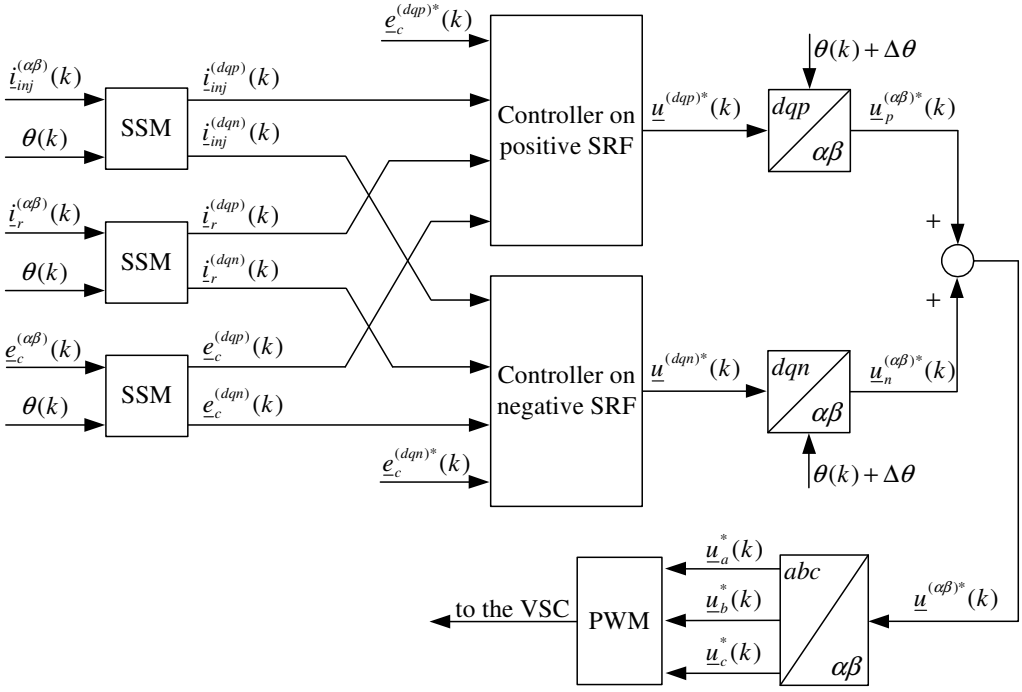


Fig. 7.20 Block scheme of improved control system for voltage dip mitigation when using shunt-connected VSC with LCL-filter.

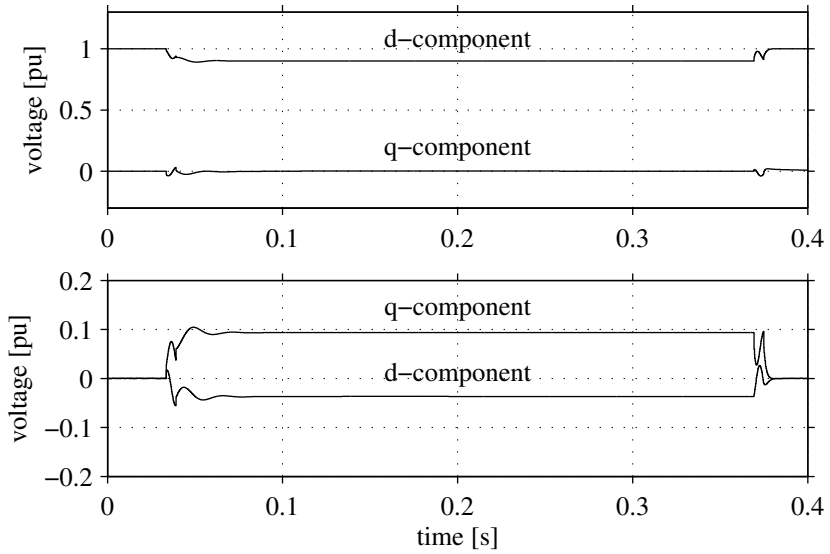


Fig. 7.21 Simulated grid voltages at PCC in dq-coordinate system during unbalanced voltage dip. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

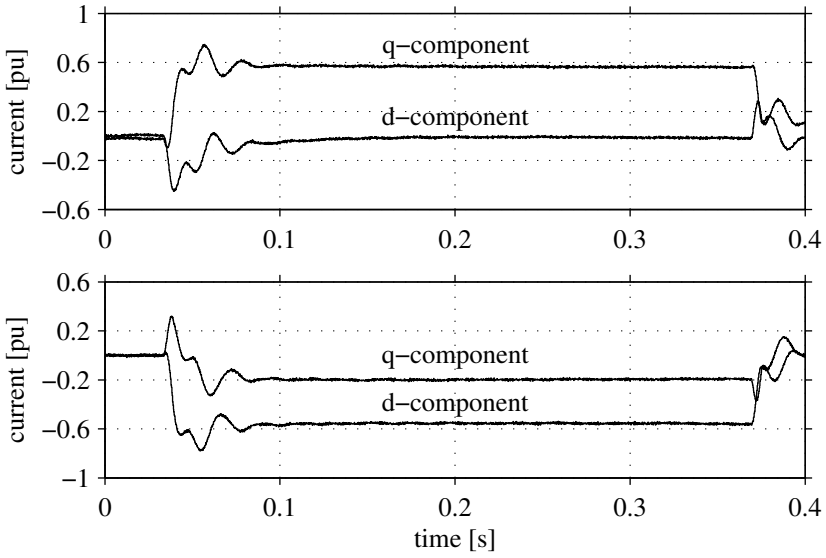


Fig. 7.22 Simulated response of d- and q-component of injected current due to unbalanced voltage dip. VSC with LCL-filter is used. Positive and negative controllers have active damping. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

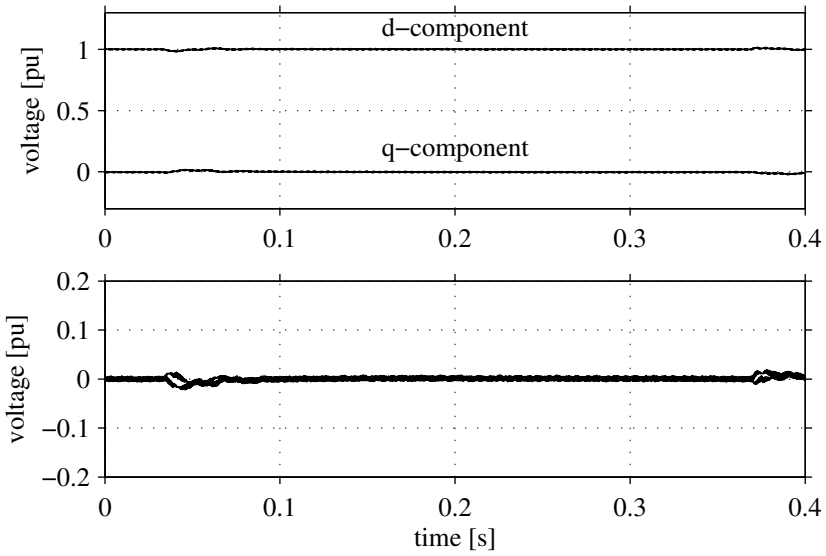


Fig. 7.23 Simulated compensated grid voltages at PCC in dq-coordinate system. VSC with LCL-filter is used. Positive and negative controllers have active damping. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

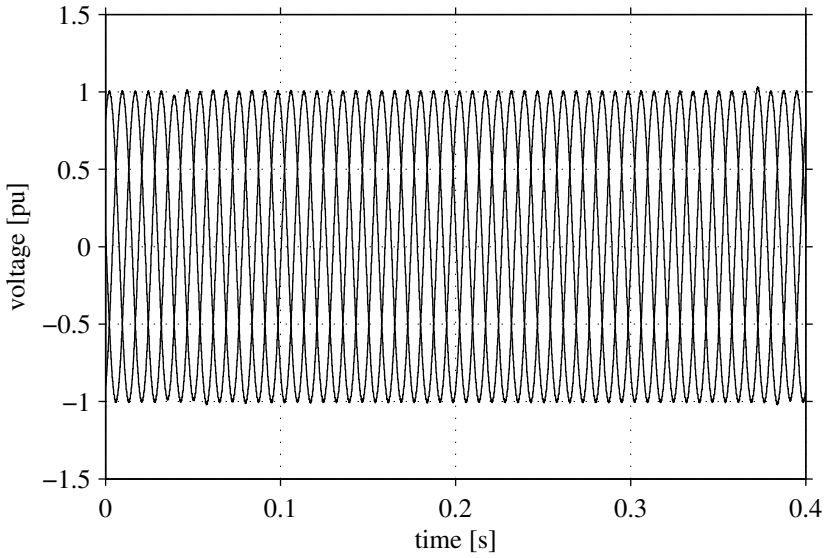


Fig. 7.24 Simulated compensated three-phase grid voltages at PCC. VSC with LCL-filter is used. Positive and negative controllers have active damping.

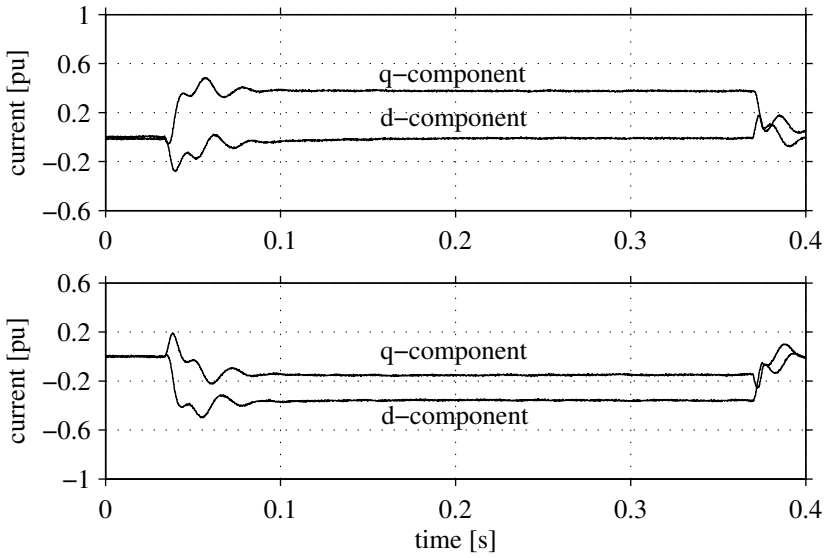


Fig. 7.25 Simulated response of d- and q-component of injected current to unbalanced voltage dip. VSC with LCL-filter and weak grid are used. Positive and negative controllers have active damping. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

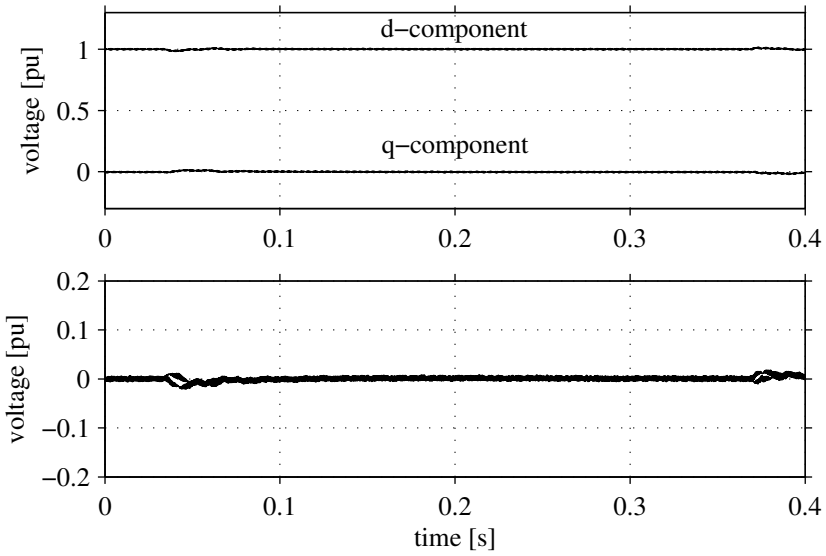


Fig. 7.26 Simulated compensated grid voltages at PCC in dq-coordinate system. VSC with LCL-filter and weak grid are used. Positive and negative controllers have active damping. Top: positive sequence in positive SRF; bottom: negative sequence in negative SRF.

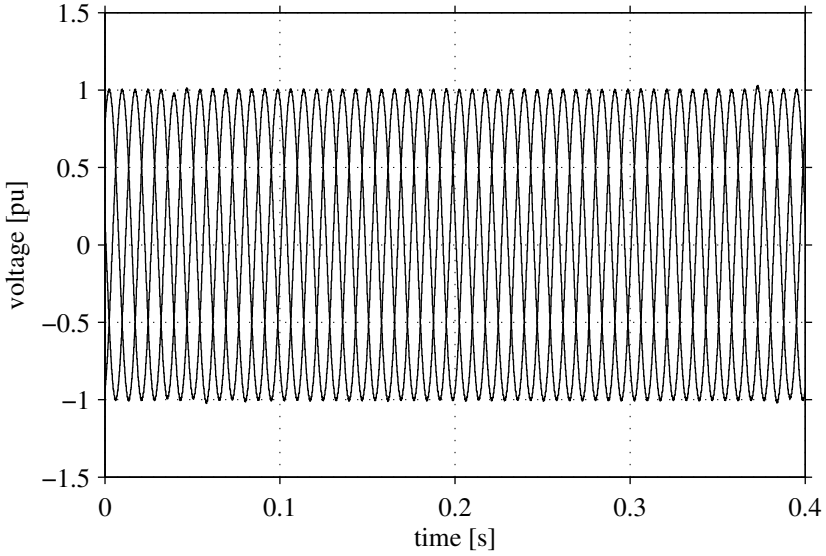


Fig. 7.27 Simulated compensated three-phase grid voltages at PCC. VSC with LCL-filter and weak grid are used. Positive and negative controllers have active damping.

7.4 Conclusions

This chapter has shown that the shunt-connected VSC can be used for voltage dip compensation. A control system that compensates for voltage dips without injecting active power has been presented. It has been shown that successful restoration of the amplitude of the voltage at PCC can be achieved. However, the phase angle of the grid voltage at PCC is affected by phase deviation during dip mitigation. It has been pointed out that this type of control system is very sensitive to system parameters variations. Therefore, to obtain a more robust controller, lower gains in the reactive-power controller must be used. This will lead to a reduced bandwidth of the control system, thus, in most cases the controller will not be fast enough to compensate for voltage dips.

To obtain a high performance and more robust controller, a configuration of shunt-connected VSC with LCL-filter has been proposed. The transient performance of the modified system with the same cascade controller, derived in Section 5.3, has been tested under balanced voltage dips. It has been shown that, due to resonance problems between the filter components, oscillations in the current at the output of the VSC can be experienced. To overcome this problem, an active damping term in the inner current controller has been added. By using this modification, satisfactory mitigation of balanced voltage dips can be obtained. However, as expected for the analysis carried out in the previous chapters, modifications in the cascade controller in order to control positive- and negative-sequence components of the controlled variables, are needed for mitigation of unbalanced voltage dip. With the proposed modification, satisfactory performance of the system also under unbalanced voltage dips can be achieved. However, also when using shunt-connected VSC with LCL-filter, large amount of current has to be injected into the mains. The VSC must then be designed such that it can handle the amount of reactive power needed.

Chapter 8

Conclusions and future work

8.1 Conclusions

This thesis has dealt with mitigation of voltage dips by using a voltage source converter (VSC) connected in series and in shunt with the grid. In both configurations, one important issue is to have a fast-response, high-performance control system that is robust to voltage disturbances. In both configurations, the core of the controller is the current controller. In Chapter 3, three different current controllers for shunt-connected VSC have been investigated and compared under balanced and unbalanced conditions of the grid voltage, both in steady-state and during transients (voltage dips). With a constant DC-link voltage, steps in the reference currents have been applied in order to test the dynamic performance of the system. To validate the simulation results, experimental results have been shown in Chapter 4 for all three controllers. It has been demonstrated that, using a vector current-controller designed by only considering positive sequence components (VCC1), the dq-currents under unbalanced grid voltage are affected by an oscillation at double the power frequency. By feeding the same controller only the positive-sequence component of the grid voltage (VCC2), the response is improved and the actual current tracks the reference current with almost no delay. The dual vector current-controller (DVCC), where both voltages and currents are separated into their sequence components and two separate current controllers are used, shows a slower response compared with VCC2, due to the delay introduced by the sequence separation. It is important to stress that these results are valid for any application of shunt-connected VSC where a robust response to voltage disturbances is required. This can be the case of VSC used as active front-end in drive systems, variable-speed wind power and VSC-based HVDC.

A high-performance current controller is also the base of the cascade controller for the series-connected VSC (or static series compensator, SSC), which has been presented in Chapter 5. The current controller is combined with an outer voltage controller loop. An extended analysis of the control system and of the interaction between the inner controller and the outer controller has been carried out. The problem of saturation of the injection transformer during voltage dip mitigation and several solutions have been discussed. Three different control systems for SSC have been investigated and compared under balanced and unbalanced voltage dips. Beside si-

mulations, experimental verification for all three cascade controllers has been carried out on a laboratory prototype of the SSC, as shown in Chapter 6. It has been demonstrated that using dual vector-controller type 1 (DVC1), designed by only considering the positive-sequence components of the measured signals, the SSC mitigates three-phase voltage dips, but not unbalanced voltage dips. A way to deal with unbalanced voltage dips is to isolate and control, with the same regulator, only the positive-sequence component of the voltage, whereas the negative sequence is fed forward, in what is called dual vector-controller type 2 (DVC2). This has been shown to mitigate also unbalanced voltage dips with very fast response, yet its performance has been proven to depend on the size of the filter capacitor. Since deadbeat gain for the current controller can be used, DVC2 is a suitable solution for SSC when fast restoration of the load voltage is required and when the filter can be made small. Finally, the dual vector-controller type 3 (DVC3), based on two separate cascade controllers for positive and in the negative sequence, has been presented. It has been demonstrated that DVC3 presents good performance when mitigating balanced and unbalanced voltage dips for different types of load. Due to the use of DVCC, DVC3 has slower response as compared with DVC2, but it ensures a perfect mitigation of the voltage dip, regardless of size of the filter capacitor and the percentage of unbalance of the dip.

The performance of the shunt-connected VSC when used to mitigate voltage dips has been investigated in Chapter 7. It has been shown that successful restoration of the amplitude of the voltage at PCC can be achieved. However, the phase angle of the grid voltage at PCC is affected by a phase deviation during mitigation. To obtain a robust high-performance controller, insensitive to grid and load impedance variations, a modified configuration of shunt-connected VSC with LCL-filter has been proposed. The transient performance of the modified system, with the same cascade controller derived in Chapter 5 for the SSC, has been tested under balanced and unbalanced voltage dips. It has been shown that, to overcome undesired resonances between the filter components, an active damping term in the inner current controller must be added. With this modification, it has been shown that satisfactory mitigation of voltage dips can be achieved. However, depending on the short-circuit power of the grid at the PCC, the VSC may have to be designed to handle injection of high amount reactive power.

8.2 Future work

The current control algorithms presented in this thesis are very general and can be applied in different applications of VSC connected to the grid. However, they have been developed and tested with a stiff voltage source connected to the DC link of the VSC. Alternatively, a capacitor can be connected to the DC link and the controller must include regulation of the voltage across the DC-link capacitor. This limits the range of active power control. An energy storage device can be connected to the DC link. Possible solutions for storage are capacitors, super-capacitors, fuel cells and batteries. A requirement is that the energy storage device must be able to deliver a high amount of power quickly. It is not clear at this point which, among all possible solutions, represents the most suitable choice for the investigated application.

It was pointed out that a drawback of using a shunt-connected VSC for voltage dip mitigation is that the current to be injected into the grid may be too high if the grid is strong. An interesting

alternative in this case is to disconnect the load from the grid when a disturbance occurs and support the load with the shunt-connected VSC. This again requires a storage device, or another source of energy, to be connected to the DC side of the VSC. Disconnection may be achieved quickly by using e.g. a static (thyristor-based) switch. If the load can be supported for the required time by a suitable active power source, this is a solution also against short interruptions.

A series-connected VSC could be used at transmission level for series compensation. In transmission systems, other control objectives are more important than voltage dip compensation. Controllable series compensation is used for e.g. power flow control, stability improvement, and damping of power oscillations. Traditional non-controllable series compensation based on series capacitors can create problems due to unwanted resonance with the rest of the power system. A specific problem that often arises in conjunction with series capacitors is subsynchronous resonance, which is most dangerous as it can cause the generator shafts to break down. A VSC-based device will not cause this problem; rather, if installed close the power station, it can change the degree of series compensation in order to move away from the risk for SSR. A challenge remains to properly design the protection system for the series device.

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Appendix A

Transformations for three-phase systems

A.1 Introduction

This appendix reports necessary transformations to calculate voltage vectors from three-phase quantities and vice versa. Expressions of the voltage vector both in the fixed and rotating reference frames are given in the general case of unsymmetrical three-phase quantities.

A.2 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities $v_1(t)$, $v_2(t)$ and $v_3(t)$ can be transformed into a vector in a complex reference frame, usually called $\alpha\beta$-frame, by applying the transformation defined by

$$\underline{v}(t) = v_\alpha + \mathrm{j}v_\beta = K(v_1(t) + v_2 e^{\mathrm{j}\frac{2}{3}\pi}(t) + v_3 e^{\mathrm{j}\frac{4}{3}\pi}(t)) \tag{A.1}$$

where the factor K is equal to $\sqrt{3/2}$ or $3/2$ to ensure power invariance or voltage invariance, respectively, between the two systems. Equation (A.1) can be expressed as a matrix equation as follows

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = C_{23} \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} \tag{A.2}$$

where, using power-invariant transformation, the matrix C_{23} is equal to

$$C_{23} = \begin{bmatrix} \sqrt{\frac{2}{3}} & \frac{-1}{\sqrt{6}} & \frac{-1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \tag{A.3}$$

The inverse transformation, assuming no zero-sequence, is given by

$$\begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} = C_{32} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A.4}$$

where

$$C_{32} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ \frac{-1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ \frac{-1}{\sqrt{6}} & \frac{-1}{\sqrt{2}} \end{bmatrix} \tag{A.5}$$

A.3 Transformation between fixed and rotating coordinate systems

Let the vectors $\underline{v}(t)$ and $\underline{u}(t)$ rotate in the $\alpha\beta$-frame with the angular frequency $\omega(t)$ in the positive (counter-clockwise) direction. If the vector $\underline{u}(t)$ is taken as the d-axis of a dq-frame that rotates in the same direction with the same angular frequency $\omega(t)$, both vectors will appear as fixed vectors in that frame. The components of $\underline{v}(t)$ in the dq-frame are thus given by the projections of the vector on the direction of $\underline{u}(t)$ and on the orthogonal direction, as illustrated in Fig.A.1.

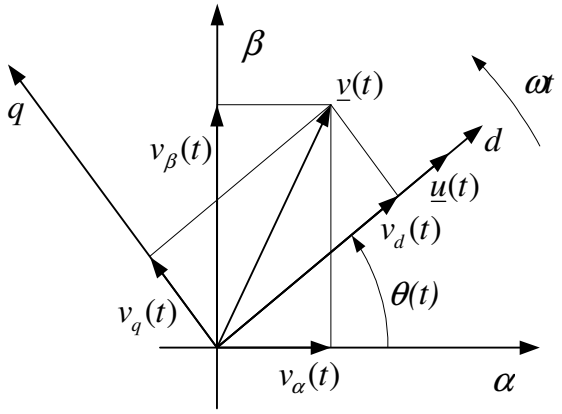

Fig. A.1 Relation between $\alpha\beta$-frame and dq-frame.

The transformation can be written in vector form as

$$\underline{v}^{(dq)}(t) = \underline{v}^{(\alpha\beta)}(t)e^{-\mathrm{j}\theta(t)} \tag{A.6}$$

with the angle $\theta(t)$ in Fig.A.1 given by

$$\theta(t) = \theta_0 + \int_0^\tau \omega(\tau)d\tau \tag{A.7}$$

The inverse transformation, from the rotating dq-frame to the fixed $\alpha\beta$-frame is defined by

$$\underline{v}^{(\alpha\beta)}(t) = \underline{v}^{(dq)}(t)e^{\mathrm{j}\theta(t)} \tag{A.8}$$

The components in the dq-frame can be determined from Fig.A.1. In matrix form, the transformation from the fixed $\alpha\beta$-frame to the dq-frame can be written as

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = R(-\theta(t)) \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A.9}$$

while the inverse is given by

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = R(\theta(t)) \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \tag{A.10}$$

where the projection matrix is

$$R(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \tag{A.11}$$

A.4 Voltage vectors for unsymmetrical three-phase systems

The phase voltages for a three-phase system can be written as

$$e_{\mathrm{a}}(t) = \widehat{e}_{\mathrm{a}}(t)\cos(\omega(t) - \varphi_{\mathrm{a}}) \tag{A.12}$$

$$e_{\mathrm{b}}(t) = \widehat{e}_{\mathrm{b}}(t)\cos(\omega(t) - \frac{2}{3}\pi - \varphi_{\mathrm{b}}) \tag{A.13}$$

$$e_{\mathrm{c}}(t) = \widehat{e}_{\mathrm{c}}(t)\cos(\omega(t) - \frac{4}{3}\pi - \varphi_{\mathrm{c}}) \tag{A.14}$$

$$\tag{A.15}$$

where $\widehat{e}_{\mathrm{a}}(t)$ and φ_{a} are the amplitude and the phase angle of the phase voltage $e_{\mathrm{a}}(t)$, while ω is the angular frequency of the system.

If the voltage amplitude of the three phases are unequal, the resulting voltage vector $\underline{u}^{(\alpha\beta)}(t)$ in the fixed $\alpha\beta$-coordinate system can be expressed as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence component vectors

$$\underline{u}^{(\alpha\beta)}(t) = E_{\mathrm{p}} e^{\mathrm{j}(\omega t + \varphi_{\mathrm{p}})} + E_{\mathrm{n}} e^{-\mathrm{j}(\omega t + \varphi_{\mathrm{n}})} \tag{A.16}$$

where E_{p} and E_{n} are the amplitudes of the positive and negative voltage vectors, respectively, and the corresponding phase angles are denoted by φ_{p} and φ_{n}.

When transforming the voltage vector $\underline{u}^{(\alpha\beta)}$ from the fixed $\alpha\beta$-plane to the rotating dq-coordinate system, two rotating frames can be used, accordingly. These two frames are called positive and negative synchronous reference frames (SRFs) and are denoted as dqp- and dqn-plane: the positive SRF rotates counterclockwise with the angular frequency, while the negative SRF rotates clockwise with the same frequency. These two frames can be defined by the following transformations

$$\underline{u}^{(dqp)}(t) = e^{-\mathrm{j}\theta(t)} \underline{u}^{(\alpha\beta)}(t) \tag{A.17}$$

$$\underline{u}^{(dqn)}(t) = e^{\mathrm{j}\theta(t)} \underline{u}^{(\alpha\beta)}(t) \tag{A.18}$$

$$\tag{A.19}$$

From the latter, it is straightforward to understand that a positive-sequence component corresponds to a DC-component (zero frequency) in the positive SRF, while a negative-sequence component corresponds to a vector that rotates with 100 Hz clockwise in the positive SRF

$$\underline{u}_{\mathrm{n}}^{(dqp)}(t) = e^{-\mathrm{j}\theta(t)} e^{-\mathrm{j}\theta(t)} \underline{u}^{(dqn)}(t) = e^{\mathrm{j}2\theta(t)} \underline{u}^{(dqn)}(t) \tag{A.20}$$

$$\tag{A.21}$$

An analogous relation can be derived for a positive-sequence component in the negative SRF.