

# CHALMERS



## Physical Simulation of GaN based HEMT

*Thesis for Erasmus Mundus Master Programme Nanoscience & Nanotechnology*

ABHITOSH VAIS

Microwave Electronics Laboratory  
Department of Microtechnology and Nanoscience  
CHALMERS UNIVERSITY OF TECHNOLOGY  
Gothenburg, Sweden 2012





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ABHITOSH VAIS

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Coordinators:

Dr. Niklas Rorsman, MC2, Chalmers University, Sweden

Dr. Hans Hjelmgren, MC2, Chalmers University, Sweden

Dr. Marc Heyns, Katholieke Universiteit Leuven, Belgium

Microwave Electronics Laboratory  
Department of Microtechnology and Nanoscience  
Chalmers University of Technology  
SE-412 96 Göteborg  
Sweden  
Telephone + 46 (0)31-772 1000

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## Abstract

Recent improvements in the understanding and fabrication of GaN have led to its application in high frequency communication and high voltage switching systems. Requirement for operation at even higher frequency and voltages is driving the research currently on design of GaN based devices which can operate at frequencies above 30 GHz and voltages up to 100 V. Reliability issues with GaN based devices operating in such conditions and lack of understanding of various phenomena are some of the factors hindering their widespread commercial development. There is a need to understand the device operation by developing a simulation model, as close to reality as possible, which could be, further, used to optimize the device design for high frequency and power operation.

This thesis work reports the design and development of a physical simulation model of AlGa<sub>N</sub>/Ga<sub>N</sub> High Electron Mobility Transistor (HEMT) using commercial software (Synopsys, Sentaurus TCAD). The model is calibrated against measurement data. The results show a close matching with measured data, although some discrepancies have been found in the linear region of DC operation and high frequency regime of AC analysis. It is observed that trap density and their energy level (surface and bulk) play an important role in device characteristics. Effects of including quantum calculations in the model are analyzed. Various methods to improve the operating frequency have been investigated. The results show that by tuning the drain to gate distance, gate length and AlGa<sub>N</sub> thickness, AC characteristics can be improved significantly ( $f_{max} > 150$  GHz). The influence of changing the epitaxial layer structure (adding more layers) on the device's AC characteristics is analysed to find an optimum design for high frequency applications.



## **Acknowledgements**

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Abhitosh Vais, Gothenburg 2012





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# Notations

## NOTATIONS

$C_{ds,gs}$	Drain/gate to source capacitance
$C_{gd}$	Drain to gate capacitance
$C_{pg,pd,ps}$	Pad capacitances to electrodes
$\Delta E_c$	Conduction band discontinuity
$\Delta E_g$	Band gap difference of heterojunction materials
$\Delta E_v$	Valence band discontinuity
$E_g$	Band gap energy
$E_{br}$	Breakdown voltage
$E_{fn}$	Electron Quasi fermi level
$E_F$	Fermi Level
$L_{g,s,d}$	Gate/Source/Drain contact inductance
$N_C$	Effective density of states
$P$	Polarization
$P^{sp}$	Spontaneous polarization
$P^{pz}$	Piezo-electric polarization
$q$	Electron charge
$R_{g,s,d}$	Gate/Source/Drain contact resistance
$R_{ds,gs}$	Drain/gate to source resistance
$v_{sat}$	Saturation velocity
$V_T$	Threshold voltage of HEMT
$xAlGaN$	Aluminium molefraction in GaN
$\mu$	Carrier Mobility

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$\rho_b$	Interface charge density
$\sigma$	Sheet Charge
$\phi_b$	Schottky barrier

## ABBREVIATIONS

AlGaN	Aluminium-Gallium-Nitride
BTE	Boltzmann Transport Equation
CMOS	Complimentary Metal-Oxide Transistor
GaN	Gallium-Nitride
GaAs	Gallium-Arsenide
HEMT	High Electron Mobility Transistor
HBT	Hetero-junction Bipolar Transistor
HCP	Hexagonal Close packed
InGaP	Indium-Gallium-Phosphide
JM	Johnson's figure of Merit
LED	Light Emitting Diode
LD	Laser Diode
MBE	Molecular Beam Epitaxy
MESFET	MEtal Semiconductor Field Effect Transistor
RF	Radio Frequency
SiC	Silicon Carbide
TCAD	Technology Computer Aided Design
2DEG	Two Dimensional Electron Gas

# 1

## Introduction

Silicon Technology has dominated the semiconductor device industry since 1960s, with its established CMOS process and in-depth material know-how [1]. However there are some applications like Light Emitting Diodes (LEDs), Laser Diodes (LDs) and Radio Frequency (RF) devices where compound semiconductors have been the workhorse materials. The reason can be attributed to physical properties like electron mobility and band-gap. Limited mobility, low band-gap (lower breakdown voltage) and low operating temperature limits the current carrying and output power generation capability of traditional silicon based devices.

### 1.1 Background

High output power at high frequencies is required in wireless communication (satellite communications, TV broadcasting, broadband wireless internet connection, transmitter base station amplifiers) and military applications (radars, missile seekers) [2].

The typical III-V semiconductors (As-based) achieved significant success in optoelectronic devices, i.e LEDs, LDs, with a wide spectral range, and High Electron Mobility Transistors (HEMT). But growing requirement for higher output power generation in case of RF and wider spectral range in LDs require new semiconductor materials and device designs [3]. A variety of power amplifier technologies with different materials of suitable band-gap are vying for market share, such as GaAs (or GaAs/InGaP) hetero-junction bipolar transistors (HBT) and HEMTs, SiC MESFETs, and GaN HEMTs [4]. Some of the material properties of various contenders are listed in Table 1.1.

A measure, Johnson's figure of merit (JM), for various materials is listed in Table 1.1 to check for the suitability of a particular material in high frequency and power applications. JM is a product of the breakdown electric field,  $E_{br}$  and saturation velocity,  $v_{sat}$ . It implies that for applicability in RF applications, the value of JM for a material should be high [5]. By comparing the JM values in Table 1.1, the materials which have



**Table 1.1:** Material Properties for three semiconductors [4,5]

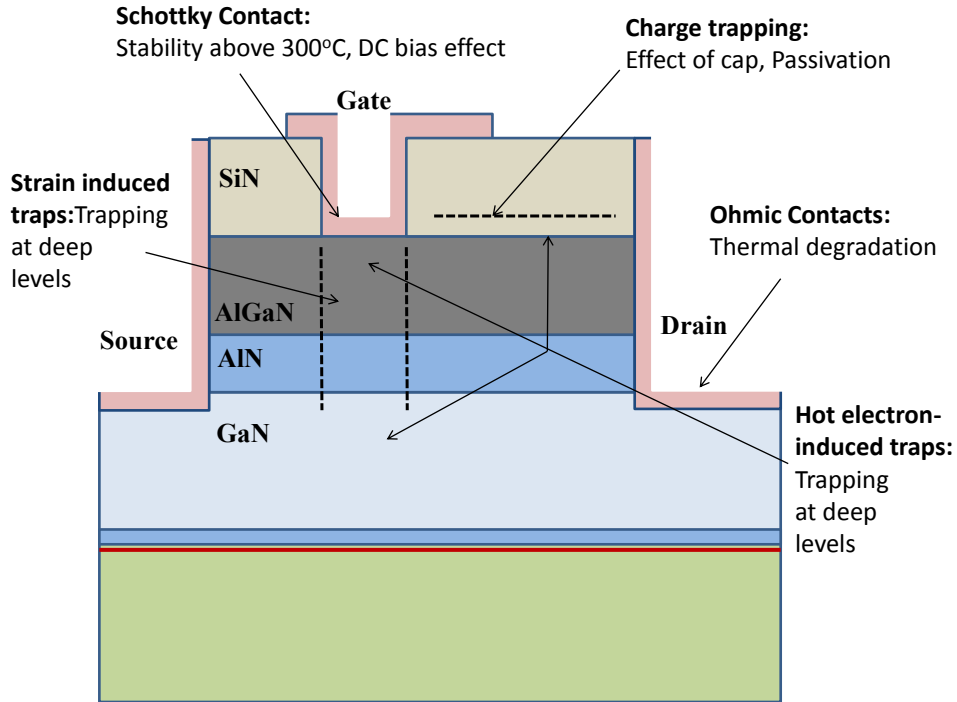
Property	4H-SiC	GaAs	GaN
$E_g$ (eV)	3.26 (Indirect)	1.42 (Direct)	3.42 (Direct)
$\mu$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	700	8500	2000
$v_{sat}$ ( $10^7$ m/s)	2	1	2.5
Ebr (MV/cm)	3	0.4	3.3
JM	60	3.5	80

better properties for RF power applications are SiC and GaN.

In addition to large band-gap and higher JM, the polar nature of the GaN crystal gives it an edge over other materials. The crystal polarization in GaN and AlGaN leads to the formation of charged interfaces. This results in accumulation of electrons and holes near the interface. In addition, piezo-electric polarization due to induced strain at hetero-interfaces gives rise to additional charges at the interface. Piezo-electric polarization in nitrides have been found to be ten times higher than in arsenides [6,7]. These two charge accumulation mechanisms result in very high polarization based electron density in GaN-based hetero-structures very near to the interface. This 2 Dimensional Electron Gas (2DEG) forms even without any significant doping [8]. The absence of doping and spatial separation of channel electrons from ionized donors leads to the reduction of ionized impurity scattering and, consequently, an increase in electron mobility. The resulting 2DEG density in GaN-based devices has been reported to be around and, in many cases, above  $10^{13} \text{cm}^{-2}$ , making it almost six times larger than that of a GaAs HEMT [3]. A higher mobility and electron density leads to higher output current density. Nowadays, the reported output power density of 30-40 W/mm is more than ten times higher than that of GaAs based transistors. Thus, for the same output power, device size can be reduced by the same factor using GaN [4].

Compared to other competitive materials like GaAs and SiC, the advantage of GaN rests on wider and direct band-gap (for opto-electronic applications), which allows for short wavelength laser diodes and LEDs [9,10,11], and high breakdown voltage (for RF applications) [12]. But, with all the remarkable properties and promises which GaN shows, the reliability and stability of such devices is still an issue [13,14,15]. A number of issues and their possible location are shown in figure 1.1.

GaN based hetero-structures are very complex in nature because of their polarized crystal structure and influence of surface and bulk traps. To make matter worse, effect of traps is twofold. They have been found to play an important role in the formation of the 2DEG and in the conduction of these electrons as well[13]. Moreover, they also cause various device degradation mechanisms during operation like current collapse and self-heating. The current collapse is a transient reduction in drain current due to trapping effects at the surface and in the bulk with sudden transients in gate and drain voltages [16,17,18]. Lack of understanding of formation of traps in GaN and their effect on



**Figure 1.1:** Various Device degradation mechanisms in AlGaIn/GaN HEMTs [13]

device current characteristics is a major factor which restrains the commercial growth of GaN based devices. Furthermore, the ever-increasing demand for higher frequencies of operation requires an optimization of various device parameters like lateral dimensions and epitaxial structure.

To predict device operation at higher frequencies, it becomes necessary to improve our understanding of various phenomena taking place inside the device. Numerical simulation is a good way to understand the device physics and behavior for different combinations of voltages, doping and trap levels and concentrations. It is being used widely to improve the comprehension of device operation by creating a model of the real device, sometimes called a simulation deck, including various phenomena happening inside. It can be used to compare, re-produce and sometimes predict the experimental output. It is not only an easy way to check or validate some complex parameter scenario and its effect on device behavior but it also saves a lot of device fabrication money.

## 1.2 Aim and Objectives

The aim of this thesis is to develop a physical simulation model for AlGaIn/GaN based HEMT to improve the understanding of the device for high frequency operation. This task includes the following objectives:

- As an initial step, develop a simulation deck for AlGaIn/GaN based HEMT includ-

ing all the physical models to simulate effects like traps and self-heating.

- Compare and calibrate the simulation deck with respect to the measured DC data.
- Propose and implement ways of optimizing GaN HEMTs in terms of operation at high frequencies (20-100 GHz).

### 1.3 Outline

The thesis is organized in the following way:

Chapter 2 introduces the physical aspects of III-N materials concentrating on GaN. Its crystal and electrical properties are discussed, leading to discussion on the polarization effects. A discussion on AlGaN/GaN heterostructures and resulting physical phenomena, such as band discontinuity and polarization induced bound charge follows leading to a discussion on the origins of the resulting 2DEG. Finally, the operation of AlGaN/GaN HEMTs is explained.

Chapter 3 concentrates on the methods and tools used in this work, i.e. the commercial simulator, Sentaurus, by Synopsys and scripts which were developed to perform various parts of simulation. In addition, various physical models used in the simulation to emulate the device is described.

Chapter 4 shows the results of simulations like DC, transient and AC analysis. Besides that, the calibration of the simulation deck with respect to measured data is described. The effect of each calibration parameter on the simulation is described separately. In addition, comparison of simulated and measured data after calibration is shown. It further concentrates on ways to improve and optimize the performance of the device for higher frequency ranges by varying the device structure.

Chapter 5 summarizes the results obtained in previous chapters and draws the corresponding conclusions. It also outlines future work to be done to improve the reliability of GaN HEMT simulations with respect to real devices.

# 2

## GaN Physics

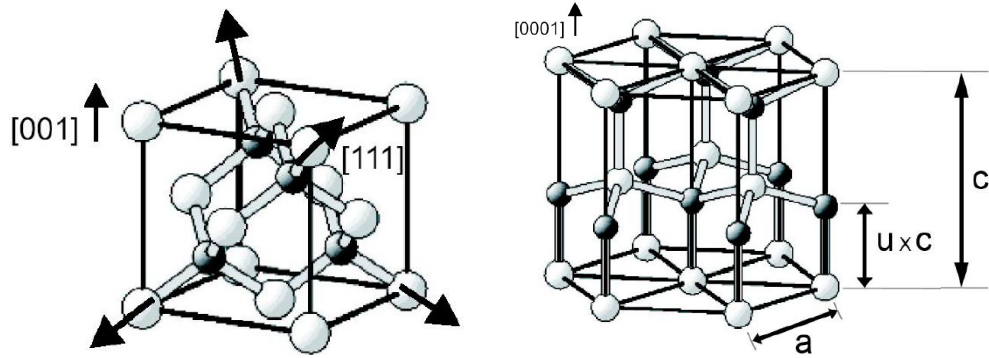
**T**his chapter introduces the physical aspects of III-Nitride materials concentrating on GaN, its material properties and polarization effects. Section 2.1 provides an overview of structural and electrical properties of GaN leading to a discussion on polarization effects. Section 2.2 consists of a discussion on AlGaN/GaN hetero-structures and resulting physical phenomena, such as band discontinuity and polarization induced bound charge, continuing with a discussion on origins of the 2DEG. In section 2.3, the AlGaN/GaN HEMT device and its operation is explained. Finally, in section 2.4, the technological challenges in the design of such a device are discussed.

### 2.1 GaN: The Material

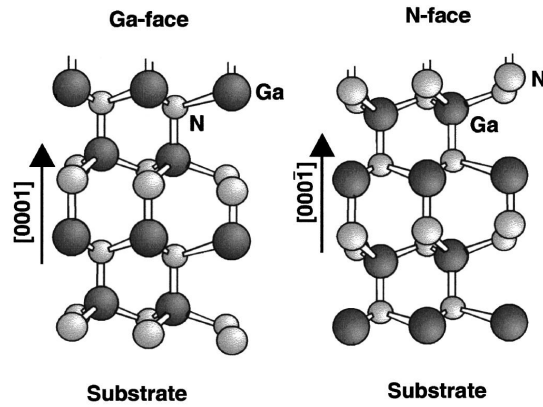
#### 2.1.1 Structural Properties

Nitride based semiconductors (AlN, GaN, InN) generally crystallize in two types of crystal structures, wurtzite hexagonal close packed (HCP) and cubic zinc-blende, where wurtzite has been found to be a more stable structure. As a result of this inherent stability, wurtzite HCP is preferred for fabricating devices. The wurtzite crystal structure has four atoms per unit cell in a hexagonal Bravais lattice [20]. The three lattice parameters are the length of a side of the hexagonal base,  $a$ , the height,  $c$  and the III-N bond length along the  $c$ -axis,  $u$ .

Crystals with non-centro-symmetric structure, like GaN, show different layer sequencing of atoms when one moves from one side of the crystal to the other in opposite directions. The GaN wurtzite HCP structure shows this crystallographic polarity along the  $c$ -axis (perpendicular to the basal plane of GaN crystal structure [21]). It is in this direction that Ga and N atoms arrange themselves in atomic bilayers. These bilayers consist of two closely spaced hexagonal layers, formed by Ga (cation) and N (anion), resulting into polar faces due to the electronegativity difference between composite atoms (Ga-and N- face) [21]. Polarization is a macroscopic material property in which differ-



**Figure 2.1:** III-Nitrides crystal structures, Cubic Zinc Blend (Left) and HCP Wurtzite (right) [19]



**Figure 2.2:** Another depiction of the GaN crystal structure with Ga and N face growth [21]

ence in electronegativity between atoms making bonds with each other results in the shift of positive and negative charge centers. This polarization of atomic bonds leads to the creation of dipoles with dipole moments whose direction depends on the type of bonding atoms [22]. In the absence of any electric field, orientation of these dipoles is random and the net polarization is zero. But in the case of GaN, which lacks symmetry in  $c$ -axis, the presence of an inherent electric field due to asymmetry can result in the formation and subsequent maintenance of a permanent dipole moment which results in polarization of the material. This kind of polarization is called *Spontaneous polarization* as it does not require any external force like electric field or deformation.

Epitaxial growth of semiconductor materials with different lattice constants causes mechanical strain. AlGaIn layer grown on GaN experiences this kind of strain. Due to the piezo-electric property, this leads to additional polarization at the interface, *Piezo-electric polarization*. Since the elasticity of a material determines the proportionality

between external stresses and internal deformation, it becomes crucial to study the elastic properties of these materials in order to understand the operation and reliability of any device grown on such layers. It becomes more important in the case of GaN because of its high piezo-electric polarization (almost 10 times as high as GaAs [4,21]).

### 2.1.2 Electrical Properties

A semiconductor material for high frequency and high output power applications should have a wide energy gap, a low value of dielectric constant, high thermal conductivity, and high breakdown field. Wide band-gap provides an ability to support high internal electric fields before breakdown occurs and also results in improved radiation resistance.

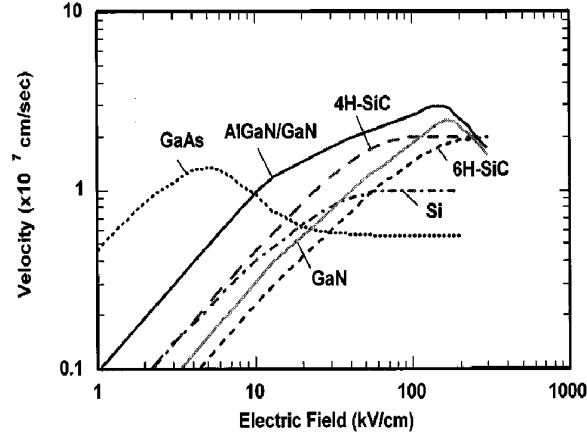
The dielectric constant indicates the capacitive loading capability of a transistor and affects the device terminal impedances [4]. The dielectric constant of wide band-gap semiconductors is about 20% lower than the conventional semiconductors which permit them to be about 20% larger in area for a given impedance. Increased area allows for higher RF currents, and therefore higher RF power.

The thermal conductance of the material defines the ease with which power can be dissipated from the device which, otherwise, would result in higher chip temperatures and degraded performance. Finally, the critical electric field for electronic breakdown is an indication of the strength of the electric fields that can be supported internally by the device before breakdown. Higher electric fields permit large terminal RF voltages which is necessary for the generation of high RF power. As discussed in section 1, the band-gap of III-Nitride material is very high (a direct band-gap of 3.42eV for GaN) which results into a high breakdown electric field (3.3 MV/cm for GaN) [4,12]. In addition, if they are grown on high conductivity substrates like SiC, it adds up to its good thermal conduction properties.

Band-gap and other electrical properties of ternary nitrides like AlGa<sub>x</sub>N can be computed by interpolation using Vegard's law given by the formula,

$$P(\text{Al}_x\text{Ga}_{1-x}\text{N}) = xP(\text{AlN}) + (1 - x)P(\text{GaN}) + bx(1 - x) \quad (2.1)$$

where  $P(x)$  represents the electrical property to be interpolated and  $b$  represents the bowing parameter which has to be experimentally determined for accurate interpolation. The current flowing in the device depends on the mobility of the charge carriers which, in turn, is the ratio of carrier velocity and applied electric field across the device [4]. If we look at the carrier velocity versus electric field ( $v$ - $E$ ) characteristics for various semiconductors, shown in figure 2.3, we observe that the carrier velocity is comparatively high for GaN and its peak velocity is observed at very high electric fields. These characteristics not only result in high output current but also operation at very high electric fields. Although mobility of GaN for low fields is not as high as for GaAs, the current is still high due to the high 2DEG density.



**Figure 2.3:** Saturation Velocity vs electric field characteristics of various semiconductors compared to GaN [3]

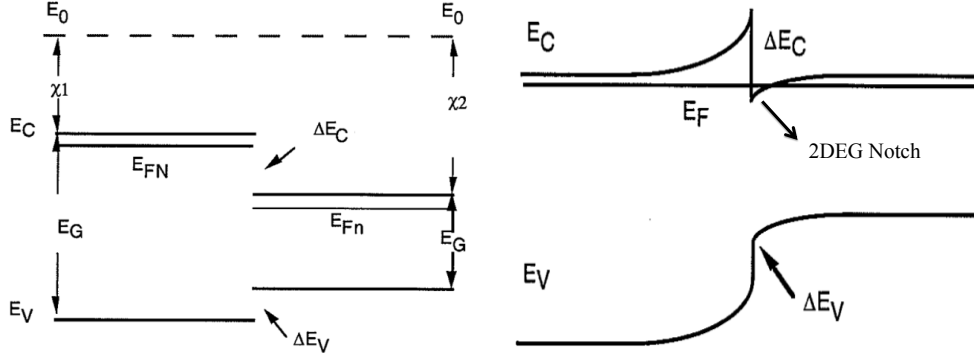
## 2.2 AlGaN/GaN: The Heterostructure

### 2.2.1 Hetero-structure: Band Gap Discontinuity

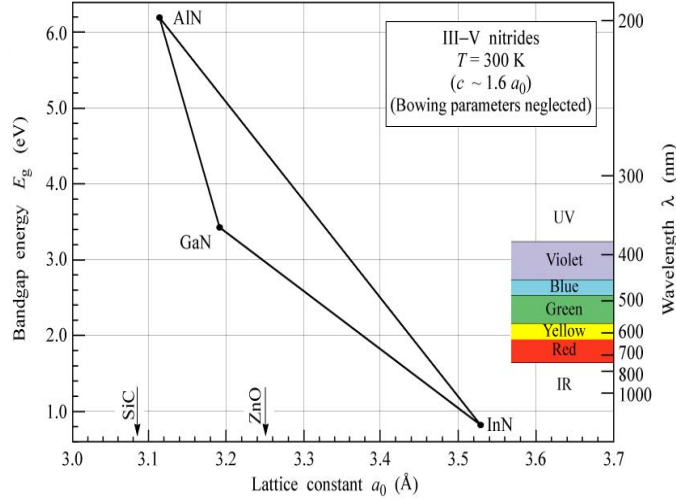
A hetero-structure is formed when two different materials are joined together or grown one over the other keeping the same crystal structure. When such a hetero-junction is formed between two materials having a large band gap difference, an energy discontinuity is created in the band diagram. Figure 2.4 visualizes a band diagram of AlGaN/GaN hetero-structure before and after the junction formation. As can be seen from the figure, the band gap discontinuity results in the formation of a notch in the conduction band at the interface and a valley in the valence band, both of which are present in the lower band gap material which, in the present case, is GaN.

The quality of the junction formed between such materials depends upon the difference between their lattice constants. The larger the difference in lattice constant of two materials, the larger is the possibility of the interface defects. The matching of lattice constant is the primary requirement for the formation of a good hetero-junction and hence, a good hetero-structure based device. If the materials to be joined are AlGaN and GaN, the parameter to be considered is the fraction of aluminum as it defines the bandgap and lattice constant of AlGaN. As shown in figure 2.5, both the lattice constant and the bandgap of the alloy changes significantly with the Al fraction.

Band gap discontinuity ( $\Delta E_g$ ) is given by the difference in the band gap of two materials. Conduction band discontinuity ( $\Delta E_c$ ) is calculated by locating the position of neutral levels in the material. In most cases, it is calculated as  $\Delta E_c = 0.68\Delta E_g$ [24]. The value  $\Delta E_c$  defines the depth of the notch, sometimes termed as Quantum Well as electrons are confined into quantum levels. As will become clear after next section, the relative position of this notch with respect to the Fermi level in the lower band gap material and its corresponding depth determines the density of charge carriers, and hence, the operation of any device using the heterojunction 2DEG [24].



**Figure 2.4:** Energy Band diagram for AlGaN/GaN Heterostructure, before(left) and after(right) the contact [24]



**Figure 2.5:** Band gap vs lattice constant for various binary III-V semiconductors [23]

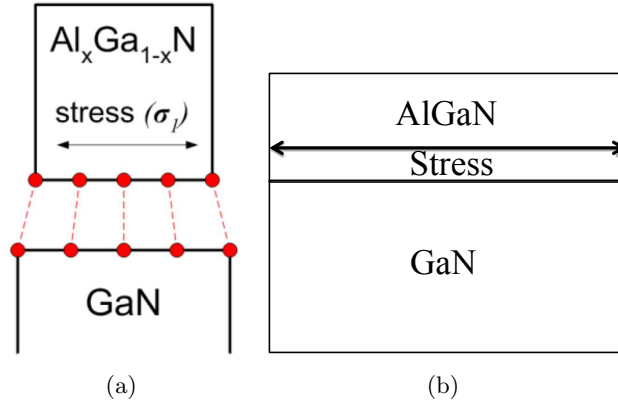
### 2.2.2 Polarization in AlGaN/GaN: 2 Dimensional Electron Gas (2DEG)

In a conventional semiconductor heterostructure like AlGaAs/GaAs, the large band gap material (AlGaAs) is intentionally doped so that when the heterojunction is formed, electrons diffuse from AlGaAs to GaAs. Due to the presence of a notch nearby the interface on the GaAs side, they accumulate and form a 2DEG. The density of carriers in the 2DEG depends on the doping in AlGaAs. Since doping in GaAs is low or negligible, the impurity scattering is small and we get a high mobility, especially at low temperatures [21]. To eliminate the possibility of reduced mobility due to extension of the 2DEG into the doped AlGaAs layer, an undoped spacer layer of AlGaAs is inserted between the junction and highly doped layer. As another option, only a part of the AlGaAs layer away from the junction is doped heavily so that, near the junction, it is still undoped.



In case of III-Nitride based devices, the principle behind the formation of 2DEG is basically different from that in conventional hetero-structures described above. In III-N based heterostructures, the dominant cause behind the accumulation of carriers at the interface is inherent net polarization, resulting in interface charge without the presence of any significant doping which further enhances their mobility.

As mentioned in previous section, III-Nitride materials possess an inherent spontaneous polarization whose direction depends on the growth face of the crystal (Ga or N at the surface). Since, the GaN substrate is comparatively thicker, it is formed in a relaxed state while the AlGaN is under stress as visualized in figure 2.6. Thus, in addition to spontaneous polarization, the strain developed in the AlGaN results in a piezo-electric polarization in AlGaN. When AlGaN is grown over the GaN substrate, due to the differ-



**Figure 2.6:** Stress is created in AlGaN layer due to lattice constant difference between AlGaN and GaN. Since GaN is a thick layer ( $1.8\mu\text{m}$ ), it is assumed to be formed in a relaxed layer [25]

ence in their polarization, a net polarization charge develops at the interface depending, again, on the face of growth of the crystal as shown in figure 2.7. The total charge can be calculated by integrating the polarization at the surface as follows [25]:

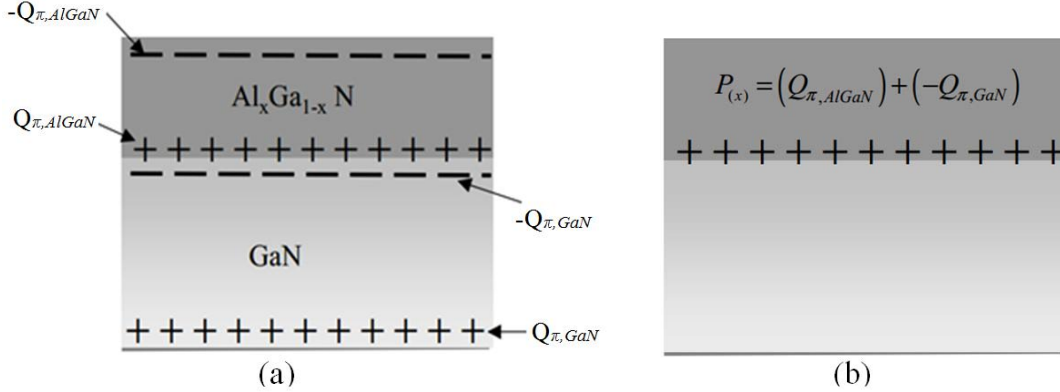
$$\oint \vec{P} \cdot d\vec{S} = -Q_b \quad (2.2)$$

$$\vec{\nabla} \cdot \vec{P} = \rho_b \quad (2.3)$$

$$\begin{aligned} \rho_b &= \frac{Q_b}{S} = -\frac{1}{S} \oint \vec{P} \cdot d\vec{S} = P_{\text{GaN}} - P_{\text{AlGaN}} \\ &= P_{\text{GaN}}^{sp} + P_{\text{GaN}}^{pz} - P_{\text{AlGaN}}^{sp} - P_{\text{AlGaN}}^{pz} \end{aligned} \quad (2.4)$$

Thus according to equation 2.4, this additional charge adds up to the charge associated with spontaneous polarization and, depending on its sign, either increases or decreases the total interface charge as described in figure 2.7.

If we consider the case of Ga face,  $c$ -axis grown GaN and AlGa $N$  layers for the structure, the polarization bound charge at the interface should be positive. This is due to the fact that the polarization in AlGa $N$  is larger compared to GaN and in the same direction (in case of stressed AlGa $N$  layer) [21]. Given the fact that piezo-electric



**Figure 2.7:** Polarization charge in AlGa $N$ /GaN Heterostructure, a) Charge polarization in individual materials,  $Q_{\pi,AlGaN}$  in AlGa $N$  is the sum of both Spontaneous and piezo-electric polarization,  $Q_{\pi,GaN}$  in GaN is only Spontaneous polarization as GaN has been assumed to be relaxed, b) Total sum of all the polarization results in a net positive charge at the interface [4]

coefficient is as high as 10 times in GaN as compared to GaAs, this addition results in a very high charge density at the interface. The presence of  $Q_{\pi}$  at the bottom side of GaN should result in a positive charge, but due to the presence of large number of electrons, traps and defects between 2DEG and substrate, there is almost negligible effect of such charge on 2DEG and hence, generally it is neglected in all computations [4]. It is to be noted that if the crystal has been grown in the direction of nitrogen atom at the surface, the charge developed due to polarization will be opposite.

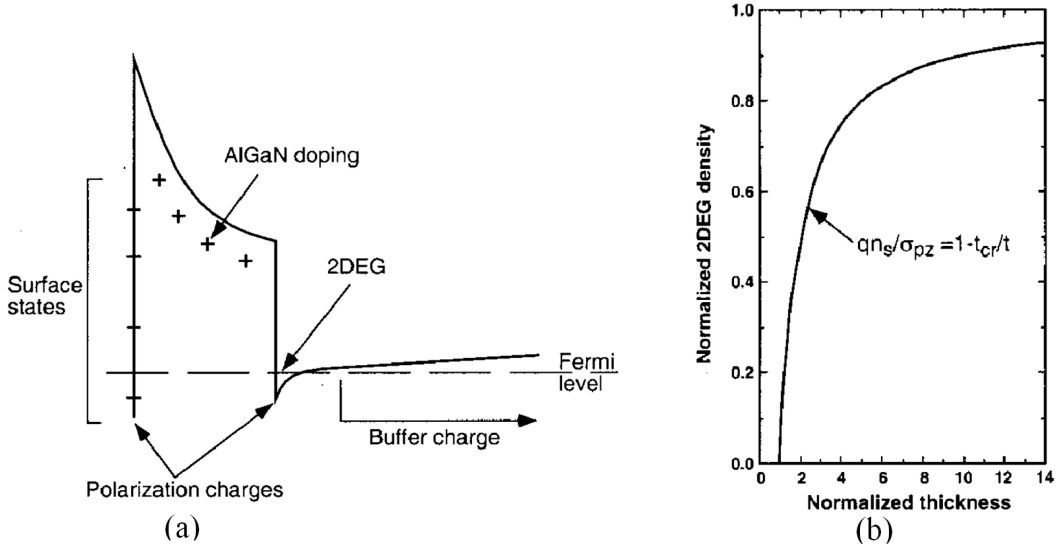
Although it is clear that there is positive charge at the interface of the AlGa $N$ /GaN hetero-structure, the device has to be neutral as a whole. The positive charge must be compensated by equal negative charge. In order to compensate for the positive charge, electrons accumulate at the interface and due to the presence of a notch at the hetero-junction, they form a 2DEG close to the interface.

But the question arises as where these electrons come from. Here we need to consider the type of charges present in the system. Firstly, there is charge due to polarization at the interface and AlGa $N$  surface ( $\pm\sigma_{PZ}$ ). In addition, charge due to electrons in 2DEG has to be counted ( $n_{2DEG}$ ). Moreover, the surface of AlGa $N$  consists of states due to broken bonds and other surface defects ( $\pm\sigma_{Surface}$ )[26]. Since, in our design, we have assumed the AlGa $N$  and GaN layer to be intrinsic, the charge due to donors is negligible. As the sheet charge due to polarization,  $\pm\sigma_{PZ}$ , is balanced, the remaining

terms of charge neutrality equation,

$$\sigma_{Surface} - n_{2DEG} = 0 \quad (2.5)$$

indicates that the source of electrons in 2DEG is the surface states [26]. The availability of these electrons to be accumulated in the 2DEG depends on the position of the energy level of these states with respect to the Fermi level. Interestingly, it has been found that the relative position of the surface states in AlGa<sub>N</sub> depends on the barrier layer thickness [26,27]. If we start with an assumption that there are no electrons in 2DEG. Due to the absence of charge neutrality, this creates an electric field due to polarization charges present at both sides of barrier layer. As the thickness increases, the resulting electric field increases, due to more charge at the interface, leading to a decrease in the difference between the Fermi level and the surface state energy level. At some thickness, this difference reduces to zero and it becomes possible for electrons to go to empty conduction band states to make a 2DEG. As the electrons fill more in 2DEG, the dipole strength reduces because of this screening, resulting in the reduction of electric field and hence, the relation between barrier thickness and 2DEG density saturates as shown in figure 2.8[27].

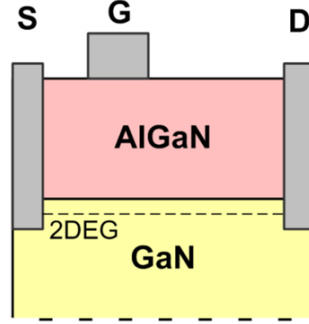


**Figure 2.8:** a) Charge distribution in AlGa<sub>N</sub>/Ga<sub>N</sub> hetero-structure in an energy band diagram with respect to surface states, b) 2DEG density dependence on barrier layer thickness [26]

## 2.3 AlGa<sub>N</sub>/Ga<sub>N</sub>: HEMT

A HEMT is very similar to a Field Effect Transistor in the sense that the current flowing between the source and drain terminals (ohmic contacts) is controlled by the electrical

field generated by the voltage applied at the gate terminal (Schottky barrier) perpendicular to the current direction as shown in figure 2.9. Electrons flow in the channel formed

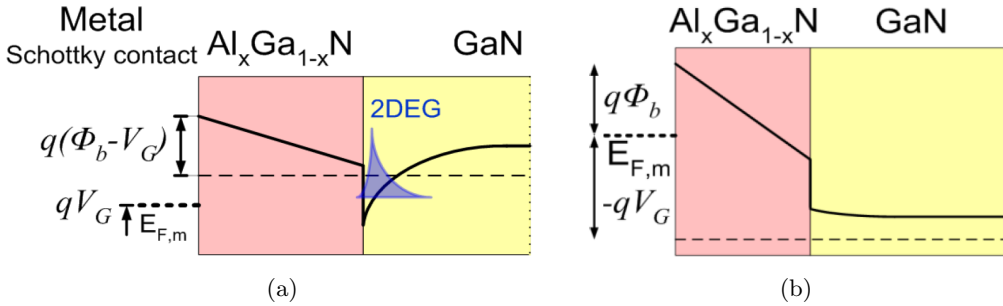


**Figure 2.9:** An AlGaN/GaN HEMT device structure. The 2DEG is formed inside the GaN layer, very near to the interface [25]

by the 2DEG region. The electron density in the channel depends on the voltage applied at the gate terminal as given in the expression [21]:

$$n_s(x,d) = \frac{\sigma_b(x)}{e} - \frac{\epsilon_0 \epsilon(x)}{e^2 d} (e(\phi_b(x) - V_G) + \Delta(x) - \Delta E_c(x)) \quad (2.6)$$

where  $n_s$  represent the electron density,  $\sigma_b$  is the sheet charge density,  $\epsilon$  is the dielectric constant of the barrier layer,  $\phi_b$  is the Schottky barrier height of the gate contact,  $V_G$  is the gate voltage and  $\Delta$  is the penetration of the conduction band into the Fermi level of the device. Thus, as the gate voltage amplitude is increased, the electron density decreases because the penetration of the conduction band edge into the Fermi level reduces as shown in figure 2.10. At the pinch-off voltage, the electron density effectively



**Figure 2.10:** Energy band diagram of 2DEG in a device cross section. a) Normally ON transistor state when the 2DEG is well below Fermi level to have high electron density, b) Conduction band edge at  $V_G < V_T$  when the edge is above Fermi level, an OFF state [25]

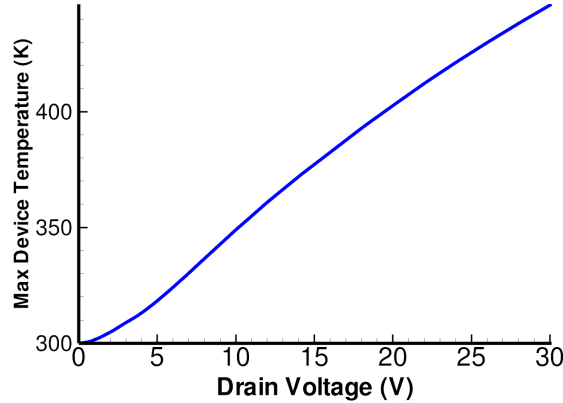
reduces to zero[24]. Since a negative voltage is needed to deplete the channel, it is called a depletion mode or normally ON transistor.

## 2.4 GaN: Technological Challenges

Issues related to GaN based device operation are discussed below.

### 2.4.1 Self Heating

Every good thing comes at some price. This applies to GaN technology too. Although GaN based devices have the advantage of high electron density, large band gap and hence high output current, the high current flow in the material generates a lot of heat which is referred to as self-heating as shown in figure 2.11. It increases the lattice temperature

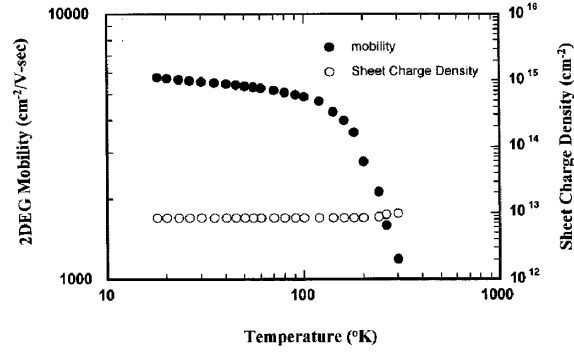


**Figure 2.11:** Simulation result showing the increase in device temperature with respect to increase in drain voltage,  $V_d$

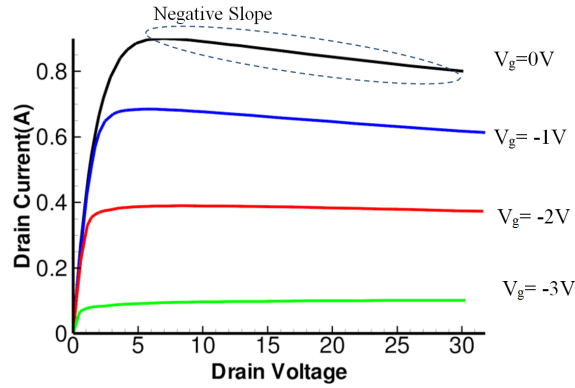
which, in turn, changes the temperature dependent material properties like band-gap and mobility, leading to the degradation of device performance as shown in figure 2.12. The reduction in mobility leads to a reduction in output current as the operation voltage is increased [13]. This reduction gives a negative slope to the saturation region of device DC  $I_d$ - $V_d$  characteristics in figure 2.13. The amount of self-heating depends upon the thermal conductivity of the materials used in the device[28]. Heat dissipation, thus, mainly depends on the type of substrate on which the device has been fabricated. It has been found by various research groups that the temperature rise in a GaN device fabricated on a SiC substrate is less than in those fabricated on sapphire substrates [3,4,13]. It can be convincingly reasoned that this is because of the relatively smaller thermal resistance of SiC as compared to sapphire. It is because of this reason that SiC is the preferred substrate material.

### 2.4.2 Bulk and Surface Traps

As mentioned earlier, any junction formed between two different materials with different lattice constant suffers from creation of traps and defect centers in the structure. The lattice constant difference and inherent stress in the material interfaces in hetero-structures



**Figure 2.12:** Change in 2DEG mobility with temperature. Also shown on right hand side axis is the corresponding variation in charge density [3]



**Figure 2.13:** Negative slope in  $I_D$  vs  $V_D$  characteristics due to self heating

leads to the formation of point defects and threading dislocations in the material which appears as defect levels inside the band gap in the energy band diagram. In addition to such defects, the unintentional impurities present in the material, due to fabrication processes, results in some extra defect levels in the band-gap which adds up to increase the recombination levels in the material. Due to their proximity to conduction band minimum or valence band maximum, depending on the type of trap, such defect levels have the potential to capture electrons or holes and trap them for a comparatively large amount of time [12,24]. This results in static or transient decrease in the electron density in the channel leading to reduction in output current.

Another important type of traps generated in hetero-structures are situated on the surface of the device. Breaking of 3D symmetry, in an otherwise bulk structure, leads to the formation of dangling bonds, surface impurities and other surface defects. Such defects form energy states in the energy band diagram which act as donor traps [12].

Such donor states can form positive surface charge and, as was discussed in previous section, are actually responsible for the 2DEG. It has been shown by various researchers that the density of surface traps plays a crucial role in the 2DEG density [21,26,27]. A change in the density of such traps has been shown to cause a significant change in the 2DEG density. Moreover, it has been speculated by many groups that at high gate voltage transients, such traps play a part in current collapse and gate tunneling [18,19,33].

Due to the impact of traps on output current, it becomes crucial to understand the trap locations in the energy band diagram and their densities. Since GaN is a comparatively new material, the knowledge of its properties and their variation with hetero-structure formation is not mature. The location, density and physical nature of traps has not, yet, been globally unified. There is still a considerable variation and, hence, a lot of confusion on the values to be used for parameters related to traps. A part of the reason behind this confusion is the variation in the type and levels of traps formed using different growth methods and their dependence on various parameters like pressure, temperature, interface, mole-fraction used for ternary compounds, the doping or unintentional impurities present in the system during fabrication. In addition, the trap levels are distributed all over the band-gap and it becomes difficult to model it using a single trap level. Moreover, deep trap levels can form due to various defects like impurities, point or line/extended defects [31,32].

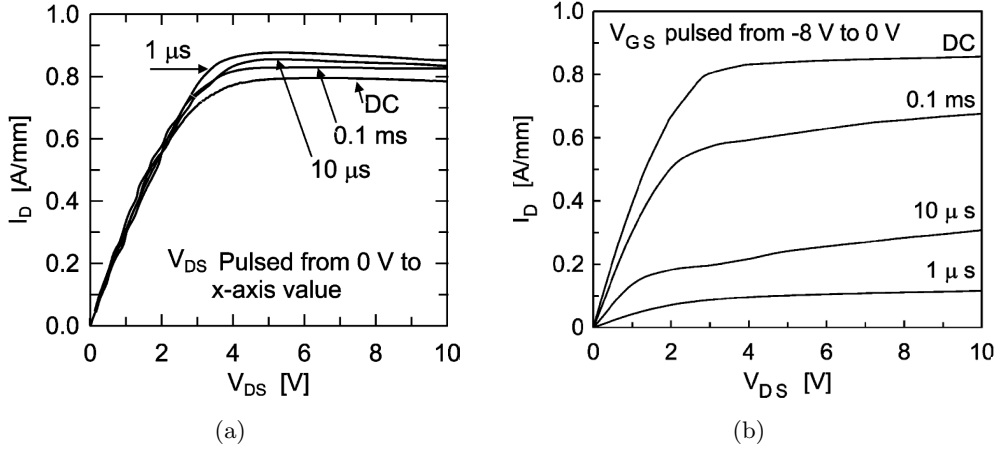
In this thesis, deep bulk acceptor traps have been assumed to be formed due to defects consisting of Ga vacancies, Nitrogen interstitials and VGa-O complexes at around 2.0 eV and 2.45 eV from the conduction band [33,35]. Although, reports on the trap levels in AlGaIn layer is rare to be found, similar levels of bulk acceptor traps have been assumed for it too.

### 2.4.3 Current Collapse

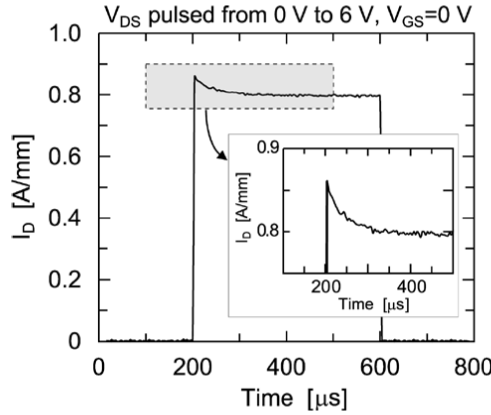
It has been observed and proven by experiments that when a high voltage transient is applied to the drain or gate, the output current is different from its corresponding DC value. However, it comes back to its DC value after some time as the current lags behind the voltage [17]. This difference was found to be negative (transient current larger than DC) for a drain transient and positive (transient current smaller than DC) in case of gate transient [18].

Since GaN based devices are to be used in high frequency applications, the current lag phenomenon becomes a crucial factor in commercial use of such devices and their corresponding success. It has been reported by some researchers that passivating the surface of the device with a passivation layer like Silicon Nitride decreases the current lag due to gate voltage transients [12]. But how much does it decrease and what happens to the drain lag is yet to be characterized. Many plausible reasons have been given to support the observation but all of them agree on the role of GaN and AlGaIn bulk traps [18,33].

Current lag due to drain voltage transients can be explained by the fact that when there is no drain voltage, electron density in the 2DEG is at its equilibrium value. Now,



**Figure 2.14:** Current lag comparison with corresponding DC values for various bias points on a) Drain voltage transient, b) Gate voltage Transient.  $V_{DS}$  and  $V_{GS}$  values are pulsed from 0V and  $V_t$  to the desired value using various pulse widths and each of such bias points and corresponding current values are plotted here to make a comparison with DC characteristics. It can be seen that in a) the transient current value is greater than DC, in b) it is less than DC [18]



**Figure 2.15:** Transient current catching up with DC value after the transient time due to de-trapping time taken by traps[18]

in the case of a DC state, at a particular voltage on the drain electrode, some of the electrons in 2DEG gain enough energy to jump from the channel and get trapped in the GaN bulk trap states. In addition, the capture of electrons by surface donor traps, due to the field created by the drain voltage, decreases the net positive charge on the surface near drain, hence reducing the 2DEG density. Thus, the DC current flowing through the channel is a value taking this entire phenomenon into consideration. It is obvious that for higher drain voltages, this event is more pronounced. Now, in case



of a transient voltage on drain, due to some slow trapping time required by traps to capture the high energy electrons, the reduction in 2DEG density due to trapping is comparatively smaller leading to a high 2DEG density even at non-zero  $V_d$  and hence a higher current compared to DC. It must be added that as time progresses, electrons get enough time to jump into the traps and hence, the current reduces back to its DC value. [18]

Current lag due to gate voltage transients can be understood by observing that when the device is off due to a negative voltage on the gate (beyond pinch-off), the 2DEG density underneath the gate is negligible. All the electrons in the channel get captured in the bulk traps or the surface states due to the field created by the gate voltage and shift in energy levels underneath the gate. When a gate transient is applied (a zero or positive voltage), due to the slow de-capturing time of the traps, not all of them are released back into the channel instantaneously. Thus, the transient 2DEG density is comparatively less than the DC value and hence, the transient current is lower. After some time (long enough for traps to release electrons), the 2DEG density comes back to its equilibrium value along with the current. [18]

# 3

## Simulation Methodology

This part of the report discusses the simulation tools and explains, in detail, the physical setup, properties and corresponding mathematical models used to develop the HEMT simulation platform. The simulation software used to perform the above task is Sentaurus TCAD software Version F-2011.09. To start with, brief information on the software is provided in section 3.1. In Section 3.2, the physical properties and corresponding mathematical models are discussed.

### 3.1 The Software

Technology Computer-Aided Design (TCAD) describes the process of developing and optimizing the semiconductor processing technologies and devices by using computer simulations. The software solves fundamental, physical partial differential equations, such as diffusion and transport equations, to model the structural properties and electrical behavior of a self-designed device structure. Sentaurus TCAD is one such software provided by Synopsys. The software package provides a selection of tools to perform above calculations which provides structured application of the software with visualization aids to observe the physical properties inside the device structure. The tools which have been used in this thesis include [36]:

- *Sentaurus Workbench (SWB)*, a framework designed to integrate all the other tools into a single entity to make it easier to perform sequential simulation, right from the structure creation to device operation simulations. It provides a flexibility to perform multiple simulations on a single device by parameterizing the structural and physical properties to check and observe, visually, the device characteristic variations depending on the values of some parameters in a single project as different experiments or scenarios. It automatically creates the output file of one tool and then, after its successful completion, passes the output files to next tool in the queue removing the need to control it manually by the user.

- *Sentaurus Structure Editor (SSE)*, a tool developed to design the structure of the device before simulation. It utilizes, as an input, a script file written by the user in order to create the structure. Due to the inherent flexibility mentioned above, the user is free to define any physical property or dimension of the device as a variable which can be changed to perform a series of experiments for different values of a parameter. It divides the structure into a series of discrete points on which physical equations will be solved by creating a mesh. The output file created by this tool contains the geometrical, material, contact and doping information about the device. It is this file that is used by other tools to perform device simulations.
- *Sentaurus Device (SD)*, a tool developed to solve numerically the set of diffusion and transport equations depending on the physical parameters and boundary conditions defined by the user in the virtual device to simulate the electrical behavior of the device. As mentioned above, the equations are solved at each discrete point in the mesh. It can be used to perform DC, AC and transient simulations and provides output files containing information on carrier densities, fields, potentials, energy levels and temperatures inside the device at various point of time during simulation.
- *Tecplot SV* and *Inspect*, a set of visualization tools to observe the 3D and 2D variations respectively, both in the device structure and during simulation.

## 3.2 Physical Models

In the Sentaurus TCAD software, a number of physical models are provided to describe the device physics as closely as possible to the real device. These models deal with the behavior of the carrier in combined effects of various boundary conditions like lattice temperature, electrostatic potentials and fields, external forces, hetero-structures band gap variations and quantum effects. Such models, depending on the type of device and operating conditions, have to be included in the model to perform simulations and do reliable predictions about the device characteristics. In this section, various models present in the software are discussed briefly. References have been given to refer for more information.

### 3.2.1 Current Transport Models

Sentaurus TCAD offers a number of transport models to suit various modeling designs and requirements. Depending on the type of material being used, all these methods can be generalized into three carrier transport models: *Drift-diffusion* (DD), *Thermodynamic* (TD) and *Hydrodynamic* (HD). Although all three of the above mentioned models are based on an ‘all-inclusive’ *Boltzmann Transport Equation* (BTE) differentiated by inclusion or exclusion of some specific physical phenomenon in BTE.

The *Drift-diffusion* (DD) model is Sentaurus’s default transport model which approximates, in a BTE, that the carrier flow inside the device is due to their drift and/or

diffusion under an external lateral or longitudinal field concurrently with recombination and generation of carriers. The current density under this model is described by the relation [36]:

$$J_n = -nq\mu_n\nabla\phi_n \quad (3.1)$$

$$J_p = -pq\mu_p\nabla\phi_p \quad (3.2)$$

where  $\mu_n$  and  $\mu_p$  are the electron and hole mobility respectively,  $\phi_n$  and  $\phi_p$  are the respective quasi Fermi levels.

The *Thermodynamic* (TD) model is an extension of the DD model with additional terms for temperature gradients in the device which makes it solve lattice temperature equations in addition to electron continuity equations. Given the current and voltage levels at which the GaN HEMT is to be operated, the heat generated and temperature inside the device and its corresponding effect on carrier behavior becomes important. The TD model is represented in Sentaurus TCAD by [36]

$$J_n = -nq\mu_n(\nabla\phi_n + P_n\nabla T) \quad (3.3)$$

$$J_p = -pq\mu_p(\nabla\phi_p + P_p\nabla T) \quad (3.4)$$

where  $P_n$  and  $P_p$  represents the thermal power generated and  $T$  is the lattice temperature.

The *Hydrodynamic* (HD) model utilizes a different approach to calculate carrier transport as compared to DD. It describes carrier transport based on energy balance equations where energy of each type of carrier (electron and hole) is calculated depending on its own temperature apart from lattice temperature. It also includes the spatial variation of electrostatic potential, carrier affinity and the band gap. The corresponding equations are [36,37]:

$$J_n = -q\mu_n(n\nabla E_c + kT_n\nabla n - nkT_n\nabla\ln\gamma_n + \lambda f_n^{td}kn\nabla T_n - 1.5nkT_n\nabla\ln m_n) \quad (3.5)$$

$$J_p = -q\mu_p(p\nabla E_c + kT_p\nabla p - pkT_p\nabla\ln\gamma_p + \lambda f_p^{td}kp\nabla T_p - 1.5nkT_p\nabla\ln m_p) \quad (3.6)$$

The first term takes into account the contribution due to the spatial variations of electrostatic potential, electron affinity, and the band gap. The remaining terms take into account the contribution due to the gradient of concentration, the carrier temperature gradients, and the spatial variation of the effective masses of the carriers.

It has been reported by some researchers that the DD model, in sub-micron gate lengths, often falls short of describing the model [38,39,40]. The speculated reason for this could be its inability to reproduce velocity overshoot effects, often seen in III-V semiconductors, because it does not take in to account effects due to hot electrons (only lattice temperature is accounted for and not the energy of carriers). Thus, at higher fields, they speculate that for short gate lengths, DD model should show discrepancies and the HD model, as it takes carrier energy in to account, should be more appropriate [38].

But in this thesis, a DD based mobility model, developed in-house after different calibrations with the measurements, has been used as it was found to give simulation

results sufficiently close to measurements. Thus, from here on in this report, only the DD model and corresponding equations will be assumed. Because of the high operating voltages, self-heating need to be accounted for. Hence, the thermodynamic model has been used in conjunction, to simultaneously solve temperature and carrier continuity equations.

### 3.2.2 Charge Distribution

The charge distribution model describes the statistical manner in which electronic states are distributed inside the conduction and valence band of the material at a particular temperature and energy. It is used to determine the electron density in the device by integrating, along with the density state function, across a particular energy band. Since the current characteristics in the device essentially depends on this density, the accuracy of this model is important for simulations. In GaN HEMT, the electron density in the channel is very high which makes Fermi statistics a good choice to be used as a charge distribution model as Boltzmann statistics are only accurate for low electron densities and temperatures. The fermi distribution is given by [24,36]:

$$f(E) = \frac{1}{1 + e^{\frac{E-E_f}{k_B T}}} \quad (3.7)$$

where  $E$  represents the energy level of electron,  $E_f$  is the Fermi level,  $T$  is the temperature and  $k_B$  represents the Boltzmann's constant.

### 3.2.3 Thermionic Emission and Tunneling

Transport equations mentioned in section 3.2.1 are valid in the bulk material but when it comes to interfaces at hetero-junctions, where there is an abrupt difference in bands, it is better to use special conditions for the interfaces. Thermionic emission, for high and thick enough energy barrier, is one such condition. As GaN HEMT is basically a hetero-structure device in which the current channel is very near to the interface, including thermionic emission improves the simulation accuracy. This model, when included in the simulations, calculates the effects of hetero-interface on the current flowing in the channel.

Although, the thermionic emission model takes care of current transport across and at the hetero-interface, the effects of gate electrode tunneling can only be included in the simulation, if the Nonlocal Tunneling model is activated. This model creates a special non-local mesh around the specified junction which consists of non-local lines that represents the tunneling path for carriers. This mesh is denser and specifically made for solving Poisson and continuity equations across the entire band-edge profile of the interface. [36]

### 3.2.4 Density Gradient Method

As mentioned in section related to 2DEG, the band discontinuity at the AlGa<sub>N</sub>/Ga<sub>N</sub> interface results in the formation of a notch in the conduction band. This notch acts as a triangular quantum well for the electrons residing in the 2DEG and consequently, resulting into quantization of energy levels in the 2DEG. Thus, electron distribution in the 2DEG with respect to energy states is different from normally assumed continuous distribution in bulk. It is much more accurate then, to include the quantization model in the simulation. Unfortunately, the Schrödinger equation solver for quantization is only available for 1D simulation. But another model using the density gradient method can be used to include quantization effects. This model does not solve the Schrödinger equation, but it changes the conduction and valence band energy distribution to more discrete-like levels which can be utilized as quantization. Mathematically, it adds up a quantization term to the conduction band energy equation for the same as shown in equation below [36]:

$$n = N_c F_{\frac{1}{2}} \left( \frac{E_{F,n} - E_c - \Lambda_n}{kT_n} \right) \quad (3.8)$$

$$\Lambda_n = - \frac{\gamma h^2}{6m_n} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \quad (3.9)$$

where  $\Lambda_n$  is the additional factor from density gradient model,  $\gamma$  is a fit factor, and  $m_n$  is the effective mass of electron. Inclusion of density gradient model makes simulation slower as an extra iterative step is added for density gradient computation. Thus, the question arises regarding the criticality of inclusion of this model. As it will become clear from the simulation results, although it changes the electron distribution across the 2DEG channel and affects the threshold voltage to some extent, the inclusion of density gradient model does not affect the current-voltage characteristics of the device. [36]

# 4

## Results

This chapter describes, in detail, the simulations performed, simulated structures and analysis of corresponding results. Section 4.1 provides the details of the general device structure used followed with results of simulation and calibration process. Section 4.2 describes the simulation methodology and corresponding results for optimizing the HEMT for higher frequencies. Section 4.3 consists of a discussion based on the analysis of all the above results.

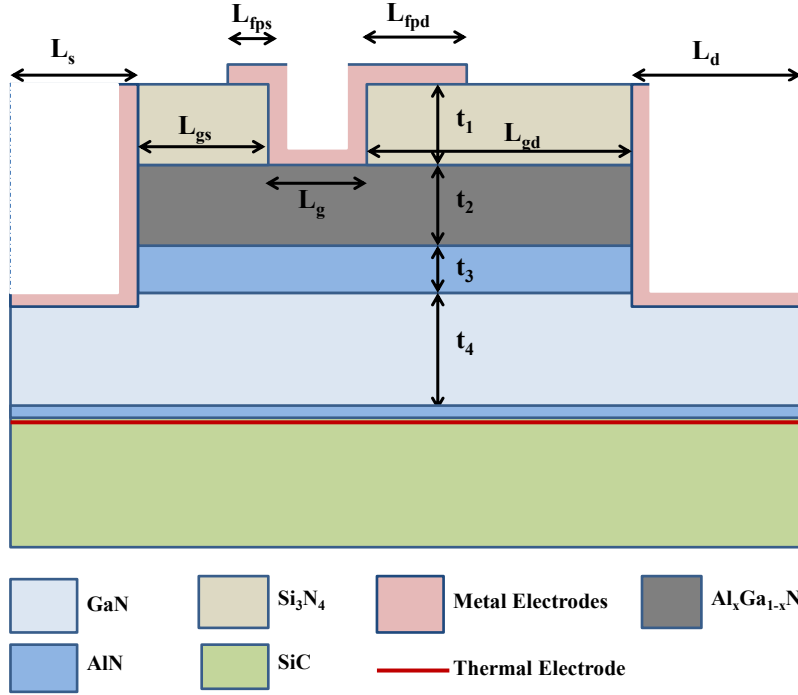
### 4.1 Model Calibration

#### 4.1.1 Device Structure

The simulated device structure, AlGa<sub>N</sub>/AlN/GaN/AlN/SiC, is shown in figure 4.1 and the corresponding dimensions are listed in table 4.1. A SiN passivation layer has been provided on the un-gated AlGa<sub>N</sub> surface to reduce the surface defects and current lagging [12,13]. An AlN layer is provided in between the AlGa<sub>N</sub> and GaN layers. Due to the wide band gap of AlN, it reduces the 2DEG electron wave-function penetration into the AlGa<sub>N</sub> barrier layer. A large band gap discontinuity also gives rise to a higher 2DEG density. To increase the breakdown voltage of the HEMT, a field plate on both sides of the gate electrode has been included [12,41,42].

In order to perform thermal simulations, a thermal electrode at the bottom of the AlN buffer layer of the device was added. Since SiC does not have any effect on the electrical performance, it has not been included in the design [38]. In order to include its material effects on thermal dissipation, the thermal resistance of the thermode has been adjusted to include the thermal resistance of SiC.

Basically, the design was done in two stages. In the first stage, simulations were done on a structure with specific dimensions (same as that of an available real device). It was followed by the calibration of the simulation deck by comparing the simulation results with the measured I/V data in the second stage.



**Figure 4.1:** Generalized structure of the simulated AlGaIn/AlN/GaN HEMT

**Table 4.1:** Geometrical parameters of the device and their description

Parameter	Description	Dimension (in $\mu\text{m}$ )
$t_1$	Thickness of Passivation layer (SiN)	0.050 - 0.060
$t_2$	Thickness of AlGaIn Barrier layer	0.019
$t_3$	Thickness of AlN barrier layer	0.001
$t_4$	Thickness of GaN layer	1.8
$L_g$	Gate electrode length	0.250
$L_{gs}$	Gate to source length	0.7
$L_{gd}$	Gate to drain length	2.0
$L_{fps}$	Field plate length on source side	0.1
$L_{fpd}$	Field plate length on drain side	0.350
$L_s$	Length of source electrode	50
$L_d$	Length of drain electrode	66

The whole device, except the source/drain contacts, has been assumed to be undoped. Although it is not an accurate representation of an actual device, it is to reduce the



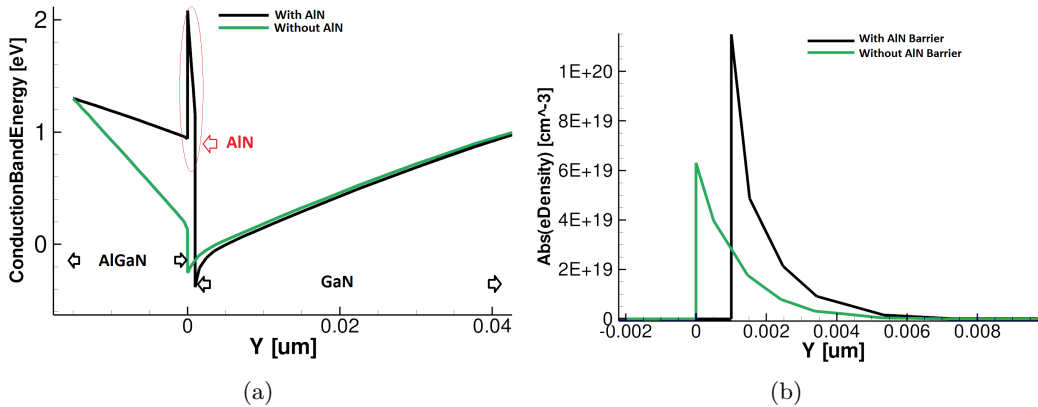
complexity of device simulation and confusion on the type and concentration of any unintentional doping present in an actual device. The drain and source contacts have been assumed to be ohmic and modeled in the device by doping the region under source and drain contacts with phosphorus of concentration  $10^{20} \text{ cm}^{-3}$ . Since most of the current flows close to the contact edges, only small part of the contact area is included to reduce the number of grid points.

The gate contact has been assumed to be of Schottky type. There is a huge variation in the value of Schottky barrier height used in the literature as it depends on the thickness of the layers, mole fraction of the AlGa<sub>N</sub> layer and the type of metal being used for the gate electrode. Since, there are no CV measurements available to ascertain the barrier height of fabricated devices, it was taken from values mentioned in different literature reports and adjusted (1.3eV - 1.6eV) to match the threshold voltage from I/V measurements. The contact resistance definitions for source and drain contacts was taken from measurements (0.4  $\Omega\text{mm}$ ) and the corresponding doping and resistance definitions in the simulation tool were adjusted to match it.

### 4.1.2 DC Simulation Results

#### Electron Density: 2DEG

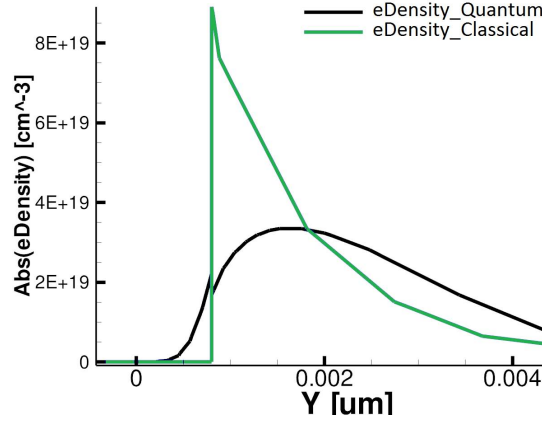
The advantage of including an AlN layer between AlGa<sub>N</sub> and Ga<sub>N</sub> is visualized in figure 4.2. As discussed in section 2.2.2, a heterostructure between AlGa<sub>N</sub> and Ga<sub>N</sub> results in the formation of a 2DEG very near to the interface. Simulations in figure 4.3 confirms that. Due to the presence of a high band gap material, the polarization at the



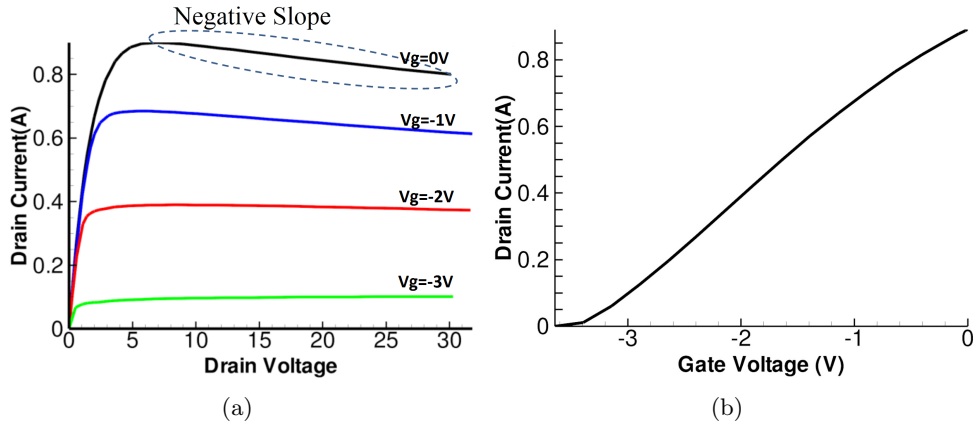
**Figure 4.2:** Effect of inclusion of AlN barrier layer in between AlGa<sub>N</sub> and Ga<sub>N</sub> layers. a) Comparison of conduction band energy diagram with and without AlN layer, b) Electron density in 2DEG with and without AlN layer. The shift in position of electron densities in (b) is due to the inclusion of AlN layer.

interface is larger which leads to higher electron density at the interface. Also, a larger band discontinuity results in reduction in the probability for a 2DEG electron wavefunction to crossover into AlGa<sub>N</sub>, and hence leading to improved mobility. An interesting

comparison has been made in figure 4.3 between electron density computations using a classical approach and a density gradient method approach which takes into account the quantization of energy levels in the potential well created by the band structure near the interface. It can be seen that the quantum approach calculates a better 2DEG approximation as the 2DEG is not formed exactly at the interface but a very small distance (1-2 nm) away from the interface and it is spread over some distances into both materials.



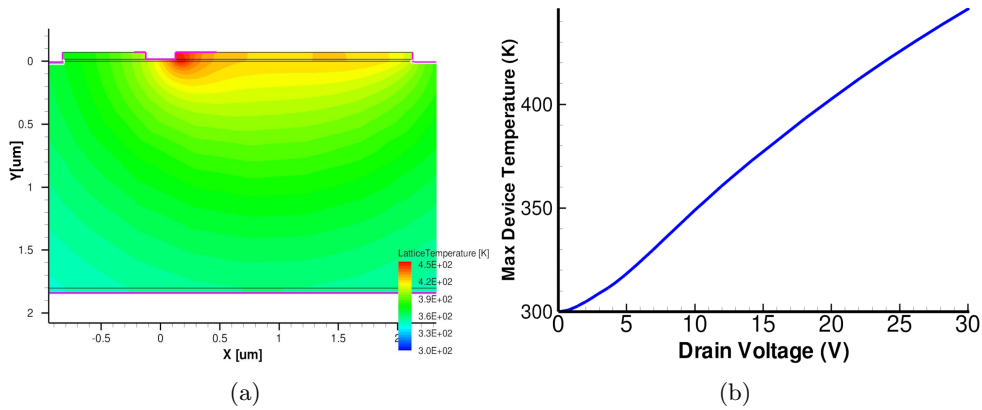
**Figure 4.3:** Electron density across the channel in a cross-section in the device using both classical and density gradient method. A very thin but high band gap AlN layer between AlGaN (left side) and GaN (right) can be clearly seen which decreases the probability of electron wavefunction in the AlGaN region



**Figure 4.4:** a)  $I_d$  vs  $V_d$  characteristics of the device, b)  $I_d$  vs  $V_g$  curve with a pinch off voltage of  $V_g = -3.25$  V. Here  $V_g$  = Gate Voltage,  $V_d$  = Drain Voltage.

### I/V Characteristics: Self-heating effect

Simulated I/V characteristics of above mentioned structure are shown in figure 4.4. It describes the drain current ( $I_d$ ) vs drain voltage ( $V_d$ ) characteristics of the device. As the drain voltage increases, the longitudinal field, current and carrier energy increase. This leads to ‘heating’ of the device and reduction of electron mobility which results in the reduction in current and hence a negative slope in the I/V characteristic curve as can be seen after  $V_d = 10$  V in figure 4.4a. The linear rise in temperature in the device, as shown in figure 4.5b, is concentrated at the drain side of the gate in the device because of the high electric fields and electron density experienced by this region as can be seen in figure 4.5a.



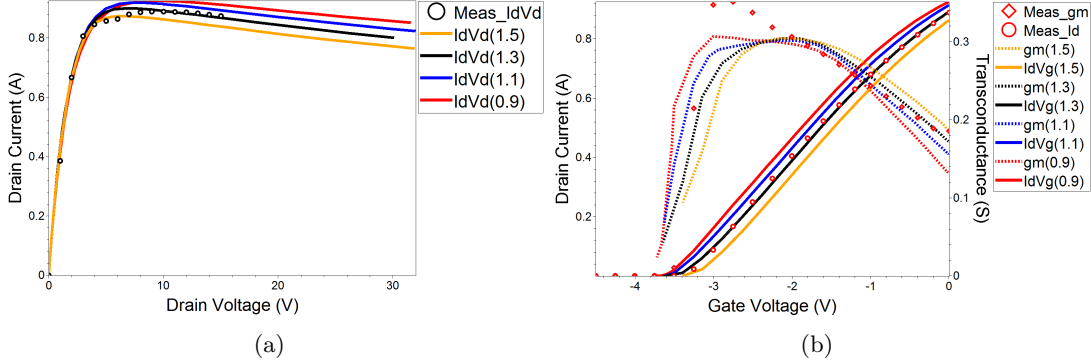
**Figure 4.5:** a) Temperature distribution in the active region of the device, b) Temperature rise with respect to drain voltage increase.

### 4.1.3 Calibration

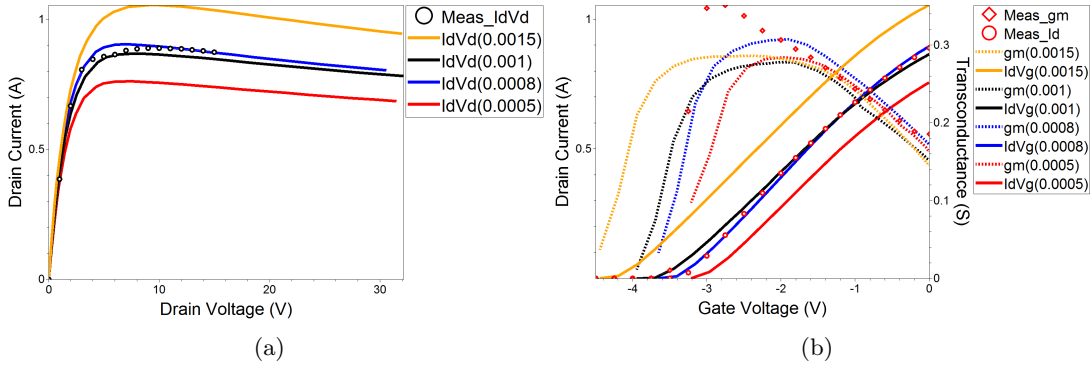
After initial simulations, there were still some parameters like trap energy levels and densities, Schottky barrier height of gate electrode, contact resistance of source and drain electrodes for which no exact values were available. In addition, various models used in the design needed to be calibrated to the current configuration. Thus, an exhaustive and iterative calibration procedure was done by comparing the simulation results with measurement on a similar device. Each of the above parameters (Schottky barrier height, contact resistance of source and drain electrodes, trap energy levels and densities) was varied to check for its effect on the comparison and to fine tune with respect to measurement data.

Schottky barrier height,  $\phi_b$ , affects the threshold voltage of the device in a way that higher the schottky barrier height, more positive voltage needs to be applied to get the same effect. Since gate voltage in case of a normally-on HEMT is negative, less negative gate voltage needs to be applied to turn it off. It was found that even by changing  $\phi_b$  to large extent, it could not match the measured  $V_t$ . The most probable

reason for this could be that the actual parameters in the real device were different from the given specifications which can be attributed to the variability factor in fabrication and material growth. This led to an investigation of various structural parameters that affect the threshold voltage. It was found that  $V_t$  was very sensitive to the AlGaIn thickness,  $t_2$ , (lesser the thickness, more the effect of gate voltage on channel), AlN thickness,  $t_3$ , (for the same reason as previous), Al mole fraction in AlGaIn and Schottky barrier. The corresponding effects of all parameters are shown in figure 4.6 - 4.10. The



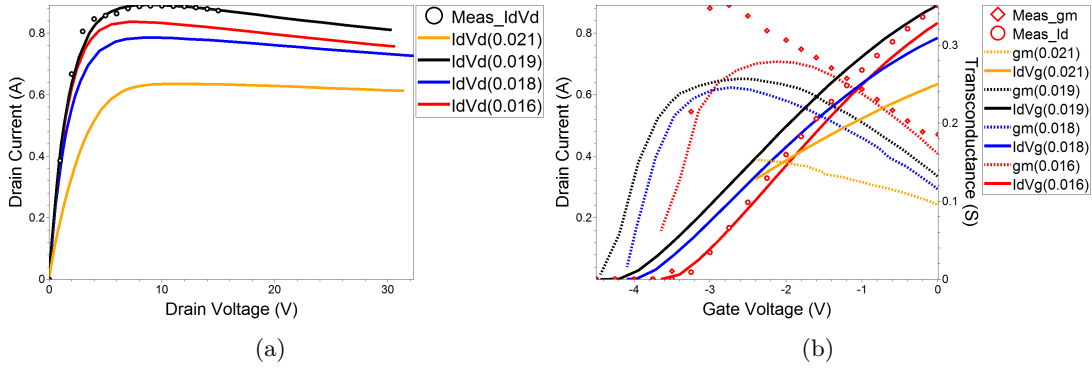
**Figure 4.6:** Effect of Schottky barrier height variation on a)  $I_d$  vs  $V_d$ , b)  $I_d$  vs  $V_g$ .



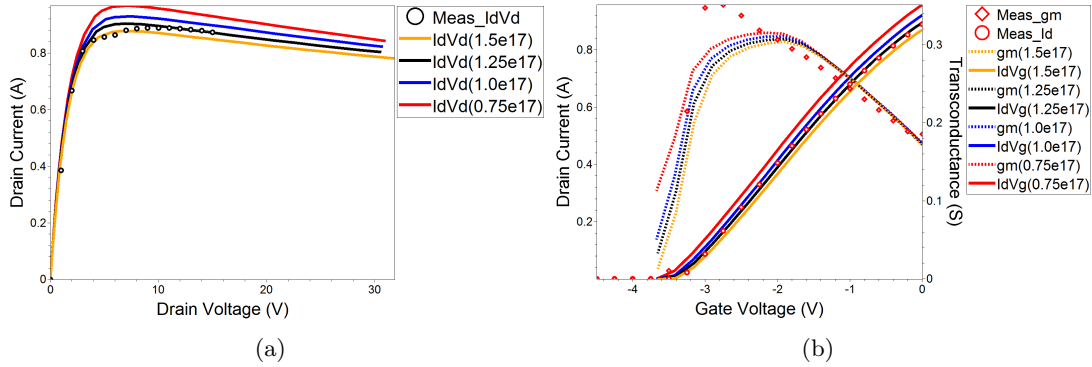
**Figure 4.7:** Effect of AlN thickness variation on a)  $I_d$  vs  $V_d$ , b)  $I_d$  vs  $V_g$ .

effect of AlN variation on output characteristics is due to the variation in 2DEG density. The  $I_d$  vs  $V_g$  curve shifts to the left with AlN thickness as distance between gate and channel increases, reducing gate control. The effect of changing the AlGaIn thickness on output characteristics is due to the combined variation in 2DEG density and gate-channel distance. The  $I_d$  vs  $V_g$  curve shifts to the left with the AlGaIn thickness for the same reason as for the AlN thickness. The gate length,  $L_g$ , also affects the threshold voltage. As the gate length increases, the gate control on the channel increases. After simulations, it was found that the effect is not that significant. Effect of bulk trap concentration on the 2DEG current density, and hence on the DC current characteristics is shown in

figure 4.9. As the trap density increases, more electrons from the channel are trapped in them leading to 2DEG reduction. It can be seen that there is not a significant shift in the threshold voltage in the  $I_d$  vs  $V_g$  curve for the same reason. Since traps only affects the 2DEG density, only a downward shift in drain current happens. The higher the bulk-trap concentration, the less is the 2DEG density as more electrons from 2DEG go into the traps. Hence, the trap concentration can be calibrated with respect to measured 2DEG density or current levels in the measured device without any bias. It can be seen in the figures that although, all these parameters have some effect on  $V_t$ , all of them affect the electron density too which affects the  $I_d$ - $V_d$  characteristics. Thus, in order to calibrate both  $I_d$ - $V_d$  and  $I_d$ - $V_g$  characteristics of the device, an iterative procedure was performed in which the effect of calibration of  $V_t$  on  $I_d$ - $V_d$  characteristics (and vice-versa) was taken into account. Thus, finally after a number of iterations of calibration procedure for each

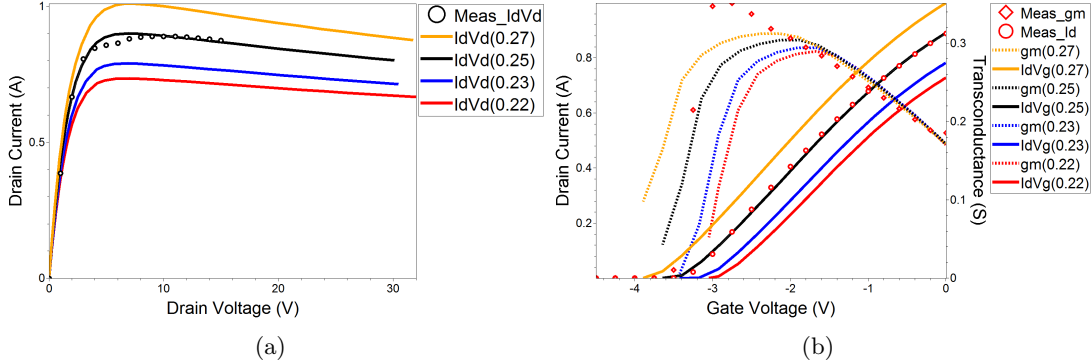


**Figure 4.8:** Effect of AlGaIn thickness variation on a)  $I_d$  vs  $V_d$ , b)  $I_d$  vs  $V_g$ .



**Figure 4.9:** Effect of Trap density variation on a)  $I_d$  vs  $V_d$ , b)  $I_d$  vs  $V_g$ .

parameter shown above, a set of values (Table 4.2) was obtained that gave the closest match to the measured results. The remaining parameters were kept as presented in table 4.1. Figure 4.11 and 4.12 show the comparison of measured data and simulated



**Figure 4.10:** Effect of AlGaIn molefraction variation on a)  $I_d$  vs  $V_d$ , b)  $I_d$  vs  $V_g$ .

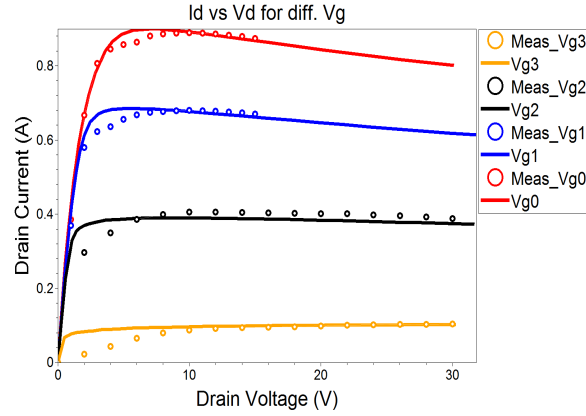
**Table 4.2:** Obtained parameter values after calibration

Parameter	Value
AlGaIn Thickness, $t_2$	16 nm
AlN Thickness, $t_3$	0.8 nm
Schottky barrier height	1.3 eV
Bulk Trap density (GaIn)	$1.25 \cdot 10^{17} \text{ atoms} \cdot \text{cm}^{-3}$
Trap Energy level (GaIn)	2.0 and 2.45 eV from CB
Bulk Trap density (AlGaIn)	$1.25 \cdot 10^{17} \text{ atoms} \cdot \text{cm}^{-3}$
Trap Energy level (AlGaIn)	2.7 and 3.10 eV from CB
Surface Trap conc	$5 \cdot 10^{13} \text{ atoms} \cdot \text{cm}^{-2}$
Energy level	1.78 eV from CB
Al mole fraction	0.25

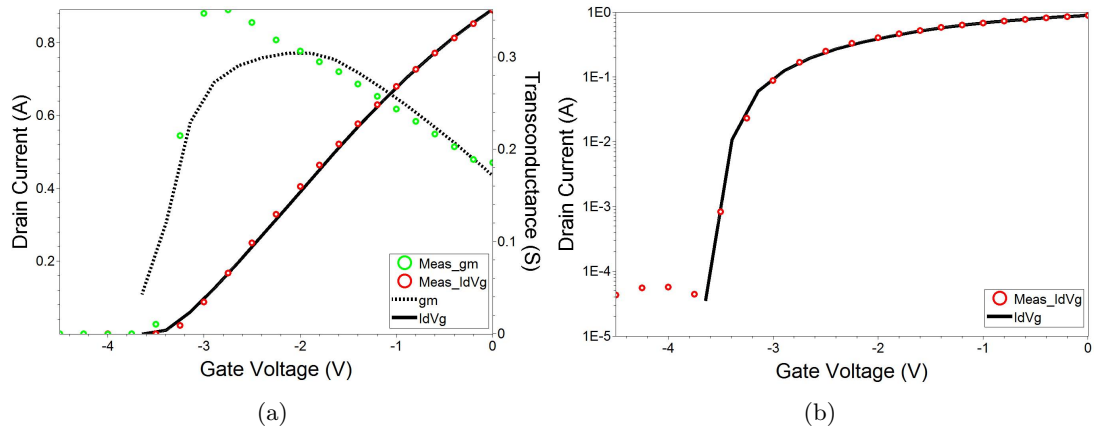
DC results after calibration.  $I_d$ - $V_g$  characteristics in figure 4.12 show a good match with a reasonable similarity in the transconductance curve too.

A point worth mentioning here is the differences in measured and simulated slope of  $I_d$ - $V_d$  characteristics in the linear region for gate voltage,  $V_g$ , lower than 0 V. Furthermore, it seems to increase as the gate voltage is reduced. Since such a slope represents the on-resistance of the device, it is obvious that the resistive behavior was not correctly simulated. A number of parameters were investigated to understand and solve the issue, which included contact resistance of the source/drain electrodes, doping in all the layers, trap concentration and energy levels, thickness of AlN intermediate layer, but the problem could not be solved. Although, the access resistance of the device could be the possible reason, varying the length of the un-gated region between drain and source electrodes could not solve the problem. Hence, this issue is still open and needs to be

investigated further.



**Figure 4.11:** A comparison of  $I_d/V_d$  characteristics for simulated and measured data at different gate voltages



**Figure 4.12:** A comparison of simulated a) Normal, b) Subthreshold  $I_d/V_g$  characteristics and measured data

#### 4.1.4 AC Simulations

Small signal analysis has been done using the model described in figure 4.13 and 4.14. The general equations for the small signal model given by equations 4.1- 4.4 have been used to compute the capacitors in the model.

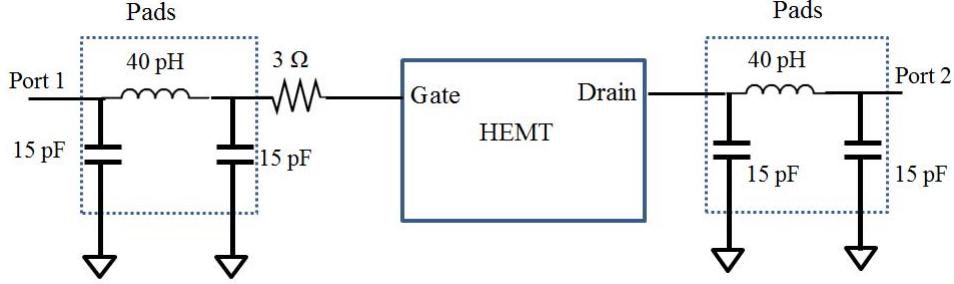
$$Y_{11} = j\omega(C_{gs} + C_{gd}) \quad (4.1)$$

$$Y_{12} = -j\omega C_{gd} \quad (4.2)$$

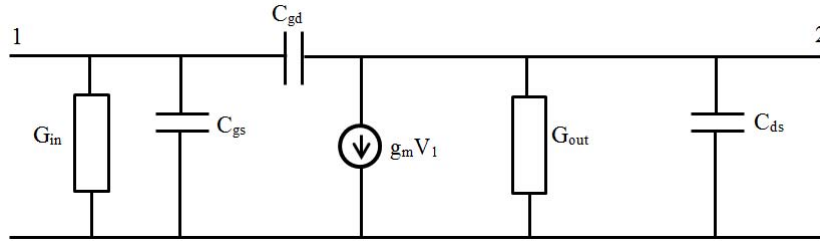
$$Y_{21} = G_{in} - j\omega C_{gd} \quad (4.3)$$

$$Y_{22} = G_{out} + j\omega(C_{ds} + C_{gd}) \quad (4.4)$$

Comparison of AC measurement and simulation is shown in figure 4.15 for various Y-



**Figure 4.13:** Equivalent circuit diagram of the small signal analysis model



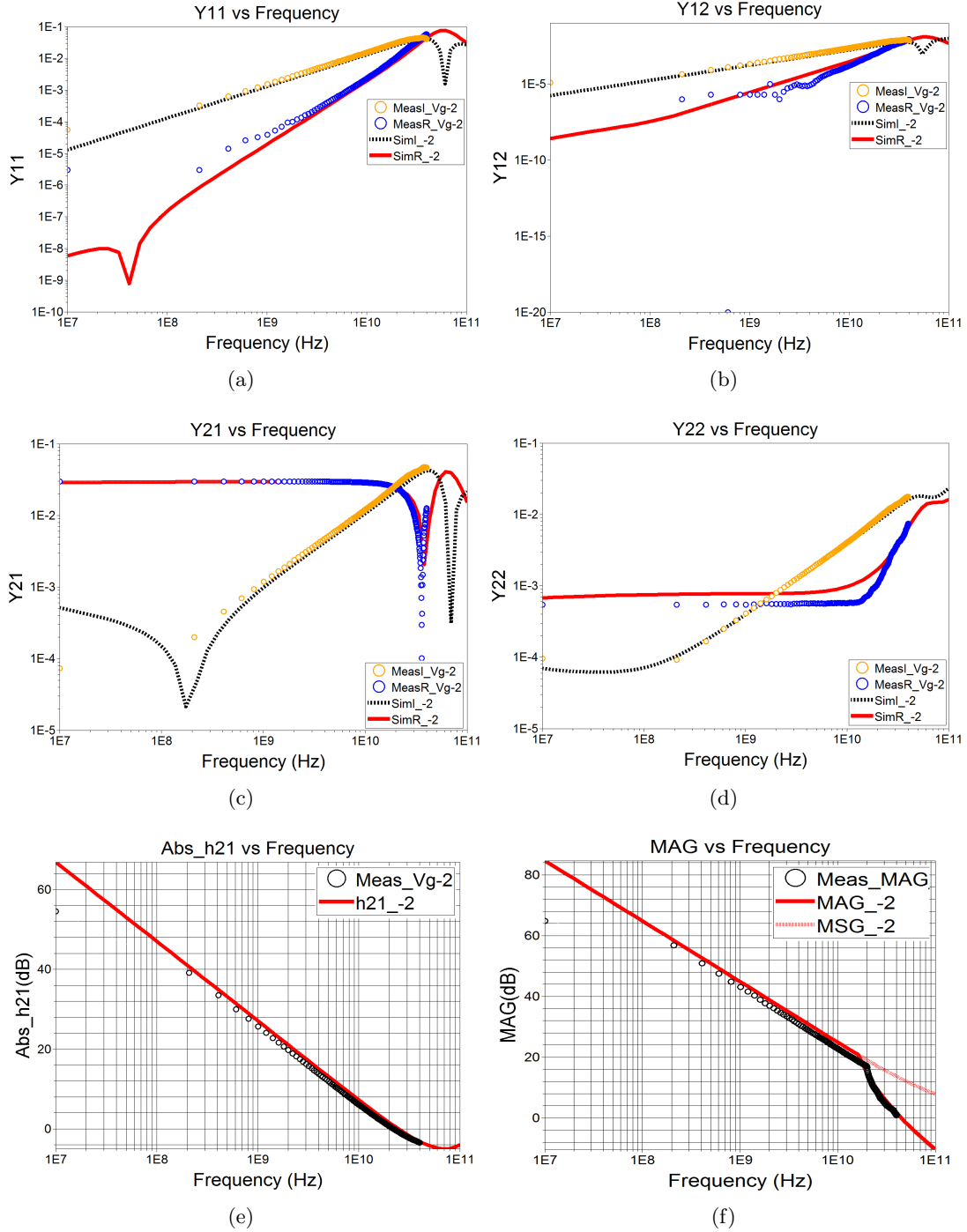
**Figure 4.14:** An equivalent small signal model of HEMT describing various capacitors

parameters. One possible reason for the variations can be due to the pad capacitor model (figure 4.13) and corresponding values assumed for small signal analysis in the simulator. There are a couple of capacitors which comes into play at higher frequencies due to coupling between the electrodes inherent in the transistor design. (Since no measurement data was available to ascertain their exact values, default values were used from previous measurements. This method, although not accurate, gave results sufficiently close to measured data. It was found sufficient to give a qualitative prediction on the operational characteristics of the device, which is further ascertained by the closeness of simulated  $f_t$  and  $f_{max}$  values to those measured.) The cut-off frequencies,  $f_t$  and  $f_{max}$  give a measure of the maximum frequency at which a device can give gain. While  $f_t$  represents the frequency at which the current gain is unity,  $f_{max}$  gives a measure of maximum frequency at which the device exhibits power gain.  $f_t$  has been calculated from  $|h_{21}| = 1$ .  $f_{max}$  has been calculated by finding the intersection of Maximum Available Gain (MAG) with the 0 dB gain line. MAG is given by the formula

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta s|^2}{2 |s_{12} \cdot s_{21}|} \quad (4.5)$$

$$\Delta s = s_{11} \cdot s_{22} - s_{12} \cdot s_{21} \quad (4.6)$$





**Figure 4.15:** A comparison of simulated AC parameters and measured data for  $V_g = -2V$ . a)  $y_{11}$ , b)  $y_{12}$ , c)  $y_{21}$ , d)  $y_{22}$ , e)  $|h_{21}|$ , f) Maximum Available Gain (MAG)

$$MSG = \left| \frac{s_{21}}{s_{12}} \right| \quad (4.7)$$

$$MAG = \left| \frac{s_{21}}{s_{12}} \right| \cdot (K - \sqrt{K^2 - 1}) \quad (4.8)$$

where  $K$  is the Rollett's stability factor.

## 4.2 Design Optimization

In order to optimize the HEMT design, we need to look at the parameters on which  $f_t$  and  $f_{max}$  depend which can be seen in figure 4.16 and the equations below [43] :

$$f_t \propto \frac{g_m}{C_{gs}} \quad (4.9)$$

$$f_{max} = \frac{f_t}{\sqrt{\frac{4}{R_{ds}}(R_i + R_s + R_g + \frac{\omega_t L_s}{2}) + 2\omega_t C_{gd}(R_i + R_s + R_g + \omega_t L_s)}} \quad (4.10)$$

It can be understood from equations above that by minimizing the gate resistance,  $R_g$ , gate to drain capacitance,  $C_{gd}$ , gate to source capacitance,  $C_{gs}$  or maximizing output resistance,  $R_{ds}$  and transconductance,  $g_m$ , should improve the HEMT operating frequencies. This can be achieved by changing the device configuration. Therefore, after the model was calibrated, a number of variations in the design were made in order to observe the effect of each of these changes on the output characteristics of the device, and subsequently to use these observations in optimizing the high frequency characteristics. These variations can be grouped into 2 different optimization experiments.

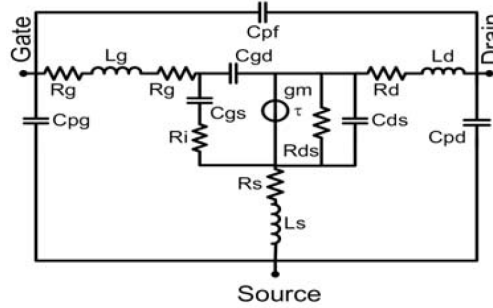


Figure 4.16: Small signal equivalent of a HEMT [43].

### 4.2.1 Type 1: Device Scaling

In the first set of optimization experiments, the epitaxial structure of the device was kept unchanged (Figure 4.1) while some of the lateral and vertical dimensions were scaled. Since it was observed during device calibration that changing some of the dimensions results in changed threshold voltage and transconductance properties, it is obvious that

AC characteristics would change as well. As the goal was to find the optimum operating frequency of the device, which inherently depends upon the maximum value of transconductance ( $g_m$ ), optimum bias point ( $V_g$  at  $\max(g_m)$ ) for each variation in a parameter should first be found out. Therefore, simulations were performed in two steps. First, DC simulations were performed to find the bias point ( $V_g$  at a particular  $V_d$ ) at which the value of  $g_m$  was maximum. It should be pointed out here that the drain voltage has been set to 10 V in all the simulations and  $V_g$  has been the variable. With this quiescent point as the AC analysis point, simulations were performed to find optimum  $f_t$  and  $f_{max}$ . This process was repeated for each change in a parameter and furthermore, for each parameter under scaling. Table 4.3 lists the parameters which were scaled and the corresponding range of variation.

**Table 4.3:** Description of various parameters of the structure under scaling and corresponding dimensions. All other parameters were kept fixed to values listed in table 4.2

Parameter	Description	Dimension (in $\mu\text{m}$ )/ Value
$x\text{AlGaN}$	Al mole fraction in AlGaN layer	0.18 - 0.5
$t_2$	Thickness of AlGaN Barrier layer	0.005 - 0.025
$t_3$	Thickness of AlN barrier layer	0 - 0.001
$L_g$	Gate electrode length	0.03 - 0.250
$L_{gs}$	Gate to source length	0.2 - 0.8
$L_{gd}$	Gate to drain length	0.2 - 2.0

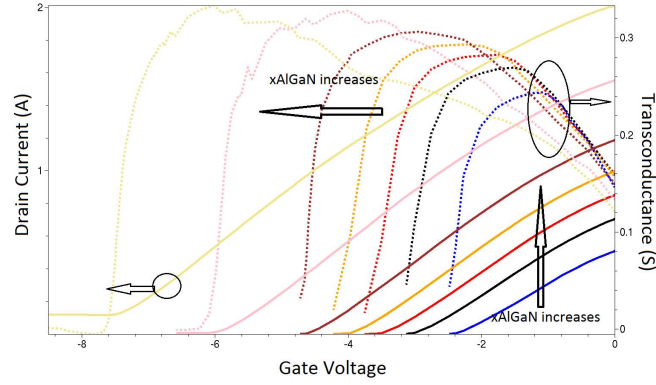
### Varying Al mole fraction in AlGaN, $x\text{AlGaN}$

Mole fraction of the AlGaN barrier layer was varied from 18% to 50%. Thickness of the layer was kept at 15 nm to take care of the critical length at higher mole fractions. Table 4.4 lists the mole fraction values and corresponding optimum bias point. Figure 4.17 shows the variation in  $I_d$  and  $g_m$  due to  $x\text{AlGaN}$  change. A mole fraction increase results in corresponding increase in the electron density in 2DEG. This increase leads to higher current which explains the increase in the current,  $I_d$  with mole fraction. Figure 4.17b and figure 4.17c show the variation of  $f_t$  and  $f_{max}$  with  $x\text{AlGaN}$ .

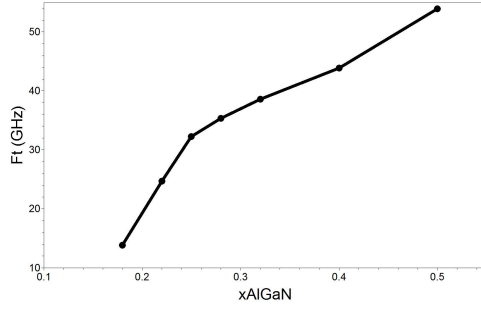
It can be seen that due to the increase in 2DEG density, transconductance,  $g_m$  increases and hence the frequency increases with Al mole fraction. This can also be explained by the fact that the increase in mole fraction leads to higher polarization induced electric field. As a result, the conduction band at the junction rises, leading to increased electron confinement. It has been envisaged that increase in electron confinement results in the reduction in scattering of electrons from 2DEG into the GaN buffer. This leads to a decrease in the short channel effects, and therefore a higher output resistance,  $R_{ds}$  [43]. As  $f_{max}$  is directly proportional to  $R_{ds}$  (see equation 4.10), it leads to higher  $f_{max}$ .

**Table 4.4:** Description of xAlGaN variation,  $V_{ds}=10$  V

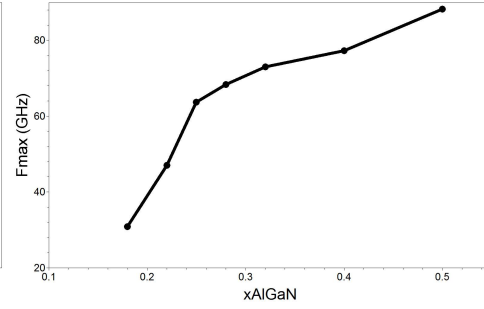
xAlGaN	Quiescent point, $V_g$
0.18	-1.35
0.22	-1.75
0.25	-2.5
0.28	-2.8
0.32	-3.2
0.40	-4.04
0.50	-6.04



(a)



(b)



(c)

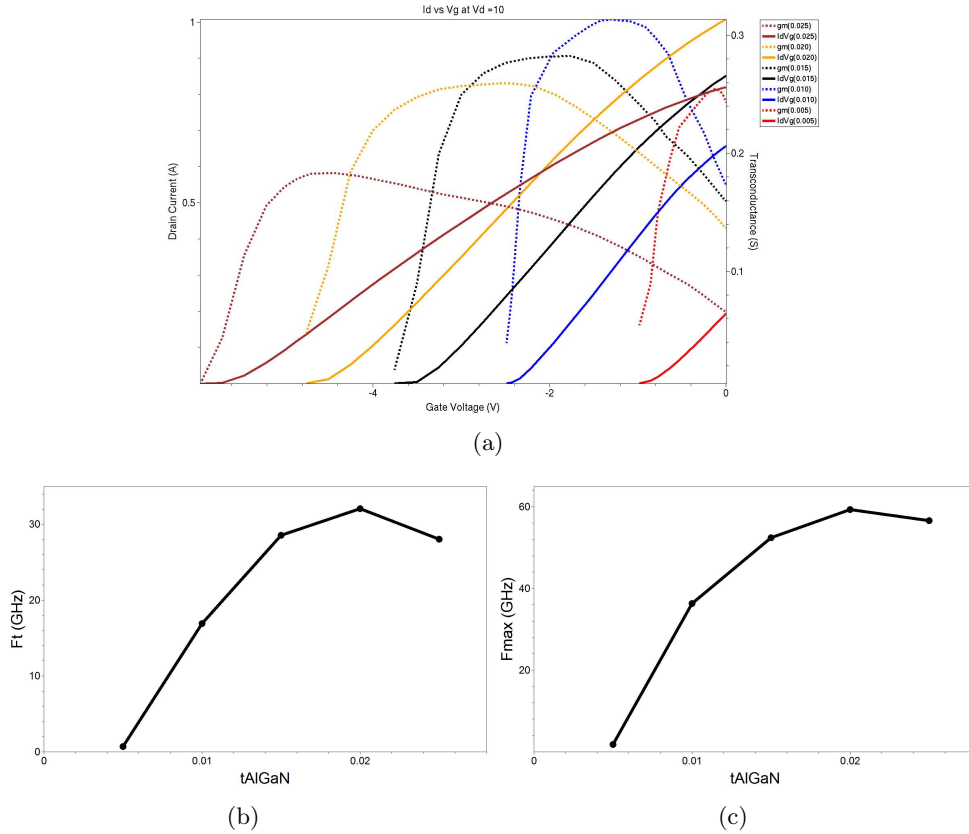
**Figure 4.17:** Effect of varying xAlGaN on DC and AC characteristics. a) Drain current and transconductance at different xAlGaN with respect to gate voltage, b)  $f_t$  and  $f_{max}$  variation with xAlGaN**Varying AlGaN barrier layer thickness, ( $t_{AlGaN}$ )**

In the next step, the thickness of the barrier layer ( $t_2$  or  $t_{AlGaN}$ ) was varied from 5 nm to 25 nm. Mole fraction was kept fixed at 25%. Parameter variation and corresponding

optimum bias point is listed in table 4.5. Corresponding variation in  $g_m$ ,  $f_t$  and  $f_{max}$  are shown in figure 4.18. The 2DEG density increases with increase in ( $t_{AlGaN}$ ) to some

**Table 4.5:** Details of AlGaN barrier layer thickness variation,  $V_{ds}=10$  V

AlGaN Thickness(in $\mu\text{m}$ )	Quiescent point, $V_g$
0.005	-0.147
0.010	-1.407
0.015	-2.401
0.020	-3.007
0.025	-4.722



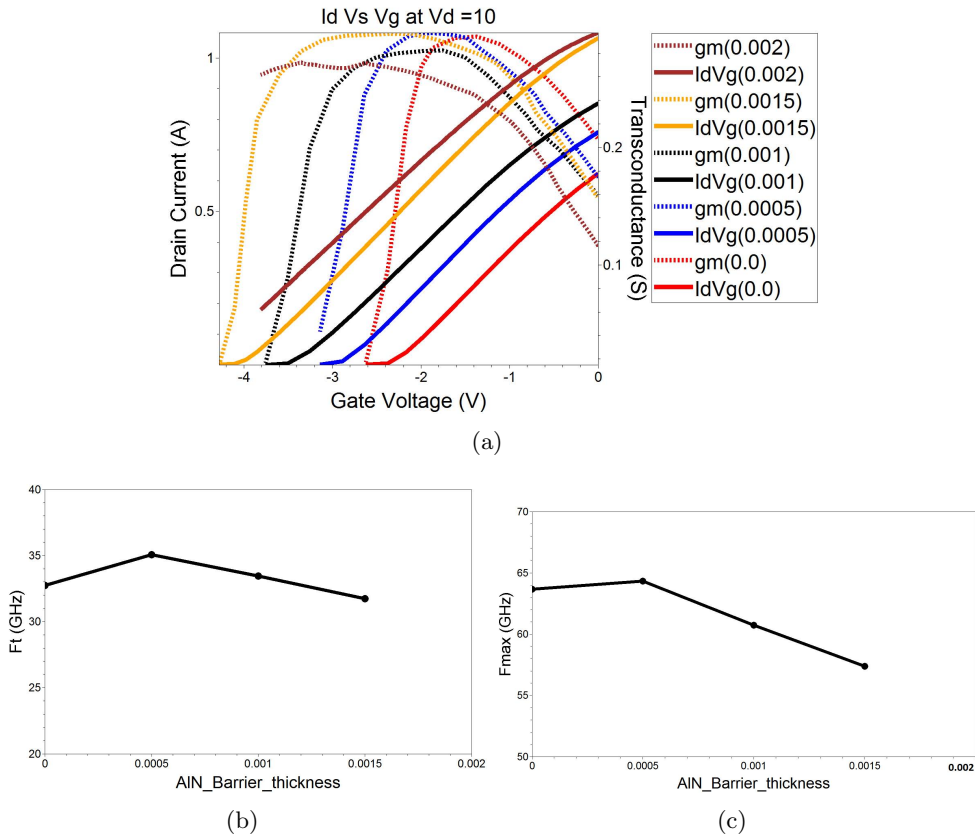
**Figure 4.18:** Effect of varying AlGaN thickness,  $t_{AlGaN}$ , on DC and AC characteristics. a) Drain current and transconductance at different AlGaN thickness,  $t_{AlGaN}$  with respect to gate voltage, b)  $F_t$  and c)  $F_{max}$  variation with AlGaN thickness,  $t_{AlGaN}$

thickness after which it saturates or decrease a little bit. This is due to the variation in the relative position of the energy level of the surface states and the AlGaN energy bands

with respect to the Fermi level of the device. As a consequence, the current,  $I_d$  increases with ( $t_{AlGaN}$ ) as shown in figure 4.18a. In addition, there is an increase in threshold voltage due to the increase in the distance between the gate and the channel. Although, above mentioned effects tend to reduce  $g_m$ , increasing the AlGaIn layer thickness results in a decrease in the capacitances,  $C_{gs}$  and  $C_{gd}$  which leads to improved  $f_t$  and  $f_{max}$ .

### Varying AlN barrier layer thickness, ( $t_{AlN}$ )

The thickness of the AlN layer ( $t_3$  or  $t_{AlN}$ ) was varied from 0 nm to 2 nm. Parameter variation and corresponding optimum bias point is listed in table 4.6. Corresponding variation in  $g_m$ ,  $f_t$  and  $f_{max}$  are shown in figures 4.19. As can be seen in figure 4.19a,



**Figure 4.19:** Effect of varying AlN thickness,  $t_{AlN}$ , on DC and AC characteristics. a) Drain current and transconductance at different AlN thickness,  $t_{AlN}$  with respect to Gate voltage, b)  $f_t$  and  $f_{max}$  variation with AlN thickness,  $t_{AlN}$

the current increases with  $t_{AlN}$ , which is due to the increase in 2DEG density due to increased band discontinuity,  $\Delta E_c$  and improved confinement of the electron wave function. There is an increase in threshold voltage due to increasing distance between gate and the channel too. Initial increase in  $f_t$ , although not significant, could be attributed

**Table 4.6:** Details of AlN barrier layer thickness variation,  $V_{ds}=10$  V

AlN Thickness(in $\mu\text{m}$ )	Quiescent point, $V_g$
0.0	-1.5
0.0005	-1.65
0.001	-1.9
0.0015	-2.5
0.002	-3.5

to an increase in the 2DEG density even though no significant improvement in  $g_m$  could be seen in figure 4.19. As increasing the AlN layer thickness further increases the distance between gate and channel, AC characteristics should reduce. This tradeoff behaviour is confirmed by the simulation results too. It was noted in some discussions that keeping the total thickness of AlGaIn and AlN layer constant should give better results on the effect of the AlN layer thickness. This could be pursued as future work in this regard.

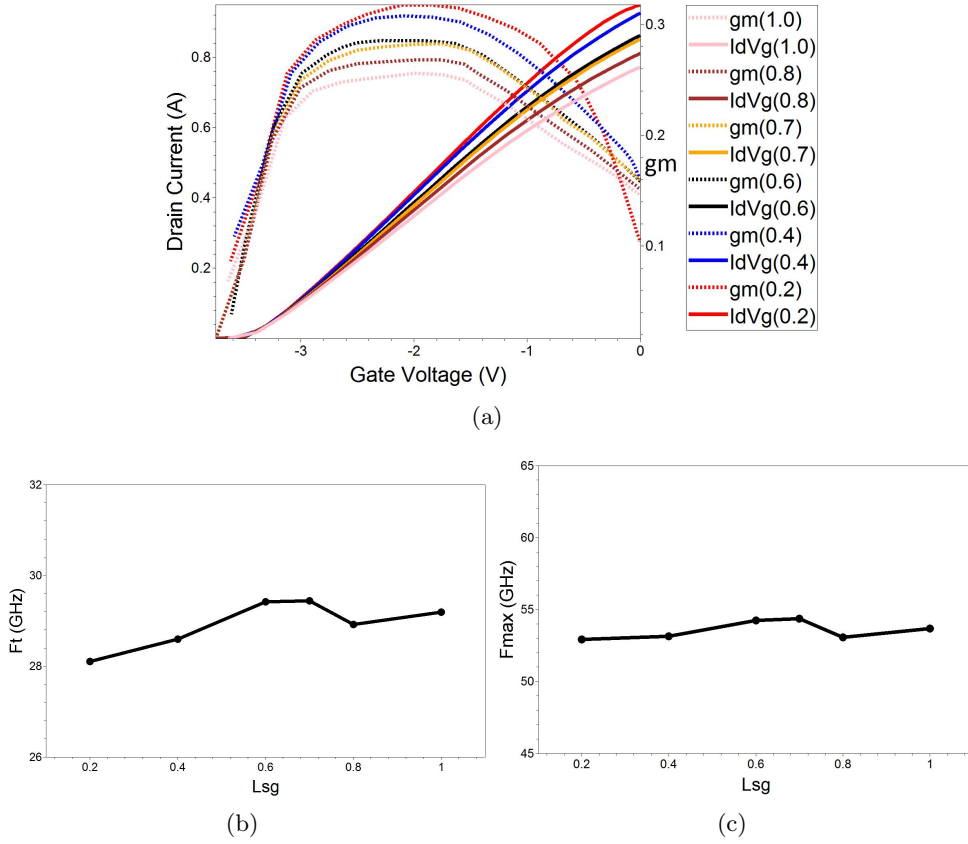
#### Varying Source to Gate distance, $L_{gs}$

Gate to source distance was varied from 0.2  $\mu\text{m}$  to 1.0  $\mu\text{m}$ . Parameter variation and corresponding optimum bias point is listed in table 4.7. Corresponding variation in  $g_m$ ,  $f_t$  and  $f_{max}$  are shown in figures 4.20. Increasing the source to gate distance increases

**Table 4.7:** Details of Source to Gate distance variation ,  $V_{ds}=10$  V

$L_{gs}$ (in $\mu\text{m}$ )	Quiescent point, $V_g$
0.2	-2.0
0.4	-2.0
0.6	-2.0
0.7	-2.0
0.8	-2.0
1.0	-2.0

the source access resistance which increases the potential drop across the ungated source to gate region. This leads to the reduction in the potential under the gate region. Thus, transconductance curve shifts downwards. However, the observation that there is no appreciable change in  $f_t$  and  $f_{max}$  could not be explained. But a probable reason could be the fact that access resistance could well be dominated by drain to gate region which is comparatively larger in length (2  $\mu\text{m}$ ) as compared to  $L_{gs}$ . Moreover, even with substantial increase in  $g_m$  with decrease in  $L_{gs}$  seems to have no effect on  $f_t$ . This could be due to the fact that with decrease in source to gate distance, the capacitance,  $C_{gs}$



**Figure 4.20:** Effect of varying gate to source distance,  $L_{gs}$ , on DC and AC characteristics. a) Drain current and transconductance at different gate to source distance,  $L_{gs}$  with respect to Gate voltage, b)  $f_t$  and  $f_{max}$  variation with gate to source distance,  $L_{gs}$

increases too which is inversely proportional to  $f_t$  (see equation 4.9). This could negate the increase in  $g_m$ . Hence, as shown in figure 4.20b, there is no appreciable improvement in  $f_t$  with  $L_{gs}$

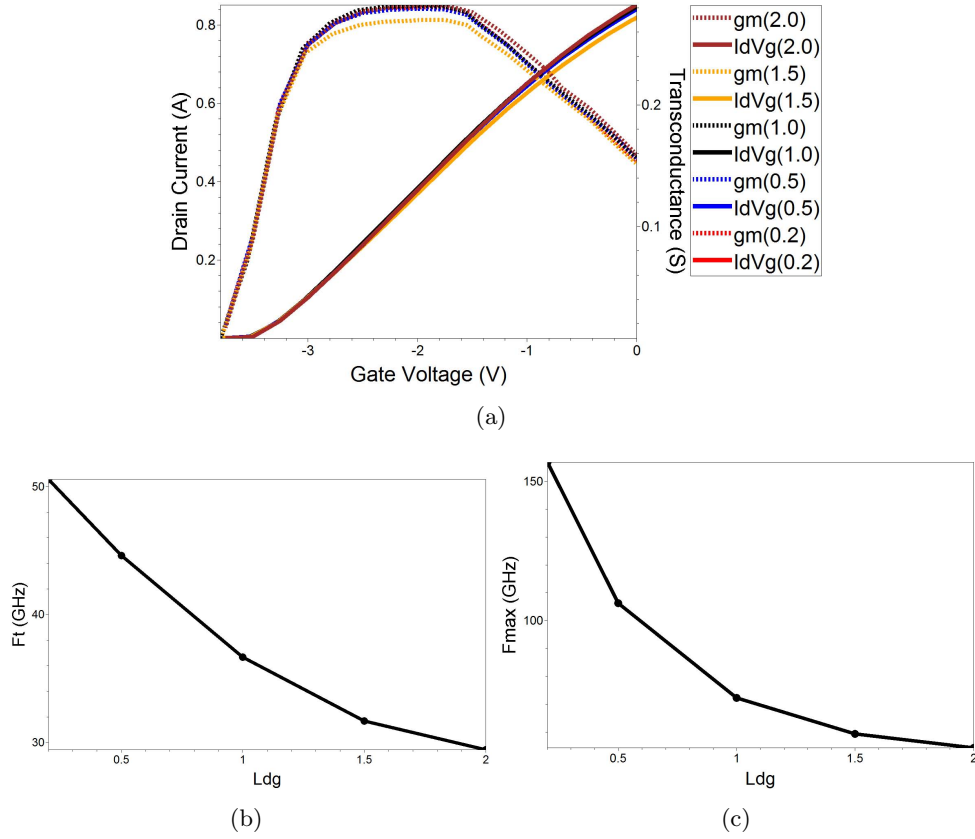
#### Varying Drain to Gate distance, $L_{gd}$

Gate to drain distance was varied from 0.2  $\mu\text{m}$  to 2.0  $\mu\text{m}$ . Parameter variation is listed in table 4.8. Since  $L_{gd} = 0.2 \mu\text{m}$  is less than  $L_{fpD}$ ,  $L_{fpD}$  value was changed accordingly to maintain the balance. Corresponding variation in  $g_m$ ,  $f_t$  and  $f_{max}$  are shown in figure 4.21. Increasing the drain to gate distance increases the drain access resistance which deteriorates the AC frequency characteristics. Thus, as the  $L_{gd}$  value increases,  $f_t$  decreases. A point to be noted here is that neither  $L_{gs}$  nor  $L_{gd}$  have any appreciable effect on threshold voltage or the 2DEG density although the surface defects increase. Probably, it is due to the reason that although surface defects increases, the density of electrons remains the same as the area increases with  $L_{gd}$  too.



**Table 4.8:** Details of Drain to Gate distance variation,  $V_{ds}=10$  V

$L_{gd}$ (in $\mu\text{m}$ )	Quiescent point, $V_g$
0.2	-2.0
0.5	-2.0
1.0	-2.0
1.5	-2.0
2.0	-2.0



**Figure 4.21:** Effect of varying gate to drain distance,  $L_{gd}$ , on DC and AC characteristics. a) Drain current and transconductance at different gate to drain distance,  $L_{gd}$  with respect to Gate voltage, b)  $f_t$  and  $f_{max}$  variation with gate to drain distance,  $L_{gd}$

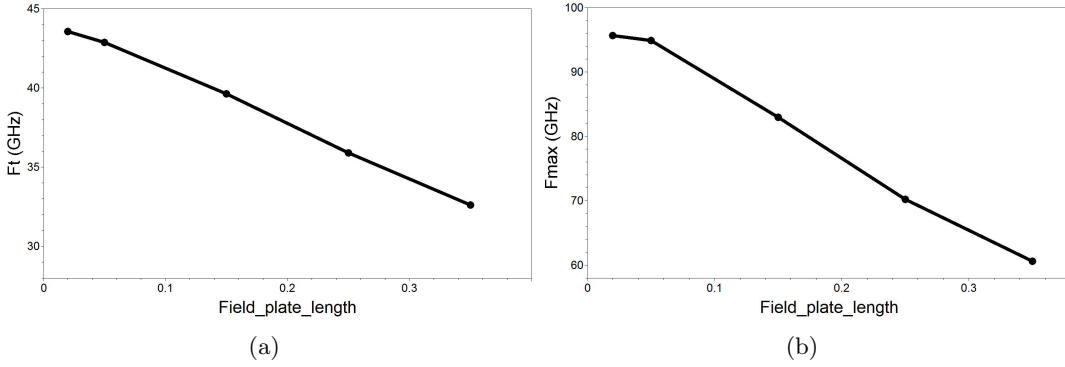
### Varying Field plate length, $L_{fp}$

The total field plate length ( $L_{fpS} + L_{fpD}$ ) was varied from 40 nm to 450 nm. Parameter variation and corresponding optimum bias point is listed in table 4.9. Corresponding variation in  $f_t$  and  $f_{max}$  are shown in figure 4.22. All other parameters were kept same

as initial design. While varying the field plate length, gate resistance was varied

**Table 4.9:** Details of Field plate length variation

Field Plate Length ( $L_{fpS}, L_{fpD}$ )(in $\mu\text{m}$ )	Gate resistance( $\Omega$ )	Quiescent point, $V_g$
0.02, 0.02	4.2912	-2.0
0.04, 0.05	3.6601	-2.0
0.06, 0.15	2.7053	-2.0
0.08, 0.25	2.1456	-2.0
0.1, 0.350	1.7778	-2.0



**Figure 4.22:** Effect of varying field plate length,  $L_g$ , on AC characteristics. a)  $f_t$  and  $f_{max}$  variation with field plate length,  $L_{fp}$

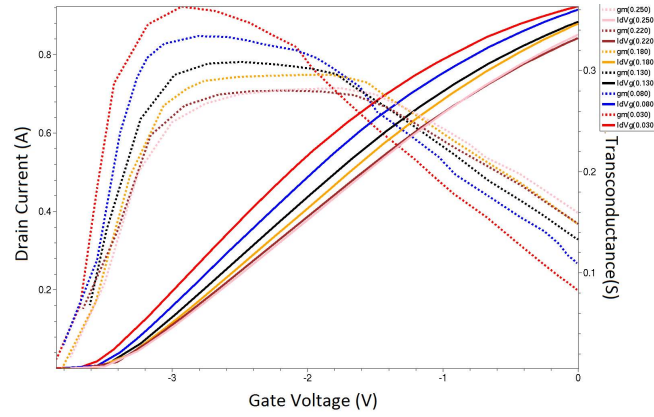
accordingly as both are related. The gate length was kept at 250 nm. Field plates are used to improve the breakdown voltage of the transistor since distributing the electric field at the gate edges increases the breakdown voltage. It has also been observed that field plates reduces the current dispersion effect due to transients on the gate electrode. It also helps in lowering the gate resistance. But increasing the field plates towards the drain and source electrodes increases the parasitic capacitances,  $C_{gd}$  and  $C_{gs}$ . This increase in parasitic capacitances results in the reduction in  $f_t$  and  $f_{max}$  from the corresponding equations. If the breakdown voltage is not a constraint in the design, the field plate length can be reduced to improve the frequency characteristics of the HEMT. This is also confirmed by simulation results where in figure 4.22, reducing the field plate length leads to increase in  $f_t$  and  $f_{max}$ .

### Varying Gate Length, $L_g$

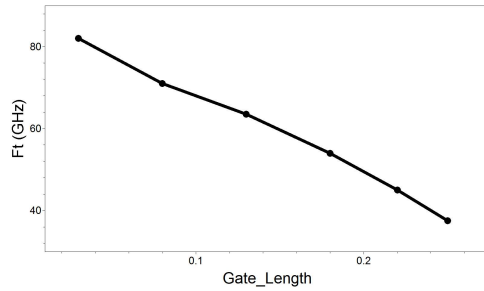
The gate Length was varied from 30 nm to 250 nm. Parameter variation and corresponding optimum bias point is listed in table 4.10. Corresponding variation in  $g_m$ ,  $f_t$  and  $f_{max}$  are shown in figures 4.23. While varying the gate length, expression Min

**Table 4.10:** Details of Gate Length variation,  $V_{ds}=10$  V

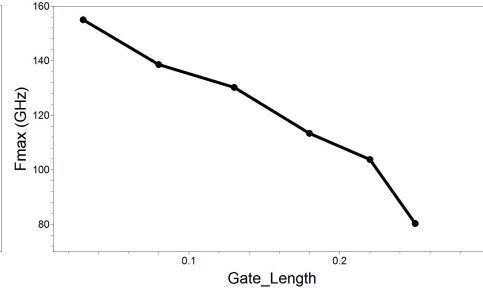
Gate Length(in $\mu\text{m}$ )	Field Plate Length ( $L_{fpS}, L_{fpD}$ ) (in $\mu\text{m}$ )	Quiescent point, $V_g$
0.030	0.9, 0.9	-3.0
0.080	0.1, 0.350	-2.85
0.130	0.1, 0.350	-2.6
0.180	0.1, 0.350	-2.2
0.220	0.1, 0.350	-2.4
0.250	0.1, 0.350	-1.8



(a)



(b)



(c)

**Figure 4.23:** Effect of varying gate length,  $L_g$ , on DC and AC characteristics. a) Drain current and transconductance at different gate length,  $L_g$  with respect to Gate voltage, b)  $f_t$  and  $f_{max}$  variation with gate length,  $L_g$

$(3 * L_g, 0.1\mu\text{m})$  was used to balance the field plate length with gate length variations. Also, gate resistance was varied accordingly. As can be seen in figure 4.23a, decreasing the gate length shifts the threshold voltage to more negative voltages but more importantly, it increases the transconductance,  $g_m$ . This leads to an increase in  $f_t$  as shown in

figure 4.23b. In addition, the decrease in the gate length leads to significant reduction in the gate capacitance. Since  $f_t$  and  $f_{max}$  are inversely proportional to such capacitance, it leads to an appreciable improvement in the AC characteristics.

A point worth noting here is that although decreasing the gate length improves the operating frequencies, it also leads to higher threshold voltage and short channel effects. These short channel effects results in effects like current leakage which can be seen as the reduction in the current or output resistance. Thus, after a certain gate length, AC characteristics of the device should deteriorate due to the appearance of the short channel effects. This, surprisingly, was not found in simulations even till  $L_g=30$  nm. This absence could not be explained and should, therefore, be investigated in the future.

#### 4.2.2 Type 2: AlGaN Buffer Layer

Figure 4.24 shows the structure of Type 2 (T2) device. Adding another AlGaN layer on the other side of the GaN channel layer should confine the electrons in a more efficient manner as the new AlGaN layer adds another barrier for the 2DEG electrons. Thinner

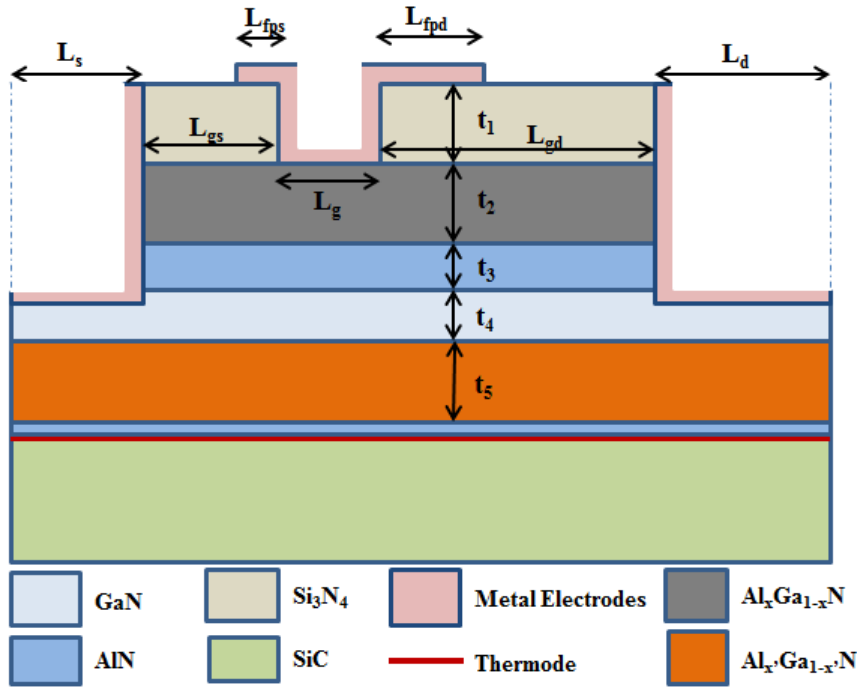


Figure 4.24: Geometric structure of simulated Type 2 HEMT.

the GaN layer and higher the mole-fraction of AlGaN layer, more the confinement. Thus, the idea of this simulation was to observe if the additional confinement would improve the AC performance of the device. Table 4.11 describes various parameters of the structure. The thickness of the GaN buffer layer and the Al mole-fraction of the AlGaN buffer layer

were varied in this set of simulation to observe the corresponding effect on  $F_t$  and  $F_{max}$ . The drain voltage has been set at 10 V. All the other dimensions were kept the same as for the type 1 device.

**Table 4.11:** Description of various parameters of the Type 2 structure and dimensions

Parameter	Decription	Dimension (in $\mu\text{m}$ )
$t_1$	Thickness of Passivation layer (SiN)	0.1
$t_4$	Thickness of GaN layer	0.02 - 0.2
$t_5$	Thickness of AlGaIn buffer layer	1.8 - $t_4$

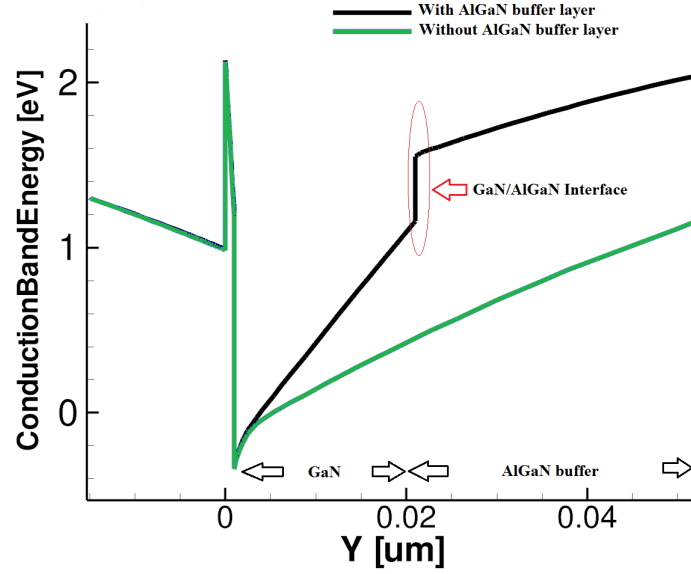
### Varying the Al mole fraction of the AlGaIn buffer layer, $x'$ AlGaIn

The Al mole fraction,  $x'$ , of the AlGaIn buffer layer was varied from 0 - 15%. The thickness of the GaN buffer layer was kept at 100 nm and the AlGaIn buffer layer thickness was correspondingly calculated. Details of  $x'$ AlGaIn variation and corresponding optimum bias points are listed in table 4.12. As the Al molefraction in the AlGaIn buffer layer increases, the confinement increases. This is due to the fact that increasing the molefraction leads to the increase in the band gap and hence, the polarization field at the GaN/AlGaIn interface. It results in the upward shift in the conduction band edge of GaN at the interface leading to improvement in 2DEG confinement as shown in figure 4.25. Although this should lead to better  $f_{max}$ , it was found that the above mole fraction variation also results in the reduction of  $g_m$  and current density in the 2DEG. It can be assumed from the simulation results shown in figure 4.26, that the effect of  $g_m$  reduction is more pronounced as compared to expected confinement effects, although a precise reason is yet to be analyzed. Although the layer thickness in this simulation

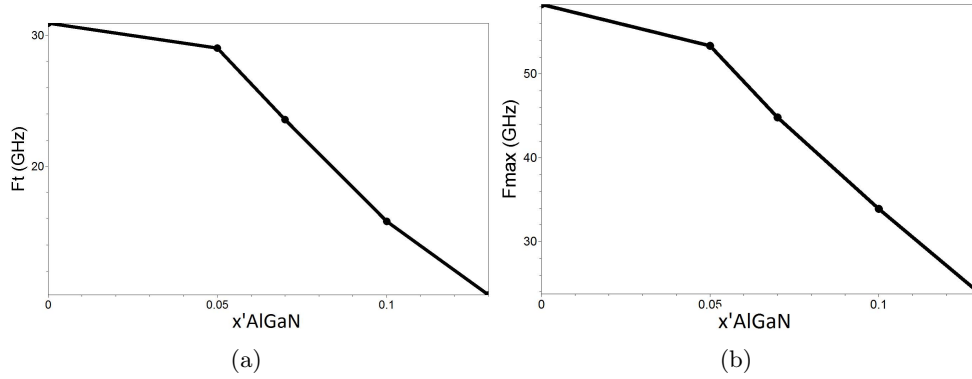
**Table 4.12:** Details of  $x'$ AlGaIn variation

$x'$ AlGaIn (in %)	Quiescent point, $V_g$
0	-1.6
5	-1.6
7	-1.6
10	-1.6
13	-1.6

was 100 nm, the same effect was observed for 20 nm thickness. Since, not just the magnitude of the 2DEG density, but its position with respect to the interface also plays an important role in AC simulations, the use of the classical approach could be the reason as it approximates the 2DEG position right at the interface while it actually lies some



**Figure 4.25:** A comparison depicting the effect of inclusion of AlGaN buffer layer on conduction band edge of the structure in a vertical crosssection



**Figure 4.26:** Effect of varying Al mole fraction of AlGaN buffer layer on AC characteristics. a)  $F_t$  and c)  $F_{max}$  variation with Al mole fraction of AlGaN buffer layer

nanometers away from the interface. It should be checked, as future work, by using the density gradient method.

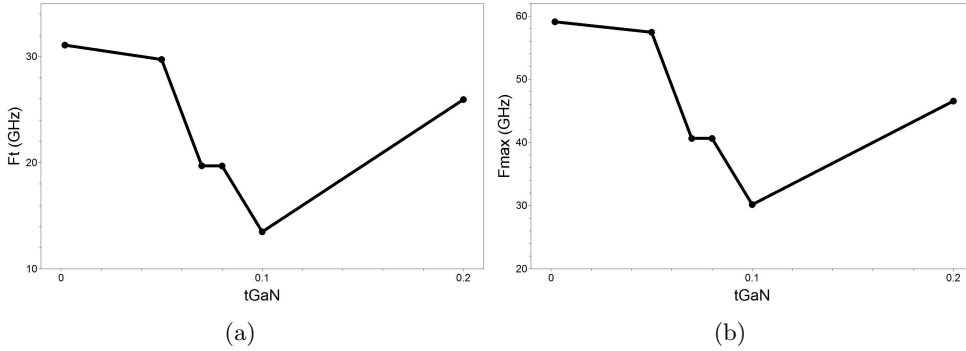
#### Varying the thickness of GaN channel layer, $t_{GaN}$

In this simulation, the thickness of the GaN channel layer was varied from 20 - 200 nm. The thickness of the AlGaN buffer layer was calculated by subtracting this value from 1.8  $\mu\text{m}$ . The Al mole fraction of the AlGaN buffer layer was kept at 10%. Details of  $t_{GaN}$  variation and corresponding optimum bias point is listed in table 4.13. Corre-

sponding variation in AC characteristics are shown in figure 4.27. The introduction of

**Table 4.13:** Details of  $t_{GaN}$  variation

$t_{GaN}$ (in $\mu\text{m}$ )	Quiescent point, $V_g$
0.02	-1.46
0.05	-1.4
0.07	-1.54
0.08	-1.55
0.1	-1.55
0.2	-1.8



**Figure 4.27:** Effect of varying GaN thickness,  $t_{GaN}$  on AC characteristics. a)  $F_t$  and c)  $F_{max}$  variation with GaN thickness,  $t_{GaN}$ . Notice that after some GaN thickness,  $f_{max}$  starts to increase

the additional AlGaIn buffer layer below the GaN channel layer leads to the formation of a double heterojunction. This results in increased electron confinement in the channel. As the thickness of the GaN layer is reduced, the electron confinement increases further. It has been reported that the increase in electron confinement results in higher output resistance,  $R_{ds}$  [43]. Therefore, from equation 4.10,  $f_t$  and  $f_{max}$  should show an improvement. This is confirmed by the simulation results shown in figure 4.27. Clearly, as the thickness of the GaN layer reduces,  $f_t$  increases too. But if we look from the opposite perspective, increasing the GaN thickness should decrease the output resistance  $R_{ds}$  from confinement point of view, and hence,  $f_{max}$  too. On the other hand, it also results in the increase in the electron density in the channel as the 2DEG area becomes wider. The increase in 2DEG density leads to the increase in the current and  $g_m$ . This results in the increase in  $f_t$ . Due to this trade-off, after some GaN thickness,  $f_{max}$  was found to increase instead of decreasing. This can be seen in figure 4.27. After a GaN thickness of 100-120 nm,  $f_{max}$  starts to increase.

# 5

## Conclusions

**W**ITH better electronic and elastic properties, GaN based HEMTs are a strong contender for high frequency and output power applications. A higher 2DEG density, achieved without any intentional doping, allows such devices to have higher output current capability. Recent research has shown that GaN has the capability to meet increasing demands for higher operating frequency and power. But due to technological challenges faced by researchers currently, innovative solutions, both in design and material configurations, are required to make it possible. It has been observed that changing the dimensions of the device, in lateral or longitudinal direction, has a significant impact on the output characteristics of the device. Thus, in order to improve the device characteristics to cater to the increasing demands of higher operating frequencies, a simulation deck was designed, calibrated and used to find out the optimum design parameters to achieve the above objective.

### 5.1 Simulation Deck

The simulation deck was designed using Sentaurus TCAD software. Simulation results clearly showed characteristics of a HEMT device with the formation of a 2DEG at the heterointerface and subsequent current flow along this channel. The density of 2DEG was found to be closely related to the density of traps at the surface and in the bulk. It was observed that increasing the trap density in the bulk results in the decrease in output current levels as the 2DEG density reduces. This is due to the fact that more electrons from 2DEG gets trapped in such traps reducing the 2DEG density. It was also seen that the energy level of such traps play an important role too. Deeper the level, more difficult it becomes for the trapped electron to detrap which, in turn, increases the relaxation time in current lag effects observed in HEMTs. Due to the confusion related to trap energy levels in literature (and unavailability of any measurement data), reasonable values were assumed based on literature.



The effect of the device temperature on the output current was simulated by defining thermal electrodes at the base of the HEMT structure. It was found that as the drain voltage,  $V_d$ , increases, lattice temperature starts to increase due to the increasing electric field. This results in reduction of mobility and further, deteriorates the output current. As shown in the simulation results in previous chapter, this gives rise to a negative slope in the output current characteristics of the device. This slope was found to depend on the thermal resistance of the substrate material in a sense that as the thermal conductivity of the substrate material decreases, the above mentioned slope increases. This observation justifies the preference given to high thermal conductivity materials in GaN HEMT manufacturing.

Simulation deck was calibrated against the measured data of real devices with the same dimensions. Physical parameters like trap density, Schottky barrier height ( $\phi_b$ ) were varied iteratively during the process of calibration. Close matching of simulated output characteristics with measured data was obtained after calibration. But still some discrepancy was observed in the linear region for gate voltages lower than 0 V. Comparison of AC simulations also showed a close match with measured data. It was observed that parasitics due to contacts with the device play an important role in AC characteristics of the device as the close matching of results was only obtained after inclusion of pad capacitances and inductances.

## 5.2 Design Optimization

It was found that AC characteristics of the device, especially  $f_t$  and  $f_{max}$ , depend on a number of factors which, in turn, are related to the design of the device. Some of these factors, like transconductance ( $g_m$ ), inherent capacitances ( $C_{gs}$ ,  $C_{gd}$ ) and resistance ( $R_{ds}$ ,  $R_g$ ) are strongly dependent on the layer structure and thicknesses, and gate to drain/source distance. Therefore, in order to look for the optimum design suitable for high frequency applications, effects of various geometrical design parameters were analyzed in a set of experimental simulations.

### 5.2.1 Scaling

In this set of simulations, the vertical and lateral dimensions were varied while keeping the epitaxial layer structure as same. It was observed from the simulation results that increasing the Aluminium mole fraction in the AlGaIn barrier layer leads to an increase in 2DEG density and electron confinement. As a result,  $f_t$  and  $f_{max}$  increase with Al mole fraction. An increase in AlGaIn layer thickness results in a decrease in the internal capacitances,  $C_{gs}$ ,  $C_{gd}$ . Therefore, as expected,  $f_t$  and  $f_{max}$  were found to improve with AlGaIn thickness. The length of the gate electrode is an important part of the gate resistance and capacitance. Reducing the gate length, hence, should reduce their values too. As confirmed by simulation results, reducing the gate length results in the improvement in  $f_t$  and  $f_{max}$  to such an extent that reducing it from 250 nm to 30 nm doubles the value of  $f_t$  and  $f_{max}$ . The distance between gate and drain electrode defines

$C_{gd}$  which, in turn, is inversely proportional to  $f_{max}$ . It was found that reducing this distance results in an increase in  $f_t$  and  $f_{max}$ . Furthermore, reducing the field plate length improves the frequency characteristics as it reduces the parasitic capacitances,  $C_{gd}$  and  $C_{gs}$ .

It can be concluded from above discussion that in order to obtain the optimum design parameters, gate length ( $L_g$ ), and gate to drain distance ( $L_{gd}$ ) should be reduced while Al mole fraction and thickness of AlGa<sub>N</sub> barrier layer should be increased. Changes in gate to source electrode length ( $L_{gs}$ ) and AlN barrier layer thickness ( $t_{AlN}$ ) should also have significant effect on the AC characteristics, but after simulation it was noticed that such variations do not cause any appreciable change in  $f_t$  and  $f_{max}$ . Nevertheless, it was observed that the thickness of the AlN barrier layer should be kept around 5-8 Å for optimum performance. In addition, the length of field plates should be optimized to maintain high enough breakdown voltage with improved frequency performance.

### 5.2.2 Epitaxial Variations

A double barrier heterostructure, with GaN channel layer sandwiched between layers of higher band gap materials (AlGa<sub>N</sub>/AlN/GaN/AlGa<sub>N</sub>), increases the confinement of the electrons in the 2DEG. This is due to the fact that electrons experience a potential barrier on both sides of the 2DEG. The increase in confinement leads to an increase in output resistance of the device as leakage current is reduced. As  $f_{max}$  is inversely proportional to this output conductance, AC characteristics are expected to improve. This was confirmed by simulation results which showed an increase in  $f_{max}$  as the thickness of the sandwiched GaN layer was reduced from 100 nm to 20 nm.

However, it must be mentioned here that the electron density was found to decrease with above mentioned GaN thickness variation. Electron density is closely related to channel resistance and capacitance. Thus, increasing the GaN channel layer thickness has a trade off. On one hand, it increases the electron density, leading to reduction in channel resistance and capacitance which should improve the AC characteristics. But on the other hand, it reduces the electron confinement in 2DEG which results in reduction in  $f_{max}$ . This tradeoff was clearly observed in simulation results when upto a GaN channel layer thickness of 100 nm, a decrease in  $f_{max}$  was noticed (reduction in 2DEG confinement) but after that an increasing behaviour was found.

Another way in which the confinement of the 2DEG can be improved is by increasing the Aluminium mole fraction in the AlGa<sub>N</sub> buffer layer. The increase in Al mole fraction results in higher bandgap, and therefore a higher potential barrier.

## 5.3 Future Outlook

Although the simulation deck designed in this thesis work has been able to model a HEMT device successfully, some of the issues faced during the work remain un-explained and need to be addressed as future work in order to further strengthen the reliability of such simulation model.

As mentioned previously, differences were found in the slope in the linear region of the I/V characteristics of the model as compared to measured data. Furthermore, this difference increased as the gate voltage,  $V_g$ , was made more negative. Since such a slope represents the on-resistance of the device, it is obvious that the resistive behavior was not correctly simulated. A number of parameters were investigated to understand and solve the issue. Although, the access resistance of the device could be the possible reason, varying the length of the ungated region between drain and source electrodes could not solve the problem. Thus, this issue is still open and needs to be investigated further.

A number of assumptions have been made with respect to values of some parameters like Schottky barrier height ( $\phi_b$ ), bulk and surface trap energy levels, pad capacitors and inductors based on literature and previous measurement experiences. In order to improve the reliability of the model, a real HEMT device need to be fabricated and measured to get above data.

While going through reported simulation results, it was noticed that the preferred mobility model for simulations is *Hydrodynamic mode* (HD). Many reasons have been listed by authors regarding the shortcomings of *Drift-Diffusion Model* (DD) for deep submicron gate lengths, a modified version of which was used in this work. Most noticeable among them is it's inefficiency in taking account of velocity overshoot effects and impact ionization caused due to hot electrons during simulations. Although, simulations done using DD model have been found to closely match the measured data, the difference which the use of HD model would make, remains to be seen.

Some of the unsolved issues in this work could possibly be due to the use of the classical approach towards the 2DEG distribution. It could be argued that not just the magnitude of the 2DEG density, but its relative position with respect to interface also plays an important role in defining AC characteristics of the the device. Since, the classical approach approximates the location of the 2DEG to be at the interface and not some nanometers away from it as has been found by experiments (due to quantum mechanical effects), the observed discrepancies in some of the optimization results could have their roots in it. Hence, it remains to be verified, by using density gradient approach, if the above reasoning is true.

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