Photoemission yield and the electron escape depth determination in metal–oxide–semiconductor structures on N^+-type and P^+-type silicon substrates

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This article gives a quantitative analysis of electron photoemission yield from N^+-type and P^+-type substrates of MOS structures. Based on this analysis, a method is presented to estimate both the scattering length, ℓ, of electrons in the image force potential well and of photoelectron escape depth, x_{esc}, from the semiconductor substrate. This method was used to estimate the scattering length and the escape depth from the substrates of Al-SiO_2-Si (N^+-type and P^+-type) structures. It was found that for N^+-type substrate structures the scattering in the image force potential well has a dominating influence on the photoemission yield while for P^+-type substrate structures both the scattering in the image force potential well and the photoemission from the subsurface regions of the photoemitter play important roles. It was found that the scattering length in the image force potential well was equal to $\ell = 6.7$–6.9 nm for structures on both N^+ and P^+ substrates, produced in the same processing conditions. For structures on P^+ substrates, the escape depth was found to be equal to $x_{esc} = 8$–9 nm. The scattering length, ℓ, determined in this study is considerably larger than the one reported previously ($\ell = 3.4$ nm) for similar MOS structures. The escape depth x_{esc} determined in this study is also considerably larger than the escape depth determined previously ($x_{esc} = 1.2$–2.5 nm) for the external photoemission from uncovered silicon surfaces into vacuum. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4722275]

I. INTRODUCTION

Application of new materials in modern MOS devices (high-k dielectrics, new gate materials, unconventional semiconductor substrates, such as GaN or SiC, etc.) necessitates determination of their basic parameters, related to energy band diagram of such systems. Band offsets, band gaps, effective contact potential difference, flat-band voltage, and other parameters have to be determined. This has generated a renewed interest in photoelectric measurements and the photoelectric phenomena observed in MOS structures (see, e.g., Refs. 8 and 9). This paper deals with a property which was observed and quantitatively characterized in the early studies on photoemission from semiconductors into vacuum[1–6] appearing as a different electron photoemission yield from differently doped semiconductor substrates. A similar phenomenon has been experimentally observed in case of the MOS systems,[7,9,10] with substrates of different types (N or P) and different doping densities. It is most pronounced (and best demonstrated) in case of a higher photocurrent, at a given positive gate voltage, due to electron photoemission from P^+-type than from N^+-type semiconductor substrates of the same doping density.

The purpose of this work is to give a quantitative characteristic of this phenomenon, allowing prediction of the electron photoemission yield from differently doped substrates of MOS structures. Taking into account significant differences in photoemission conditions existing at the dielectric-semiconductor interface, and at the clean semiconductor surface in vacuum, special attention was given to determination of the electron escape depth x_{esc}, which plays an important role in determining the yield of electron photoemission from a semiconductor. The value of this quantity in case of photoemission from Si into vacuum was estimated as $x_{esc} = 2.5$ nm in Ref. 4 and as $x_{esc} = 1.2$ nm in Refs. 5 and 6. In Refs. 4 and 6, it was also assumed that these values do not change significantly when the photon energy $h\nu$ changes in the range of $h\nu = 5.3$–6 eV. To the best of our knowledge, the only attempt at estimating the escape depth from the silicon substrate of the MOS structure was reported in a short note,[10] in which it was estimated at $x_{esc} = 4.5$ nm. No detailed description however was given in this note of the calculations leading to this result.

In Refs. 4 and 6, the photoemission yield, Y, vs. wavelength, λ, characteristics were used to determine the escape depth x_{esc}. Here, a different approach was applied, namely, the escape depth, x_{esc}, and the scattering length, ℓ, in the image force potential well were determined by fitting the experimentally determined yield vs. gate voltage, $Y(V_G)$, characteristics to the $Y(V_G)$ characteristics calculated for different ℓ and x_{esc} values.

In the experimental part of this research classical, large Al-SiO_2-Si structures were used. Although such structures are not of interest in present day electronics, they were used for two reasons:

— To maximize the sensitivity of the photoelectric measurements.
— To make use of the well established electrical and optical parameters and properties of such structures.

Throughout this paper, Boltzmann statistics is applied in relation to the carrier concentrations in substrates of the MOS structures under consideration, since doping density of these substrates does not exceed $3 \times 10^{18}\,cm^{-3}$, however, for the higher doping densities, close to $10^{19}\,cm^{-3}$ or higher, the full Fermi-Dirac statistics should be used instead of Boltzmann statistics.[11,12]

When accumulation or inversion is approached in the MOS structure, quantization of electron states in energy bands occurs due to the narrow potential well established at the dielectric-semiconductor interface. However, for the silicon doping levels and voltages applied in this work, these effects need not be taken into account for the following reasons.

For N^+-type substrate structures, where accumulation takes place, the small band bending at the silicon surface has practically no influence on the photoemission yield, Y, in comparison with the influence of scattering in the image force potential well. This is evidenced by the shape of the reduced Y vs. gate voltage, V_G, characteristics shown in Fig. 1, which does not show any influence of band bending (as opposed to the shape of their counterparts for the P^+-type substrate structures, shown in Figs. 2 and 3).

For P^+-type substrate structures, the large band bending at the substrate surface (see Fig. 5) does influence the photoemission yield as reflected in the reduced Y vs. V_G characteristics shown in Figs. 2 and 3. However, for the gate voltages used, inversion has not been reached and the potential well at the SiO_2-Si interface was too wide to cause quantization of electron states.[13,14]

II. THEORY

A. The yield of electron photoemission from P and N-type substrates

Although results of this research have a wider application, the main ideas will be explained by comparing the electron photoemission yields from substrates of MOS structures, which differ only in the substrate type (P^+ or N^+). The electron photoemission yield, Y, which is the ratio between the number of electrons contributing to the photocurrent and the number of photons impinging on the photoemitter is a result of two groups of processes taking place in the semiconductor photoemitter and in the barrier region of the dielectric.

The first group of these processes is characterized by the probability P1 of the electron photoemission from the semiconductor substrate valence band, over the energy barrier E_B at the semiconductor-dielectric interface (SDI). Following

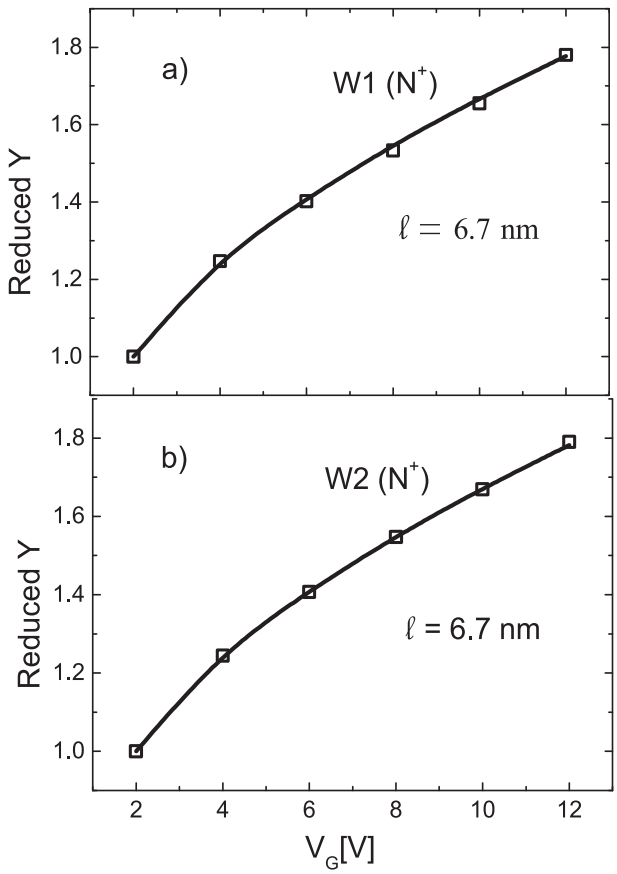

FIG. 1. Experimentally determined reduced Y vs V_G values (symbols) and the reduced Y(V_G) characteristics calculated using Eq. (5) for $\ell = 6.7$ nm (solid lines) for MOS structures on (a) wafer W1 and (b) wafer W2.

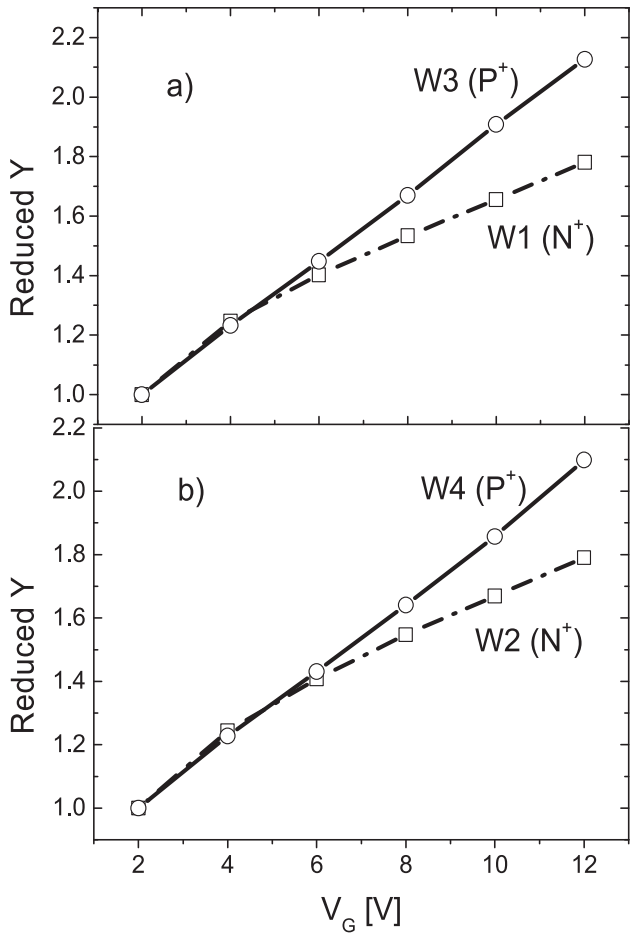

FIG. 2. Comparison of experimentally obtained reduced yield vs. gate voltage characteristics for MOS structures on (a) N^+ wafer W1 and P^+ wafer W3, and (b) N^+ wafer W2 and P^+ wafer W4. Straight lines connect the symbols representing measurement results.

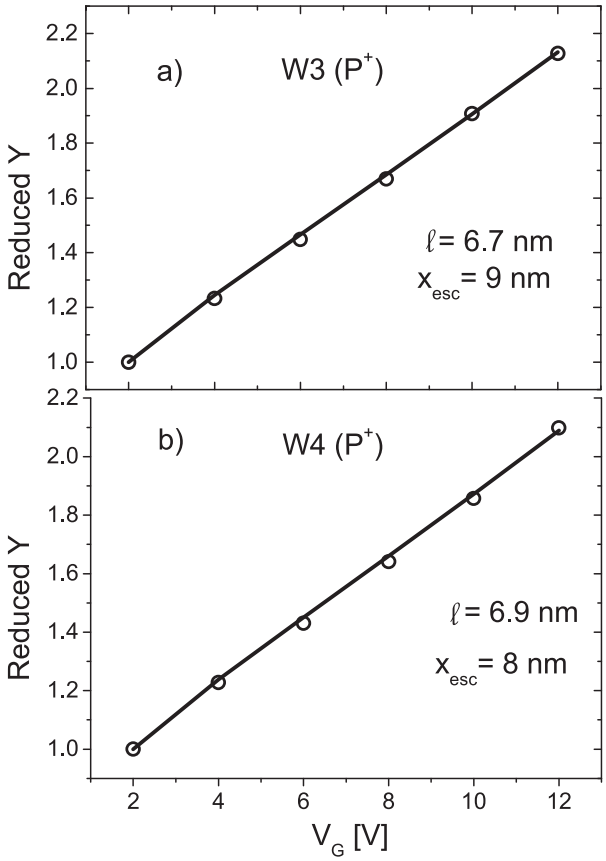

FIG. 3. Experimentally determined reduced Y vs V_G values (symbols) and the reduced $Y(V_G)$ characteristics calculated using Eq. (11) (solid lines) for MOS structures on (a) wafer W3 and (b) wafer W4. In calculations of the reduced Y vs. V_G characteristics, values of $\ell = 6.7$ nm, $x_{esc} = 9$ nm were used for structures on W3 wafer and values of $\ell = 6.9$ nm, $x_{esc} = 8$ nm were used for structures on W4 wafer.

Ref. 15, it is widely accepted[9,16,17] that this probability is given by the relation

$$P1 = A(h\nu - E_B + mV_I^{1/2})^3, \tag{1}$$

where $h\nu$ is the photon energy of light causing photoemission, V_I is the voltage drop in the dielectric layer, A is a function of $h\nu$, but does not depend on V_I.[18] Taking, z, as a coordinate perpendicular to the SDI, with $z = 0$ at the SDI and $z = z_I$ at gate dielectric interface (hence z_I is dielectric thickness), the m coefficient which is a constant for any particular MOS structure is given by

$$m = \sqrt{\frac{q}{4\pi\varepsilon_i\varepsilon_0 z_I}}, \tag{2}$$

here ε_i is the relative (optical) permittivity of the dielectric, ε_0 is the permittivity of free space, and q is the electron charge.

The second group of processes takes place in the dielectric between the SDI at $z = 0$ and the plane at $z = z_0$ at which the barrier reaches its maximum value. In the region between the SDI and $z = z_0$, electrons injected from the semiconductor substrate are scattered in the image force potential well and as a result some of them will not contribute to the photocurrent, being returned to the semiconductor substrate. The probability P2 of overcoming these scattering events by electrons photoinjected into the dielectric is given by[19]

$$P2 = C_1 \exp(-z_0/\ell), \tag{3}$$

where ℓ is the electron scattering length, C_1 is a constant, and z_0 is given by[9,19]

$$z_0 = \sqrt{\frac{qz_I}{16\pi\varepsilon_i\varepsilon_0 V_I}}. \tag{4}$$

As a consequence of the above, it is commonly accepted that the photoemission yield Y, in case of electron photoemission from the semiconductor substrate is given by the relation[9]

$$Y = C(h\nu)(h\nu - E_B + mV_I^{1/2})^3 \exp(-z_0/\ell). \tag{5}$$

It should be noted, however, that the influence of band bending at the semiconductor surface on the photoemission yield has not been taken into account in Eq. (5). However, the band bending does have an influence on the photoemission yield, which results from the following. The light illuminating the MOS structure penetrates to a certain depth into the semiconductor substrate. Taking x as a coordinate perpendicular to the SDI with $x = 0$ at the SDI and increasing with increasing depth into the substrate, electrons photo excited in a substrate layer of thickness dx at a distance x from the SDI have to surmount a barrier which is lower by $\Delta E_B(x)$ then the barrier E_B at $x = 0$, as illustrated in Fig. 4. Hence, Eq. (5) should be complemented by taking into account the influence of $\Delta E_B(x)$ on photoemission yield, as shown below

$$Y(x) = C(h\nu)(h\nu - E_B + mV_I^{1/2} + \Delta E_B(x))^3 \exp(-z_0/\ell). \tag{6}$$

To determine the influence of $\Delta E_B(x)$ on the photoemission yield, consider the following:

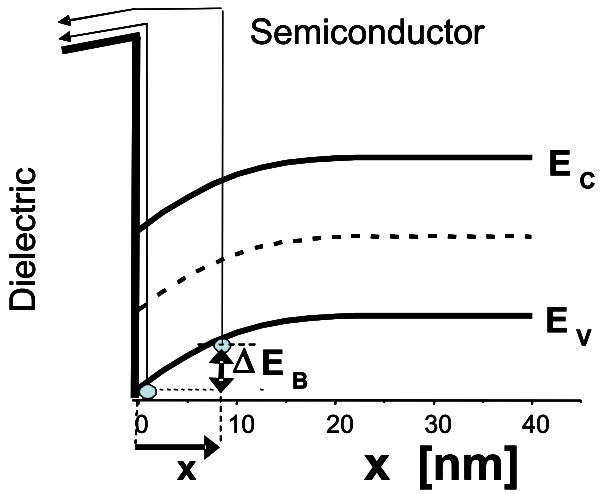

FIG. 4. Band diagram of the dielectric-semiconductor interface showing that the electron photo excited at a distance x from the interface may have to overcome a lower (by $\Delta E_B(x)$) barrier to get into the conduction band of the dielectric than the electron photo excited at $x = 0$.

The number of electrons n(x) photo excited at depth x in the substrate is proportional to the light intensity i(x) which penetrates the distance x into the semiconductor

$$n(x) = C_2 i(x), \tag{7}$$

where C_2 is a constant and i(x) is given by

$$i(x) = i(0)\exp(-\alpha x), \tag{8}$$

here i(0) is the light intensity at the SDI (at $x = 0$) and α is the absorption coefficient of the semiconductor substrate, given by

$$\alpha = \frac{4\pi k}{\lambda}, \tag{9}$$

where k is the extinction coefficient and λ is the wavelength of light. The k(λ) characteristics are known for commonly used semiconductors.[20] Both i(0) and α are further assumed to be the same for N and P-type semiconductors of the same doping density.

Another fact that has to be taken into account is that, due to scattering, only a part of the electrons photo excited at depth x in the semiconductor arrives at the SDI and may attempt to overcome the potential barrier. The probability that n electrons photo excited at depth x will be able to reach SDI is given by[4]

$$P3 = n(x)\exp(-x/x_{esc}) = C_3 i(0)\exp[-(\alpha + 1/x_{esc})x], \tag{10}$$

where C_3 is a constant and x_{esc} is the escape depth of electrons, which we will try to determine in this investigation.

Taking the above considerations into account, Eq. (6) may be replaced by

$$Y = C(h\nu)B\exp(-z_0/\ell), \tag{11}$$

where B is a function which will be determined now. The elementary component of this function is given by

$$dB(x) = (h\nu - E_B + mV_I^{1/2} + \Delta E_B(x))^3 \exp[-(\alpha + 1/x_{esc})x]dx. \tag{12}$$

Hence

$$B = \int_0^\infty (h\nu - E_B + mV_I^{1/2} + \Delta E_B(x))^3 \exp[-(\alpha + 1/x_{esc})x]dx. \tag{13}$$

To calculate the value of B, one has to find the $\Delta E_B(x)$ function which directly depends on the potential profile $\phi(x)$ (or the band bending) in the semiconductor and is given by

$$\Delta E_B(x) = \phi(0) - \phi(x), \tag{14}$$

where $\Delta E_B(x)$ is expressed in eV.

Hence, determination of the potential profile $\phi(x)$ will be discussed in Sec. II B.

B. Determination of the potential profile in P and N-type substrates of MOS structures

To determine the potential profile $\phi(x)$, we start from the relation which is valid for any MOS system with a metal gate

$$V_G = \phi(0) + V_I + \phi_{MS}, \tag{15}$$

in which V_G is the gate potential, V_I is the voltage drop in the dielectric, ϕ_{MS} is the effective contact potential difference between the gate and the substrate, and $\phi(0)$ is the surface potential of the semiconductor $\phi(x = 0)$, as shown in Fig. 5.

The value of V_I in a real MOS structure is given by

$$V_I = -\frac{Q_S + Q_{eff}}{C_I}, \tag{16}$$

where Q_S is the semiconductor surface charge, Q_{eff} is the effective charge of the dielectric, and C_I is the capacitance of the dielectric layer.

For a given MOS structure of known ϕ_{MS}, Q_{eff}, and C_I values, a matrix of correspondence between $\phi(0)$ and V_G values can be established. This is done by assuming a set of $\phi(0)$ values, calculating by standard methods the corresponding Q_S values and the values of V_I using Eq. (16), which allows determination of V_G using Eq. (15). The so established correspondence between the sets of $\phi(0)$ and V_G values can be accurately approximated by an analytic function g, such that

$$\phi(0) = g(V_G), \tag{17}$$

which allows immediate determination of semiconductor surface potential $\phi(0)$, for a given gate voltage V_G.

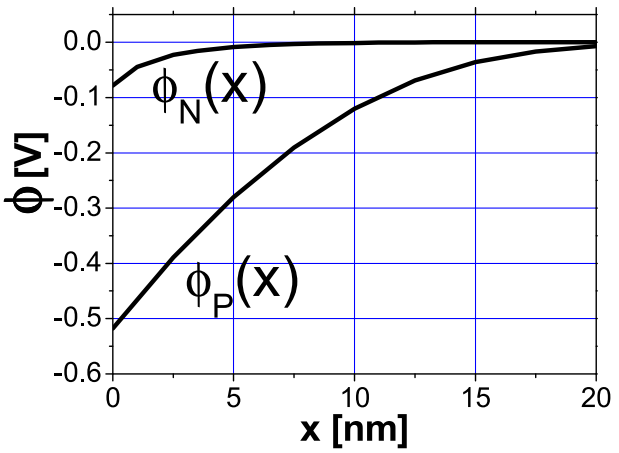

FIG. 5. Illustration of different band bendings in N^+ ($\phi_N(x)$) and P^+-type ($\phi_P(x)$) silicon substrates of the same doping density $N = 2 \times 10^{18}\,cm^{-3}$, calculated for the Al-$SiO_2$-Si system, with SiO_2 layer thickness $t_{ox} = 60\,nm$ at the gate voltage $V_G = 9\,V$. The assumed effective oxide charge density is $Q_{eff}/q = 2 \times 10^{11}\,cm^{-2}$ and the effective contact potential difference is $\phi_{MS}(N) = 0.03\,V$ for the N^+-type substrate and $\phi_{MS}(P) = -0.96\,V$ for the P^+-type substrate.

The shape of the potential barrier $\phi(x)$ can be found using the relation[12]

$$\frac{x}{L_D} = \int_{u(0)}^{u} \frac{du}{\sqrt{e^{u_F}(e^{-u}+u-1)+e^{-u_F}(e^{u}-u-1)}}, \quad (18)$$

in which

$$u = u(x) = \frac{q\phi(x)}{k_B T} \text{ and } u_F = \frac{q\phi_F}{k_B T}, \quad (19)$$

where q is the electron charge, ϕ_F is Fermi potential in the semiconductor, k_B is the Boltzmann constant, T is the temperature, and L_D is the intrinsic Debye length of the semiconductor, given by

$$L_D = \sqrt{\frac{\varepsilon_{rs}\varepsilon_0 k_B T}{2q^2 n_i}}. \quad (20)$$

Here, ε_{rs} is the relative electrical permittivity of the semiconductor, ε_0 is the electrical permittivity of free space, $k_B T/q$ is the diffusion potential, and n_i is the semiconductor intrinsic carrier concentration.

Numerical integration of Eq. (18) for a set of u values (between $u = u(x = 0)$ and $u = 0$) establishes the correspondence between u and x values. This allows, making also use of Eq. (19), to determine the analytic function $\phi(x)$ approximating the shape of the potential distribution.

It has to be stressed here that $\phi(x)$ distributions in P and N-type semiconductor substrates of the same doping density and at the same gate voltage are quite different, as illustrated in Fig. 5 for P^+ and N^+-type substrates. Once the potential distribution, $\phi(x)$, has been determined, the $\Delta E_B(x)$ function can be found using Eq. (14) and used in Eq. (13) to determine the B value and subsequently the photoemission yield Y from Eq. (11).

III. EXPERIMENTAL

The samples used in this investigation were Al-SiO_2-Si structures with circular gates of 1 mm diameter and with gate thickness $t_{Al} \approx 20$ nm. A series of heavily phosphorus doped and heavily boron doped silicon wafers of (111) orientation were used as substrates of the MOS structures to be used in this investigation. After the initial cleaning sequence, the wafers were thermally oxidized in dry oxygen at a temperature $T = 1000\,^{\circ}C$, with a 10 min post oxidation annealing in nitrogen, to grow a SiO_2 layer of thickness $t_{ox} \approx 70$ nm. Aluminum metallization was sputtered on the front side and patterned by photolithography. Backside oxide was etched off and aluminum contact was sputtered on the backside. Post metallization annealing was carried out for 20 min in the forming gas atmosphere, at the temperature $T = 450\,^{\circ}C$. After rejecting the defective structures on each of the wafers, electrical and photoelectric measurements were made on at least 6 MOS structures on each of the 4 wafers chosen for this investigation, i.e., 2 (N^+) wafers designated W1 and W2 and 2 (P^+) wafers designated W3 and W4. Average values were found of each parameter measured on structures of each wafer and these average values were used in further analysis and processing of the data.

C(V) measurements were made (on at least 6 structures on each wafer), both in the dark and under the same illumination conditions under which photoelectric measurements were made. From the results of dark C(V) measurements, the oxide thickness t_{ox} was determined, as well as the substrate doping density (N_D or N_A), which was determined making use of the method based on the slope determination of the $1/C^2 = f(V_G)$ characteristic, as it is applied for MOS structures.[12,22,23]

The thickness of the oxide was confirmed by independent spectro-ellipsometric measurement, with negligible differences between t_{ox} values determined by both methods. The C(V) measurements under illumination were made to allow determination to what extent the illumination influences the surface potential $\phi(0)$ in the subsequent photocurrent measurements. Under the very low illumination level (the power of the light beam $P \approx 10\,\mu W$) used for both photocurrent and C(V) measurements, it was found that the change in the surface potential $\Delta\phi(0)$ caused by illumination was $\Delta\phi(0) < 1$ mV for N^+-type substrates and $\Delta\phi(0) < 5$ mV for P^+-type substrates. Hence, this influence on the surface potential was neglected in further considerations.

Photoelectric measurements were made using the multifunctional system for photoelectric measurements (MSPM), described elsewhere.[21] To determine the experimental $Y = f(V_G)$ characteristics, photocurrent I vs. wavelength λ characteristics were first taken for different gate voltages V_G, at a constant power P of the light beam illuminating the structure. Typical example of such $I(\lambda)$ characteristics is shown in Fig. 6. The shape of these characteristics and the wavelength $\lambda(I_{max})$ at which the photocurrent reaches the maximum value is determined by the optical properties of the Al-SiO_2-Si stack. Namely, the optical interference of light in the SiO_2 layer causes that the power of light absorbed by the silicon substrate P_T, changes with changing the wavelength, while the power P of light illuminating the entire structure is kept constant by the measurement system. This influence of wavelength on the photocurrent can be quantitatively determined, as shown in Refs. 12 and 24. As shown in Fig. 6, for MOS structures used in this investigation, the maximum current value I_{max} is obtained for the wavelength $\lambda(I_{max}) = 214$ nm, i.e., for photon energy $h\nu(I_{max}) = 5.79$ eV. Further analyses and calculations are based on investigation of the I_{max} vs. V_G characteristics, at a constant value of photon energy $h\nu(I_{max}) = 5.79$ eV.

At $I = I_{max}$, the relation between the photoemission yield Y and the photocurrent I_{max} is given by the formula

$$Y(h\nu, V_G) = \frac{I_{max} h\nu(I_{max})}{P_T}, \quad (21)$$

in which I_{max} is the maximum photocurrent value in [A], $h\nu$ is the photon energy in [eV] at $I = I_{max}$, and P_T is the light power absorbed in the substrate in [W]. Since all photocurrent measurements were made at the same illumination

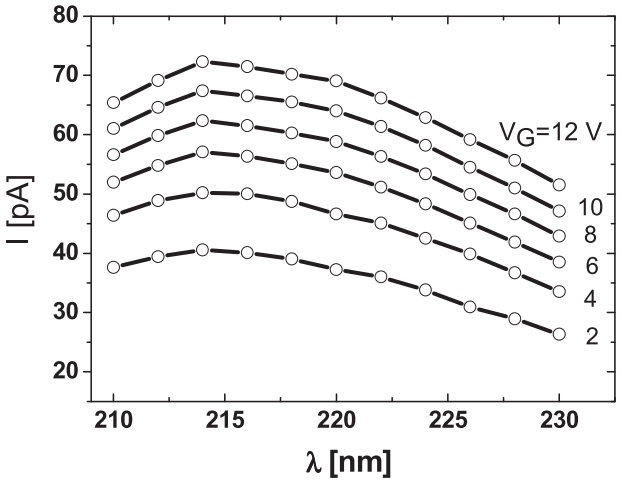

FIG. 6. Typical example of experimental photocurrent I vs. wavelength λ characteristics, taken for a MOS sample on N^+ substrate, at different gate voltages V_G in the vicinity of the photocurrent maximum.

conditions (same $h\nu$ and P_T values), a direct proportionality between Y and I_{max} was maintained throughout the measurements. The average I_{max} values (for at least 6 measured structures) were determined for the gate voltages $V_G = 2$, 4, 6, 8, 10, and 12 V. The gate voltage range of $V_G = 2$–12 V was chosen for the following reasons. The upper voltage limit (12 V) was chosen because at that voltage the z_0 value approaches 1 nm, below which (for higher voltages) the simple image force theory applied in our analysis is no longer valid, as indicated in Ref. 19. The lower voltage limit (2 V) was chosen because at that voltage the electric field in the dielectric approaches 10^5 V/cm, below which our Eqs. (5) and (11), as well as Eqs. (15) and (16) in Ref. 19 do not correctly describe the dependence of photocurrent on the electric field in the dielectric, as shown in Refs. 25 and 26. The average I_{max} values at different gate voltages were reduced to the average I_{max} value for $V_G = 2$ V. The reduced $I_{max}(V_G)$ characteristics are identical with the similarly determined reduced $Y(V_G)$ characteristics.

The reproducibility of the reduced $Y(V_G)$ characteristic measurement results is very good as demonstrated in Fig. 7(a), for MOS structures on N^+-type wafers (W1 and W2) and in Fig. 7(b), for structures on P^+-type wafers (W3 and W4).

IV. RESULTS AND DISCUSSION

As expected, the $Y(V_G)$ characteristics taken for structures on P^+-type wafers are quite different from their counterparts taken for structures on N^+-type wafers, as shown in Figs. 2(a) and 2(b). This results from the fact that in case of the MOS structures on P^+-type substrates, the ΔE_B component of Eq. (13) plays a significant role, particularly at higher gate voltages, while for structures on N^+-type substrates its role is insignificant (see Fig. 5). Hence, for the structures on N^+-type wafers (W1 and W2), it is assumed that the Y vs. V_G characteristic behaves according to Eq. (5), while for the structures on P^+-type wafers (W3 and W4), the entire equation (11) applies. To compare the calculation results with the experimental data for structures on wafers W1 and W2, the $C(h\nu)$ value in Eq. (5) was chosen in such a way as to obtain fit between the calculated and measured Y values at the lowest gate voltage used (2 V in this case). Then the reduced Y vs. V_G characteristic was determined by dividing Y values for all gate voltages by the Y value at $V_G = 2$ V, so that the reduced Y for $V_G = 2$ V becomes equal to 1. These reduced Y vs. V_G characteristics are further used in fitting the calculated curve with the measurement results. The best fit of Eq. (5) to the measurement results of structures on both W1 and W2 wafers yields the value of scattering length $\ell = 6.7$ nm, as shown in Figs. 1(a) and 1(b).

For structures on P^+-type wafers (W3 and W4), calculations using the entire equation (11) were compared to the measurement results as shown in Figs. 3(a) and 3(b). The value of the B function, given by Eq. (13) was determined by numerical integration, for a number of x_{esc} values. To speed up this operation, the upper integration limit was taken as the x value at which the potential $\phi(x)$ falls down to 2% of its value at the SDI ($0.02\ \phi(0)$). All the factors appearing in Eq. (13) were determined as described in Sec. II, with the barrier height at the Si-SiO_2 interface taken as $E_B = 4.35$ eV. Having determined the B function for different x_{esc} values, the value of $C(h\nu)$ in Eq. (11) was again chosen in such a way, as to obtain fit between calculated and experimental Y values at the lowest gate voltage used ($V_G = 2$ V in our case) and the reduced Y vs. V_G characteristic was determined in

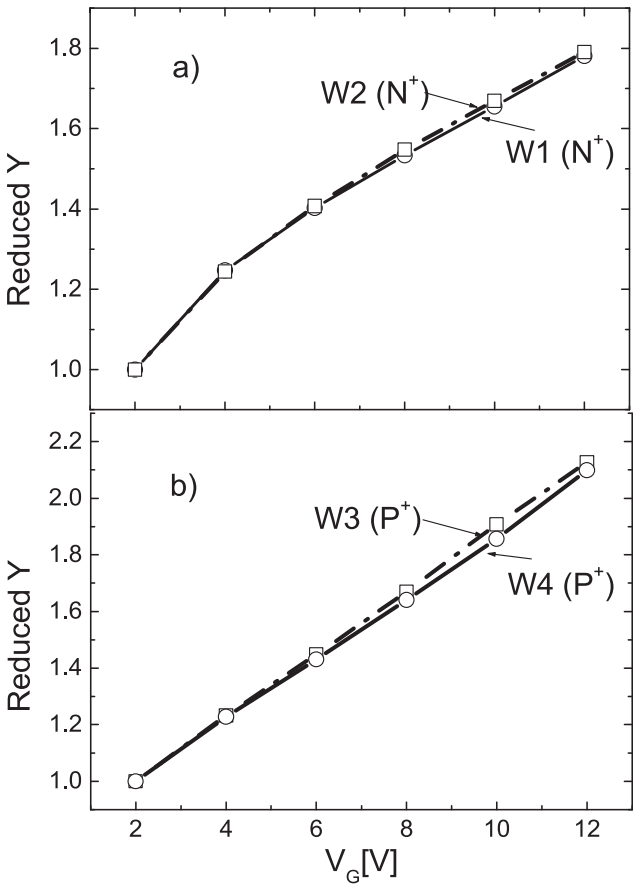

FIG. 7. Comparison of experimentally obtained reduced yield vs. gate voltage characteristics for MOS structures on (a) N^+ wafers W1 and W2 and (b) P^+ wafers W3 and W4. Straight lines connect the symbols representing measurement results.

the same way as it was done for structures on N^+ substrates. The shape of the reduced Y vs. V_G characteristic for structures on P^+-type substrates depends on the relative roles played by the scattering length, ℓ, and the escape depth, x_{esc}. For larger, ℓ, values the slope of the reduced Y vs. V_G characteristic decreases with increasing V_G, while it increases for the larger values of x_{esc}. In other words, the increasing value of, ℓ, tends to make the $Y(V_G)$ characteristic more convex, while the increasing, x_{esc}, value tends to make it more concave. This property allows determination of both the values of the scattering length ℓ and of the escape depth x_{esc}, which yield the best fit of the calculated and experimental reduced Y vs. V_G characteristics. In fitting the calculated characteristics to the experimental ones, it is important and helpful to realize that the influence of the scattering length, ℓ, on the $Y(V_G)$ characteristics is the strongest for low V_G values, when the z_0 value is large (see Eq. (4)), while the influence of, x_{esc}, is the strongest for large V_G values, when the band bending becomes large.

For structures on wafer W3, the best fit was obtained for the scattering length $\ell = 6.7$ nm and the escape depth $x_{esc} = 9$ nm, while for structures on wafer W4, the values of $\ell = 6.9$ and $x_{esc} = 8$ nm yielded the best fit, as shown in Figs. 3(a) and 3(b).

Various situations resulting from possible measurement errors and possible inaccuracies in determination of parameters used in calculations of the I vs. V_G curves were simulated to estimate the accuracy of the described method. The reproducibility of measurement results, as well as the resolution in assessing the fit between measurement results and the calculated curves were also taken into account in the simulation procedures. As a result of these simulations, we estimate that the accuracy of scattering length, ℓ, determination is better than ± 1.0 nm and the accuracy of escape depth, x_{esc}, determination is better than ± 2.0 nm.

V. CONCLUSIONS

The yield of electron photoemission from differently doped substrates of MOS structures has been quantitatively analyzed and an original method of photoelectron escape depth x_{esc} determination in the MOS system has been developed. This method is based on the examination of the photoemission yield Y vs. gate voltage V_G characteristics of the structures under investigation. Calculation procedures have been developed allowing determination of the reduced yield vs. gate voltage $Y(V_G)$ characteristics of such structures. Photoelectric measurements have been made on a series of MOS samples with N^+ and P^+ substrates and their experimental $Y(V_G)$ characteristics have been determined. Both the calculated and experimentally determined electron photoemission yields were found to be higher for P^+ than for N^+ substrate structures. As stated in the Introduction, this phenomenon observed earlier, caused our attempt at quantitative characterization of electron photoemission yields from differently doped substrates of MOS structures.

Two physical phenomena were found to have the decisive influence on the values of the photoemission yield Y and on the shape of the reduced Y vs. gate voltage V_G characteristics: The electron scattering in the image force potential well, represented by the scattering length, ℓ, and the electron escape depth from the semiconductor substrate, represented by the escape depth x_{esc}. Taking into account the different influence of ℓ and x_{esc} on the shape of the reduced Y vs. V_G characteristic, one can determine both the scattering length, ℓ, and the escape depth, x_{esc}, by finding the best fit between the experimental reduced $Y(V_G)$ characteristic and the corresponding characteristic calculated using the relations derived in this paper.

It was found that the scattering length, ℓ, has nearly the same value of $\ell = 6.7$–6.9 nm for all the identically processed wafers of the examined lot of samples. This fact, together with the observation that other values of, ℓ, were found for differently processed wafers, indicates the processing dependence of the scattering length, or in other words, the dependence of, ℓ, on the quality of the oxide layer. It is worthwhile to notice that the, ℓ, values found in this work are larger than the value of $\ell = 3.4$ nm obtained in Ref. 19 and used by other authors since then.

In this study, the ℓ value was determined using the photon energy of $h\nu = 5.79$ eV while in Ref. 19 the photon energy of 5.0 eV was used. Hence, the ℓ value determined in this work may (potentially) differ from the one determined at 5.0 eV. It was pointed out however in Ref. 19, as well as in, e.g., Refs. 27 and 28, that with increasing energy of excited electrons more intensive scattering takes place, hence ℓ becomes shorter. This means that if our measurements were made at 5.0 eV, we could have obtained still higher values of ℓ. This leaves us with the conclusion that the scattering lengths in the structures used in our work are longer than in the structures under consideration in Ref. 19.

The escape depth determined for the structures on P^+-type substrates was found to be $x_{esc} = 8$–9 nm being significantly larger than the values of $x_{esc} = 1.2$–2.5 nm determined previously for external photoemission from silicon into vacuum,[4–6] it is also larger than the value of $x_{esc} = 4.5$ nm estimated in Ref. 10. These results suggest a difference in the structure of the sub-surface layers of oxidized silicon and of the sub-surface layers of silicon with the uncovered surface exposed to vacuum.

[1]J. J. Scheer and P. Zalm, Philips Res. Rep. **14**, 143 (1959).
[2]J. J. Scheer, Philips Res. Rep. **15**, 584 (1960).
[3]J. Van Laar and J. J. Scheer, Philips Res. Rep. **17**, 101 (1962).
[4]G. W. Gobeli and F. G. Allen, Phys. Rev. **127**, 141 (1962).
[5]L. F. Wagner and W. E. Spicer, Phys. Rev. Lett. **28**, 1381 (1972).
[6]C. Sebenne, D. Bolmont, G. Guichar, and M. Balkanski, Phys. Rev. B **12**, 3280 (1975).
[7]V. K. Adamchuk and V. V. Afanas'ev, Prog. Surf. Sci. **41**, 111 (1992).
[8]V. V. Afanas'ev and A. Stesmans, J. Appl. Phys. **102**, 081301 (2007).
[9]V. V. Afanas'ev, *Internal Photoemission Spectroscopy: Principles and Applications* (Elsevier, Amsterdam, 2008).
[10]V. A. Gritsenko and K. P. Mogil'nikov, Sov. Phys. Semicond. **13**, 1162 (1979).
[11]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, Hoboken, 2007).
[12]E. H. Nicollian and J. R. Brews, *MOS (Metal-Oxide-Semiconductor) Physics and Technology* (Wiley, New York, 1982).
[13]F. Stern, CRC Crit. Rev. Solid State Sci. **4**, 499 (1974).
[14]T. Ando, A. B. Fowler, and F. Stern, Rev. Mod. Phys. **54**, 437 (1982).
[15]R. H. Fowler, Phys. Rev. **38**, 45 (1931).

[16]E. O. Kane, Phys. Rev. **127**, 131 (1962).
[17]E. O. Kane, Phys. Rev. **147**, 335 (1966).
[18]R. J. Powell, J. Appl. Phys. **41**, 2424 (1970).
[19]C. N. Berglund and R. J. Powell, J. Appl. Phys. **42**, 573 (1971).
[20]E. D. Palik and G. Ghosh, *Electronic Handbook of Optical Constants of Solids* (Academic, 1999).
[21]S. Porebski, P. Machalica, J. Zajac, L. Borowicz, A. Kudla, and H. M. Przewlocki, IEE Proc.-Sci., Meas. Technol. **150**, 148 (2003).
[22]W. Van Gelder and E. H. Nicollian, J. Electrochem. Soc. **118**, 138 (1971).
[23]D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).
[24]R. J. Powell, J. Appl. Phys. **40**, 5093 (1969).
[25]H. M. Przewlocki, J. Appl. Phys. **78**, 2550 (1995).
[26]H. M. Przewlocki, J. Appl. Phys. **85**, 6610 (1999).
[27]C. N. Berglund and W. E. Spicer, Phys. Rev. **136**, A1030 (1964).
[28]J. J. Quinn, Phys. Rev. **126**, 1453 (1962).