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Sb-Heterostructure Backward Diode for Millimetre-Wave Detection

Master's Thesis in the Master's Programme Wireless and Photonics Engineering

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CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2012

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Cover:
The Scanning Electron Micrograph (SEM) of a Sb-heterostructure backward diode with the circular cathode radius of 0.65 μm.

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Abstract

Sb-heterostructure backward diode (HBD) is one of the most promising candidates for millimitre-wave and terahertz direct detection. Sb-HBDs have demonstrated excellent performance in the millimetre-wave range with high sensitivity, high cut-off frequency and low noise characteristics. Although Sb-HBDs are also predicted to be very promising for terahertz frequency applications, little effort has been made, and few have reported on its operation above 100 GHz. From the material point of view, few have reported on how the material quality affects the device performance. This thesis work encompasses modelling, fabrication and characterisation of Sb-HBDs, to explore the potential of Sb-HBDs for terahertz direct detection and to improve the device performance through material growth optimisation. The first part of this thesis deals with modelling of Sb-HBD diode to perceive the underlying physics of the device and to guide the experimental work. This is done by using Synopsys' TCAD Sentaurus software. As the second part of this thesis, MBE growth of Sb-HBDs has been conducted to investigate the effect of various buffer thicknesses and the tunnelling interface (InAs/AlSb) bonding types. Large scale test diodes were fabricated and the I-V characterisation was assessed at both ambient and cryogenic temperatures. Finally, fabrication techniques of sub-micron scale devices were developed.

Keywords: millimetre-wave detectors, terahertz, direct detectors, Sb-heterostructure backward diodes

Contents

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Abbreviations and Notations

β_v	Voltage sensitivity
γ	Curvature coefficient
ρ	Total charge density
ε	Dielectric constant
ε_s	Permittivity
φ	Wavefunction
C_j	Junction capacitance
E_0	Energy
E_g	Bandgap
f_c	Cut-off frequency
F_A	Quasi-Fermi level in region A
F_B	Quasi-Fermi level in region B
G^{b2b}	Band-to-band generation rate
G_n	Electron generation rate
h	Planck's constant ($6.626 10^{-34}$ J.s)
J_n	Electron current density
J_t	Tunnelling current
$K(x)$	Wave vector
m^*	Effective mass
N_A	Number of filled states in region A
N_B	Number of empty states in region B
N_D	Donor's Impurity concentration
q	Elementary charge
R_J	Junction resistance
R_n	Electron recombination rate
R_s	Series resistance
T	Temperature

T_t	Tunnelling probability or transmission amplitude
U	Potential barrier height
V_n'	Energy difference between conduction band edge and Fermi level in the n-region
V_p'	Energy difference between valence band edge and Fermi level in the p-region
Z_s	Source impedance
AP	Adhesion Promoter
BCB	Benzocyclobutene
CVD	Chemical Vapor Deposition
DUV	Deep Ultraviolet
FIB-SEM	Focused Ion Beam-Scanning Electron Microscope
GHz	Gigahertz
GSG	Ground-Signal-Ground
GUI	Graphical User Interface
HBD	Heterostructure Barrier Diode
HBT	Heterojunction Bipolar Transistor
HCl	Hydrochloric acid
HEMT	High Electron Mobility Transistor
ICP	Inductively Coupled Plasma
IF	Interface bonding
IPA	Isopropanol
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MMW	Millimetre-Wave
mTorr	MilliTorr (0.133322 Pascals)
NDR	Negative Differential Resistance
NEP	Noise Equivalent Power
P(MMA)	Poly(Methyl Methacrylate)

|	
PDBD	Planar Doped Barrier Diode
RIE	Reactive-Ion Etching
RT	Room Temperature
RTD	Resonant Tunnelling Diode
SBD	Schottky Barrier Diode
sccm	Standard Cubic Centimeters per Minute
SEM	Scanning Electron Microscope
SMMW	Sub-Millimetre-Wave
TCAD	Technology Computer-Aided Design
TEM	Transmission Electron Microscopy
TLM	Transmission Line Model
WKB	Wentzel Kramers Brillouin

1 Introduction

1.1 Introduction to Millimetre-Wave Detection

Before beginning an in-depth discussion of millimetre-wave detection systems, it is essential to understand the characteristics of millimetre-waves. Millimetre-waves are defined as those of having the wavelength range, 10 to 1 millimetre (30-300 GHz). That is; they have longer wavelength than infrared waves, yet smaller wavelengths than microwaves and radio waves, see Figure 1.1. There are various applications in the millimetre-wave (MMW) region, due to the atmospheric propagation characteristics at these frequencies such as radar, avionics, safety, security and imaging [1], [2]. One of the most prominent applications is imaging resulting from lower scattering and absorption by atmospheric obscurant and water vapor [3]. Lower attenuation of radiation in the MMW region compared to visible and infrared radiation, along with the potentiality of usage in day or night and low-visibility conditions (e.g. foggy weather), have made MMW radiation an attractive candidate for imaging, see Figure 1.2.

Generally speaking, imaging techniques in MMW region are classified as either ac-
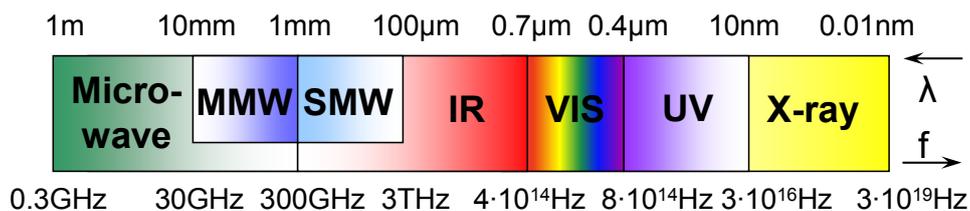
Figure 1.1: *Electromagnetic spectrum showing the location of millimetre and sub-millimetre waves (MMW and SMMW) [4].*
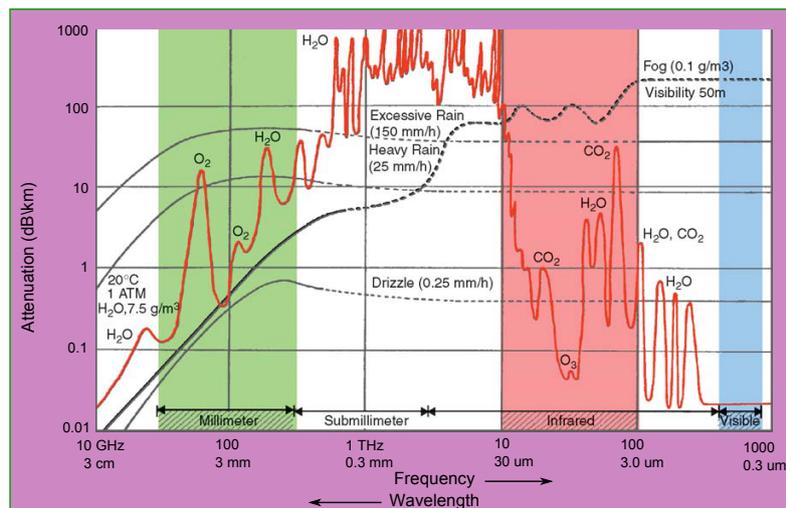
Figure 1.2: *The attenuation of radiation from visible to radio frequency under clear weather conditions (red curve, which shows the absorption by atmospheric constituents such as water vapor (H_2O) and oxygen) and under poor conditions e.g. foggy weather[2].*

(a) Active imaging method   (b) Passive imaging methode
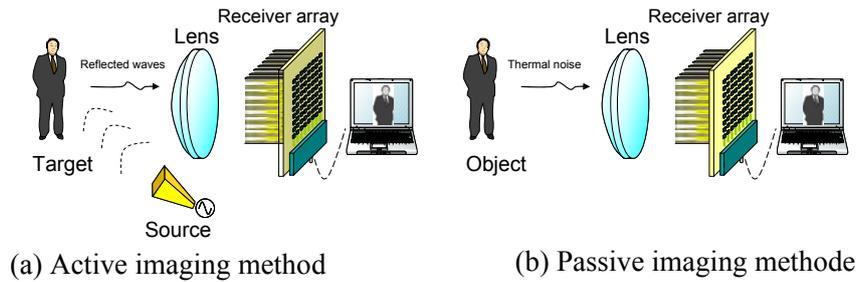
Figure 1.3: *The classification of imaging methods: Active and passive imaging [8].*

tive or passive imaging method, see Figure 1.3. In the active detection technique the object is illuminated using a source and the detector senses the scattered radiation [5]. The illumination of the subjected scene increases both the signal level and the scene contrast. However, the drawback of these systems is that the power consumption, complexity and the cost are appreciably increased, mainly due to the use of oscillators and amplifiers. However, this method has found applications in chemical detection, material analysis and indoor security screening [6], [7], [4].

In passive MMW imaging technique the received emissivity (blackbody radiation from objects) of different materials is assessed, and the contrast between warm and cold body (e.g. detecting cooler metal weapon from warmer human body) is detected [5]. By eliminating the use of a source, the passive imaging technique tackles the problem of high cost and complexity. It should be noted that, passive imaging technique in MMW region has its own challenges. As can be seen in Figure 1.4, the conspicuous issue is the weakness of the blackbody radiation from room-temperature (RT) objects at MMW frequencies compared to infrared frequencies. Consequently, the passive imaging technique requires highly sensitive and extremely low-noise detector technology. Although the passive technique's image quality is not as good as active's, it has found applications such as vision under adverse weather and detection of concealed weapons (outdoor security screening) [4].
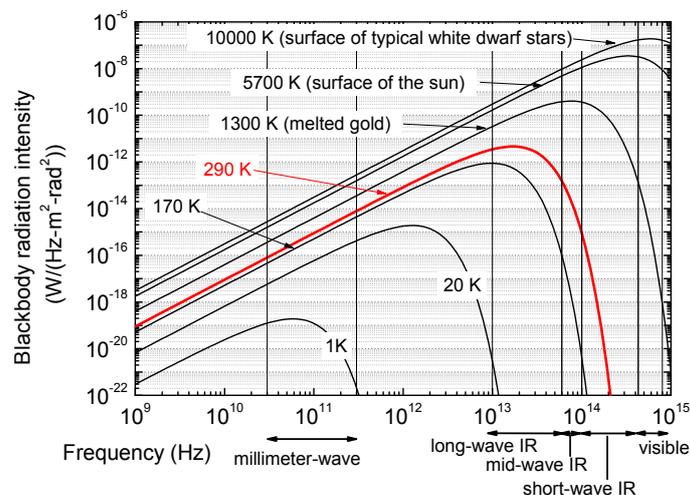
Figure 1.4: *The blackbody radiation intensity curve [6].*

(a) Heterodyne detection   (b) Direct detection with peramplifier   (c) Direct detection
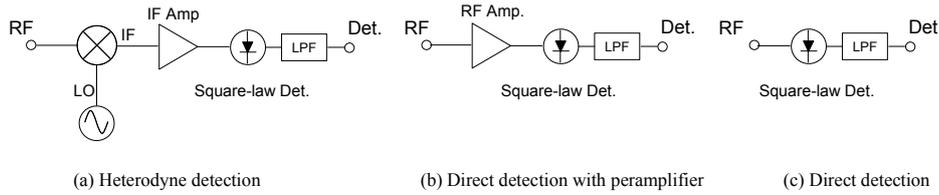
Figure 1.5: *The schematic of receiver's front-end block diagram with heterodyne detection method (a) and direct detection with (b) and without pre-amplification (c) [8].*

1.2   Millimetre-Wave Detectors

Detection in millimetre and sub-millimetre wave region is classified into two types; Coherent and incoherent detection. The fundamental difference between these two methods is that in the incoherent or direct method only the amplitude of the signal can be detected, while with the coherent or heterodyne method both the amplitude and phase of the signal are detected [9].

Heterodyne detection systems offer higher spectral resolution [9], although meeting the requirements such as local oscillators power and fast detector response is critical, see Figure 1.5(a). Given the complexity and bulkiness of these systems, it is challenging to scale them into 2-D arrays of detectors which are suitable for imaging applications. Heterodyne detection systems with frequency selectivity, and strong directivity are useful in applications such as astronomical measurements [10].

When ultra-high spectral resolution is not required [11], the heterodyne configuration is problematic for attaining high frame rates and low-cost passive imaging applications. To circumvent these problems, the direct detection method is chosen, see Figure 1.5(b) and (c). Direct detection method has compact, low power and low cost system block. By choosing a highly sensitive and extremely low noise detector the need for pre-amplification is eliminated and the system block is further simplified, as it is shown in Figure 1.5(c). Generally, direct detectors are utilised in applications such as spectroscopy and technical vision systems where sensitivity is more critical than spectral resolution.

So far, among direct detectors, low-temperature bolometers have exhibited highest sensitivity with the noise equivalent power (NEP) limited by the cosmic background radiation fluctuations up to $\sim (0.4-3)*10^{-19} W/Hz^{\frac{1}{2}}$ at $\sim 100-300mK$ temperatures [9]. Also, there exist different types of cooled semiconductor detectors (e.g. hot electron InSb, Si, Ge bolometers) with NEP of $\sim 10^{-13} - 5 \times 10^{-17} W/Hz^{\frac{1}{2}}$ operated at $T \leq 4$ K [9]. Furthermore, among the RT direct detectors the NEP ranges from 10^{-10} to $10^{-9} W/Hz^{\frac{1}{2}}$ [9]. RT semiconductor detectors can be advantageous over both cooled semiconductor detectors and bolometers considering the low cost, less complexity, and low power consumption of the set up. Additionally, towards sub-millimetre wave frequencies, there is still lack of RT semiconductor-based direct detectors with relatively high sensitivity.

Most of the semiconductor-based detectors are biased to decrease the impedance to facilitate the impedance matching. However, the bias circuitry induces the flicker noise (1/f) and adds up complexity to the system. Therefore, the zero-bias rectification is a favorable feature for imaging applications.

Based on principle of operation, these diodes are divided into thermionic-emission diodes such as Schottky barrier diodes (SBD) [12] and quantum mechanical tunnelling based diodes e.g. Esaki Diode [13]. Also, there exist diodes which operate based on the mixture of the two current mechanisms such as the case for planar doped barrier diodes (PDBD) [14].

In SBDs, forward current is due to the injection of majority carriers from semiconductor into metal. The absence of minority carrier injection in low current levels and the associated storage delay time are the main reasons for high frequency properties and high switching speed of SBDs. However, strong temperature dependence is one of the disadvantages of Schottky diodes performance [15]. SBDs are usually biased to provide sufficient curvature coefficient of the I-V curve. This brings about the major shortcoming of SBDs, the 1/f noise which comes from the DC bias circuitry.

PDBD is also a majority carrier rectifying device which has weaker temperature-dependance performance compared to SBD. Zero-bias detection can be realized in both SBD [16] and PDBDs [17] by controlling the barrier height. However, as for the SBDs, this approach still needs further investigations to be applied for different material systems. Experiments have demonstrated that PDBDs are difficult to produce in large numbers required for arrays at reasonable costs primarily due to control of the doping and the need for sophisticated technology for mesa construction [18].

As an alternative to SBDs and PDBDs, Esaki tunnel diode is more robust against temperature variation and has exhibited high sensitivity. Furthermore, high operational frequencies are possible due to intrinsically high speed of tunnelling process. One type of tunnel diodes (modified from Esaki diode), known as backward diode with a Sb-based heterostructure, has exhibited superior performance with high sensitivity, high cut-off frequency, low noise and desired temperature dependance compared to GaAs PDB diodes[19],[20][21]. These diodes exhibit high curvature coefficient in the I-V characteristics near zero-bias that enables rectification without bias. The underlying physics of the Esaki diodes and backward diodes will be explained in more details in chapter 2.
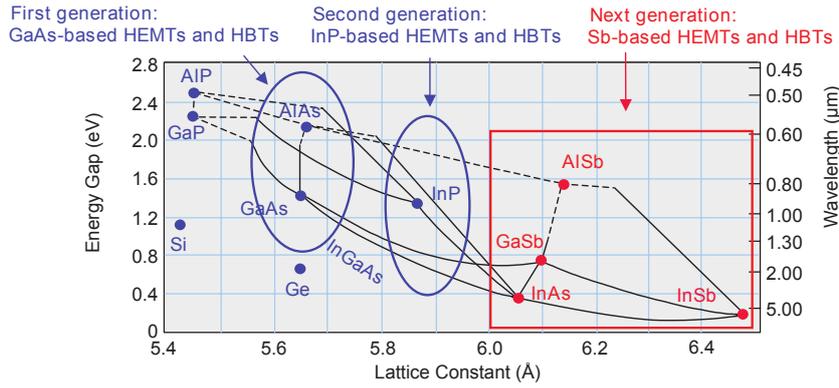
Figure 1.6: *The graph of energy gap versus lattice constant illustrating the transistor technology moving towards materials with higher lattice constant and smaller bandgaps [22].*

1.3 Sb-Heterostructure Backward Diodes

AlSb, GaSb, InSb and InAs have been the material system choice for high-speed and low-power electronic device applications such as high electron mobility transistors (HEMT), heterojunction bipolar transistors (HBT) and resonant tunnelling diodes (RTD) [22]. It has been predicted that Sb-based materials will be the most promising candidates to the next generation of HEMTs and HBTs, see Figure 1.6. Another application of the 6.1 Å material system (AlSb, GaSb, InAs) is a type of MMW detector known as Sb-heterostructure backward diode (Sb-HBD). Heterojunctions depending on their band-alignments are classified into three types, see Figure 1.7. As shown in Figure 1.8, Sb-HBD encompasses all the three possible band-alignments. Due to the broken-gap band-alignment between GaSb and InAs, the inter-band tunnelling current dominates the device current. The obtained current (Zener tunnelling through bandgap) from this band line up is so large that intrinsic AlSb layer (same as tunnel barrier in PDB diodes) is added to control it.

Recent Sb-HBD developments have exhibited a record-high curvature coefficient of -47 V^{-1} and unmatched sensitivity of 4600 V/W which is measured at 94 GHz [6]. Furthermore, a record low NEP_{min} of 0.18 $pW/Hz^{1/2}$ is also reported, which challenges other RT detectors operating in MMW region. The working principle of the Sb-HBD will be discussed in more details in section 2.3.2.
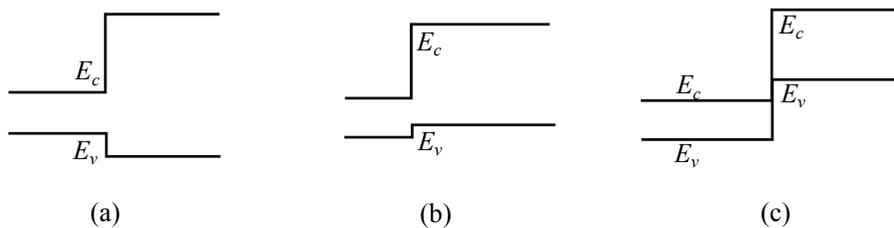
Figure 1.7: *The three different band bendings of heterojunctions. (a) The straddling or type-I, (b) staggered or type-II and (c) broken-gap or type-III heterojunctions [15].*
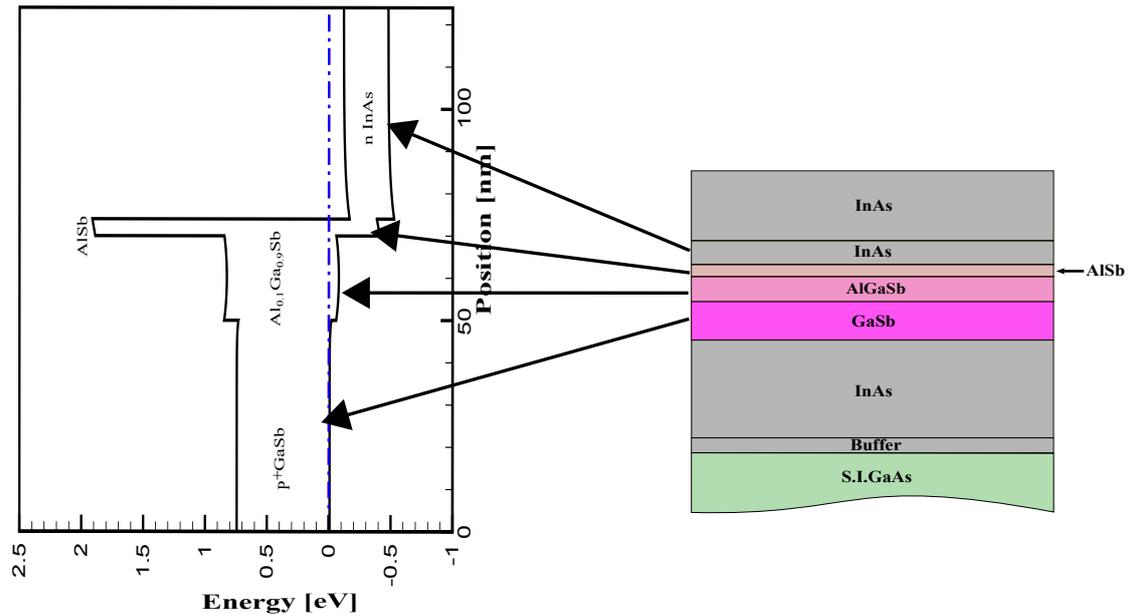
Figure 1.8: *Schematic of the band diagram corresponding to the material structure of a typical Sb-HBD.*

1.4 Outline for This Thesis

The rest of this thesis is divided into four chapters. Chapter 2 provides a broad overview of the theoretical aspects of this thesis. In this chapter, firstly, the quantum mechanical tunnelling is briefly explained. Then the calculations of the tunnelling probability and the corresponding approximation methods are presented. Later on, the background and the underlying physics of both Esaki diode and backward diode is discussed. The state-of-the-art backward diodes are reviewed. Continuously, the theory behind manipulating different parameters in the Sb-HBDs is explained, followed by introducing the important figure of merits in these types of detectors. Chapter 3, represents the introduction to Synopsis TCAD and the device modelling and later on the simulation results are discussed. Chapter 4, summarizes the impact of material quality and tunnelling interface bonding types on device performance. In this chapter, the measurement data from test diodes is presented. The last chapter 5 deals with the experimental approach towards the fabrication of Sb-HBDs both in micron and sub-micron scale. At the end of this chapter, the realized fabrication process challenges are described. Finally, chapter 6 presents the conclusion remarks and the future work ideas.

2 Theory

2.1 Quantum Mechanical Tunnelling

In the classical sense, consider a traveling particle, such as an electron with energy E_0. The electron can pass through a potential barrier (U_0) when its kinetic energy exceeds the height of the barrier i.e. $E_0 > U_0$, which is called thermionic-emission. Conversely, when $E_0 < U_0$, the electron is confined by the barrier walls. Quantum mechanically, however, the wave-particle duality changes the particle-picture of the electrons to a wave-picture. This "wave" nature of the electrons is known as wavefunction ψ, which is the solution to Schrödinger equation. The wavefunction associated with the particle represents the probability amplitude for finding the electron at a given point in space at a given time.

For the barrier with infinite walls, ψ is forced to zero at walls, due to the boundary conditions. As a result, in this case, wavefunctions are obtained rather easily. For a potential barrier with finite height, the ψ is not forced to zero [15]. Instead, the $\frac{d\psi}{dx}$ is continuous at the boundaries of the barrier. In other words, quantum mechanical tunnelling is bound to the uncertainty principle. If the barrier thickness is thin enough compared to the particle's Block wavelength, not only is there a chance for the electron's wave function to exist in the barrier, but also is there a finite probability for it to penetrate through the barrier (without having the energy to surmount it) and emerge on the other side, see Figure 2.9. This penetration through a barrier with finite height is known as quantum mechanical tunnelling.

When the particle reaches the barrier, it must satisfy the schrödinger equation with boundary condition mentioned above. Time independent schrödinger wave equation in one dimension is:

$$\frac{-h^2}{2m}\frac{\partial^2\Psi(x)}{\partial x^2} = (E_0 - U)\Psi(x) \tag{2.1}$$

The solution to this equation demonstrates an exponentially decaying wave function inside the barrier. This concept is the basics of tunnelling probability and tunnelling current. The tunnelling phenomenon is a majority-carrier effect [15] and the transition time through the barrier is remarkably short which is not governed by conventional transit time concept. These characteristics have enabled the tunnelling diodes to operate in the millimetre-wave region. The quantum tunnelling concept was first applied by Esaki in his classic paper in 1958 [23], where he explained the anomalous I-V characteristics in the forward bias.

2.1.1 Tunnelling Probability

Tunnelling through a barrier created in homojunctions with high doping levels (typical Esaki diode) is illustrated in Figure 2.10a. The depletion region in these types of diodes with high doping levels is substantially narrower than a p-n junction's.
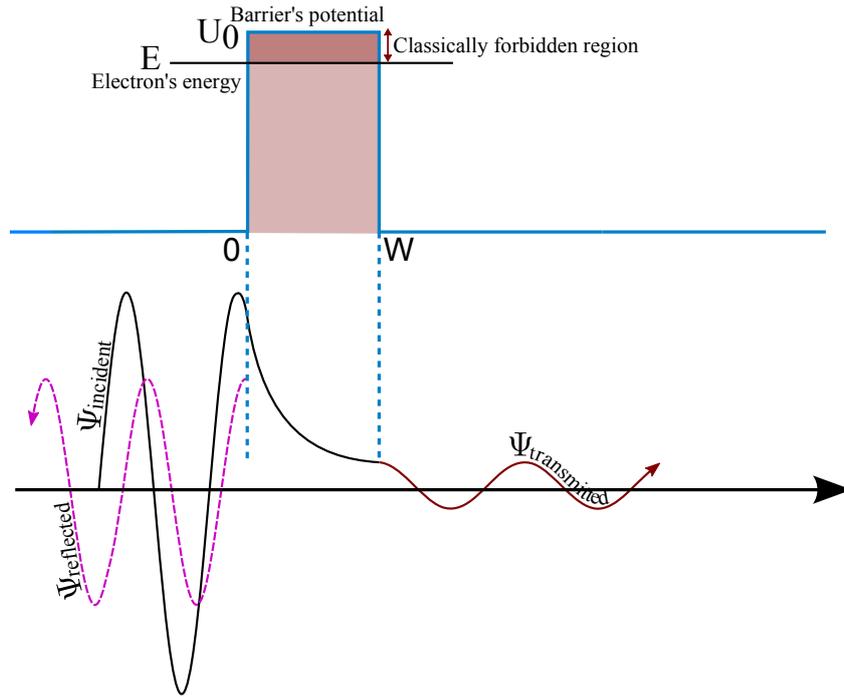
Figure 2.9: *Schematic of wavefunctions (Ψ) of an electron with energy (E) through a rectangular potential barrier (U_0 barrier height). The incident wave ($\Psi_{incident}$), reflected wave ($\Psi_{reflected}$) and the transmitted wave (Ψ_{exit}) are illustrated.*

The energy barrier created looks like a triangle, as shown in Figure 2.10b. In this case, the energy of the incoming electron is equal to the bottom of the energy gap, and the variation of the conduction-band edge can be expressed in terms of the electric field $\mathscr{E}$.
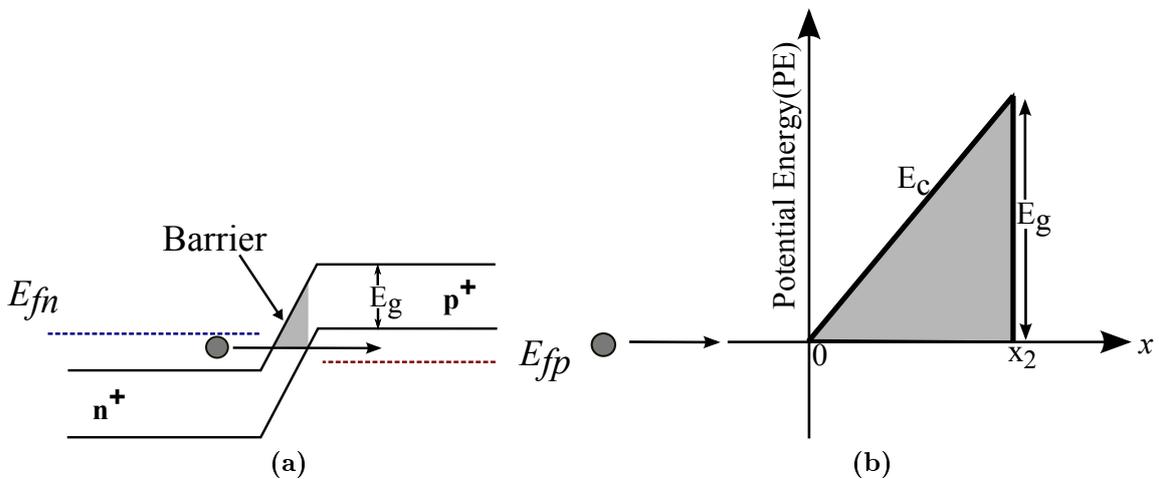
Figure 2.10: *Tunnelling through bandgap in a typical tunnel diode (a). The tunnelling barrier resembles a triangle which it's maximum height is the bandgap (b) [15].*

Resonant tunnelling diodes and heterostructure backward diodes have a discontinuity in band diagram due to different material systems with different bandgaps. This discontinuity can be modeled with a rectangular potential barrier as shown in Figure 2.9.

The time independent Schrödinger equation can also be written in the form of Equation 2.2. For simple rectangular potential barrier (with constant height U), the wavefunction has a general form of Equation 2.4 which is indicated as simple plane waves.

$$\frac{\partial^2 \Psi}{\partial x^2} + \frac{2m^*}{\hbar^2}[E_0 - U]\Psi = 0 \tag{2.2}$$

$$k = \sqrt{2m^*(E - U_0)}/\hbar \tag{2.3}$$

$$\Psi(x) = Ae^{\pm ikx} \tag{2.4}$$

When tunnelling occurs, $E < U_0$, according to Equation 2.3, k becomes imaginary. The related tunnelling probability obtained from the Schrödinger equation is:

$$T_t = \frac{|\psi_B|^2}{|\psi_A|^2} = \left[1 + \frac{U_0^2 sinh^2(|k|W)}{4E(U_0 - E))}\right]^{-1}$$

$$\approx \frac{16E(U_0 - E)}{U_0^2} \exp\left(-2\sqrt{\frac{2m^*(U_0 - E)}{\hbar^2}}W\right) \tag{2.5}$$

A technique to obtain approximate solutions to the time-independent Schrödinger equation is the Wentzel-Kramers-Brillouin (WKB) method. Suppose that the potential is not constant unlike the Figure 2.9, but it changes slowly with x in comparison with λ ($k = \frac{2\pi}{\lambda}$), then k becomes:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(E - U(x)}\tag{2.6}$$

And the solution is:

$$\Psi(x) = Ae^{i\phi(x)} \tag{2.7}$$

$$\Phi(x) = xk(x) \tag{2.8}$$

Now the solution is still practically exponential, except that k(x) is a slowly varying function of x. This approximation is the most commonly used method for calculating the tunnelling probabilities when the potential barrier ($U(x)$) doesn't vary rapidly. Although it has been shown that there are ways to modify this method to be applicable for higher dimensions, here the focus is on using WKB method for one-dimensional simulations.

Substituting $\Psi(x) = Ae^{i\phi(x)}$ into the Equation 2.2 gives:

$$i\frac{\partial^2 \phi}{\partial x^2} - (\frac{\partial \phi}{\partial x})^2 + (k(x))^2 = 0 \tag{2.9}$$

By assuming that k(x) is a slowly varying function of x, $\phi(x)$ also becomes slowly varying function of x. With this assumption, the second derivative of the $\phi(x)$ becomes negligible. By putting $\frac{\partial^2 \phi}{\partial x^2} \approx 0$, the Equation 2.9 becomes:

$$(\frac{\partial \phi}{\partial x})^2 = (k(x))^2 \tag{2.10}$$

$$\phi_0(x) = \pm \int k(x)dx + C \tag{2.11}$$

$$\Psi_0(x) = e^{\pm \int k(x)dx + C} \tag{2.12}$$

This is the 0th order approximation[24]. The first order approximation is thoroughly explained in Quantum Mechanics by Merzbacher[24]. Merzbacher explains that this approximation only holds when "the change of momentum over a wavelength is small compared to the momentum itself". This condition breaks down at classical turning points when $U(x) = E$. Either a more accurate solution is used in these points or special treatments in WKB approximation is needed. The tunnelling probability (T_t) which is also known as transmission amplitude can be calculated by WKB approximation as follows[25]:

$$T_t \approx \exp\left[-2 \int_0^{x_2} |k(x)dx|\right] \tag{2.13}$$

Where $|k(x)|$, Equation 2.6, is the absolute value of the wave vector of the carrier inside the barrier and $x = 0$ and $x = x_2$ are the barrier boundaries.

It is interesting to see that, for the homojunctions with triangular barrier (Figure 2.10), by using equation 2.13 and substituting $E_c = -q\mathscr{E}_x$ and also $x_2 = E_g/q\mathscr{E}$ (triangular barrier with uniform field), the following equation is yielded:

$$T_t \approx \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar}\right) \tag{2.14}$$

The tunnelling current can be calculated with the known tunnelling probability (T_t) multiplied by the product of number of filled states in region A (N_A) with the number of empty states in region B (N_B):

$$J_t = \frac{qm^*}{2\pi^2\hbar^3} \int F_A N_A T_t (1 - F_B) N_B dE \tag{2.15}$$

According to the result, it is clear that in order to obtain large tunnelling probability, both effective mass and bandgap should be small (see equation 2.14)while the electric field should be large. In conclusion, the conditions for tunnelling to happen are: (1)filled energy states on the side which electrons tunnel; (2) empty states exist at same energy level on the side to which electrons tunnel to; (3)the tunnelling potential barrier is thin enough and its height is low that there is a finite probability; and (4) the momentum is conserved within the tunnelling process[15].

2.2 Esaki Tunnelling Diodes

In early 1950, there was particular interest directed towards different types of break-down mechanisms in reversed biased p-n junctions. Zener breakdown was postu-lated as a breakdown mechanism in reverse biased heavily doped p-n junctions in which tunnelling occurs from the valence band in p^+ side to the conduction band in n^+ type region. Investigations showed that the breakdown voltage decreases when the impurity density of one side of the p-n junction increases to the order of 10^{17} cm^{-3}. Based on these findings, Esaki experimented higher dopings on one side in the order of 10^{18} cm^{-3} and observed the breakdown voltage less than 1 V. In this case, the current in the reverse bias was also more than the forward bias which be-came the basic idea of the backward diodes operation. Esaki's further experiments on applying high doping levels on both sides led to tunnelling currents at very low forward bias voltage and a unique negative differential resistance behavior: To honor this discovery, this tunnelling diode is referred to as the Esaki diode.

Consider a simple p-n junction (typical Esaki diode) where both regions are highly doped (degenerately doped $> 10^{19}$ cm^{-3}). If the doping on both sides is such that the fermi level lies within the allowed bands on one hand, and the barrier of the depletion layer is thin enough on the other hand, there would be a probability for the particles on the side with filled states to tunnel to the side with empty states, see Figure 2.11. Typically the width of the depletion region in these diodes is of the order of 10 nm or less. The tunnelling process can happen in both di-rect and indirect bandgap semiconductors. In direct tunnelling, both conduction band minimum and valence band maximum have the same momentum. While, the difference between valence band maximum and conduction band minimum momen-tum through indirect tunnelling can be compensated by phonons or impurities by applying a very large voltage.

According to the Figure 2.11, in a typical Esaki diode, with a very small forward bias, the potential barrier is so high that the only noticeable current in the for-ward bias is due to the electrons tunnelling from n-side to p-side(point a in the Figure 2.11). By increasing the forward bias voltage the number of occupied states opposite to the empty states in p-side becomes equal at some point, leading to max-imum tunnelling current (b). As the voltage is increased, the number of electrons opposite to empty states on p-side reduces which indicates an abrupt abatement in tunnelling probability (c). The negative differential resistance is observed at this voltage. At some point, when the conduction band on n-side is in level with valence band on p-side, the tunnelling current drops to zero. By further increasing the voltage, the potential barrier gets smaller, and the normal diffusion current together with the excess current begin to dominate (d). Finally, as for the reverse current (e), the tunnelling from the valence band in p-side to the conduction band in n-side starts with a very small negative voltage.

Based on the explanations above, the static I-V characteristics of an Esaki diode can be assigned to three different current components (Figure 2.12): Band-to-Band tunnelling, excess current, and thermionic emission current. Ideally, when the con-
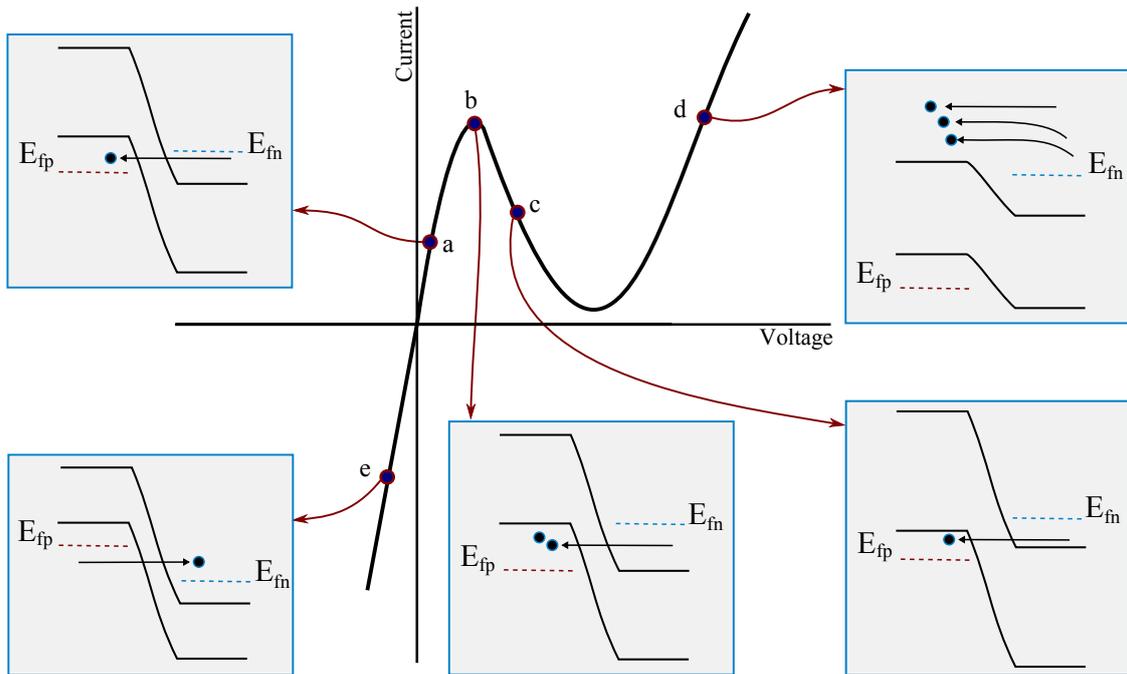
Figure 2.11: *The I-V characteristics of a typical tunnel diode (Esaki diode) with the description of regions through band diagram schematics.*

duction band of n-side overlaps the valence band of p-side, the tunnelling current in a single energy conserving transition should be impossible. Practically, the actual current is considerable in excess of the normal diode current; hence the term excess current[26]. The mechanism of excess current is through tunnelling of carriers by way of local energy levels (impurity states) within the forbidden bandgap. Chynowth quantitatively explained the dependance of exponential excess current on doping and bombardment damage [26]. Figure 2.13 illustrates different possible tunnelling routes for the electron.

According to Meyerhofer [27], hump current is the second type of excess current, that is characterized by the structure in the I-V curve beyond the current minimum. The shape is strongly dependent on the temperature. If there is no intentionally added impurities or defects, the diode does not exhibit hump currents.

The third component of seemingly excess current is the valley current [27], see Figure 2.12. It was clearly observed in junctions that have a well-defined exponential excess current component. This current is calculated by extrapolating the exponential excess current to lower voltages and subtracting it from I-V characteristic. The valley excess current is nearly temperature-independent. In heavily doped junctions, the valley current increases faster than the exponential excess current and the latter may disappear almost entirely.
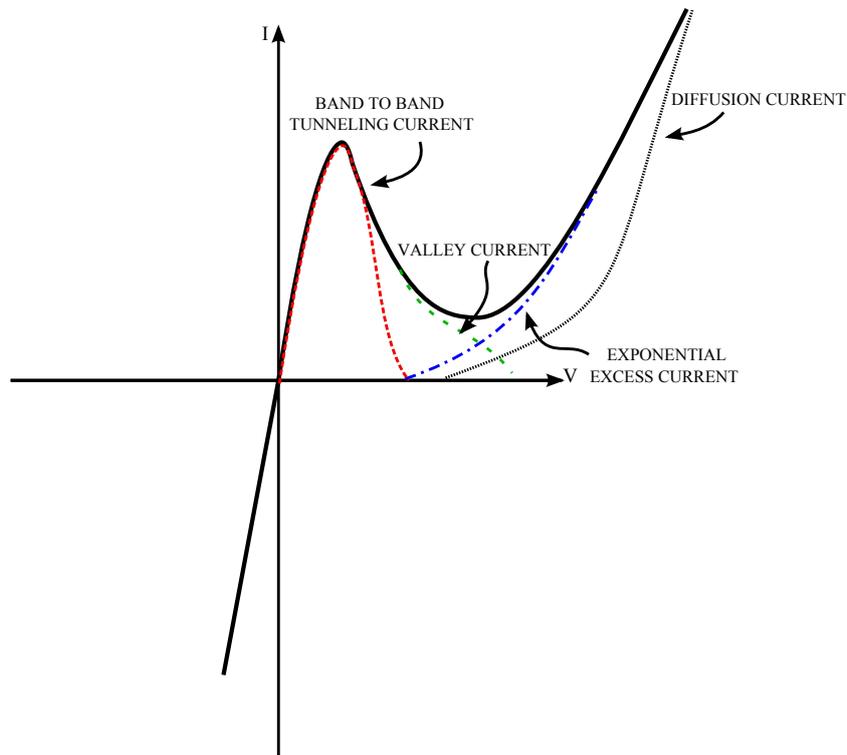
Figure 2.12: *The static I-V characteristics of tunnel diode consists of three main components: Band to band tunnelling current, excess current, diffusion current [15].*
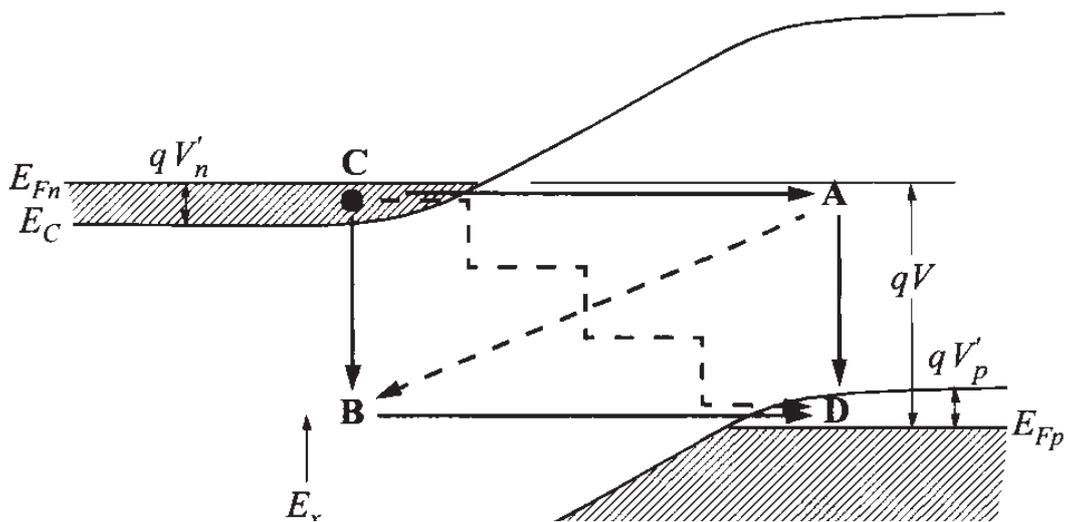

Figure 2.13: *The mechanisms of tunnelling via local states in forbidden bandgap. The resulting current is known as excess current [26].*

2.3   Backward Diodes

Tunnel diodes such as RTD, esaki diode and backward diode, benefit from the advantages of quantum effect devices such as RT operation, high switching speed and low power consumption. Extremely high sensitivity is obtained in Esaki diode, when biased near peak current. Unfortunately, this high sensitivity is followed by high capacitance, limited dynamic range and the need for a stable bias circuitry.

Homojunction backward diode has the same operational principle as the Esaki diode, but the doping concentration either on the p-side or on the n-side is not quite degenerate (not as highly doped as the other side). This slight difference makes the bands to align in such a way that in thermal equilibrium, the fermi level is close to band edges. Consequently, the backward current is larger than the forward current with a small bias. For a backward diode, the purpose is to reduce the forward tunnelling current compared to high levels in Esaki tunnelling diode to such levels that, either negative resistance does not happen anymore or it is so high that can be neglected. The difference between typical tunnel diode and backward diode is depicted in Figure 2.14.

As shown in the Figure 2.14, the shape of the backward diode's I-V curve is most suitable for zero-bias rectification, due to extreme nonlinearity at the origin. Another advantage of backward diode is low impedance due to tunnelling current which leads to higher bandwidth and simplifies the matching.
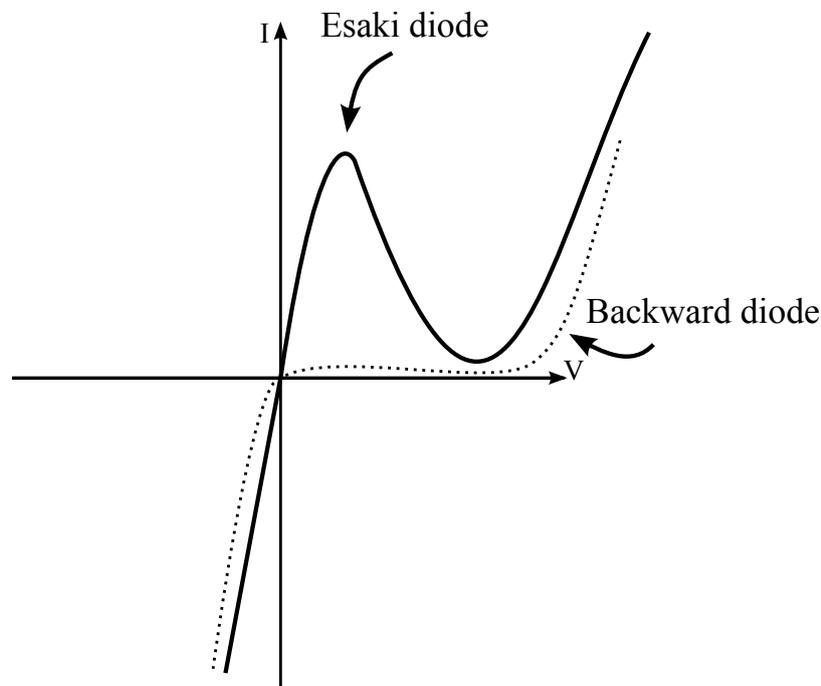
Figure 2.14: *The I-V characteristics of a backward diode and a typical tunnel diode [15].*

A backward diode is used as a square-law detector in direct detection. At low voltages the diode operates in the square-law regime. In this regime, the output voltage is proportional to the square of the input voltage. In other words, when a high frequency AC signal is applied across the diode, it will be "rectified" and the output dc voltage will be proportional to the incident RF power. Consequently, one of the most prominent figure of merits of high-speed switching devices is the curvature coefficient which is mainly used to evaluate the detector sensitivity performance. Ultimately, the voltage or current sensitivity is directly proportional to this value through a constant which is related to the detector embedding impedances and matching networks. The definition of the curvature coefficient is:

$$\gamma \equiv \frac{\frac{d^2 I}{dV^2}}{\frac{dI}{dV}} \tag{2.16}$$

The value of curvature coefficient (γ) is the measure of nonlinearity normalized to admittance level. For SBDs and p-n junctions this value is calculated by q/nkT [15] which reveals the temperature-dependance performance of Schottky diode. However, the γ value of backward diodes can be obtained from the relationship between tunnelling current and bias voltage as[15]:

$$\gamma(V = 0) = \frac{4}{V_n' + V_p'} + \frac{2}{\hbar}\sqrt{\frac{2\varepsilon_s m^*(N_A + N_D)}{N_A N_D}} \tag{2.17}$$

According to Equation 2.17, the γ value is dependent on effective masses of the carriers (m^*), permittivity and impurity concentrations (N_A and N_D), which are not strong functions of temperature. This implies that the curvature coefficient in backward diodes is relatively insensitive to temperature variation unlike in Schottky diodes.

Depending on the material system selection, backward diodes operation frequency ranges from microwave frequencies to millimetre-waves. By a proper selection of material system and the structure, optimum performance in terms of band width, sensitivity and NEP can be achieved.

2.3.1 Material System Selection and State-Of-The Art Backward Diodes

Generally, a wide range of materials can be used for backward diodes. Germanium, silicon, indium arsenide, silicon carbide and other alloyed materials from III-V family has been reported to be the main materials in backward diodes [28–30]. The range of material selection can be narrowed down depending on the application. For instance, materials such as SiC with high bandgap and large effective mass operate only up till 1 GHz [29]. Large capacitance is a serious problem for wide bandgap materials because of creating an extremely narrow tunnelling junction. Smaller area devices might be a solution for high frequency operation of these materials, but they might be fragile and susceptible to burnout at low power levels [28]. However, this wide bandgap is advantageous for high temperature, high power and
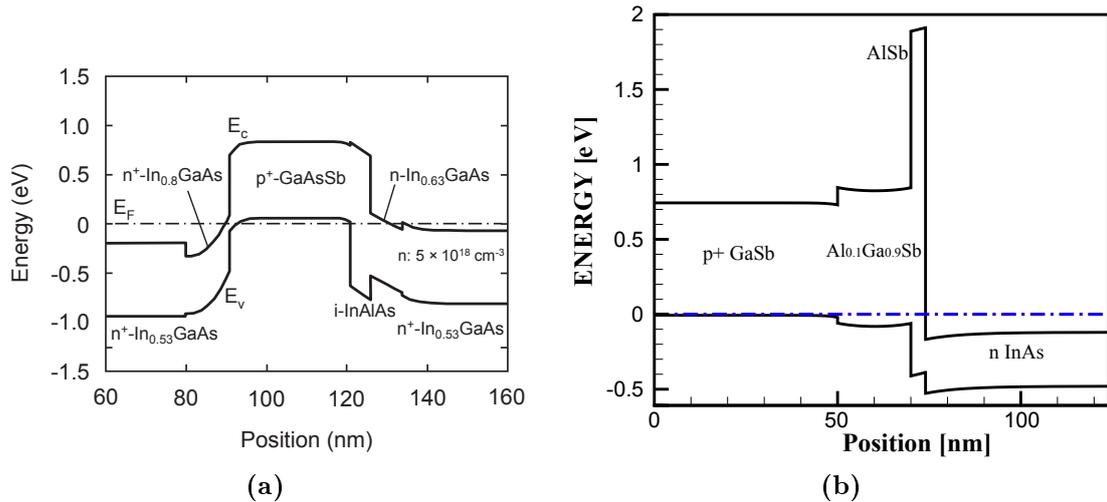
Figure 2.15: *The band diagram of Sb-heterostructure backward diode(a), and the band diagram of GaAsSb-based backward diode(b).*

high radiation operation of the device as it suppresses thermally generated current.

Homojunction backward diode with Ge with measured sensitivity of as high as 70 V^{-1} [31] and high current densities, have been a frequent choice. However, their performance is limited to few tens of gigahertz and reproducibility is a challenge [32]. As an alternative, in order to operate beyond frequency limitations of materials such as Ge, asymmetric tunnelling mechanisms can be investigated.

Heterostructure based backward diodes are more advantageous over homojunction backward diodes as they offer additional degrees of freedom such as bandgap engineering plus tailoring doping profiles.

In order to permit the operation of the backward diodes well into the millimetre-wave region, semiconductors with small effective mass and bandgap, high tunnelling probability and small junction area (small capacitance per unit area) are preferred. A study of optimum material for microwave backward diodes was carried out [28]. This research concludes that good microwave backward diodes can be produced with expecting significant improvements in sensitivity and reliability with InAs leading to larger junctions compared to the ones fabricated with germanium [28].

The two most important reported heterostructure backward diodes are: p-GaAsSb/i-InAlAs/n-InxGaAs which are lattice-matched to InP (Figure 2.15a) and n-InAs/i-AlSb/p-GaAlSb/p-GaSb which is metamorphically grown on semi-insulating GaAs substrate by molecular beam epitaxy (MBE) (Figure 2.15b).

GaAsSb-based backward diodes were proven to be highly sensitive under zero-bias operation with unmatched sensitivity of 1495 V/W with a diode mesa diameter of 2.0 μm at 94 GHz [33]. The possibility of easy integration with InP-based high

electron mobility transistors as high performance low noise amplifiers makes them very attractive for millimetre-wave detection.

In case of the latter, several attempts have been made to improve the performance of Sb-heterostructure backward diodes (InAs/AlSb/(Al)GaSb)[34–42]. The state-of-the-art figure of merits of these diodes such as NEP and the sensitivity is mentioned in the introduction chapter.

2.3.2 Sb-Heterostructure Backward Diode

The first attempt to analyze the GaSb-AlSb-InAs system's I-V behavior was done by Takaoka et al [43]. He states that according to the energy diagram of the GaSb-AlSb-InAs (with no intentional doping for GaSb and InAs) junction (Figure 2.16a), at low bias voltages the forward bias current is smaller than the reverse direction's current. He also describes that in high bias voltages (not high enough for thermionic emission), where the InAs conduction band minimum becomes higher than GaSb valence band edge, this tunnelling current is blocked. However, according to the Figure 2.16b, there is a tunnelling current of Fowler-Nordheim type that the electrons tunnel from AlSb's valence band to empty portions of GaSb's valence band in forward bias. The second attempt was to demonstrate the negative differential resistance in this system by Luo et al [44].

Later on, J. N. Schulman and D. H. Chow [45], set the goal on further minimizing the current in forward direction. The investigated backward diode consists of n-InAs/i-AlSb/i-GaAlSb/p-GaSb. Tunnelling current is across the bandgap and through the depletion region. The concept of using staggered InAs/GaSb band line up is to produce the condition for high tunnelling current as well as reaching a large I-V curve nonlinearity.

The doping concentrations should be such that, the fermi level lies closely above n-InAs conduction band and closely below the valence band in p-GaSb(Figure 2.16). With this band alignment in forward bias, there will be very few empty states in valence band of p-GaSb leading to very small tunnelling current of filled states in n-InAs. Additionally, by employing thick intrinsic layer of AlGaSb, forward current is further blocked by AlGaSb bandgap, see Figure 2.15b. In other words, if the fermi level is close or above AlGaSb valence band edge so there will not be enough holes for InAs electrons to tunnel. However, the reverse bias tunnelling current is larger due to AlGaSb valence band electrons moving in a monotonically increasing manner through the tunnel barrier into n-InAs conduction band.

Generally in tunnel diodes, by increasing the doping concentrations, the electric field increases and the depletion region width decrease that will enhance the tunnelling in both directions. Conversely, in the backward diode [35], by increasing the N_D the backward current decreases. The reason is that the tunnelling is through the AlSb barrier, and a barrier is less affected by the electric field as compared to a depletion region. Moreover, the enhancement in InAs electron concentration may perform as blocking the electrons tunnelling from AlGaSb leading to decrease in backward tunnelling current. Additionally, the backward tunnelling current is exponentially proportional to barrier thickness (see equation 2.5). By increasing Al compositions, the energy overlap between the anode and cathode decreases, thus larger nonlinearity is obtained. However, it should be noted, that the selection of percentage of the Al is critical. Since, even not very high fraction of Al (e.g. 20 percent) lowers AlGaSb's valence band too much relative to the fermi level of InAs, which leads to reduction of current both in forward and backward direction [35].
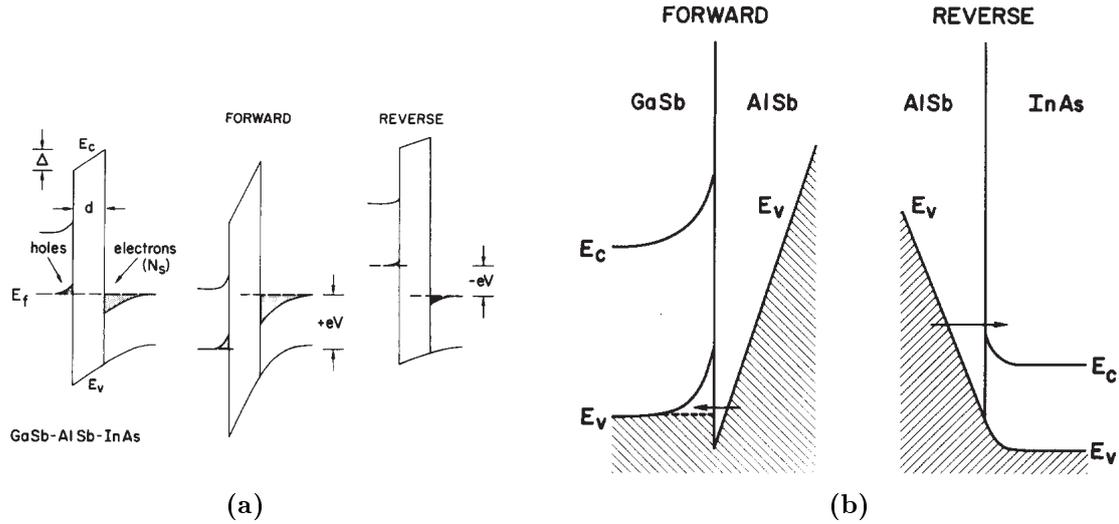
Figure 2.16: *(a) Schematic band diagram of GaSb-AlSb-InAs junction at zero and low forward and reverse bias voltages, (b) The tunnelling current indicated by arrows in high bias voltages[43].*

2.3.3 Figure of Merits

The most important figures of merits which evaluate the performance of the zero-bias direct detectors are; sensitivity, cut-off frequency, and noise equivalent power (NEP). The equivalent circuit model for the diode and the probe pad is illustrated in Figure 2.17.

Junction resistance (R_J), is an important factor for determining the voltage sensitivity and the frequency response. R_s is the series resistance which together with junction capacitance C_j, defines the cut-off frequency (f_c).

$$R_J = \frac{dV}{dI} \tag{2.18}$$

$$f_c = \frac{1}{2\pi R_s C_j} \tag{2.19}$$

Curvature coefficient described in Equation 2.16 can also be defined as:

$$\gamma = R_J \frac{d^2I}{dV^2} \tag{2.20}$$
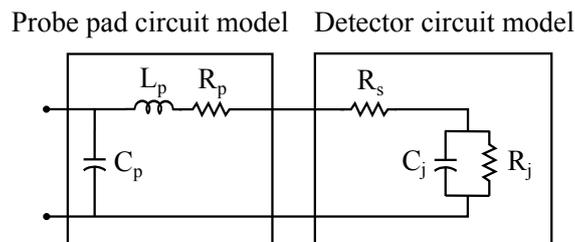
Figure 2.17: *The equivalent circuit of a typical Sb-HBD and the probe pad [36].*

Reducing the area of the device, increases the junction resistance and the series resistance (for very small areas junction resistance increases dramatically)[35]. Obviously, in order to reach to high frequency operation, the parasitics should be reduced, specially the series resistance. A fairly thick InAs contact layer with high electron mobility was chosen [36] to reduce the lateral access resistance, and thus the series resistance is minimized. The band alignment (type II staggered) between this thick InAs in anode side and GaSb prepares a low-resistance contact without the need for ohmic contact directly to p-type GaSb [39]. Furthermore, vertical scaling of the device affects both junction resistance and junction capacitance. Another factor that affects the junction resistance is the tunnel barrier thickness. R_J increases exponentially with the barrier thickness is already discussed in section 2.1.

In contrast, the thinning of the tunnel barrier increases the C_j which deteriorates the cut-off frequency and makes the wide band matching difficult. Junction capacitance is found to be dependant on device area (lateral scaling), bias voltage and the ambient temperature. Junction capacitance increases insignificantly with bias voltage and decreases approximately linearly by reducing the device area [36].

Another factor that can impact the junction capacitance is using a p-type δ-doped layer in cathode [36]. The concept is that, on one hand, this layer increases the space charge region width (i.e. separates the charge centroids) which leads to reducing the junction capacitance. On the other hand, the δ-doped layer reduces the electron concentration in InAs layer. This means that the δ-doped layer brings the fermi level close to InAs conduction band which reduces forward tunnelling current more intensely than backward current leading to increased nonlinearity hence increased curvature [34, 36].

Voltage sensitivity β_v as another important figure of merit of HBDs, can be obtained from the detector current voltage characteristics at low frequencies. The detectors voltage sensitivity is approximated by $\beta_v \approx 2Z_s\gamma_{IV}$, where $Z_s = 50\ \Omega$ is the source impedance.

The zero-bias Johnson-noise limited NEP[46] can be expressed as:

$$NEP = \frac{\sqrt{4KTR_J}}{\beta_v} \qquad (2.21)$$

NEP is the most relevant figure of merit of detectors, since it takes into account the opposing effects of junction resistance on both sensitivity and noise performance.

It can be concluded that, reducing the device lateral scale, increases the junction resistance which leads to degrading the noise performance. Simultaneously, the junction capacitance decreases which improves the cut-off frequency. It should be noted that, improving only one of the figure of merits might lead to unacceptable performance of the device. According to the previous discussions, the optimisation of the device should be based on overall consideration of figure of merits and specified application.

3 Simulations

3.1 Introduction to Synopsis TCAD

3.1.1 Overview

Part of this work presents numerical simulation of the current-voltage (I-V) characteristics of Sb-HBDs. Physical device simulation can both give great insight into the detailed operation of the device and predict the characteristics of novel devices within the limitations of information available on semiconductor material properties. Synopsys TCAD encompasses comprehensive suit of products including process and device simulation tools that paves the road for developing and optimizing semiconductor processing technologies and devices. Herein, different numerical tunneling models implemented in Synopsys TCAD simulator, Sentaurus Device, are discussed and the most appropriate one is chosen to model Sb-HBDs.
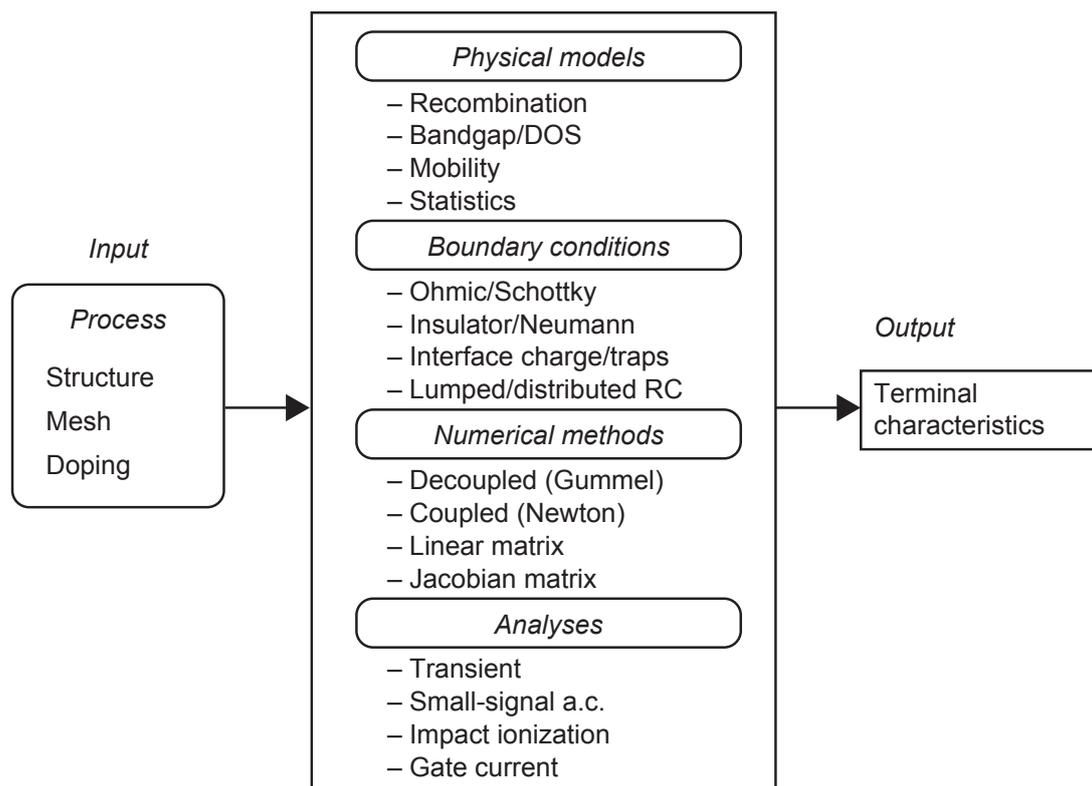
Figure 3.18: *Sentaurus device editor's command file consists of physical models, boundary conditions, numerical methods and analyses[47].*

3.1.2 Device Simulation

Synopsis TCAD is employed to study the electrical behavior of virtually designed devices. Some features of Sentaurus device simulation tool are depicted in Figure 3.18. Geometric structures are designed in either process simulator or 2-D/3-D Sentaurus structure editor. The grid file includes the description of the various regions regarding doping concentrations, the location of electrical contacts and mesh definitions. The purpose of meshing of the device is to create the nodes at different regions for electrical measurement. In regions of both high current density and electric field or the regions where quantum mechanics is the dominating concept, denser mesh is required to obtain accurate results close to experiment. The grid file can be obtained by either extracting the commands from Sentaurus Structure Editor's GUI (Graphical User Interface) environment or by writing the commands in the grid file from the very beginning.

The parameter file which includes the semiconductor physical models and parameters combined with the command file are the two input files for the device simulator. As a result, the analysis (dc, ac analysis, noise, transient and large signal cyclic analysis) on the basis of various transport equations such as drift-diffusion and thermionic emission is done in device simulator. Depending on every device's characteristics, the device simulator command file can contain various physical models, boundary conditions, numerical methods and different types of analyses, see Figure 3.18.

3.2 Establishing the Model

In order to simulate the Sb-HBD accurately, different physical processes beyond the standard drift-diffusion equations should be considered with extra caution. Practically, the tunnelling interface traps (InAs/AlSb surface) and the dislocation density from the growing conditions might prepare the condition for the trap-assisted tunnelling current in forward direction after reaching certain bias voltage. Yet, with near zero-bias operation, only the band to band tunnelling is taken into account as the main contributor in this bias range. Consequently, tunneling models and in the appearance of the hetero-intefaces, thermionic emission in some cases is also taken into account.

The simple transport model, drift-diffusion, is calculated by default in the simulator. In our case, since we assume that carriers are in thermal equilibrium with the lattice, drift-diffusion model rather than the hydrodynamic transport model is selected.

In the absence of magnetic field, the semiconductor device operation is governed by reduced Maxwell's equations:

Poisson's equation
$$-\nabla^2\varphi = \frac{\rho}{\varepsilon} \tag{3.1}$$

Electron continuity equation
$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n - R_n + G_n \qquad (3.2)$$

Hole continuity equation
$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla J_p - R_p + G_p \qquad (3.3)$$

In equation 3.4, φ, ρ, ε represent the electric potential, the total charge density, the dielectric constant, respectively. In equation 3.2, q, n, J_n, R_n/G_n represent the elementary charge, the electron concentration, the electron current density and the electron recombination/generation rate, respectively. In equation 3.3, h, J_p, and R_p, represent the hole concentration, the hole current density, and the hole recombination/generation rate, respectively. In the device simulator, the above equations are solved self-consistently with the coupled or Newton method which are considered as the basic equations [48].

The parameter files specific for some of the materials exist in the Sentaurus structure editor. However, the parameter files for AlSb, GaSb and AlGaSb was created due to the lack of these files in the simulator. Most of these physical parameters of the stated materials was extracted from [49].

AlSb is an indirect bandgap material with Γ valley bandgap of 2.3 $[eV]$ and X valley bandgap of 1.6 $[eV]$. The value chosen for the input of the simulator was the Γ valley bandgap. During the band-to-band tunneling, the transition from Γ valley to X valley can only happen if the X band of AlSb falls below the Fermi level on the InAs side. This would happen in large bias voltages and is not applicable in near zero-bias operation [50].

The bandgap narrowing has pronounce effect on performance of the devices such as HBTs. However, in the case of Sb-HBDs, only the contact layers are heavily doped unlike HBTs and this effect is neglected.

The basic mobility model which is a function of lattice temperature and is called constant mobility model is chosen. However, in some highly doped materials and high field saturations other mobility models can be selected.

In heterostructure bipolar devices such as HBD, the generation and recombination models become more pronounced. Shockley-Read-Hall (doping dependent) and Auger recombination models are applied in the simulator.

Figure 3.19 illustrates different tunneling current mechanisms across a barrier. In Sentaurus device tool, there are three tunneling current models, which simulate the elastic charge-transport processes at contacts or interfaces. The direct tunneling model is restricted to tunneling through insulators. The Fowler-Nordheim model is also a particular case where tunneling is to conduction band of the oxide. The most versatile tunneling current model is nonlocal tunneling model which can be used to simulate tunneling at Schottky contacts, heterostructures and gate leakage through thin, stacked insulators[48].
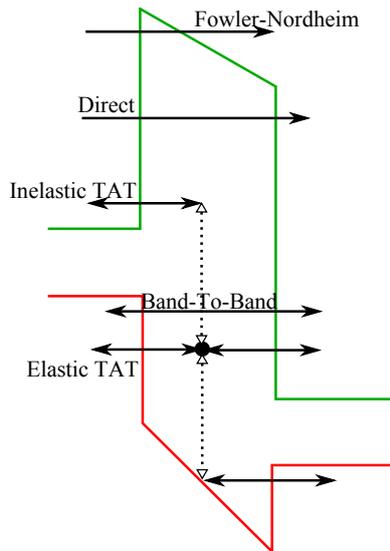
Figure 3.19: *Different tunneling current mechanisms.*

The tunneling phenomenon also plays a role in some generation-recombination models. Most of the generation-recombination models except for trap-assisted model and one of the band-to-band tunneling models do not involve (sometimes in opposition to reality) spatial transport of charge. Based on the charge transfer realization, the tunneling models are divided into two groups; Nonlocal and local tunneling models, see Figure 3.20.

It is vital for a realistic band-to-band tunneling model to meet certain requirements. The two most important characteristics of such a model are as follows. Firstly, the band-to-band tunneling phenomena has a nonlocal nature, where it happens amongst quantities located in different spatial locations. As discussed in the theory part of this thesis, the band-to-band tunneling rate depends both on
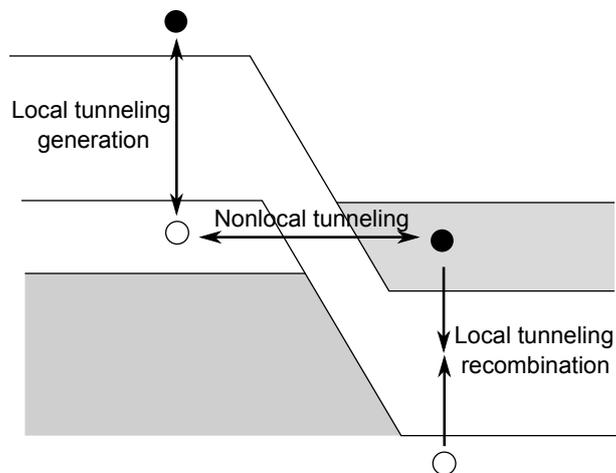
Figure 3.20: *Difference between the spatial behavior of the local and nonlocal tunneling models [51].*

the tunneling probability and the carrier concentration on both sides of the barrier. This implies that, under thermal equilibrium where the quasi-Fermi levels are constant, the tunneling current doesn't happen even if the tunneling probability is high. Secondly, the band-to-band tunneling model should not be highly sensitive to the density of the mesh used in the Sentaurus structure editor for the drift-diffusion solver.

The local tunneling model is a straightforward method to simulate tunnelling diodes, where there is no real carrier transport through barrier. In this model, band-to-band tunneling leads to generation or recombination of the carriers. The recombination/generation rate is calculated at a point, from the electric field value or the gradient of the Fermi potential at that point. This term can be added to the continuity equation to account for band-to-band tunneling current. One simple band-to-band tunneling model in TCAD uses the following expression based on Kane's derivation,

$$G^{b2b} = A.E^{\alpha} exp\left(-\frac{B}{E}\right) \tag{3.4}$$

This approach is unphysical since it doesn't consider the recombination due to tunneling and predicts nonzero rate under thermal equilibrium [48].

Hurkx band to band tunnelling model suggests a correction for this formula which accounts also for the recombination. However, it is still considered as a local model.

Conversely, in the nonlocal tunneling model, there is real spatial carrier transport through barrier. The generation-recombination term added to the continuity equation is derived by integrating over the tunneling path using WKB formula. In this model, the recombination is at different positions while in local tunneling model, electron and hole recombine in the same location, see Figure 3.20.

In the research conducted by Hermle [51], the comparison of local and nonlocal tunneling models was investigated. He concluded that in high peak tunneling currents, in tunnel diodes used in multi-junction solar-cells, there is saturation of the derivative of the IV curve at zero-bias for local tunneling models, see Figure 3.21. These results were in contradiction with measurements data where the IV curve derivative is almost constant near zero-bias. It should be noted that, curvature coefficient in zero-bias is a pivotal figure of merit of zero-bias backward diodes. As a result, among these models (summarized in Table 3.1) the nonlocal tunneling model is more accurate for modeling the zero-bias backward diodes.

There are two types of nonlocal band to band tunneling models implemented in Sentaurus Device; Band-to-band tunneling current model based on nonlocal mesh (node-pair based) and dynamic nonlocal path band-to-band tunneling model (tunnel-path based). In case of the former model, a separate mesh called "nonlocal mesh" in Sentaurus device editor's command file is defined by the user which determines the tunneling path for the carriers. In the latter model, direct band-to-band tunneling ($\Gamma_V - \Gamma_C$ transition) and indirect band to band tunneling generation
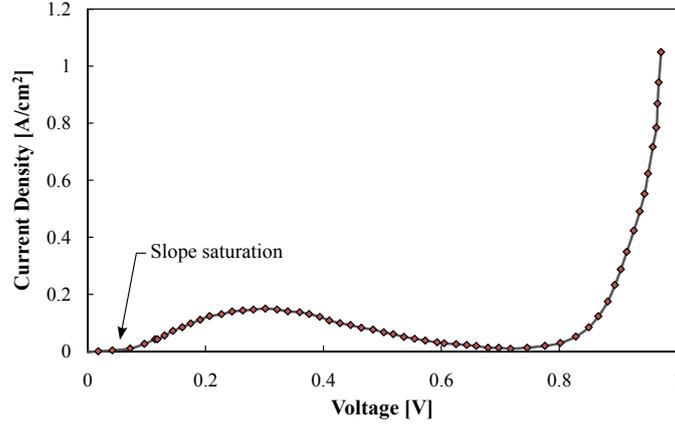
Figure 3.21: *The simulation of the IV curve of GaAs tunnel diode using local tunneling model, resulting in saturation of the IV slope near zero-bias [51].*

rates ($\Gamma_V - X$ and $\Gamma_V - L$ transitions) are calculated using a tunneling path, defined automatically based on energy band profile.

The present model for dynamic nonlocal path band-to-band tunneling is not suitable for AC analysis [48]. Moreover, in such complicated structure as Sb-HBD, it is extremely difficult to find out the correct prefactors. Consequently, in this study, the band to band tunneling current model based on nonlocal mesh is chosen to model the Sb-heterostructure backward diode.

The nonlocal band-to-band tunneling model can be switched on by using eBarrierTunneling or hBarrierTunneling term in the physics part of the command file. The four contributions to the total tunneling current is illustrated in the Figure 3.22.

In order to include the contributions by tunneling from "valence band to the conduction band", to the "conduction band to the conduction band" tunneling term,

Table 3.1: *Summary of existing band-to-band tunnelling current models in TCAD simulator [52].*

| Model	Local model	Nonlocal model, node-pair based, user-defined mesh	Dynamic nonlocal model, user-defined tunnel paths
Approach	Generation of carriers according to local E-field	Search for node pairs satisfying $E_{C,A} < E_{V,B}$. Generate electron and hole at A and B, respectively.	Divide device into strips along the tunnel paths. Sum up contribution from all strips.
Drawbacks	Numerically robust but unphysical	Highly sensitive to the position of mesh node, requires extremely dense meshes. Leads to unphysical results in non-uniform mesh.	Requires the user to specify the tunnel paths explicitly, which are not obvious in advanced devices.
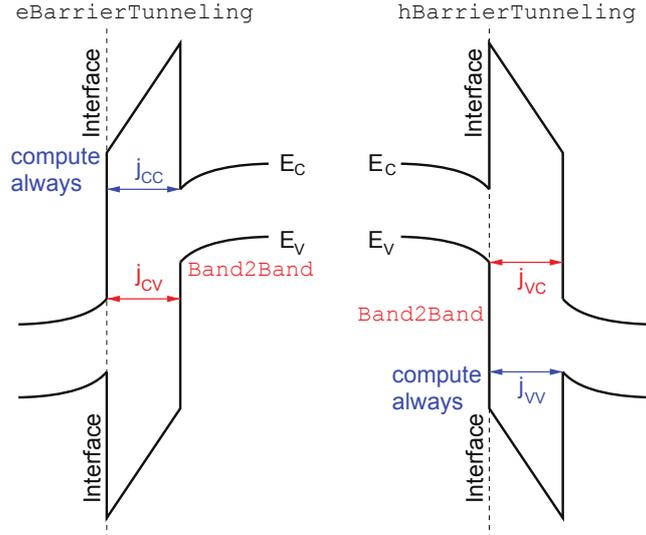
Figure 3.22: *The different nonlocal tunneling current contributions [48].*

the option $Band2Band = Simple$ have to be assigned to eBarrrierTunneling parameter set.

The band diagram of a typical Sb-HBD under forward bias is depicted in Figure 3.23. As can be seen, the band-to-band tunneling generation rate is negative under forward bias. In forward bias, an electron belonging to the conduction band of InAs, tunnels through the AlSb intrinsic layer to the valence band on the $Al_xGa_{1-x}Sb$ and recombines with a hole. This leads to loss of both holes and electrons on n-side and p-side. On the contrary, under reverse bias, an electron belonging to the valence band of the $Al_xGa_{1-x}Sb$ layer tunnels through the barrier to InAs conduction band. This electron leaves behind a hole on the p-side but generates an electron on the n-side which results in positive eBarrierTunneling generation rate.

3.3 Simulation Results

Finding the optimum operating point of the device, depending on the application, requires a deep understanding of the device physics. The first step towards this goal is to find out the effect of every parameter on the performance of the device. Several simulations are executed in Synopsis TCAD, to discover the effects of doping concentration on either sides, the barrier thickness and the mole fraction of Al in AlGaSb on the sensitivity and noise performance of the device. In order to make sure that the simulation results are valid, the model has to be verified. The experimental data for two structures with 3.2 nm and 4 nm barrier thicknesses is collected, and the corresponding models are created. Figure 3.24 illustrates the simulation data versus experimental data for the two structures. One structure has 200 Å of $Al_{0.1}Ga_{0.9}Sb$ and 500 Å of p^+ GaSb (doped $4e10^{18}cm^{-3}$) followed by 500 Å of n-type InAs (doped $7e10^{17}~cm^{-3}$) [53]. Another one has 200 Å of $Al_{0.12}Ga_{0.88}Sb$
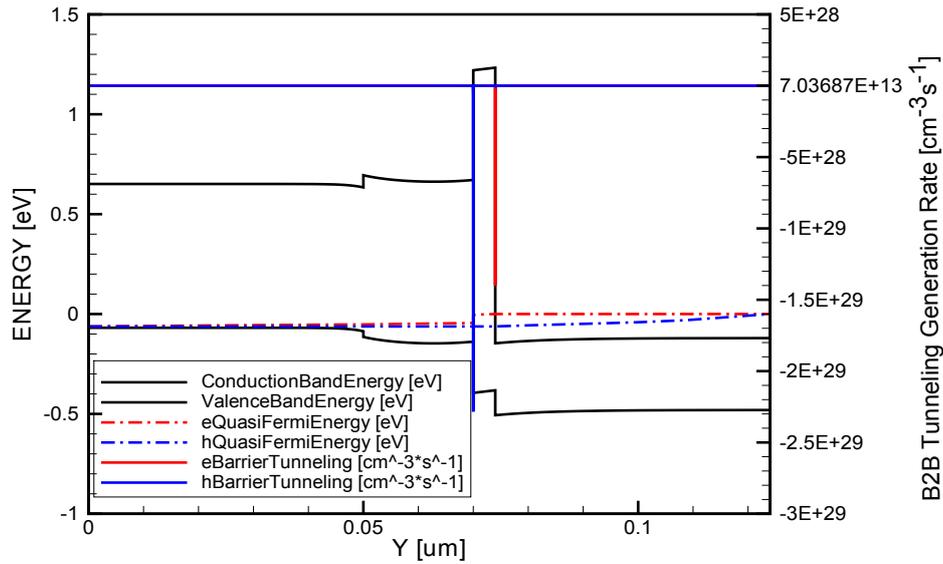
Figure 3.23: *The band diagram of a typical Sb-HBD, showing the band-to-band tunneling generation rate on the right hand side axis.*

and 500 Å of p^+ GaSb (doped $8e10^{18}cm^{-3}$) followed by 500 Å of n-type InAs (doped $4e10^{17}$ cm^{-3}) [36]. In this Figure, the effect of the barrier thickness on the current density is also noticeable.
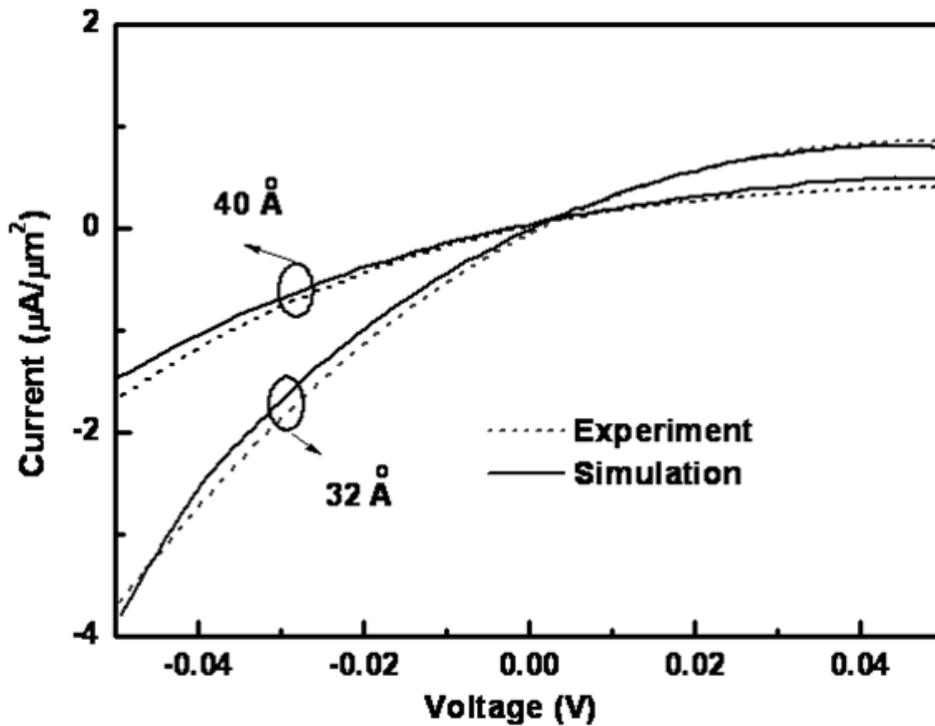
Figure 3.24: *The simulated and experimental results for structures with 4 nm and 3.2 nm barrier thicknesses [36].*

The first parameter variation was done by sweeping barrier thickness in the 3.2 nm structure. As seen in the Figure 3.25, the junction resistance increases almost exponentially by barrier thickness. This is due to the exponential dependance of the tunneling probability through the barrier on the width of the barrier, as it was explained in section 2.1.1.

The InAs doping concentration is another variable that has been investigated. As shown in the Figure 3.26, the smaller the InAs doping concentration, the larger is the values for junction resistance and curvature coefficient. With smaller InAs doping concentration, the Fermi level is closer to the conduction band. Consequently, fewer electrons are available in InAs to tunnel through the barrier, resulting in additional suppression of forward current (nonlinearity enhancement).

The Al mole fraction variation is another way to control the inter-band tunneling current. With more Al mole fraction, the AlGaSb bandgap is larger, which leads to more filtering of the forward current, see Figure 3.27.

So far the band engineering of the Sb-HBD is investigated. Area of the device is another compelling parameter to be investigated. The effect of reducing the area of the device on the junction resistance is illustrated in Figure 3.28. As can be seen, the simulated results are in well agreement with experimental data. By reducing the area of the detector, the junction resistance increases while the curvature coefficient remains constant. The most notable effect of reducing the area of the detector is the reduced junction capacitance. The AC analysis was also done in Sentaurus device editor and the corresponding junction capacitances for different diode areas was extracted. The junction capacitance from the measurement data and the simulated ones is plotted in Figure 3.29. The series resistance from experimental data is also plotted with junction capacitance. These values for series resistances are used to plot the extrinsic cut-off frequency. These curves can predict the optimum frequencies where the device can have acceptable performance. It was mentioned before, that the sensitivity of the detector in low frequencies can be approximated by:

$$\beta_{vdc} \approx R_j \gamma / 2 \tag{3.5}$$

The sensitivity of the detector vs. frequency can also be predicted by the equation 3.6.

$$\beta = \frac{\beta_{vdc}}{(1 + \frac{R_s}{R_j})(1 + \frac{R_s}{R_j} + (2\pi f C_j)^2 R_s R_j)} \tag{3.6}$$
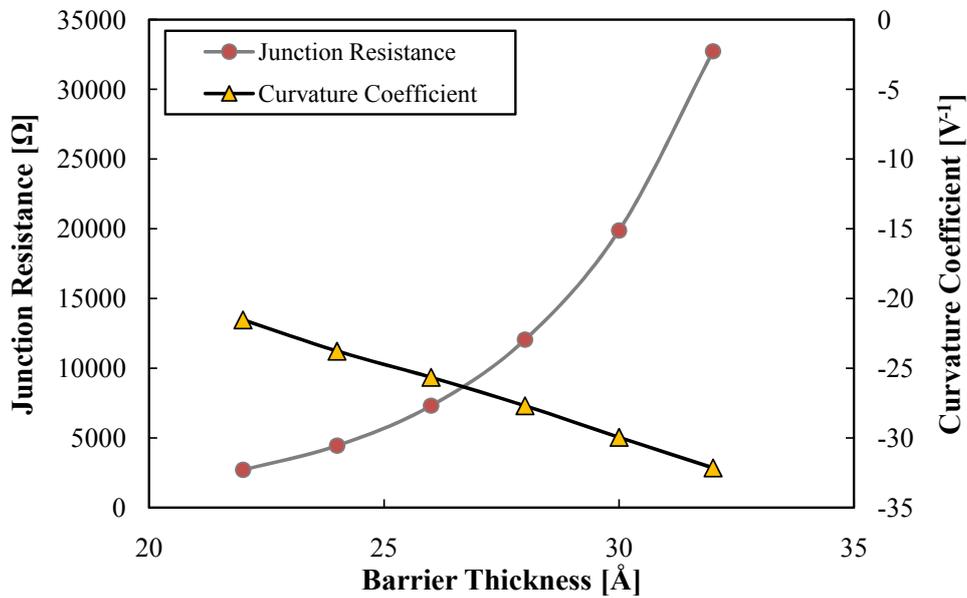
Figure 3.25: *The junction resistance and curvature coefficient versus barrier thickness for the device with 1 μm^2 area.*
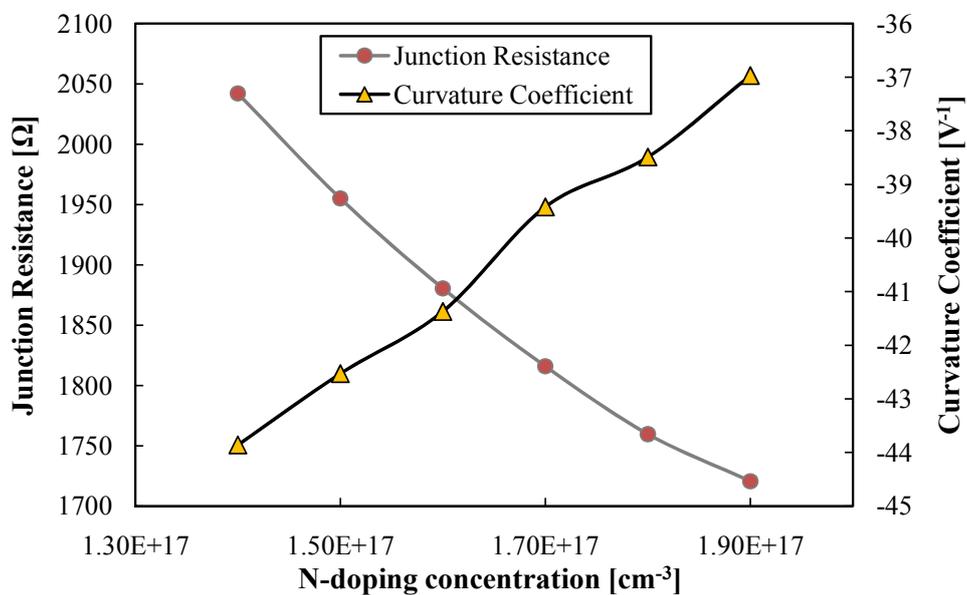

Figure 3.26: *The junction resistance and curvature coefficient versus InAs n-doping concentration for the device with 1 μm^2 area.*
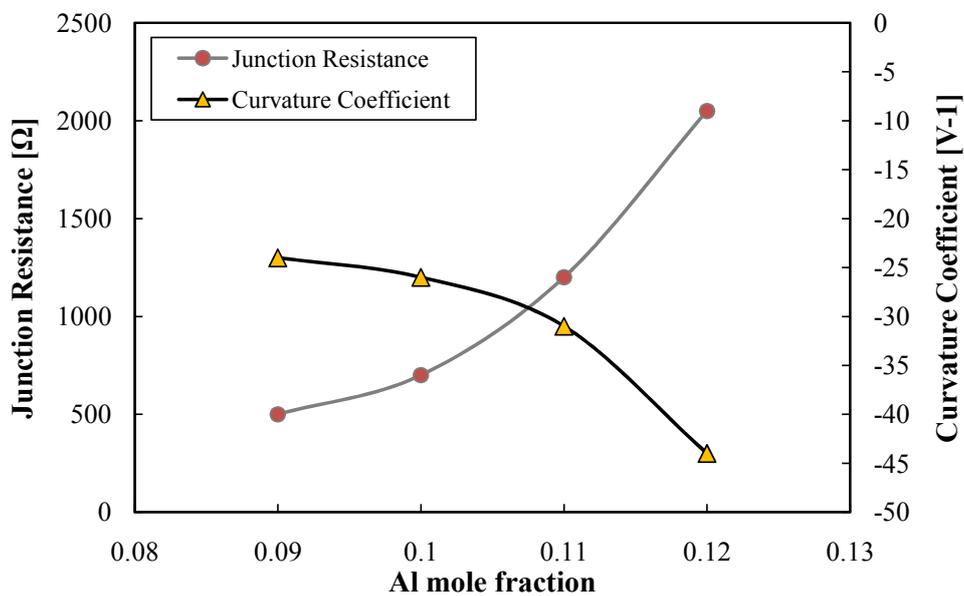
Figure 3.27: *The junction resistance and curvature coefficient versus Al-mole fraction for the device with 1 μm^2 area and δ-doping layer.*
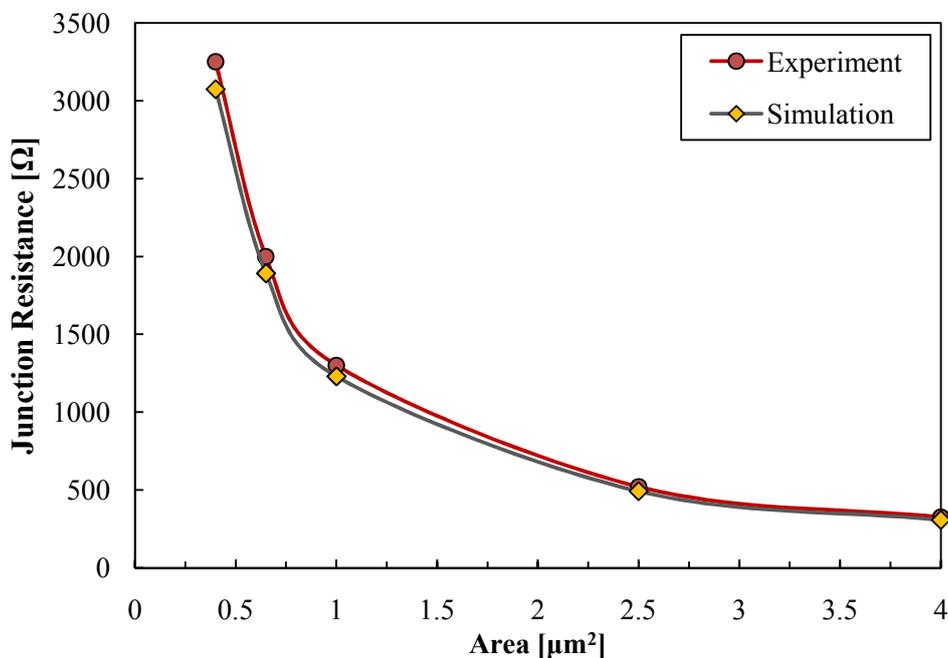
Figure 3.28: *The simulation and experimental data [36] for junction resistance versus area, for the device with 1 nm barrier thickness.*
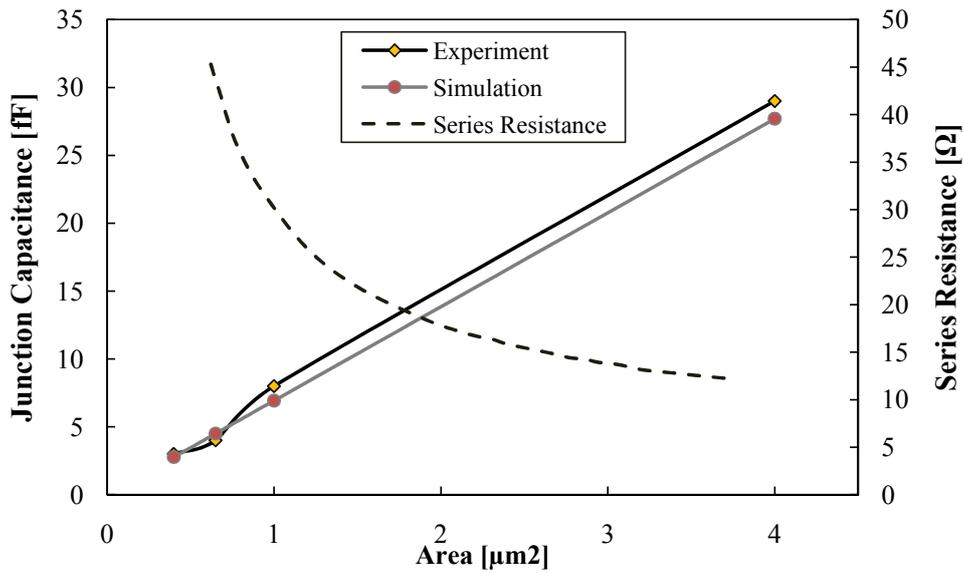
Figure 3.29: *The simulation and experimental data for junction capacitance versus area, for the device with 1 nm barrier thickness [36].*
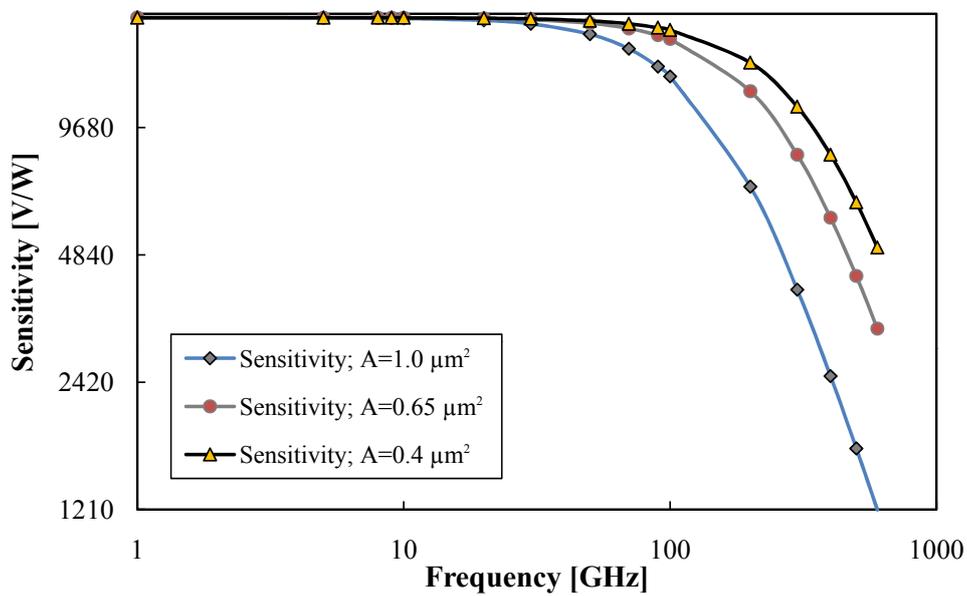
Figure 3.30: *The calculated voltage sensitivity versus frequency for three diodes with mesa area of 0.4 μm^2, 0.65 μm^2 and 1 μm^2 .*

4 MBE Growth and Characterisation of Sb-HBD Structures

Though Sb-HBD has shown excellent performance to be one of the best candidates for millimetre wave detectors, few have reported on how the material quality affects the device performance. From the material growth point of view, it is quite difficult to grow the Sb-HBD structures on GaAs, due to the 7% large lattice mismatch between the epi-structures and GaAs substrates. Although metamorphic growth technique enables accommodating such large lattice mismatch and success has been made with InAs/AlSb HEMTs where an AlSb metamorphic buffer is used, growth of InAs metamorphic buffer on GaAs is much more difficult. Growth of InAs on GaAs is likely to follow the Stranski-Krastanov mode, inducing island formation and rough surface. However, the reported Sb-HBDs are all grown directly on GaAs with rather little information on material growth. In this chapter, MBE growth of Sb-HBD structures is discussed and optimized.

n+ InAs	1000Å	$N_d = 1.3e19 \text{ cm}^{-3}$
n InAs cathode	500Å	$N_d = 1.4e17 \text{ cm}^{-3}$
Be δ-doping		$1e12 \text{ cm}^{-2}$
n InAs	45Å	$N_d = 1.4e17 \text{ cm}^{-3}$
AlSb	10-30Å	undoped
$Al_{0.12}GaSb$	150Å	undoped
p+ GaSb anode	300Å	$N_a = 1.3e19 \text{ cm}^{-3}$
n+ InAs	5000Å	$N_d = 1.3e19 \text{ cm}^{-3}$
InAs metamorphic buffer		0-1.5 μm
GaAs semi-insulating (100) substrate		

Figure 4.31: *The epitaxy structure of Sb-HBDs.*

4.1 MBE Growth of HBD Structures

The foreseeable challenges to grow Sb-HBD structure includes: (a) Precise calibration of growth rate and doping concentration are critical, as the device performance is very sensitive to the epi-structures such as AlSb thickness (can be as thin as 7

Å), InAs doping, and $Al_xGa_{1-x}Sb$ composition. (b) Growth of high quality InAs metamorphic buffer on GaAs is challenging. Due to the large lattice mismatch (7%) between the epi-structures and GaAs substrates, threading dislocations in the InAs metamorphic buffer may affect significantly on the I-V curves, acting as traps inducing leakage current and/or trap-assist tunneling. We shall optimize metamorphic buffer designs and growth conditions based on our long time experiences on strain engineering aiming at achieving a low threading dislocation density. (c) The bonding construction at the InAs/AlSb interface would have a significant effect on the Sb-HBDs. The interface of InAs/AlSb, which can be either Al-As like or In-Sb like, has been found significantly influencing InAs/AlSb HEMT performance. Al-As like interface is not recommended due to the Al-related defects. For Sb-HBDs, the band diagram can be quite different between the two type interfaces especially for a rather thin AlSb barrier thickness (several Å).

Sb-HBDs with different buffer thickness were grown on (100) semi-insulating GaAs substrate using a Riber C21 MBE system. The growth temperature for the whole structure was fixed at 510 °C. The structures of the Sb-HBDs are shown in Figure 4.31. The InAs buffer thickness, AlSb thickness and $Al_xGa_{1-x}Sb$ composition were varied. Figure 4.32 illustrates a Transmission Electron Microscopy (TEM) of the cross section of a grown Sb-HBD sample.

For samples in sections 4.1 and 4.1.1, the interface of InAs/AlSb was grown to be an In-Sb like bonding. This is achieved by controlling the switch sequence of the source shutters, which will be discussed more in section 4.1.2.

Test diode with four different sizes, 60x60, 80x80, 100x100 and 120x120 μm^2 were fabricated. The fabrication of these test diodes are explained in section 5.2.
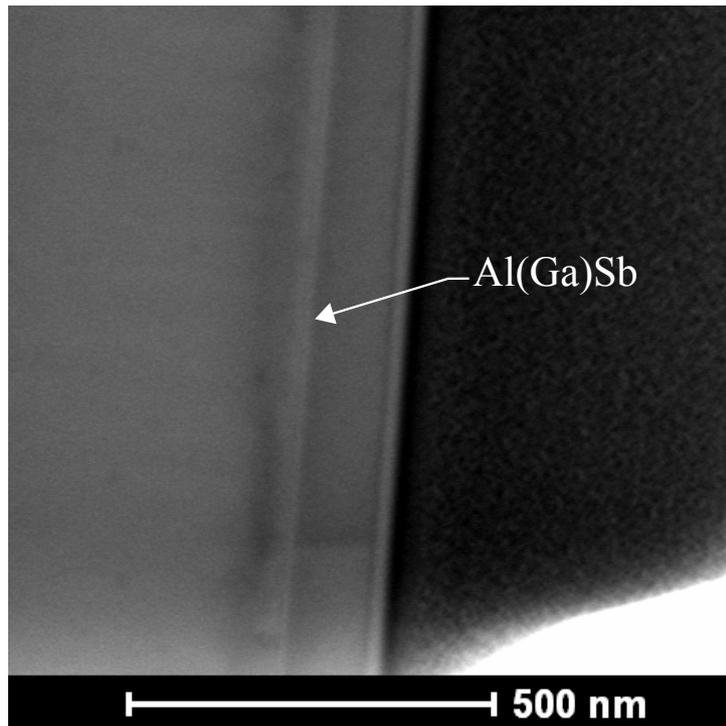
Figure 4.32: *TEM image of the buffer layer and the epi-structure; the bright color of Al(Ga)Sb layer makes it distinctive.*

(a) (b)
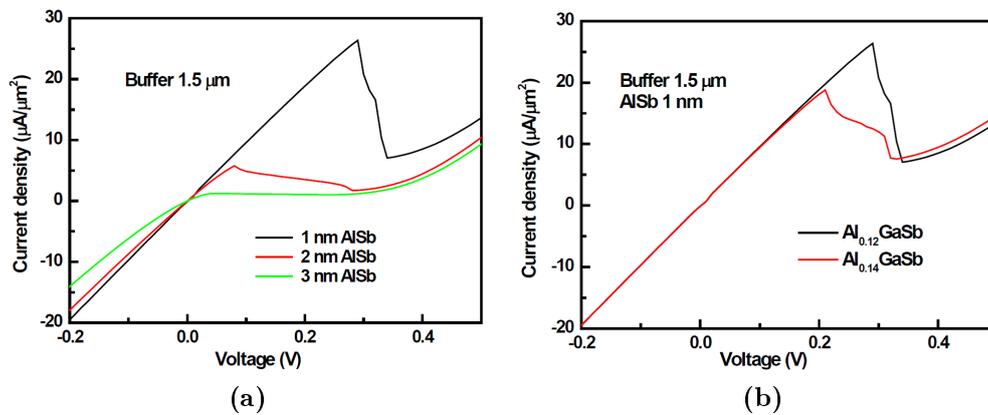
Figure 4.33: *The effect of various tunnel barrier thicknesses and Al composition on the I-V characteristics.*
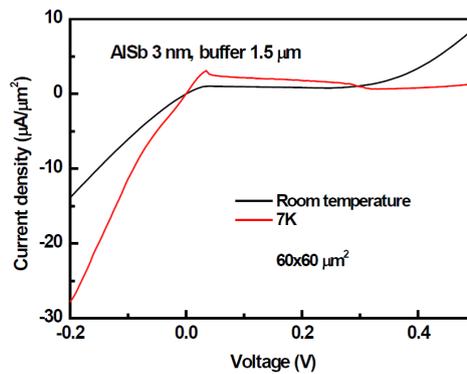
Figure 4.34: *The effect of temperature on the I-V characteristics.*

Figure 4.33a illustrates the current density as a function of applied voltage for diodes with different barrier thicknesses. As it has been discussed before, thicker barrier thickness increases the junction resistance and the curvature coefficient. For a 3 nm thickness AlSb barrier, the I-V characteristic is similar to that with 1 nm thick AlSb barrier. But due to a thicker AlSb barrier, both the forward and backward currents were smaller.

As it is evident in Figure 4.33b, incrementing the Al composition lowers the $Al_xGa_{1-x}Sb$ valence band, which further blocks the forward tunnelling current. Since, in this case, the lowering of the AlGaSb valence band edge is not discernible relative to the Fermi level on the InAs side, the backward current is insignificantly blocked.

Figure 4.34 compares the I-V curves of a diode measured at room temperature and at 7 K. The diode has a 3 nm thick AlSb barrier and a 60x60 μm^2 area. The difference between the ambient and cryogenic I-V behavior is a result of several parameters. Firstly, the band diagram also changes in different temperatures, see Figure 4.35a. However, the trend shows that, by lowering the temperature the valence band of AlGaSb moves closer to the Fermi level and so is the conduction band of InAs. Therefore, this doesn't significantly influence the tunnelling current. Secondly, lowering the temperature increases the backward current more significantly compared to the forward tunnelling current due to the different temperature dependency of the cathode and the anode's carrier spatial distribution as illustrated in Figure 4.35b. Thirdly, possibly due to a lower resistance at cryogenic temperatures, the tunneling current in reverse bias is higher than that at room temperature. The higher current at room temperature in higher voltages than the valley voltage (forward bias) is due to the thermionic-emission current, which is suppressed at cryogenic temperatures

Figure 4.36 shows the current (a) and the current density (b) as a function of applied voltage for diodes with a 2 nm thick AlSb barrier and 1.5 μm thick InAs buffer thickness. The backward tunneling current doesn't change too much with the diode size, but the forward current looks quite variant for different diode sizes. The forward current is more suppressed and the peak current shifted to lower voltage as the diode size decreases.

Figure 4.36b shows the current density for different diode sizes. Ideally, the current density for the same diode but different sizes should be the same. Interestingly, the current densities deviate from each other. The tunnelling current in forward bias has almost the same level, but with slightly misaligned peak voltages. The tunnelling current in reverse direction, though, varies remarkably. This also was observed in sample with 3 nm barrier in both ambient and crygenic temperatires, see Figure 4.37. These observations could to some extent address the state of the grown materials quality.
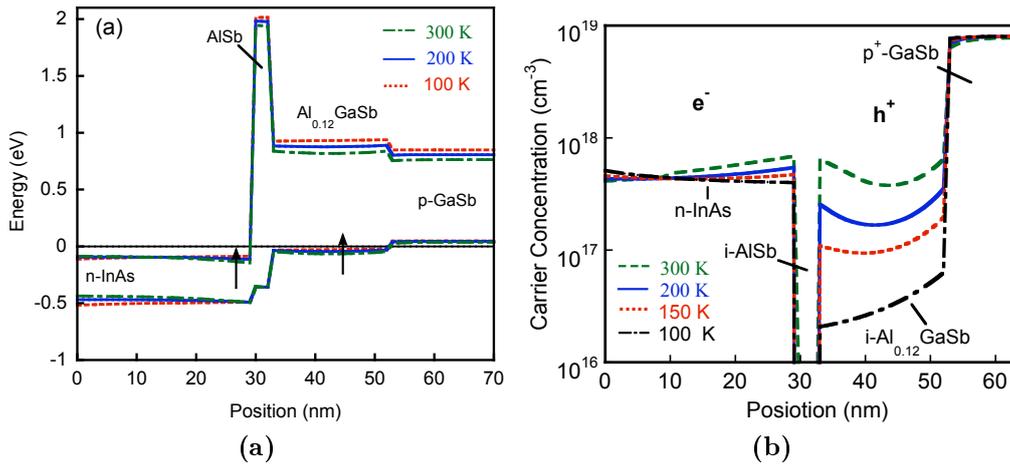
Figure 4.35: *The band diagram (a) and the spatial carrier distribution (b) of Sb-HBD in different temperatures [36].*
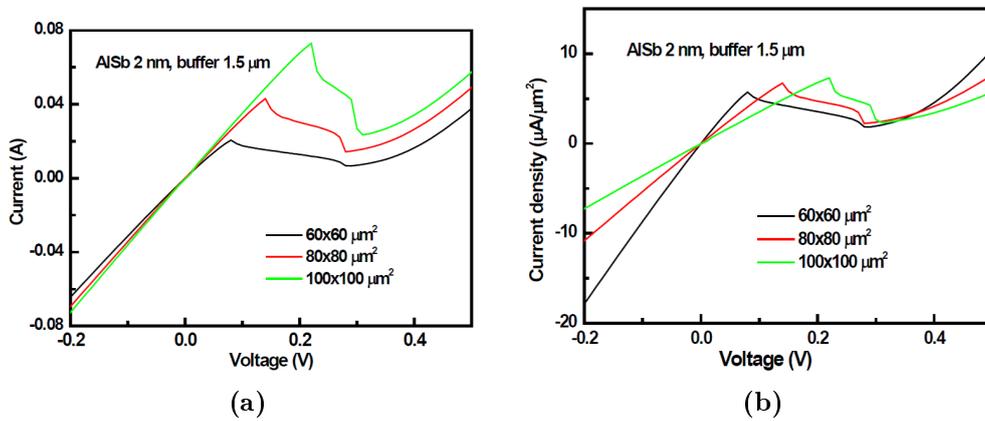
Figure 4.36: *Size dependency of current-voltage (a) and current density-voltage (b) characteristics.*
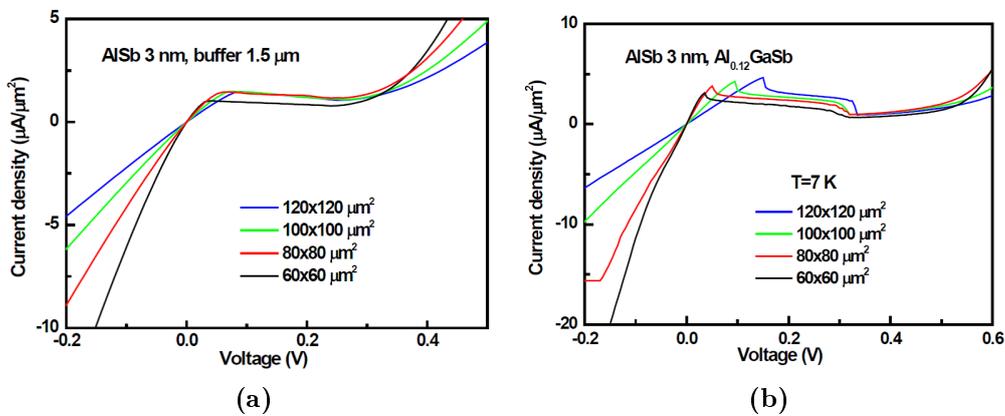
Figure 4.37: *The effect of different sizes on the I-V characteristics at both ambient and cryogenic temperatures.*

4.1.1 The Effect of Buffer Thickness

It is well known that the dislocation density decreases exponentially with the increase of the metamorphic buffer thickness. Based on this fact, we have grown Sb-HBDs with different InAs buffer thickness, to check the effects of dislocation on the device performance.

Four Sb-HBD samples were grown with different InAs metamorphic buffer thicknesses (0, 0.5, 1 and 1.5 μm). For the sample without buffer layer, the 500 nm highly doped InAs cathode layer can be regarded as the metamorphic buffer. TEM image of the cross section of the four samples were investigated, see Figure 4.38. Most of the dislocations were buried at the interface between the metamorphic InAs buffer and GaAs substrate, however, there are still a lot of dislocations penetrating into the epi-structures when the buffer thickness is thin. For the sample with a 1.5 μm buffer thickness, the top region of the buffer is almost dislocation free. This is because the dislocations can glide along some crystalline directions and annihilate each other during the growth of the metamorphic buffer. The thicker is the metamorphic buffer, the larger possibility is for annihilation of the dislocations.

Figure 4.39 shows the effect of buffer thickness on the performance of a diode with a 3 nm thick AlSb barrier and two different device areas. It is apparent that the backward current is higher for samples with thicker buffers, indicating a lower resistance. This is because the dislocations in the epi-structures can trap the carriers which do not contribute to the overall current, i.e. inducing a larger resistance. And a higher forward tunneling current in the NDR region was observed for samples with a thinner buffer, probably due to a trap assisted tunneling. This states that, thick buffer layer is beneficial by introducing higher curvature coefficient near zero-bias which leads to better sensitivity.

It was also observed that there was a larger discrepancy between the I-V characteristics of the same size test diodes in the same chip with thin buffer layer. This could be ascribed to the worse material quality obtained with a thin buffer compared to the thick ones.

Figure 4.40 shows the I-V curves of the diodes with different buffer thicknesses at cryogenic temperature. By comparing the I-V characteristics of the same diode with various buffer thicknesses at both cryogenic and ambient temperatures, it can be noticed that the difference between forward tunnelling current becomes negligible at cryogenic temperatures. This can be attributed to the higher probability of trap-assisted tunnelling to happen at ambient temperatures compared to cryogenic temperatures. As the phonon energy required for trap-assisted tunnelling is more probable to be obtained at room temperature rather than at cryogenic temperatures.
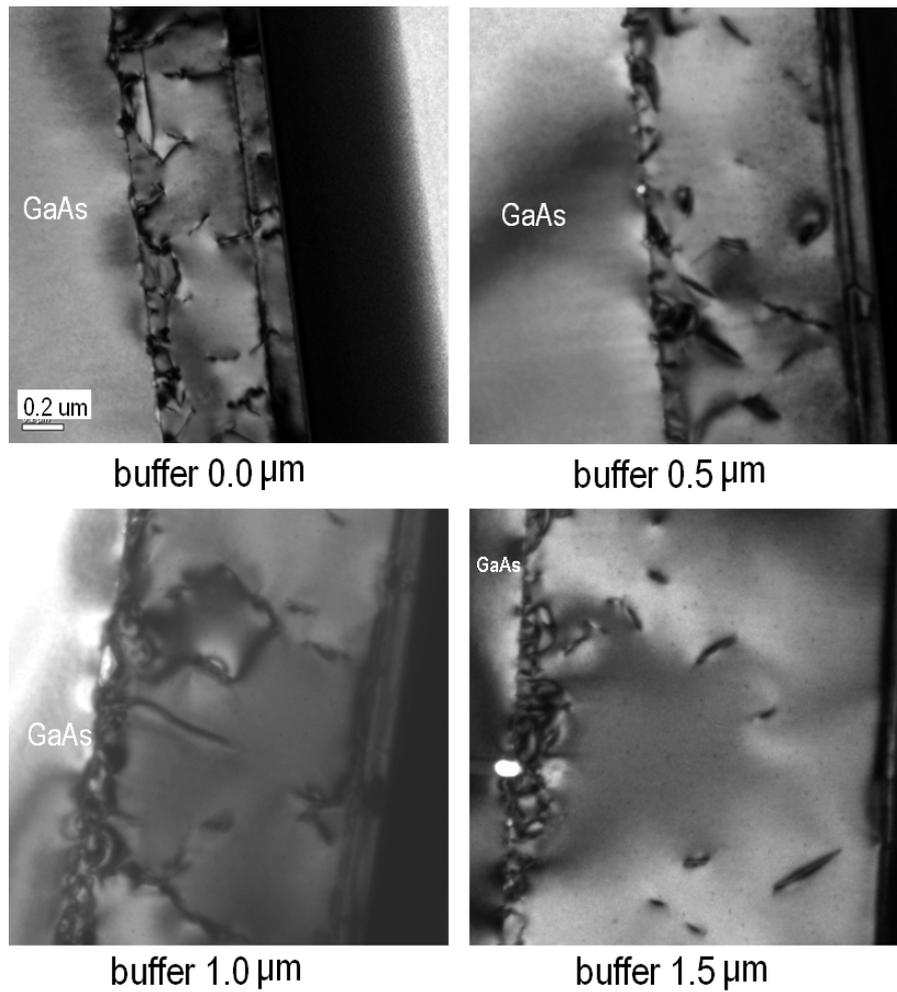
Figure 4.38: *The TEM images of four samples with different buffer thicknesses showing the penetration of the dislocations into the epi-structures.*
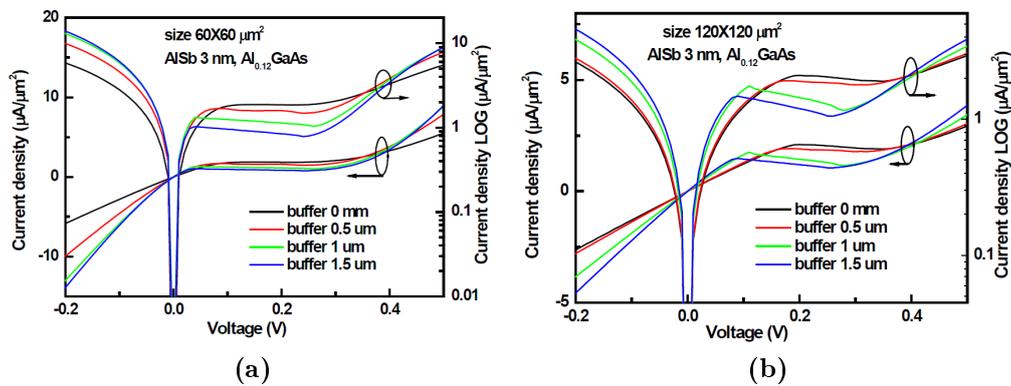
Figure 4.39: *The comparison of the I-V characteristics of four diodes with two different sizes and varoius buffer thicknesses at room temperature.*
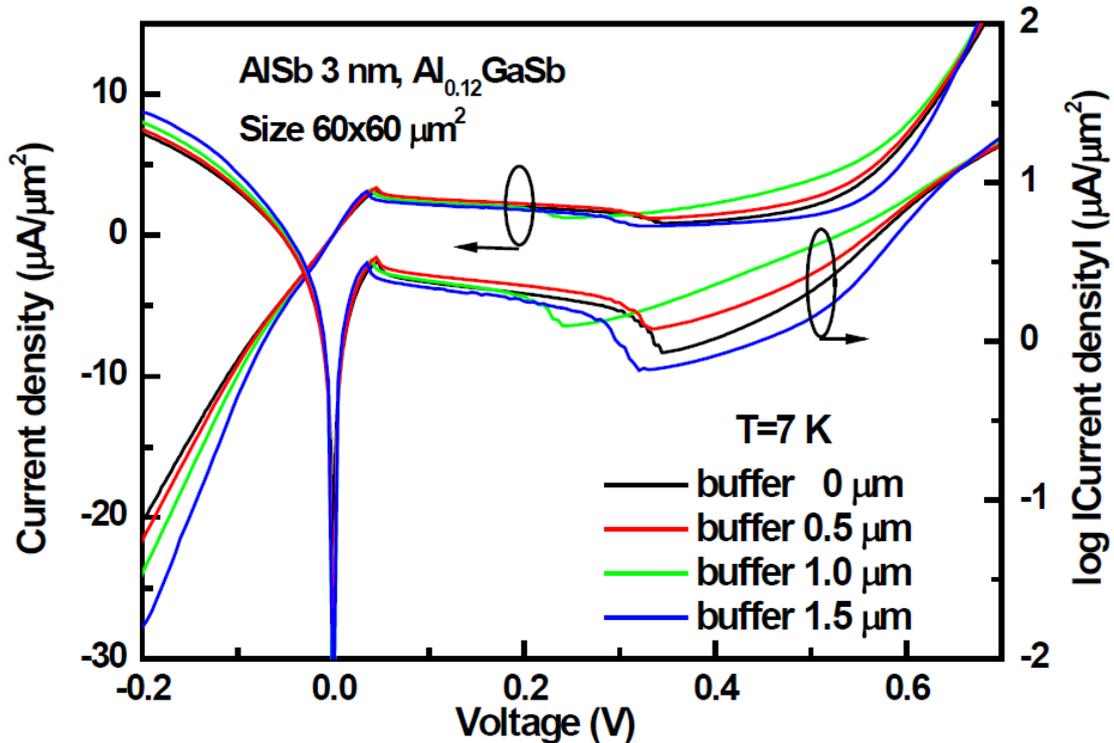
Figure 4.40: *The comparison of the I-V characteristics of four diodes with different buffer thicknesses at cryogenic temperature.*

4.1.2 The Effect of Interface Bonding

As mentioned before, the interface of InAs/AlSb is either Al-As like or In-Sb like since both the cation and the anion are changed [54], see Figure 4.41. The construction of interface bonding can be controlled by the sequence of open/close of the source shutters, i.e. using either Sb soaking or As soaking. Figure 4.42 illustrates the growth procedure for forming either an In-Sb like or an Al-As like interface. As seen in Figure 4.42(a), after finishing growth of InAs, both In and As shutter were closed and Sb shutter was open for 3 seconds, afterward we opened In for 1 second followed by another 3 second Sb, then we opened Al to grow the AlSb. In this way, the interface is forced to be an In-Sb bonding. Figure 4.42(b) shows a similar way to grow an Al-As bonding interface. In this section, Sb-HBD samples with 1 nm or 3 nm thick AlSb barriers were grown. The effects of the interface bonding constructions on the thin or thick barrier Sb-HBDs were investigated. Previous studies about interface bonding of InAs/AlSb have reported [55] that the interface quality of InSb-like is better than AlAs-like bonding. This roughness of AlAs IF introduces a relatively high density of additional crystal defects such as misfit dislocations and stacking faults [55]. With AlAs like interface bonding higher peak to valley ratio (PVR) is observed. Lower resistance leading to higher backward current is evident for AlAs-like surface.

Since in InAs/AlSb HEMTs the InAs layer is used as the channel, higher channel mobility is preferred. This can be achieved with In-Sb IF bonding [56]. Conversely,
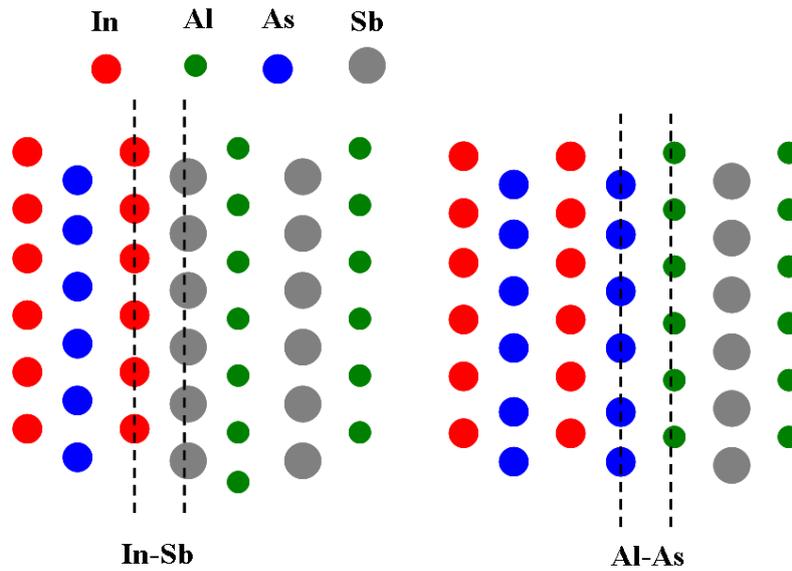
**Figure 4.41:** *The creation of the In-Sb IF and Al-As IF bonding.*
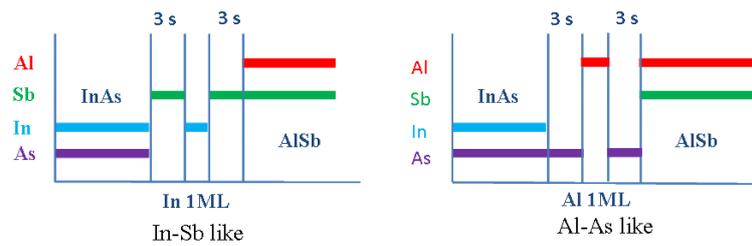
Figure 4.42: *Growth procedure for forming In-Sb IF and Al-As If bonding.*
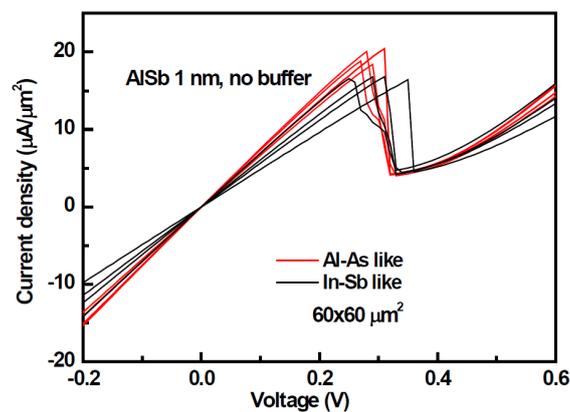

Figure 4.43: *The comparison of the I-V characteristics of two possible interface bonding, In-Sb like and Al-As like.*
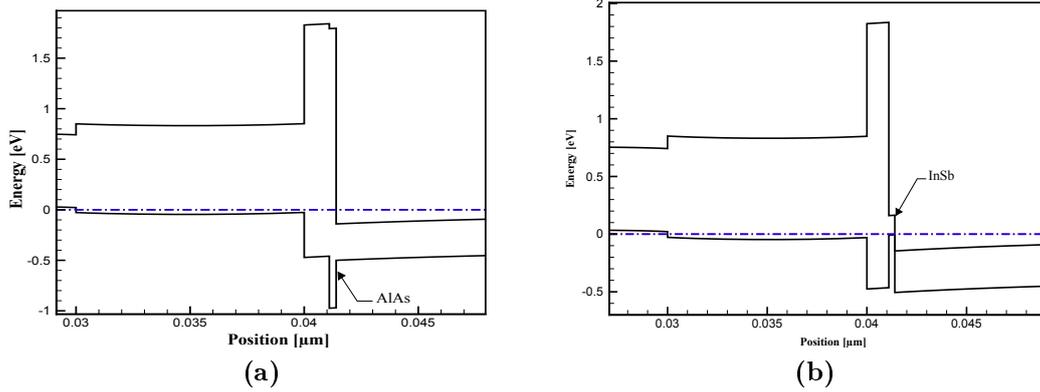
Figure 4.44: *InAs/AlSb tunnelling interface bonding structure (a) AlAs-like and (b) InSb-like.*

in Sb-HBDs, the current is vertical to the InAs/AlSb interface. One monolayer of the either AlAs-like or InSb-like interface bonding is approximately the lattice constant divided by two, resulting in 3 Å thickness. In Sb-HBDs with 10 Å barrier thickness, one monolayer becomes comparable. To be able to discuss more about these two types of IF bonding, the band diagram with both AlAs IF and InAs IF is calculated with TCAD, see Figure 4.44. As it is shown in Figure 4.44b, a quantum well is created in the InSb IF bonding. In this case, in forward direction, the electrons leaving InAs might get trapped in the quantum well and the holes leaving AlGaSb valence band might as well recombine with the electrons in the quantum well. This could be the reason for lower forward current peak value. Also the same can be described for the backward current of In-Sb IF bonding case having higher resistance. In high forward bias voltages, the sample with AlAs IF, has lower thermionic emission current due to thicker barrier width.

It can be concluded that AlAs-like IF bonding is advantageous in the case of Sb-HBD for having relatively higher curvature coefficient near zero-bias.
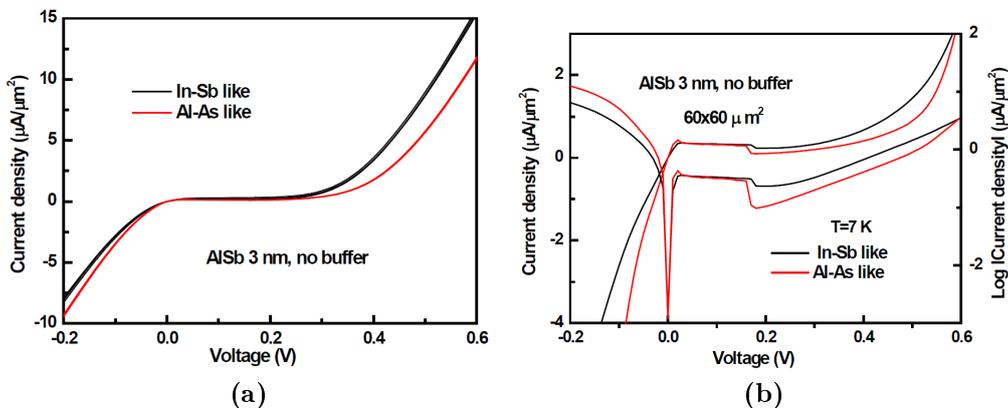
Figure 4.45: *The comparison of the I-V curves of two different tunneling interface bonding types, Al-As like and InSb like, at both ambient and cryogenic temperatures.*
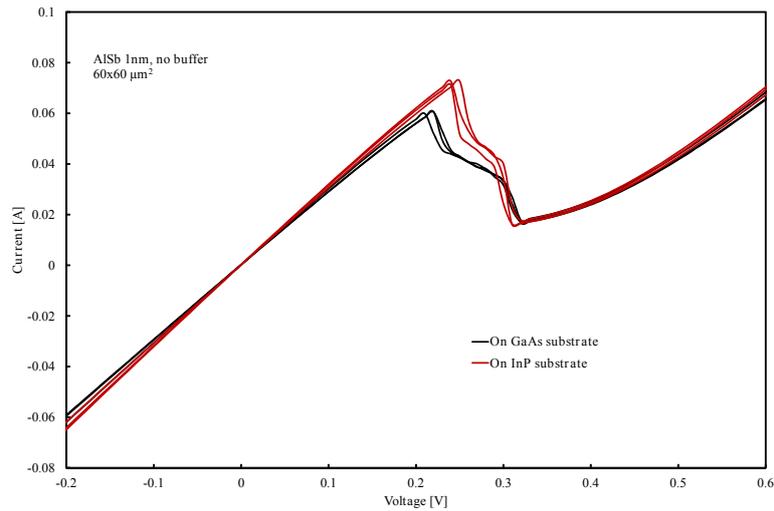
Figure 4.46: *The comparison of the I-V curves for the heterostructures on InP and GaAs substrate.*

The Sb-HBDs were also grown on the InP substrate. According to Figure 4.46, the I-V curve for InP and GaAs substrate looks very similar, except for the higher peak current in the case of InP substrate.

5 Fabrication

## 5.1 Fabrication and Process flow

This study mainly aims to investigate fabrication techniques for developing detectors with small areas ranging from sub-micron to micron scale. The entire fabrication was carried out at Chalmers Nanofabrication Laboratory. The details of process steps including mesa etching, passivation, dielectric via etching and airbridge for metal interconnect definition are further discussed. A mix-and-matched approach, exploiting both the electron-beam lithography and optical lithography is used for defining the contacts. Controlling the etch rates and having adequate alignment accuracy in lithography is of considerable concern in these process developments. The fabrication of Sb-heterostructure backward diodes consists of six mask layers. Figure 5.47 shows the complete mask set drawn in AutoCAD that is used for the fabrication of the sub-micron scale diodes.

As shown in Figure 5.48, the Transmission Line Model (TLM) structures were also included in the mask design to evaluate the contact resistances of the metallic pads.

Figure 5.49, illustrates the thermometer mask design which is used later on in the e-beam lithography dose test. The thermometer consists of several rectangles with 50 nm width. By approaching the bottom of the thermometer, the distance between rectangles reduces. Generally, depending on the e-beam calibration, resist type, dose value and development the final pattern can be smaller or larger than that of the design in the mask. This structure is designed such that if the resist is positive, after development, these distances between rectangles will be left with resist on top of them. However, towards the bottom, these distances are so small that if either one of the conditions above is not suitable, the resist in between would be removed. Therefore, the values to the left of the developed region defines the resolution of the attained lithography.

To attain an adequate alignment accuracy and to measure the actual misalignment, alignment structures shown in the Figure 5.50 are added. As seen in the layout, the big rectangles in the middle are aligned and the other ones to the left and the right are misaligned by specific values such as 0.25 μm, 0.5 μm, etc. For instance, if either one of the rectangles which are designed to be misaligned, wound up to be aligned, that specific value is the inaccuracy in the alignment.

Eventually, the diode structure mask layer is shown in Figure 5.51. In the diodes mask layer, the metallic pads with ground-signal-ground (GSG) structure are added to also enable S-parameter measurement.
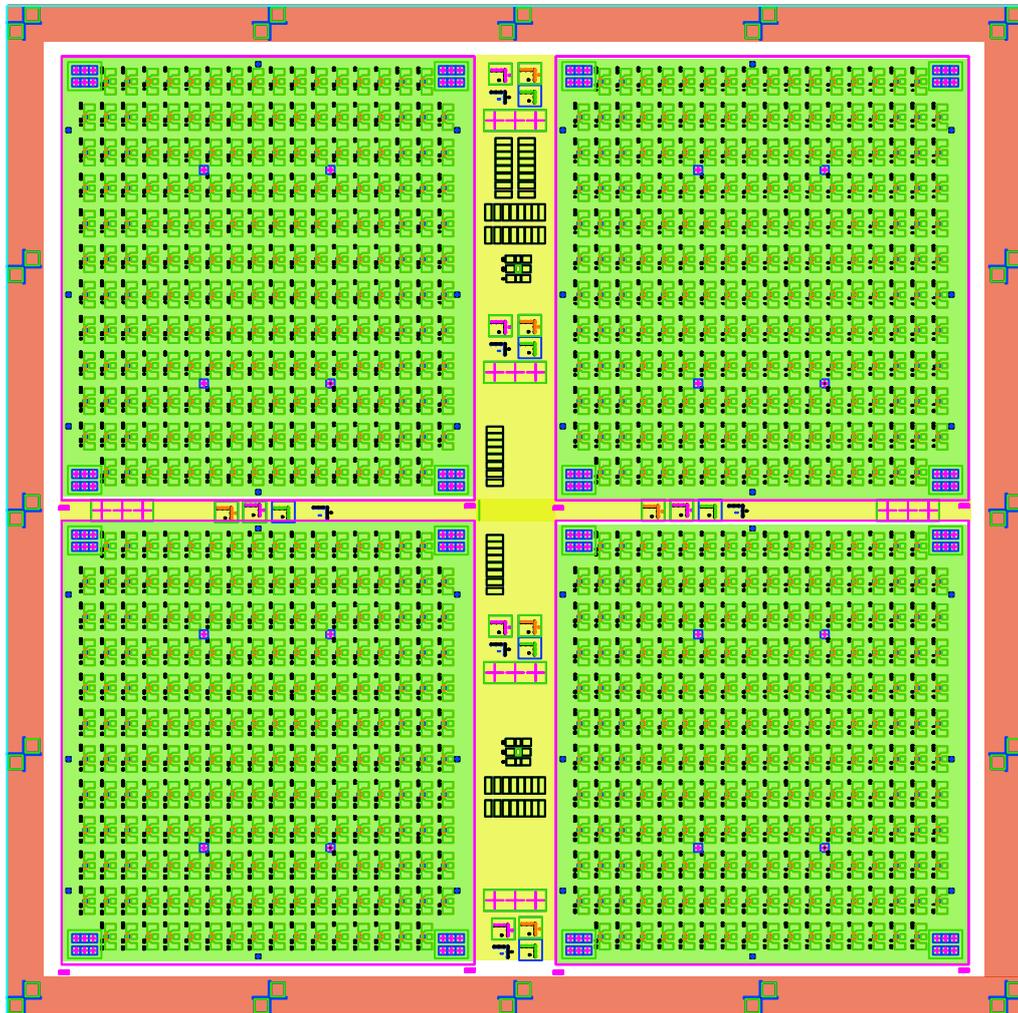
Rough photolithography alignment marks

TLM structures, photolithography alignment marks, e-beam lithography P&Q marks

Diode structures with different cathode diameters plus the e-beam lithography chip marks

Figure 5.47: *The schematics of sub-micron scale Sb-HBD's mask layer.*
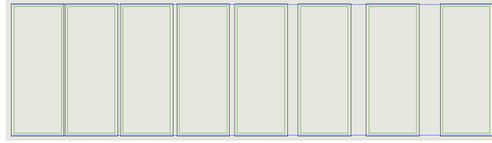
Figure 5.48: *The TLM structures for contact resistance measurements.*
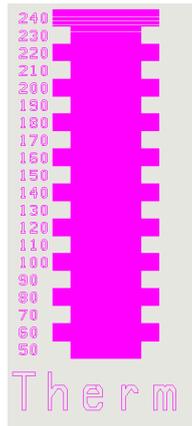
Figure 5.49: *The schematics of the "thermometer" structure utilised in e-beam lithography dose test.*
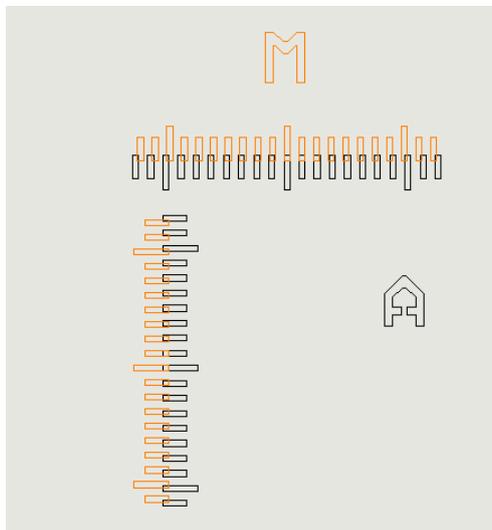
Figure 5.50: *The alignment marks used for aligning the anode contact mask layer to the already defined cathode contact.*
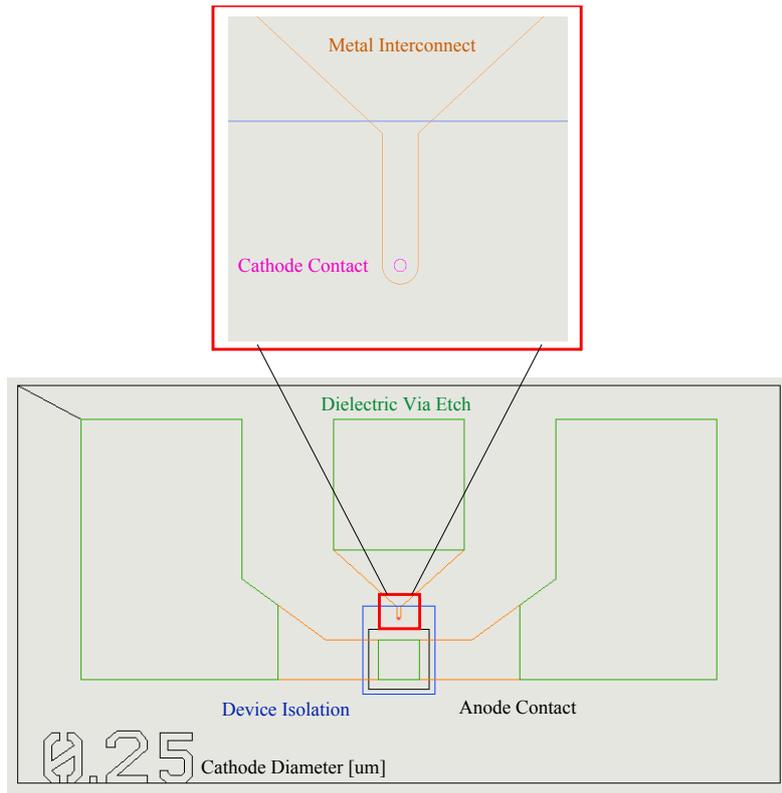
Figure 5.51: *The schematic of the diode's structure consisting of the cathode contact, anode contact and the S-parameter measurement pads. The signal pad width is 65 μm and the gap width between signal and ground pads is 45 μm.*

5.1.1 Cathode contact formation

The first step is the cathode contact formation. This was first done using optical lithography for bigger area detectors which were fabricated using dummy samples. Due to the resolution of optical lithography technique, the minimum achievable cathode diameter was limited to about 1 μm. Later on, e-beam lithography was employed to define sub-micron cathode areas.

To avoid coating the sidewalls of the resist while evaporating metal, an undercut resist profile is needed which is well-suited for lift-off. In order to obtain the lift-off profile for the cathode contact two types of bilayer resist were chosen. Commonly, the MMA (8.5)(methyl methacryllate)/PMMA (poly methyl methacryllate) is used for lift-off of the metallic structures. Due to extremely high-resolution (20nm), ease of handling and stability, PMMA is the most commonly used e-beam resist. Figure 5.52 illustrates the lift-off process steps with MMA/PMMA bilayer e-beam resist. MMA (8.5) is spun on the sample and is soft baked at 130 °C for 5 minutes. This is followed by the same process for PMMA (A2).

LOR as an undercut layer followed by UV5-0.8, DUV/e-beam resist as the top layer (imaging resist) for lift-off process was investigated as the second choice of bilayer resist structure. The UV5 is the imaging resist, meaning that the final shape of

PMMA

MMA

Substrate

MMA solves more in the developer than PMMA

Metal evaporation
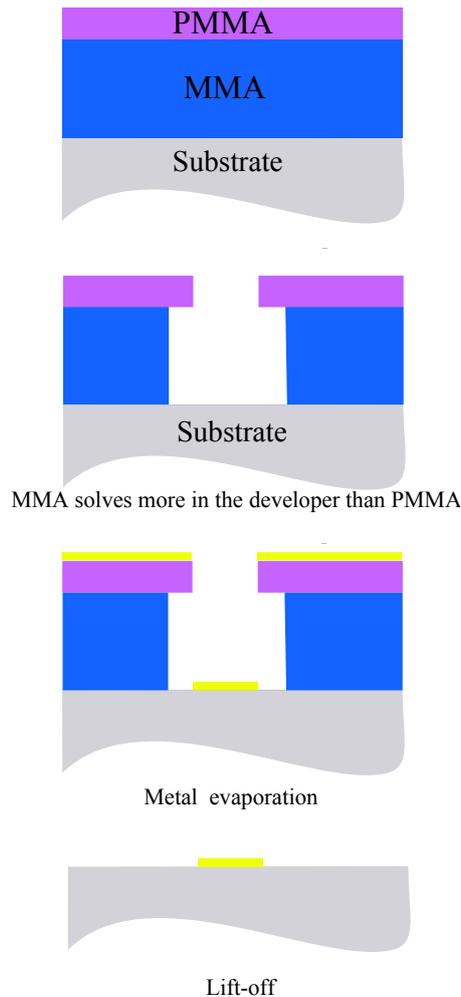
Lift-off

Figure 5.52: *The Lift-off process steps with e-beam lithography resist stack, MMA/PMMA.*

the metal will be the shape of UV5. First, LOR 3A as bottom layer is spun at 5000 rpm and soft baked at 160 °C which gives a thickness of approximately 250 nm. UV5 is then spun at 4000 rpm and soft baked at 130 °C with final estimated thickness of 700 nm.

Right after the e-beam exposure, the sample with UV5 resist had to be baked at 130 °C. Then it was developed in MF24A developer and rinsed in DI water. The sample with MMA/PMMA stack resist was directly developed in IPA:water (10:1) solution and rinsed in IPA.

A dose calibration was conducted for the samples with either MMA/PMMA or LOR 3A/UV5 to determine the optimum dose. The mask consists of several cells and the dose is swept along one direction with judicious increments. Within each cell there exists circles with diameters ranging from ten microns to three hundred nanometers. A thermometer as shown in Figure 5.49 was included in each cell to

better visualize the process of under or over developing of the structures. Eventually, due to the faster exposure and suitability for big patterns of the last fabrication step (metallic pads), the LOR 3A/UV5 resist stack was selected. Although PMMA offers higher resolution, the resolution provided with UV5 was sufficient for the current structures. In this step of e-beam lithography aperture five and 1 nA current is chosen.

Right before cathode metallisation by e-beam evaporation, the native oxide on the wafers surface was removed by a 5 second dip etch in $HCl : H_2O$ (ratio 1:25) solution to have clean InAs surface. First, 200 Å of Ti was deposited to compensate for poor adhesion of Au on semiconductor surface. Secondly, 2000 Å of Au, which serves as low electrical resistance layer, was evaporated. For the lift-off process, the sample with PMMA resist was soaked in acetone. As for the UV5 sample, after soaking it in acetone, the sample should be placed in 1165 remover to clean up the LOR 3A. Figure 5.53 shows the scanning electron micrograph (SEM) of the cathode contact after metallisation from the sample with UV5 resist. The e-beam mask for this contact was designed for a radius of 400 nm. It is evident in the image that the side walls have a slope. This certain topography of the cathode contact is due to the deposition of metal not only on the top side of the imaging resist but also on the inner sides of it. This states that, during the evaporation the opening of the top resist becomes smaller and smaller leading to a slope. Figure 5.54 shows the cathode contact formed with the MMA/PMMA stack resist which the disfigured (irregular) shape of the cathode is due to the insufficient applied dose.
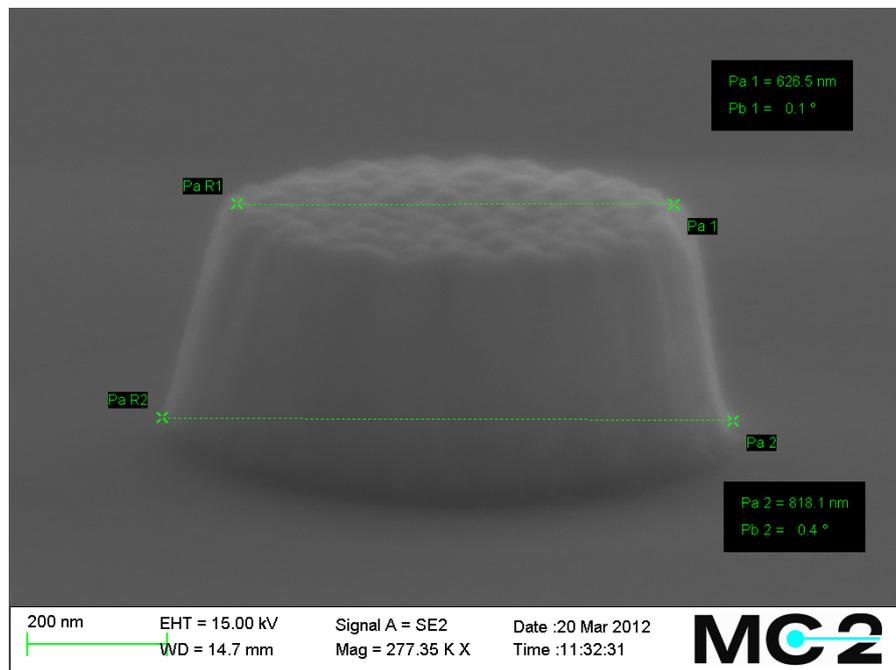
Figure 5.53: *The sub-micron cathode contact formed with LOR/UV5 e-beam resist stack layer.*
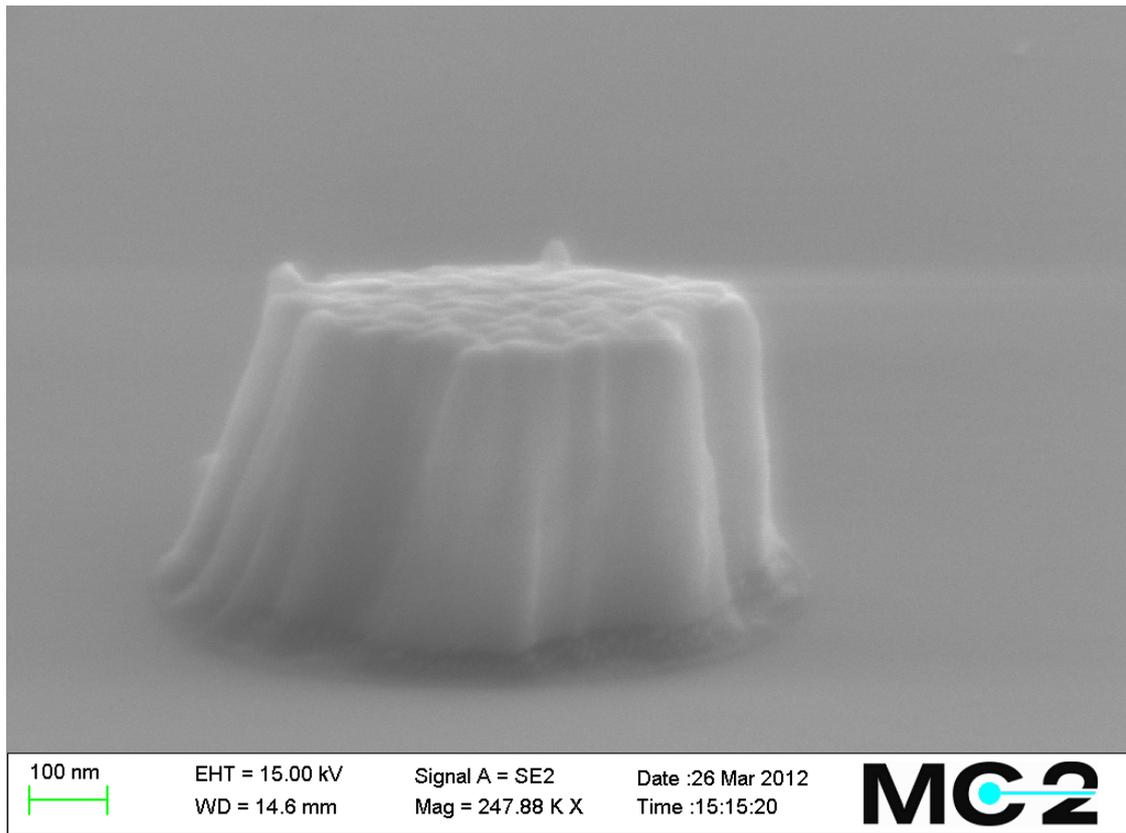
Figure 5.54: *The sub-micron cathode contact formed with MMA/PMMA e-beam resist stack layer.*

5.1.2 Mesa Etch

As the heterostructure mesa can be defined by both wet chemical etching and dry etching, several experiments were conducted to investigate the appropriate etching method, prior to main device fabrication. The first attempt was to evaluate selective etchant for both InAs and Sb-containing layers. Accordingly, test samples with either InAs or GaSb grown on GaAs substrate were selected. $NH_4OH : H_2O$ solution with ratio (1:4) which is highly selective over InAs [57] and developer MF319 were selected for GaSb sample. As for the InAs sample, citric acid aqueous and H_2O_2 with 1:2 ratio, acetic acid (CH_3COOH): $H_2O_2 : H_2O$ (5:10:100) and $HNO_3 : H_2O_2 : H_2O$ (1:1:4) solution were chosen. Etching with acetic acid solution led to lower rate (15Å/sec) than citric acid solution (20Å/sec) and both left rough surface, see Figure 5.55a and Figure 5.55b. As for the GaSb sample, the surface was less rough with ammonium solution, see Figure 5.56.

Later on, $H_2SO_4 : H_2O_2 : H_2O$ (1:8:80) and $H_3PO_4 : H_2O_2 : H_2O$ (1:1:100), as nonselective etchant for InAs, GaSb, AlSb and AlGaSb were examined on InAs/GaSb super-lattice. Table 5.2 summarizes the etchant used for different samples. The sulfuric acid solution left an extremely rough surface, unlike phosphoric acids, see Figure 5.57. The colored surface is due to the reflections from the very

rough surface.

One of the disadvantages of wet chemical etching for Sb-bearing materials is that a large amount of samples are sacrificed to determine the etching rate. As AlSb is highly reactive when exposed to air, the sample can only be etched as long as it is not exposed. Therefore, any attempt to etch after taking the sample out of the solution would be unsuccessful. Apparently, the oxide created on the surface can not be removed further after exposing to air. Furthermore, since in wet chemical etching the semiconductors get etched both vertically and horizontally, precise investigation of the measures of the undercut created under the metal is needed.

Dry etching using Inductively Coupled Plasma (ICP) method with $Ar : Cl_2$ is another alternative. A repeatable etch rate was obtained with both material grown in Chinese Academy of Science and Chalmers, see Figure 5.58. In this tool, a laser beam pattern at 674.3 nm is used to monitor the etching depth. One period of this reflectance pattern corresponds to half wavelength. In the reflectance pattern, four changes of direction of the curve are observable which indicates the four changes of materials. The desired etch depth is achieved while the curve reaches the straight horizontal line, which indicates InAs buffer (stop layer) layer. Approximately, one minute and thirty seconds of etching is equivalent to 2400 Å. Herein, the metal layer is used as the mask layer. Since in the dry etching process part of the Au on top is also etched, 200 Å of Ni was additionally evaporated on top of Au as the cap layer. In order to prevent unstable etch rate, dry etching was performed in several steps with wait sequences. Additionally, the use of thermal tape as a heat sink is recommended. Figure 5.59 shows a SEM image of a test structure after dry etching. The boundary between the semiconductor layers and the top metallic layer is apparent. There are signs of oxidation in the Sb-bearing material, due to long exposure to air. Figure 5.60 and Figure 5.61 illustrate the SEM image of the side and the top view a cathode contact after dry etching step, respectively.

After dry etching the cathode, a very short etch was done in $H_3PO_4 : H_2O_2 : H_2O$ (1:1:100) solution. This can be considered as the surface treatment to smooth out the sidewalls.

Table 5.2: *The etchant used for different samples.*

	InAs	GaSb	InAs/GaSb
Etchant	$CH_3COOH : H_2O_2 : H_2O$ (5:10:100) $HNO_3 : H_2O_2 : H_2O$ (1:1:4) citric acid aqueous : H_2O (1:2)	$NH_4OH : H_2O$ (1:4) MF319 developer	H2SO4 : $H_2O_2 : H_2O$ (1:8:80) H3PO4 : $H_2O_2 : H_2O$ (1:1:100) Citric acid aqueous : H_2O (1:2)

Figure 5.55: *The microscopic image of InAs sample's etched surface using citric acid solution(a), and acetic acid solution(b). The round features are the micron-scale cathode contacts with Ti as the cap layer with the radius of 1-4 μm.*
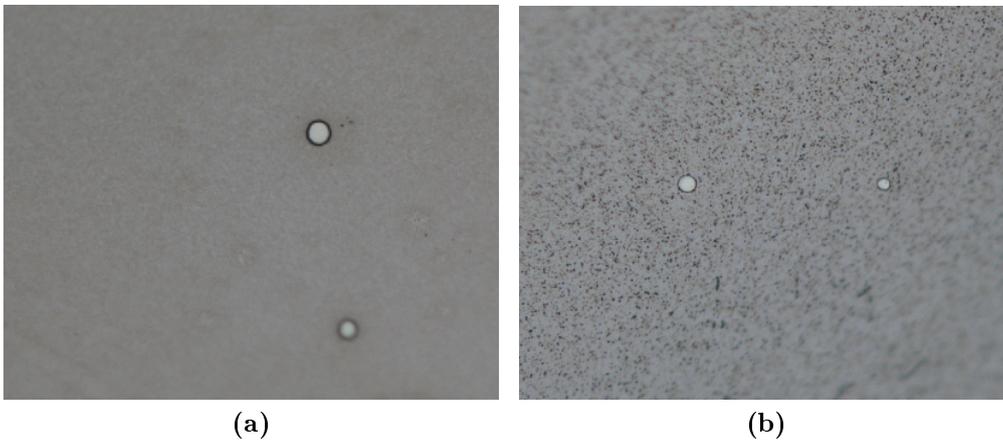
Figure 5.56: *The microscopic image of GaSb sample's etched surface using Ammonium solution(a), and MF319 developer(b).*
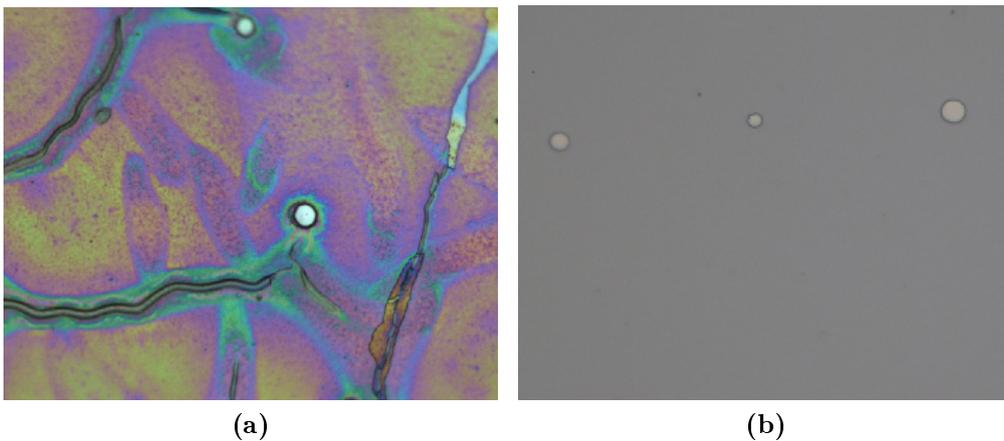
Figure 5.57: *The microscopic image of InAs/GaSb super-lattice sample's etched surface using sulfuric acid solution(a), and phosphoric acid solution(b).*
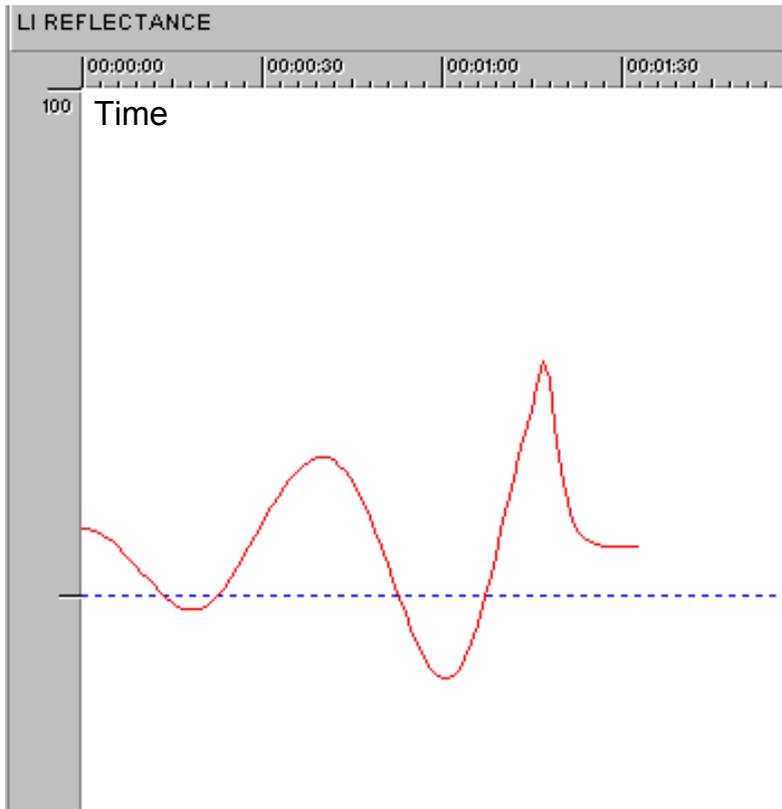
Figure 5.58: *The reflectance curve obtained from dry etching Sb-HBD using ICP tool.*
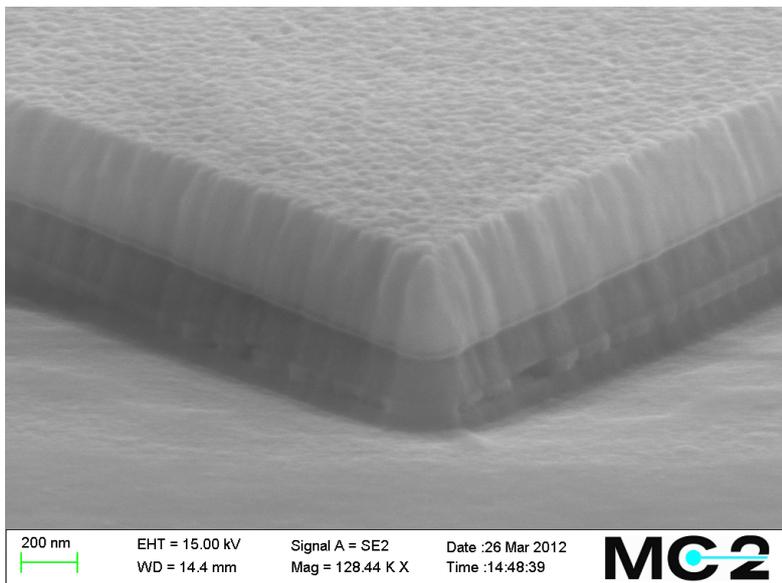
Figure 5.59: *SEM image of a test structure after the dry etching.*
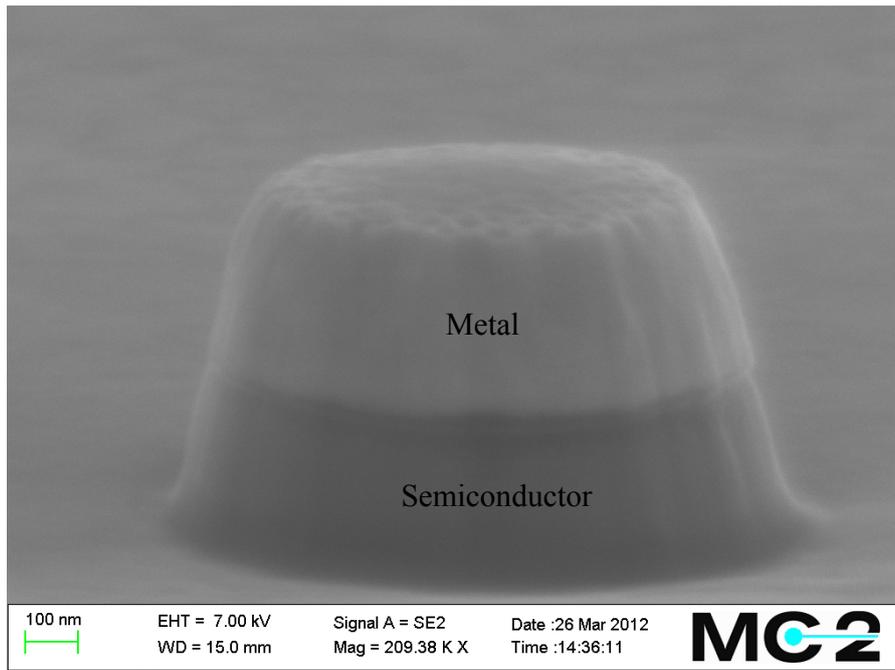
Figure 5.60: *The SEM image of a cathode after dry etching using ICP tool (side view).*
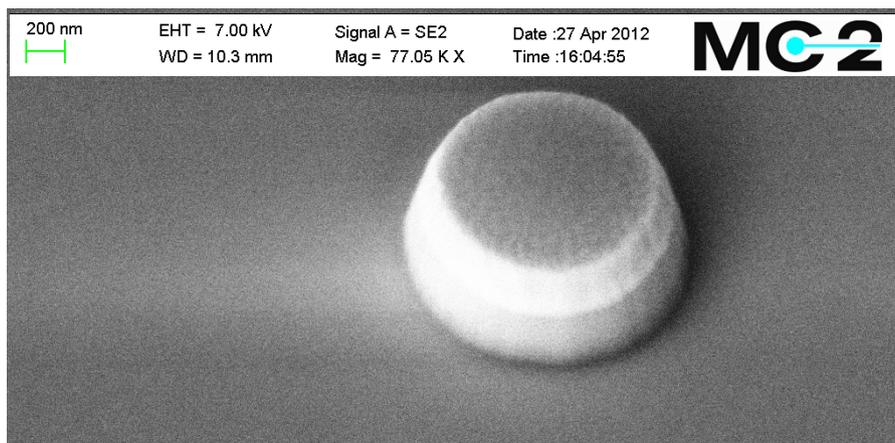
Figure 5.61: *The SEM image of a cathode after dry etching using ICP tool (top view).*
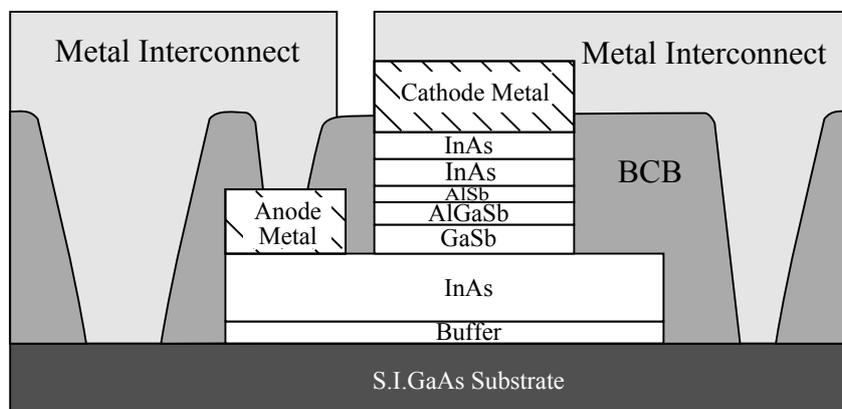
Figure 5.62: *The schematic cross-section of the Sb-heterostructure backward diode [36].*

5.1.3   Anode Metallisation and Device Isolation Etch

The anode contact was defined using image reversal photolithography to ease the lift-off process. In this recipe photoresist AZ 5214 is spun on the sample and soft baked on hotplate. In this step the photolithography mask is aligned using the alignment structures shown in Figure 5.64. As can be seen in the Figure 5.62, the anode contact is realized by evaporating Ti/Au (200/2000) on the fairly thick highly doped InAs layer. After anode metal contact deposition using electron beam evaporation, device isolation patterns are defined with optical lithography such that the resist covers the area containing both the anode and the cathode contact.

The device isolation is defined by etching down to the substrate using ICP dry etching. Device isolation etch can also be realized using wet chemical etching. If the etch rate is not fast enough, the longer stay in the acid solution might create undercut in the resist which appears as bubbles under resist. Figure 5.63 is the microscopic view of the test device which shows bubbles underneath the resist. This problem can be solved by using HMDS (adhesion promoter) before spinning the resist and post baking it. However, post baking has the disadvantage of creating round edges, but in this step, it is not critical.

Herein, the buffer layer and the anode contact are 1.5 μm and 0.5 μm thick, respectively. Therefore, in the device isolation step, 2 μm should be etched down which needs a quite long etching with the ICP tool. Since, during the etching of semiconductor, the photoresist mask also gets etched, three photoresists with different thicknesses have been tested. AZ 4533, SPR 220-3.0 and S 1813 with various thicknesses were selected. AZ 4533 has a thickness of 3.8 μm after spinning at 4000 rpm. SPR 220-3.0 was spined at 3000 rpm with an approximate final thickness of 2.3 μm. Photoresist S 1813 reached the thickness of 1.3 μm after spinning at 4000
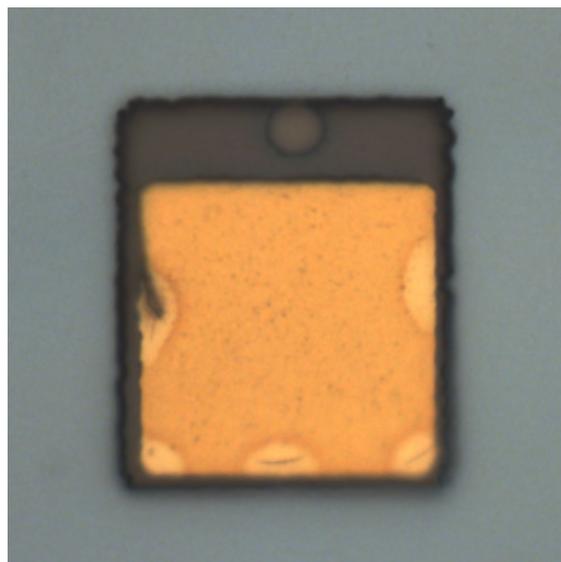
Figure 5.63: *The microscopic view of a test device after long time etching. The bubbles-like undercuts of the resist are evident.*

rpm. The AZ 4533 sample ended up to be the only sample with the resist mask left on top after the dry etching test of 2 μm depth. Figure 5.65 illustrates the SEM image of the diode after device isolation step.
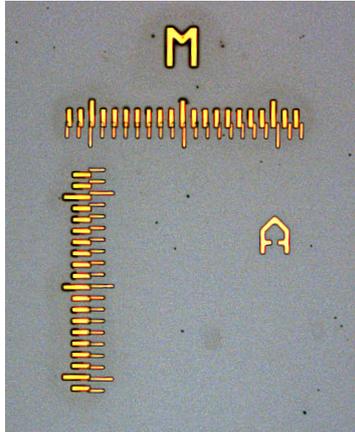
Figure 5.64: *The alignment marks which show a misalignment of 1 μm in x-direction.*
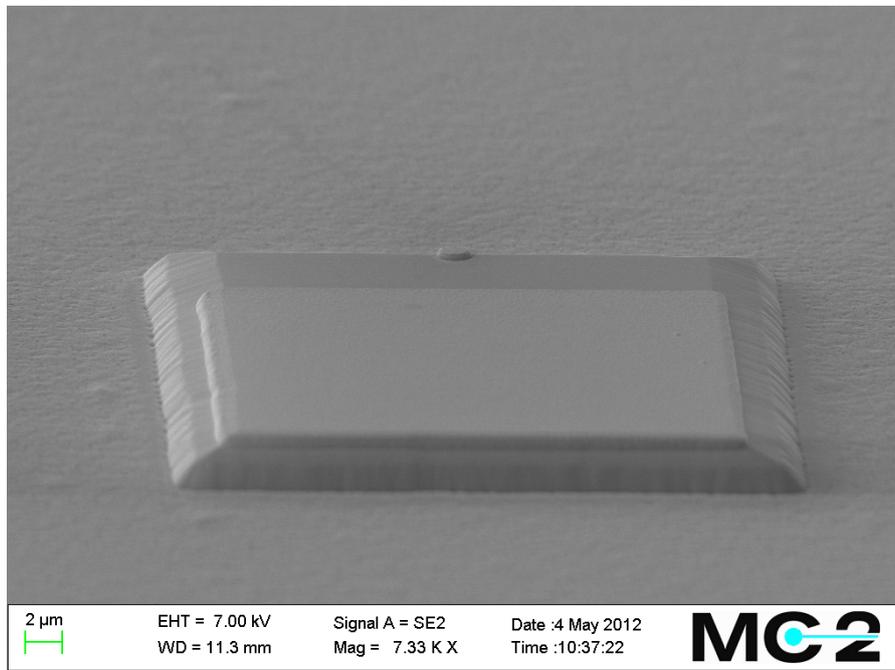
Figure 5.65: *The SEM image of the diode after device isolation step.*

5.1.4 Device Planarization

In order to fabricate metal interconnects for small area devices more reliably and provide more consistent device performance, device planarization is needed. Chemical vapor deposition (CVD) of dielectrics such as SiO_2 and SiN_x on the device is conformal. On the contrary, spin-on dielectrics such as Benzocyclobutene (BCB) with rather low dielectric constant of 2.5, can be used also as a planarization for the device. Good adhesion and low water absorption properties of BCB makes it a good candidate for metal interconnect technology.

BCB 4024-40 and 4026-46 with final measured thickness of 3.6 μm and 7.2 μm, respectively, have been tested. Before spinning the BCB, adhesion promoter AP300 should be applied. After spinning the BCB, the samples are soft baked at 85 °C. Prior to designing the photolithography mask, it should be noted that, BCB is like a negative tone resist. In this photolithography step, the vias for the anode contact and its pads are opened. To do so, after the exposure by UV, the sample is sit on the chuck with few drops of DS2100 developer on top and is dry spined after few minutes to avoid rinsing with water. In this step, great care must be taken to obtain clean openings on the anode contact for good adhesion of the metal interconnect. After the post develop bake, the diodes were hard cured at 260 °C for 60 minutes.

5.1.5 Dielectric Etching and Metal Interconnect

As shown in the Figure 5.62, the thickness of the BCB on the cathode contact is thinner. Accordingly, the top BCB is etched down to cathode contact by using reactive ion etching (RIE) with $CF_4 : O_2$ and ratio of 10 : 40 sccm at pressure of 50 mTorr and power of 25 W. BCB 4026-46 has the etch rate of approximately 130 nm/min. In this step, which is considered to be the most arduous step, the etch depth must be controlled carefully to prevent opening the sidewalls.

At the beginning, the height to be etched can roughly be estimated by the surface profiler. SEM is useful to determine whether the cathode contact is exposed when the remaining BCB on top is thin. It should be noted that the existence of BCB leads to charge collection on the surface. Hence, getting a decent image with SEM is impossible. A straightforward solution is to spin E-SPACER resist which has a high conductivity. E-SPACER is an aqueous solution which dissolves in water.

The total height of the cathode mesa relative to the substrate is approximately 2.5 μm. According to the conducted experiences with the two BCBs with different thicknesses, the BCB thickness should be slightly more than that of the mesas i.e. 2.5 μm. Since the thicker is the BCB, the more time is spent for plasma etching. This makes the BCB surface extremely rough and uneven. This could be due to the present particles in plasma chamber which act as a etch mask. This is evident in the the sample processed with BCB 4026-46, see Figure 5.66, 5.67 and 5.68. Also, Figure 5.69 and Figure 5.70 illustrate the tope view and side view of the device after the attempt for exposing the cathode contact. Still the "grass like" BCB is observable on the contact. Consequently, it is suggested that with diluting BCB 4024-40, less etching time is needed and better BCB surface can be achieved.
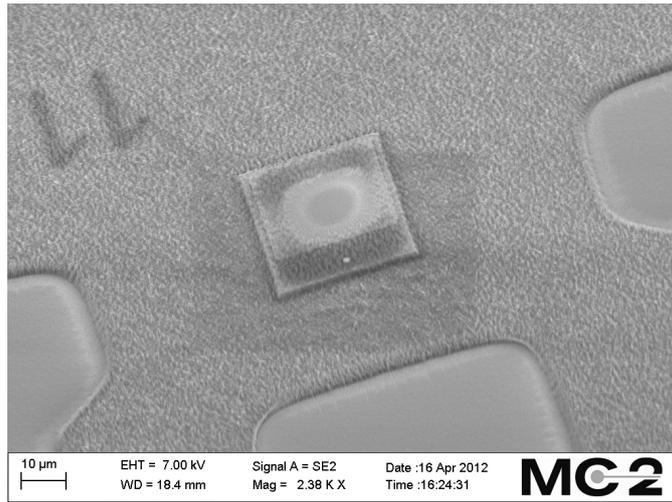
Figure 5.66: *The SEM image of a Sb-HBD and the pads with opened vias after partly etching the BCB.*
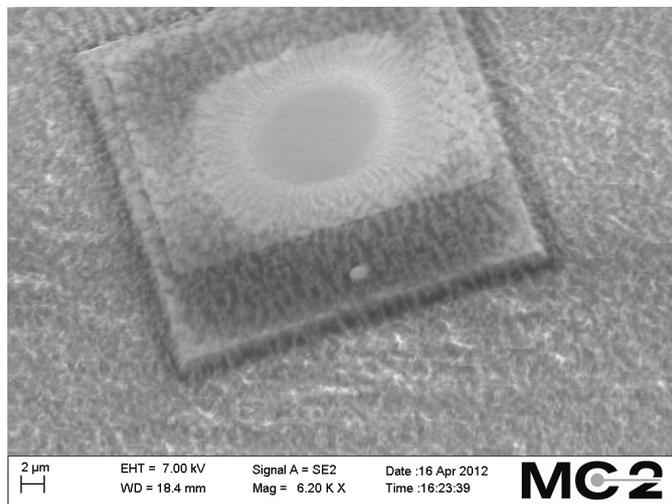
Figure 5.67: *The SEM picture of the Sb-HBD with very rough BCB surface resulting from long time plasma etching.*
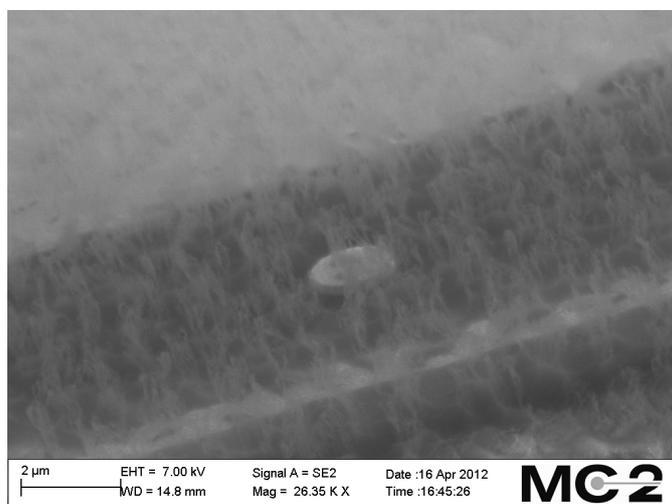
Figure 5.68: *A closer view of the Sb-HBD cathode contact and the rough texture of the etched BCB.*

The last step is to define the metal interconnect patterns. This can be realized by both optical lithography and e-beam lithography. According to the mask design for the interconnect fingers, the alignment accuracy should be within 500 nm. With this condition and having thick BCB on the sample surface, e-beam lithography is the appropriate tool. Therefore, the LOR 3A/UV5 resist stack is spined on the sample as mentioned in preparation of the sample for cathode contact formation, see section 5.1.1. In this step, because of relatively larger structures, e-beam process is faster than cathode formation step. Therefore, a bigger aperture (aperture 7) and higher current (10 nA) is used. Figure 5.71 shows the metal interconnect patterns after developing. Afterwards, the interconnect metal Ti/Au (20/200nm) is deposited using e-beam evaporation. Figure 5.72 is a microscopic view of the finished device.

Since BCB is somewhat uneven throughout the device, some of the cathodes are not exposed from BCB. This is apparent from the Figure 5.73 which compares the two cathodes. The cathode on the left side has also the color of the pads, which means there is still BCB left. The image of the right side is the cathode exposed from BCB, due to the observable color difference between the cathode and the pads.

Finally, Figure 5.74 and Figure 5.75 illustrate SEM image of the finished Sb-HBD. As can be seen in the Figure 5.75, the metal interconnect has very rough surface, due to the nonuniform surface of the bottom BCB.
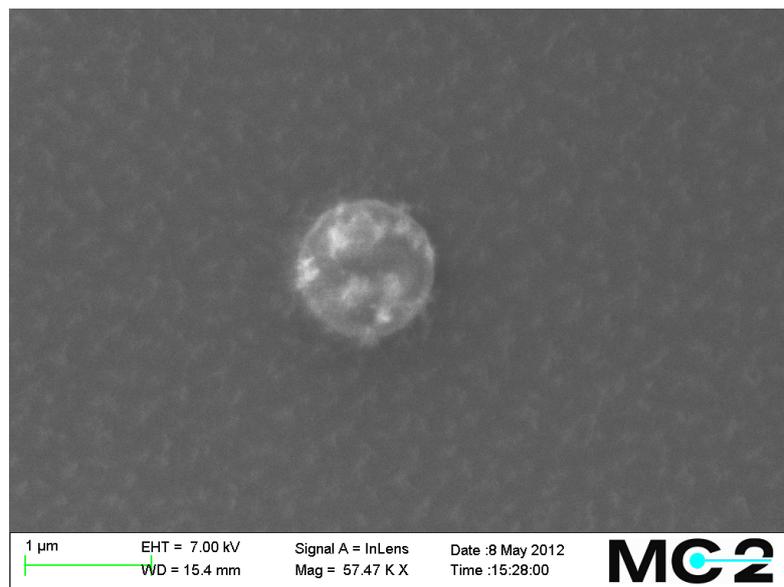
Figure 5.69: *The top view SEM image of a cathode contact with remaining BCB on top of it.*
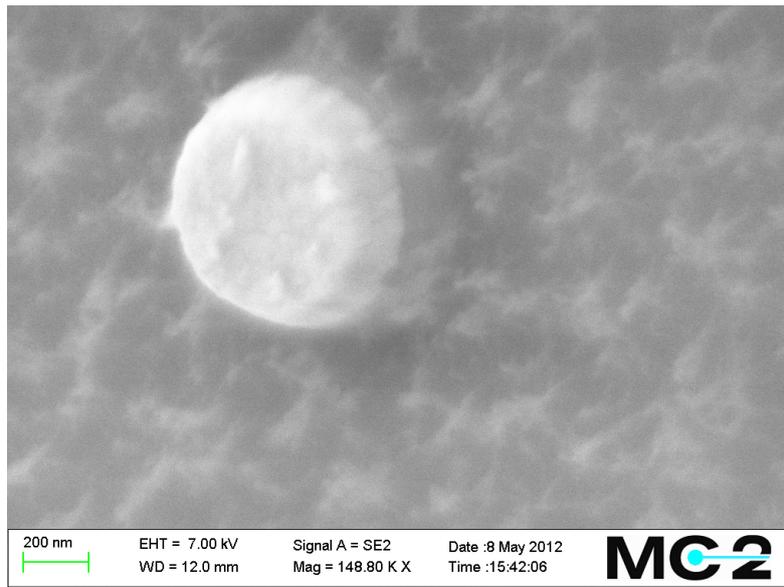
Figure 5.70: *A top-side view of the cathode contact showing the residual BCB on top.*
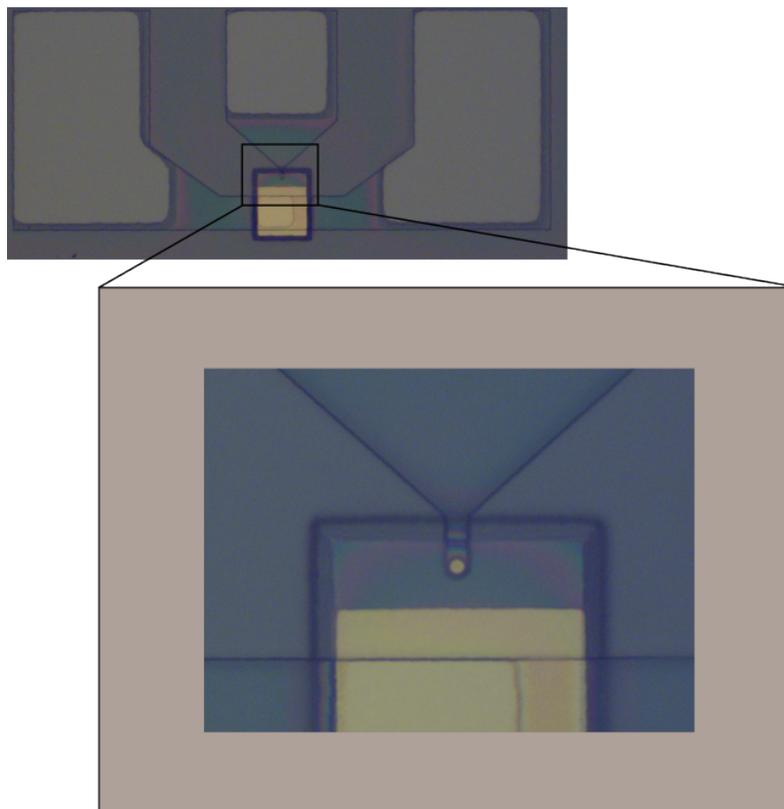
Figure 5.71: *The microscopic view of the Sb-HBD with developed metal interconnect patterns.*
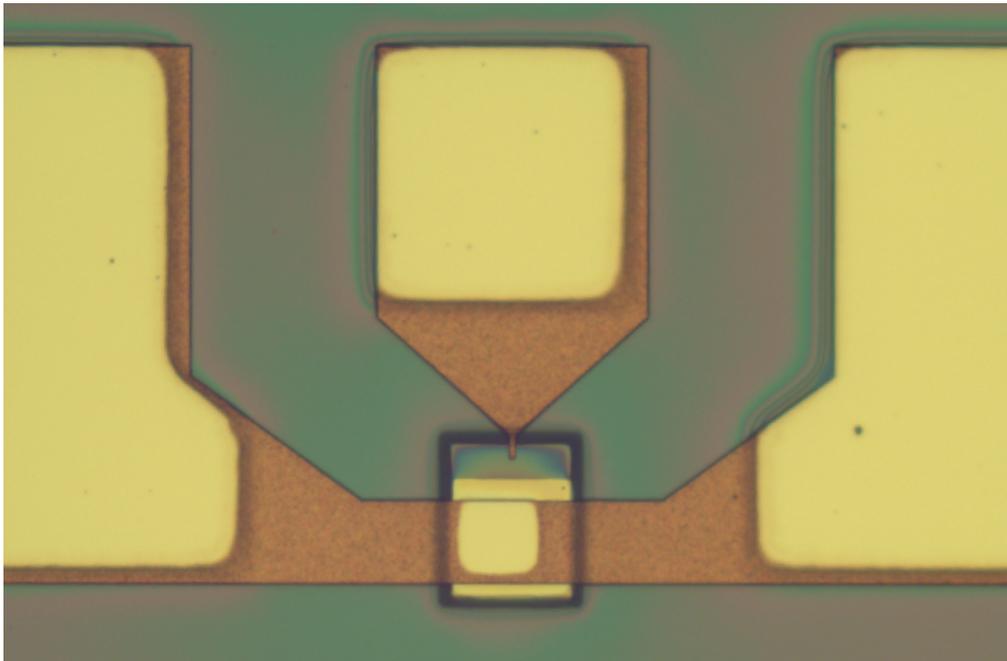
Figure 5.72: *A microscopic image of the finished Sb-HBD.*
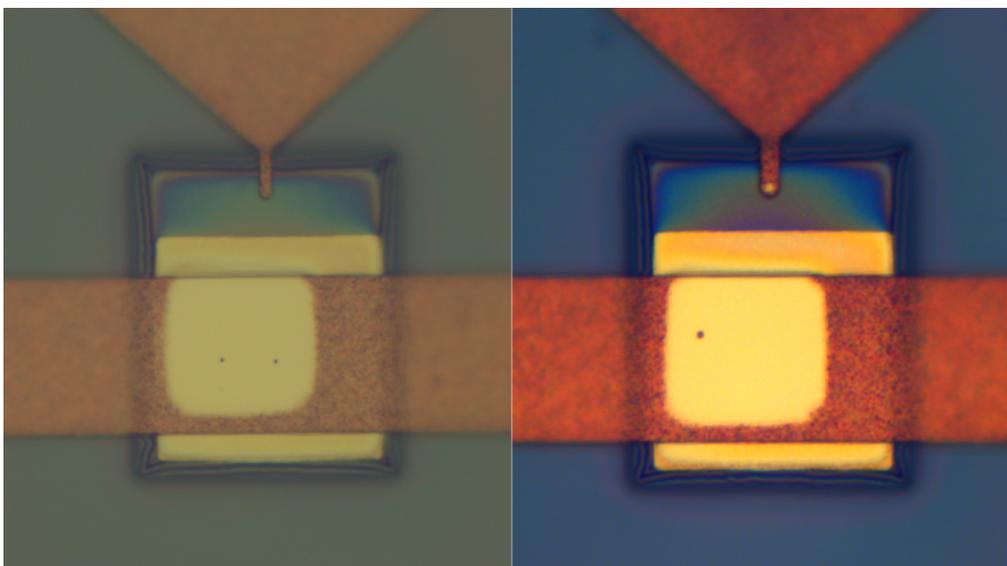
Figure 5.73: *The comparison of two finished devices with unexposed cathode (left image) and exposed cathode (right image).*
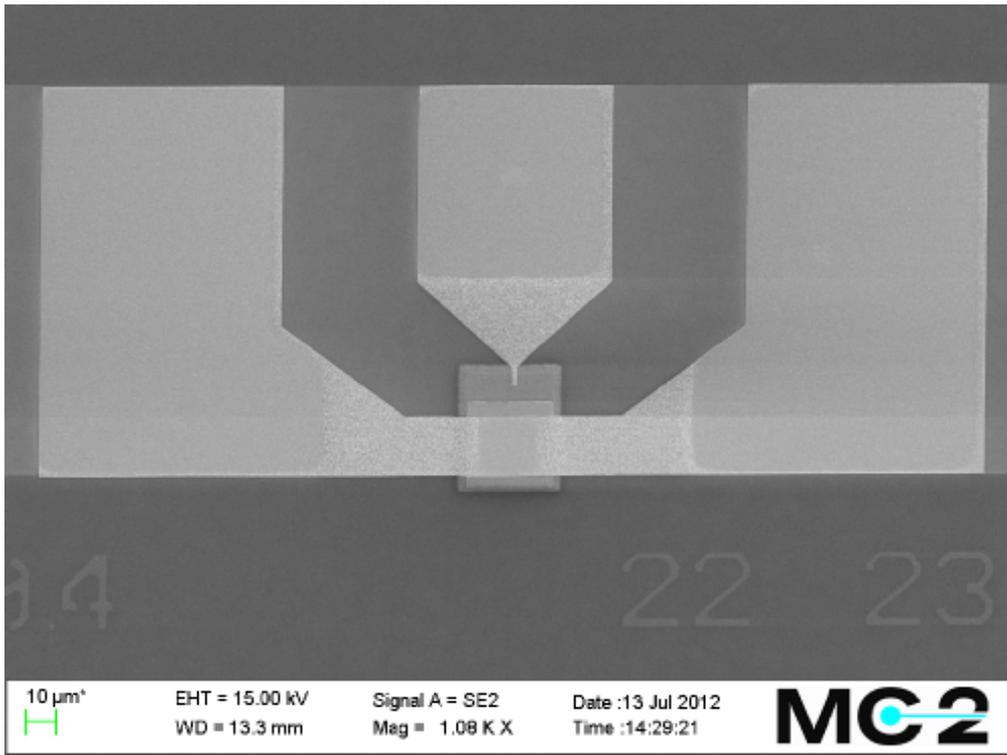
Figure 5.74: *The top view SEM image of a finished device.*
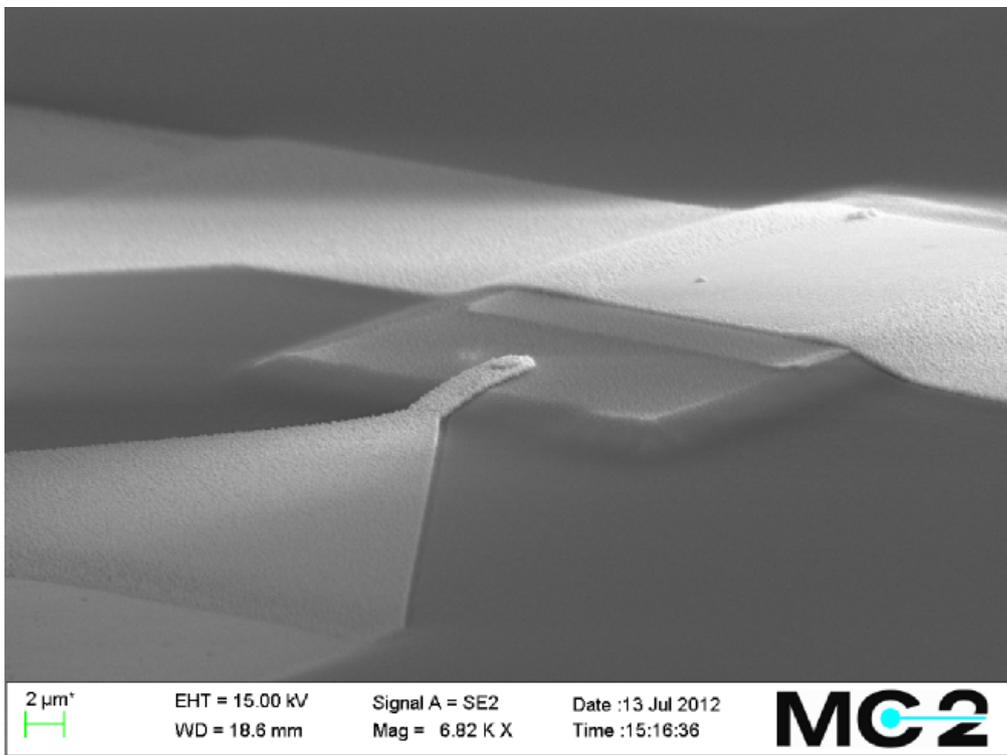
Figure 5.75: *The SEM image of a finished device. The metal interconnect with very rough surface is a result of nonuniform and "grass like" bottom BCB.*

Sample Cleaning:

2 minutes in acetone
2 minutes in isopropanol (IPA)   on hotplate
2 minutes in methanol

Mesa Definition:

e-beam resist LOR 3A/UV5 spinning
Soft Bake at 160°C for 5 min/ at 130°C for 2 min, respectively

After e-beam exposure:
Soft bake at 130°C for 90 seconds
Developed with MF 24A

Metal evaporation:

e-beam evaporation of Ti/Au/Ni (20/200/20 nm)

Lift-off in warm acetone

Mesa Formation:

Dry etch using ICP:
(RIE/CVD tool)
    RF power: 100 W
    ICP power: 150W
    Pressure: 2 mTorr

Figure 5.76: *Sb-Heterostructure backward diode Mask layers.*

Anode Contact (Image reversal methode):

Spin AZ5214
Soft bake at 110°C for 1 min
Frame exposure
Develop AZ351B:H2O 1:5   **+**   e-beam evaporation
Pattern exposure   of Ti/Au (20/200 nm)
Image reversal bake 120°C
Flood exposure

Lift-off in warm acetone

Device Isolation:

Device isolation definition:
Spinning AZ 4533
Soft bake at 110°C for 3 min
Frame exposure 2 min
Develop AZ351B:H2O 1:5
Pattern exposure 1 min
Develop AZ351B:H2O 1:5

Device Isolation Formation:

Dry etch using ICP:
(RIE/CVD tool)
     RF power: 100 W
     ICP power: 150W
     Pressure: 2 mTorr

Dielectric Passivation:

Spin AP3000
Spin BCB
Spin Dry
Removal of thick BCB in the corners

Figure 5.77: *Sb-Heterostructure backward diode Mask layers (continued).*

Vias Definition:

Soft bake 85˚C, 90 sec
Via pattern exposure 90 sec
Develop (developer DS2100) for 5 min
Post develop bake 90˚C, 60 sec

    +

Cathode Exposure:

Hard cure 260˚C, 60 min
Etch by RIE:
   .CF4:O2 (10:40) sccm
   .Pressure 50 mTorr
   .Power 25W
   .Controlling depth by SEM
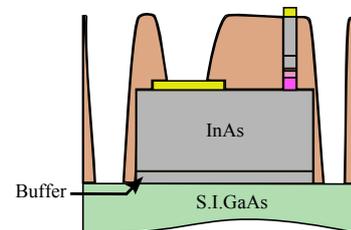
Metal Interconnect Definition and Formation:
e-beam resist LOR 3A/UV5 spinning
Soft bake at 160˚C for 5 min/ at 130˚C for 2 min, respectively

After e-beam exposure:
Soft bake at 130˚C for 90 seconds
Developed with MF 24A
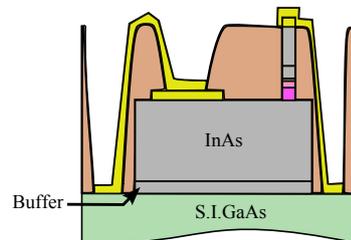
Figure 5.78: *Sb-Heterostructure backward diode Mask layers(continued).*

5.1.6 Discussion

In the measurement of the sub-micron devices a high leakage current was observed in the I-V characteristics. This high leakage current can be first attributed to the material quality. For instance, in some samples there existed holes with few tenth of a micron diameter which in some cases were comparable with the cathode contact sizes. Secondly, this might be due to the surface current induced by the rough surface of the side walls of the mesa after dry etching.

To further investigate the reasoning behind this high leakage current, Focused Ion Beam-Scanning Electron Microscopy (FIB-SEM) is applied for the device. Figure 5.79 and Figure 5.80 show the FIB-SEM image of a diode. As seen in Figure 5.80, there exists something in between the metal interconnect and the top metal layer on the mesa. This can be the residual BCB still left on the top of the contact.

On the other hand, as it is discussed before, the height of the uneven BCB is extremely difficult to control. Therefore, in some diodes throughout the chip, BCB might be etched too much that the later evaporated metal could short the mesa.
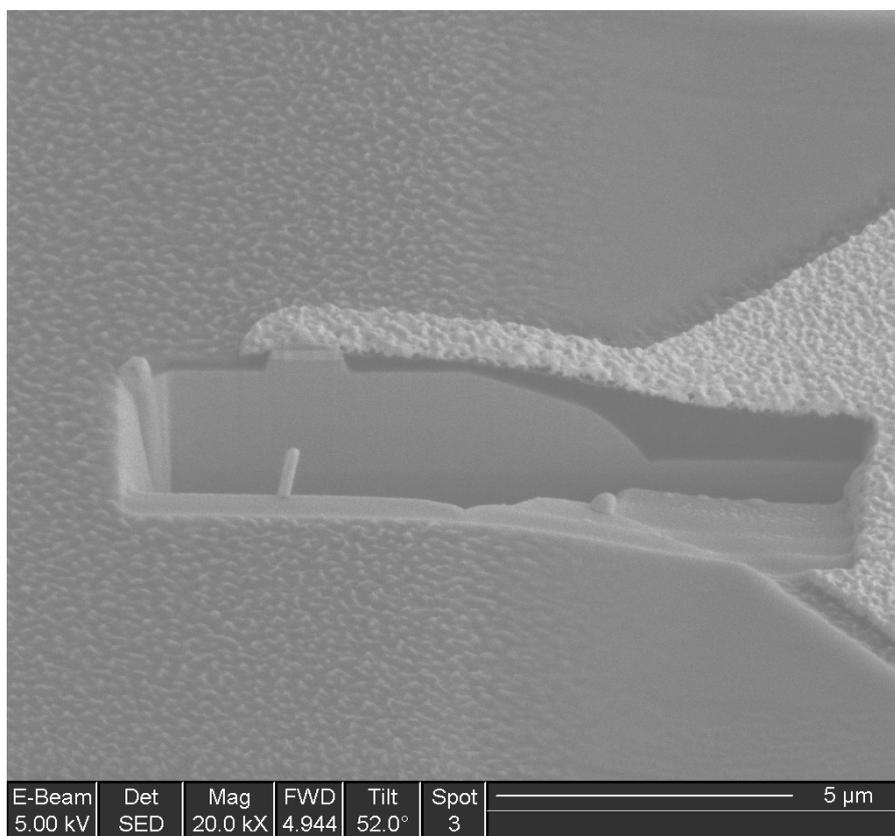
Figure 5.79: *The FIB-SEM image of the Sb-HBD.*

E-Beam	Det	Mag	FWD	Tilt	Spot		2 µm
5.00 kV	SED	50.0 kX	4.948	52.0°	3		
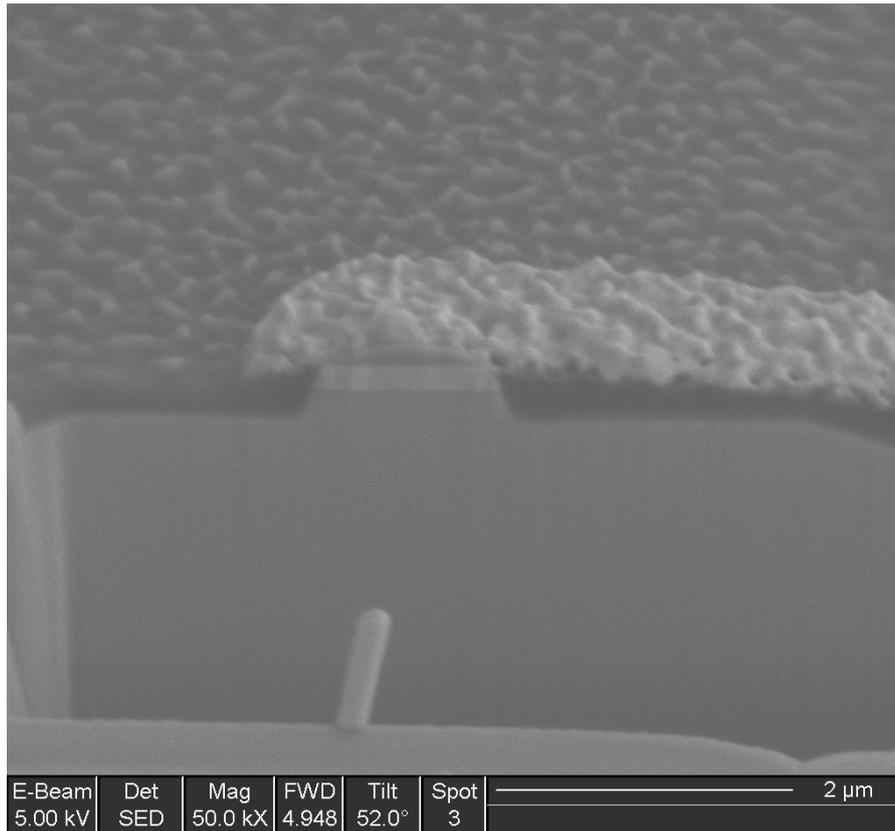
Figure 5.80: *A closer look in the FIB-SEM image of the Sb-HBD*

5.2 Test Diode Fabrication

The material structure for the backward diodes was grown with Molecular Beam Epitaxy (MBE) growth method in Chalmers Nanofabrication Labratory. In order to investigate the effect of substrate material, the InAs/AlSb interface bonding type and the buffer thickness on the Sb-HBD's performance, test diodes were developed prior to the sub-micron device fabrication. Also, these diodes were fabricated to observe the effect of various barrier widths and Al mole fraction.

The fabrication of the test diodes consists of three mask layers and totally six process steps, see Figure 5.82 and 5.83. The first step is defining the cathode pattern with positive photoresist Shipely S1813. Then the mesa is formed using ICP tool, by etching down to the InAs contact layer. Photoresist S1813 is considered as the mask layer. In order to prevent heating up the sample which leads to burnt resist, dry etching was performed in several steps with wait sequences. Figure 5.81 presents three examples of burnt resist after 90 seconds of continued etch.

The cathode contact formation is defined by photolithography using image reversal method. In this step the positive photo resist, AZ5214E is changed to negative tone resist to create the lift-off profile. Then, Ti/Au (20nm/200nm) is deposited on the sample using e-beam evaporation tool. Later on, the lift-off step is done by putting the samples in warm acetone. The pattern definition and contact formation for
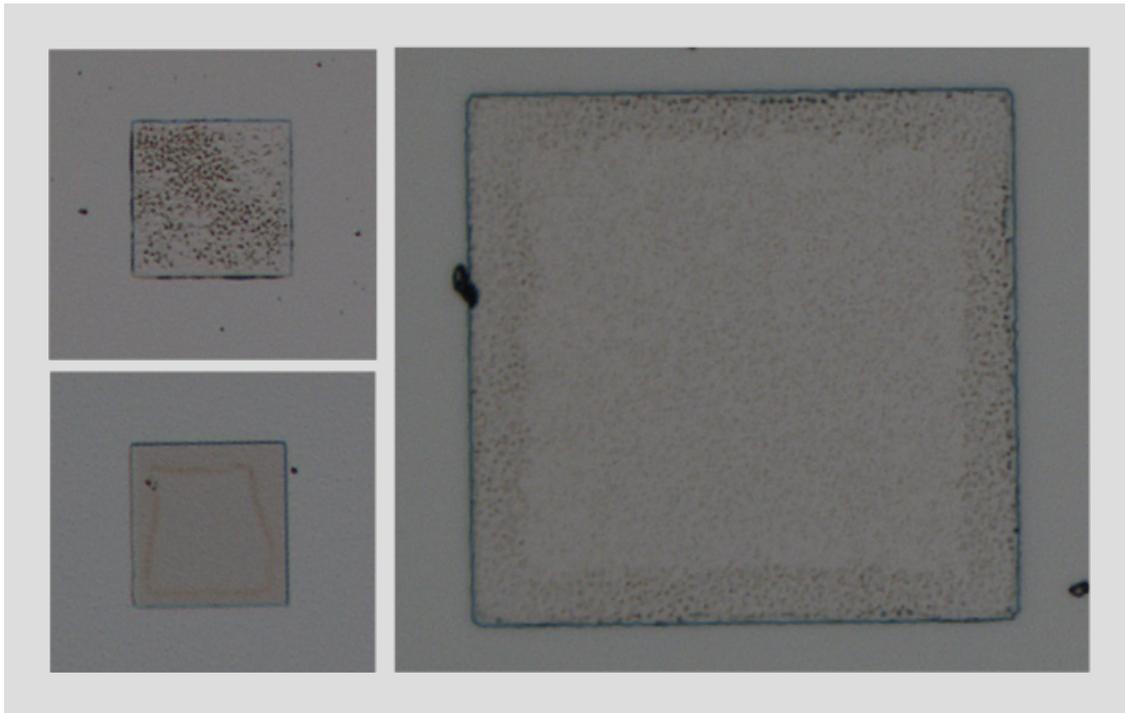
Figure 5.81: *Shows the burnt resist after long time etch.*

anode is also done similar to cathode's.

Sample Cleaning:

2 minutes in acetone
2 minutes in isopropanol (IPA)   on hotplate
2 minutes in methanol

Cathode Pattern Definition:

Spin photoresist S 1813
Softbake at 110˚C for 2 min
Expose with optical lithography
Develope in MF 319

Mesa Formation:

Dry etch using ICP:
(RIE/CVD tool)
    RF Power: 100 W
    ICP Power: 150W
    Pressure: 2 mTorr

Remove Photoresist and Clean the Sample:

2 minutes in acetone
2 minutes in isopropanol (IPA)   on hotplate
2 minutes in methanol

Cathode Contact Definition:

Spin AZ 5214E
Softbake at 110˚C
Frame exposure and Develop in AZ351B:H2O 1:5
Pattern exposure
post exposure bake 120˚C
Flood exposure
Develop in AZ351B:H2O 1:5

Figure 5.82: *Sb-HBD's test diode fabrication process.*

Metal evaporation:

e-beam evaporation of Ti/Au (20/200 nm)

InAs
AlGaSb
GaSb
AlSb
InAs
Buffer
S.I.GaAs

Lift-off in warm acetone

InAs
AlGaSb
GaSb
AlSb
InAs
Buffer
S.I.GaAs

Lift-off Pattern Using Image Reversal Method:

Spin AZ 5214E
Softbake at 110˚C
Frame exposure and Develop in AZ351B:H2O 1:5
Pattern exposure
post exposure bake 120˚C
Flood exposure
Develop in AZ351B:H2O 1:5

InAs
AlGaSb
GaSb
AlSb
InAs
Buffer
S.I.GaAs

Metal evaporation:

e-beam evaporation of Ti/Au (20/200 nm)

InAs
AlGaSb
GaSb
AlSb
InAs
Buffer
S.I.GaAs

Lift-off in warm acetone

InAs
AlGaSb
GaSb
AlSb
InAs
Buffer
S.I.GaAs

Figure 5.83: *Sb-HBD's test diode fabrication process (continued).*

6 Conclusion and Future Work

In this thesis, device modelling, material growth characterisation and fabrication of the Sb-HBDs are carried out.

In the simulation part, the 2-D device modelling of Sb-HBDs is done by Synopsys TCAD simulator. The model is verified by comparing the simulated I-V characteristics with the experimental results. Curvature coefficient and junction resistance which are considered the two most critical device parameters were simulated with different heterostructures and device geometries. In this part, the following conclusions can be drawn:

- The obtained simulation results exhibited good agreement with the experimental results using the WKB approximation for tunnelling current calculation. The simulation results give an insight into further optimisation of the device performance. For instance, the results indicate that the lower is the InAs n-doping concentration, the higher is the curvature coefficient. However, this also leads to a gradual increase in junction resistance.

- The simulation results shows strong sensitivity of the diode's performance on the doping profiles and lateral and vertical scalings.

- In order to further optimise the device performance in terms of its desired I-V characteristics, more effort can be put into band engineering of the device. For example, other materials with interesting properties can be employed to bring the InAs conduction band closer to Fermi level so that higher curvature coefficient with a steady junction resistance can be achieved. Furthermore, by new device structures that lower series resistance and junction capacitance, sub-millimetre wave operation of the device can be realized. However, in our simulation results for terahertz frequencies, the voltage sensitivity drops, which indicates the requirement of a Low Noise Apmlifier (LNA).

In the material optimisation part, the effect of various buffer thicknesses and different interfacial bonding construction (either AlAs-like or InSb-like) on device performance are investigated. The test diodes were fabricated and the DC characterisation was carried out. The results from TEM inspections and temperature-dependant I-V characteristics are discussed.

- Al-As IF bonding is favorable in Sb-HBDs, since it results in higher curvature coefficient. However, for the case of Sb-HEMTs, Al-As IF bonding is not suitable, due to introducing defects in the channel.

- Thick buffer thickness increases the curvature coefficient and results in better material quality (more uniformity in the surface).

- For the future work, dislocation blocking techniques should be further explored.

In the fabrication part, processing techniques for sub-micron scale Sb-HBDs are developed. The fabrication process was done using a mix-and-match technique in Chalmers nanofabrication laboratory. The cathode contact formation was defined using e-beam lithography for diodes with mesas down to 300 nm diameter. As for the anode contact and the device isolation the optical lithography was employed. In the development of sub-micron scale Sb-HBDs, the following conclusions are drawn:

- In this work, the dry etching technique is used for the formation of the heterostructure mesa. According to the SEM images of the cathode mesa, the sidewalls have slightly rough surface.

- The passivation of the device is done using spin-on dielectric BCB film.

- In future, more investigation of the appropriate dry etching recipes and surface treatment techniques can be done to reduce the carrier surface recombination. Also, further investigation of the passivation methods and the metal interconnect technology is suggested.

In summary, Sb-HBDs have been proven to be promising candidates for direct detection and imaging in the W-band [36]. Further study of the underlying physics of the device and modelling in the terahertz regime is suggested. The material properties and the growth techniques using MBE can be further optimized. Moreover, for terahertz imaging applications there is a need for more sensitive detectors. This can be realized by monolithic growth and fabrication of highly sensitive Sb-HBD and InAs/AlSb HEMT, resulting in a compact receiver with improved sensitivity.

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Paper A

Modeling of Sb-Heterostructure Backward Diodes for Millimetre-Wave Detection

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Modeling of Sb-Heterostructure Backward Diodes for Millimeter-wave Detection

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Abstract

Millimeter-wave detection has drawn considerable interest, due to its less atmospheric attenuation compared to the infrared detection and possibility to penetrate into clothing and building material [1]. Superconducting bolometers and semiconductor based detectors are conventionally used for millimeter-wave detection [2]. However, semiconductor detectors are advantageous over superconducting bolometers considering the possibility for higher integration level and batch processing.

Semiconductor diode detectors benefit from simplified structure and elimination of external bias circuitry. This also leads to reduction of shot noise and low frequency noise. Such diode detectors are often implemented with planar-doped barrier (PDB) diodes, Schottky diodes and Esaki diodes. Reliable and reproducible PDB diodes are difficult to produce. While zero biased Schottky diodes exhibit strong temperature dependence, Esaki diodes are more robust against temperature variation. However, achieving high sensitivity in Esaki diodes is accompanied by a limited dynamic range [3].

Backward diode has a similar operation principle as the Esaki diode, where the current is manipulated by interband tunneling between adjacent energetically offset semiconductor regions. Sb-heterostructure diodes are very promising devices for backward diode millimeter wave detectors due to the large band gap difference between InAs and AlSb that offers great flexibility for band gap engineering [3]. The composition of the $Al_xGa_{1-x}Sb$ layer and the doping concentration in the n-InAs and p-GaSb layers can be adjusted to make the Fermi level lie in the conduction band of n-InAs and near the valence band edge of the $Al_xGa_{1-x}Sb$ layer [4]. This band alignment favors the backward current through electrons tunneling from p-GaSb to n-InAs, but blocks the forward current via electrons tunneling from n-InAs to p-GaSb. This asymmetry in the current flow in combination with a strong non-linearity at zero bias in the I-V characteristics makes it suitable for square-law rectification.

In this work, Sb-Heterostructure backward diodes are simulated using the device simulation tool Sentaurus TCAD. Fig.1 shows schematic diagram of a typical Sb-heterostructure backward diode and the corresponding energy band diagram from self-consistent solutions to Poisson and Schrödinger equations. Herein, the barrier thickness, composition of $Al_xGa_{1-x}Sb$ as well as the doping profile has been optimized to improve noise equivalent power (NEP). We will present comparisons of simulation results with experimental data to verify the model. In addition, novel device structures are proposed considering the feasibility of the growth technique.
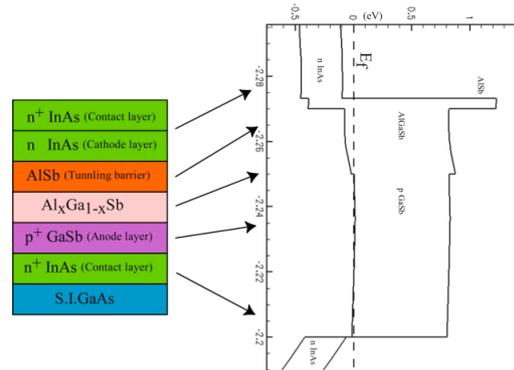

Fig1: Schematic of a typical Sb-heterostructure backward diode and the energy band diagram

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Paper B

Modeling of Sb-Heterostructure Backward Diode for Millimeter- and Submillimeter- Wave Detection

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Modeling of Sb-Heterostructure Backward Diode for Millimeter- and Submillimeter-Wave Detection

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Abstract:

Millimeter wave and submillimeter wave detection and imaging have attracted considerable interest due to its potential in applications such as security, defense, and medical diagnosis. For such sensing and imaging systems, highly sensitive and compact solid-state detectors are the key components. Among the various existing device technologies, the antimonide based heterojunction backward tunneling diodes (HBDs) has been demonstrated as one of the most sensitive millimeter wave direct detectors [1]. These diodes exhibit especially high curvature in the current-voltage characteristic that produces the rectification without bias. Operation without bias is a highly disable feature as the device does not suffer from large *1/f* noise, a major shortcoming in other devices such as Schottky barrier diodes or resistive room temperature bolometers. HBDs with matched sensitivity as high as 50 kV/W and noise equivalent power below 0.2 pW/Hz$^{1/2}$ have been demonstrated at 94 GHz, exceeding the theoretical prediction of Schottky diodes [2]. Though Sb-HBDs were predicted very promising for submillimeter wave applications as well, little effort has been made and few have reported on its operation above 100 GHz. To improve both the performance and the operation frequency, device modeling of HBDs is strongly needed for guidance of future detector heterostructure design.

In this work, Sb-HBDs are simulated using the Sentaurus device simulator of Synopsys Technology Computer-Aided Design (TCAD) [3], which capable of 3D simulating electrical, thermal, and optical characteristics of compound semiconductor devices. Fig.1 shows epitaxial structure of a typical Sb-HBD and the corresponding energy band diagram from self-consistent solution to Poisson and Schrödinger equations. The working principle of the HBDs can be found in [1]. For the device simulation, a non-local band to band tunneling model in the appearance of hetero-interfaces has been combined with the standard drift-diffusion equations. Both direct and indirect bandgap tunneling at the InAs/AlSb interface have been considered in comparison of experimental results. Fig.2 shows the simulated I-V curves near zero bias. Critical device parameters for detector performance such as curvature coefficient and junction resistance were simulated with different heterostructures and device geometries, and good agreement with experiment results has been obtained. The sensitivities as a function of operating frequency are also presented, see Fig.3. Proper device structures enabling submillimeter wave operation will be proposed.

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|		
InAs	n++	1000 Å
InAs	n	500 Å
AlSb	undoped	11Å
Al $_{0.1}$GaSb	undoped	150 Å
p-GaSb	p++	300 Å
n+InAs	n++	10000 Å
GaAs	semi-insulating	substrate
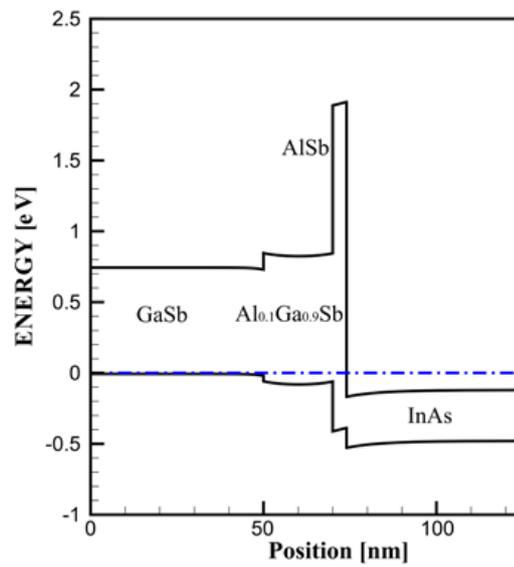
Fig.1 Epitaxial structure of a typical Sb-HBD and the corresponding energy band diagram
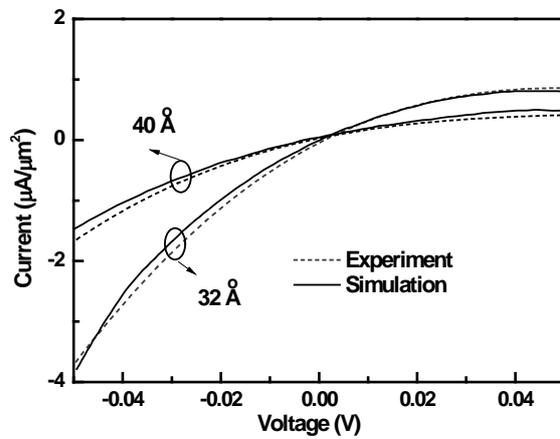
Fig.2 Simulated I-V curves of Sb-HBDs near zero bias, which agrees very well with experimental measurements
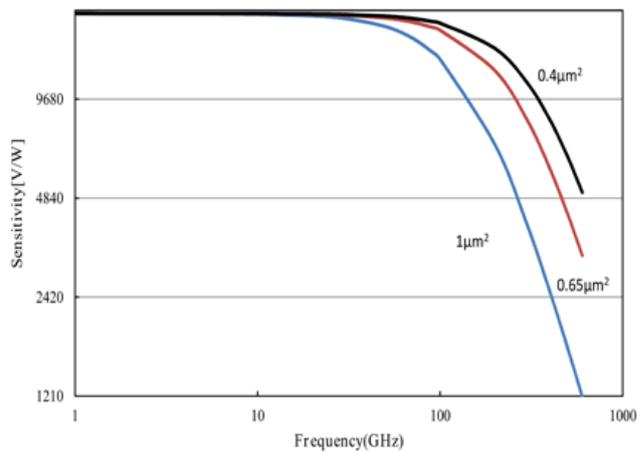
Fig.3 Sensitivity of Sb-HBDs with different sizes as a function of frequency

B - 2