On Regularity and Integrated DFM Metrics

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***Abstract*—Transistor geometries are well into the nanometer regime, keeping with Moore's Law. With this scaling in geometry, problems not significant in the larger geometries have come to the fore. These problems, collectively termed variability, stem from second-order effects due to the small geometries themselves and engineering limitations in creating the small geometries. The engineering obstacles have a few solutions which are yet to be widely adopted due to cost limitations in deploying them. Addressing and mitigating variability due to second-order effects comes largely under the purview of device engineers and to a smaller extent, design practices. Passive layout measures that ease these manufacturing limitations by regularizing the different layout pitches have been explored in the past. However, the question of the best design practice to combat systematic variations is still open. In this work we explore considerations for the regular layout of the exclusive-OR gate, the half-adder and full-adder cells implemented with varying degrees of regularity. Tradeoffs like complete interconnect unidirectionality, and the inevitable introduction of vias are qualitatively analyzed and some factors affecting the analysis are presented. Finally, results from the Calibre Critical Feature Analysis (CFA) of the cells are used to evaluate the qualitative analysis.**

I. Introduction

Transistor geometries have been scaling more or less in line with Moore's Law [1] for the past four decades. This push towards smaller geometries has been fueled by a demand for compact, efficient and high-performance electronics. The cost of mitigating variability, however, has been rising with the shrinking geometries. On the device side, a number of innovative material choices have reined in the leakage power significantly [2]. The 45-nm process from Intel [3], [4] introduced hafnium-based compounds as high-k dielectrics in combination with a metal gate. This results in a number of benefits, chiefly, lower leakage current in the device.

The engineering side of the problem—creating patterns in very small geometries—remains and is creating an increasing number of problems as scaling continues. A number of complex, cost-intensive remedial steps such as double patterning and immersion lithography have been adopted to enhance patterning fidelity. Techniques like Optical Proximity Correction (OPC) and unconventional illumination are widely adopted today to assist resolution enhancement and mitigate effects related to the lithography process such as Line Edge Roughness (LER) and Across-the-Chip Linewidth Variation (ACLV). Fig. 1 shows the cost of ownership of a 5,000 wafer lithography run, highlighting the rapidly increasing mask costs to obtain high image fidelity. According to the 2009 ITRS report on lithography trends [5], for each reduction of the technology node, the mask contents typically grow by a factor of 2. However, in order to accommodate the OPC corrections to achieve pattern creation using current technologies, the data growth per node has been expanding at a historical data growth rate of 2.7x per node over the last 8 years rather than the 2x that would be expected.

Newer lithography techniques using Extreme Ultra Violet (EUV) light have been proven in controlled settings but suffer from problems related to reliable light sources. In addition, the cost of deployment has proven to be a hurdle to widespread adoption [5].

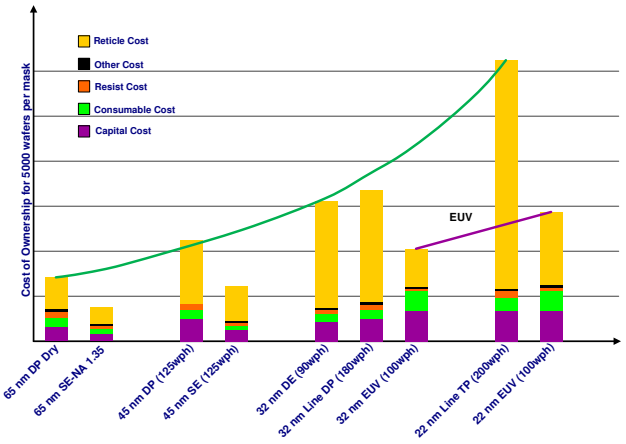

Fig. 1: Relative cost of ownership of a $5,000$ wafer run device (reproduced from [5]).

Regular layout structures adopted in creating nanometer patterns have long been studied and prescribed to limit the effect of current engineering limitations thereby reining in variability. Here, we study the implied benefits of layout regularity on the manufacturability. The connection between layout choices and manufacturability, tenuous at best, are qualitatively explored.

The rest of this paper is organized as follows: an extensive background detailing the taxonomy of variability and related work are presented in Sec. II; Sec. III explains the classes of regularity explored in this work and the layout measure that are used to implement such circuits; Sec. IV details these measures as applied to the cells considered in this study. Finally, the results of the Critical Feature Analysis are presented in Sec. V and we will conclude the paper with a summary (Sec. VI) of the work and a discussion about the results along with some thoughts about future work.

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II. Background

In general, there is an area overhead to adopting a high degree of regularity in the layout of more complex cells. Creation of these cells using current design rule checks (DRCs) suffer from this shortcoming, since these rules must be respected in order to create the regular devices in the first place. We use complex cells here to refer to cells not belonging to the family of basic boolean functions. Strictly, functions that cannot be implemented in a single stage using CMOS technology will likely suffer an area overhead when constraints related to regularity are imposed.

We adopt a structured approach to the background material by briefly looking into the sources of variability and describing the notions of regularity in literature.

A. Variability Taxonomy

Traditionally, variability analysis has fallen under two categories. Front-End-Of-the-Line (FEOL) variability refers to variability arising out of defects in the device creation steps of fabrication, while Back-End-Of-the-Line (BEOL) variability refers to the variability in the interconnect creation process [6], [7]. Lithography is a dominant source for FEOL variability while Chemical-and-Mechanical Polishing (CMP), used to planarize the metal used in interconnect at different levels, is the major contributor to BEOL variability. While interconnect variability has not been dominant in the past, it is becoming increasingly important as the devices scale and their delays become smaller.

FEOL variability affects device performance. Fundamental device variability is displayed in threshold voltage variation, oxide thickness variation, energy level quantization and Line Edge Roughness (LER). The first three are random in nature since they depend upon the number and placement of dopant atoms. LER, the variation of the gate length along the width of the channel, however, is largely dependent on the photolithography process used to create these features. Since the transistor leakage current has an exponential dependence on the gate length, the impact of LER on device performance is tremendous. This power limitation leads to large yield losses, since it occurs in high frequency bins which are also the most profit generating bins. Another width variation which occurs is the device width variation. However, width variation impacts device performance most at minimum width, when variations such as corner rounding reduce the effective transistor width [6], [7].

An associated term used by lithographers to describe the gate length is the Critical Dimension (CD), which can be associated with lithographic parameters by:

$$CD = k_1 \frac{\lambda}{NA}$$

where λ is the wavelength of the lithography light source, NA is the numerical aperture of the optical system and k_1 is a process dependent parameter which is a measure of lithographic aggressiveness [6]. This value is between 0.5 and 0.25 for current technologies. The wavelength used in current lithographic processes is 193 nm and the numerical aperture is between 0.93 and 1.35 for the latest patterning and lithography techniques. NA improves if lithography occurs through a medium that has a higher refractive index than that of air (refractive index 1). Lithography performed under water (refractive index 1.44), called immersion lithography, increases NA above one thereby reducing CD. Thus with extremely aggressive lithography techniques, it is still possible, at considerable expense, to pattern features of the order of 35 nm. With increasing NA (of around 1.65) and double patterning (reducing k_1) it is possible to further reduce the resolution to about 22 nm.

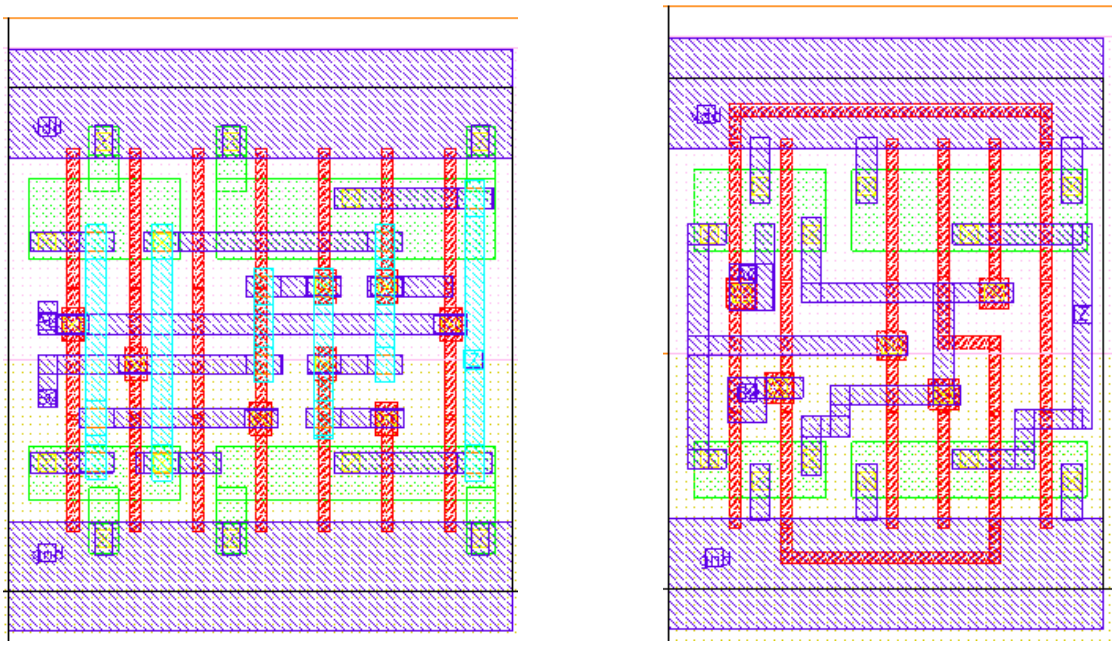
BEOL variability contributes directly to variation in interconnect thickness and indirectly to variation in interconnect width. Since imperfections in the CMP process cause planar defects, the lithography steps in multi-level interconnect are also affected. The insulating layer reliability is also of concern in these steps. These effects can cause large variations in the interconnect resistance and capacitance making it more difficult to model these effects and correct for them at the physical design stage. Vias and contacts present at both FEOL and BEOL stages are often cited as being concerns for reliability. These fixed geometry structures are etch dependent and also require CMP steps to complete, making them more prone to defects.

B. Notions of Regularity

Regularity has been studied from different viewpoints since the 1990s. Kutzenbausch et al. considered the extraction of regularity at the logic synthesis stage [8]. They applied regularity in conjunction with a driver-transform concept using global information to guide local transformation. The conclusion of the paper points to symmetric decomposition as a possibly important addition to extracting structural regularity. In earlier work [9], [10] we have explored regularity at this level of abstraction for arithmetic circuits and found that while the results were encouraging, imposing a high degree of regularity results in routing congestion and increased wire length.

Work carried out by Menezes et al. propose regular layouts based on a single type of cell to investigate the effects of regularity [11], [12]. Using a custom synthesis tool, they show results indicating an improvement of delay at the expense of area and wire length. Lin et al. propose a transistor-level high-density layout generator for regular circuits based on Vertical Slit Field Effect Transistors (VeSFETs) [13]. The scope of this generator is limited to circuits with a few tens of transistors; however, the work also considers routing. In our work so far, cell creation is done manually and the methods described in [13] could prove useful in the future. The underlying fabric is based on a different technology but the principles should be applicable to regular cell creation. Dal Bem et al. have proposed lithography-aware regular layouts based on Via Configurable Transistor Arrays (VCTA) [14], [15]; however, the impact on area due to the DRCs is large. Subramaniam et al. have proposed a scheme involving optimization of the design rule deck [16]. Their results indicate savings on leakage power without detrimental effects to performance.

Talalay et al. propose an approach to designing regular logic



(a) Ultra-regular cell layout **(b) Semi-regular cell layout**

Fig. 2: Custom-characterized XOR gates.

blocks using pre-generated layout templates [17]. Their study also proposes a possible definition for repeatable block and switch transistor logic model to describe functionality. This will be important when automated means for managing layout complexity at small geometries are desired. Similar to this effort Ryzhenko et al. propose extremely regular diffusion structures extending the so-called Lithographers Dream Pattern paradigm [18]. Their results, carried out in the more advanced 32-nm node, feature automatic cell synthesis onto the regular fabric and propose simultaneous cell synthesis and metal1 routing resulting in area advantages. Their work, however, incurs a small leakage penalty.

In, by far, the most comprehensive coverage of regular fabrics, Javheri et al. showcase different strategies at implementing regular fabrics [19]. Their work, based on a methodology of co-optimization, proposes the use of logic bricks to implement commonly occurring logic functions in the design. Other co-optimization techniques to significantly reduce the area impact in a wider design context are also proposed. Their results indicate that adopting regularity has no significant impact on circuit performance either. However, co-optimization requires support from the foundry and predictive assessment has not been possible in any other simplified form. The work by Javheri et al. has been inspired by the highly dense and regular SRAM cells. The styles and the associated restrictions of the SRAM cells have also been migrated to logic layouts.

III. Ultra-Regular and Semi-Regular Layouts

Ultra-regular layouts, as presented in this work, refer to layouts in which, in addition to maintaining a single device orientation and constant poly pitch, the directions of the local routing resources are also fixed. Widths and spacings for the layout geometries in a semi-regular layout are held as constant as allowed by area constraints but minor deviations are allowed. Poly pitch is constant across devices with multiple fingers, but routing in poly is allowed. The local routing resources are constrained in the number of layers used, but not the direction.

While it is relatively easy to implement these constraints for simple two input cells at no impact to the area, it becomes increasingly difficult to do so when the complexity of the cell grows either in terms of the number of inputs or the number of devices or both.

In order to analyze the tradeoffs involved in implementing regular layouts, with little or no impact on area (and performance too) in a larger design context, it was necessary to create standard cells with regular geometries. A basic set of eight logically complete combinational cells have been created using a commercial 65-nm process. These cells are listed in Table I and compared in terms of width to a comparable library cell. The library cells listed, especially the more complex cells, are chosen based on device sizing and performance, leading to some additional difference in the widths. Only the XOR, HA and FA are optimized completely for width. The other cells can be boundary optimized further. The label in the parentheses, under the cell functionality column, will henceforth be used to describe the cells. Fig. 2 shows the ultra-regular and semi-regular implementations of an AOI-based two input XOR gate. In order to focus the design effort, it was decided to implement only combinational cells, which form the bulk of most digital implementations. It should be recognized here that a number of standard cell parameters, such as cell height and width, are greatly influenced by the routing requirements for sequential

TABLE I: Custom characterized cells.

Cell Functionality	Width (μm)		
	Ultra-regular	Semi-regular	Library
And (AND)	1.6	1.4	1.0
Buffer (BUF)	1.0	1.0	0.8
Inverter (INV)	0.6	0.6	0.6
Nand (NAND)	1.0	1.0	0.8
Nor (NOR)	1.0	1.0	0.8
Exclusive-Or (XOR)	2.6	2.2	1.8
Half Adder (HA)	3.4	3.2	2.0
Full Adder (FA)	5.2	4.4	3.6

cells like scan-enabled flip flops, which are typically denser. As another simplification of the overall implementation effort, the custom cells were implemented to have the same pitch as that of the library cells in order to focus the assessment on the less dense but more utilized combinational logic. Since these decisions also entail interactions between cells from two libraries, the widths of the power rails were also retained.

The layouts were checked against the standard DRC deck for the technology using the Calibre nm-DRC tool. Layout Versus Schematic (LVS) checks were also successfully carried out using the Calibre nm-LVS tool. Parasitic extraction was performed using the StarRCXT tool from Synopsys. The qualified layouts were then used to extract standard cell Layout Exchange Format (LEF) files.

A. Choice of Layouts Explored

We focus on a subset of the cells created, in order to emphasize the results of this study. The other cells implemented are also included in order to maintain the robustness of the methodology adopted for the study.

The cell layouts that we focus on primarily in this study were chosen mainly based on their utility in arithmetic circuits like adders and multipliers. Additionally, they were chosen for the layout characteristics they exhibit when only static AOI architectures are considered. We make this choice constraining the architecture based on existing knowledge related to the performance characteristics of other layout architectures [20], [21] and assertions in existing literature [19]. These characteristics implicitly influence the manufacturability analysis presented in Sec. V-B.

The XOR structure presented in Fig. 2 represents a commonly used AOI-based architecture. The definition of the XOR function requires the availability of inverted versions of the inputs. Under the layout constraints of single device orientation, the routing of the inputs is qualitatively explored in this work. Given the classification of layouts in Sec. III, in each case we qualitatively assessed the quality of routing using the number of gate contacts as a raw measure of input routing efficiency.

The HA and FA circuits were chosen as functional extensions of the XOR gate. While both of these circuits, by definition, depend on the XOR gate, they differ vastly in layout. Due to the fact that there is additional functionality in these circuits, the number of devices is higher. There is also an impact due to the different number of inputs and outputs. Commonly used AOI-based architectures were implemented for these circuits as well.

B. Factors Affecting Analysis

The process of manufacturing reliable electronics in the nanometer regime involves considerations across a number of levels of abstraction and requirements. Additionally, due to the complex nature of the manufacturing process, intellectual property of the different domains in design and manufacturing is also a concern. This makes it difficult to obtain data from the foundry. However, the chief concern for a physical design engineer involves the creation of a manufacturable solution under area and performance constraints.

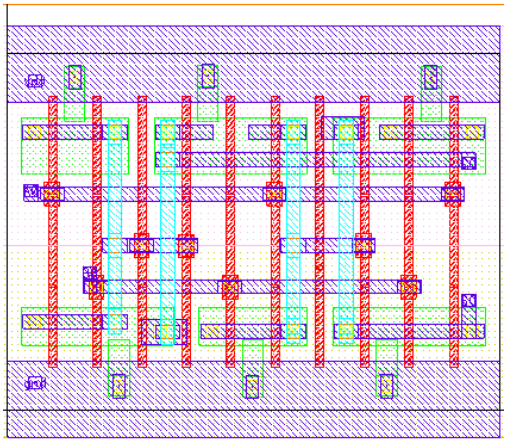
Some of the main factors having a large implicit effect on the implementation of regular cell layouts are listed under the following sub-headings.

1) Gate Pitch: The gate pitch is the first stage of regularity and sets the device density for a given circuit. It affects regular measures for all other geometries directly or implicitly. Two broad definitions of gate pitch can generally be used: The contacted gate pitch of a device can be expressed as the sum of the gate length, spacing between poly and contact and the contact width. When dummy poly is used between isolated diffusions, the isolated gate pitch can be written as the sum of the poly length, contact width, poly-contact spacing, diffusion extension over contact and diffusion-poly spacing. Assuming that upstream methodology follows the normal standard cell flow and when regular layouts are prioritized (or even mandatory) in order to keep mask costs to a minimum, a relaxed gate pitch like the isolated gate pitch will usually be preferred.

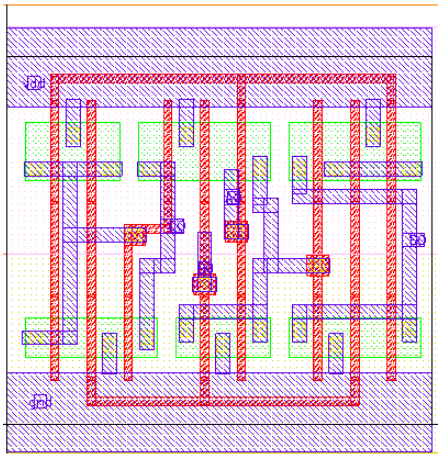
2) Device Pitch and Interconnect: In the past, the only consideration influencing the device pitch was the performance of the cell in question. It is usually the case for digital circuits that the minimum width is not used for performance reasons and this is advantageous when DFM considerations are taken into account.

With scaling geometries, however, a big concern from a manufacturability point of view is the availability of contact redundancy. It is common knowledge within the design community that redundancy of contacts and vias increases the reliability of the fabricated circuit. Doubling contacts for the sake of reliability can however have detrimental effects on the performance as it necessarily means that device widths are going to be larger and thus increase diffusion capacitance.

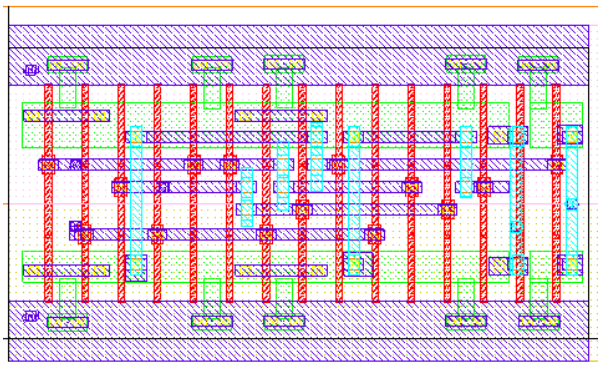
The device pitch also influences the choice of metal routing for the local interconnect. Traditionally, alternating orthogonal directions, starting with horizontal metal1 have been used. Choosing metal1 perpendicular to poly makes for better local routing but decreases the availability of redundancy. Routing metal1 parallel to poly is an alternate solution, eliminating the redundancy problem at the cost of diffusion width and, additionally, increased metal2 usage. With these considerations in mind, for this work we chose to implement cells with metal1 perpendicular to poly, without redundancy for the present discussion.



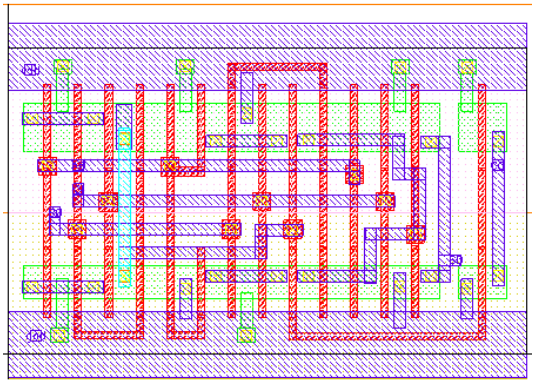
(a) Ultra-regular half-adder cell



(b) Semi-regular half-adder cell



(c) Ultra-regular full-adder cell



(d) Semi-regular full-adder cell

Fig. 3: Custom-characterized ultra-regular and semi-regular cells.

Assessing the impact of routing is more complicated due to disparate considerations like choice of architecture and choice of routing directions. Enforcing unidirectionality of routing incurs a penalty for upstream routing since it introduces blockages not seen when only metal1 is used. Additionally, this measure introduces vias, which intuitively make printability simpler, but have critical manufacturability constraints. In addition to this there is also an impact to parametric yield due to the etch- and CMP-related defects. On the other hand, allowing jogs creates problems with metal printability but poses fewer reliability concerns.

3) Power Supply Rails: The supply rail aspect of cell layout architecture has far reaching consequences for performance and area. Standard cells share supply rails through abutment on successive rows. This provides significant savings in power routing and die area. Power supply rails are typically in the lower layers and are wider than normal interconnect nets in order to retain a large current carrying capacity. The width of the power rails spans 2 to 3 horizontal routing pitches.

In cells that are not routing limited, the power can be supplied to the source terminals using metal1 and contacts to diffusion. This allows for low RC losses in the power supply network, but takes up routing resources. Also in the context of ultra-regular layouts, unidirectional routing would no longer be followed if a metal1 perpendicular to poly style is chosen.

In spite of the risk of higher RC losses, in this work, we chose to implement the power supply connections through the diffusion to assess the tradeoff against routing resource availability. Alternate power supply strategies can be adopted for further enhancement [19], but are not considered here.

4) Circuit Considerations: The choice of architecture used to implement the logic function under consideration affects a number of parameters associated with enforcing regularity on layouts. It has been observed that AOI structures lend themselves more easily to regular layouts than other types of static gates (like transmission gates etc.) [19].

If the device supply connections are completed using diffusion then maintaining a spacing of one horizontal pitch yields, between the supply rails and device diffusion, another metal routing track that can be used for parallel device connections. In the layouts created for this work, a spacing of one horizontal pitch is maintained between the power supply rails and diffusion.

The overall pitch of the cell is a tradeoff between the routing requirements for densely connected logic functions, usually the scan flip-flops, and the width.

IV. Layout Implementation

The previous section (Sec. III-B) highlighted the influences on creating regular layouts. This section details the specific adoption of these measures with respect to the cells considered in this study.

Noting the specific problems detailed in Sec. II-A, the following measures were adopted for the layouts in line with the constraints introduced at the end of Sec. III:

- The transistor widths used here are higher than the minimum width specified by the technology.
- The traditional technique of equalizing the drives of the pull-up and pull-down networks by having a wider P-MOSFET is still followed here. The P-MOSFETs are one and a half times wider than the N-MOSFETs.
- Regularity is maintained on a per cell basis, using single lines of diffusion as far as possible. In the case of the semi-regular layouts only the diffusion widths and poly pitch are regular.
- The poly layer pitch is set to the contacted gate pitch for the semi-regular cells, while this is increased to the isolated pitch for the ultra-regular cells.
- All routing layers including poly are made unidirectional for the ultra-regular layouts. This means that metal2 has to be used to complete the local interconnect within the cell. Keeping the preferred directions, poly is directed vertically, metal1 horizontally and metal2 vertically.
- For the semi-regular layouts, with the exception of the full adder, all layouts use only metal1 to complete internal routing[1]. Poly is used extensively in routing inputs to the gates of the transistors.
- In as many cases as possible, an effort is made to run input and output pins out to the edge of the cells for both the semi-regular and ultra-regular layouts. This is done in order to minimize extra routing within the cell during cell-to-cell routing.
- Dummy poly is employed to simplify the mask for the poly layer. In this work it is used only in the ultra-regular layouts with the observation that half-space rules are used at the cell edges. In more advanced nodes, it will probably become mandatory to employ isolated poly lines at cell edges.

V. Critical Feature Analysis: Metrics and Results

Calibre Critical Feature Analysis (CFA) is a DFM solution that is integrated with the DRC and LVS suites for advanced nodes. The tool runs rule- and model-based checks related to defects, lithography, OPC, CMP and etching to assess the manufacturability of a circuit in addition to the DRCs. These checks are organized in the verification framework as an extension of the DRC checks and are similarly presented. The overall results of a DFM run for a certain design are a Weighted DFM Metric (WDM), computed on all rules, and a Normalized DFM Score (NDS). In addition, the results for individual checks are also presented. For the sake of brevity, only the NDS is presented here for the different cells.

[1]It is possible to complete that net without the use of metal2 but it would result in obstructions. This is another tradeoff not considered explicitly in this work.

A. Metrics

The WDM is a weighted score computed on rules defined to obtain better manufacturability. The rules are categorized on criticality depending on the geometric value for the current check. The weight changes according to the criticality and is, as such, assigned by the foundry based on experience. The rules are designed in such a manner that the degree of benefit is reflected and ranges from a failure to comply with the DRC to a value beyond which no further benefit is expected. This binning is again based on the experience of the foundry with those geometries. The WDM score presented is a summation of the WDM for individual rule scores averaged over the total number of checks that are run.

The NDS is a negative-indexed exponential of the normalized WDM score. This means that a score of 1 indicates perfect manufacturability, while a value tending to 0 indicates catastrophic failure or no functionality. Equivalently, a low WDM indicates better manufacturability, while a higher one indicates problematic patterns.

TABLE II: CFA results for XOR, HA and FA cells.

Cell	Normalized DFM Score (NDS)		Normalizor
	Ultra-regular	Semi-regular	
XOR	0.58	0.74	4.14
HA	0.61	0.73	5.52
FA	0.68	0.74	9.66

B. Results

Table II shows the DFM scores for the ultra-regular and semi-regular XOR, HA and FA standard cells developed for this work. Analyses were run on these cells with the standard DFM deck provided by the foundry. The results indicate that the semi-regular layouts are more manufacturable than the ultra-regular ones. The fact that the layouts analyzed for DFM issues are small is highlighted by the small value of the normalizor. All the same, a few insights can be obtained.

Noting that the gate geometries are the smallest and unequivocally critical, the mask for that layer is going to have to use manufacturing techniques that are the latest-and-greatest or at least something suitably close. Given that the device diffusions are identical in both the ultra-regular and semi-regular cases, it is the choice(s) on other layers that impacts the DFM score obtained through CFA. Looking at the tradeoffs discussed in the previous sections it is clear that one of contact and/or via redundancy is a chief contributor. Given that the contacting scheme in both types of layouts is nearly identical, it is reasonable to assume that the culprits are the vias. The individual rule results (not shown here) confirm the fact that the contact and via1 related checks for the ultra-regular layouts have a high contribution in the WDM computation and thus impact the NDS. In the case of the semi-regular layouts,

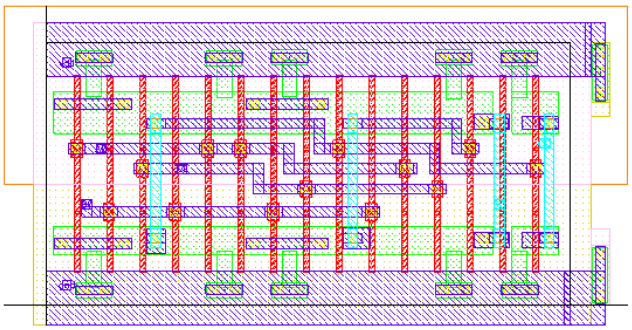


Fig. 4: A full adder cell regular in poly pitch and direction.

the primary source of concern turns out to be the contacts followed by poly-spacing rules. This indicates that using a single layer of metal to complete the internal connections rather than enforce unidirectionality of routing is a tractable option in terms of manufacturability. As a confirmation, the layout for the FA cell was modified such that regularity is enforced in poly pitch and direction, but no strict regularity of other interconnect elements are followed (Fig. 4). The CFA NDS has a value of 0.69 with the same normalizor value of 9.66. In spite of the fact that the number of layer changes is minimized, the NDS is only marginally better owing to the the fact that the vias are not backed up. From Fig. 4 it is clear that backup vias can be placed at a few locations without alteration of the routing solution. Once all the vias and as many contacts as possible are backed up, the NDS rises to 0.73. It then stands to reason that using a single metal layer for interconnect is still viable as long as the contacts are backed up. Thus, at the level of a design with a few tens of transistors, there are diminishing returns from the point of view of design effort. This may, however, prove to be offset in a larger design context.

The CFA trends for the rest of the cells created in the semi-regular and ultra-regular libraries are illustrated in Table III. While the total number of cells is still small when compared to the size of a "normal" digital VLSI circuit, there is sufficient layout diversity to minimize the possibility of ambiguity in the results. The NDS values, though lower in absolute terms than for the cells presented earlier, display a similar difference in value between the ultra-regular and semi-regular variants. If we momentarily ignore the CFA results for the INV gate, we can see from Table III that the NDS results for the semi-regular implementations are, in general, more absolutely consistent as in the case of the results for the larger cells. The normalizor value for all of these cells is also lower,

TABLE III: CFA results for other cells.

Cell	Normalized DFM Score (NDS)		Normalizor
	Ultra-regular	Semi-regular	
AND	0.55	0.65	2.07
BUF	0.55	0.63	1.38
INV	0.49	0.55	0.69
NAND	0.61	0.66	1.38
NOR	0.61	0.67	1.38

providing some indication of the number of devices and the kind of architecture chosen for the cells implemented. With these results further credence is lent to the observations made for the small set of cells in Table II when the NDS values for the other cells in the library are considered. A trend, very similar to the one observed earlier, is seen for these cells as well. Thus, inclusion of CFA results for these basic cells serves to maintain the integrity of the methodology adopted for this study and minimize the possibility of error in the interpretation of the results.

VI. Conclusion

We explored a number of regularity measures at the cell layout level intended to improve manufacturability. These measures were applied in the implemented set of eight logically complete combinational cells testing the impact of enforced interconnect unidirectionality and the implied impact of contacts and vias. The qualitative measures were tested using the Calibre Critical Feature Analysis tool from Mentor Graphics. The results show counter-intuitive trends warranting further (likely expanded) research on different aspects of the topic.

Given the counter-intuitive nature of the results, the following observations can be used as topics of discussion and avenues for further research.

- At the cell level, unidirectional interconnect routing is not beneficial. In a larger design context where interconnect issues dominate device issues, unidirectionality may have a larger impact. The results from the CFA tool, with great emphasis on via- and contact-doubling, strongly suggest this.
- The results, put into perspective, also reveal the need for different analysis methods. For the cell level checks any use of higher metal layers is penalized, but in a larger design scenario the problem posed by vias would far outstrip those posed by devices, skewing the results unfairly. While the NDS provides a tractable measure, it could be misleading. Perhaps, methods defining DFM metrics separately for the devices and for interconnect will provide a different picture.
- As far as manufacturability is concerned, regular layouts have empirically been shown to be as good as current designs [19]. However, the need to combine regular layouts with concepts for regular routing using automated methods is still an area requiring more research. Heuristic routing yields "good enough" solutions, but when the cost of manufacturing becomes critical due to the need for mask corrections such methods may no longer pay dividends.
- From a manufacturing point of view, a designer working with cutting edge technology must accept the fact that the smallest geometries in the design, namely the gate related geometries, need patterning at the highest fidelity. Is it then possible to reduce interconnect masking cost by any means? The answer to this is a topic of analysis in itself and we refrain from commenting further on this here.
- Careful tuning of the regular structures is an important consideration to improve timing and reduce capacitance.

- Without knowledge of reliability numbers for vias and contacts, it is difficult to assess the tradeoff to enforce routing unidirectionality, especially when feature analysis tools penalize them heavily on account of lack of redundancy. One *ad hoc* solution is to adopt relaxed gate pitches and allow limited wrong way routing at the cell level. Assessment of manufacturability for the higher layers of metal should then be carried out with a different set of rules (or patterns, when the checks are model based).

The work presented here is in many ways simpler than the works surveyed in Sec. II-B and in other parts of this work, but the motivation for doing so comes from consideration of a wider context spanning different levels of abstraction. In order to strengthen the indications of the results of this study, the next step involves the application of the cells developed in this work to a complete design. Usage of the cells developed here can be studied with the intent of extracting similar manufacturability metrics; for this purpose benchmark circuits such as the ISCAS'89 [22] benchmarks would serve as good vehicles. Application of these cells to digital blocks such as multipliers and shifters (which display some degree of inherent regularity) would serve to test the impact of regularity on other, higher-level metrics such as area utilization and also allow a study of the impact on traditional performance metrics such as timing.

In the long term, future work in this area will revolve around connecting the synthetic assessment techniques to a quantifiable measure thus effectively capturing the link between "soft" measures and the manufacturing process. Other efforts are also needed in creating algorithms that create routing solutions for large designs that are regular, in an efficient manner. Also to be researched are the performance tradeoffs involved in applying a high degree of regularity. An interesting offshoot of this is the automated creation of lithography-aware layouts. Part of such an effort would involve estimation of the effective device width for the best performance-regularity tradeoff.

This work just listed a few of the things necessary individually; what is more important however is the need to define seamless methodology that enables design of high performance electronics in a manner that reflects the performance of today but are not vitiated by the limitations of tomorrow.

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