Prime DC/AC Buck-Boost Converter

Derivation of mathematical models and evaluation of lumped transmission lines with focus on size and efficiency

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2012
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Cover:
A picture of a Prime Buck-Boost converter prototype.

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Abstract

Introducing a transmission line into the fundamental power conversion circuits
(Buck, Boost and Buck-Boost) has given the possibility to create converters types
with new properties. A modified Buck-Boost converter in DC/AC operation has been
evaluated. The main goal was to verify if a DC/AC conversion could be made and to
optimize its efficiency with different lumped transmission lines (LTL). The idea was
to decrease the total area of the LTL in order to make the solution more attractive for
the power electronic market. Moreover, there was no theoretical explanation of the
converter. Therefore the transfer function was investigated and a mathematical
explanation of the converter was provided.

The converter works in two different modes, inverting and non-inverting. In its
inverting mode it works as a regular Buck-Boost converter and in its non-inverting
mode it can provide an output voltage with the same polarity as the input voltage.
The current and voltage wave propagating inside the LTL can be described with
general microwave theory. The converter was also proven to work in DC/AC mode
and has an efficiency of 69% with a LTL with U-core inductors. The efficiency can
be interpreted as low since old measurements with an LTL incorporating surface
mounted inductors instead, showed an efficiency of 81%. The decrease in efficiency
is most likely due to a malfunctioning MOSFET. In non-inverting mode the
efficiency was increased with two of the U-core LTLs. The Prime Buck-Boost
solution has great potential, but at the moment the efficiency is too low and the total
area is too big. An investigation of the converter in AC/DC mode with GaN switches
and LTLs with E-cores has been proposed for future work.

Index Terms: Buck Boost, Buck/Boost, Buck-Boost, Converter, Transmission Line,
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Mike Kiprianoff
Göteborg, Sweden, 2012
List of Symbols

Δ₁ - Δ₄ – Different time intervals in non-inverted mode.
ΔVc – Voltage difference when load capacitor is charged
Δx – Time interval between chosen reflections.
γ – Propagation constant
η – Efficiency
η_{PwSt} – Power stage Efficiency
Γ_g – Reflection coefficient at generator
Γ_L – Reflection coefficient at S_C when it’s on
Γ_{L1} – Reflection coefficient at S_C when it’s off
Γ_{L2} – Reflection coefficient at load
C – Capacitance
d – Transmission line length
D – Duty cycle
G – Conductance
f_{r₁} – First resonance frequency
f_{sw} – switch frequency
I_{1⁺} – Initial current wave propagating in a TL
I_{5⁻} – Current amplitude when interval Δ₄ begin
I_L – Load current
I_{SA} – Current at switch S_A
I_{SC} – Current at switch S_C
l – Inductance per meter
L – Inductance
L’ – Total inductance of a shorted TL below its resonance frequency
M – Number of reflections
N – Number of LC elements
N_{Γ_g} – Number of reflections at S_A during interval Δ₁ – Δ₂
N_{Γ_L} – Number of reflections at S_C during interval Δ₁ – Δ₂
N_{Γ_{L1}} – Number of reflections at S_C during interval Δ₃ – Δ₄
N_{Γ_{L2}} – Number of reflections at load during interval Δ₃ – Δ₄
P_{drv} – Driver power
P_{iso} – Isolator power
P_{in} – Input power
P_{out} – Output power
P_{PwSt} – Powerstage power
R – Resistance
S – Switch
S_A – High- side switch
S_B – High- side switch for synchronous rectification
S_C – Low-side switch for non- inverting operation
t_d – Delay time in TL
T_S – Period time
V – Voltage wave when interval Δ₂ begin
V_{1⁺} – Initial voltage wave propagating in a TL
$V_2^+$ - Second voltage wave propagating in a TL after reflection
$V_{IN\ AC}$ – AC input voltage
$V_{in}$ – DC input voltage
$V_{out}$ – Output voltage
$V_{rect}$ – Rectified voltage
$X_L$ – Inductive reactance
$z'$ – Transmission line position
$Z_0$ – Characteristic impedance
$Z_L$ – Load impedance
$Z_{in}$ – Generator input impedance
## Abbreviations

<table>
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<th>Description</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCR</td>
<td>Direct Current Resistance</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>LTL</td>
<td>Lumped Transmission Line</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>PBB</td>
<td>Prime Buck-Boost</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Board Circuit</td>
</tr>
<tr>
<td>PRIME</td>
<td>Propagation MEdium</td>
</tr>
<tr>
<td>PPC</td>
<td>Prime Power Conversion</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>TL</td>
<td>Transmission Line</td>
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Chapter 1

1 Introduction

For the last three years, Ericsson has conducted an internal research project regarding power electronic converters utilizing transmission lines. The project is called Prime Power Conversion (PPC) and concerns DC-DC, DC-AC and AC-DC converters. Sverker Sander who is the founder and main executor of the project, had an idea of replacing the inductance, which is normally used as an energy storage device for a power electronic converter, with a transmission line\(^1\) (TL). By introducing a TL into the fundamental power conversion circuits (Buck, Boost and Buck-Boost), new configurations previously not addressed in literature could be made possible [1].

The idea of introducing a TL to accumulate energy within a converter, have been proven to give properties that are not available with conventional converters. Examples of these properties are reduced number of semiconductors, multiple voltage outputs and if using a Buck-Boost configuration the output voltage can be non-inverted i.e – it has the same polarity as the input voltage. The last example also enables the possibility to build an AC/DC converter with a reduced number of semiconductors [2].

The AC/DC concept is named Prime Buck-Boost (PBB) converter and was realized into a prototype in late 2011. It was tested in a DC/AC configuration and was proven to have a decent efficiency. In order to make the PBB converter more attractive for future work, it continued as this master thesis.

1.1 Problem Description

The previous TL in the PBB converter, from now on called lumped transmission line 0 (LTL\(_0\)), was built with an LC network made of 40 lumped surface mounted inductors and capacitors, see illustration in Fig. 1.

\[\begin{array}{c}
L_1 \\
\cdots \\
L_N \\
\end{array}
\begin{array}{c}
C_1 \\
\cdots \\
C_N \\
\end{array}\]

Fig. 1 A lumped LC network illustrating the inductances and capacitors.

\(^{1}\) A transmission line could be some sort of cable; a printed circuit board microstrip or stripline; a delay line or an LC network of lumped inductors and capacitors (LTL) [1].
Chapter 1. Introduction

Many power electronic companies compete by decreasing size and component cost of their products; LTL₀ will consequently be hard to implement in a real product due to its size. A decision was made in the PPC project to replace the old LTL in order to reduce its drawbacks, which are:

1. Each inductor requires two pads on the PCB top layer to interface its terminals, creating 80 pads in total.
2. The inductor building height is 3mm which result in a ‘low and wide’ LTL distribution with a total size of 30.5cm², see Fig. 2.
3. Each inductor can carry a 50A RMS which is oversized for the desired application.

Due to the drawbacks, three new LTLs were designed and produced in parts. These will from now on be called LTL₁, LTL₂ and LTL₃, see Appendix A for dimensions. The difference between them is that the two first uses ferrite U-cores and the third uses ferrite toroidal cores as inductances. LTL₀ was on the other hand made out of 40 surface mounted Coilcraft inductors and 40 Murata capacitors see Table 1 for specification. The capacitors are common for each LTL.

![Fig. 2 Size and design of LTL.](image)

Table 1 Specifications for L and C used in LTL₀.

<table>
<thead>
<tr>
<th>Coilcraft</th>
<th>Murata</th>
</tr>
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<tr>
<td>SLC7530S-101MLC</td>
<td>GRM1555C1H561J</td>
</tr>
<tr>
<td>L = 100±20nH</td>
<td>C = 560±5pF</td>
</tr>
<tr>
<td>DCR = 0.123 mΩ</td>
<td>ESR = 0.057Ω</td>
</tr>
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1.2 Purpose

To theoretically and practically evaluate a new DC/AC Buck-Boost Converter that features controllable inverting and non-inverting power conversion. It incorporates derivations of mathematical models, optimization of efficiency and electrical verification of lumped transmission lines. The idea is to make the solution more attractive for further development in the power electronic industry.
1.3 Objectives

The first objective of this thesis was to finalize the manufacturing of the LTLs and obtain the same impedance for the new LTLs as the old one in order to be able to compare them regarding efficiency. The second goal was to simulate the current magnitude, the efficiency and the DC/AC conversion of the PBB converter. The third objective was to practically optimize and increase the converter efficiency with the new LTLs and to verify the DC/AC conversion. Finally there was no theoretical explanation of the converter transfer function. Therefore, the fourth objective was to investigate the transfer function and provide a theoretical explanation of how the converter operates.

1.4 Previous Work

Transmission lines have long been used in radio frequency applications in order to shape waveforms and improve efficiency [3]-[4]. A transmission line which is open- or short circuited has a certain resonance frequency dependant on the impedance of the line. If the TL is used at a frequency equal to its first resonance frequency it enforces odd- and even harmonics in the voltage and current [3] [5]. By the use of transmission lines in high frequency power conversion circuits and a switch frequency equal or close to the first resonance frequency, new power conversion properties and/or the possibility to utilize the harmonic content is possible [3]-[11]. Distinguished from these studies, the PPC research project at Ericsson shows solutions were the energy storage device is replaced with a transmission line inside the converter topologies Buck, Boost and Buck-Boost [1]-[2]. As mentioned, the solutions have given the possibility to have multiple voltage outputs, a reduced number of semiconductors and a controllable non-inverting and inverting power conversion. A key thing in the project has been the use of switch frequencies an order of magnitude lower than the first resonance frequency [2]. The same switch principle is used for the PBB converter in this master thesis.
Chapter 2

2 Technical Background

This section discusses the Prime Buck-Boost converter, general transmission line theory, the basic idea of energy accumulation in a TL and how the non-inverting function is possible with the converter.

2.1 AC/DC Conversion with Prime Buck-Boost

A common technique to do an AC/DC conversion is to use a full wave diode rectifier followed by a converter, see Fig. 3a. In this example, the converter is a Buck-Boost converter. The conversion is achieved by a high side switch $S$. When $S$ is on, energy is accumulated within the inductance $L$ and the capacitor $C$ supplies the load with energy. When $S$ is off, the inductor supplies $R$ and $C$ with energy, due to a free-wheel current from $L$ through $R$, $C$ and the diode $D$. It can further be noted that the transfer function of a regular Buck-Boost converter is

$$\frac{V_{\text{out}}}{V_{\text{rect}}} = \frac{-D}{1-D}$$

(1)

where $V_{\text{out}}$ is the output voltage, $V_{\text{rect}}$ the rectified voltage and $D$ the duty cycle. This means that $|V_{\text{out}}|$ can either be increased or decreased compared to $V_{\text{rect}}$, with the side-effect that the voltage polarity is inverted, see Fig. 3b [12].
The PBB idea was to create an AC/DC- conversion with only three semiconductors, achieving the same result as the above. The difference between a regular Buck-Boost and the PBB converter is that the inductor is replaced with a transmission line and the diode with a switch $S_B$. There is also an added switch $S_C$ at the end of the TL, see Fig. 4a.

In order for an AC/DC- conversion to be possible, it implies that the converter can both have positive and negative output voltage regardless of the input voltage polarity. This is achieved with switch $S_C$. The basic idea is that if $S_C$ is continuously on and $S_A$ and $S_B$ are switched sequentially, the circuit works as a regular Buck-Boost converter. If $S_C$ is briefly opened instead, the output polarity retains the same as the input, see Fig. 4b. Exploiting this fact, enables the converter to work in two operations modes, inverting and non-inverting. This gives the possibility to do a full wave rectified AC/DC- conversion incorporating only three semiconductors.
Chapter 2. Technical Background

![Diagram of Prime Buck-Boost converter and modulation technique](image)

**Fig. 4** The Prime Buck-Boost converter and the modulation technique for the different switches in order to achieve AC/DC conversion.

For the AC/DC conversion to work, it implies that switch $S_A$ and $S_B$ block both positive and negative drain-source voltages. The most common switch in the low voltage power electronic industry is the MOSFET. The drawback with regular power MOSFETs is that they have an intrinsic body diode between drain and source. Normally it causes no problems, since the voltage blocking polarity is constant. But when using MOSFETs in a PBB AC/DC conversion, they will be exposed to both positive and negative voltage which will cause a short-circuit. It exist switches without body diodes. One type that offers this property is called GaN switches. Unfortunately, these GaN switches were not available during the PBB project. Instead the non-inverting function was tested and verified by building a DC/AC converter circuit with MOSFETs, see Fig. 5. The PBB converter can be seen to be big due to the input capacitors and the total surface of $LTL_0$. The big input filter is used to attenuate low frequency 50Hz input current ripple. The placement of components is not optimal either, since it is a prototype. The total size of the converter can therefore be reduced. The converter schematics can be found in appendix B.
2.2 Transmission Line Theory

The telegraph equations can be used to find the voltage and current at a specific point along the transmission line. These can be expressed as

\[ V(z') = I_L (Z_L \cosh \gamma z' + Z_0 \sinh \gamma z') \]  
\[ I(z') = \frac{I_L}{Z_0} (Z_L \sinh \gamma z' + Z_0 \cosh \gamma z') \]  

with terms of load current \( I_L \), load impedance \( Z_L \), propagation constant \( \gamma \) and characteristic impedance \( Z_0 \). \( \gamma \) and \( Z_0 \) can be found as

\[ \gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \]  
\[ Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \]

Dividing (2) with (3) and inserting the line length \( z' = l \) gives

\[ Z_{in} = Z(l) = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \]  

where \( Z_{in} \) is the input impedance the generator sees when looking into the line [13]. The input impedance is plotted in Fig. 6 with respect to frequency for short circuit, open and terminated load. \( L \) and \( C \) are set to 100nH and 560pF (the Coilcraft and Murata component values used in LTL0). In this case, the line is considered lossless (\( R \) and \( G \) are zero).
As seen, the impedance has several resonance frequencies. The first resonance can be found as

$$f_{r1} = \frac{1}{4N \sqrt{LC}}$$

where $N$ is the number of combined LC elements [5]. For the case of 40 LC elements in LTL$_0$, the first resonance frequency $f_{r1}$ becomes 835kHz. This can also be seen in Fig. 6.

2.3 Transients on a transmission line

In the simplest case, a DC- voltage source $V_{in}$ is applied through a series internal impedance $Z_g$ to a lossless transmission line, see Fig. 7. It has the characteristic impedance $Z_0$ and load impedance $Z_L$. The reflection coefficients are denoted $\Gamma_g$ at the input end and $\Gamma_L$ at the output end.

![Fig. 7 A DC- source applied to a transmission line.](image-url)
When the switch $S$ is closed at time $t = 0$, a voltage wave of magnitude

$$V_1^+ = \frac{Z_0}{Z_0 + Z_g} V_m$$  \hfill (8)

and a current wave of magnitude

$$I_1^+ = \frac{V_m}{Z_0 + Z_g}$$  \hfill (9)

will travel towards the load. If $Z_L \neq Z_0$, the wave will be reflected at time $t = t_d$ and travel back to the DC-source with a magnitude of

$$V_1^- = \Gamma_L V_1^+$$  \hfill (10)

where the reflection coefficient ($\Gamma_L$) is defined as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}. \hfill (11)$$

If $Z_g \neq Z_0$ the wave will be reflected once again at time $t = 2t_d$ according to

$$V_2^+ = \Gamma_L \Gamma_g V_1^+$$  \hfill (12)

where

$$\Gamma_g = \frac{Z_g - Z_0}{Z_g + Z_0} \hfill (13)$$

is the reflection coefficient at the generator side.

The waves will reflect at each end at $t = nT_d$ where $n$ is an integer (1, 2, 3 . . . n). This will occur infinitely if the transmission line is lossless. The voltage across the load can then be written as

$$V_L = V_1^+ (1 + \Gamma_L + \Gamma_L \Gamma_g + \Gamma_L^2 \Gamma_g + \Gamma_L^3 \Gamma_g^2 + \ldots + \Gamma_L^n \Gamma_g^{n-1} + \Gamma_L^n \Gamma_g^n)$$ \hfill (14)

and the load current as

$$I_L = I_1^+ (1 - \Gamma_L + \Gamma_L \Gamma_g - \Gamma_L^2 \Gamma_g + \Gamma_L^2 \Gamma_g^2 - \ldots - \Gamma_L^n \Gamma_g^{n-1} + \Gamma_L^n \Gamma_g^n) \hfill [13]. \hfill (15)$$

These two equations can be used to theoretically explain the current and voltage in the PBB converter LTL.
Consider the two circuits in Fig. 8 which both have a DC-voltage source connected at the input with a switch \( S \) and with its ends grounded. The difference between the circuits is the energy storage device. One uses an inductance \( L' \) and the other uses a transmission line (TL).

If \( S \) is closed at \( t = 0 \), a DC-voltage is applied to the inductor and the current \( I_L \) will increase linearly, see Fig. 9. If the same procedure is repeated with a TL, the current \( I_{TL} \) will increase stepwise. This is because of the reflection coefficients \( \Gamma_L \) and \( \Gamma_g \) become \(-1\) since \( Z_L = Z_g = 0 \). Using these values in (15) shows that the current increases immediately by \( I_1^+ \) when \( S \) is closed and by \( 2I_1^+ \) every \( 2t_{dL} \).

If a long accumulation interval \( T_{acc} \) is allowed, the TL can be modeled as an inductor according to

\[
L' = dl \tag{16}
\]

where \( d \) is the TL length in meters and \( l \) the inductance per meter. If an lumped transmission line is used, the inductance can be expressed as

\[
L' = NL \tag{17}
\]

where \( N \) is the amount of LC elements and \( L \) is the inductance of one \( L \) element [1].
2.5 Non-inverting Operation of Prime Buck-Boost

Using the theory above makes it possible to explain the operation cycle for a lossless PBB converter in DC/AC conversion mode. The first operation cycle can be found in Fig. 10. The current (cross-hatched) and voltage waves (hatched) are plotted as a function of t (s) and the switch states for $S_A$, $S_B$ and $S_C$. Furthermore, the duty cycle is set to 50% in this example.

$t=0$

Start up of PBB Converter. The Switches $S_A$ and $S_C$ are conducting whereas a voltage wave $V_1^+$ (hatched) and a current wave $I_1^+ = V_{av}/Z_0$ (crosshatched) will start to propagate along the line.

$t=t_d$

The waves have reached the TL output end where the reflection coefficient $\Gamma_{L1}$ is equal to -1 since the TL output end is short circuited. Consequently, according to (14) and (15), the voltage wave will be reflected into $V_1^-$ with inverted polarity and the current wave polarity remains unchanged. The sum of $V_1^-$ and $V_1^+$ becomes zero and the current increases to $2I_1^+$.
Chapter 2. Technical Background

$t=2t_d$

The waves have reached the TL input end. The input filter is assumed to have a low impedance compared to the characteristic impedance which result in a reflection coefficient $\Gamma_g$ close to -1. The current at the input side is increased to $3I_1^+$ and a new voltage wave equal to $V_1^+$ will start to propagate towards the TL output.

This procedure between $0 < t < 2t_d$ can be repeated several times to accumulate energy in the TL. However, to limit the size of the graph the total energy accumulation interval was set to $4t_d$ (the time interval $S_A$ is on).

$t=3t_d$

The waves reach the TL output end once again. Switch $S_A$ is still conducting and $S_C$ is turned off, thus creating an open termination. The impedance at the output end becomes infinite and no current will flow through $S_C$. All energy stored as a current wave in the TL, is transformed to a voltage wave equal to $4V_1^+$. The reflection coefficient $\Gamma_{L1}$ becomes 1 and the voltage wave is reflected with unchanged polarity. This process is considered the core event of the converter’s non-inverting operation.

$t=4t_d$

At this time instance, the positive voltage wave reaches the TL input. Switch $S_A$ is turned off, $S_B$ is turned on and $S_C$ is still conducting. Thus, the capacitor $C_{out}$ and the load $R_{load}$ is connected to the TL input end. At this time instant, the voltage wave begin to transform into a current wave, equaling $-4V_1^+ / Z_0$. The current wave propagates towards the TL output end with negative polarity. This is due to that the reflection coefficient $\Gamma_{L2}$ becomes -1 because of the load $Z_L$ ($R_{load}$ parallel to $C_{out}$) is assumed to be much lower than the characteristic impedance of the TL.

$t=5t_d$

The voltage wave is completely transformed to a current wave and switch $S_C$ is turned on again. The current wave reaches the TL output and will be reflected with the same condition as described in time instance $t=t_d$. At the same time, until switch $S_B$ is turned off, the energy stored in the TL will partially charge the output capacitor $C_{out}$ to a positive voltage (not shown).

It can also be noted that switch $S_C$ is kept in off state a total time of $2t_d$, the time it takes for the wave to propagate back and forth along the TL. This is because of the waves need to have enough time to convert and invert between $3t_d < t < 5t_d$. If $S_C$ conducts less than $2t_d$, a part of the wave will be non-inverted and will be added to the inverted wave. The magnitude of the current will therefore be decreased and result in a lower converter efficiency.

$t=8t_d$

The operation cycle starts over and Switch $S_A$ is turned on and $S_B$ is turned off. The operation cycle is repeated several of times it will eventually lead to steady state. This means that the converter convert the input DC voltage to an output DC voltage with the same polarity which depend on the duty cycle.
Chapter 2. Technical background

Fig. 10 Time space diagram of the voltage and current waves in the converter.
Chapter 3

3 Prime Buck-Boost DC/AC Simulation

A first simulation of the LTL\textsubscript{0} was performed to investigate how the input impedance $Z_{\text{in}}$ depends on frequency. The idea was to see how well the simulation software LTspice correspond to the transmission line theory. Secondly a simulation of the PBB converter in non-inverting operation was made to investigate efficiency and how $V_{\text{out}}$ depends on duty cycle. Furthermore, a simulation of the PBB converter in DC/AC configuration was made in order to evaluate the efficiency and the DC/AC functionality.

3.1 LTL Simulation

A simulation model of 40 L and C elements, with the same values as the original LTL\textsubscript{0} was implemented, see Fig.11. The LTL simulation was performed to verify the transmission line theory for the LTL input impedance. The input voltage is an AC supply. The AC amplitude was set to 1V.

![Simulation setup.](image)

The simulated LTL and a theoretical TL derived from (6), where L and C were set to the same value as in the simulation, can be seen in Fig. 12. The simulated LTL coincide well with the transmission line theory.
Chapter 3. Prime Buck Boost DC/AC Simulation

3.2 Efficiency

A simulation of the PBB converter with LTL₀ was made in LTspice to see how high the efficiency could be, see Fig. 13.

![Simplified model of the simulated DC/AC Buck-boost converter with a LTL.](image)

The input filter and output filter was set according to the values in the PBB converter, see Table 2. The MOSFETS in the converter was modeled as switches with $R_{D_{son}}=28\,\text{mΩ}$, $R_{D_{soff}}=10\,\text{MΩ}$, and threshold voltage $V_t=0.5\,\text{V}$. The input voltage was set to $14\,\text{V}$. The switch frequency was adjusted until the highest efficiency was achieved. Test simulations in non-inverting mode showed a decrease in efficiency with a duty cycle lower or higher than 50%. Therefore, for the non-inverting mode, it was decided to record the efficiency when the output voltage corresponded to 50% of $V_{in}$ at 50% duty cycle. For inverting mode, the output voltage could not be set to 50% of $V_{in}$. The reason is because of the load resistance would become too small,
which result in a high current in the LTL that saturates the inductors. Therefore, for the inverting mode, the efficiency was simulated with 50% duty cycle and a load of 6Ω which resulted in an input current of approximately 2.4A in the LTL. The efficiency was 93.4% and for the non-inverting mode it was 90.5% at a switch frequency of 278kHz.

### Table 2 Input and output filter data.

<table>
<thead>
<tr>
<th></th>
<th>Input filter</th>
<th></th>
<th>Output filter</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>L</strong></td>
<td>2x Vishay</td>
<td></td>
<td>10x Murata</td>
</tr>
<tr>
<td></td>
<td>IHLP-6767GZ-11</td>
<td></td>
<td>GRM2195C1H103J</td>
</tr>
<tr>
<td></td>
<td>L=4.7µH</td>
<td></td>
<td>C=10nF</td>
</tr>
<tr>
<td></td>
<td>DCR = 40.7Ω</td>
<td></td>
<td>ESR=0.051Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ESL=0.53nH</td>
</tr>
<tr>
<td></td>
<td>10x Nippon</td>
<td></td>
<td>C=470µF</td>
</tr>
<tr>
<td></td>
<td>EMVY630ADA471MLH05S</td>
<td></td>
<td>ESR=0Ω</td>
</tr>
<tr>
<td></td>
<td>C=10nF</td>
<td></td>
<td>ESL=7nH</td>
</tr>
<tr>
<td></td>
<td>10x Murata</td>
<td></td>
<td>C=2.2µF</td>
</tr>
<tr>
<td></td>
<td>GRM32ER72A225K</td>
<td></td>
<td>ESR=0.029Ω</td>
</tr>
<tr>
<td></td>
<td>C=10µF</td>
<td></td>
<td>ESL=0.98nH</td>
</tr>
<tr>
<td></td>
<td>5x Murata</td>
<td></td>
<td>C=0.018pF</td>
</tr>
<tr>
<td></td>
<td>GRM32DR71E106K</td>
<td></td>
<td>ESR=0.023Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ESL=0.44nH</td>
</tr>
<tr>
<td></td>
<td>1x Coilcraft</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SLC7530S-101ML</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>L=100nH</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DCR = 40.7Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cp=0.018pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.3 **Decrease and Increase of LC elements**

An increase and decrease of LC elements was made in order to see how the efficiency varies. The same simulation setup and procedure as in section 3.2 were used except that the number of elements in the LTL were either decreased or increased with 8 elements at a time.

The switch frequency was adjusted as a ratio in the simulation. A ratio of 6 were used, which is the same ratio as the one corresponded to 278kHz for 40 LC elements were used. The reason was to see how the efficiency is affected when the switching frequency is increased or decreased as a function of number of LC elements. Moreover, the converter was operated in non-inverting mode, the load was adjusted until $V_{out}$ corresponded to 50% of $V_{in}$ at 50% duty cycle. The efficiency was recorded, see Fig. 14.

It is concluded that the efficiency increases with an increase in LC elements, but it also contains two local minimums at 40 and 64 elements. According to the simulation the optimum amount of LC elements is at 56 or 72 for this specific switch ratio.
3.4 DC/AC Function

A low frequency modulation was applied to the gate voltage of switch $S_C$. A transition from approximately negative (-7V) to positive (7V) output voltage, or vice versa, was effectuated every 1.8ms to create a 278Hz AC output voltage. To obtain an output voltage of ±7V, the load ($R_{\text{load}}$) was set to 2Ω and the duty cycle was set to 25% for non-inverting mode and 35% for inverting mode.

The switch frequency for the switches $S_A$, $S_B$ (and $S_C$ during non-inverted mode) was set to 84 kHz. Fig. 15 shows $V_{\text{in}}$, $I_{\text{in}}$, $V_{\text{out}}$ and $I_{\text{out}}$ during ten cycles. As seen, a DC/AC conversion is possible with the PBB converter. The efficiency was calculated according to

$$\eta = 100 \frac{P_{\text{out}}}{P_{\text{in}}} \quad (18)$$

where $P_{\text{out}}$ and $P_{\text{in}}$ is the average output and input power according to

$$P_{\text{out}} = V_{\text{out}} I_{\text{out}} \quad (19)$$

$$P_{\text{in}} = V_{\text{in}} I_{\text{in}} \quad (20)$$

Furthermore, the converter efficiency was 82.5%.

*Fig. 14 Efficiency as a function of number of LC elements.*
Fig. 15 Input and output voltage & current to show the DC/AC function.
Chapter 4

4 Mathematical Model

This chapter discusses the derivation of the transfer function and in detail how the transmission line theory can be applied to the converter in its non-inverting mode.

4.1 Transients in Non-inverting Operation

The same simulation setup as in section 3.2 were used, see Fig. 13. The duty cycle was set to 50% and the input voltage $V_{in}$ to 14V. There are four different switch states forming a complete switch cycle, see Fig. 17.

![Switch patterns for $S_A$, $S_B$ and $S_C$ during one and a half cycle at 50% duty cycle.](image)

Fig. 16 Switch patterns for $S_A$, $S_B$ and $S_C$ during one and a half cycle at 50% duty cycle.
These states correspond to four time intervals designated $\Delta t_1 - \Delta t_4$ and are calculated according to

\[
\Delta t_1 = DT_s - t_d
\]

(21)

\[
\Delta t_2 = t_d
\]

(22)

\[
\Delta t_3 = t_d
\]

(23)

\[
\Delta t_4 = (1 - D)T_s - t_d
\]

(24)

where $D$ is the duty cycle, $T_s$ the period time and $t_d$ the time it takes for the wave to travel along the line from one end to the other. $T_s$ and $t_d$ [13] can be found as

\[
T_s = \frac{1}{f_{sw}}
\]

(25)

\[
t_d = N\sqrt{LC}
\]

(26)

where $f_{sw}$ is the switch frequency and $N$ the number of LC elements in the LTL. It can be seen that switch $S_A$ conducts during interval $\Delta_1 - \Delta_2$, switch $S_B$ during interval $\Delta_3 - \Delta_4$ and $S_C$ during interval $\Delta_1$ and $\Delta_4$.

The output voltage $V_{out}$, the input current $I_{SA}$ at switch $S_A$ and the output current $I_{SC}$ at switch $S_C$ of the LTL are presented in Fig. 17. During interval $\Delta_1$, the input current increases step wise until interval $\Delta_3$. The same applies for the output current, except it increases until interval $\Delta_2$ begin. During $\Delta_2$, all energy stored as a current wave is transformed into a voltage wave. When interval $\Delta_3$ begins, all energy stored as a voltage wave is transformed back to a current wave. During interval $\Delta_3 - \Delta_4$ the current charges the capacitor and the output voltage increases. This coincides well with the theoretical explanation made in section 2.5.
Chapter 4. Mathematical Model

Fig. 17 Input and output current of the LTL and $V_{out}$ during roughly one and half cycle at 50% duty cycle.

4.1.1 Interval $\Delta_1$

It has been stated that LTL is built with 40 LC elements of 100nH and 560pF. This gives a characteristic impedance of

$$Z_0 = \sqrt{\frac{L}{C}} \approx 13.4 \Omega.$$  \hspace{1cm} (27)

If the internal generator resistance $Z_g$ is assumed to be zero and the input voltage $V_{in}$ is set to 14V, the current wave magnitude can be calculated as

$$I_1^+ = \frac{V_{in}}{Z_0 + Z_g} \approx 1.047 \text{A}$$  \hspace{1cm} (28)

which initially propagates in the LTL. The magnitude is close to the simulated value of 1.045A, see $I_{SA}$ at t<0.5μs in Fig. 17. The small difference is because of the inductance DC resistance in the input filter.

At the LTL end the load impedance $Z_L$ is 0Ω, since $S_C$ is conducting, see Fig. 18.
Chapter 4. Mathematical Model

The reflection coefficient for each side of the LTL therefore becomes

\[ \Gamma_L = \frac{0 - Z_0}{0 + Z_0} = -1 \]  \hspace{1cm} (29)

\[ \Gamma_g = \frac{0 - Z_0}{0 + Z_0} = -1 \]  \hspace{1cm} (30)

where \( \Gamma_L \) is the reflection coefficient at switch \( S_C \) and \( \Gamma_g \) the reflection coefficient at switch \( S_A \). The number of reflections at each end is

\[ N_{\Gamma_L} = \frac{DT_s - t_d}{2t_d} = 2 \]  \hspace{1cm} (31)

\[ N_{\Gamma_g} = \frac{DT_s}{2t_d} = 3 \]  \hspace{1cm} (32)

where \( N_{\Gamma_L} \) is the number of reflections at \( S_C \) and \( N_{\Gamma_G} \) is the number of reflections at \( S_A \). Note that the last reflection at \( S_C \) does not increase the current amplitude in the case of 50% duty cycle. This is due to that \( S_A \) is turned off at the same instance as interval \( \Delta_1 \) ends. The currents at each end become

\[ I_{sc} = I_1^+ (1 - \Gamma_L + \Gamma_L \Gamma_g - \Gamma_L^2 \Gamma_g) \approx 4.19A \]  \hspace{1cm} (33)

\[ I_{sa} = I_1^+ (1 - \Gamma_L + \Gamma_L \Gamma_g - \Gamma_L^2 \Gamma_g + \Gamma_L^2 \Gamma_g^2) \approx 5.24A \]  \hspace{1cm} (34)

According to simulations, the currents become 4.15A and 5.18A. The small difference is because of DC resistance in the input and LTL inductances. In reality it would also involve crosstalk between the LC elements, but that is not included in the simulation.
4.1.2 Interval $\Delta_2$

During this interval, switch $S_A$ is still on and $S_C$ is turned off, see Fig. 19.

![Circuit diagram]

*Fig. 19 Circuit during interval $\Delta_2$, switch $S_A$ on and $S_C$ off.*

All energy stored as a current wave is transformed into a voltage wave according to

$$V^- = (N_{r_l} + N_{r_g})I_1^+ + V_{in} = 6V_{in} = 84\,V.$$  \hspace{1cm} (35)

The voltage wave will begin to propagate towards switch $S_A$. It can be noticed that the current amplitude at switch $S_A$ is constant for one $t_d$ (half the time switch $S_C$ is kept in off state). This means that the voltage wave will reach $S_A$ when interval $\Delta_3$ begins and it will not affect the current amplitude which was previously calculated to $5.24A$. At switch $S_C$, it can be seen that the current amplitude is zero because it is transformed into a voltage wave.

The reflection coefficient at $S_A$ is the same as to $\Gamma_g$ in (30) and at $S_C$ it can be calculated as

$$\Gamma_{L1} = \frac{\infty - Z_0}{\infty + Z_0} = 1.$$  \hspace{1cm} (36)

4.1.3 Interval $\Delta_3$

The voltage wave front, created during interval $\Delta_2$, has reached switch $S_A$ and $S_B$ when interval $\Delta_3$ begins. Switch $S_A$ is turned off and Switch $S_B$ are turned on, see Fig. 20.

All energy stored in the voltage wave in (35) is transformed into a current wave

$$I_5^+ = -\frac{(N_{r_l} + N_{r_g})I_1^+ + V_{in}}{Z_0} = -\frac{6V_{in}}{Z_0} \approx -6.29\,A$$  \hspace{1cm} (37)

which propagates towards $S_C$. It reaches the other end after one $t_d$, the same time as interval $\Delta_4$ begins. The simulated value of $I_5^+$ is $-6.2A$ and is still close to the
theoretical one. The difference is greater compared to the simulated value in interval $\Delta_2$ because of the DC resistance losses in the LTL increases linearly dependant on the wave propagation time inside the LTL.

The load impedance is formed by the load ($R_{\text{load}}$) parallel with the output capacitor ($C_{\text{out}}$) according to

\[ Z_{L2} = \frac{R_{\text{load}} X_C}{R_{\text{load}}^2 + X_C^2} - j \frac{R_{\text{load}} X_C}{R_{\text{load}}^2 + X_C^2}, \]  

(38)

where $X_C$ is the reactance. The reactance can be found as

\[ X_C = \frac{1}{2 \pi f_{\text{sw}} C_{\text{out}}} \]  

(39)

where $f_{\text{sw}}$ is the switch frequency. In the simulation $R_{\text{load}}$ was set to 5.9Ω, $C_{\text{out}}$ to 50µF and the switching frequency to 277kHz. This result in a load impedance ($Z_{L2}$) of 0-0.0113jΩ and a reflection coefficient as

\[ \Gamma_{L2} = \frac{|Z_{L2}| - Z_0}{|Z_{L2}| + Z_0} \approx -0.9983 \]  

(40)

The reflection coefficient at $S_C$ is the same as $\Gamma_{L1}$ in (36), i.e 1.

### 4.1.4 Interval $\Delta_4$

The negative current wave, created during interval $\Delta_3$, has reached switch $S_C$ when interval $\Delta_4$ begins. Both $S_B$ and $S_C$ are on, see Fig. 21.
Chapter 4. Mathematical Model

The reflection coefficient at \( S_C \) is the same according to \( \Gamma_L \) in (29) and the reflection coefficient at the load impedance (\( C_{out} \) parallel to \( R_{load} \)) is according to \( \Gamma_{L2} \) in (40). The number of reflections at \( S_C \) and at the load can be calculated as

\[
N_{r_{11}} = \frac{DT_s - t_d}{2t_d} = 2 \tag{41}
\]

\[
N_{r_{12}} = \frac{DT_s - 2t_d}{2t_d} = 2 \tag{42}
\]

Since the reflection coefficient at the load is \( \Gamma_{L2} \), the current at switch \( S_C \) increases by \((1+\Gamma_{L2})\) every time the wave is reflected. Therefore the current barely increases during interval \( \Delta_4 \). Furthermore, it can be noticed in the simulation that all current will flow into the output capacitor. The current in a capacitor can be expressed as

\[
i = C \frac{dv_c}{dt} \tag{43}
\]

which gives that

\[
\Delta v_c = \frac{I_L \Delta t}{C} \tag{44}
\]

where \( \Delta v_c \) is the voltage difference during the time the capacitor is charged by the current \( I_L \). The current \( I_L \) can be assumed to be \( I_5^+ \) since it barely changes during interval \( \Delta_3 \) and \( \Delta_4 \). This gives a voltage difference according to

\[
\Delta v_c = \frac{I_5^- (\Delta t_3 + \Delta t_4)}{C} = 223 \text{ mV} \tag{45}
\]
which is close to the simulated one of 217mV. This assumption can only be made during the first cycles and it was only made to verify that (43) is accurate compared to the simulation. At subsequent cycles, the current amplitude varies more during interval $\Delta_3$ and $\Delta_4$ because of reflections. The increase of $v_c$ is therefore not linear during these intervals; it is rather equal to the increase in output voltage for each cycle. This is due to the fact that the capacitor is charged with energy during interval $\Delta_3$ and $\Delta_4$ every cycle. This results in an increased output voltage which eventually reaches a steady state DC value. The output voltage can be expressed as

$$ V_{out} = V + \Delta v_c $$

where $V$ is the output voltage from the previous cycle. If $t = 0$ and $C_{out}$ is assumed to be completely discharged when starting the converter, $V$ is initially zero.

The theoretical amplitude values of the current and voltage waves propagating in the LTL can be considered to be accurate compared to the simulation. As a result these mathematical models can be used to describe the currents and voltages propagating inside the LTL.

### 4.2 Transfer Function

One of the goals was to investigate the transfer function of the PBB converter. Therefore, a simulation of $V_{out}$ as a function of duty cycle was made. For the inverting mode, the simulated result can be seen in Fig. 22.

![Fig. 22 $V_{out}$ as a function of duty cycle for 14V input voltage in inverted mode.](image)

The solid line represents the simulated output voltage and the dashed an ideal Buck-Boost converter operating in continuous mode. As seen, the PBB converter in inverting mode works as a theoretical Buck-Boost converter. The transfer function can therefore be expressed as

$$ V_{out} = V + \Delta v_c $$

where $V$ is the output voltage from the previous cycle. If $t = 0$ and $C_{out}$ is assumed to be completely discharged when starting the converter, $V$ is initially zero.
Chapter 4. Mathematical Model

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-D}{1-D}.
\]  

(47)

For the non-inverting mode the result is different compared to the inverting mode, see Fig. 23. As seen, the output voltage increases until 50% duty cycle and decline as the duty-cycle is further increased. None of the regular power electronic converters have this kind of transfer function.

![Fig. 23 V_{\text{out}} as a function of duty cycle for 14V input voltage in non-inverting mode.](image)

If the steady state current in the LTL is studied when operating in non-inverting mode, it can be seen that the average is approximately zero for all duty cycles, see Fig. 24. During the time intervals \(\Delta_1-\Delta_2\) (the same time intervals as in section 4.1), the current increases almost linearly. When interval \(\Delta_3\) begins (\(S_A\) turns off, \(S_B\) turns on and \(S_C\) is kept in off state), the current polarity is changed to negative and start to increase almost linearly until next operation cycle were interval \(\Delta_3\) begin again. It can also be noted that the starting current (\(S_A\) turn on) and the maximum and minimum value of the current increases with duty cycle, see Table 1.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.3</td>
<td>-3.7</td>
<td>2.8</td>
<td>6.5</td>
<td>-388</td>
</tr>
<tr>
<td>30</td>
<td>1.8</td>
<td>-6.3</td>
<td>5.9</td>
<td>12.2</td>
<td>-451</td>
</tr>
<tr>
<td>50</td>
<td>0.0</td>
<td>-8.3</td>
<td>7.1</td>
<td>15.4</td>
<td>-194</td>
</tr>
<tr>
<td>70</td>
<td>-5.5</td>
<td>-9.0</td>
<td>7.2</td>
<td>16.2</td>
<td>-356</td>
</tr>
<tr>
<td>90</td>
<td>-6.8</td>
<td>-9.0</td>
<td>8.4</td>
<td>17.4</td>
<td>-151</td>
</tr>
</tbody>
</table>

Table 3 Steady state current data at different duty cycles \(D\).

Two common techniques to derive the transfer function of a DC/DC converter, is Fourier analysis or state space averaging (SSA) [12]. In the Fourier analysis
method the DC component of a waveform is given by its average value. For example, in a Buck converter the transfer function is derived from the average voltage over the inductor. This can’t be made with the PBB converter due to that the voltage across the LTL is varying with time and is depending on the reflection coefficients and the delay. Furthermore, in the SSA method, a Buck converter is modeled with Kirchhoff’s laws in its two circuit states, i.e when the switch is on and off. The equations are then converted into state space matrices and are averaged. This method can’t be used straight away either, since the PBB converter has a transmission line instead of an inductor. Moreover, it was shown that the steady state current in the PBB converter almost increases linearly. By studying the slope in Fig. 24, it almost corresponds to an inductor with the same value as the total inductance of 40 L elements in the LTL, i.e 4µH. It could therefore be assumed that the LTL can be modeled as an inductor. However, there are still problems to use the state space averaging method. The first problem is that the inductor will be floating during interval $\Delta_2-\Delta_3$. The second is that the current changes polarity when switch $S_A$ turn off and $S_B$ turn on. Due to these problems the transfer function was not derived. Further work has to be made.

Fig. 24 The simulated steady state current into the LTL with different duty cycles to the right.
Chapter 5

5 Inductance Design and Measurement

One of the goals was to obtain the same impedance for the new LTLs as the old one in order to be able to compare them regarding efficiency. This chapter explains the procedure to measure the inductance for the Coilcraft, U-cores and toroidal inductors. It also contains the measurement result and an analysis of the result.

5.1 Equipment

The test equipment used for the following measurements is listed in Table 4.

<table>
<thead>
<tr>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance Analyzer (IA)</td>
</tr>
<tr>
<td>Wayne Kerr precision IA 3245</td>
</tr>
<tr>
<td>Wayne Kerr precision IA 3245</td>
</tr>
</tbody>
</table>

5.2 Measurements

In all measurements the temperature was ~25°C. The inductance analyzer was set to 300kHz and 25mA AC.

5.2.1 Coilcraft Inductance

The inductor analyzer was used to measure two Coilcraft SLC7530S-101MLC inductances to verify if they correspond to the datasheet. Two short 1mm wires were soldered on each side of the inductors and connected to the crocodile clamps of the analyzer. The result of the two samples can be seen in Fig. 25. The inductance is within the tolerance of 100nH±20% for bias currents less than 5A. Furthermore, these measurements are hard to compare to the datasheet due to the manufacturers deficient descriptions of measurement setup. Therefore, this measurement should only be used for comparison for the U-cores.
Chapter 5. Inductance Design and Measurement

5.2.2 U-core Air Gap Adjustment

The inductor design of LTL\textsubscript{1} and LTL\textsubscript{2}, was made by placing the U-core on top of a ferrite plate. This quadratic plate designated TKD-EPC QU40/40/2, was 2mm thick and 40x40mm wide. In order to achieve an inductance of roughly 100nH, an air gap was required between the U-core and the ferrite plate. To achieve an air gap, different plastic films were evaluated. They were placed between the Ferrite plate surface and the U-core. Moreover, a 1mm thick wire were routed between the U-core legs and connected to the analyzer, see Fig. 26. Furthermore, an undefined mechanical force $F_{\text{mech}}$ was applied on top of the U-cores in order to obtain accurate inductance result.

![Fig. 25 Inductance as a function of bias current for Coilcraft inductor samples.](image)

The measured inductance for five U-core samples with different plastic films can be found in Table 5. Since the values should be as close as possible to 100nH, it
can be noticed that one layer of 0.0254 mm plastic film gives the best result. It was also observed that the ferrite surface affected the inductance value by 8.5-10nH depending on position during the measurement. The minor impact was neglected.

Table 5 The U-core inductance with different plastic films for five samples.

<table>
<thead>
<tr>
<th>Plastic film</th>
<th>Sample #001 [nH]</th>
<th>Sample #002 [nH]</th>
<th>Sample #003 [nH]</th>
<th>Sample #004 [nH]</th>
<th>Sample #004 [nH]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0254</td>
<td>88.5</td>
<td>94.0</td>
<td>91.5</td>
<td>93.0</td>
<td>92.0</td>
</tr>
<tr>
<td>0.0508</td>
<td>58.0</td>
<td>61.0</td>
<td>60.0</td>
<td>60.0</td>
<td>60.0</td>
</tr>
<tr>
<td>0.0762</td>
<td>41.0</td>
<td>43.0</td>
<td>42.5</td>
<td>42.5</td>
<td>41.0</td>
</tr>
<tr>
<td>1.7780</td>
<td>39.5</td>
<td>30.0</td>
<td>30.0</td>
<td>32.0</td>
<td>31.0</td>
</tr>
</tbody>
</table>

5.2.3 Ferrite U-core Inductance

Different DC bias currents were applied to 80 U-core samples with a 0.0254mm thick plastic film between the U-core and ferrite surface. The force applied on top of the U-core was measured with a precision scale and varied between 7.76-7.95Nm. The small variation in force was observed to not affect the measured inductance, due to the inductor analyzer accuracy of 0.5nH. However, during measurement, it was noted that the inductance value varied depending on the analyzer temperature and wire and ferrite surface position. With all these factors taken into account, the measurement uncertainty was estimated to be ±4nH. The inductor analyzer was therefore calibrated before and after each U-core measurement.

The result for the 40 U-cores used in LTL$_1$ and LTL$_2$ can be seen in Fig. 27 and Fig. 28. The circles, shown as vertical thick lines, represent the measured values at different bias currents. The dotted lines show the interval between the lowest and highest values and the numbers point out the minimum and maximum value of each measuring node. It can also be seen, that the inductance value is slightly lower than the two Coilcraft samples in section 5.2.1 up to 10A. At 10A bias current the inductance value for the U-cores and Coilcraft inductances deviate roughly 20% from the inductance value at zero bias current. This is considered acceptable.

In section 4.2, it was shown in a simulation that the highest current magnitude in steady state would be 9A at 90% duty cycle. However, as mentioned in 3.2, it is not reasonable to operate the PBB converter at really low or high duty cycle, due to the decrease in efficiency. Therefore, the current of 8.3A at 50% duty cycle is considered to be the maximum current for the design of inductor cores. Since it is lower than 10A and has a decent safety margin of roughly 17%, the U-cores was accepted for use in the PBB converter.
5.2.4 Ferrite Toroidal Core Inductance

To verify that the toroidal core for LTL3 has acceptable inductance when bias current is applied, the inductance of one sample of Amidon FT-23-77 and two samples of Amidon FT-23-43 toroidal cores were measured. As seen in Fig. 29, the two samples of FT-32-43 are far away from 100nH and saturates at less than 1A. It is much lower than the simulated current of 8.3A at 50% duty cycle. Therefore, these toroids will be saturated and if used in the PBB converter, the efficiency will be reduced compared to the U-cores. The result of the FT-32-77 sample is shown in Fig.
30. It can be seen that the inductance varies too much and as a result was excluded for further use in the converter.

Fig. 29 Inductance as a function of bias current for two samples of the toroid FT-23-43.

Fig. 30 Inductance as a function of bias current for one sample of the toroid FT-23-77.
Chapter 6

6 LTL Impedance Measurement

It was shown in the previous chapter that the inductance value for the U-cores was close to the Coilcraft inductances up to 10A and the toroids between 0.4-0.7A. This doesn’t necessarily mean they have the same total impedance as LTL₀ if they are put inside LTL₁-₃. In order to be able to compare if the impedance of LTL₁-₃ is close to the LTL₀, the LTLs were assembled and the impedance as a function of frequency was measured. The assembled LTLs can be seen in Fig. 31.

![Fig. 31 The different LTLs; from left LTL₁, LTL₂ and LTL₃.](image)

6.1 Equipment

The measurement equipment used for the impedance measurement is listed in Table 6.

<table>
<thead>
<tr>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vector Network Analyzer</td>
</tr>
<tr>
<td>Rohde &amp; Schwarz ZVC</td>
</tr>
<tr>
<td>Impedance/Gain-phase Analyzer</td>
</tr>
<tr>
<td>HP4194A</td>
</tr>
<tr>
<td>HP16034B test tweezers</td>
</tr>
</tbody>
</table>
6.2 Measurement Setup

The input impedance was measured in two ways. The first way was to measure the input reflections (complex $\Gamma$) by sinusoidal waves with different frequencies and derive the impedance from

$$Z_{\text{in}} = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

(48)

where $\Gamma$ is the reflection coefficient and $Z_0$ is the characteristic impedance [13]. A vector network analyzer Rohde & Schwarz ZVC was used. The other way was to measure the absolute input impedance $|Z_{\text{in}}|$ with an impedance analyzer HP4194A.

For the reflection measurement method, the output power of the sinusoidal wave was set to -10dBm, the start frequency to the lowest possible i.e (20kHz) and the end frequency to 5MHz. Coaxial cables were soldered to the input and the output were short circuit to ground with a 1mm thick wire for each LTL. The instrument was calibrated with each coaxial cable for short circuit, open circuit and with a matched resistor of 50Ω before the cables were soldered on the LTLs.

To obtain the characteristic impedance, the values for the Coilcraft inductor and Murata capacitor were used in (48), i.e L was set to 100nH, C to 560pF and the resistance to 0.123mΩ which is the DC resistance value of the inductor. $G$ was set to zero due to the problem of approximating the conductance of a surface mounted inductor and capacitor. The ESR value of the capacitance was neglected due to its minor impact on $R$. It can also be noted that the characteristic impedance depends on the frequency. However, this was neglected, since the impact is considered to be insignificant.

For the impedance measurement, the start frequency was set to the lowest possible (i.e 100Hz) and the end frequency to 5MHz. To measure the input impedance, HP16034B test tweezers were used on the input and output of the LTL. The instrument was calibrated with the tweezers for short circuit, open circuit and with a matched resistor of 50Ω.

An acrylic glass device was used to keep constant and even pressure on the U-cores in LTL1 and LTL2. In addition for LTL2, the center U-cores were loose, due to height tolerances. Hence, a strip of the same plastic film as between the Ferrite surface and U-core was used in order to apply more even pressure on the U-cores. Furthermore, two 1mm thick wires were soldered on the input and output for the impedance measurement, see Fig. 32 and 33 for LTLs with additional connections. For complete LTL specifications, see appendix D.
Chapter 6. LTL Impedance Measurement

Fig. 32 Two acrylic plates tighten under and above LTL₁ and LTL₂. A strip of purple film was used on the center lines of U-cores to apply even pressure.

Fig. 33 A coaxial cable and 1mm wire soldered on LTL₃.

6.3 Measurements

The first conclusion from the measurement is that the input impedance varied depending on the type of measurement instrument. It can be seen in Fig. 34 that the input impedance measured with Rohde & Schwarz network analyzer has an offset of roughly 8dB compared to the same measurement with the HP4194 impedance analyzer. The same behavior was recorded for all four LTLs and it is believed to origin from a vaguely described offset in the operation manual. The manual mentions that there could be an offset varying between 0-9dB without further explanations. Consequently, that is why two instruments were used to validate the result.

It can also be seen in Fig. 34 that LTL₀ almost had the same resonance frequency as the theoretical curve. This is most likely because all 40 Coilcraft inductances had the average value close to 100nH. It can also be noted that the two Coilcraft inductor samples measured in section 5.2.1, had less than 100nH, but it is known from Table 1 that they have a ±20% tolerance. The capacitors have a tolerance of ±5pF which do not affect the resonance frequency in a distinguishable way.
Chapter 6. LTL Impedance Measurement

Fig. 34 The theoretical and measured input impedance independent of characteristic impedance for LTL₀. The instrument used for this measurement is Rohde & Schwarz vector analyzer and HP4194A impedance analyzer.

The measured impedance for LTL₁ and LTL₂ shows that they have a slightly higher resonance frequency than LTL₀, see Fig. 35. This is reasonable since all the measured U-cores in section 5.2.3 had an inductance lower than 100nH at zero bias current. It can also be seen that LTL₃ has the lowest resonance frequency. This is also reasonable, since the toroid samples in section 5.2.4 were measured to have an inductance of roughly 50nH higher than 100nH. Furthermore, the total DC resistance value for LTL₁₋₃ was several times lower than for LTL₀, see Table 7.

Fig. 35 The input impedance independent of characteristic impedance on all LTLs measured with HP4194A impedance analyzer.
### Table 7 Total DC resistance for each LTL.

<table>
<thead>
<tr>
<th>LTL</th>
<th>DCR [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>18.6</td>
</tr>
<tr>
<td>1</td>
<td>5.96</td>
</tr>
<tr>
<td>2</td>
<td>1.55</td>
</tr>
<tr>
<td>3</td>
<td>3.06</td>
</tr>
</tbody>
</table>
Chapter 7

7 Efficiency Optimization

In the previous chapter, the LTLs were compared to each other with respect to impedance as a function of frequency. This chapter analyzes the optimum efficiency of the PBB converter with the different LTLs. The optimization is done in non-inverting mode.

7.1 Measurement Setup

To control the MOSFETS and not have the same ground potential for all switches (Source on \( S_A \) and \( S_B \) is not connected to ground), digital isolators and drive circuits is used in the PBB converter. Four power supplies were used to supply the isolators, drivers and the power stage of the converter. The isolator voltages were set to 3.3V, the driver voltages to 5.5V and the input voltage was set to maximum 14V. The input, output and driver voltages and currents were measured using both true RMS multimeters and oscilloscope probes. The gate patterns were created using an Agilent 16903A logic analysis system, see Fig. 36 for measurement setup.

![Fig. 36 Measurement setup for efficiency measurement with the different LTLs.](image-url)
When LTL\_1,3 was connected to the converter, the first and last L element of LTL\_0 was removed from the converter. Two 2mm thick copper wire were then soldered between the original input and output of LTL\_0 to the input and output of the LTL, see Fig. 37. The LTL was also connected to the same ground plane as the rest of the converter via a ground wire.

![Diagram of Prime Buck-Boost converter with LTL1 connected.](image)

**Fig. 37** Prime Buck-Boost converter with LTL\_1 connected.

For the following measurements the input power can be found as

\[ P_{in} = P_{drv} + P_{PwSt} + P_{iso} \]  (49)

where \( P_{drv} \) is the driver power, \( P_{PwSt} \) the PowerStage input power and \( P_{iso} \) the isolator power. The isolator power is low (<2mW) and fairly constant. Thus, it was considered negligible and not recorded. \( P_{drv} \) and \( P_{PwSt} \) can be calculated as

\[ P_{drv} = (V_{drvA} I_{drvA}) + (V_{drvB} I_{drvB}) + (V_{drvC} I_{drvC}) \]  (50)

\[ P_{PwSt} = V_{PwSt} I_{PwSt} \]  (51)

The output power is defined as

\[ P_{out} = V_{out} I_{out} \]  (52)

and the efficiency and powerstage efficiency can be calculated as

\[ \eta = 100 \frac{P_{out}}{P_{in}} \]  (53)

\[ \eta_{PwSt} = 100 \frac{P_{out}}{P_{PwSt}} \]  (54)
Chapter 7. Efficiency Optimization

7.1.1 Equipment

The test equipment can be found in Table 8. Some components were removed and changed on the prototype converter before the efficiency was measured, see Appendix C.

Table 8 Test equipment for the following measurements.

<table>
<thead>
<tr>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic analysis system and equipment</strong></td>
</tr>
<tr>
<td>Agilent 16903A</td>
</tr>
<tr>
<td>Agilent 16720A Pattern Generator (module)</td>
</tr>
<tr>
<td>Agilent 16522-61601 Output Cable</td>
</tr>
<tr>
<td>Agilent 10566A 3-state TTL / 3.3 Data Pod</td>
</tr>
<tr>
<td><strong>Power Supplies</strong></td>
</tr>
<tr>
<td>TTI EX354D</td>
</tr>
<tr>
<td>Powerbox 3000 B</td>
</tr>
<tr>
<td>Powerbox 3000 B</td>
</tr>
<tr>
<td>Delta Elektronika SM 7020-D</td>
</tr>
<tr>
<td><strong>Multimeter (True RMS Multimeter)</strong></td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Fluke 87</td>
</tr>
<tr>
<td>Tektronix TX3</td>
</tr>
<tr>
<td><strong>Oscilloscope and probe</strong></td>
</tr>
<tr>
<td>LeCroy WaveSurfer 44MXsB 400 MHz</td>
</tr>
<tr>
<td>LeCroy PP005A 500Mhz Probe</td>
</tr>
<tr>
<td>LeCroy PP006A 500 Mhz Probe</td>
</tr>
<tr>
<td>LeCroy AP015</td>
</tr>
<tr>
<td><strong>IR Camera</strong></td>
</tr>
<tr>
<td>Flir ThermaCam 300</td>
</tr>
<tr>
<td><strong>Adjustable load</strong></td>
</tr>
<tr>
<td>Metrel 100Ω 1,8A</td>
</tr>
<tr>
<td>Berco 5Ω</td>
</tr>
</tbody>
</table>

7.2 Measurements

The efficiency optimization was done in the following procedure:

1. Measurement of LTL delay time.
2. Switch frequency and switch $S_C$ off time adjustment.
3. Introduction of dead time between $S_A$ and $S_B$.
4. Adjustment of the load until $V_{out}$ correspond to 50 % of $V_{in}$.
5. Recording of efficiency with RMS multimeters and oscilloscope probes.
7.2.1 LTL delay time

The delay time, i.e. the time it takes for the voltage wave to travel back and forth along the LTL, was measured by applying a short voltage pulse into the LTL. This was achieved by turning on switch $S_A$ for a short period, turn it off and let switch $S_B$ conduct for a long time. By doing this, the reflections in the voltage wave could be measured over time, see Fig. 38.

![Reflections along LTL when applying a short pulse.](attachment:image.png)

The delay time can be found with

$$T_s = \frac{\Delta x}{M}$$

where $\Delta x$ is the time interval between the reflections and $M$ is the number of reflections. In order to obtain an accurate result, the mean time value was calculated for five reflections. The result for the different LTLs can be found in Table 9.

<table>
<thead>
<tr>
<th>LTL</th>
<th>Delay [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>606.2</td>
</tr>
<tr>
<td>1</td>
<td>549</td>
</tr>
<tr>
<td>2</td>
<td>535.8</td>
</tr>
<tr>
<td>3</td>
<td>783.4</td>
</tr>
</tbody>
</table>

The theoretical delay time with an inductance of 100nH and a capacitance of 560pF can be calculated as
\[ T_s = 2t_d = 2N\sqrt{LC} = 2 \cdot 40 \cdot \sqrt{100 \cdot 10^{-9} \cdot 560 \cdot 10^{-12}} = 599\text{ns}. \] (56)

The delay time of LTL_0 is close to the theoretical one; meanwhile LTL_{1,2} has a slightly shorter delay time and LTL_3 a longer delay. This seems reasonable compared to the impedance measurements in section 6.3, since the first resonance frequency is lower for LTL_3 and higher for LTL_{1,2}, compared to LTL_0.

7.2.2 Switch Frequency

The switch frequency plays a big role in how high the efficiency becomes. A simplified explanation is that if the switch frequency is high, the switching losses in the MOSFET increase. It also results in a higher power demand for the MOSFET drivers and as a consequence lowers the efficiency. On the other hand, if the switch frequency is too low, the imaginary part of the converter inductive impedance decreases and the DC resistance becomes more distinct. Hence, the losses increase.

The clock period of the pattern generator was put to a 100\textsuperscript{th} of the delay time. This means that 2t_d equals 100 segments. This was made because of the pattern generator had a limiting clock frequency between 1MHz and 300MHz. It was also a way to easily decrease the switch frequency by adding 100 segments each time. Consequently, the switch frequency is adjusted as an integer of 2t_d and could not be set to arbitrary values. This had to be accepted since no other options were available.

7.2.3 Input Voltage

It was seen that the efficiency increased when the input voltage increased. A limiting factor of the input voltage was the LTL capacitor voltage at switch S_C (LTL output end). According to the capacitor datasheet, it has a maximum recommended voltage of 50V. However, if an input voltage of 14V with 50% duty cycle were used, it resulted in a voltage wave with a magnitude of 102V in LTL_0, see Fig. 39. Therefore, no further increase on input voltage was made. The voltage wave amplitude for the other LTLs was roughly the same.
7.2.4 Switch $S_C$ Off Time

The time it takes for the voltage and current waves to propagate back and forth along the LTL, has been mentioned to be $2t_d$. Switch $S_C$ must therefore be turned off $2t_d$ to completely inverse the voltage wave polarity. In reality the wave is no ideal square pulse and has a certain fall and rise time. It is also partially outspread over a slightly longer time interval because of dispersion. Consequently, some parts of the wave will not be inverted if the off time is exactly $2t_d$. The non-inverted wave will add up to the inverted wave and result in a decrease in efficiency, see Fig. 40a. The black line represent $V_{GS}$ in switch $S_C$, the blue dashed line the ideal wave and the dotted red one the real voltage wave divided by 10 at $S_C$. As seen a part of the tail is not included during the off time of switch $S_C$. In Fig. 40b the same measurement is done, but with an increase of switch $S_C$ off time. It can be seen that the tail is more included which result in less losses and higher efficiency. The efficiency as a function of switch $S_C$ off time can be found in Fig. 41. An increase of the off time above 100 segments ($2t_d$) increase the efficiency for each LTL.
Chapter 7. Efficiency Optimization

7.2.5 Dead Time for Switch $S_A$ and $S_B$

To avoid cross conduction losses, dead time is normally introduced in power electronic converters. The purpose is to avoid the high side switch to conduct at the same time as the low side switch, or vice versa. This is done by adding a delay time, according to the fall time of the $V_{DS}$ voltage for both switches.
Introducing dead time to switch $S_A$ and $S_B$ surprisingly decreased the efficiency for each LTL. The cause is believed to be that the increased energy accumulation, due to the longer conduction time of switch $S_A$, is higher than the cross conduction losses. Therefore, no dead time were introduced, see Fig. 42. It can be seen that $S_A$ and $S_B$ in LTL_0 are on a short interval at the same time. The duty cycle was set to 50% and $S_C$ off time to 116 segments during this measurement.

![Graph](image)

**Fig. 42 Switch $S_A$ and $S_B$ going from ON to OFF and vice versa for LTL_0.**

### 7.2.6 Efficiency Non-Inverting Operation

To give a perspective of the efficiency, the load was adjusted until the output voltage reached 50% of the input voltage at 50% duty cycle. The efficiency and the parameters for the efficiency optimization were then recorded, see Table 10.

<table>
<thead>
<tr>
<th>LTL</th>
<th>Delay [ns]</th>
<th>Switch freq [kHz]</th>
<th>$S_C$ off time [ns]</th>
<th>Deadtime [ns]</th>
<th>Vin [V]</th>
<th>Iin [mA]</th>
<th>Vout [V]</th>
<th>Iout [mA]</th>
<th>$\eta$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>606</td>
<td>206</td>
<td>703.0</td>
<td>0</td>
<td>14</td>
<td>1583</td>
<td>7</td>
<td>2239</td>
<td>69.7</td>
</tr>
<tr>
<td>1</td>
<td>549</td>
<td>303</td>
<td>713.7</td>
<td>0</td>
<td>14</td>
<td>948</td>
<td>7</td>
<td>1597</td>
<td>81.4</td>
</tr>
<tr>
<td>2</td>
<td>536</td>
<td>312</td>
<td>664.4</td>
<td>0</td>
<td>14</td>
<td>1082</td>
<td>7</td>
<td>1793</td>
<td>80.5</td>
</tr>
<tr>
<td>3</td>
<td>783</td>
<td>213</td>
<td>1378.8</td>
<td>0</td>
<td>4</td>
<td>435</td>
<td>2</td>
<td>142</td>
<td>13.8</td>
</tr>
</tbody>
</table>

In the right column the efficiency of LTL_1-2 is roughly 11% better than LTL_0. The reason is most likely that the total DC resistance in LTL_0 was three times greater than in LTL_1 and nine times greater than in LTL_2, see section 6.3. It can also be noted, that the input voltage for LTL_3 was set to 4V and the LTL had much lower...
efficiency. It was shown in section 5.2.4 that the FT-23-44 toroid varies a lot in inductance and saturate at low currents. This means that a low voltage is beneficial for the efficiency. It also means that the drive power is relatively big compared to the input voltage. Thus, the efficiency is much lower compared to the other LTLs. Moreover, the simulation of PBB converter efficiency made in section 3.2, showed an efficiency of 90.5%. It is approximately 10% higher than for LTL\(_1\).

It has been mentioned that the switching frequency could not be set to arbitrary values. As a consequence, the optimum frequency may not have been achieved for the LTLs. This means that the efficiency could be slightly better at switch frequencies close to the ones in the table. Furthermore, the above result corresponds to 50% duty cycle. If the duty cycle is decreased or increased, the efficiency becomes lower, see Fig. 43. The load is constant and set to 5.9Ω for each LTL. The efficiency of LTL\(_0\) is therefore higher than the efficiency when the output voltage was set to 50% of the input voltage.

![Efficiency as a function of duty cycle for the different LTLs at R\(_{\text{load}}\)=5.9Ω.](image)

**7.3 Increase of LC Elements**

The simulation in section 3.3 was performed in order to investigate what happens with the efficiency if an increase or decrease of LC elements were made. The same was done with the real PBB converter, except that the LC elements were only increased, because of the risk of too high currents at higher switch frequency. In section 7.2.6, LTL\(_1\) had the highest efficiency. Therefore, two more LTL\(_1\) were built and connected in series, see Fig. 44. The first and last L elements of LTL\(_0\) were removed. Two 2mm thick copper wire were then soldered between the original input and output of LTL\(_0\) to the input and output of the two LTL\(_1\)s. Furthermore, a ground wire was connected to the converter ground plane.
Chapter 7. Efficiency Optimization

The same process as in the previous efficiency measurements was made, i.e. LTL delay time was measured, switch frequency were adjusted, the $S_C$ off time was set, the load was adjusted until $V_{out}$ corresponded to 50% of $V_{in}$ at 50% duty cycle and the efficiency was recorded. This was made with an increase of 8 LC elements at a time. The idea of doing this was to see how the efficiency depends when the switch frequency is decreased because of the increased number of LC elements. The efficiency was measured in non-inverting mode, see Fig. 45.

![Fig. 44 Measurement setup with 2x LTL1 series connected.](image)

![Fig. 45 Simulated and measured efficiency as a function of number of LC elements and different switch frequency segments.](image)

The dotted line represent the simulated result from section 3.3. The solid black line represents the efficiency when the switching frequency was put to 300 segments.
Chapter 7. Efficiency Optimization

for both switch $S_A$ and $S_B$. The dashed represent the same except the switching frequency was put to 400 segments instead. As, seen the efficiency has a maximum at 48 elements and a minimum at 56 and 72 elements dependant on the switch ratio (number of segments). Compared to the simulation, the result is different. According to the simulation it has a minimum at 40 and 64 elements. The difference is less distinct as for the measured result. Since the procedure to measure and simulate the efficiency is a slow and expensive process, no further work was done.

The data records for switch frequency equal to 300 segments can be seen in Table 11.

Table 11 Data records with different numbers of LC elements.

<table>
<thead>
<tr>
<th>Number of LC elements</th>
<th>Delay [ns]</th>
<th>Switch freq [kHz]</th>
<th>$S_C$ off time [ns]</th>
<th>Deadtime [ns]</th>
<th>Vin [V]</th>
<th>Iin [mA]</th>
<th>Vout [V]</th>
<th>Iout [mA]</th>
<th>$\eta$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>503</td>
<td>332</td>
<td>624</td>
<td>0</td>
<td>14.00</td>
<td>1027</td>
<td>7.01</td>
<td>1696</td>
<td>79.87</td>
</tr>
<tr>
<td>48</td>
<td>607</td>
<td>275</td>
<td>753</td>
<td>0</td>
<td>14.01</td>
<td>1064</td>
<td>7.01</td>
<td>1766</td>
<td>80.79</td>
</tr>
<tr>
<td>56</td>
<td>721</td>
<td>232</td>
<td>836</td>
<td>0</td>
<td>14.02</td>
<td>1132</td>
<td>7.00</td>
<td>1824</td>
<td>78.71</td>
</tr>
<tr>
<td>64</td>
<td>822</td>
<td>203</td>
<td>954</td>
<td>0</td>
<td>14.01</td>
<td>1336</td>
<td>7.02</td>
<td>1999</td>
<td>73.72</td>
</tr>
<tr>
<td>72</td>
<td>923</td>
<td>180</td>
<td>1071</td>
<td>0</td>
<td>14.00</td>
<td>1735</td>
<td>7.02</td>
<td>2374</td>
<td>67.83</td>
</tr>
<tr>
<td>80</td>
<td>1037</td>
<td>160</td>
<td>1203</td>
<td>0</td>
<td>13.99</td>
<td>1328</td>
<td>7.01</td>
<td>1993</td>
<td>74.24</td>
</tr>
</tbody>
</table>

7.4 Double $S_C$ switching

In the previous measurements and defined in section 2.5, switch $S_C$ has been kept in off state for at least $2t_d$ centered when $S_A$ is turned off and $S_B$ is turned on. This section will show what happens with the efficiency if $S_C$ is also kept in off state when $S_B$ is turned off and $S_A$ is turned on, see Fig. 46. The idea was to convert the current wave into a voltage wave and convert it back to a current wave with opposite sign (see appendix E) in the interval $7t_d$-$9t_d$. Thus, in theory an increase of efficiency would be obtained.

![Fig. 46 Switching pattern for switch $S_A$, $S_B$, and $S_C$ for 50 % duty cycle.](image-url)
Chapter 7. Efficiency Optimization

The efficiency was shown to be roughly the same as in section 7.2.6, i.e. for operation with single $S_C$ switching in non-inverting mode, see Table 12. The efficiency is between 0.5-2% lower for each LTL compared to single $S_C$ switching. It is believed to be because of at $8t_d$ the current wave polarity should not be inverted, i.e. keep the same polarity as the voltage wave. Moreover, the $S_C$ off time is the total time for both off states in each converter cycle.

Table 12 Data records for each LTL at 50% duty cycle with double $S_C$ switching.

<table>
<thead>
<tr>
<th>LTL</th>
<th>Delay [ns]</th>
<th>Switch freq [kHz]</th>
<th>$S_C$ off time [ns]</th>
<th>Deadtime [ns]</th>
<th>Vin [V]</th>
<th>Iin [mA]</th>
<th>Vout [V]</th>
<th>Iout [mA]</th>
<th>$\eta$ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>606.2</td>
<td>206</td>
<td>1406</td>
<td>0</td>
<td>14.00</td>
<td>1610</td>
<td>7.01</td>
<td>2259</td>
<td>68.98</td>
</tr>
<tr>
<td>1</td>
<td>549.0</td>
<td>303</td>
<td>1427</td>
<td>0</td>
<td>14.00</td>
<td>989</td>
<td>7.01</td>
<td>1617</td>
<td>78.49</td>
</tr>
<tr>
<td>2</td>
<td>535.8</td>
<td>312</td>
<td>1329</td>
<td>0</td>
<td>14.01</td>
<td>1088</td>
<td>7.00</td>
<td>1814</td>
<td>80.06</td>
</tr>
<tr>
<td>3</td>
<td>783.4</td>
<td>213</td>
<td>2758</td>
<td>0</td>
<td>4.05</td>
<td>77.8</td>
<td>2.00</td>
<td>39.7</td>
<td>11.05</td>
</tr>
</tbody>
</table>
Chapter 8

8 Prime Buck-Boost DC/AC Function

In section 3.4, it was shown that the PBB converter is able to perform a DC/AC conversion. To verify the simulations, the real converter was also tested. This chapter explains the procedure and result of the converter in DC/AC mode with LTL. LTL was chosen because it had the highest efficiency in section 7.2.6. The measurement setup is the same as in section 7.1 and all gate patterns were manually created with the logic analyzer system.

8.1 Transition from Negative to Positive Output Voltage

The DC/AC function was tested by applying a DC voltage $V_{in}$ and converting it to an alternating output voltage $V_{out}$ of approximately ±7V, see Fig. 47 for circuit diagram. To get an output voltage of ±7V the load $R_{load}$ was set to 4.6Ω and the duty cycle to 33% for both inverting and non-inverting mode. $S_C$ off time was set to 120 segments.

![Fig. 47 Circuit diagram of Prime Buck-Boost with DC/AC configuration.](image)

To verify the transition from negative (-7V) to positive (+7V) output voltage, the converter was configured to operate in inverting mode, i.e by letting $S_C$ conduct constantly. The output voltage was made sure to have settled to a constant -7V before switching into non-inverting mode a couple of cycles later. $V_{GSA}$, $V_{GSB}$, $V_{GSC}$ and $V_{out}$ was recorded, see Fig. 48. As seen the duty cycle is 33% between $S_A$ and $S_B$, switch $S_C$ goes from constantly on to modulation in non-inverting mode and $V_{out}$ increases almost linearly. The whole transition from -7V to +7V is shown in Fig. 49.
Chapter 8. Prime Buck Boost DC/AC Function

**Fig. 48** Start of transition from negative to positive output voltage.

**Fig. 49** Full transition from negative to positive output voltage.
8.2 Low Frequency AC Modulation of Output Voltage

In section 3.4 it was shown that a DC/AC conversion is possible with the PBB converter. To verify that it works, a low frequency modulation was applied to the gate voltage of switch \( S_C \). A transition from approximately negative (\(-7V\)) to positive (7V) output voltage, or vice versa, was effectuated every 10ms to create a 50Hz AC output voltage. To get an output voltage of \( \pm 7 \text{V} \) the load \( R_{\text{load}} \) was set to 4.6\( \Omega \) and the duty cycle to 33\% for both modes. The switch frequency for the switches \( S_A, S_B \) (and \( S_C \) during non-inverted mode) was set to 313 kHz. The gate pattern was manually created to get a square wave output voltage modulation. Fig. 50 shows \( V_{\text{in}}, I_{\text{in}}, V_{\text{out}} \) and \( I_{\text{out}} \) during ten cycles. As seen a continuous DC/AC conversion is possible with the PBB converter.

The RMS values of the output and input voltage and current was measured with the oscilloscope. It resulted in an efficiency of 69\% with drive power losses taken into consideration. Compared to the simulation, the efficiency is almost 14\% lower which was surprisingly low. Since an old test measurement with LTL showed an efficiency of 81.6\% in DC/AC mode. The converter was therefore tested in non-inverting and inverting mode in order to investigate if it works correctly. For the non-
inverting mode the efficiency was roughly the same as in section 7.2.6, i.e 81.4%, but for the inverting mode it was 67.4%. Another test measurement with the same setup, but with LTL0 instead, showed an efficiency of 87.7%. This explains the higher efficiency of 81.6% in DC/AC mode. The difference between the latest DC/AC measurement and the old one, is believed to be because of two $S_c$ MOSFETs were burnt during the latest DC/AC measurement. During these two faults something may have happened to other components or the replacement MOSFET was malfunctioning, since the efficiency in inverting mode was measured to 67.4%. It should be equal or higher than 87.7%.

### 8.3 $V_{\text{out}}$ as a Function of Duty Cycle

A simulation was made in section 4.2 where $V_{\text{out}}$ was plotted as a function of duty cycle. The same was made for the converter with the same measurement setup as in section 7.1. $V_{\text{out}}$ was measured as a function of duty cycle for both operations modes. For the inverting mode the result can be seen in Fig. 51.

![Graph]

*Fig. 51 Theoretical and measured output voltage as a function of duty cycle in inverting mode.*

The solid lines represent the measured values for different input voltages. The dashed lines represent the output voltage for an ideal Buck-Boost converter operating in continuous mode where the transfer function is according to (1). It can be noticed the PBB in inverting mode works as a regular Buck-Boost converter. The small difference is because of the losses in the real converter. For the inverting mode the result has the same shape as in the simulation in section 4.2, see Fig. 52.
Fig. 52 Measured output voltage as a function of duty cycle in non-inverting mode.
Chapter 9

9 Conclusions

In this thesis work, it is shown that it is possible to build smaller lumped transmission lines (LTLs) with U-cores and toroidal cores instead of using surface mounted inductors. The target impedance was not achieved with the toroidal LTL since the inductance saturated at 1A and varied a lot as a function of DC current. The same impedance was achieved with the U-core LTLs for frequencies up to 1MHz and was slightly different at higher frequencies.

Compared to a Prime Buck Boost converter with surface mounted inductors, the converter efficiency was increased with 11% with the U-core LTLs and decreased by 55% with the toroidal core LTL. The increase in efficiency for the U-core LTLs makes the PBB converter a more attractive solution for power conversion. However, the building concept of using a plastic film to create an air gap is not optimal. It is too dependant on mechanical tolerances and equal pressure on top of the U-cores. An investigation of other alternatives, such as using E-cores with a gapped middle leg or open toroidal cores is proposed.

The efficiency for LTL\textsubscript{1} in non-inverting mode was measured to 81.4% and simulated to 90.5%. The result is reasonable and is an efficiency increase of roughly 12% compared to the old LTL. Furthermore, it was shown in both simulations and measurements, that a DC/AC conversion is possible for the PBB converter. The efficiency was measured to 69% with the U-core LTL\textsubscript{1} which is considered low, since a test measurement with the old LTL showed an efficiency of 81.6%. The difference between the measurements is believed to be because of a malfunctioning MOSFET (S\textsubscript{C}), since an efficiency of 67.4% in inverting mode was measured when it was expected to be approximately 85%.

The function of efficiency as a number of LC elements could not be derived. In order to obtain a function from measured data, new measurement has to be performed with LC elements lower than 40 and higher then 80. A simulation with the same conditions could also be of value. Moreover, double S\textsubscript{C} switching was shown to not increase the efficiency compared to single S\textsubscript{C} switching. It was also shown that transmission line theory can be used to explain how the PBB converter works during its different switching states. The transfer function was shown to be the same as a regular Buck-Boost converter in inverting mode. For non-inverting mode the transfer function has a typical hyperbolic characteristic.

Disregard of the size of the Prime Buck Boost converter, it is an interesting concept that has the possibility to perform AC/DC and DC/AC power conversion, with fewer semiconductors than the conventional solutions. With further work, the size of the PBB converter can be reduced with other types of inductor cores and the efficiency may increase.
9.1 Future work

The Prime Buck Boost converter is proven to work in DC/DC and DC/AC conversion with decent efficiency. However, an investigation of how and in what applications the converter is usable has not been done. In order to make the converter attractive for the power market a study of cost, reliability and other possible application areas is of value for future work. The size of the converter is therefore one important aspect. If E-cores with gapped middle leg or open toroidal cores are used, it may reduce the build complexity and size of the converter. It may also increase the efficiency. Therefore, a new LTL prototype study is suggested. It should investigate other inductor cores and if the LTL can be reduced to fewer LC elements. A theoretical explanation of efficiency as a number of LC elements is therefore also of importance. Moreover, the derivation of transfer function in non-inverting mode could be of interest. An idea is to model the transmission line as a delay transfer function or look into how a floating inductor can be modeled during interval $\Delta_2 - \Delta_3$ since switch $S_C$ is kept in off state. Finally, the main idea of the converter is to use it for AC/DC conversion. Instead of using MOSFETs as in the existing prototype, they should be replaced with GaN switches without body diodes and the AC/DC conversion could be verified.
10 References


Chapter 10. References


Appendix A

A LTL Drawings

The drawings for LTL₁-₃, U-cores and toroids can be found below. The measurements are in millimeters.

A.1 LTL₁
Appendix A. LTL Drawings

A.2 LTL$_2$

Terminal Laminate

TDK-EPC U8/6/2

35 um Film

TDK-EPC QU40/40/2

35 um Film

Terminal Laminate

Mid Laminate

End Laminate

Mid Laminate with cores shown

GND IN OUT GND

TDK-EPC QU40/40/2

35 um Film
Appendix A. LTL Drawings

A.3 LTL₃

[Diagram of LTL₃ with labels for GND, OUT, IN, Terminal Laminate, Mid Laminate, Top Laminate, and specifications including AWG12, Dₓ=2.06, Dₓ=urtles shown, Amidon FT-23-43, dimensions 26.2, and height of 85.]

[Additional text or captions for the diagram if needed]

67
Appendix A. LTL Drawings

A.4 U-core

TDK-EPC U8/6/2

A.5 Toroid

Amidon FT 23-43
Appendix B

B Prime Buck-Boost Schematic

On the next page the schematic for the Prime Buck-Boost converter is shown.
Appendix B. Prime Buck-Boost Schematic
Appendix C

C Removed and Changed Components

Some components were removed or changed from prototype converter with product number INX 106 781/15 P1A before the efficiency was measured, see table.

Table 13 Removed and changed components.

<table>
<thead>
<tr>
<th>Component</th>
<th>ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removed</td>
<td></td>
</tr>
<tr>
<td>Snubbers</td>
<td>R3002, R3006, R3012, C3106, C3137, C3147</td>
</tr>
<tr>
<td>Gate A, B, C inv/ non-inv</td>
<td>R3035, R3031, R3033, R3042, R3038, R3039</td>
</tr>
<tr>
<td>Input gate signal impedance matching</td>
<td>R3027, R3028, R3029</td>
</tr>
<tr>
<td>Optional output matching NW</td>
<td>C3077, C3066</td>
</tr>
<tr>
<td>Connection to US_A thru X1021 for driver/iso ref.</td>
<td>R3023</td>
</tr>
<tr>
<td>External supply of VDD_DRV_A/B/C</td>
<td>R3019, R3020, R2021</td>
</tr>
<tr>
<td>External supply of VDD2_ISO_A and B</td>
<td>R3011, R3010</td>
</tr>
<tr>
<td>Removed 50Ohm test points</td>
<td>R3060, R3062</td>
</tr>
<tr>
<td>Removed driver supply</td>
<td>V3013, V3014</td>
</tr>
<tr>
<td>Changed</td>
<td></td>
</tr>
<tr>
<td>Input gate signal impedance matching</td>
<td>R3024, R3025, R3026 put to 0Ω</td>
</tr>
<tr>
<td>Connection to US_A thru X1021 for driver/iso ref.</td>
<td>R3022 put to 0Ω</td>
</tr>
<tr>
<td>External supply VDD_DRV_A/B/C</td>
<td>Banana jacks soldered to: C3032, C3034, C3035 (yellow, orange, pink)</td>
</tr>
<tr>
<td>External supply VDD2_ISO_A/B</td>
<td>Banana jacks soldered to: C3025, C3024 (red, purple)</td>
</tr>
<tr>
<td>Connections</td>
<td></td>
</tr>
<tr>
<td>VDD1_ISO</td>
<td>+3.3VDC</td>
</tr>
<tr>
<td>VDD2_ISO_A, B</td>
<td>+3.3VDC</td>
</tr>
<tr>
<td>VDD_DRV_A, B, C</td>
<td>+5.5VDC</td>
</tr>
<tr>
<td>V_IN</td>
<td>+14VDC</td>
</tr>
<tr>
<td>VOUT</td>
<td>5.6Ω</td>
</tr>
<tr>
<td>GATE_A_3_50OHM</td>
<td>10446A:3</td>
</tr>
<tr>
<td>GATE_B_3_50OHM</td>
<td>10446A:2</td>
</tr>
<tr>
<td>GATE_C_3_50OHM</td>
<td>10446A:1</td>
</tr>
</tbody>
</table>
Appendix C. Removed and Changed Components
Appendix D

D LTL Specifications

This chapter contains the specific data for each LTL.

D.1 LTL₀

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Ericsson Nr/Man. Designation</th>
<th>Function Designation</th>
<th>Pcs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L₁-L₄₀</td>
<td>Coilcraft SLC7530S-101MLC</td>
<td>100nH 20% 0.123mΩ</td>
<td>40</td>
</tr>
<tr>
<td>C₁-C₄₀</td>
<td>Murata GRM1555C1H561J</td>
<td>560pF 5% 0402 50V C0G</td>
<td>40</td>
</tr>
<tr>
<td>1</td>
<td>TVK 128 1591 R1A</td>
<td>PCB</td>
<td>1</td>
</tr>
</tbody>
</table>

D.2 LTL₁, INX 106 781/16 P1A

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Ericsson Nr/Man. Designation</th>
<th>Function Designation</th>
<th>Pcs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L₁-L₄₀</td>
<td>TDK-EPC U8/6/2</td>
<td>Ferrite U-core</td>
<td>40</td>
</tr>
<tr>
<td>Plate</td>
<td>TDK-EPC QU40/40/2</td>
<td>Ferrite Plate</td>
<td>1</td>
</tr>
<tr>
<td>C₁-C₄₀</td>
<td>RJC 463 3523/56</td>
<td>560pF 5% 0402 50V C0G</td>
<td>40</td>
</tr>
<tr>
<td>1</td>
<td>TVK 128 1891 R1A</td>
<td>PCB</td>
<td>1</td>
</tr>
<tr>
<td>Film</td>
<td>PSG, Polymex A 0.001”</td>
<td>Polyester Film Purple</td>
<td>1</td>
</tr>
<tr>
<td>Mech. Plate</td>
<td>-</td>
<td>Acrylic 85 x 85 mm</td>
<td>2</td>
</tr>
<tr>
<td>Screw</td>
<td>-</td>
<td>M6</td>
<td>4</td>
</tr>
<tr>
<td>Nut</td>
<td>-</td>
<td>M6</td>
<td>4</td>
</tr>
</tbody>
</table>

D.3 LTL₂, INX 106 781/16 P1A

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Ericsson Nr/Man. Designation</th>
<th>Function Designation</th>
<th>Pcs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L₁-L₄₀</td>
<td>TDK-EPC U8/6/2</td>
<td>Ferrite U-core</td>
<td>40</td>
</tr>
<tr>
<td>Plate</td>
<td>TDK-EPC QU40/40/2</td>
<td>Ferrite Plate</td>
<td>1</td>
</tr>
<tr>
<td>C₁-C₄₀</td>
<td>RJC 463 3523/56</td>
<td>560pF 5% 0402 50V C0G</td>
<td>40</td>
</tr>
<tr>
<td>1</td>
<td>TVK 128 1892 R1A</td>
<td>PCB</td>
<td>1</td>
</tr>
<tr>
<td>Film</td>
<td>PSG, Polymex A 0.001”</td>
<td>Polyester Film Purple</td>
<td>1</td>
</tr>
<tr>
<td>Mech. Plate</td>
<td>-</td>
<td>Acrylic 85 x 85 mm</td>
<td>2</td>
</tr>
<tr>
<td>Screw</td>
<td>-</td>
<td>M6</td>
<td>4</td>
</tr>
<tr>
<td>Nut</td>
<td>-</td>
<td>M6</td>
<td>4</td>
</tr>
</tbody>
</table>
### D.4 LTL₃, INX 106 781/16 P1A

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Ericsson Nr/Man. Designation</th>
<th>Function Designation</th>
<th>Pcs</th>
</tr>
</thead>
<tbody>
<tr>
<td>L₁-L₄₀</td>
<td>FT</td>
<td>Ferrite toroid</td>
<td>40</td>
</tr>
<tr>
<td>C₁-C₄₀</td>
<td>RJC 463 3523/56</td>
<td>560pF 5% 0402 50V C0G</td>
<td>40</td>
</tr>
<tr>
<td>𝑖</td>
<td>TVK 128 1892 R1A</td>
<td>PCB</td>
<td>1</td>
</tr>
</tbody>
</table>
Appendix E

E Time Space Diagram for Double $S_C$ Switching

On the next page the time space diagram for double $S_C$ switching is shown.
Fig. 53 Time space diagram for double $S_C$ switching.