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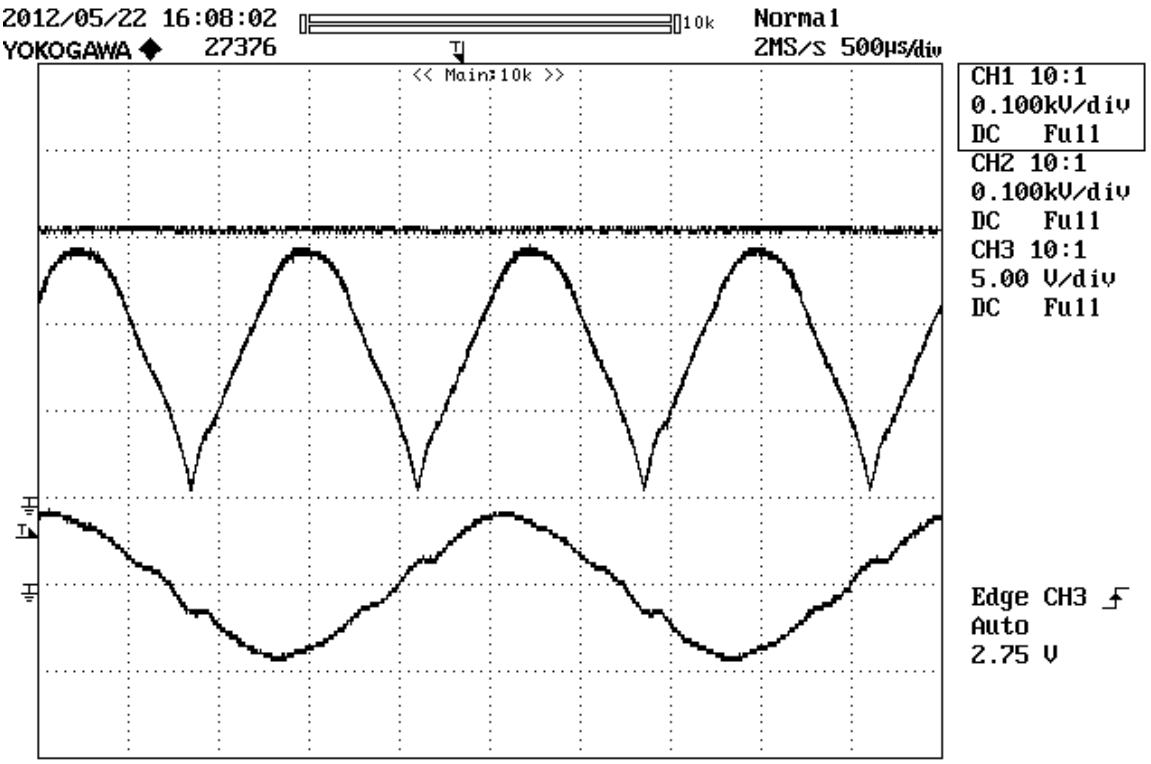

Active Power Factor Correction for Airborne Applications

Master of Science Thesis

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Abstract

This thesis deals with the topic active single phase power factor correction circuits to be used in airborne applications. Specifically, the boost-type power factor correction topology was investigated with a three-phase modular approach in mind. The boost-type power factor correction topology was simulated using Matlab/Simulink with a simplified dynamic model of the current stage. A digitally controlled prototype boost PFC test system was designed (partly using existing hardware designed for 50 Hz), set up and evaluated for 50 and 400 Hz line voltage. The evaluation was performed for the input voltage levels 115 and 200 Volts. Results at 50 Hz and power levels of 300-500W showed a Total Harmonic Distortion (THD) of 4-8% and a Power Factor (PF) of >0.99 for this set-up. Similar tests were performed at 400 Hz and a THD of 7% and PF of 0.95 were observed with an input filter originally designed for a 50 Hz system, a PF of 0.998 was observed without the filter.

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List of figures

List of Acronyms

ACMC - Average Current Mode Control
ADC - Analog to Digital Converter
CCM – Continuous Conduction Mode
DCM – Discontinuous Conduction Mode
DPFC - Digital Power Factor Correction
DSP - Digital Signal Processor
EMI – Electromagnetic Interference
EMC – Electromagnetic Compability
ePWM - enhanced Pulse Width Modulation
ESR - Equivalent Series Resistance
FFT – Fast Fourier Transform
PF - Power Factor
PFC - Power Factor Correction
PI - Proportional Integral
PWM - Pulse Width Modulation
RMS - Root Mean Square
HW - Hardware
IC - Integrated Circuit
ISR – Interrupt Service Register
THD – Total Harmonic Distortion
S/H - Sample & Hold
SMPS - Switch Mode Power Supply
SoC – Start of Conversion

List of symbols

d – duty cycle
i_L (t) - inductor current
i_D (t) – diode current
i_{cap}(t) – capacitor current
I_{out} – constant output current
v_{in} (t) – input voltage
$|v_{in}(t)|$ - rectified input voltage
V_{rect} – rectified voltage
V_{out} – output voltage
V_{dc} – output dc-voltage
V_{dchi} – output dc-voltage high
V_{dclo} – output dc-voltage low
$v_{dc,ripple}$(t) – output voltage ripple
$v_{control}$ – Control voltage, output of voltage controller

v_i – input voltage RMS in Ridleys model
ii – input current RMS in Ridleys model
v_o – dc output voltage in Ridleys model
i_o – average output current over one cycle in Ridleys model
v_c – control voltage in Ridleys model
r_o – small signal resistor in Ridleys model

K_{vp} –proportional gain of the voltage controller
K_{vi} – integral gain of the voltage controller
K_{ip} – proportional gain of the current controller
K_{ii} – integral gain of the current controller

ω_{zv} – voltage controller zero
ω_{cv} – cut-off frequency of voltage loop
ω_{zi} – current controller zero
ω_{ci} – cut-off frequency of current loop

T_{sw} – switching period
T_{ts} – Time step of simulation
f_{sw} – switching frequency
f_{line} – line frequency

Contents

1. Introduction

1.1. Background

There are inherent mechanisms in diode rectification systems which cause these systems to produce severe distortion of the input current and, consequently, a poor power factor (PF). These problems arise because the rectifier diodes are backward biased for a large amount of the line voltage period. This leads to the fact that the current is only drawn when the instantaneous input voltage surpasses that of the output capacitor. Thus, the current will be a "pulse" which is centered around the peak value of the input voltage, this current pulse will act to charge the capacitors. Moreover, the output voltage is directly proportional to the input peak voltage and as such disturbances in the input voltage will be reflected in the output voltage.

Problems with diode rectification may be alleviated by using an active Power Factor Correction (PFC) circuit after the diode rectification bridge - typically a boost converter is used. There is also a possibility to introduce the PFC directly into the rectification bridge. This circuit is controlled so that the inductor current follows a sinusoidal reference to produce an input current which is in phase with the input voltage; thus, emulating the subsequent circuitry as a resistor to the power source. Another great benefit of this set-up is that the output voltage of the rectifier is being controlled independently of line voltage. Previously, PFC-circuits have been incorporated in Switch Mode Power Supplies (SMPS) - e.g. computer power supplies - and these are operated at public grid frequency of 50/60 Hz. These systems have been implemented with varying sophistication depending on cost and application. Cheap consumer electronics may have better displacement power factor but with a relatively high distortion of input current; however, some sensitive electronics may be more sophisticated to reduce harmonics to a very low level (THD < 5%). Research has been done on these kinds of PFC-circuits, and a lot of the applications are designed for 50-60Hz, relatively low power (<1kW) and they are mainly controlled by analog Integrated Circuits (IC). There are standards regulating equipment connected to the grid; for example, IEC61000-3-2 for Europe and IEC555-2/Energy Star Program for USA. According to Nilsson[1] the driving force of these regulations are that the power companies strive to reduce the amount of reactive power into consumer appliances since this is not paid for by the consumers, whom only pay for active power consumed.

The AC/DC power supplies of aircrafts may be fed with a voltage of variable frequency (360-800Hz), commonly called "wild frequency", which is the cause of the generator being coupled directly to the engine. There are restrictions regarding harmonics in airborne systems. Therefore it is of great importance to control these to make sure they stay well in range of what might be allowed. This is to make sure sensitive equipment is not affected by the current-harmonics. According to Nilsson the AC/DC power supplies of modern airborne applications functions with a multi-phase transformer which outputs 21 phases from 3 phases

[1] Valter Nilsson, SAAB EDS, Gothenburg, 2012

to a 42-pulse rectifier. These systems produce very low THD and work very well. However, active Power Factor Correction in a three-phase setting is believed, apart from the obvious reason to reduce THD and PF, to be able to reduce size and weight of the AC/DC converter since no bulky passive components are used in these kinds of systems.

1.2. Standards

When designing equipment for different applications and areas of use, it is of great importance that the design process is performed with the relevant standards in mind; this is to make sure that equipment follows the requirements and to make sure it follows the rules and regulations set in place by, for example, governments, institutes and departments. The range of these standards might cover ground and airborne applications. As for airborne applications it is of great importance that systems does not interfere or disturb other components and systems that may cause equipment to stop working properly. Considered in this work are harmonics in the current, frequency limits and voltage regulation requirements, as well as input voltage stability to the power unit.

The standards regulating current harmonics, and other factors, for airborne equipment are MIL-STD-704F and RTCA DO-160F[2] amongst others. These standards cover everything from environmental standards to equipment standards regulating different levels of harmonics as mentioned etc. Regarding the current harmonics there are levels for the amount of ripple and harmonics that are allowed. The values are calculated from the maximum fundamental current in the equipment. The values are also based on a set number of harmonics that will be evaluated and computed to calculate the total harmonic distortion. In tables 1 and 2 below there are examples of what magnitude the harmonics are allowed to be, which comes from the RTCA DO-160F standard.

Table 1 Harmonics limits for single phase equipment

Harmonic	Limits
Odd Non Triplen (h=5,7,11,13,...,37)	$I_h=0,3*I_1/h$
Odd Triplen (h=3,9,15,21,...,39)	$I_h=0,15*I_1/h$
Even, 2 and 4	$I_h=0,01*I_1/h$
Even > 4 (h=6,8,10,...,40)	$I_h=0,0025*I_1/h$

Table 2 Harmonics levels for three-phase systems

Harmonic	Limits
3rd, 5th, 7th	$I_3=I_5=I_7=0,02*I_1/h$
Odd triplen (h=9,15,21,...,39)	$I_h=0,1*I_1/h$
11th	$I_{11}=0,1*I_1$
15th	$I_{15}=0,08*I_1$
Odd Triplen 17,19	$I_{17}=I_{19}=0,04*I_1$
Odd Triplen 23,25	$I_{23}=I_{25}=0,03*I_1$
Odd Triplen 29,31,35,37	$I_h=0,3*I_1/h$
Even, 2 and 4	$I_h=0,01*I_1/h$
Even > 4 (h=6,8,10,...,40)	$I_h=0,0025*I_1/h$

[2] These standards where available at the company, but they may also be available online either for free or for a certain fee.

The allowed levels of Total Harmonic Distortion is set to be under <5%for the RTCA DO-160F standard.

As mentioned there are also regulations for the input voltage stability into the power unit. These standards regulate how much the voltage may differ and what requirements there are regarding times for recovery at transients etc. Figure 1 shows an "Envelope of Normal AC Voltage Transient", inspired from the standards document, which illustrates what requirements there are regarding these transients. This envelope is valid during nominal operation, 115V 400Hz and variable frequency (360-800Hz).

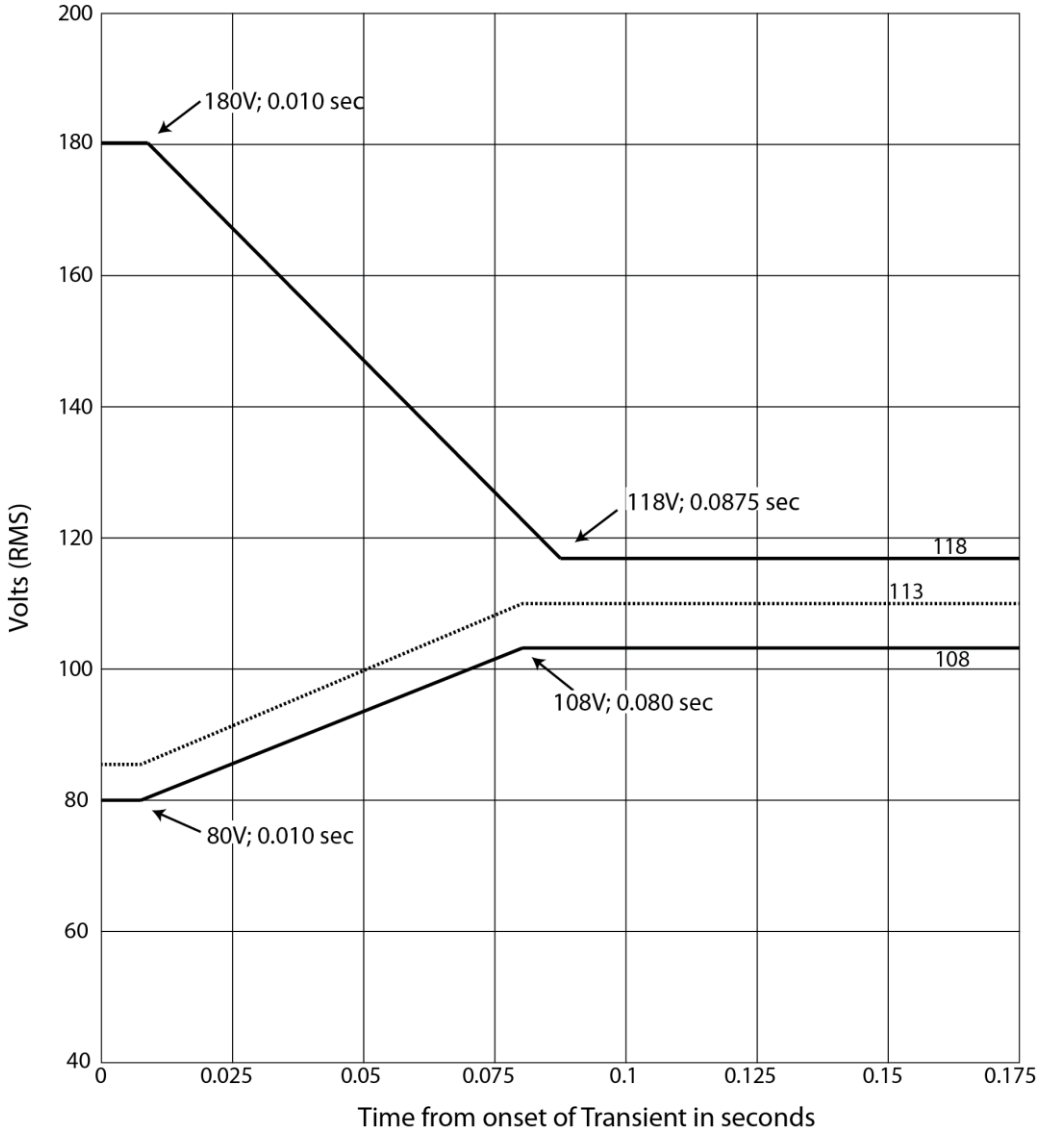

Figure 1 Operating conditions for supplying voltage

Equipment is not only required to work continuously inside given specifications, it also has to work under "abnormal conditions". The standards for these conditions states what the equipment has to withstand without breaking and what is required to bring it back to normal conditions. This is very important to make sure the equipment will not fail if something

unexpected happens plus make sure abnormal conditions does not make the equipment disturb or damage other equipment and components.

1.3. Design Specifications and Goals

There are some design specifications that has to be taken into account to be able to design the device in a way suitable for the application. These specifications involve what input power levels are desired, efficiency and PF etc. These specifications are also closely connected to the given standards mentioned earlier, such as levels at which the equipment will work at and so on.

The rectification system may be fed with a three phase voltage 115/200 V; 360-800 Hz or 400 Hz coming directly from the generator of the aircraft.

Subsequent electronics – supplied from the rectifier system - are operating at a DC bus, e.g 56 V Dc input voltage and the voltage ripple is desired to be limited to 0.7 V_{p-p}.

Design criteria for these kinds of systems involve working towards a Total Harmonic Distortion (THD) of less than 5% and a Power Factor of above 0.99. The overall efficiency of these kinds of systems is generally desired to be above 90%

The weight and size that is preferred a 3kW 3-phase application are set to be <5kg and <5 liters in volume. This is to be able to fit it into the given applications for this kind of power unit.

1.4. Purpose

The purpose of this thesis is to investigate the concept of active power factor correction for airborne applications. This includes modeling and simulation of a single phase module; propose a feasible design of a digitally controlled single phase solution and evaluate this; and a theoretical overview of feasible three-phase solutions using a modular approach. A choice was to be made during the project if the focus should lie on the digital control of the hardware or on the hardware itself. Digital control of the hardware was chosen. Also, determination of the THD for this circuit is of great interest and this will also be evaluated.

1.5. Scope

Due to the increased complexity associated with constructing and evaluating three phase circuits, this is omitted in favor of proposing and evaluating a scalable single phase solution, with a three-phase modular approach in mind.

For the demonstration of the hardware the availability of functioning hardware, such as evaluation kits, decide the outcome.

Another consideration is that practical information about digital control schemes for 400-800Hz is very limited so control algorithms designed for 50Hz will be reworked for the above frequency range, then simulated and implemented. Advanced modeling of the system and associated control algorithms are beyond the scope of this thesis.

Evaluation of the system will primarily be directed at 50Hz operation. If the outcome of these tests is successful, a 400Hz scenario might be tested also. However simulations may cover 50, 400 and 800Hz.

1.6. **Thesis outline**

This thesis has been divided into six different chapters, including Chapter 1, *Introduction*. In Chapter 2, *Technical Background,* the relevant technical background is covered and known technologies in the field are presented. Chapter 3, *Modeling and Simulation of Single Phase Boost Power Factor Correction Module,* a simplified dynamic model using Simulink is set-up to simulate a digital controller and the current shaping properties at 50Hz, 400 Hz and 800 Hz. In Chapter 4, *Design and Evaluation of Single Phase Module Prototype,* a prototype system is proposed and evaluated. In Chapter 5, *Conclusion,* the results and experiences are discussed from previous sections. Lastly, in Chapter 6, *Future Work,* ideas for future work and improvements from this thesis is discussed.

2. Technical background

Diode rectifier systems suffer from inherent mechanisms causing them to draw a distorted input current, containing current harmonics of varying amplitude. This may be alleviated by using power factor correction techniques, either by using controlled power electronics in single-phase or multi-phase (e.g three-phase) topologies or passive solutions. The difference between diode rectification and PFC may be viewed in Figure 2.

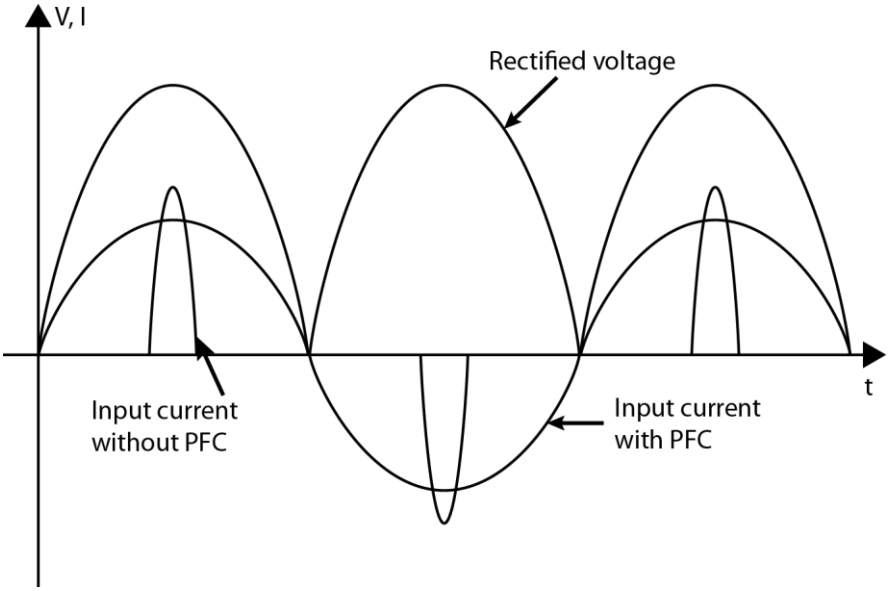

Figure 2 The ideal difference in current with and without Power Factor Correction of the diode rectifier

The aim of performing power factor correction is to align input current and voltage waveforms in an AC-system, and also reduce the amount of harmonics in the system. Since power factor is defined as (Undeland, Mohan & Robbins 2003)

$$PF = \frac{I_{s1}}{I_s}\cos(\varphi) = \frac{1}{\sqrt{1+THD^2}}\cos(\varphi) \tag{2.1}$$

where cos(φ) represents the displacement of voltage and current, I_{s1} is the RMS (Root Mean Square)-value of the fundamental current and I_s is the total current of the input. It is desired to decrease the angle between voltage and current so that cos(φ) approaches unity. In ordinary undistorted systems, the power factor is 1 if only the voltage and current waveforms are aligned without any phase shift; however, in systems containing harmonics this is not the case and the distortion of the input current leads to a decrease of the power factor. Also, the power factor also affects the complex power (S) drawn by the system as

$$PF = \cos(\varphi) = \frac{P}{S} = \frac{P}{\sqrt{P^2+Q^2}} \tag{2.2}$$

where P and Q is the active and reactive power respectively.

Another important matter involving power factor correction is to decrease the Total Harmonic Distortion (THD) of the system. THD is defined as (Undeland, Mohan & Robbins 2003)

$$\%THD_i = 100\frac{I_{dis}}{I_{s1}} = 100\frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} \tag{2.3}$$

where I_{dis} is the RMS-values of the harmonics, I_{s1} is the RMS-value of the fundamental frequency of the input current and I_s is the total RMS-value of the input current. The above quantity, as described in chapter 1.2, is typically under regulation for equipment to be connected to the mains of the power grid or to airplane generators.

2.1. Single Phase Power Factor Correction Topologies

While not technically being a "topology" there is still a way of improving the power factor of the diode bridge rectifier using passive components on the input, namely inductors and capacitors. The addition of a inductor on the ac-side helps to increase the power factor by making the current waveform better; however, the resulting power factor is not perfect (Undeland, Mohan & Robbins 2003). By only providing passive PF-correction the output voltage remains uncontrolled and dependent on the input voltage. To make the output voltage controllable there are some different topologies that can be used depending on the need of either increasing or lowering the output voltage.

The buck-converter topology in Figure 3 works in a way that it decreases the output voltage compared to the input voltage. Due to the criteria of having an input voltage greater than the output voltage to work properly this makes the buck-topology a bad choice for a pre-regulator because of the inability to work in the skirts of the half input sine wave having V_{in} less than V_{out}. On the other hand having a buck converter connected after for example a boost pre-regulator makes it a great choice for lowering the "constant" DC voltage or providing a current limiting feature.

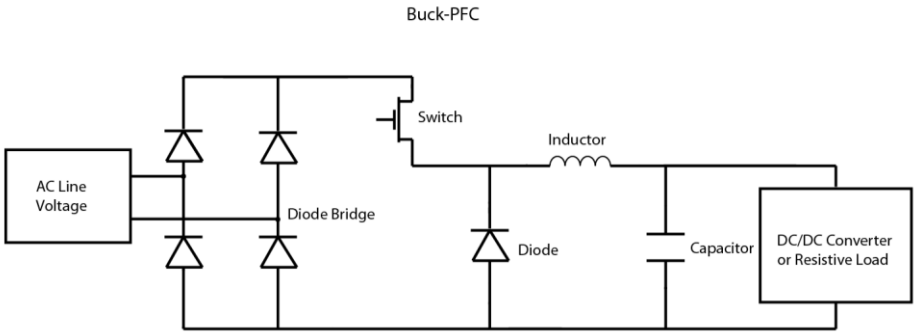

Figure 3 Buck PFC topology

Compared to the buck-converter, the boost converter in Figure 4 boosts the output voltage compared to the input voltage. The Boost-PFC topology is the most used and preferred topology in PFC-circuits (Dixon 2003) and one of the reasons to this is the ability to control the input current. Criteria's for making a boost-converter work in a convenient way is that the output voltage is higher than the input voltage. If the circuit is constructed in such a way that the output voltage exceeds the maximum peak of the input voltage it will be able to work in the full range from zero to max peak value. Due to the ability to work at high power levels and the possibility to use current mode control to program the input current half sine wave it

makes the boost topology a popular choice. If the converter works in Continuous Conduction Mode(CCM) the inductor- and input current will always be continuous, helping to reduce input current harmonics. If there is a need to have lower voltage levels it is often popular to have a buck converter connected in series with the boost to make this transformation instead of having a buck right from the start. One drawback with the boost topology is that it does not have a switch in series between the input and output, therefore it is unable to limit the input current. This means overload and/or startup currents cannot be controlled. Also, if the input voltage surpasses that of the output voltage the converter is unable to control the current as the diode will be forward biased and the current will flow continuously.

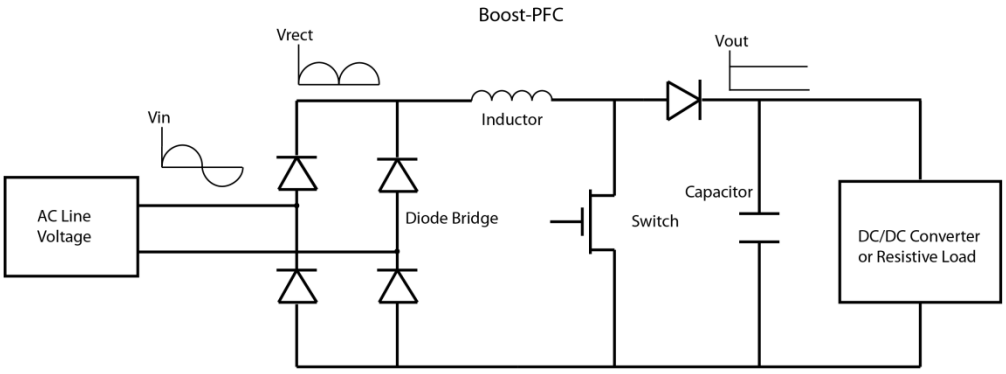

Figure 4 Boost PFC circuit

When it comes to the feature to both be able to have the possibility to create a higher and a lower output voltage compared to the input voltage there are some different converters that can be used. This can come in handy when there is a special need for the circuit to be able to do both conversions without using two different converters connected in series. Two common converters are the Buck/Boost-converter and the Flyback-converter. The mentioned features make these topologies viable choices compared to only a Buck or Boost. The basic concept of the two is the same but they are constructed in two different ways that will be described further down. Examples of simple schematics that are most common for the converters are shown in figures 5 and 6 below.

Several different approaches are possible when constructing Buck/Boost and Flyback-converters. In the Buck/Boost case there are versions where two switches are used instead of the conventional single-switch topology, there are also some topologies involving magnetic isolation i.e. there is a galvanic isolation between the input and output sides. Also, Flyback-converters have the advantage of having low cost and galvanic isolation of the voltage. (Feng, Tsai & Tzou, 2001) It is also able to both regulate the output voltage both up and down as mentioned making it a competitively choice when choosing converter topologies for power electronics. Working under optimal conditions Flyback-converters have high efficiency, and that is in power levels <500W. For applications using higher power levels it is required to parallel devices. To achieve this there is also a need to have control algorithms able to perform these tasks, to do this a DSP is optimal to drive the circuit.

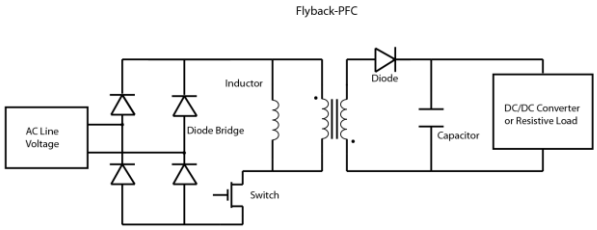

Figure 5 Flyback PFC converter

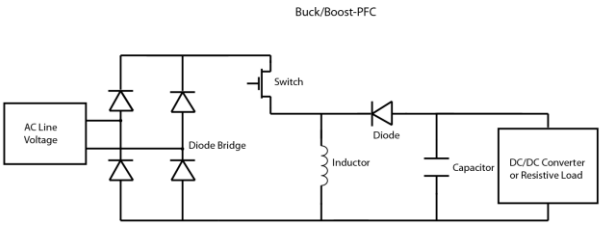

Figure 6 Buck/Boost PFC

The Buck-, Buck/Boost- and Flyback-topologies have discontinuous input current due to the fact that there are switches in series with the line for these topologies. However, the input current of Boost-topology can have an input current in both CCM and DCM. The ability to operate in CCM makes the Boost-topology the most viable option of the mentioned topologies for high performance power factor correction circuits.

2.2. The Boost Power Factor correction Topology

As discussed in the previous section, the boost PFC-topology has the ability to control the input current in continuous conduction mode which makes it a suitable candidate to be explored for a single phase power factor correction topology for airborne applications.

2.2.1. Theory of the boost-type PFC topology

This is a very common single-phase PFC topology (Undeland, Mohan & Robbins 2003) which utilize a diode rectifier with a complementary step-up power converter (boost) before the output capacitor, figure 7. The step-up converter is set in place to control two things, the shape of the input current and the magnitude of the output voltage. For this to work there are two conditions which must be met: the output voltage is higher than the peak of the rectified input voltage, and the power flow is unidirectional.

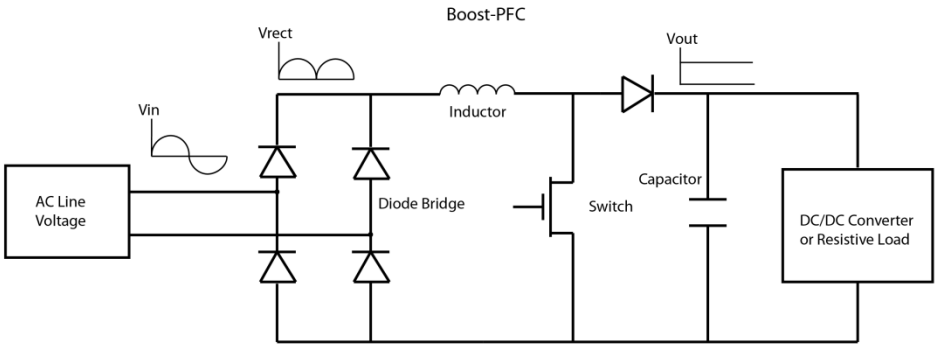

Figure 7 The boost PFC single phase module

The current paths for different time instants may be viewed in figures 8 and 9 for the boost PFC converter. While the switch is conducting, the current will flow through the inductor and, through the switch and back to the mains. This is because the diode is blocking thus disconnection the output. The load current will be supplied from the capacitor, depleting it and decreasing the voltage. However, when the switch is blocking, the inductor will force the

current to flow through the diode into the capacitor and load, which will recharge the capacitor bank and thereby increasing the voltage.

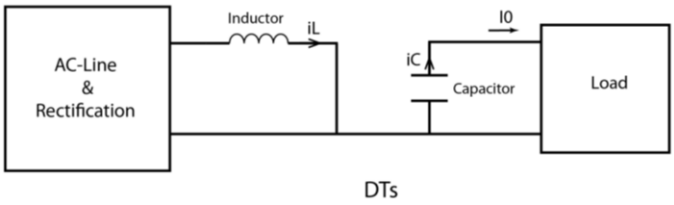

Figure 8 Current path during turn on of transistor

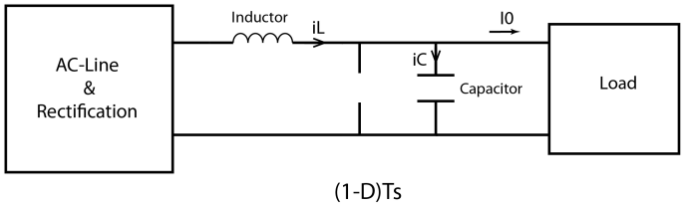

Figure 9 Current path during turn off of the transistor

The idea is to control the variable duty cycle of the switch in the step-up converter to shape the input current. When the switch is conducting the voltage over the inductor causes the current to increase, according to the following equation for the ideal boost-converter

$$\frac{di}{dt} = \frac{|v_{in}(t)|}{L} \tag{2.4}$$

where $|v_{in}(t)|$ is the rectified input voltage, L is the inductance of the current shaping inductor and di/dt is the current derivative. However, when the switch is blocking the current will decrease, according to

$$\frac{di}{dt} = \frac{|v_{in}(t)| - V_{dc}}{L} \tag{2.5}$$

since V_{dc} is assumed to be higher than $|v_{in}(t)|$. The switching of the transistor is performed at a switching frequency far greater than that of the input line voltage. Subsequently, the converter may be operated in either Continuous Conduction Mode (CCM), figure 10.a, or Discontinuous Conduction Mode (DCM), figure 10.b. The appearance of the input current will have a "saw tooth" ripple; however, it will be a significant improvement compared to the ordinary bridge rectifier. The THD of the CCM waveform is significantly better than that of the DCM waveform since it closely emulates a sine-wave. The methods of application vary as DCM may be used in applications under less strict regulations than those where CCM is needed. CCM is usually employed when there is a need to decrease the THD to very low levels.

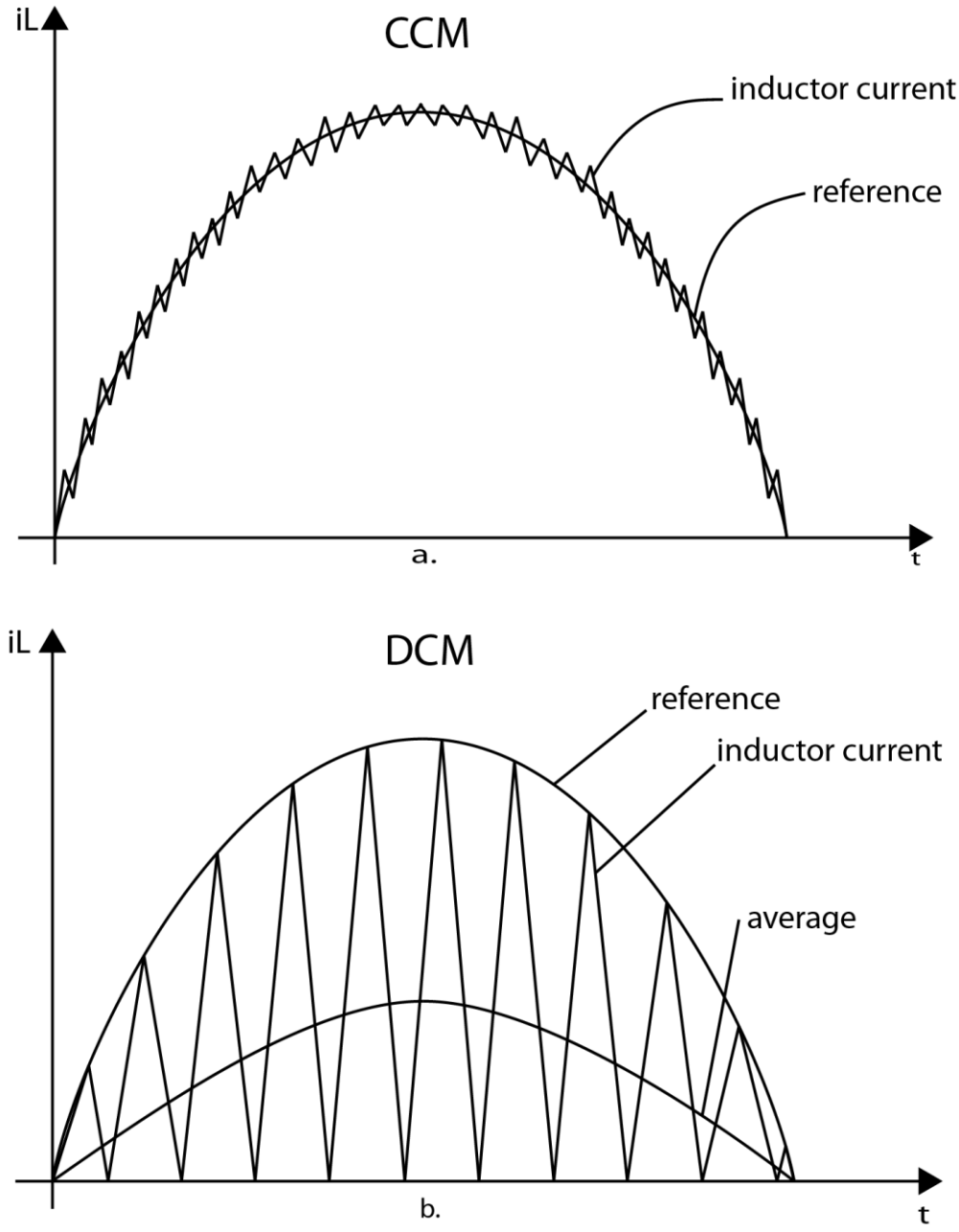

Figure 10 Operation modes of the boost PFC

The output voltage is dependent on the stored energy/charge in the output capacitor bank. For the boost-converter, in figure 7, the output voltage can be described by the general differential equation for the output voltage

$$v_{dc} = v_{cap} = v_{cap}(t_1) + \frac{1}{C}\int_{t1}^{t} i_{cap}dt \tag{2.6}$$

where C is the value of the output capacitor bank. The capacitor current, i_{cap}, from the above equation which may be described as

$$i_{cap} = i_D - I_0 \tag{2.7}$$

where I_0 is the output current and i_D is the current from the inductor flowing through the diode during the off-time of the switch. The equations above show that during the time that the switch is on, the load draws a current which discharges the capacitor bank; however, the bank is then charged again during the off-time of the switch.

2.2.1. Ripple components of the boost type power factor correction topology

There are ways of determining the inductor current and output voltage ripple of the converter (Undeland, Mohan & Robbins 2003) and these equations provide deeper understanding on the operation of this PFC-topology. Hereafter, the switching period will be assumed constant; thus, operating in what is called "constant frequency mode". Starting with the current ripple there are some assumptions to be made: during one switching cycle the output voltage V_{dc} and input rectified voltage $|v_{in}|$ will be assumed constant. The peak-to-peak ripple can then be described as the derivative during one switching cycle; thus, during the on time

$$t_{on} = \frac{LI_{rip}}{|v_{in}|} \tag{2.8}$$

and when the switch has turned off

$$t_{off} = \frac{LI_{rip}}{V_{dc} - |v_{in}|} \tag{2.9}$$

Since the converter is assumed to be in continuous conduction mode then the switching frequency can be described as

$$f_s = \frac{1}{t_{on} + t_{off}} \tag{2.10}$$

Thus, by using the three above equations the following can be derived

$$I_{rip} = \frac{(V_{dc} - |v_{in}|)|v_{in}|}{f_s L V_{dc}} \tag{2.11}$$

and this function has a maximum

$$I_{rip,max} = \frac{V_{dc}}{4 f_s L} \tag{2.12}$$

which occurs when $|v_{in}|=V_{dc}/2$. It can be noted that the ripple of the output current can be actively controlled during the design process by changing switching frequency and inductor value.

The ripple of the output voltage may also be derived and this is done by looking at the power balance equations. The input and output power is assumed constant each instant. The input power can be described as

$$p_{in}(t) = V_{in,peak}|sin\omega t| I_{in,peak}|sin\omega t| = V_{in}I_{in} - V_{in}I_{in}cos2\omega t \tag{2.13}$$

The output power can be described as

$$p_{out}(t) = V_{dc} i_d(t) \tag{2.14}$$

where V_{dc} is assumed to be constant due to the presence of a sufficiently large output capacitor bank. The diode current may be described as

$$i_d(t) = I_{out} + i_c(t) = \frac{V_{in} I_{in}}{V_{dc}} - \frac{V_{in} I_{in}}{V_{dc}} \cos(2\omega t) \tag{2.15}$$

and the average value of i_d is

$$I_d = I_{out} = \frac{V_{in} I_{in}}{V_{dc}} \tag{2.16}$$

Thus, the current to the capacitor is

$$i_c(t) = -\frac{V_{in} I_{in}}{V_{dc}} \cos(2\omega t) = -I_d \cos(2\omega t) \tag{2.17}$$

and by applying integration and dividing with the capacitor value, the output voltage ripple may be found

$$v_{dc,ripple} \approx -\frac{I_d}{2\omega C} sin2\omega t \tag{2.18}$$

where ω is the angular frequency of the line voltage and C is the output capacitor. To be noted is that the ripple is of double line frequency and the ripple magnitude may be reduced by increasing the output capacitor.

2.2.2. Small-signal model of the Boost type PFC AC/DC converter

There is a benefit associated with developing a small signal model of the boost converter as this may be used in control purposes of the output voltage. Ridley (1989) proposes an averaged model of the boost power factor correction circuit over one half period. The model is based on some assumptions; first, the voltage is assumed constant during one switching cycle. This assumption is valid due to that the switching frequency is far greater than that of the rectified sine-wave of the input voltage and as such the change in voltage over that period of time is negligible. The second assumption is that the current tracks the "scaled input voltage". The basis of this analysis comes from the power balance equations

$$v_i i_i = v_o i_o \tag{2.19}$$

where v_i and i_i are the RMS-values of the input voltage and current respectively; v_o is the DC voltage on the output and i_o is the average output current. Further, for "line-referenced" control, meaning that the input current tracks the scaled rectified voltage, the input current may be written as

$$i_i = \frac{v_i v_c}{k} \tag{2.20}$$

where k is a scaling factor of the rectified voltage. The above is called "current control law" by Ridley (1989). A "steady state conversion ratio" is introduced

$$M = \frac{V_0}{V_i} = \sqrt{\frac{V_c r_0}{k}} \tag{2.21}$$

where r_0 is denoted as a "small signal resistance" according to the following

$$r_0 = \frac{V_0}{I_0} \tag{2.22}$$

With these basic definitions it is possible to introduce perturbations around the stable DC-operating point of (2.19) with the addition of (2.20). Products of small signal variations and DC-terms are neglected which yields

$$\widehat{\imath_o} = \frac{2M}{r_0}\hat{v}_i + \frac{{V_i}^2}{kV_0}\hat{v}_c - \frac{1}{r_0}\hat{v}_0 \tag{2.23}$$

for the output current, and using the same method on the current control law (2.20) a small-signal model of the input current may be found to be

$$\hat{\imath}_i = \frac{V_i}{k}\widehat{v_c} + \frac{M^2}{r_0}\widehat{v_i} \tag{2.24}$$

With these equations Ridley (1989) creates an equivalent small signal circuit and from this the following is derived

$$\frac{\widehat{v_o}}{\widehat{v_c}} = g_c \frac{r_0 // Z_L}{1 + sCr_0 // Z_L} \tag{2.25}$$

where Z_L is the output impedance and C is the output capacitor. This output impedance may be modeled in two different ways, depending on what the converter is connected to. Ridley (1989) claims that for a resistive load the small-signal resistance is equal to the load resistance. The other case is when the PFC is connected to a subsequent converter; in this case it is called a "constant power load", where the input impedance of the converter is

$$R_i = r_0 = -\frac{V_0}{I_0} \tag{2.26}$$

which is also the same as the output impedance of the PFC-stage. Under these assumptions models of the PFC-stage may be built for both load-scenarios. For the resistive load, the control-to-output function becomes

$$\frac{\widehat{v_o}}{\widehat{v_c}} = g_c \frac{R_L}{2 + sCR_L} \tag{2.27}$$

where R_L is the load resistance. For the constant power load the transfer function becomes

$$\frac{\widehat{v_o}}{\widehat{v_c}} = g_c \frac{1}{sC} \tag{2.28}$$

For the two equations above the constant g_c is defined as

$$g_c = \frac{V_i}{kM} \tag{2.29}$$

There is also a possibility to perform an averaged state space analysis of the current stage as well, which is needed to extract the transfer function of duty cycle to inductor current. To start off, the derivative of the inductor current will be used, which yields

$$\frac{di_L}{dt} = \frac{v_{in}}{L} d + \frac{(v_{in} - v_{dc})(1 - d)}{L} \tag{2.30}$$

where V_{in} is the rectified input voltage, V_{dc} is the output voltage and L is the current shaping inductor of the circuit. If the voltages are assumed constant during one switching period and by applying the Laplace operator this leads to

$$i_L = \frac{(v_{in} - v_{dc} + v_{dc} d)}{sL} \tag{2.31}$$

and by introducing perturbations around the operating point of i_L and d and assuming V_{in} and V_{dc} being fairly constant – the following can be derived

$$\frac{\widetilde{i_L}}{\tilde{d}} = \frac{V_{dc}}{sL} \tag{2.32}$$

which is a result usually adopted for the compensation process by, for example, Choudhury (2005) and Skanda (2007). These small signal models are important for the compensator design process.

2.3. **Current mode control**

In ordinary power supplies a current mode strategy may be applied. And as such there are two loops in the control system. There is an outer voltage control loop, this loop provides a reference for the current controller. This system then controls the average inductor current to the output stage in such a way that it will maintain the output voltage. This can be beneficial since both voltage and current is controlled. This makes paralleling of devices more simple.

The main difference for current mode control for switching power supplies and PFC-circuits lies in the fact that, over time, the current reference for the SMPS will be more or less constant while the current reference for the PFC will vary over time and be proportional to the rectified voltage, taking on the shape of a sinusoidal. However, for switching purposes the

current reference will be more or less constant over one switching period because of the significant difference in line and switching frequencies.

The generic control block for a PFC-circuit can be viewed in Figure 11. It can be seen that the input voltage is controlled by a Proportional Integral (PI)-controller. The output of the voltage controller, $V_{control}$, is then used to provide the peak-value of the rectified *sin*-current reference for the inductor current. The rectified voltage, V_{rect}, is used to provide the "shape" of the input current as it is desired to have the rectified voltage and inductor current in phase with one another. The measured inductor current, and the previously mentioned reference, are then fed into a current mode-control block. The dashed arrow is the voltage feed forward which may be used to feed forward the input voltage. This is used for correction in input current reference when the input voltage is decreased, meaning that the input power remains constant (Choudhury, 2005)

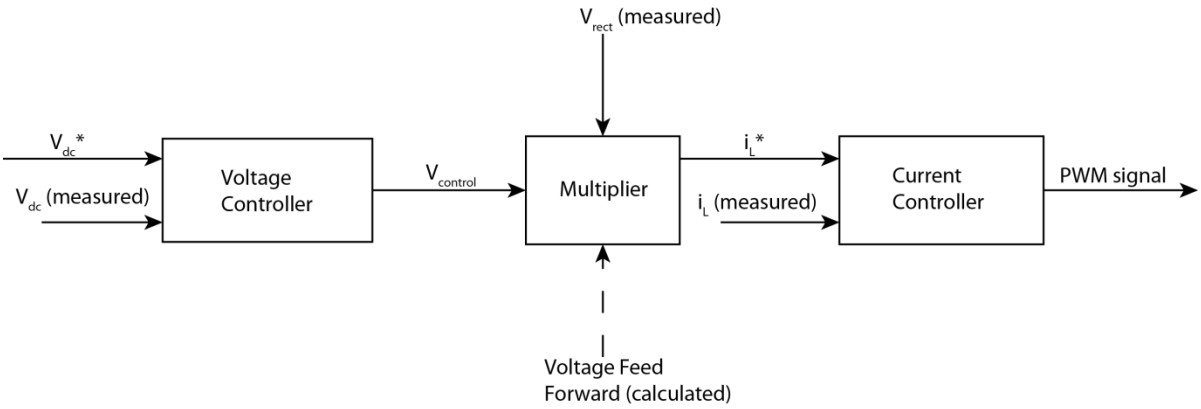

Figure 11 Control block of the boost PFC

Generally, the current may be controlled in various ways. "Tolerance Band Control" (Undeland, Mohan & Robbins 2003) is used in such a way that it attempts to control the average inductor current. The output of the voltage PI-controller sets a reference for the average inductor current. Then, there is a design parameter of the inductor current ripple di_L. With this information available a controller scheme can be constructed in such a way that the switch is on until the inductor current reaches

$$i_L = I_{L,avg} + \frac{\Delta i_L}{2} \tag{2.33}$$

where $I_{L,avg}$ is the average current out from the voltage control system and, consequently, Δi_L is the previously mentioned design parameter. When the limit has been reached in (2.33) the switch will turn off until

$$i_L = I_{L,avg} - \frac{\Delta i_L}{2} \tag{2.34}$$

has been reached. Since $I_{L,avg}$ will have a shape which is proportional to the rectified voltage, the current will, if using this control mode for PFC, be sinusoidal in shape with a ripple envelope corresponding to Δi_L.

Another type called “constant-off-time mode” (Undeland, Mohan & Robbins 2003) will be a bit different from the tolerance band control. In this type of control there is a clock signal, of constant frequency, which turns the switch of the converter on. The switch then remains on until the current reaches the inductor average current reference $i_{L,peak}$. The switch then turns off till the next clock signal is received, which starts the process all over.

The above control schemes may only be applicable in analog systems and may be unpractical for a digital implementation. The reason being that to control the average current multiple samples may be required every switching period. This yields a problem since the conversion of the signals is not ideal and, thus, will intervene on the computation time of the processor. Rather, one current sample for every switching period could be converted. Therefore, the constant frequency control scheme is more suited for a digital controller implementation. Here the switching frequency is set constant and the duty cycle of the switch is being controlled by the current controller.

The bandwidth of the two control loops vary dramatically. The voltage loop usually employ a bandwidth at ¼ to ½ of the line frequency at 50 Hz (Dixon 2003) and the current loop cut-off frequency may lie in the range of 2 – 8 kHz for a 50 Hz system (Dixon 2003) and (Choudhury 2005) thus placing the crossover frequency at in the range of the 40^{th} to the 160^{th} current harmonic.

Due to the fact that the diode-current has the approximate shape of a sinusoidal the output voltage will show a ripple component which is the same as the frequency of the first line harmonic. If the first harmonic is fed back without any mitigation this will modulate the input current. However, there are methods to alleviate this problem and raise the power factor and decrease the current distortion of the system. There are a couple of ways to mitigate this problem.

One way of solving the problem is to have a voltage compensation which makes the voltage loop mitigate the certain frequency and, thus, not transferring it to the control voltage. This means that the cut-off frequency of the voltage loop must be very low (approximately 10-20Hz) and, thus, making the compensation slow to react on changes in load and such.

If the control bandwidth is not desired to be low then Ridley (1989) suggests a notch-filter, at the first line harmonic, may be introduced so that it is not fed back to the voltage controller. However, for a wild frequency scenario, there is a need for a band-stop filter solution since the frequency band with attenuation for the notch-filter is very narrow, and the band with attenuation must be about 400Hz wide.

Another possibility suggested by Dixon (2003) is to “sample and hold” the control voltage over one half-period of the line voltage or one period of the rectified voltage. This means that the voltage controller will not modulate the current to provide the best possible reference for the inductor current.

“If a Power factor of .95-.98 is acceptable, don’t bother with the sample and hold. On the other hand, to achieve 3% distortion (P.F = .999), the sample/hold technique is very useful.” (Dixon 2003)

2.3.1. Voltage and current compensation

To find the parameters for the voltage and current compensator of the boost type PFC-circuit the small signal models of 2.2.2 are adopted. Starting with the voltage compensation there are

different suggestions on this approach as the gain of the transfer function changes under different line conditions. If the voltage open loop is modeled as (Xie, 2003)

$$T_v = G_{vc}K_{vp} \tag{2.35}$$

where G_{vc} is the small signal analysis of the control-to-output (2.28) when the load is assumed to be a constant power load as this is usually the case in these kinds of applications, from section 2.2.2, K_{vp} is the proportional gain of the voltage PI-controller (high frequency gain) then this equation is set to 1 (0dB) for the desired cross-over frequency; thus yielding

$$K_{vp} = \frac{\omega_{cv}C}{g_c} = \frac{\omega_{cv}CkM}{V_{in}} \tag{2.36}$$

where ω_{cv} is the desired cut-off frequency of the compensator, C is the output capacitor and k is the input voltage scaling factor, M is the conversion ratio and V_{in} is the input voltage. The cut-off frequency of the voltage controller for active boost PFC is usually chosen to be at ¼-1/2 of the line frequency (Dixon, 2003).

Another suggestion proposed by Ridley (1989) is that the "high frequency gain" (K_{vp}) of the compensator should be chosen as

$$K_{vp} = \frac{\omega_{line}CkM_{min}}{2V_{in}^{max}} \tag{2.37}$$

Where M_{min} is the conversion ratio in eq (2.21), and k is the scaling constant of the rectified voltage in the model in section 2.2.2. Further, the voltage compensator zero ω_{zv} is chosen as

$$\omega_{zv} = \frac{2}{CR_L} \tag{2.38}$$

for a resistive load where R_L is the load resistance and

$$\omega_{zv} = \frac{\omega_{line}}{\sqrt{3}}\left[\frac{V_{in}^{min}}{V_{in}^{max}}\right]^2 \tag{2.39}$$

for a regulator load . Then, the voltage compensator zero can be set equal to the crossover frequency (Skanda, 2007)[3], or follow the guidelines suggested by Ridley (1989) if there is a wide variation in input voltage. There is no consistent recommendation throughout literature.

The voltage controller can be written as following for the continuous case

$$H_v(s) = \frac{v_c}{e} = K_{vp} + \frac{K_{vi}}{s} \tag{2.40}$$

where K_{vp} is the proportional gain and K_{vi} is the integrator gain.

$$K_{vi} = K_{vp}\omega_{zv} \tag{2.41}$$

[3] This is motivated that the digital delays are insignificant at the very low bandwidth of the voltage controller.

The current controller may be done in a similar manner as the voltage controller above. The open loop gain of the current loop can be written as[4]

$$T_i = G_{id} K_{ip} F_m \tag{2.42}$$

where G_{id} is the transfer function of the current stage (2.32) , K_{ip} is the proportional gain of the current PI-controller, F_m is the modulator gain which is set to 1 since when the output of the current controller is 1 the duty cycle is 100% (Choudhury 2005). By setting the above equation equal to 1 (0dB) for the desired cut-off frequency of the system the proportional gain may be found as

$$K_{ip} = \frac{\omega_{ci} L}{V_{dc}} \tag{2.43}$$

where L is the inductance of the current stage, ω_{ci} is the cut-off frequency of the current loop and V_{DC} the output voltage. The cut-off frequency of the current controller is usually chosen at 8-10 kHz for a 50-60 Hz system (Choudhury 2005). The compensator zero is chosen so that it is placed about 1/10 of the crossover frequency to provide 45^0 phase margin in the digital control system as some phase margin may be lost due to sampling and computational delays (Choudhury 2005). The final compensator has the following appearance

$$H_i(s) = \frac{d}{e} = K_{ip} + \frac{K_{ii}}{s} \tag{2.44}$$

where K_{ip} is the proportional gain and

$$K_{ii} = K_{ip} \omega_{zi} \tag{2.45}$$

is the integral gain of the controller.

2.4. **Analog and digital PFC-control**

Power Factor Correction may be performed by either analog or digital controllers. There are certain Integrated Circuits designed especially to perform power factor correction, such as UC3854 (Texas Instruments 1999). The integrated circuit incorporates a voltage amplifier for controlling the output voltage, a multiplier/divider for computing the reference of the inductor current, a current amplifier and a voltage feed forward term. As a final stage the IC incorporates a drive circuit for driving the switching MOSFET of the used topology. The UC3854 is able to be used in single or three-phase applications in the voltage range 75-275 Volts and frequency range 50Hz-400 Hz (Texas Instruments 1999). Therefore, there are uncertainties if the IC is able to operate appropriately in the range 400Hz to 800 Hz.

A digital control scheme emulates the analog controller by incorporating dual compensators, one for voltage and one for current, and input voltage feed forward. A digital PFC control scheme need to sample different signals (usually rectified and output- voltage and inductor

[4] The open loop gain of that resource is not entirely the same but includes a scaling constant aswell. However, that is because that controller is implemented using another notation than the one used in this thesis.

current) and then compute the duty cycle of one or several switching transistors - depending on PFC-topology.

The main advantage of the analog circuit is that the bandwidths of the error amplifiers are very high since no sampling is required. However, there are certain advantages of the digital PFC control scheme. A digital controller is quite simple to program as it may be implemented in a DSP and thus may be programmed using a high level programming language, such as C++. Consequently, the code is rather simple to reconfigure, in contrast to the analog controller where components must be replaced to change compensation or reference. It could even be so that the controller can adapt to changing conditions such as changes in line frequency where it can be suitable to change control parameters for the control system. Further, a processor may communicate with the rest of the power control system such as send error messages in times of failure and so on. A very powerful processor would perhaps be able to control a three-phase PFC circuit and subsequent DC/DC-converters.

2.5. Three-Phase Systems Using Single Phase Modules

While single-phase 50-60 Hz PFC-rectifiers are quite common and off the shelf products, three-phase variants are harder to come by. The complexity of constructing a single stage three-phase rectifier system is described to be considerably harder (Levy 2009) than a single-phase system. There are two basic philosophies of developing three phase active Power Factor Corrected rectifier systems. The first variant is to use single-phase modules coupled together in a three-phase configuration. It is possible to construct it with either isolated- or non-isolated output voltage. The design is somewhat harder with the isolation. These designs often involve down-stream DC/DC-converters. The benefit of the modular approach to three phase power factor correction topologies is that the existing knowledge and technology on single phase topologies may be used to form a three phase system. There is also the direct way of doing these things, in this approach the rectifier systems is constructed with starting point in the ordinary three-phase diode rectifier. There is a multitude of different solutions to this. There are buck- and boost-type systems working directly with the mains connected diode rectifier. There is also the possibility of introducing intentional harmonics in the rectifier to cancel the same harmonics in the mains-current.

Combinations of readily available single-phase modules (Kolar & Friedli, 2011) can be to achieve PFC at three-phases. The modules are then combined with down-stream DC/DC-converters, which may be galvanically isolated, to form a single output voltage which is connected to a single DC-bus on the output. There are two possibilities of coupling these systems; either in a Y-connection, or a delta-connection. The benefit of the y-coupled rectifiers is that the voltages on the semiconductors are lower compared to that of the delta-coupled system, this because the input is essentially connected to the main voltage for the delta-rectifier, while the y-rectifier is connected to the phase-voltage. While the y-rectifier has this advantage, it also has a disadvantage that the modules are coupled together. According to Kolar and Friedli (2011), the following can be concluded about the delta-rectifier.

“On the whole, then, and excellent potential for industrial application of this system can be discerned” (Kolar & Friedli, 2011)

According to Nilsson[5] there may be no neutral in the three-phase system or it may not be used for larger loads. To use this there could be demands for a "compensation net" which may be eliminated by using the delta-connection.

Mao et. Al (1997) discusses the ability to is to connect a single phase module to each of the three feeding phases to neutral. Advantages of this design is the relatively low complexity of using single phase modules and the fact that the outputs are coupled to the same capacitor and thereby eliminating the voltage ripple of the output voltage (Mao et al. 1997) which generate the possibility of fast voltage control since no ripple component is transferred back to the current control system. However, since the input current is not the same as the output current this system usually have a THD of about 10%, even though the boost inductor and the freewheeling inductor have been split. The efficiency is also claimed by Mao et al. (1997) to be quite low (90%) which makes it unsuitable for high performance applications.

Another way of combining single-phase PFC modules is to use a three-phase transformer with delta connected primaries and three separate secondary windings, which is discussed by Levy (2009). On the secondary winding there are non-isolated single phase boost PFC modules which controls the current in respective module, the controller used for this is for example the UC3854. The outputs of the capacitor banks are then connected to a common capacitor bank. This system achieves galvanic isolation through the power transformer. This design is believed to achieve 5% THD of the input current and an overall efficiency of the converter is claimed to be 95%. Moreover, this system is said to be able to deliver 3kW of power. However, this design is quite large as the 3 PFC modules have a volume of 4.3 L a weight of about 3.3 kg and the power transformer has a volume of 4.6 L and a weight of about 20 kg. The total weight and volume for this system is about 9 Litres and 24kg.

[5] Valter Nilsson, SAAB EDS, Gothenburg, 2012

3. Modeling and Simulation of Single Phase Boost PFC Module

The simulations of the single phase boost PFC circuit were done to test the current shaping properties of such a converter. The simulations where made under a general case with a 1kW single phase module in mind, this rated output power was chosen so that a three phase AC/DC converter would be 3kW. The following was investigated

- Test current shaping using a model of a digital controller for 50 Hz and adjusting the current controller bandwidth and switching frequency for 400 and 800 Hz.
- Test how different connections for delta- and y-connection will affect the current shaping properties of the circuit
- Test how the current shaping functions using the sample/hold technique suggested by Dixon (2003) for the control voltage.

In 50 – 60 Hz systems, usually a cut-off frequency of the current controller is chosen at 8-10 kHz and a switching frequency of 80-100 kHz (Choudhury 2005). However, in airborne systems the frequency varies from 360-800Hz. If having the same ratios between line frequency, current controller cut-off frequency and switching frequency as the 50-60 Hz system it would mean that the bandwidth of the current controller at 400 Hz would be 64 kHz and the switching frequency would be 640 kHz. For 800 Hz the system would have to have a switching frequency of 1.28 MHz! This could be unpractical in an actual application with current semiconductors, controllers and circuits, and as such a reduced ratio needs to be evaluated in simulations. Therefore, a reduced ratio between current controller bandwidth and switching frequency is to be investigated. The current controller cut-off frequency is chosen at the 40^{th} harmonic of the line frequency, 16 kHz for 400 Hz and 32 kHz for 800 Hz. The switching frequency is chosen to be constant for the entire interval at 160 kHz.

3.1. Simulink © model of the boost rectifier

The PFC-circuit was simulated in Simulink© with a dynamic model to represent the dynamics of the boost PFC and, specifically, to simulate the current shaping properties of the topology. The dynamics of the system was represented by implementing the differential equations described in section 2.2.1. The model is being developed by using some assumptions and objectives. The following assumptions were made

1. The input voltage is a perfect sine-wave which is being held constant, meaning no sudden changes in amplitude or frequency. Only the fundamental of the voltage is included so no harmonics are present in the voltage.

2. The output current is assumed constant and ripple-free, as there may be a regulator stage connected to the PFC-circuit.

3. The system is assumed to be operating in steady state. Thus, startup is not considered.

and the following control objectives are in place

1. The output DC-voltage shall be controlled to match the reference

2. The input inductor current shall follow the shape of the scaled rectified input voltage while having the appropriate amplitude to keep the output voltage at the correct level.

3. Feed forward of the input voltage is not considered as this is more of a phenomenon during transients.

Since the transfer functions for inductor current and output voltage are the same for both states, there must be an alternating input signal to these transfer functions to emulate the circuit dynamics. This will be discussed later on.

The overall model can be seen in Appendix D, where it consists of two blocks which represents the PI-controllers and the power electronics. The input signal for the model is the line voltage which is squared to simulate a perfect rectified voltage from the diode bridge. Moreover, another input to the model is the output voltage reference and the assumed constant output current. There are also some input "initial conditions" for the output voltage and control voltage. These are put in place for simulation purposes as to there may be a desire to simulate steady-state like behavior of the circuit. The relevant signals are then saved to the workspace for post-processing for creating plots and testing of DSP-implementable algorithms.

In Appendix D the model of the controller can be seen. It is simulated with a digital controller in mind without the input voltage feed forward, thus the controller model used is a discrete one and not the default continuous one. The discretization method is Forward Euler in these simulations. The voltage controller compares the output voltage reference to the simulated output voltage from the power electronics block - which is being applied to a "zero order hold"-block to represent the sampling of the signal. The error is controlled by an ordinary PI-controller with cut-off frequencies as described in section 3.2. The output of the voltage controller block is the so called "control-voltage" which is multiplied with the rectified scaled input voltage to form the reference of the input current. The sample and hold method was chosen to provide the best possible reference for the current to see what the best possible scenario is. The current from the power electronics is also being sampled and there is a choice in the main file of when in the switching cycle the value should be taken. Then, the PI-current controller controls the current to match the current reference. Again, the bandwidth of this controller is discussed in the next section.

The driving block of the simulation is the "PWM"-block which has three inputs: the input voltage, the simulated output voltage and the duty cycle from the current controller. The outputs consist of a voltage step and the pulses of the PWM. The voltage step is generated by taking the difference of the input and output voltage for each time instant. To represent the switching, the output voltage is multiplied with zero during the "on-time" of the switch, this to represent the voltage to ground. The PWM is an ordinary comparison of a triangular repetitive waveform with a reference and thus creating the pulses.

The voltage step and the pulses are then fed to the blocks which represent the boost circuit of the PFC-circuit; namely the "Model of the inductor" which is a simple integrator

$$i_L = \frac{v_L}{sL} \tag{3.1}$$

with the inductor value as gain to represent the inductor. This block sees the alternating voltage steps

$$v_L = |v_{in}| \quad (DT_s) \tag{3.2}$$

and

$$v_L = |v_{in}| - V_{dc} \quad (1-D)T_s \tag{3.3}$$

where $|v_{in}|$ and V_{dc} is the input and output voltage respectively.

The "Current Splitting" block then splits the inductor current into two individual currents to represent the current which is flowing in the switch and diode respectively. This is done by multipliying the inductor current with the pulses for the MOSFET current and the inverse of the pulses for the diode current, and then routing them to separate outputs.

The diode current is then used for the "Output Voltage Calculation" to represent the instant when the capacitor bank is charging. The output voltage is simulated by feeding the simulated capacitor current into an integrator

$$v_{dc} = \frac{i_{cap}}{sC} \tag{3.4}$$

with the capacitor value as a gain. As previously, there are input steps, as follows

$$i_{cap} = -I_o \quad DT_s \tag{3.5}$$

And

$$i_{cap} = i_D - I_0 \quad (1-D)T_s \tag{3.6}$$

where I_o is the output current and i_D is the diode current.

3.2. Simulation set-up

The boost-converter was decided to be simulated, at first, under the condition that the module is delta-connected to the feeding three-phase system. Under this circumstance the highest transient phase voltage which it may be subject to is 180 $V_{rms,transient}$, as described in section 1.2. To be able to perform current shaping even under high voltage transients, the DC voltage must surpass

$$V_{dc} = \sqrt{3} * \sqrt{2} * V_{rms,transient} = 440V \tag{3.7}$$

and as such the voltage V_{DC} is simulated using 450 Volts. For the Y-connected case the DC voltage was calculated to be 270 Volts using the same argument as above. Also, the converter is simulated with a rated power of 1kW and connected to a constant power load. This is to simulate a module in a 3kW three phase configuration.

Values for the capacitor and inductor had to be chosen for the simulations. Since the design specification said that one requirement was that the output voltage ripple should have a

maximum of 0.7 $V_{p\text{-}p}$ the capacitor had to be chosen accordingly, therefore the theoretical value of the capacitor bank can be computed from (2.17)

$$C = 2\frac{I_{out}}{2\omega_{line}v_{ripple,p-p}} = 2\frac{1000W/450V}{2 * 2\pi * 400Hz * 0.7V} = 1300\mu F \tag{3.8}$$

where I_{out} is chosen at full load during steady state operation, ω_{line} is chosen at 400 Hz due to that this is where the ripple will be highest. The whole expression is multiplied with 2 since (2.17) is the amplitude and not the peak-to-peak value of the output voltage ripple. Also, here was the 50 Hz capacitor calculated to be 10 mF. Similarly, the inductor value can be calculated from 2.11

$$L = \frac{V_{dc}}{4f_s I_{rip,max}} = \frac{450V}{4 * 160kHz * 0.5A} = 1.4mH \tag{3.9}$$

where the switching frequency f_s is set to 160kHz and the maximum ripple is chosen at 0.5 A as a simple design choice. The inductor for 50 Hz, at 80 kHz switching frequency, was calculated in a similar manner and yielded 2.8 mH. For the Y-connected case to also here have a maximum ripple current of 0.5 A the inductor is 0.8 mH for 400 Hz.

As mentioned earlier the bandwidth of the current controller is usually chosen at the 8 kHz for a 50 Hz system, the 160th harmonic of the line frequency, and then the switching frequency at around 80-100 kHz. However, the switching frequency of the 400-800 Hz system would be incredibly high as the 160th harmonic at 800 Hz would be 128 kHz and then a switching frequency of 1.28MHz. This is unreasonable for this system, thus a bandwidth limit was chosen at 32kHz which is the 40th harmonic of the 800Hz – the highest harmonic in the standards to be regulated - line frequency and a ratio of 1:5 was chosen for the switching frequency which gave 160 kHz. As mentioned earlier the compensator zero is often chosen as 1/10 of the cut-off frequency of the current loop.

Table 3 Simulation parameters

Parameter	Line frequency (Hz)	Value
Output Capacitor	400 & 800	1300 uF
Output Capacitor	50	10 mF
Current Shaping Inductor	50	2.8 mH
Current Shaping Inductor	400 & 800	1.4 mH
Current Controller bandwidth	400	16kHz
Current Controller zero	400	1.6kHz
Current Controller bandwidth	800	32kHz
Current Controller zero	800	3.2kHz
Current Controller bandwidth	50	8kHz
Current Controller zero	50	800Hz
Voltage loop frequency	400	100 Hz
Switching frequency	400 & 800	160kHz
Switching frequency	50	80kHz
Output DC-voltage Delta		450 Volts
Output DC-voltage Y		270 Volts
Time step		Tsw/100

3.3. **Simulation results**

A few simulations were run to study the current waveforms of the current over time for different circumstances.

3.3.1. Ripple components in simulation.

To verify that the simulation model is yielding reasonable results the voltage and current ripple are studied and compared to the theoretical values. In figure 12 the maximum current ripple can be studied. The data-tips[6] are located at the intersection $|v_{in}| = v_{dc}/2$ and the current ripple of the positive slope is 0.46A which is very close to the theoretical design value of 0.5A in (3.9). Similarly, the voltage ripple in figure 13 is simulated to be 0.6 Volts which is very close to the design value of peak-to-peak ripple in (3.8). Also, the frequency of the ripple is about 800 Hz which is to be expected for this 400 Hz simulation.

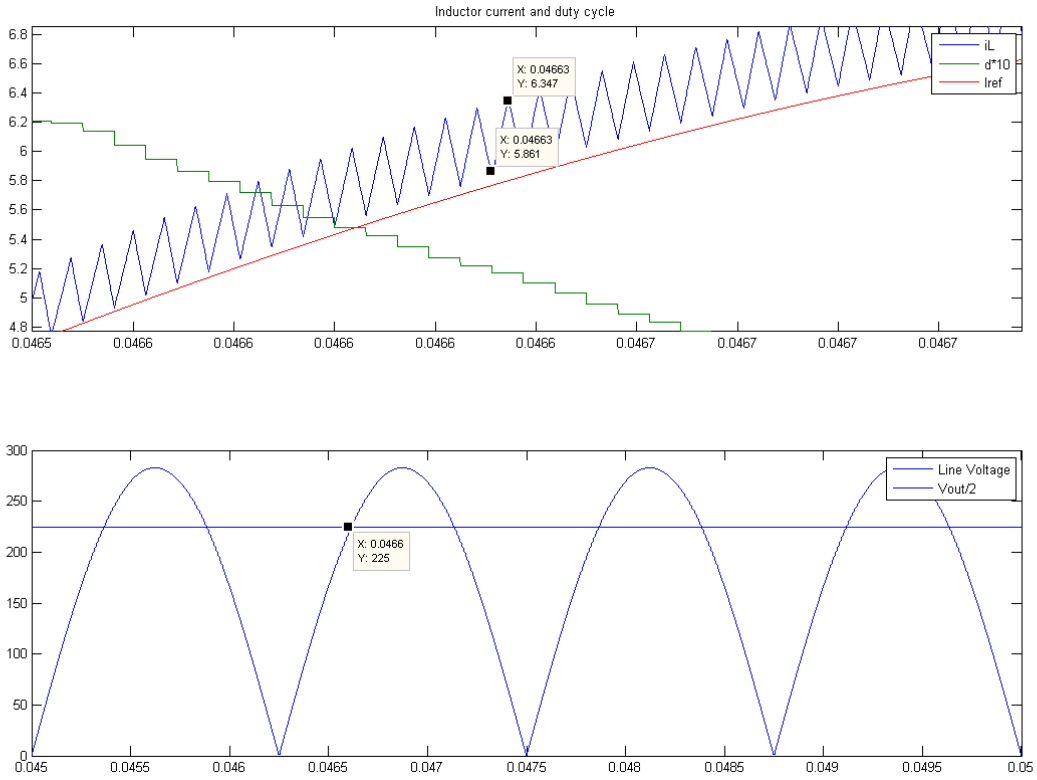

Figure 12 Current ripple of the inductor current at 400 Hz and a switching frequency of 160 kHz

[6] Information tags in Matlab plots

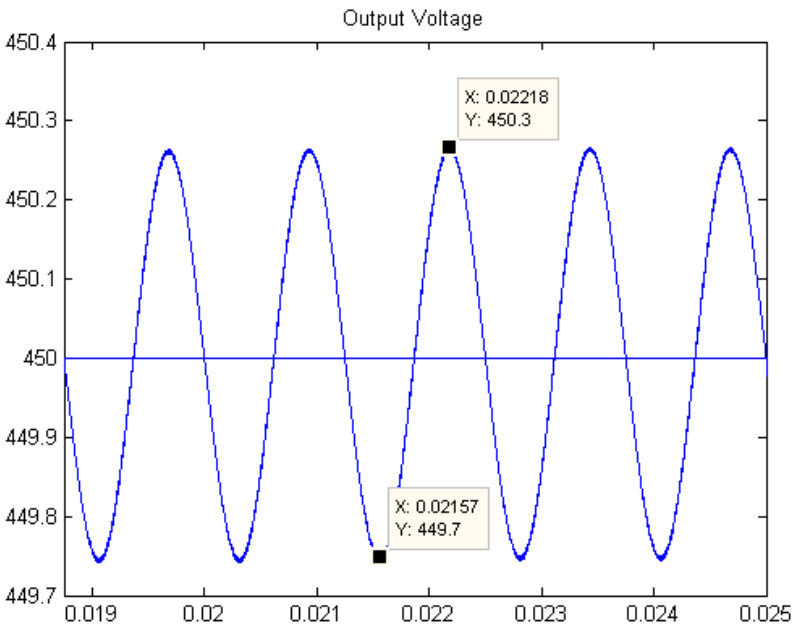

Figure 13 Output voltage ripple at 400 Hz and 1 kW output power

3.3.2. Steady state simulations for current waveforms for 50 Hz

A simulation of 50 Hz was performed with the usual cut-off frequency and switching frequency as described in section 3.2. These are to be used as a baseline for the 400 and 800 Hz simulations. The results may be viewed in figures 14 and 15. The inductor current matches the reference curve very well and there is very little zero-crossing distortion present. In figure 15 the simulated input voltage and current can be seen, these align very well and there seems to be no noticeable phase-shift between the two simulated waveforms. The oscillation in the duty cycle in figure 14 is the control system which adjusts to follow the reference.

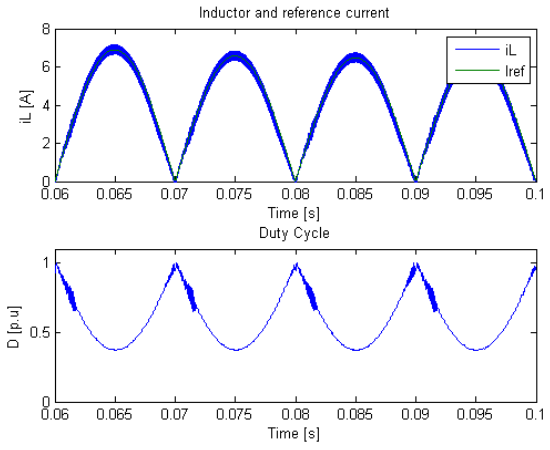

Figure 14 Steady state simulation of inductor current and duty cycle for 50 Hz

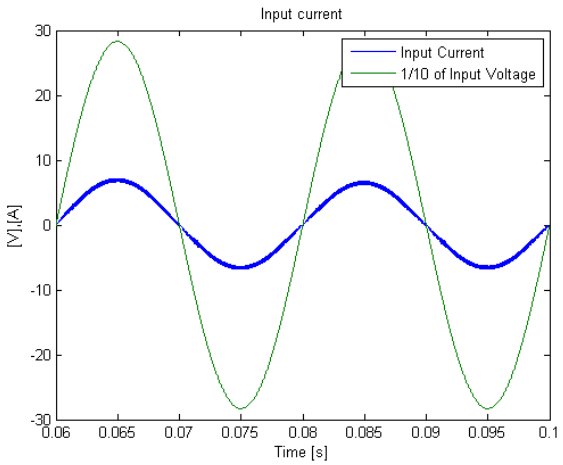

Figure 15 Simulated input current at 50 Hz

3.3.3. Steady state simulation of current waveforms for 400 and 800 Hz

The waveforms from the simulations at 400 Hz and 800 Hz can be seen in figures 16 through 19. These were simulated at the same switching frequency (160 kHz) but with different current controller bandwidth – 40th harmonic. The 400 Hz waveforms are following the

reference fairly well; however, there is a problem with zero crossing distortion. This is a known problem and is called cusp distortion (Sun 2003). The deviance from reference close to the top is likely due to the reason that the integrator of the controller builds up during the cusp-distortion period. The voltage and current waveforms in figure 17 can be seen to have very little phase displacement.

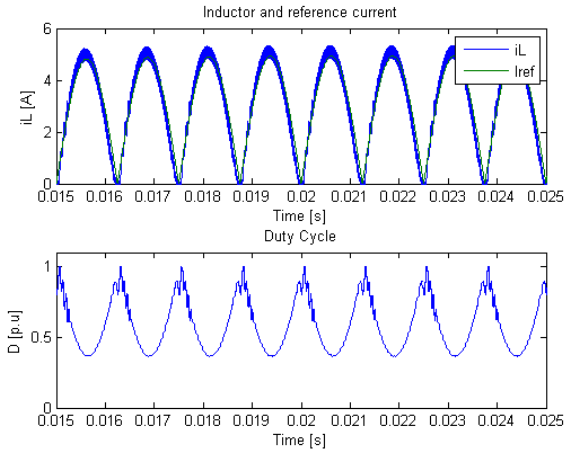

Figure 16 Inductor current and associated duty cycle at steady state for 400 Hz

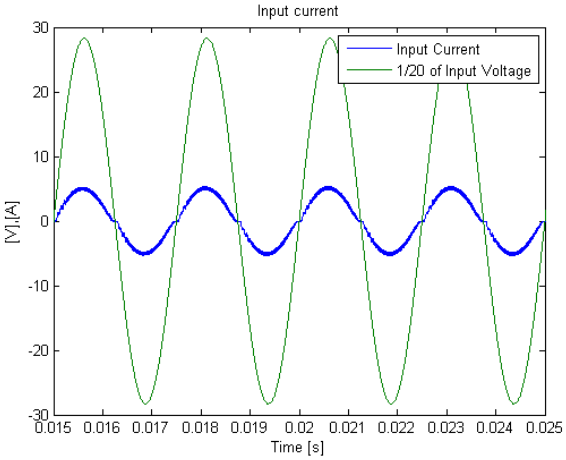

Figure 17 Steady state input current at 400 Hz

At double the line frequency the waveforms for 800 Hz show a considerably more distorted waveform; however, it does follow the reference and the input current shows very little phase displacement compared to the input voltage. As mentioned earlier, the switching frequency is held constant during these two simulations but the line frequency is doubled meaning there are only half the amount of switching periods in the latter case. Also, the derivatives at the zero crossings are significantly higher at 800 Hz then at 400 Hz.

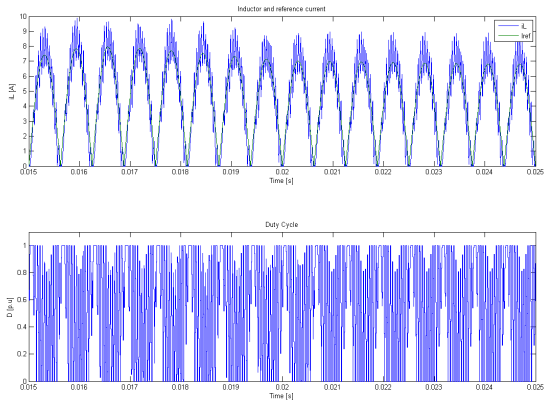

Figure 18 Inductor current and duty cycle for 800 Hz

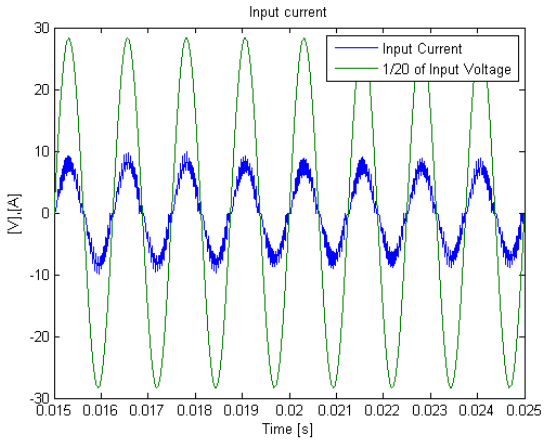

Figure 19 Input current at 800 Hz

3.3.4. Changes in current controller parameters and the effect on current control

Another simulation was made where the bandwidth of the current controller was changed to be placed at the 80th harmonic and the switching frequency was changed to 320 kHz. The simulation was performed at full output power and with an inductance which causes $I_{rip,max}$ to still be 0.5A. The results can be viewed in figures 20 and 21. In figure 20 the results for the

400 Hz simulation can be seen to be very smooth but still some problems with zero crossing distortion. The 800 Hz case in figure 21 can be seen to have quite a large ripple component but it displays a sinusoidal appearance all the same.

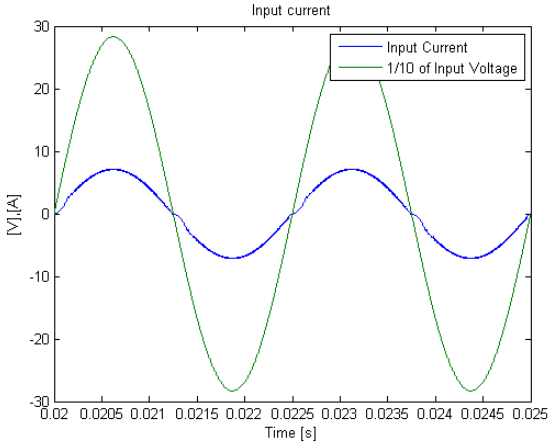

Figure 20 Input current at 400 Hz with changed parameters at double bandwidth and switching frequency

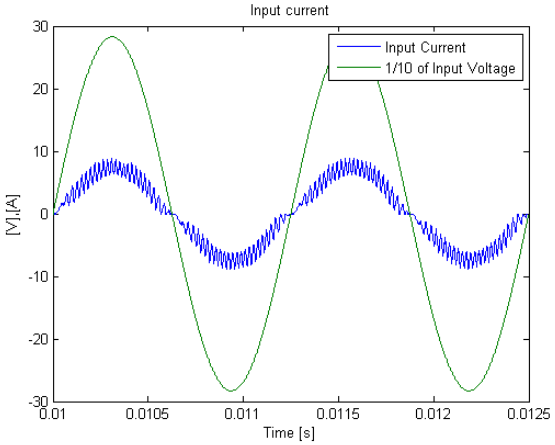

Figure 21 Input current for 800 Hz with changed parameters

In figures 22 to 23 a common cut-off frequency, with a switching frequency of 160 kHz, was set to 32kHz. The results are that the system tries to overcompensate both for the 400 and 800 Hz case. However, both systems display a sinusoidal input current but quite distorted.

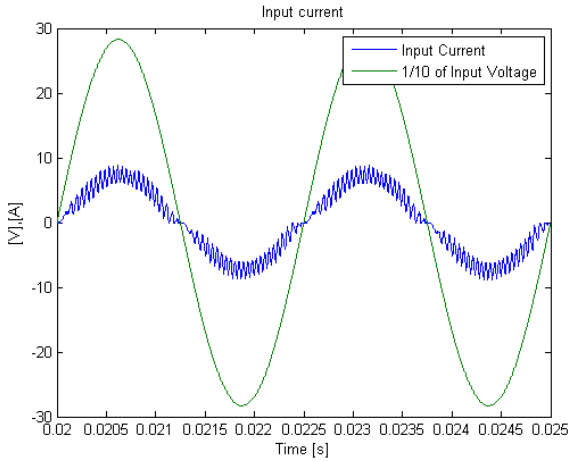

Figure 22 Common bandwidth scenario for 400 Hz

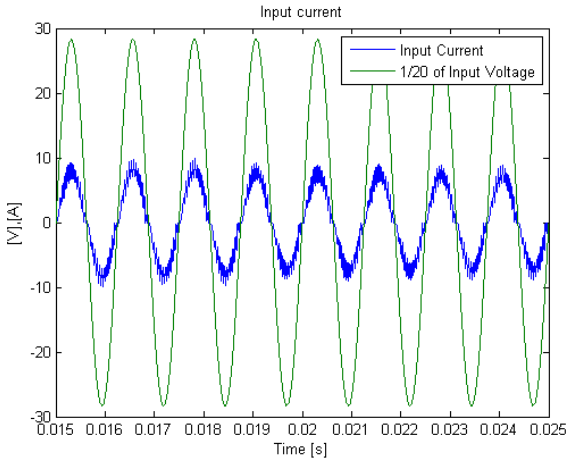

Figure 23 Common bandwidth for 800 Hz

3.3.5. Single phase module in Y-connection

In figure 24 the waveform for a Y-connected case was simulated, with line voltage 115 Volts at 400Hz, at rated output power. When the input voltage is decreased the current must increase to maintain the output power at the same level. This means that the amplitude and, consequently, the zero crossing derivative increase. The inductor value is recalculated for this scenario so that the maximum current ripple is set to 0.5 A.

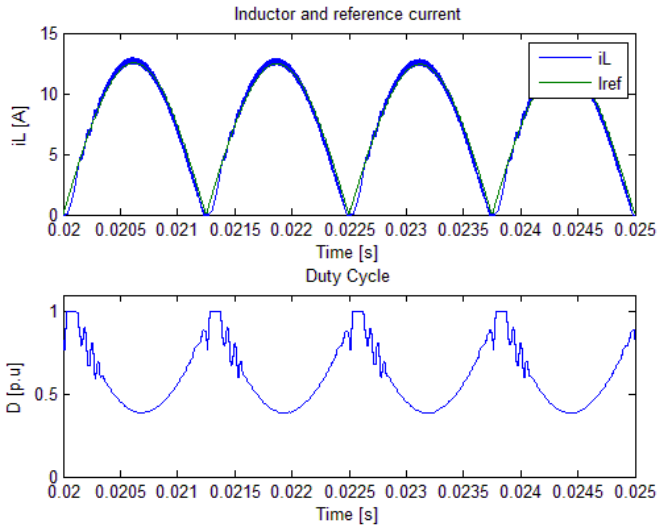

Figure 24 Inductor current at 400 Hz Y-connected

3.3.6. Applying a filter to the inductor current

The waveforms of section 3.3.2 and 3.3.3 were filtered by an ideal software low-pass filter in the post-processing to remove the switching harmonics of the current which are located at 160 kHz and multiples of that. The filter was chosen at 10 kHz suggested by Nilsson[7], as this is to be needed to maintain Electromagnetic Compatibility (EMC) in these kinds of airborne systems. The 50 Hz simulated waveform displays a near perfect appearance when the switching harmonics are removed. The 400 Hz wave form also displays a very smooth waveform, albeit the zero-crossing distortion. The waveform of the 800 Hz simulation is also improved.

A spectral analysis was performed on the waveforms in figures 25 through 27 using the Fast Fourier Transform (FFT) algorithm in Matlab and from the data the THD was calculated using (2.3) and taking the 40 first harmonics – with the motivation that these are the harmonics under regulation in the standards. The THD was calculated to be 3.2%, 5% and 12% for 50 Hz, 400 Hz and 800 Hz respectively. Thus, the distortion for 50 and 400 Hz is on an excellent level while for the 800 Hz case it is not as excellent

[7] Valter Nilsson, SAAB EDS, Gothenburg ,2012

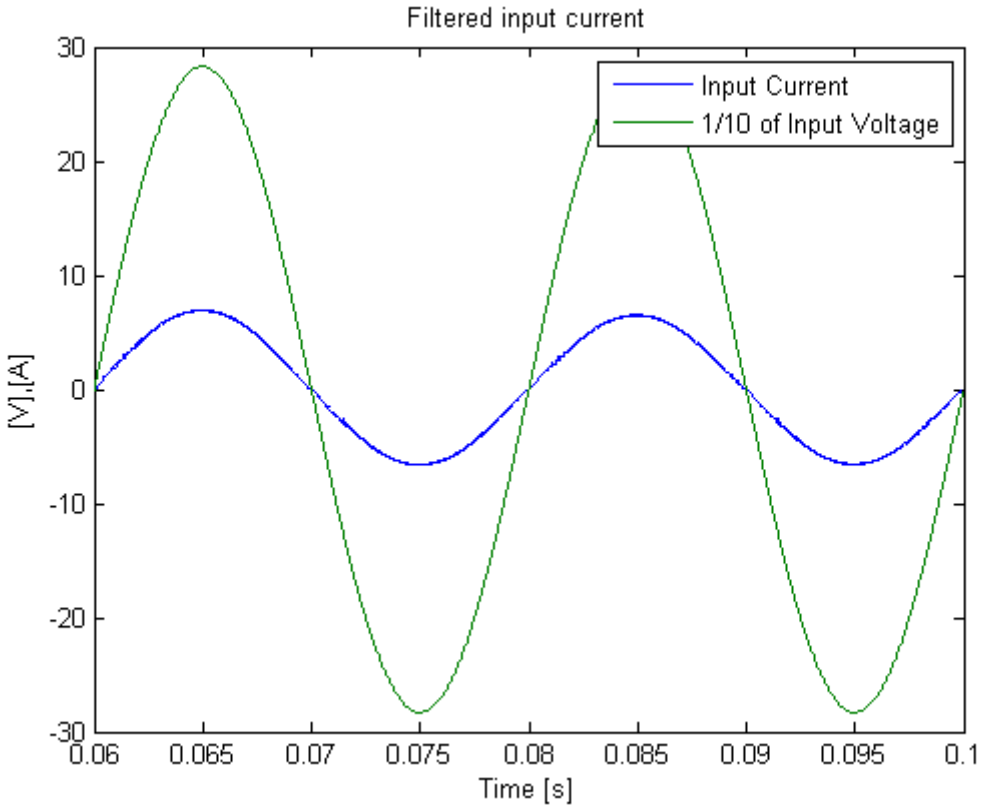

Figure 25 Filtered 50 Hz input current

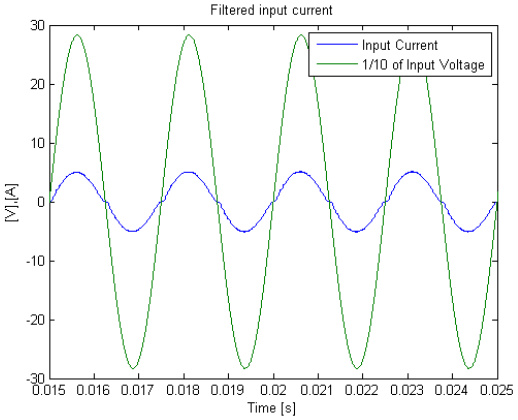

Figure 26 Filtered input 400 Hz current

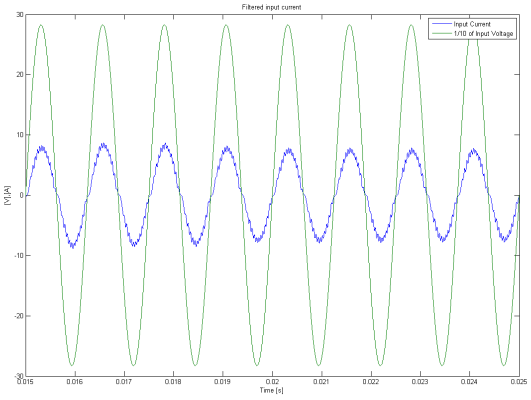

Figure 27 Filtered input 800 Hz current

3.4. **Summary**

The simulations were performed to examine the current control of a single phase PFC-module operating in continuous conduction mode. This was also done to test the feasibility of using a reduced ration between line voltage frequencies, current controller bandwidth and switching frequency. These simulations were performed under the best possible conditions.

A base line simulation was made at 50 Hz with a current controller bandwidth of 8 kHz and a switching frequency of 80 kHz. This simulation, picture 15, shows a near perfect sinusoidal

input current which has no visible phase displacement compared to the input voltage. Thus, the current control for 50 Hz seems to work fine.

At 400 Hz, using the bandwidth 16 kHz and 160 kHz switching frequency, the current follows the current reference fairly well and it is only under certain conditions where the cusp distortion becomes more pronounced; for example, when using an Y-connection where the current derivative is very steep in the beginning.

In the simulations where 800 Hz was examined the current (under the associated bandwidth and switching frequency) overcompensates. A theory to this behavior is that the controller is fed with a significantly larger value for the current error and as such saturates the controller making the system to overcompensate which gives a fairly distorted input current.

The results from the FFT indicate that the distortion of the input current is excellent for the 50 Hz case and very good for the 400 Hz case. For 800 Hz the distortion is ok but not excellent. These results show that it is feasible to run a digital controller to control the distortion of the input current to low levels for all three frequencies.

3.5. **Cusp distortion**

Zero crossing distortion is a problem in Power Factor Correction, as seen in simulations, and becomes more evident at higher frequencies. This provides to the total harmonic distortion of the system. A known phenomenon is called cusp distortion discussed by Sun (2003) and occurs near the zero crossings of the voltage. The cause of this problem is inherent in the topology and the reason is that there is an inductor shaping the current. As the current derivative can be described as

$$\Delta i_L = \frac{v_L}{L}\Delta t = \frac{|v_{in}|}{L} DT_{sw} \tag{3.10}$$

this means that the rate of change of the current near the zero crossing of the voltage is very low or near inexistent. This problem is more profound when the line frequency is increased. The behavior of three sine waves, of equal amplitude but with different frequencies, near the zero crossings can be seen in figure 28. It can be seen that derivative becomes significantly higher for 400 and 800 Hz compare to 50 Hz.

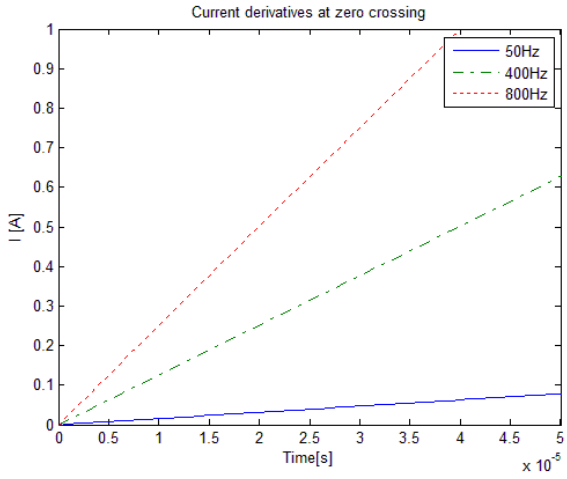

Figure 28 Current derivatives near the zero crossing

If the ripple of the current is assumed the same for the different line frequencies it is evident that the current will be less able to follow the reference as there is no way that the current can increase, even though the current controller is saturated at 100%, meaning that the switch is on all the period. An analytical function (Sun 2003) concerning this phenomenon can be derived as

$$i_L = \frac{\sqrt{2}V_{in,rms}}{2\pi f_{line}L}[1 - \cos(2\pi f_{line}t)] \tag{3.11}$$

where $V_{in,rms}$ and f_{line} are the voltage and frequency regarding the grid voltage and L is the current shaping inductor. This function can be seen in figure 29 where it has been plotted for 4 different values of the current shaping inductor, the voltage was 200 Volts and the frequency 400 Hz. The assumption is that the controller is saturated at 100% during the interval. Also, in the figure there are four different sine waves representing ideal sinusoidal currents at varying amplitude. From this figure it can be noted that the current is unable to reach the reference due to this phenomena and current amplitude adds to this problem. In figure 30 the inductor value is constant at 4 mH for the 3 different frequencies (50, 400 and 800 Hz) and the voltage is held constant at 200 Volts. These values are inserted into (3.11) and the result is plotted in figure 30. From inspection it is evident that the cusp distortion is more prominent the higher the frequency of the feeding line becomes and at 50 Hz there is barely any visible distortion at the zero crossing at all.

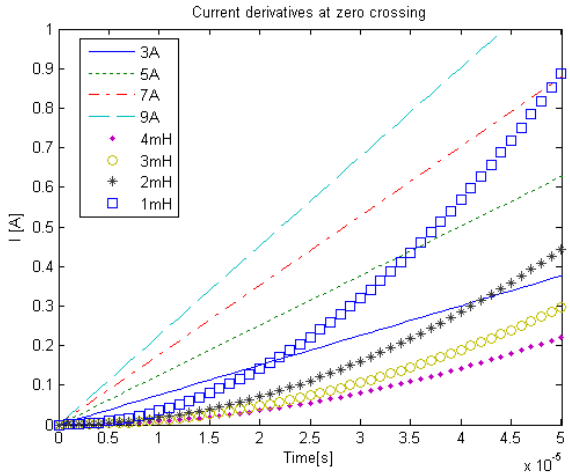

Figure 29 Cusp distortion for different inductor values

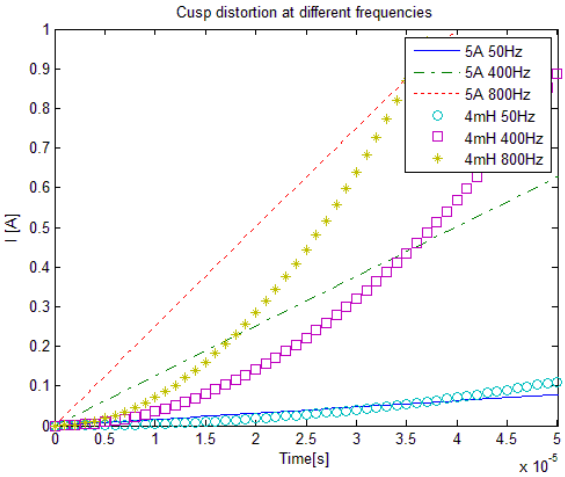

Figure 30 Cusp distortion for different frequencies

This problem may be alleviated by using a smaller value for the current shaping inductor as the rate of change near the zero crossings is increased. In figures 31 through 34 the simulated waveforms for inductor current and the reference can be viewed. The reference is a sine wave of 400 Hz and 10A amplitude. The simulations were performed by changing the inductor value so that the maximum ripple is 0.5A, 1.0A, 1.5A and 2.0A as seen in (2.12). It can be seen that with increasing allowed ripple current the problem with cusp distortion becomes less substantial, but as a consequence the ripple of the current is increased. The oscillation on the positive slope can be traced to the controller response of the current controller.

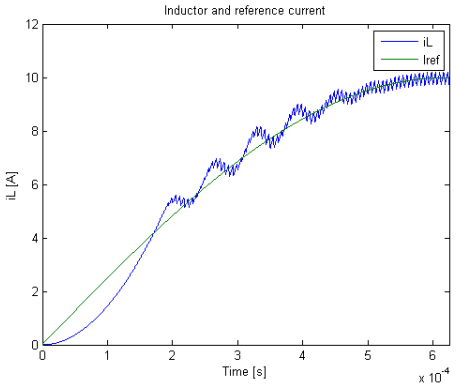

Figure 31 Cusp distortion with maxium current ripple 0.5 A

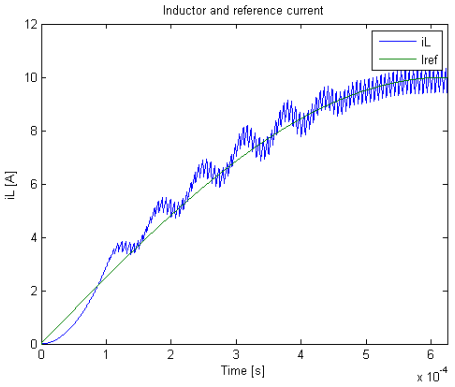

Figure 32 Cusp distortion with maxium current ripple 1.0 A

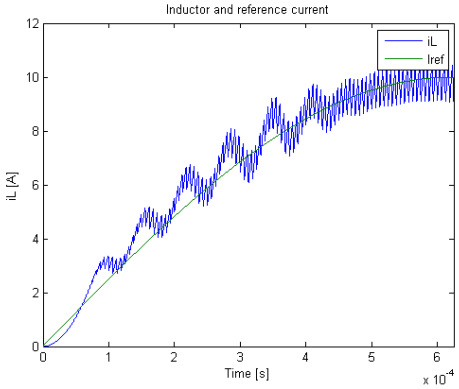

Figure 33 Cusp distortion with maxium current ripple 1.5 A

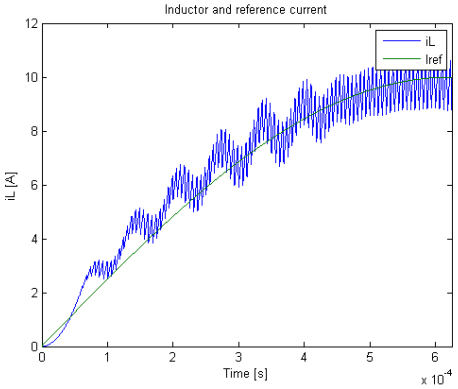

Figure 34 Cusp distortion with maxium current ripple 2.0 A

4. Design and evaluation of single phase PFC-module prototype

A prototype test system was set up to test and evaluate how a single-phase module works. The entire system can be seen in figure 35. This test system consists of several parts including hardware, digital control system and equipment related to testing. The power electronics was an old power unit which was modified, and a simple interface card was constructed for the testing. The DSP is a readily available processor with an evaluation board which was used for the testing.

The design goal is to get the system working with a feeding voltage, V_{in}, into the power unit of 115/200V and then boost this voltage to the given PFC output voltage, V_{dchi}, 190-330V. To get the voltage level at which the load operates at a downstream DC/DC bus converter with output voltage, V_{dclo}, of approximately 30-55V at no load can be used. Moreover, the input current should be sinusoidal and controlled to maintain the desired output voltage.

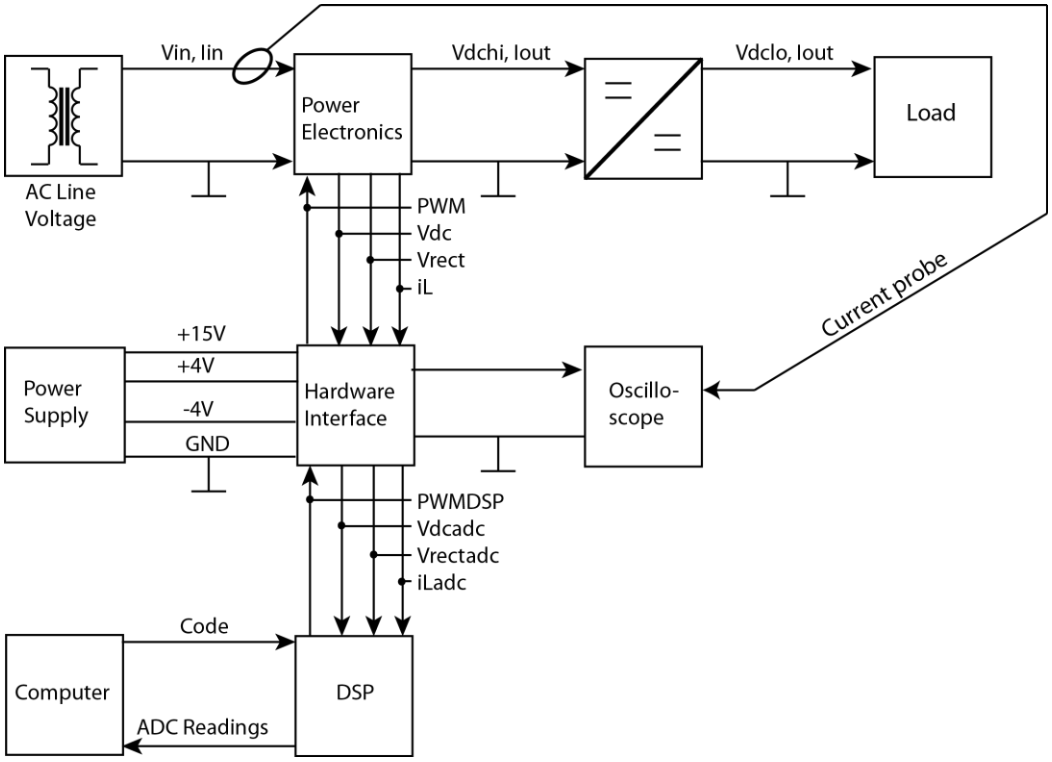

Figure 35 The entire system set-up for the single phase PFC-module prototype test system

4.1. Hardware Implementation

The entire prototype set-up contains several subsystems. Here the entire system is presented with the relevant interconnections. The block diagram of the system can be seen in figure 36, where the bold lines indicate the hardware used and following is a discussion of the different blocks, with the functions being discussed in later sections more in detail. The system will again be discussed in the evaluation-section where the experimental set-up is discussed.

The power electronics (the Power Factor Correction circuit) - consisting of diode bridge rectification and boost converter - is fed by single phase AC (50 or 400 Hz) from a stationary test signal through an isolation transformer. At certain points within the power electronics

there are extracted points where signals can be sensed, such as the rectified voltage, V_{rect}, the output voltage, V_{dc}, and the voltage over a current shunt for sensing the current, i_L. Also input current waveforms will be monitored with a current-probe connected to a oscilloscope to monitor its behavior.

These signals are fed from the hardware into a hardware interface where the signals are adjusted so that the DSP may sense them. This is necessary since the maximum voltage allowable on the ADC inputs of the DSP is 3 Volts while the actual signals may range from 0-400 Volts. This calls for a hardware interface between the two circuits. Also, the PWM pulses created by the DSP is approximately 3 Volts and as such they need to be amplified on the interface card to be able to drive the switching MOSFET of the Power Electronics.

Downstream DC/DC converters can be put in place because the subsequent systems works at a voltage which is far lower than the one generated by the PFC system (190-330 Volts). These are manufactured by VIcor Corporation and they are reducing the voltage with a fixed ratio. The modules can be put in parallel so that load sharing is accomplished; thus increasing the power output of the system.

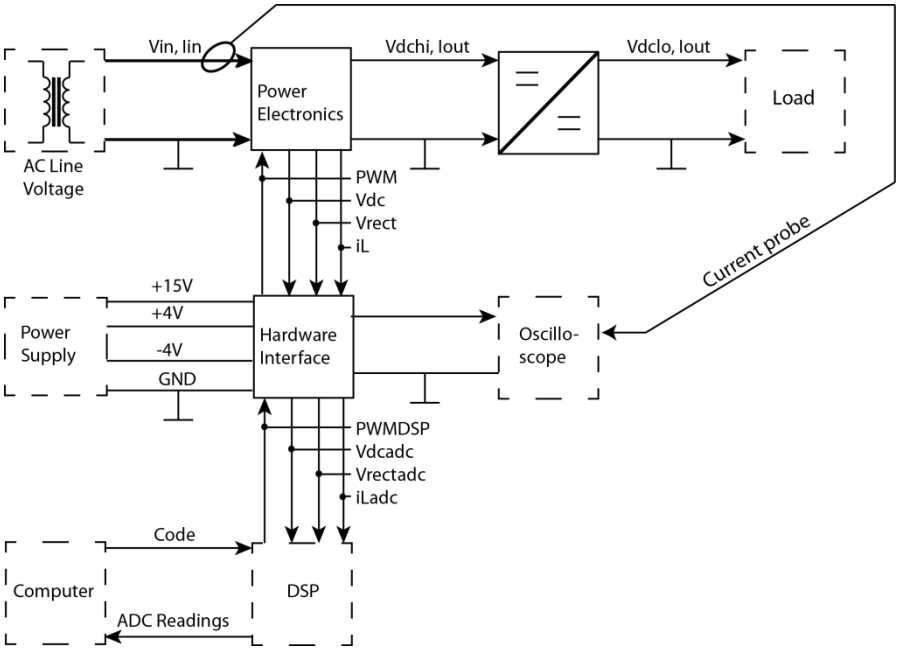

Figure 36 Hardware set-up

4.1.1. Power circuit

The power circuit, figure 37, is an old prototype, the schematic can be found in Appendix B. First there is a boost-type PFC-circuit with a line filter in front of it with a cut off frequency of approximately 8 kHz. The current shaping inductor has a value of 0.9 mH. At the output there are two parallel connected output capacitors each with a value of 330 uF.

Directly after the boost-converter there is a buck-converter lowering the output voltage to a voltage used by the other equipment (285V) on the card. This buck-converter is to no use for this project and is therefore bypassed. Incisions into the circuit were made to bypass the buck-

converter by removing its MOSFET, only keeping the PFC-circuit. Wires were soldered to key places to sense key signals and driving the switching transistor of the PFC circuit. The modification made to be able to connect the gate-driver from the interface card to the PFC includes disconnection of the old PFC-control "chip". This is made by "de-soldering" the components following the gate-driver output of the PFC-chip. Some capacitors were removed to improve the waveform of the rectified voltage. To lower interference from the surroundings, the driver connection between the MOSFET and the hardware interface card is made by a coaxial cable tightly mounted on the card with paths as short as possible.

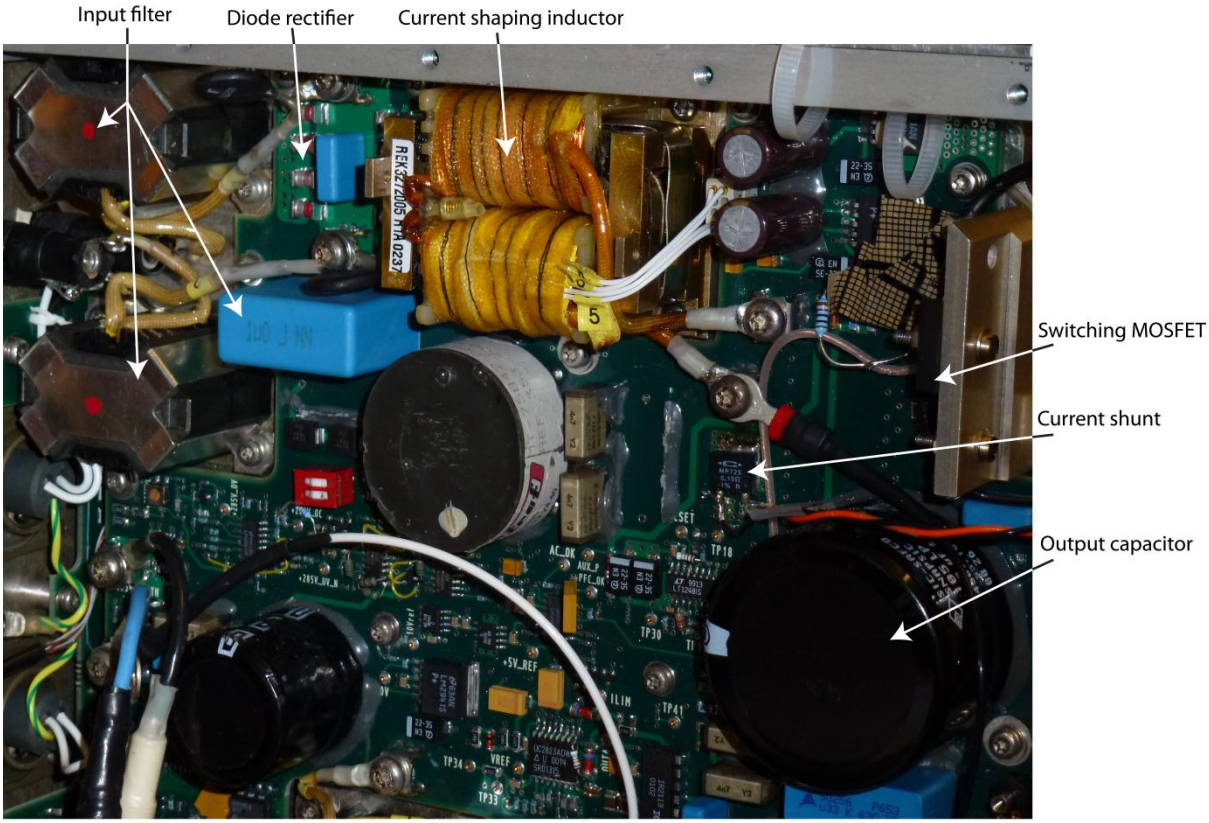

Figure 37 Hardware power circuit

4.1.2. Hardware interface between Digital Signal Processor and power circuit

The processor and the power circuit are not in any way suited to be coupled together directly. The measured signals from the power circuit may range from 0-400 Volts and the maximum voltage on the IO-pins of the processor shall not exceed 3 Volts. Also, the processor is not able to drive the MOSFET of the PFC-circuit. Therefore, a hardware interface, Appendix B, between the two systems must be introduced,

There is a need for measuring voltages in the rectifier, and therefore ordinary voltage dividers will be put in place to convert the high voltage into voltage levels more suitable for the ADC-conversion of the DSP. Since the ADC is done by charging capacitors inside the DSP (Shinde 2008), there is a need to adjust the impedance of the source to ensure accurate readings. Thus, a buffer will be used in conjunction with all voltage dividers. The buffer circuit used is OPA230.

The inductor current will be measured with a low-ohmic resistor in the return path of the current. The signal will then be sensed via a differential amplifier. This differential amplifier is an IC (INA134) which has unity gain.

Since the DSP only sends PWM-pulses at 3.3 V, it cannot drive power MOSFETs on its' own. Thus, a drive circuit (MCP14E10) has been put in place to amplify the pulses to 15 Volts. Great care was taken so that the drive circuit was separated from the sensing circuits to avoid noise in the sensing of the signals. This includes separating the grounding paths from the other and twinning the signal wires to try keep disturbances low.

Power supplies were used to provide +15V, +4V, -4V and ground. An important matter in the supply of the circuits is to introduce adequate decoupling to reduce noise in the circuit. 10 nF and 10 uF tantallum capacitors were inserted in the circuit. Test points were set up through a 10kohm resistor to alleviate sensing with the oscilloscope.

4.1.3. Down-stream DC/DC converter

As mentioned earlier there is a need to lower the output voltage of the PFC-boost converter which ranges to the 300-400V-level down to the specified output voltage for the power unit in the 50-60V range. This "bucking" of the voltage is done in this case with bus-converters from VIcor Corporation (2011) with a fixed ratio of 1/6 at no load. The modules are prefabricated and already have a set ratio; therefore the input voltage to the device has to be regulated to the right levels to get the desired output voltage. The modules are connected in series with the AC/DC converter which makes it possible to regulate the voltage into the bus-converters. To be able to manage the load condition for the power unit these bus-converters has to be paralleled, this is due to their maximum power level of 270W. These bus-converters also has the feature of being galvanic isolated which is of great importance for these applications.

To make paralleling possible of several Bus Converters of the VIcor type (VIcor 2011), there is a need of having a "trigger voltage" connected to all devices fed from the same source. This is done to make the devices switch at the same time at all instances making them split the current and thereby taking higher input power rates. If not, the devices will switch at different times making the transfer-capacity of the whole device lower.

Things that have to be taken into consideration upon deciding on what component to use are what specifications the device has. That may involve how it behaves under certain conditions such as ripple, THD, Power Factor etc. As mentioned among the different standards there are regulations regarding these parameters, and all these has to be considered upon designing of the whole circuit. The VIcor components investigated has the nice feature of being specified for different standards, among them are the MIL-STD-704E/F (Airborne standard) included for the device. This makes it a great choice for this application.

4.2. **Digital control**

The reason for choosing digital control for this kind of project is to study how the system behaves and what benefits digital control may have. Also the possibility to monitor values in real time and the ease to change parameters and control algorithms instead of changing the hardware as is in an analog control set-up is a great advantage. Also, the prospect of controlling a three-phase application was interesting to observe.

In figure 38, the control system is shown and it can be seen how the set-up is configured. The hardware interface is constructed, as mentioned earlier, in such a way that the signals from the Power Electronics are senseable by the DSP - ensuring that they are in the 0-3 Volt range. Also, the PWM signal from the DSP is amplified to drive the MOSFET. Further signals are those between the computer, connected via a USB interface, to the evaluation board and the DSP. The computer is there to provide the processor with the software that it utilizes and to monitor the readings of the ADC in real time in the computer as well as giving power to the DSP making it run in this case. Also, relevant parameters in the code of the DSP may be updated continuously from the computer.

In this section the digital control is presented and discussed. First, an overview of the evaluation kit is presented. Second, some information regarding the peripherals of the processor is discussed. Third, the program outline and how the controller runs is discussed. Fourth, the control algorithm is discussed and how it was implemented. Lastly, the "slow loop" is discussed. The program code may be viewed in Appendix A.

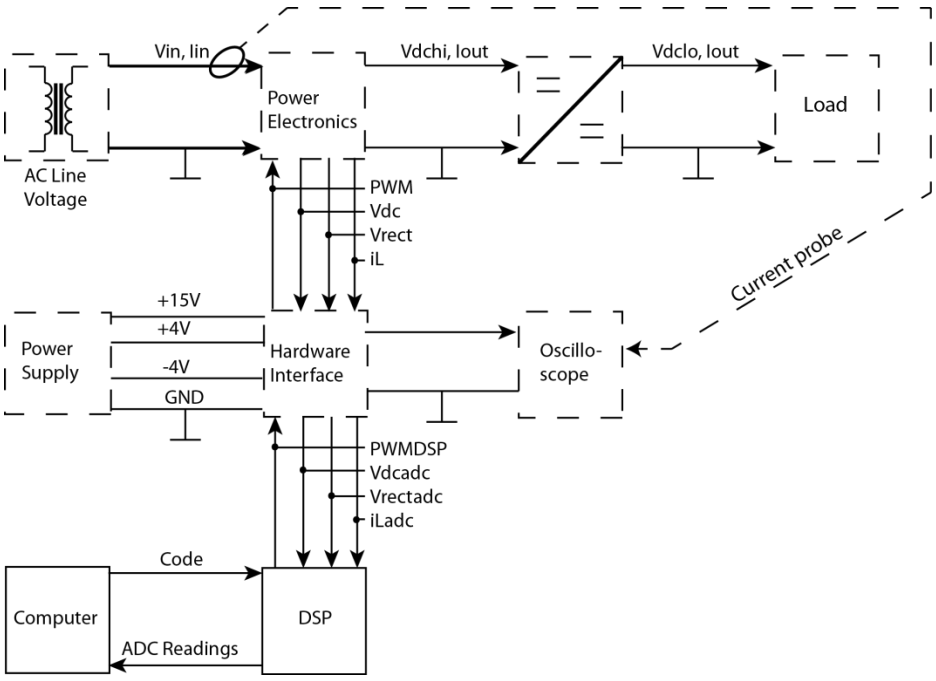

Figure 38 Connection of Computer and DSP

4.2.1. Digital Signal Processor

The Digital Signal Processor (DSP) that is used in this project is one of Texas Instruments (Texas Instruments 2012) development kits including processor and Experimenter's Kit USB Docking Station in Figure 39. The processor-unit is the F28335 Delfino™. This processor is the top model of the F2833*-series with a clock-frequency of a maximum 150MHz, built in flash 512kb, 18 PWM-channels and a ADC conversion time of 80ns for the 16, 12-bit ADC-channels. Programming and implementation of control algorithms are carried out in Code Composer Studio v5. also distributed by Texas Instruments. This software lets the user monitor variables live to make evaluation easy and make changes in an easy way. The programming-language used are C/C++ and much of the code are carried out in "predefined" code blocks that includes the settings for different parts of the DSP like the ADC-module, ePWM-module, CPU-clock etc. where changes may be done to make it behave in different ways.

The DSP get its power from the computer USB-port through the docking station, but there is also a possibility to connect external power to the docking station. In that way there is no need of having the computer present when running the DSP, except if there is a need to monitor values live and when the code is loaded into the processor.

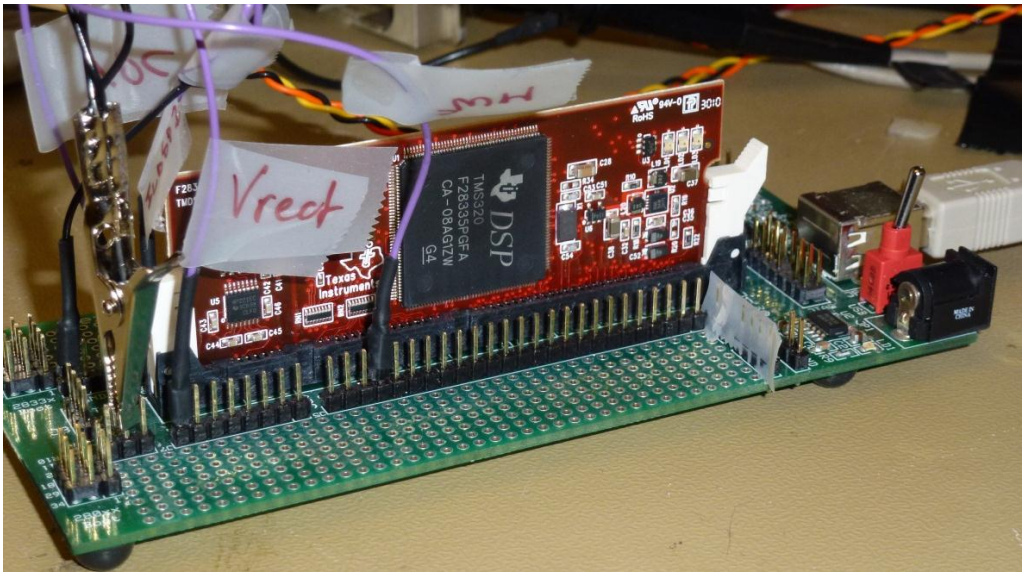

Figure 39 Digital Signal Processor

4.2.2. Configuration of DSP peripherals

As for configuration and programming of the DSP some things has to be decided before start of the actual program. These things are for example decisions of how to sample analog signals, what kind of PWM that is desired for the applications amongst other details. All these settings are put into different configuration files programmed to suit the DSP to be able to make it operate as desired. Modules necessary for this project are mainly except the usual CPU-configuration, clock settings etc. the ADC and PWM modules which will be discussed more in detail here. The other modules used to configure the DSP are carried out in "predefined" code blocks as mentioned in the previous chapter.

As for the ADC module it consist of two 8-channel multiplexer (MUX) sets which makes the module consist of 16 channels in total (Texas Instruments 2007). These channels can either be configured to work as one single 16 channel module or to be able to work as two separate 8 channel modules individually. Once the sampling is done, a value is stored in the ADC-result registers, and from here values can be extracted and used for whatever application wanted with the right conversion factor. Each of the two multiplexers are connected to a separate S/H circuit which makes it possible to sample one channel each simultaneously and thereby be able to calculate the instantaneous power for example. What has to be taken into consideration when connecting analog signals to the experimenter's card and ADC module is that the unit can't take values higher than 3V, as previously mentioned. As for synchronization and start of conversion for the ADC module there are some ways to trigger this. It can either be done by an external signal or input triggering the sampling, or as in this case with the ePWM pulse. This means that when the ePWM period starts it also triggers a start of conversion meaning that the ADC starts to sample signals in the given order programmed in the ADC-module. Then after the values has been sampled the main-routine are triggered and calculations are being done.

The conversion circuit can be represented by a resistive network with a switch (Shinde 2008), figure 40[8]. The source is represented with an alternating voltage source and a source resistance. Subsequent passive elements in the figure includes the parasitic capacitance of the input pin, C_p, the resistance of the multiplexer path, R_{on}, and the sample & hold capacitor. The S/H capacitor is charged to attain the value of the input signal; thus requiring the signal to be somewhat stable during the conversion interval. However, to increase the accuracy of the conversion, a buffer and low-pass filter may be added to the input to decrease the source impedance and filtering away noise. Another benefit being that this setup adds isolation for the processor.

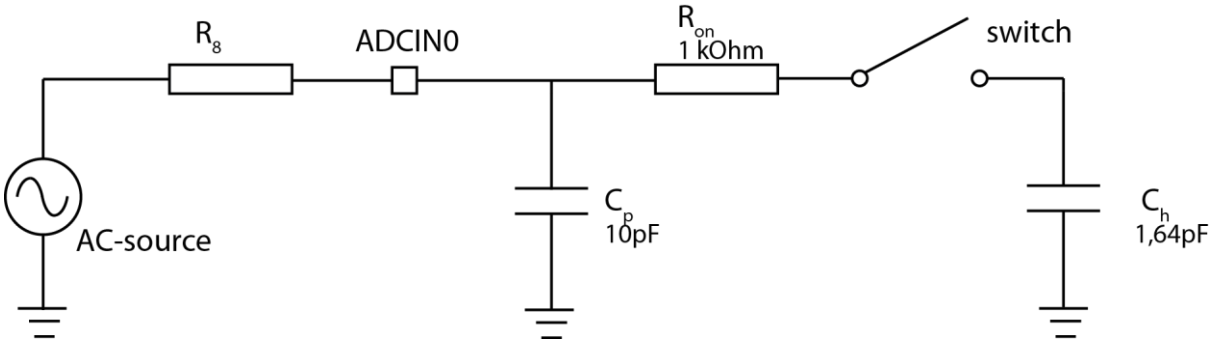

Figure 40 Physical input of the Analog to Digital Conversion Module

The PWM generation of a digital processor differs somewhat from the conventional technique in which analog control systems creates the driving PWM-pulses. In the conventional analog system, a controller outputs a voltage, which is within a given interval, and this is compared with a repeating triangular wave with a set switching frequency. Consequently, depending on choice of design, when the two voltages are equal the pulse either goes from high to low or

[8] Inspired by Shinde (2008)

low to high. There are numerous different integrated circuits which are able to perform this and, as well, control the output voltage, limit overcurrents, performing soft-start of the converter and so on.

The function of the processor is somewhat similar; however there is an increased ability to configure the PWM. While the analog system uses an actual ramp, the digital system uses user-defined software counters and counter-compare functions (Texas Instruments, 2009). The counter is set relative to the system clock; thus, the number of counts and the clock determines the switching period. The counter-compare function on the other hand determines the duty cycle. How this works is that when the two above mentioned counters are equal, the processor will act by either changing the output from high to low or low to high, based on user customization. Further, the counting may be done in different ways. The processor may choose to make the processor count up to its' final value, count down and count up and down. For this project up-count mode is used. This is shown in Figure 41 together with the previously described ADC-logistics and calculations.

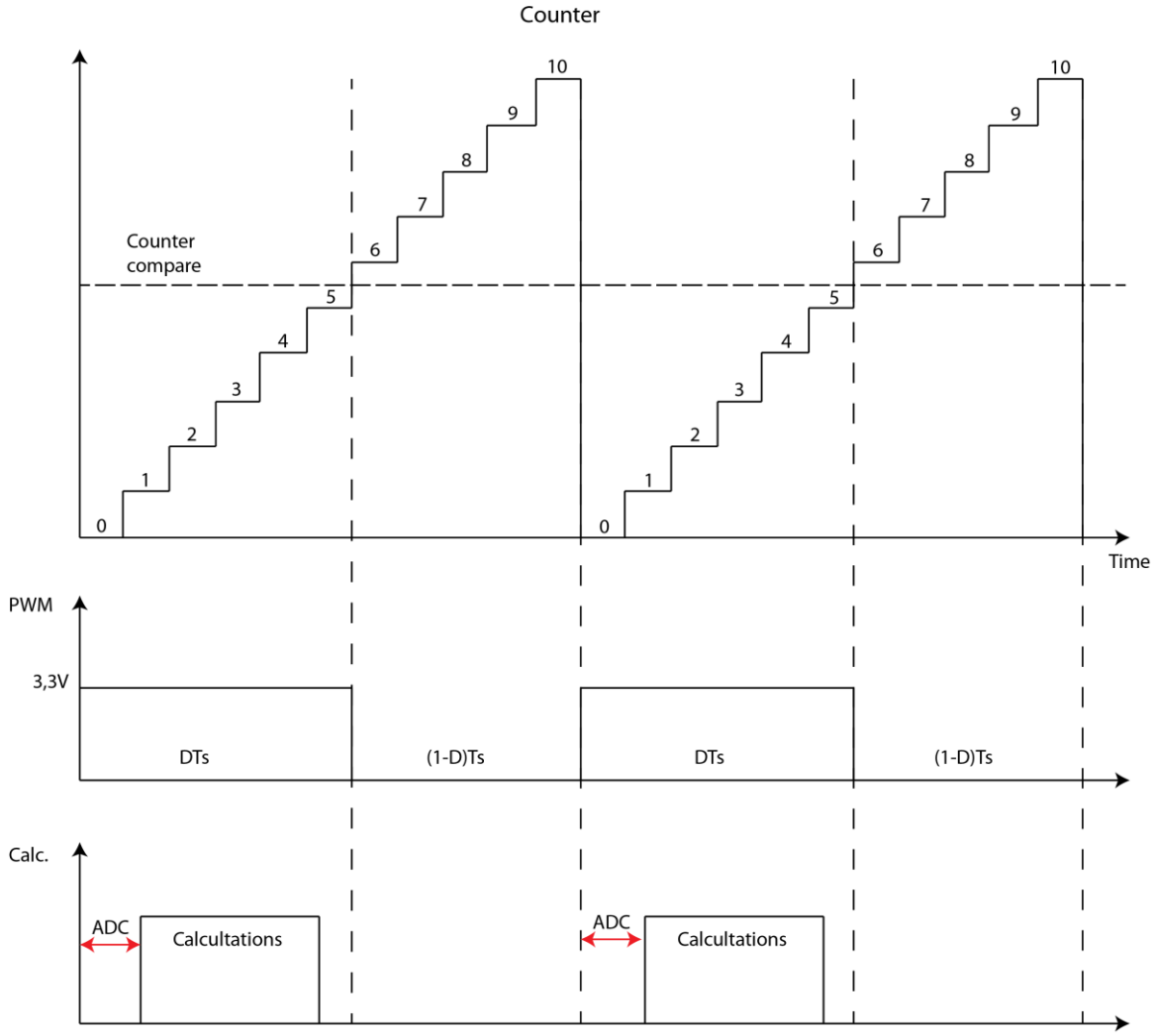

Figure 41 Illustration of PWM creation in a digital system

The pulse width modulation module consist of seven sub-modules which each help during configuration of the ePWM. The different sub-modules each has different registers where values are input to set different registers making the ePWM behave in a way the user wants.

The Time-Base sub-module is used to scale the PWM clock compared to the system-clock, this also includes settings of the counter period and frequency, resulting in what switching frequency will be used. Also there are settings of how the counter will work. These choices may be if one wants to have the counter count up, down or up-down count. The counter compare module specifies the duty and at which times switching will occur in the two PWM registers EPWMxA and EPWMxB. To specify what action will be taken when a time base or counter compare action occurs, an Action-qualifier module will be used. This module sets if there is no action to be performed or for example toggle the PWM-registers high or low. This module also configures and controls the PWM dead-band through the software. The control of supplementary dead-band are set in a Dead-band sub-module where the times are setup regarding the upper/lower switch. What is specified here are what delay values will be used for the rising and falling edge. To enable ePWM events that triggers interrupts and start of conversion in the ADC a Event-trigger sub-module are configured in different ways to meet the requirements wanted. This module also sets at which rates and how often different events will occur. A lot of settings can be made to make the ePWM behave in a way specified for the task. Two modules not used for this specific project are a module that configures the ePWM to react on trip-zone pins located on the experimenter cards as well as events that creates a chopped carrier frequency etc.

4.2.3. Program outline

The program outline for controlling the PFC circuit can be seen in figure 42. At the end of the PWM-period there is a signal, Start of Conversion (SoC), indicating for the ADC-module that conversion of values should commence. After this is done there is an interrupt for the Interrupt Service Register (ISR) to execute the main-routine of the program.

At the very beginning, the values from the ADC-conversion are gathered from the register and these are converted to the actual values i.e. before the potential dividers and such; thus, the actual voltage and current measurements. Afterwards, the “slow loop” is being executed to progress a counter and to gather values of the rectified voltage. If the voltage falls below a certain level the average voltage and line frequency are calculated since this means that there is an incoming new period.

After the counters have been progressed or new values has been calculated, the two compensators acts. The voltage compensator will act to reduce the error in output voltage by increasing the input current amplitude which is being sent to the current compensator. Subsequently, the current compensator acts to adjust the duty cycle enough so that the input current follows the reference. The current reference consists of three components: the rectified voltage for shape, the output of the voltage controller for magnitude and the input voltage feed forward which adjusts for changes in line voltage as described earlier. When a new duty cycle has been calculated this is sent to the PWM counter compare register for the next pulse.

Last in the main routine, certain values of the current iteration of the control loop is being saved for the next iteration i.e. the duty cycle, voltage- and current- error and control voltage.

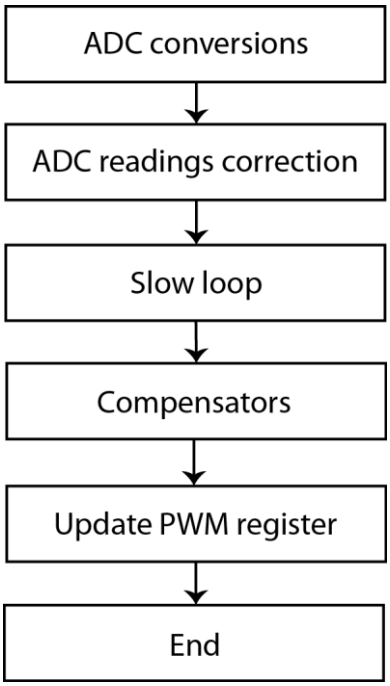

Figure 42 Program outline

4.2.4. Control algorithm

The control algorithm is based upon a two loop control system where there is an inner current loop which controls the current by adjusting he duty cycle to follow a rectified sinusoidal reference whereas the input voltage provides the shape of the current, the output of the outer voltage controller provides the amplitude, and the voltage feed forward term provides information regarding voltage amplitude.

The PI-controllers has been discretized from the continuous form by applying the forward Euler-method. The Forward-Euler method was used since this is the one being used by the discrete controllers in chapter 3. The voltage controller is on the following form

$$u[n] = u[n-1] + K_{vp}e_v[n] + \left(K_{vi}T_{sw} - K_{vp}\right)e_v[n-1] \tag{4.1}$$

where K_{vp} denotes the proportional constant, K_{vi} is the integral constant and T_{sw} is the time step – which is equal to the switching period. The term $e_v[n]$ is the voltage error from the most actual samples taken and $e_v[n-1]$ is the cumulative error from the previous period. The output u[n] is the control voltage and u[n-1] is the control voltage from the last iteration.

The current PI-controller is on the same form as the voltage controller

$$d[n] = d[n-1] + K_{ip}e_i[n] + \left(K_{ii}T_{sw} - K_{ip}\right)e_i[n-1] \tag{4.2}$$

where K_{ip}, K_{ii} and T_{sw} is the proportional constant, integral constant and time step respectively. $E_i[n]$ and $e_i[n-1]$ are the errors, similarly, as in the case of the voltage controller.

The output of the current controller is he duty cycle d[n] and this value is directly sent to the PWM-registers. The above equations are directly implementable in the software of the DSP.

Regarding references in the control loops, the voltage reference is externally set (or possibly saved in the code) so the program will strive to control the output voltage i.e. the voltage over the output capacitor bank to a certain value. To do this, the amplitude of the sinusoidal input current must be controlled so that this is achieved. As mentioned before, the samples of the rectified input voltage provide the controller with the shape of the current and the voltage feed forward term is used to correct for changes in input voltage. Thus, the current reference will be

$$i_{ref} = v_{rectified} v_{control} v_{feed\ forward} \tag{4.3}$$

and the feed forward term comes from the following term suggested by Choudhury (2005) and Skanda (2007)

$$v_{feed\ forward} = \frac{1}{V_{avg}^2} \tag{4.4}$$

where V_{avg} is the average voltage which is being computed in the "slow loop" during each half cycle of the input voltage. The above term is proportional to the RMS-voltage of the input voltage (Choudhury 2005). Thus, if the input voltage is decreased the i_{ref} term will be increased and vice versa to maintain constant power.

Considerations that has to be done while implementing the control algorithm are that values from the ADC must have time to be read and calculations needs to be done before the next period starts. To do this, algorithms must be optimized to only take necessary variables and equations into account in the given timeframe.

4.2.5. The slow loop

The "slow loop" was mentioned earlier and it is used to perform calculations regarding average voltage and line frequency. The method utilize the same principle as zero crossing detection and was inspired from Choudhury (2005) and Skanda (2007) and the method can be viewed in figure 43. Essentially, the software samples the rectified input voltage several times per half period and if the voltage is above a certain voltage level - about 3-10 volts to achieve increased noise resistance near zero crossings - a counter is progressed and the value of the voltage is being saved. These values are then used when the voltage drops below the preset voltage level again to perform the computation of the line frequency

$$f_{line} \approx \frac{1}{2NT_{sw}} \tag{4.5}$$

and

$$V_{avg} \approx \frac{1}{N} \sum |v_{in}(i)| \tag{4.6}$$

where N is the counter value, T_{sw} is the switching period (which is constant) and $|v_{in}(i)|$ are the samples of the rectified input voltage.

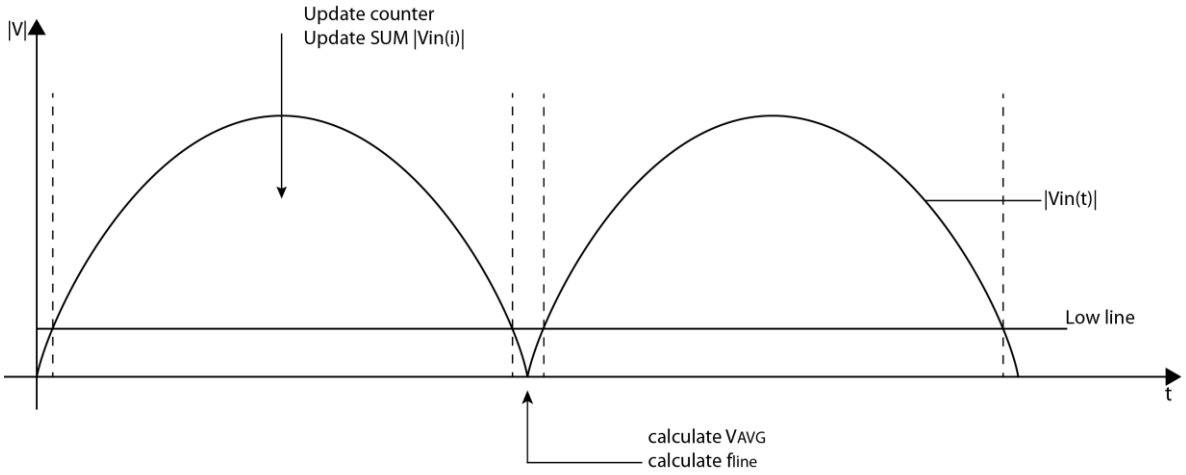

Figure 43 Illustration of slow-loop algorithm

The reason for computing the line frequency is that this gives the possibility of adjusting control parameters after the input voltage frequency if need be. If it is desired to perform sample and hold on the control voltage this could be programmed into this loop so that the amplitude of the current is updated when the rectified voltage falls below the "Low line"

4.3. Evaluation

The test system was set up as in figure 44. The power electronics were fed through a stationary AC-voltage of 50 or 400 Hz. An isolation transformer of approximately 500 VA was used for the 50 Hz testing and a larger three-phase transformer of approximately 3kVA for the 400 Hz. These were set up before the power electronics, purely for isolating the system. The load in this case was ordinary adjustable resistors in the range 0-300Ω and the power supplies were ordinary laboratory power supplies. Digital Multi-Meters were set-up to measure input voltage and current RMS as well as output voltage. The actual set-up may be seen in figure 45.

The oscilloscope was connected to monitor input current, output voltage and the rectified voltage directly after the bridge rectifier of the power electronics. The test points on the interface card alleviated the sensing of the voltage. Also, a power analyzer (Norma 4000) was put in place right before the power electronics to compute Total Harmonic Distortion, Power Factor, active and reactive power. Test-notes can be found in Appendix C.

For 50 Hz, the tests were performed with input voltages 115 Volts and 200 Volts to simulate a single phase module in either delta or y-connection since these are the line voltages to be expected in an airborne system. However, in the 400 Hz case the voltage was set to 200 Volts directly.

During the testing the downstream DC/DC converter was not used. The reason for this is that since the device has a fixed ratio it was not so interesting to examine its' function because if

V_{dchi} was of appropriate magnitude V_{dclo} would be so as well. Also, voltage control was only studied in a superficial manner.

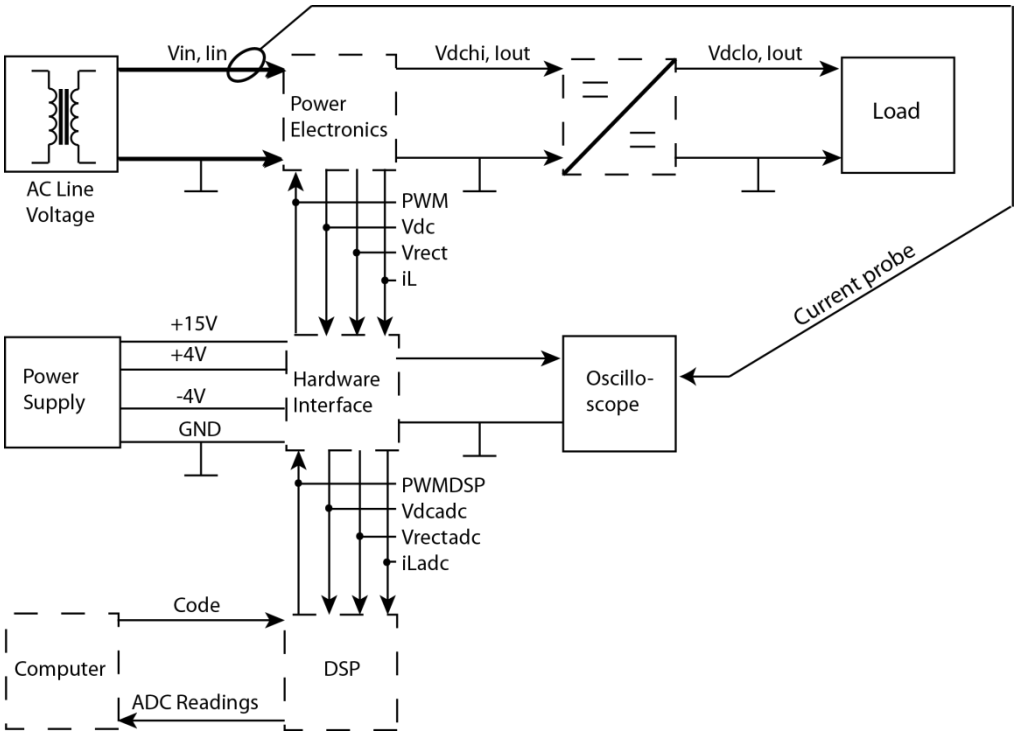

Figure 44 Test set-up block diagram

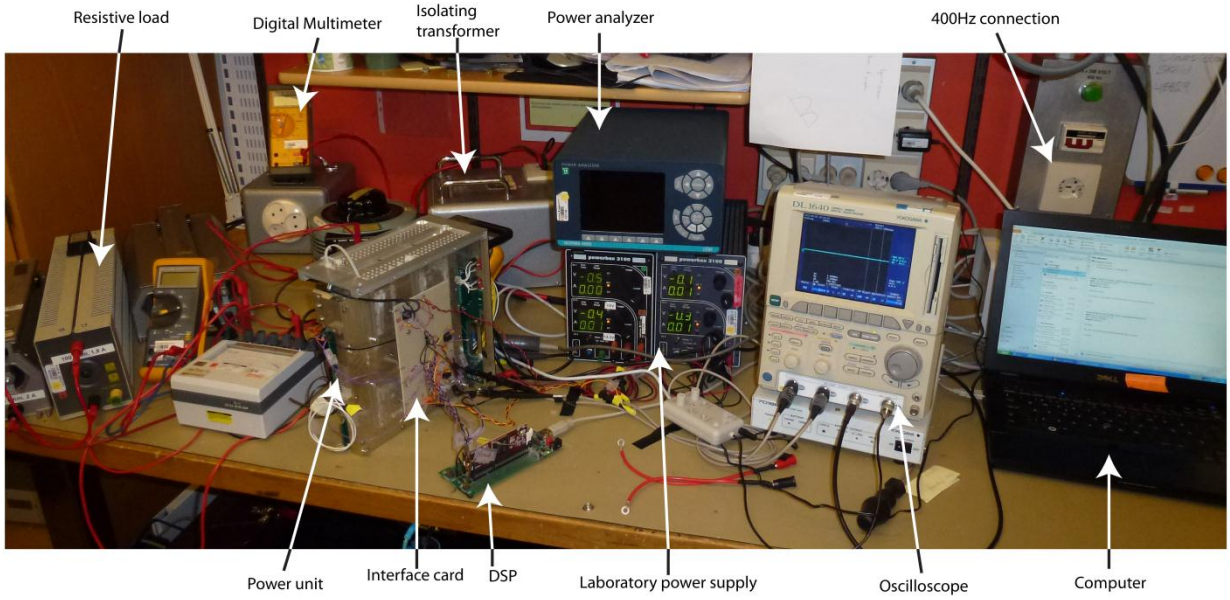

Figure 45 The actual set-up

4.3.1. Test of system at 50 Hz and 115 Volts

The system was operated for a case when the module would be assumed to be y-connected to the three-phase system. The control parameters were calculated using the equations in 2.3.1 and the cut-off frequency was set to 8kHz for the current controller and 20Hz for the voltage controller. The system was run at 190 Volts output voltage and about 200 Watts of output power. The switching frequency was set to 160kHz for convenience between testing.

The before case can be seen in figure 46 when the system only works as an ordinary rectifier. The output power at this point was 211 W and measured output voltage was 176 Volts. The top trace is the output voltage; middle trace is the rectified voltage[9]; and bottom trace is the input current measured via the current probe. Evidently, the input current is heavily distorted and the THD is 78% and the PF is 0.7584

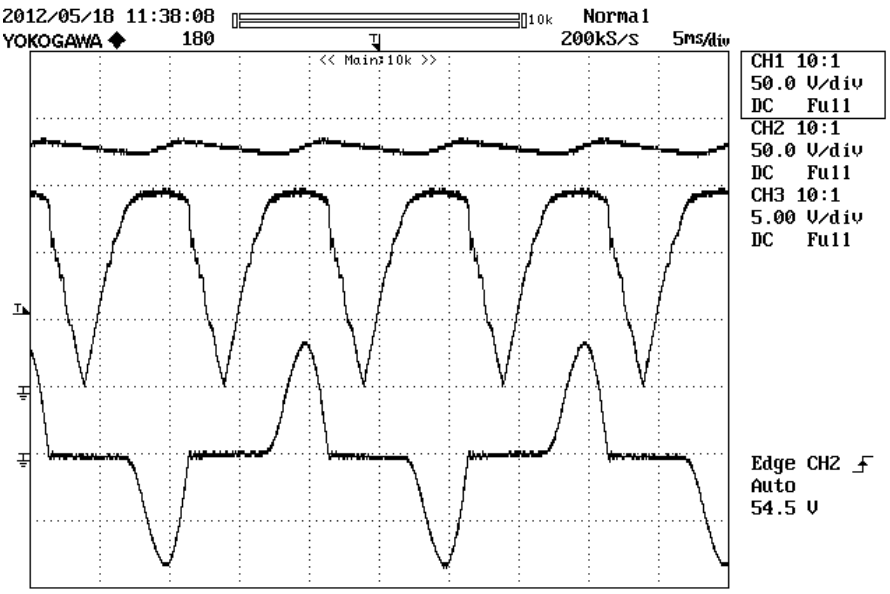

Figure 46 Waveforms at 50 Hz, 115 Volts without PFC

Then, the PFC-control algorithm was activated and the output voltage was controlled to 193 Volts DC and the output power was increased to 308 W. The results can be seen below in figure 47 where the top trace is again the output voltage, middle trace is the rectified voltage and bottom trace is the input current. The controller acts to shape the current after the input voltage and the distortion is drastically reduced. The power analyzer calculated the THD to 4.15% and the power factor as 0.9987. It should be noted that the voltage itself had a distortion of approximately 2%

[9] The non-sinusoidal appearance of the rectified voltage is likely due to the presence of capacitors by the rectifier. Also, a small duty cycle of about 20% was applied here to discharge these capacitors.

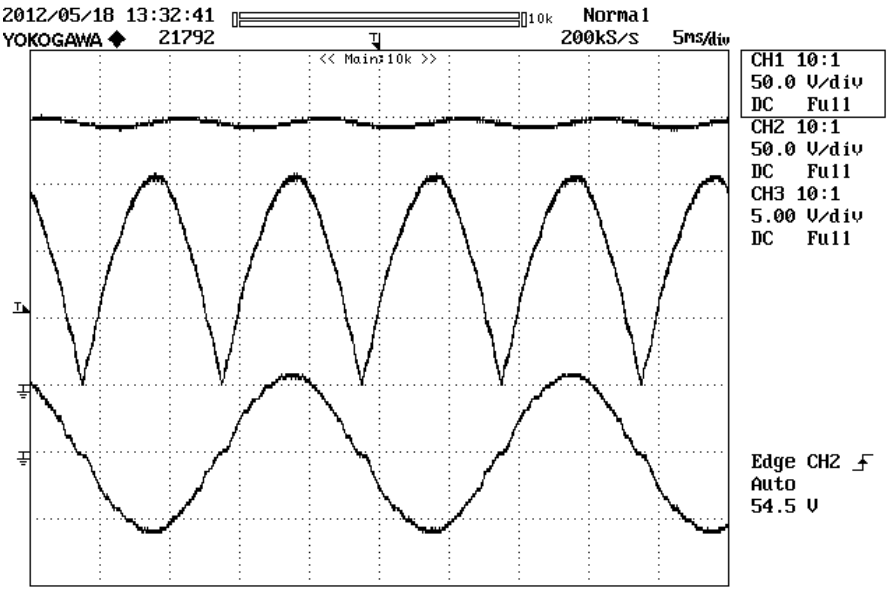

Figure 47 Waveforms at 50 Hz and 115 Volts with PFC

The THD and Power Factor were drastically improved by using this algorithm and the THD was different depending on the loading condition. In table 4 the results for THD and PF was observed for different loading of the converter and it is evident that THD and PF were improved the higher the loading became.

Table 2 THD and PF for 50 Hz and 115 Volts at different output power

Output Power [W]	THD [%]	PF
155	6.25	0.995
197	5.41	0.9967
231	4.80	0.9976
270	4.44	0.9982
308	4.15	0.9987

By having a cut-off frequency of 20 Hz the voltage control system was extremely slow to react on changes in load and reference. Therefore, an increase in cut-off frequency to 100 Hz was tested and this caused the voltage control to be much faster. The THD and Power Factor were compared for a couple of loadings to see if the first line harmonic of the output voltage would modulate the current, the results where that the THD and Power Factor were not deteriorated at all; instead, they were improved.

Table 3 THD and PF with changed control parameters for the voltage controller

Output Power [W]	THD [%]	PF
197	5.32	0.9966
270	4.42	0.9966

In figures 48 and 49, the spectrum, saved from the oscilloscope, of the two cases above can be seen. Evidently, the harmonics are much higher for the case without power factor correction, figure 48, than for the case with power factor correction figure 49. The “A” to the right in figures 48 and 49 indicate the 0dB line of the FFT.

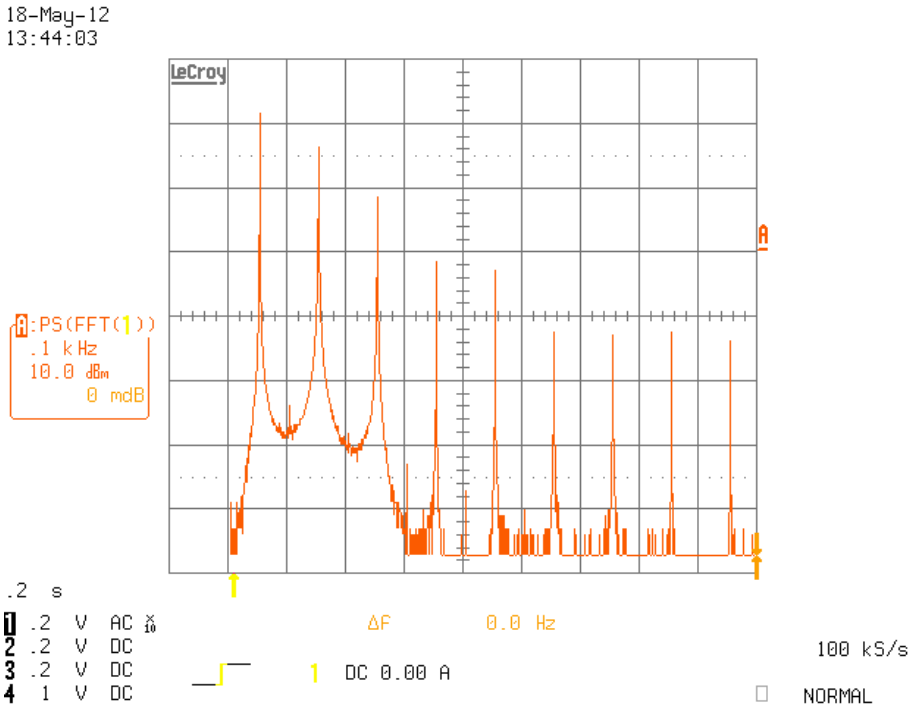

Figure 48 Spectrum of the case where no PFC is performed

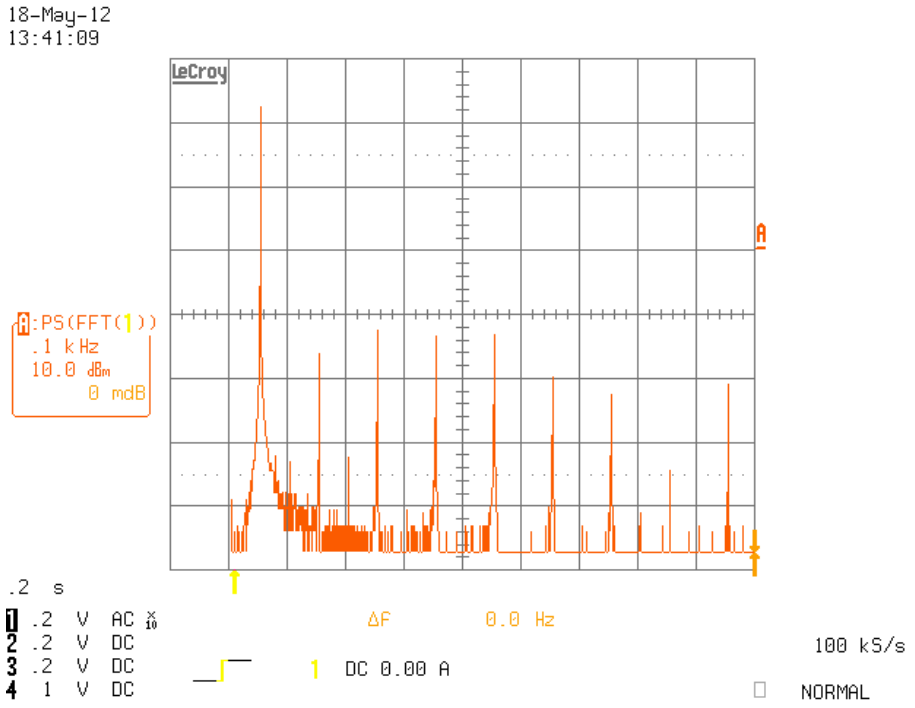

Figure 49 Spectrum of the case where PFC is activated.

The output voltage ripple was examined for the case with 115 Volts voltage, and at an output power of 187 W, as seen in figure 50. The peak-to-peak ripple is about 4.4 Volts for this case;

theoretically, using (2.18), the output voltage ripple at this loading and line frequency should be 4.8Volts. Thus, the two values coincide quite well; however, the output capacitors have a tolerance of 20% and the input voltage frequency is not constant at 50 Hz as the feeding line voltage is not perfect. Also, the theoretical equation surely does not take ESR of the capacitor into account and that may be a reason for discrepancies.

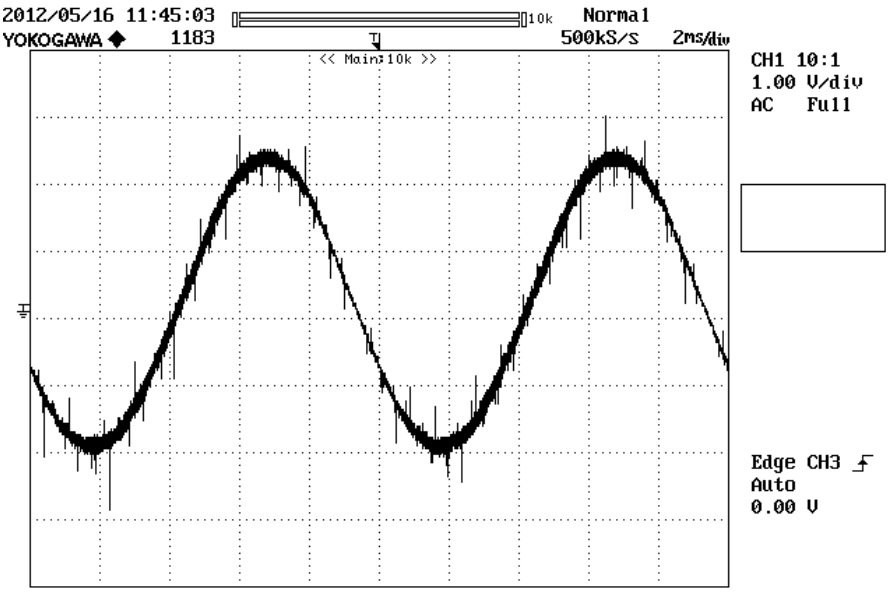

Figure 50 Output voltage ripple at 115 Volts 50 Hz and an output power of 187 W

4.3.1.Test of system at 50 Hz and 200 Volts

Another test was set-up where the feeding voltage was changed to 200 Volts which would simulate the event when the module is delta-connected to the feeding line voltage. At first the same cut-off frequency for the current controller was kept as for the previous case and it showed to deteriorate the THD to 7.96% for 367 W and 6.52% for 466 W so the cut-off frequency was changed to 16 kHz.

The before case can be seen below in figure 51 where the top trace is output voltage, middle trace is the rectified voltage and the bottom trace is input current. The output voltage is 314 Volts dc and the output power is 470 W. The THD of the input current is 81% and the power factor is 0.75.

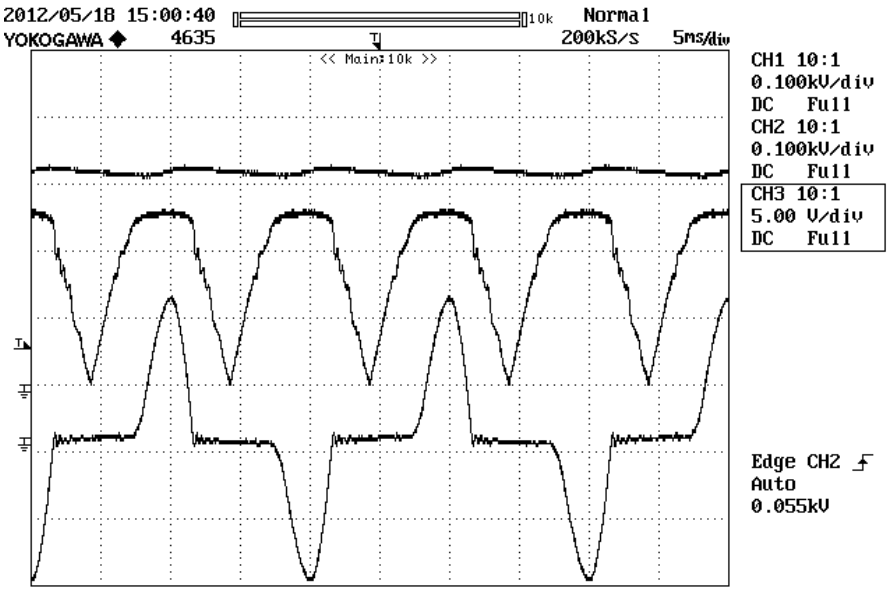

Figure 51 Waveforms for 50 Hz and 200 Volts feeding voltage before PFC.

The PFC –algorithm was operated with the new cut-off frequency and the results can be seen in figure 52. The voltage is controlled to 330 Volts and the output power is 473 W. The distortion for the below waveform is 4.9% and the power factor is 0.9972. For another case where the output power was 367 W the THD was 5.6%. Thus, again, the THD is improved the higher the output power becomes as previously observed.

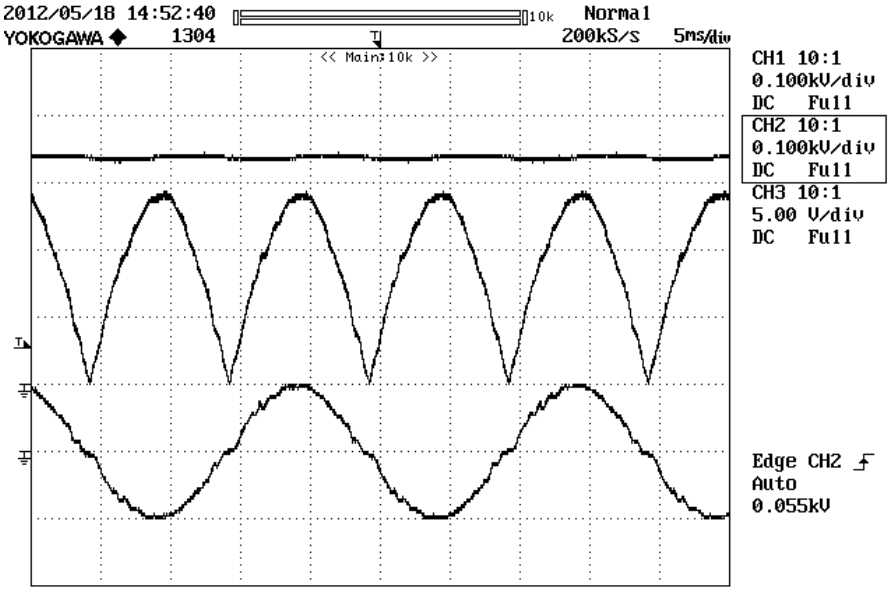

Figure 52 Waveforms at 200 Volts 500 Hz and output power of 473 Watts with PFC

4.3.2. Test of system at 400 Hz and 200 Volts.

Another set of tests were performed with a voltage of 200 Volts at 400 Hz feeding frequency. The current was set to be controlled for different cut-off frequencies in the current controller. The uncompensated case can be seen in figure 53. No power analyzer was available in this case as this device was needed for more urgent matters in the laboratory. However, top trace is the output voltage, the middle trace is the rectified voltage and the bottom trace is the input

current. As can be seen, the input current is severely distorted and has an oscillation of about 3.5 kHz on the flanks. The origin of this oscillation is unknown but it could come from the filter. The output power in this case was approximately 350 Watts.

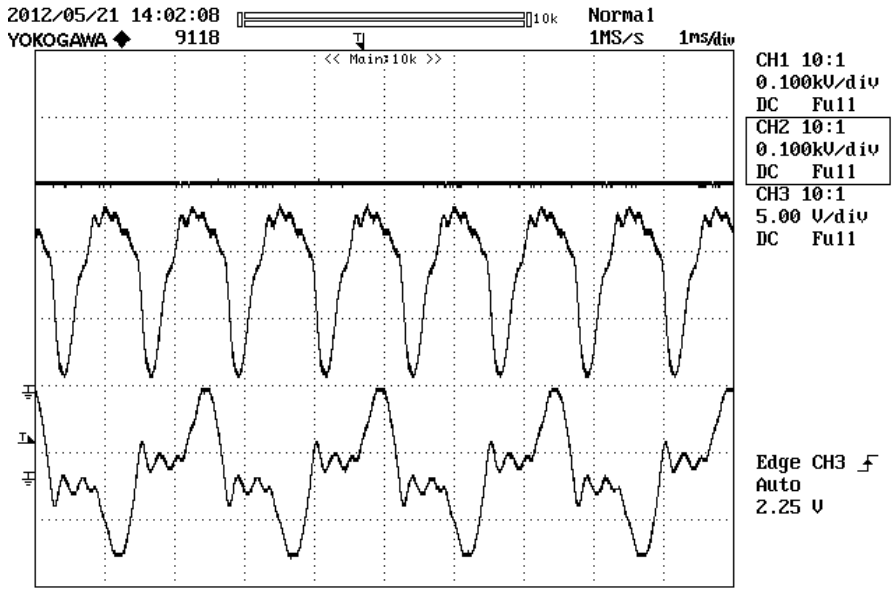

Figure 53 Waveforms at 400 Hz without PFC

The current was examined with different cut-off frequencies of the current control system: 16 kHz, 24 kHz and 32 kHz. The case of the 16kHz cut-off frequency can be seen in figure 54. The distortion of the current has been significantly decreased but there is some unwanted phase displacement between the two waveforms. The output power at this point was 360 Watts and output voltage was 300 Volts.

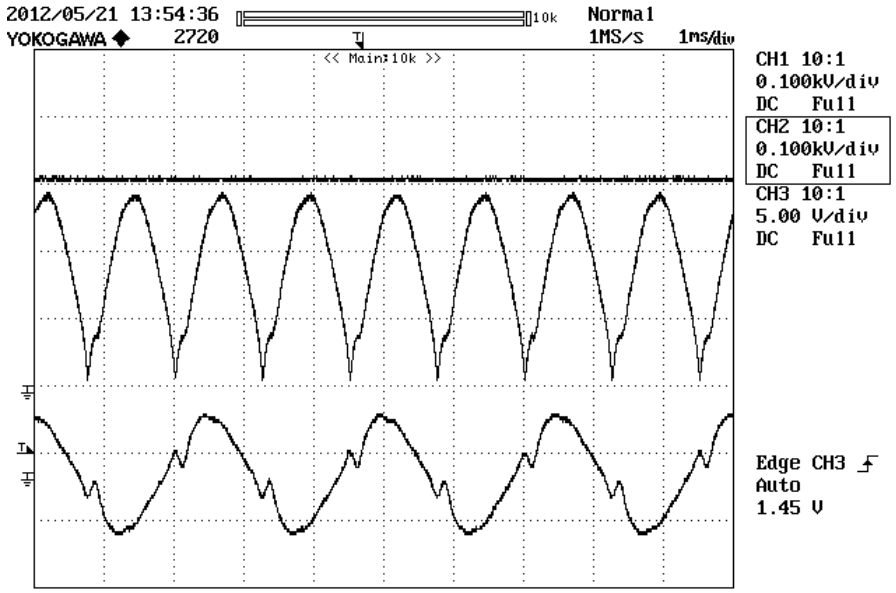

Figure 54 Waveforms at 400 Hz with PFC and fci =16kHz

Another attempt was made at 24kHz cut-off frequency and the output voltage was kept to 303.7 Volts and the power was still 360 Watts. The results can be seen below in figure 55 and

the shape of the input current has become slightly more sinusoidal in appearance but the unwanted phase displacement persists.

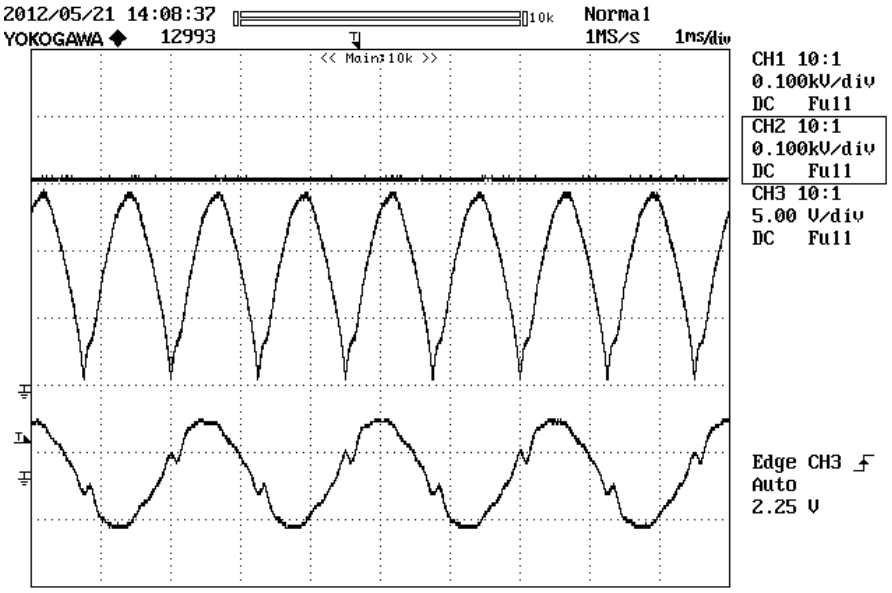

Figure 55 Waveforms at 400 Hz with PFC and fci = 24kHz

The last attempt was to change the cut-off frequency to 32kHz and with the same output voltage and output power magnitudes as before. The results for this try can be seen below in figure 56. At this point stability issues appeared in the current controller and the current flickered. The phase displacement is still present.

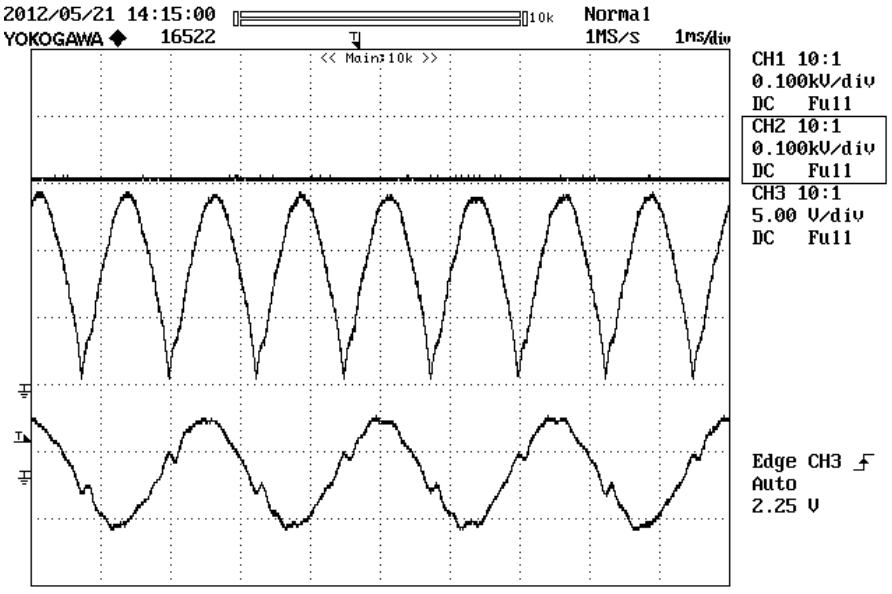

Figure 56 Waveforms at 400Hz with PFC and fci=32kHz

Even though the current is more distorted for the 400Hz case than for the 50 Hz case the change in harmonic content compared to the uncompensated case is significant. The spectrum for the before and after case (with cut-off frequency 24kHz) can be viewed in figures 57 and 58. The “A” to the right in figures 57 and 58 indicate where the 0 dB line is. In the case

without PFC there is only a difference of approximately 3 dB between the fundamental and the 3rd harmonic while the difference is approximately 30 dB for the case with PFC. Thus, the PFC-algorithm does reduce the distortion of the system significantly.

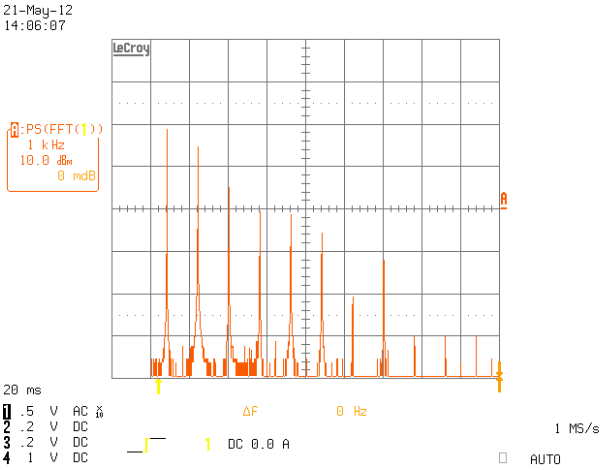

Figure 57 Spectrum without PFC

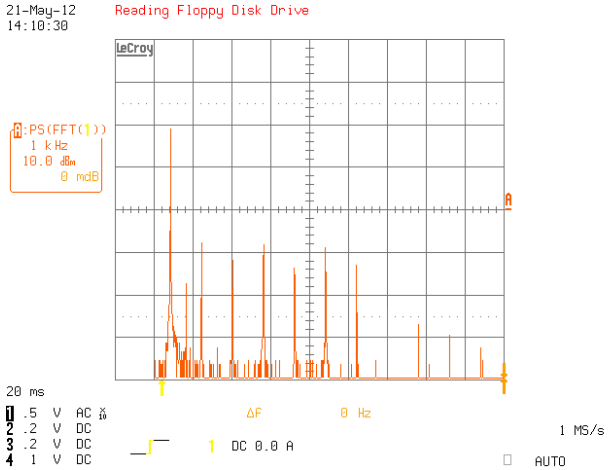

Figure 58 Spectrum with PFC

Another set of tests were performed with a power analyzer available and the results for the case when the cut-off frequency was set to 24 kHz can be seen in figure 59. The converter was run with an output voltage of 303 Volts and an output power of 360 W. The THD of the current for this waveform is 7.3% and the power factor was 0.95. This was a significant improvement from the THD of 70.2% and PF of 0.79 of the diode bridge rectifier. In these tests it should be noted that the measured THD of the input voltage was between 2-3% and was changing over time as the same voltage was utilized elsewhere in the laboratory.

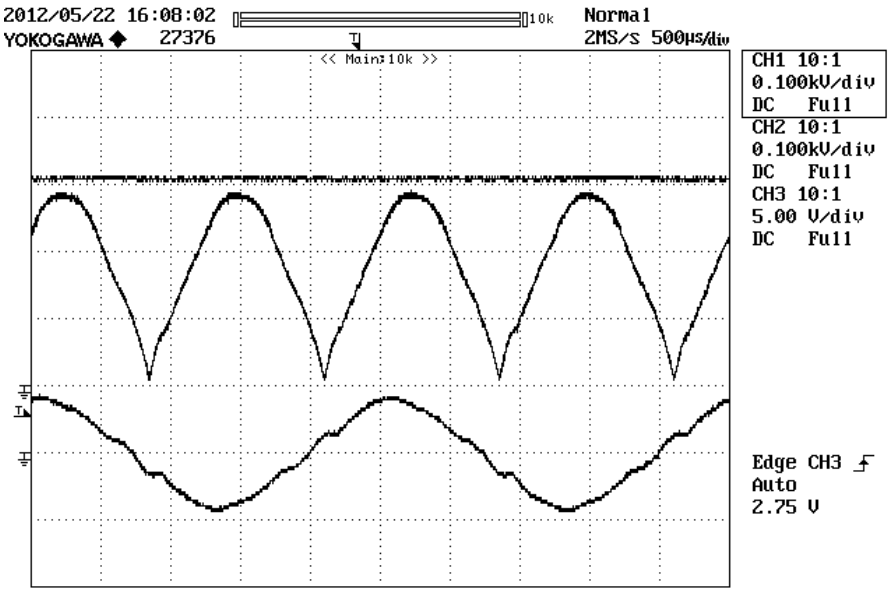

Figure 59 Waveforms at 400 Hz with PFC and fci = 24kHz

The reason for the phase displacement is likely related to the input filter which consists of inductors and capacitors. As the line frequency increases the impedance of this filter changes and as such draws more reactive power from the grid. If the output active power is more or

less the same, due to the output dc voltage and resistive load, this will lead to a phase shift in current and voltage. The reactive power of this circuit, with the same feeding voltage, was measured to be -37.4 VAr for the 50 Hz case and -118 VAr for the 400 Hz case while the output power was 473W and 360W respectively. These changes in reactive can be traced to the capacitor (approximately 1 uF) in the input filter. Consequently, these changes in reactive power will deteriorate the PF as seen in (2.3).

The input filter was bypassed to see how this would affect the power factor of the input current and the results may be viewed in figure 60. Now, the ripple from the switching is not filtered and the current affects the input voltage. However, the power factor was increased significantly to 0.998 showing that the cause of deterioration in power factor likely was the impedance of the input filter.

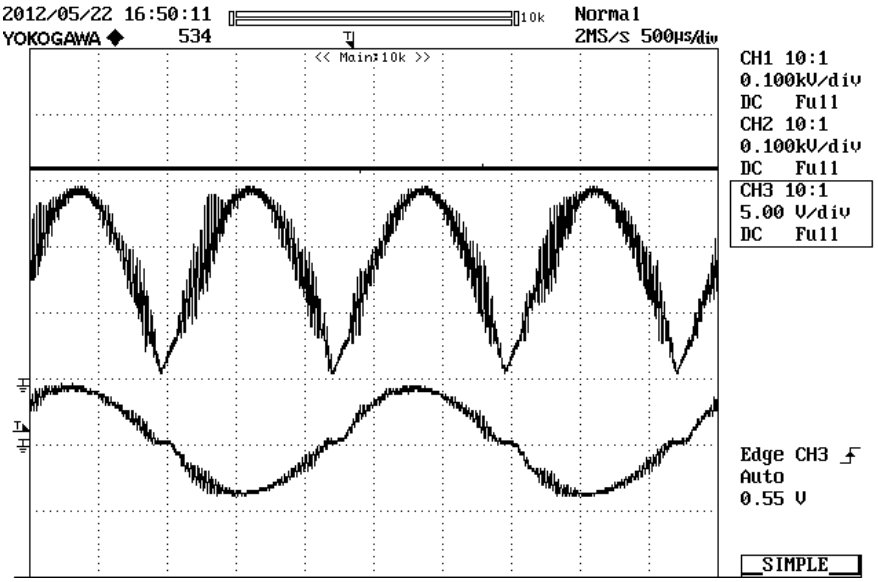

Figure 60 Input current without filter at 400 Hz

4.3.3. Computation time of processor

In figure 61 the computation times of the processor can be viewed. The top trace is the PWM-pulses while the DSP is working under a low voltage and low power test. The bottom trace is the output of one I/O-pin which is high during the time when the DSP is performing calculations. The ADC is triggered by the PWM so the time between the start of the PWM-pulse and the beginning of the lower pulse is the time required for sampling the signals used for the PFC-routine. The computation time was calculated and it was shown that it was only performing calculations for 48% of the available time. Thus, there is significant remaining capacity in the DSP. Also, it should be noted that the code used for the PFC-algorithm is very unoptimized and it could be made much more efficient by, for example, converting the C++ code to assembler.

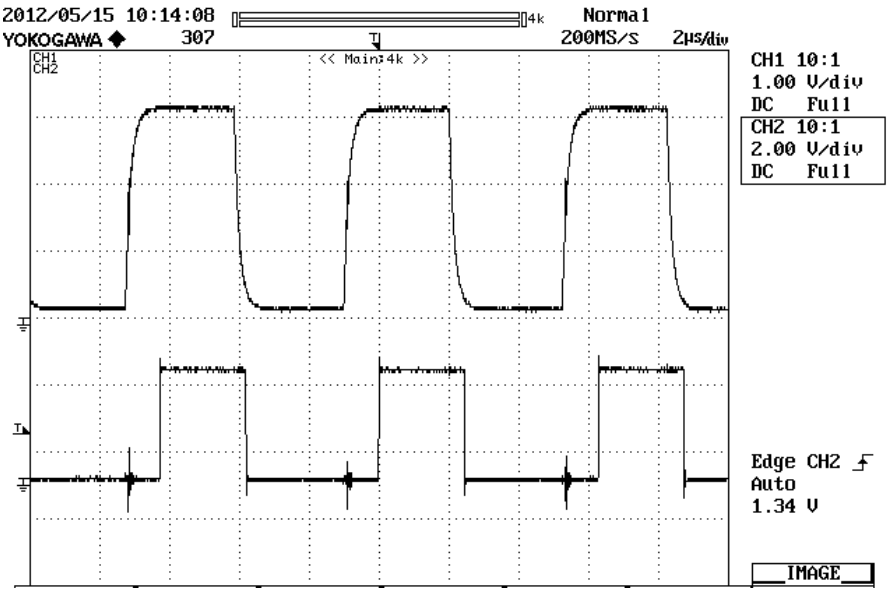

Figure 61 PWM pulses and the computation time of the DSP

4.4. **Summary and analysis**

The practical part was initiated to test the potential of using a digital control scheme for Power Factor Correction. Some work had to be done to build the finished system which included modifications of the power unit, construction of a relatively simple signal conditioning card, developing a suitable control scheme using the digital controller, setting up a test environment and performing tests and analyzing the results.

Practical information regarding digital control of PFC-circuits is very limited and the information available regarding the control of these systems regarding airborne systems is near inexistent. Most information is focused on the analog solutions traditionally used. Therefore, the process leading up to this point has been of both an investigative and an innovative nature. Moreover, the information regarding digital control of PFC-circuits has probably been directed to meet standards which are much less strict than those used in airborne systems.

The current control worked very well for the 50Hz case where a THD of 4-8% and Power Factor of above 0.99 were achieved under varying conditions. The THD was shown to improve when the output power was increased. A theory is that the ripple current amplitude is less prominent under these conditions; thus the quota in (2.2) becomes smaller which decrease the THD of the system. On a side note, it was observed that the circuit had an efficiency of roughly 94% even though the switching frequency was 160kHz.

For the 400 Hz case an improvement in THD was achieved when using the PFC-control, even though there were still problems with phase displacement, as the amplitude of the harmonics was decreased significantly. It should be noted that the Power Electronics which was used as a test bed had originally been developed for 50 Hz and as such this affects the results of the 400 Hz case. The THD of the current at 360 Watts output power was 7.3% and the Power

factor 0.95. It was also noticed that the input filter influenced the power factor of the input current quite significantly and by removing it he PF was improved to 0.998. One note, it could be that the THD is not taken into account when calculating the PF and maybe the results are somewhat misleading.

Regarding the voltage control of the converter there are uncertainties in this area. The model developed by Ridley (1989) seems correct and is referred to, for example, by Choudhury (2005). The compensation for the voltage model was chosen with this result in mind. However, there is a factor "k" which is a scaling constant in Ridleys (1989) model – perhaps representing voltage divider of the rectified voltage- and there are uncertainties of how to choose this constant as the values in the control system are already corrected for in the processor and as such this value can take on the values 1 or, perhaps, the average value of the feed forward voltage squared. In the 50 Hz case, when setting k equal to 1, and having a cut-off frequency of 20 Hz the system was unbearably slow. However, in the scenario for 100 Hz in the 400 Hz system the voltage control was noticeably improved.

Regarding the calculation time of the processor it is evident that there are room for more computations, or increasing the switching frequency, since only 48% of the available capacity of the processor is used. It should be noted that the code has room for improvements and could be made more efficient. There is certainly a possibility that this method could be used to control a three-phase modular PFC-system and, maybe, downstream DC/DC converters plus auxiliary functions.

5. Conclusion

This project was focused on power factor correction in airborne applications which means that the circumstances of operation is different than for terrestrial applications; for example, feeding line frequency (360-800Hz), demands on THD (<5%) and PF (>0.99), feeding voltages etc. This thesis was also originally meant to deal with the subject of having three-phase power factor correction. However, there was a conscious decision to focus on single phase PFC due to knowledge and time constraints and only mention three-phase briefly. Simulations, design and testing were performed to evaluate the concept of power factor correction.

The simplified simulation model of the boost PFC-current stage – which had ideal supply voltage, near ideal current reference and a simplified model of the input filter –was simulated to show a THD of 3%, 5% and above 10% for 50Hz, 400 Hz and 800 Hz respectively. These results are very hard to compare to measurements straight up because of the very ideal conditions in which they were simulated, but theory and actual measurements indicate that the model has a fair degree of validity. Improvements to the model would be to use actual data of the grid voltage to further improve the model. Other than simulating the circuit the work with this model and the simulation results held the great benefit of increased understanding of involved parties.

A prototype test system was set-up using the PFC of an existing power supply unit which was modified so that the PFC-part of the power unit was kept and the subsequent buck converter was bypassed. For the 50 Hz case the THD of the input current was taken as low as 4-8%, with THD improving at higher power levels, and the power factor was increased to above 0.99. Similar results were achieved for the 400 Hz case where the THD of the current was taken down to 7.3 % and a PF of 0.95. It should be noted that the set-up which was being used was originally intended for 50 Hz. The role of the input filter was shown to affect the deterioration in PF as this component consumes more reactive power at higher frequencies. The removal of the filer showed that the PF was improved to 0.998 for the 400 Hz case; thus, confirming the theory. Apart from this another conclusion is that the distortion of the voltage will affect the distortion of the input current and deteriorate THD and PF.

It can be concluded that the control scheme being used in this thesis has significant potential to perform power factor correction in continuous conduction mode to very good levels in both THD and PF. This control scheme was developed under guidance of some resources, Choudhury (2005) and Skanda (2007), where the main objective likely has been to comply with standards on input current distortion which are much less strict. There is certainly room for improvements in the controller such as implementing another control structure where a PID-controller could be used for further improvements in controller response, try other discretization techniques of the controllers, making the code more efficient, implement a way to either measure or calculate the average inductor current etc.

The work on the single phase module has continuously been performed with a three-phase implementation in mind. This is the reason why both 115 Volts and 200 Volts feeding voltage have been examined as these are the two alternatives in an airborne system. Even though it is

hard to conclude, without designing and testing, it is a feasible prospect to be able to couple three modules in a delta-connection and use a single DSP to control them. However, this must be designed, tested and verified to be absolutely certain.

6. Future work

There is room for improvement of the controller of this circuit and a more advanced model could be extruded of the current stage. In his work, Sun (2003) holds some points on control which could be examined. Other than that, different discretization techniques of the controllers could be studied with performance in mind. The sample/hold method, mentioned earlier, on the control voltage could be tested to see if this brings any special benefits. Implementation of average inductor current sampling/calculation could also improve THD. Also, the voltage control is suboptimal and as such the model could be revised and a more suitable scheme could be implemented in this.

The hardware used in this project had little room for improvements but there could be things to be made. THD could be reduced by adjusting the inductor value of the boost inductor to a more suitable level. There was also during the course of the project an idea to exchange the diode of the boost converter to a Silicon Carbide diode to reduce the losses in the switching MOSFET.

There are certain single phase modules on the market, Emerson (2010), which claims to be able to reduce the THD of the input current to levels below 10% for different input frequency intervals such as 50-60 Hz and 360-800 Hz. These modules could be used in a delta-connected modular three-phase application to see what potential this set-up has.

According to Louganski and Lai (2007) the standard analog controller is not suitable for PFC in the frequency interval 360-800 Hz but in their work there are suggestions on how to improve the performance of such a circuit. This could be of interest in the future to examine

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8. Appendix

A. Control code

*********The MAIN file***************

```
#include "DSP28x_Project.h"     // Device Headerfile and Examples Include
File
#include "DSP2833x_EPwm_defines.h"    // useful defines for initialization
#include "Dlog4CH.h"
#include "ADCSettings.h"
#include "PWM_config.h"

interrupt void MainISR();

// Declare your function prototypes here
//-----------------------------------------------------------------

void InitAdc();
void InitSysCtrl();
void InitPieVectTable();

struct Converter_PWM Pwm_config=INVERTER_PWM_DEFAULT;

// General System nets - Useful for debug
Uint16 i,j,/*DutyFine,update,*/ n;
//int16 PWM1,PWM2,PWM3 ;
Uint32 temp;
//float Duty, voltage;

DLOG_4CH dlog = DLOG_4CH_DEFAULTS;
int16 DlogCh1=0;
int16 DlogCh2=0;
int16 DlogCh3=0;
int16 DlogCh4=0;

Uint16 update;
Uint16 PWM1=937.5;
Uint16 PWM2=750;
Uint16 PWM3=1000;

//ADC & Conversion Parameters
float Duty=0.5;
float DutyFine=300;
float VdcADC=0;
float VrectADC=0;
float Vdc=0;
float Vrect=0;
float CurrentADC=0;
float IL=0;
float Vin=0;
//float Vdc=0;
int16 start = 0;
//Slow loop Parameters
Uint16 N_avgcalc = 0;
float Vavg = 0;
Uint16 perform_calc = 0;
float f_line = 0;
```

```
float Vrectified_avgcalc =0;
Uint16 N = 1;
Uint16 K = 0;


// Controller parameters
float Kvp = 0.001; //Proportional voltage compensator constant
float Kvi = 0.1339; //Integrator voltage compensator constant
float Kip = 0.266; //Proportional current compensator constant
float Kii = 355; //Integrator voltage compensator constant
float Tsw = 0.00000625;
Uint16 Vref =15;
float e_v = 0;
float e_v_nminus1 = 0;
float e_i = 0;
float e_i_nminus1 = 0;
float i_amplitude = 0;

float Igain=0.00001;
float Duty_openloop = 0.2;

float vcontrol = 0;
float vcontrol_nminus1 = 0;
float iref = 0;
float d = 0;
float d_nminus1 = 0;
Uint16 Counter_Compare = 0;

Uint16 R1dc=47000;
Uint16 R1=47000;
Uint16 R2dc=355;
Uint16 R2=499;

void main()
{
        InitSysCtrl();

        InitPieVectTable();//Create a table of ISR address

        EALLOW;
        PieVectTable.SEQ1INT=&MainISR;
        EDIS;

        EALLOW;
           GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0;
           GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1;
        EDIS;

        PieCtrlRegs.PIEIER1.bit.INTx1=1;//Enable the ADC interrupt in PIE
level
        IER |=M_INT1;//Enable the ADC interrupt in CPU level

        EDIS;

//      ePWM1_Config(PWM1);
        INITIAL_PWM()

        InitAdc();
        SETTING_ADC()

////////////////////////////////////////////////////////
```

```
///ADC setting has been moved into the header file as a macro
////////////////////////////////////////////////////////////////

        EINT;
        ERTM;

}

interrupt void MainISR()
{
        GpioDataRegs.GPBSET.bit.GPIO34 = 1;

        AdcRegs.ADCST.bit.INT_SEQ1_CLR=1;//clear the SEQ1

        // PFC code
        // Adc & Conversion

        VdcADC=(AdcMirror.ADCRESULT0/4096.0*3);
        VrectADC=(AdcMirror.ADCRESULT1/4096.0*3);
        CurrentADC = (AdcMirror.ADCRESULT2/4096.0*3);

        // Measurement correction
        Vdc=(400/3)*VdcADC;
        Vrect=(200*1.414213562/3)*VrectADC;
        IL=CurrentADC/0.1;


        // Slow loop counting while the voltage is above 3 volts
        // and computing new values once the voltage drops below 3 volts
        // and some other conditions are met
        if (Vrect>15) {
                N_avgcalc = N_avgcalc + 1;
                Vrectified_avgcalc = Vrectified_avgcalc+VrectADC;
                perform_calc = 0;
        }

        if ((Vrect>=0)&&(Vrect<=15)&&(perform_calc==0)&&(N_avgcalc>=20)&&
(start!=2)){
                        f_line = 1/(2*N_avgcalc*Tsw);
                        Vavg
=(200*1.414213562/3)*Vrectified_avgcalc/N_avgcalc;
                        perform_calc = 1;
                        Vrectified_avgcalc = 0;
                        N_avgcalc = 0;
                }

        if ((Vrect>=0)&&(Vrect<=15)&&(perform_calc==0)&&(N_avgcalc>=20)&&
(start==2)){
                f_line = 1/(2*N_avgcalc*Tsw);
                Vavg =(200*1.414213562/3)*Vrectified_avgcalc/N_avgcalc;
                perform_calc = 1;
                Vrectified_avgcalc = 0;
                N_avgcalc = 0;
                i_amplitude = vcontrol;
        }

        // PFC code without S/H
        if (start==1){
        // Voltage compensator: Calculating new control-value from the
errors
        // originating from the output voltage.
```

```
                e_v = Vref-Vdc;
                vcontrol = vcontrol_nminus1+Kvp*e_v+(Kvi*Tsw-
Kvp)*e_v_nminus1;

        // Current Compensator
        //iref = (i_amplitude*VrectADC*0.33);
        //iref = (i_amplitude*VrectADC*0.33)/(Vavg*Vavg);
                iref = (vcontrol*Vrect)/(Vavg*Vavg);

        // Limit the current reference from ever going
        // above 10 at any point on the curve
                if (iref >10){
                        iref = 10;
                }

                e_i = iref-IL;
                d = d_nminus1 + Kip*e_i+(Kii*Tsw-Kip)*e_i_nminus1;
        }

        // PFC code with S/H
        if (start==2){
        // Voltage compensator: Calculating new control-value from the
errors
        // originating from the output voltage.
                e_v = Vref-Vdc;
                vcontrol = vcontrol_nminus1+Kvp*e_v+(Kvi*Tsw-
Kvp)*e_v_nminus1;

        // Current Compensator
        //iref = (i_amplitude*VrectADC*0.33);
        //iref = (i_amplitude*VrectADC*0.33)/(Vavg*Vavg);
                iref = (i_amplitude*Vrect)/(Vavg*Vavg);

        // Limit the current reference from ever going
        // above 10 at any point on the curve
                if (iref >10){
                        iref = 10;
                }

                e_i = iref-IL;
                d = d_nminus1 + Kip*e_i+(Kii*Tsw-Kip)*e_i_nminus1;
        }

        // DC/DC open loop
        if (start ==3){
                d= Duty_openloop;
                vcontrol=0;
                vcontrol_nminus1=0;
        }

        // DC/DC rough closed loop.
        if (start ==4){
                e_v=Vref-Vdc;
                d= d_nminus1+Igain*e_v;
        }

        //Limit duty cycle
        if (d >0.97)
                d=0.97;
        else if (d<0)
                d=0;
```

```
        // Send d to PWM register
        Counter_Compare = d*PWM1;
        Pwm_config.dutyfine=Counter_Compare;
        PWM_config_OUTPUT(Pwm_config)

        // Save values for next ISR
        e_v_nminus1 = e_v;
        e_i_nminus1 = e_i;
        vcontrol_nminus1 = vcontrol;
        d_nminus1 = d;

        // MISCELLANEOUS CODE.
        //      d=0.5;

        //      d=d_nminus1+Igain*e_v;

        //      Counter_Compare = 0.5*PWM1;

        //  End control loop
        //      e_v_nminus1 = 0.35;
        //      e_i_nminus1 = 0.22;
        //      vcontrol_nminus1 = 2;
        //      d_nminus1 = 0.3;

        //      DutyFine=PWM1*Duty;    //EPwm1Regs.CMPA.half.CMPA =
DutyFine;
        //      DutyFine=PWM1*(voltage/3);
        //
        //      Pwm_config.dutyfine=DutyFine;
        //      PWM_config_OUTPUT(Pwm_config)

        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 0x1;
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;

        GpioDataRegs.GPBTOGGLE.bit.GPIO34 = 1;
}
```

*****The PWM settings*****

```
#ifndef Converter_PWM_H_
#define Converter_PWM_H_

#include "DSP28x_Project.h"

struct Converter_PWM
{
        float dutyfine;
        float Duty_PWM;
};

#define INVERTER_PWM_DEFAULT \
{\
        0.0,\
        0.0\
}

#define INITIAL_PWM(period)\
```

```
EALLOW;\
GpioCtrlRegs.GPAMUX1.bit.GPIO0=1;\
GpioCtrlRegs.GPAMUX1.bit.GPIO1=1;\
EDIS;\
EPwm1Regs.TBCTL.bit.CLKDIV=0;\
EPwm1Regs.TBCTL.bit.HSPCLKDIV=0;\
EPwm1Regs.TBCTL.bit.CTRMODE=0;\
EPwm1Regs.TBPRD=937.5;\
EPwm1Regs.TBPHS.half.TBPHS=0;\
EPwm1Regs.TBCTL.bit.PHSEN=0;\
EPwm1Regs.TBCTL.bit.PRDLD=0;\
EPwm1Regs.TBCTL.bit.SYNCOSEL=1;\
EPwm1Regs.CMPCTL.bit.SHDWAMODE=0;\
EPwm1Regs.CMPCTL.bit.SHDWBMODE=0;\
EPwm1Regs.CMPCTL.bit.LOADAMODE=0;\
EPwm1Regs.CMPCTL.bit.LOADBMODE=0;\
EPwm1Regs.AQCTLA.bit.CAU=1;\
EPwm1Regs.AQCTLA.bit.CAD=1;\
EPwm1Regs.AQCTLA.bit.ZRO=2;\
EPwm1Regs.DBCTL.bit.OUT_MODE=3;\
EPwm1Regs.DBCTL.bit.POLSEL=2;\
EPwm1Regs.DBCTL.bit.IN_MODE=0;\
EPwm1Regs.DBFED=0;\
EPwm1Regs.DBRED=0;\
EPwm1Regs.ETSEL.bit.SOCAEN=1;\
EPwm1Regs.ETSEL.bit.SOCASEL=1;\
EPwm1Regs.ETPS.bit.SOCAPRD=1;\
EALLOW;\
EPwm1Regs.HRCNFG.all = 0x0;\
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_REP;\
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;\
EPwm1Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;\
EDIS;

#define PWM_config_OUTPUT(p) \
               p.Duty_PWM=(p.dutyfine);\
               EPwm1Regs.CMPA.half.CMPA = p.Duty_PWM;
#endif /*INVERTER_PWM_H_*/
```

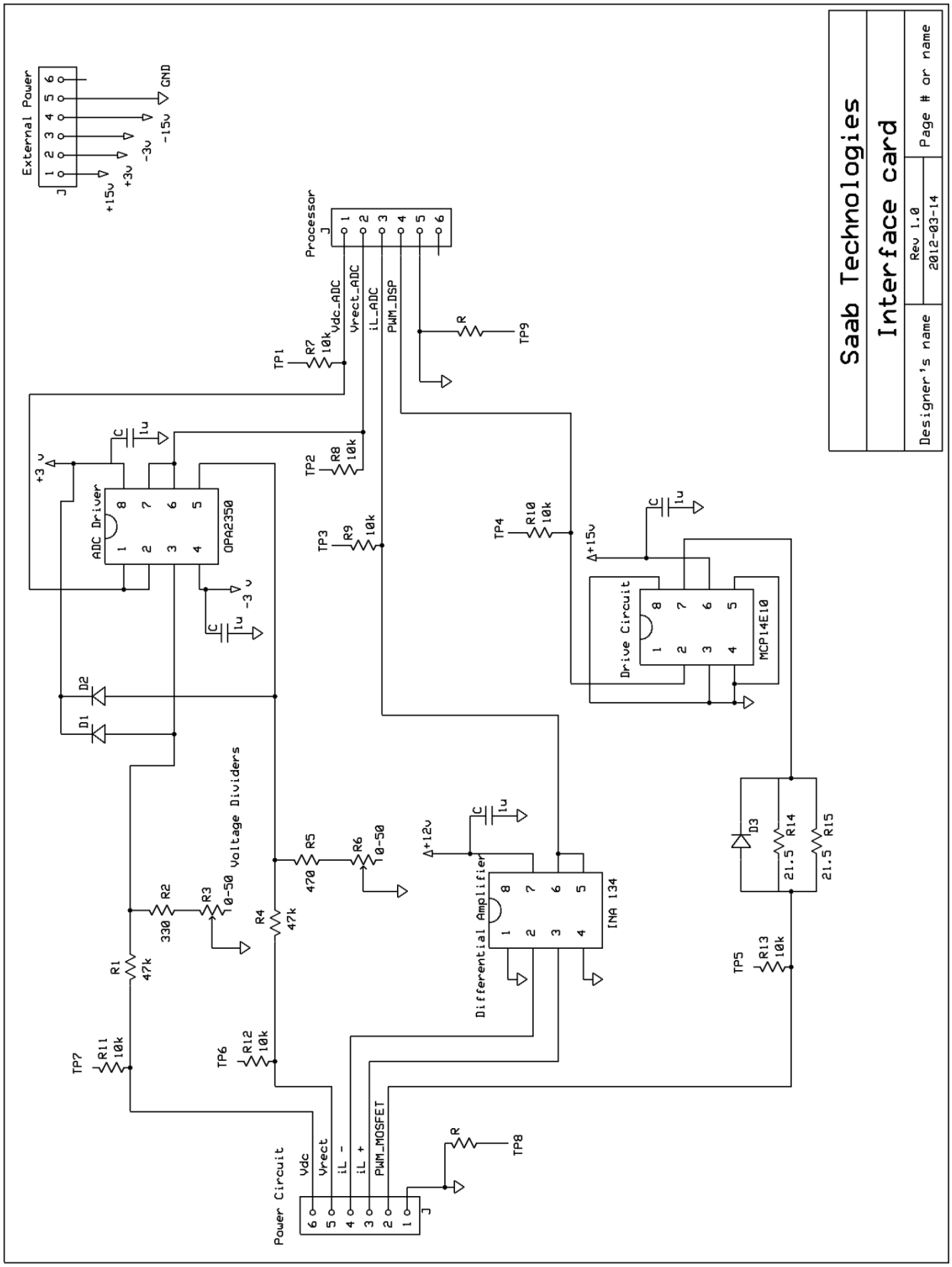
**********The ADC settings*********

```
#ifndef SETTINGADC_H_
#define SETTINGADC_H_

#define SETTING_ADC() \
       EALLOW;\
       AdcRegs.ADCTRL1.bit.ACQ_PS = 1;\
       AdcRegs.ADCTRL1.bit.CPS = 0;\
       AdcRegs.ADCTRL3.bit.ADCCLKPS =  2;\
       AdcRegs.ADCTRL1.bit.SEQ_CASC = 0;       /*0x0 Dual Sequencer Mode,
0x1 Cascaded Mode*/\
       AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1=1; /*ADC triggerred by PWM =1,
not triggered by PWM = 0*/\
       AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 0x1;       /*enable the interrupt
in cascaded mode*/\
       AdcRegs.ADCTRL3.bit.SMODE_SEL = 0x1;     /*simutanous sampling*/\
       AdcRegs.ADCTRL2.bit.RST_SEQ1 = 0x1;       /*reset the sequency*/\
```

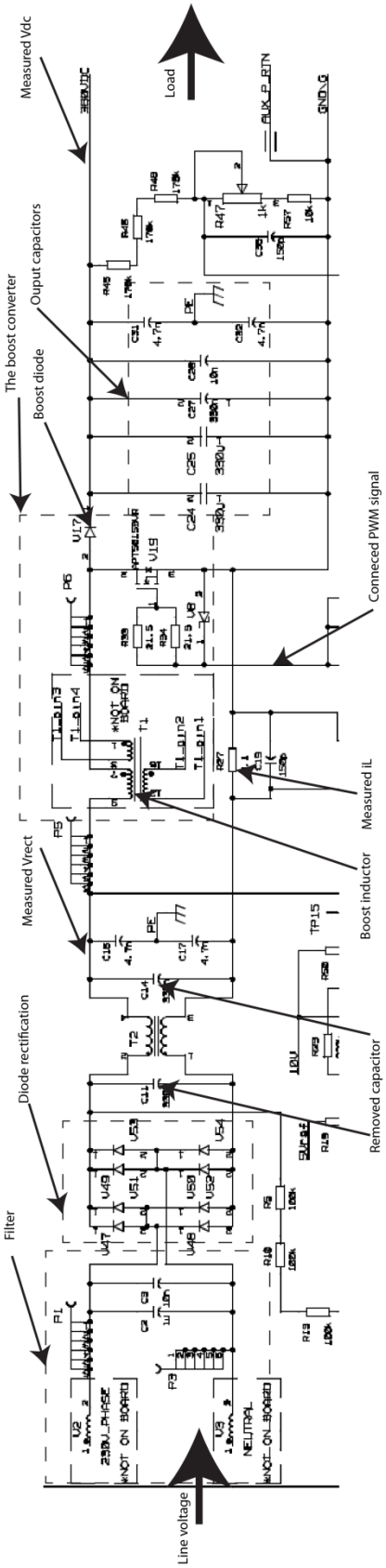
```
        AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0;  /* ChSelect: ADC A0-> Phase A
Current; ADC B0-> Phase B Current */\
        AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 1;  /*Sample the second time*/\
        AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 1;\
    EDIS;
//      AdcRegs.ADCTRL2.bit.SOC_SEQ1=1;              \


#endif /*SETTINGADC_H_*/
```

B. Circuit schematics

Interface card



Power Electronics



C. Test notes

Test notes for “4.3.1 Test of system at 50 Hz and 115 Volts”

Kvp = 0.001
Kvi = 0.266
Kip = 0.126
Kii = 1337
Vin = 115 Volt
fsw = 116 kHz

Norma 4000 använd för beräkning av effektfaktor

Innan
Lägre Last (sparad som: Innan)
Vin = 114.78 Volt rms
Iin = 2.16 A rms
Pin = 186.2 W
Sin = 248 VA
Qin = 164 VAr
Vout = 180 Volt dc
Iout = 0.95 A dc
Pout = 171 W

PF = 0.75 (ind)
THD = 82%

Högre last(sparad som: Innan2)
Vin = 114 Volt rms
Iin = 2.67 A rms
Pin = 230 W
Sin = 304 VA
Qin = 198 VAr
Vout = 176 Volt dc
Iout = 1.21 A dc
Pout = 211 W

PF = 0.7584 (ind)
THD = 78%
I1 H01 = 2.1 A

Efter
Lägre last
Vin = 114.2 Volt rms
Iin = 1.8 A rms
Pin = 204.7 W
Sin = 205.4 VA
Qin = -17.45 VAr
Vout = 189 Volt dc
Iout = 1 A dc
Pout = 189 W

PF = 0.9964 (cap)
THD = 5.5%
I1 H01 = 1.8

Högre last (sparad som: Efter)
Vin = 113.4 Volt rms
Iin = 2.18 A rms
Pin = 246.3 W
Sin = 247 VA

```
Qin = -17.45 VAr
Vout = 189.3 Volt dc
Iout = 1.21 A dc
Pout = 228.7 W

PF = 0.9975 (cap)
THD = 4.8%
I1 H01 = 2.17

Högre last (sparad som: Efter2)
Vin = 112 Volt rms
Iin = 2.97 A rms
Pin = 330 W
Sin = 331 VA
Qin = -17.2 VAr
Vout = 193 Volt dc
Iout = 1.6 A dc
Pout = 308 W

PF = 0.9987 (cap)
THD = 4.15%
I1 H01 = 2.97

Tabell wcv = 2*pi*20
Put   THD    PF
155W  6.25%  0.995 (cap)
197W  5.41%  0.9967 (cap)
231W  4.80%  0.9976 (cap)
270W  4.44%  0.9982 (cap)
308W  4.15%  0.9987 (cap)

Tabell nya parametrar wcv = 2*pi*100
Put   THD    PF
197W  5.32%  0.9966
270W  4.42%  0.9966
```

Test notes for “4.3.2 Test of system at 50 Hz and 200 Volts”

```
Vout = 333.6 Volts
Vin = 200
fci = 8kHz

Kip = 0.137
Kii = 689
Kvp = 0.0059
Kvi = 3.74

Put    Thd
367 W  7.96%
466 W  6.52%

****
fci = 16kHz
Kip = 0.266
Kii = 1337
Kvp = 0.0059
Kvi = 3.74

Put    THd
367 W  5.6%
```

```
466 W  4.9%


Efter (sparad som: Efter)
Vin = 199 Volt rms
Iin = 2.53 A rms
Pin = 500W
Sin = 502 VA
Qin = 37.4 VAr
Vout = 333.5 Volt dc
Iout = 1.42 A dc
Pout = 473.7 W

PF = 0.9972 (cap)
THD = 4.9%
I1 H01 = 2.53 A

Innan (sparad som: Innan)
Vin = 200 Volt rms
Iin = 3.37 A rms
Pin = 503W
Sin = 675 VA
Qin = 445 VAr
Vout = 314 Volt dc
Iout = 1.5 A dc
Pout = 470 W

PF = 0.75 (cap)
THD = 81%
I1 H01 = 2.53 A
```

Test notes for “4.3.2 Test of system at 50 Hz and 200 Volts”

```
Power Analyzer not available due to urgent matters at the laboratory

Vin = 200
Vout = 300

Kvp = 0.0031
Kvi = 1.95

**
Sparad som: Innan
Spektrum sparad som: Spektruminnan
Vin = 198.6
Iin = 2.35 A
Vout = 298.1
Iout = 1.2
D = 0.2

**
sparad som: Efter16kHz
Spektrum sparad som: Spektrum16kHz
fci = 16kHz
Kip = 0.3
Kii = 3015

Vin = 199.4
Iin = 2.1 A
Vout = 303.6
```

Iout = 1.2A

**
sparad som: Efter24kHz
Spektrum sparad som: Spektrum24kHz
fci = 24kHz
Kip = 0.45
Kii = 6821

Vin = 199.9 V
Iin = 2.05 A rms
Vout = 303.7 V
Iout = 1.2 A

**
sparad som: Efter32kHz
Spektrum sparad som: Spektrum32kHz
fci = 32kHz
Kip = 0.6
Kii = 12127

Vin = 199.3 V
Iin = 2.035A rms
Vout = 303.5 V
Iout = 1.2A

Second try

Innan

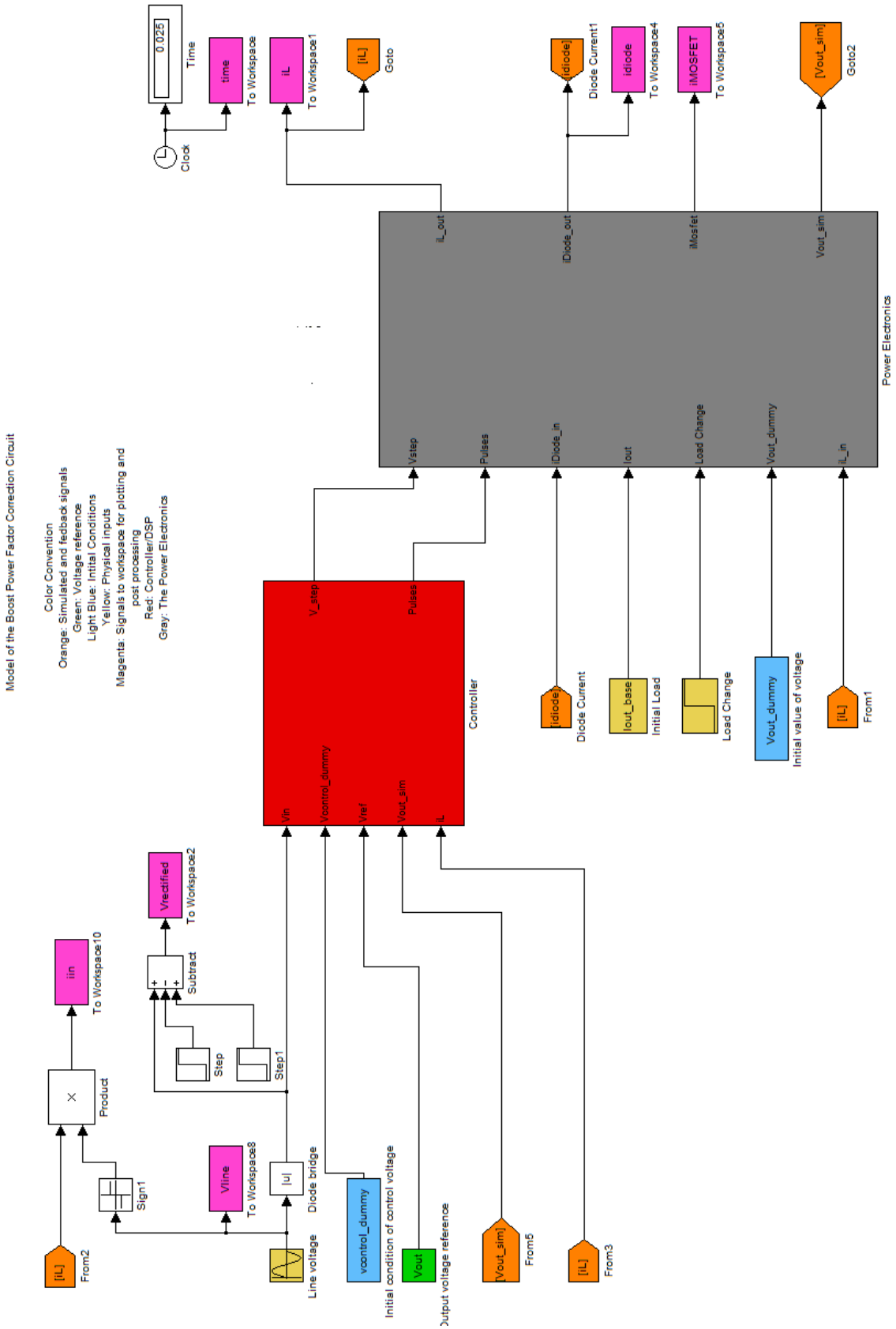
Sin = 476 VA
Qin = -290 VAr
Pin = 376
Vin = 200 Volt AC
Iin = 2.4 A
Pout = 360
Vout = 300 V
Iout = 1.2 A
PF = 0.791
THD I = 70.2%
THD U = 6%

Efter
Sparad som: Efter
Sin = 400 VA
Qin = -118 VAr
Pin = 385 W
Vin = 198.6 Volt AC
Iin = 2.03 A
Pout = 260 W
Vout = 303 V
Iout = 1.2 A
PF = 0.95 cap
THD I = 7.3%
THD U = 2-3%

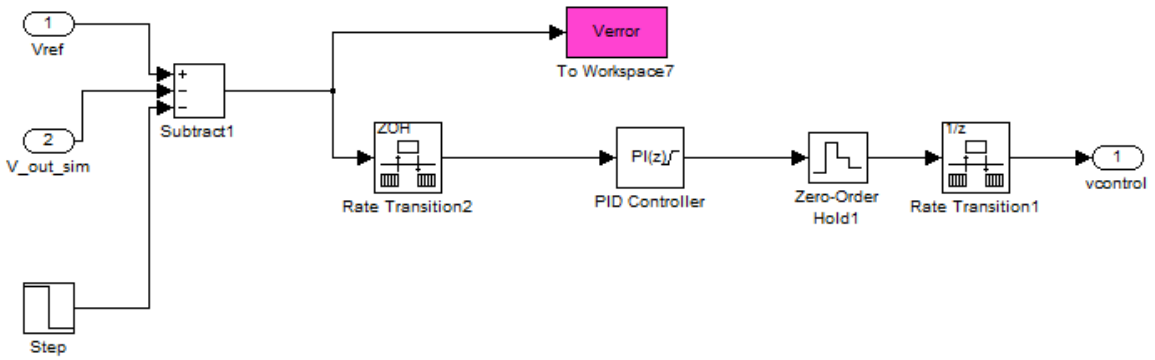
Efter borttagning av kondensator
PF = 0.998
Inspänning distorterad utan in-filter

D. Simulation model

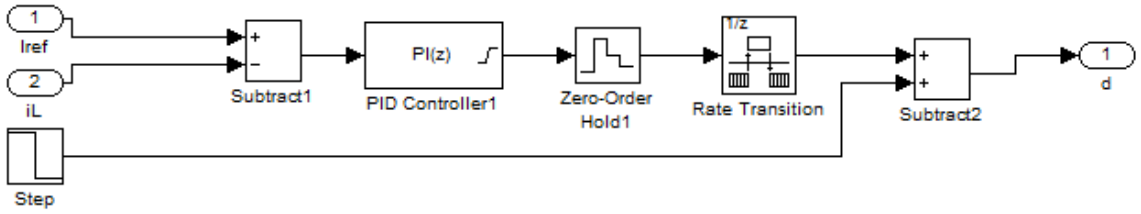
Whole simulation model



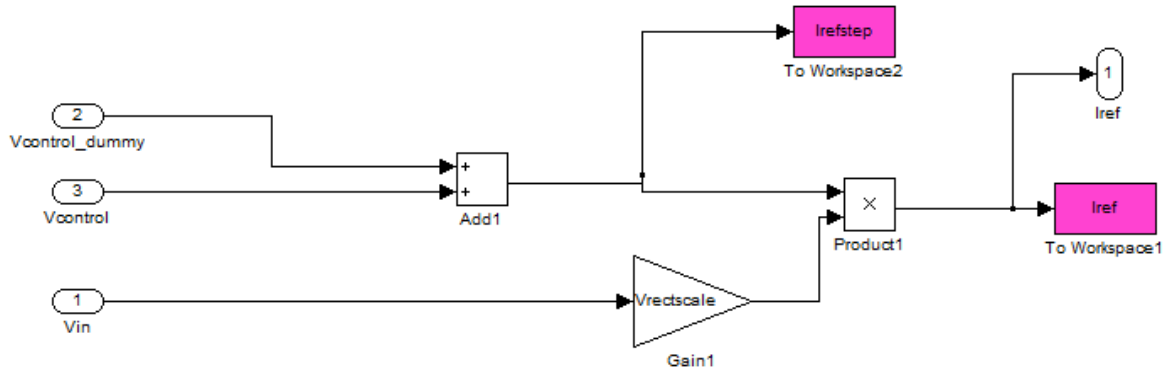
Voltage controller model



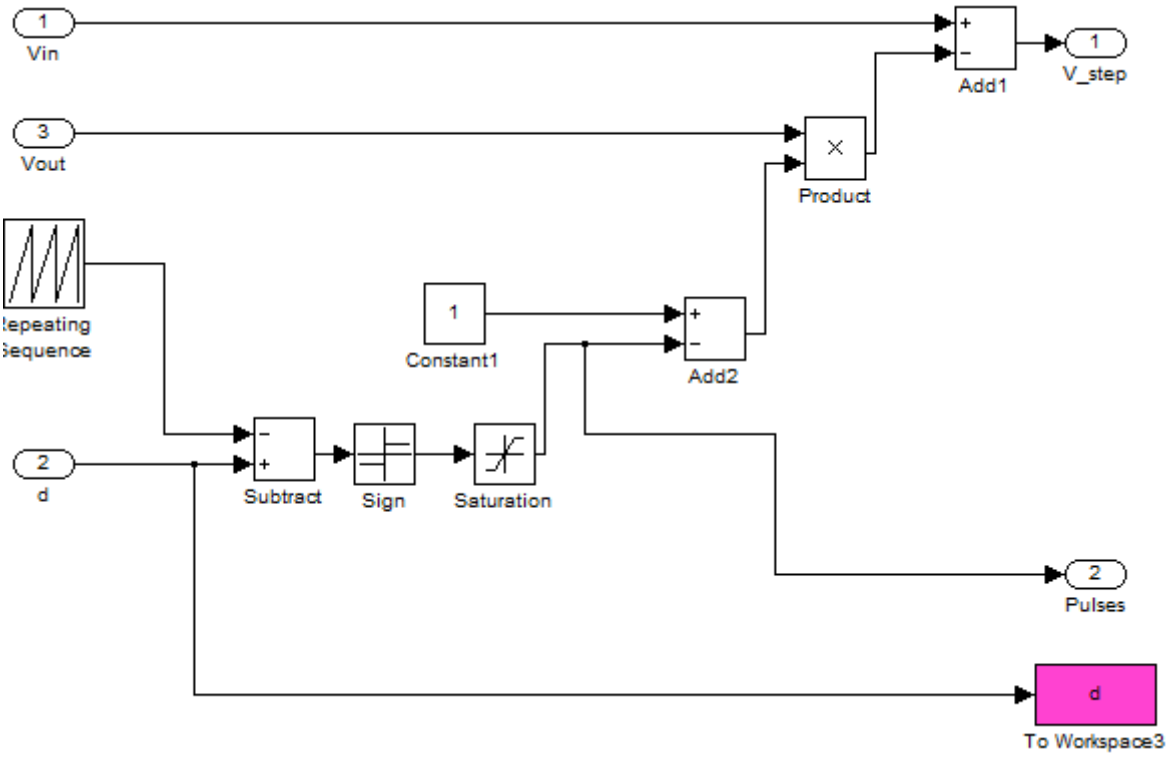
Current controller



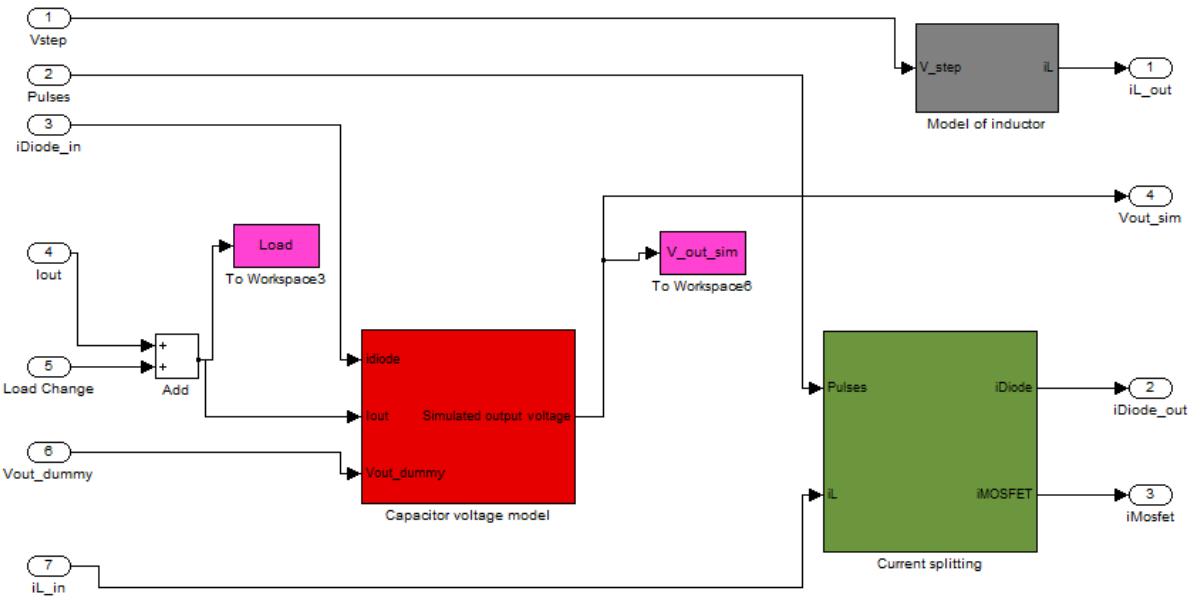
Current reference calculation



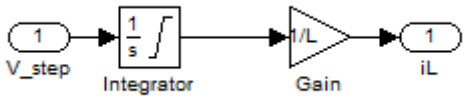
"PWM module"



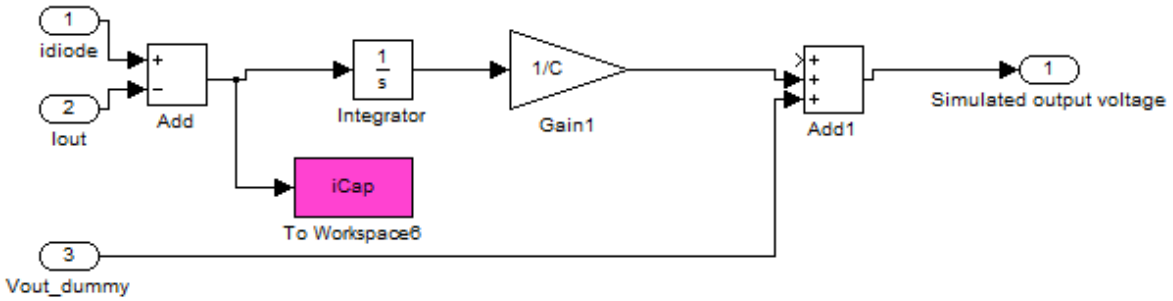
Model of Power Electronics



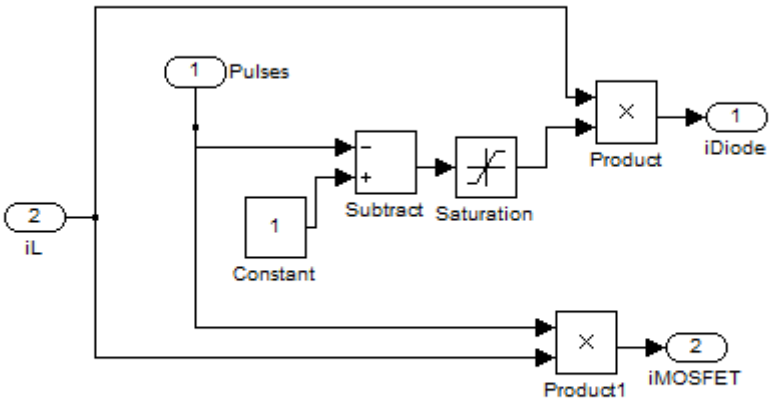
Model of inductor



Capacitor voltage model



“current splitting”



*************Model Main file*******************

```
clear all; clc; close all;
%% Parameters
% Variables related to the input and output voltage
V_amp = 115*sqrt(2);              % Input Voltage amplitude
V_freq = 2*pi*400;                % Input Voltage frquency in rad/s
Vrectscale = 1/V_amp;             % Scaling factor for the multiplier
Vout= 450;                        % Reference for the output voltage
Vout_dummy =450;                  % "Initial condition" for the output voltage
vcontrol_dummy = 3;               % "Initial condition" for the control voltage - 6.5 high line & 17 low line
Pout = 1000;                      % Output power
Iout = Pout/Vout;                 % Output current - assumed constant for the time being
Iout_base = Iout*1;
Iout_step = Iout*0;
Duty_init = 1;                    % Initial value of duty cycle, output of current controller.

%Circuit parameters
C = (2*Iout)/(2*V_freq*0.7)       % Capacitor value with 0.7 V p-p voltage ripple
%C= 660e-6;                       % C= 660e-6;
%rC = 0;                          % ESR of the 330 uF output caps - 0.3/2
%L = 0.9e-3;                      % Specific value for L
L = Vout/(4*160000*0.5);          % L = 0.9e-3H; @ 50 Hz, fsw = 100 kHz. L = 4.75e-5; @ 400 Hz, fsw =
200kHz
%rOn = 0.35;                      % on-state resistance for power MOSFET
%rL = 0.02;                       % contact resistance of transfomer
%rDiode = 0;                      % conduction resistance of diode
%r = rL+(rDiode+rOn)*0.5;         % "Averaged" model of parasitic elements concerning the inductor
current

%% Simulation settings
% Parameters for the different times of the model
T_Period = pi/(V_freq);           % Voltage control sampling
Stop_time = T_Period*20;          % End time of the simulation
Tsw = 1/(1*1.6e5);                % Switching frequency -
Tts = Tsw/100;                    % Time-step
Tsample = -1;                     % Sample time, not important, "-1" means inherited.
T_iL_sample_delay =   0.3*Tsw;    % Sample delay of the ADC (3) of the current
T_iL_sample_delay_2 = 0.2*Tsw;    % Sample delaf of the ADC (4) of the current
dt_sample = T_iL_sample_delay_2-T_iL_sample_delay;

%% Voltage compensator
wcv = (1/4)*V_freq;
wzv = wcv/1;
Mmin = Vout/200;
gc = 200/(V_amp*Mmin);
Kvp = (wcv*C)/(2*gc);
Kvi = Kvp*wzv;

%% Current Controllers
%wci = V_freq*40;
wci = 16000*2*pi;
```

```
wzi = wci/10;
Kip = (wci*L)/(Vout);
Kii = Kip*wzi;
Params = [Tsw Kvp Kvi Kip Kii]

%% Initialize simulation
% sim('TheModel_VoltageCurrentController');
% sim('TheModel_VoltageCurrentController_Version1');
% sim('TheModel_VoltageCurrentController_Version2');
% sim('TheModel_VoltageCurrentController_Version3');
sim('TheModel_VoltageCurrentController_Version4');
% sim('TheModel_VoltageCurrentController_Version5');
DynModelPP

**********Post processing file**********
close all;
%% Simulation of input filter
tau = 1/(2*pi*10e3);
a = Tts/tau;
iin_filter = filter(a, [1 a-1], iin);

% % z  = iin_filter_avg;
% % Lz =pow2(nextpow2(length(iin_filter_avg)));
% % dfz = 1000/Lz;
% % Z = fft(z,Lz);
% %
% % figure
% % plot((1:Lz/2),2*abs(Z(1:end/2))/Lz)
%% Computations of RMS
% % RMS of Currents - using the last 33% of the values (represent steady
% % state)
% I_RMS_Diode = sqrt(mean(idiode(length(idiode)*0.666:length(idiode)).^2))
% I_RMS_MOSFET = sqrt(mean(iMOSFET(length(iMOSFET)*0.666:length(iMOSFET)).^2))
% I_RMS_Cap = sqrt(mean(iCap(length(iCap)*0.666:length(iCap)).^2));
% I_RMS_L = sqrt(mean(iL(length(iL)*0.95:length(iL)).^2))
% I_RMS_L1= sqrt(mean(Iref(length(Iref)*0.666:length(Iref)).^2));    % Assumption that Iref has
minimal distortion
% I_RMS_iin = sqrt(mean(iin(length(iin)*0.9:length(iin)).^2))
% % Total Harmonic Distortion
% THD_procent = 100*(sqrt(I_RMS_L.^2-I_RMS_L1.^2)/I_RMS_L1);
% % Conduction losses
% Plosses_L = I_RMS_L.^2*rL;
% Plosses_C = I_RMS_Cap.^2*rC;
% Plosses_diode = I_RMS_Diode.^2*rDiode;
% Plosses_switch = I_RMS_MOSFET.^2*rOn;
% Total_losses = Plosses_L+Plosses_C+Plosses_diode+Plosses_switch;

%% Average Current Calculation
% i1 = iL_sample_ADC3;
% i2 = iL_sample_ADC4;
% t1 = T_iL_sample_delay;
% t2 = T_iL_sample_delay_2;
```

```
% m = (i2-i1)/(t2-t1);
% IL_avg = i1-m.*(t1)+m.*d*Tsw*0.5;


%% Plotting of simulation output voltage and current controller
% figure
% subplot(3,1,1)
% plot(time, iL, time, Iref, time,IL_avg, time, iL_sample_ADC3,time, iL_sample_ADC4)
% legend('iL','Iref','IL', 'iADC3','iADC4')
% title('Inductor and reference current')
% ylabel('iL [A]')
% xlabel('Time [s]')
% subplot(3,1,2)
% plot(time, Load, time, Irefstep)
% legend('Voutsim/60','Vcontrol')
% title('Output current and control voltage')
% ylabel('Vout [V], iL[A]')
% xlabel('Time [s]')
% subplot(3,1,3)
% plot(time, d)
% ylim([0 1.1])
% ylabel('D [p.u]')
% xlabel('Time [s]')
% title('Duty Cycle')

% Inductor current and cuty cycle whole run
figure
subplot(2,1,1)
plot(time, iL, time, Iref)
legend('iL','Iref','IL')
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
subplot(2,1,2)
plot(time, d)
ylim([0 1.1])
ylabel('D [p.u]')
xlabel('Time [s]')
title('Duty Cycle')

% Output voltage - model verification
figure
plot(time, V_out_sim)
line([0 Stop_time], [Vout Vout])
title('Output Voltage')
xlim([15*T_Period 20*T_Period])

% Vout, iL, D
figure
subplot(3,1,1)
plot(time, V_out_sim,'k')
line([0 Stop_time], [Vout Vout])
```

```
title('Output Voltage')
legend('Vout','Voutref')
subplot(3,1,2)
plot(time, iL, time, Iref)
legend('iL','Iref','IL', 'iADC3','iADC4')
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
subplot(3,1,3)
plot(time, d)
ylim([0 1.1])
ylabel('D [p.u]')
xlabel('Time [s]')
title('Duty Cycle')


% figure
% plot(time, iL_sample_ADC3, time, iL)
% title('Sampled and actual inductor current')
%
figure
subplot(2,1,1)
plot(time(length(time)*0.9:length(time)),
iL(length(iL)*0.9:length(iL)),time(length(time)*0.9:length(time)),
10*d(length(d)*0.9:length(d)),time(length(time)*0.9:length(time)), Iref(length(Iref)*0.9:length(Iref)));
legend('iL','d*10','Iref')
title('Inductor current and duty cycle')
xlim([4*0.01125 4*0.0125])
subplot(2,1,2)
plot(time(length(time)*0.9:length(time)),Vrectified(length(Vrectified)*0.9:length(Vrectified)))
line([0 0.1], [Vout/2 Vout/2])
legend('Line Voltage','Vout/2')
xlim([4*0.01125 4*0.0125])

figure
plot(time(length(time)*0.9:length(time)),
iin(length(iin)*0.9:length(iin)),time(length(time)*0.9:length(time)),
0.05*Vline(length(Vline)*0.9:length(Vline)))
xlim([0.0225 0.025])
title('Input waveforms')
ylabel('[V],[A]')
xlabel('Time [s]')
legend('Input current','1/20 scale of Input Voltage')


% figure
% plot(time(length(time)*0.9:length(time)), iin(length(iin)*0.9:length(iin)))
% hold on
% plot(time(length(time)*0.9:length(time)), 0.05*Vline(length(Vline)*0.9:length(Vline)))
% hold on
% plot(time(length(time)*0.9:length(time)), Iref(length(Iref)*0.9:length(Iref)))
% legend('Input Current','Input Voltage','Inductor Current reference')
```

```
figure
plot(time(length(time)*0.9:length(time)), iin(length(iin)*0.9:length(iin)),
time(length(time)*0.9:length(time)),
0.05*Vline(length(Vline)*0.9:length(Vline)),time(length(time)*0.9:length(time)),
Iref(length(Iref)*0.9:length(Iref)))
legend('Input Current','1/20 of Input Voltage','Inductor Current reference')
xlim([0.0225 0.025])
title('Waveforms of inputs one period')
ylabel('[V],[A]')
xlabel('Time [s]')

figure
plot(time(1:length(time)), iin(1:length(iin)), time(1:length(time)), 0.1*Vline(1:length(Vline)))
legend('Input Current','1/20 of Input Voltage','Inductor Current reference')
title('Waveforms of inputs whole run')
ylabel('[V],[A]')
xlabel('Time [s]')

figure
plot(time(1:length(time)), iin_filter(1:length(iin_filter)), time(1:length(time)),
0.1*Vline(1:length(Vline)))
legend('Input Current','1/20 of Input Voltage','Inductor Current reference')
title('Waveforms of inputs whole run')
ylabel('[V],[A]')
xlabel('Time [s]')

figure
plot(time(length(time)*0.95:length(time)), iL(length(iL)*0.95:length(iL)),
time(length(time)*0.95:length(time)),  Iref(length(Iref)*0.95:length(Iref)))
legend('Inductor Current','Inductor Current reference')
xlim([0.02375 0.025])
title('Waveforms of inductor current and reference')
ylabel('[A]')
xlabel('Time [s]')

%% Load step plot
figure
subplot(3,1,1)
plot(time, V_out_sim,'k')
line([0 Stop_time], [Vout Vout])
title('Output Voltage')
legend('Vout','Voutref','South')
xlim([0.02 T_Period*40])
subplot(3,1,2)
plot(time, iL, time, Iref)
legend('iL','Iref','South')
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
xlim([0.02 T_Period*40])
subplot(3,1,3)
```

```
plot(time, Load)
ylabel('I [A]')
xlabel('Time [s]')
xlim([0.02 T_Period*40])
title('Load dc current')

figure
subplot(3,1,1)
plot(time, V_out_sim,'k')
line([0 Stop_time], [Vout Vout])
title('Output Voltage')
xlim([0.02 T_Period*40])
subplot(3,1,2)
plot(time, iL, time, Iref)
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
xlim([0.02 T_Period*40])
subplot(3,1,3)
plot(time, Load)
ylabel('I [A]')
xlabel('Time [s]')
xlim([0.02 T_Period*40])
title('Load dc current')


% figure
% plot(time(length(time)*0.9:length(time)), idiode(length(idiode)*0.9:length(idiode)))

% figure
% plot(time(length(time)*0.9:length(time)), iMOSFET(length(iMOSFET)*0.9:length(iMOSFET)))
%% Plots of steady state
% 800 Hz
figure
subplot(2,1,1)
plot(time, iL, time, Iref)
legend('iL','Iref','IL')
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
xlim([T_Period*16 T_Period*20])
subplot(2,1,2)
plot(time, d)
ylim([0 1.1])
ylabel('D [p.u]')
xlabel('Time [s]')
title('Duty Cycle')
xlim([T_Period*16 T_Period*20])

figure
plot(time(1:length(time)), iin(1:length(iin)), time(1:length(time)), 0.1*Vline(1:length(Vline)))
legend('Input Current','1/10 of Input Voltage','Inductor Current reference')
```

```
title('Input current')
ylabel('[V],[A]')
xlabel('Time [s]')
xlim([T_Period*16 T_Period*20])

figure
plot(time(1:length(time)), iin_filter(1:length(iin_filter)), time(1:length(time)),
0.1*Vline(1:length(Vline)))
legend('Input Current','1/10 of Input Voltage','Inductor Current reference')
title('Filtered input current')
ylabel('[V],[A]')
xlabel('Time [s]')
xlim([T_Period*16 T_Period*20])

%%
figure
plot(time, iL, time, Iref)
legend('iL','Iref')
title('Inductor and reference current')
ylabel('iL [A]')
xlabel('Time [s]')
xlim([0 T_Period*0.5])


%% Save values to files
%save('simuleringsvarden400Hz.mat','time','iin_filter','iin','Vline')
```