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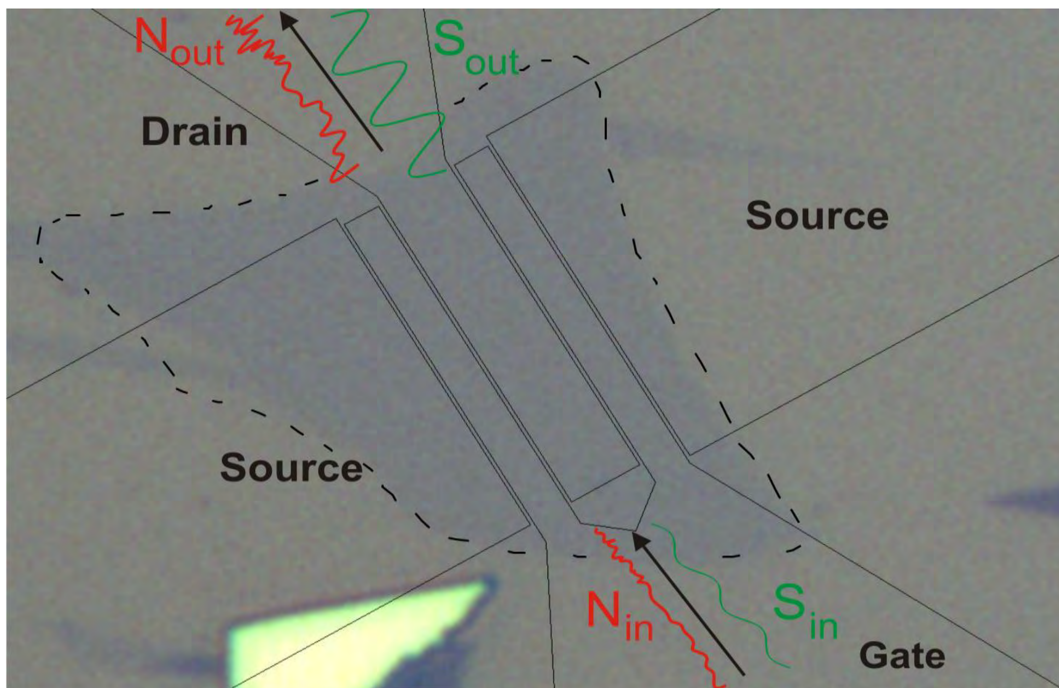

Noise Characterisation of Graphene FETs

Investigation of noise in amplifier and mixer applications

Thesis for the degree of Master of Science in Wireless and Photonics Engineering

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Cover:
AutoCAD pattern for a G-FET on an exfoliated graphene flake, with the aim of amplifying a microwave signal while adding a minimum level of noise. The dashed line is a help for the eye to distinguish the single-layer graphene.

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Abstract

This thesis deals with the first noise performance study of graphene field effect transistors (G-FETs) at microwave frequencies. It considers G-FETs in two different applications, as a subharmonic resistive mixer and in an amplifier. The work encompasses cleanroom fabrication, as well as characterisation by measurement and modelling. As part of the work a G-FET amplifier operating at 1 GHz with 10 dB small-signal power gain is designed, an 8 dB improvement comparing to earlier reports. The amplifier noise figure is measured to be 6.4 $\pm$ 0.4 dB at 1 GHz. Modelling by the Pospieszalski temperature noise model predicts the minimum extrinsic and intrinsic noise figure of the G-FET itself to be $F_{min,ex}$ = 3.3 dB and $F_{min,in}$ = 1.0 dB, respectively. Furthermore, the subharmonic mixer exhibits a down-conversion loss of 20-22 dB to f_{IF} = 100 MHz in the RF frequency interval f_{RF} = 2-5 GHz. The mixer noise figure closely mimics the conversion loss, which suggests the noise of the mixer to be thermal in origin. Conventional FET modelling methods have proven helpful in the analysis also for G-FETs.

Keywords: Graphene FET, microwave amplifiers, noise measurements, noise figure, subharmonic resistive mixer

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Abbreviations and acronyms

ALD	Atomic Layer Deposition
CPW	Coplanar Waveguide
CVD	Chemical Vapour Deposition
CL	Conversion Loss
DOS	Density Of States
EBL	Electron Beam Lithography
ENR	Excess Noise Ratio
F_{min}	Minimum noise figure
$F_{min,ex}$	Minimum *extrinsic* noise figure
$F_{min,in}$	Minimum *intrinsic* noise figure
FET	Field Effect Transistor
f_T	Cutoff frequency
f_{MAX}	Maximum frequency of oscillation
G_A	Available power gain
G_T	Transducer power gain
G-FET	Graphene Field Effect Transistor
hBN	Hexagonal Boron Nitride
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric acid
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NFA	Noise Figure Analyser
PECVD	Plasma Enhanced Chemical Vapour Deposition
RF	Radio Frequency
RL	Return Loss
RT	Room Temperature (T = 290 K)
THz	Terahertz (10^{12} Hz)
U	Mason's unilateral gain

Chapter 1

Introduction

Most people in modern society certainly utilise microwaves, usually defined as frequencies in the range from 300 MHz to 300 GHz, as a part of their everyday life. Applications range from communication in cellular phones and wireless LANs, navigation and positioning with GPS and entertainment by means of satellite based TV broadcasting to more indirect usage via e.g. weather forecasting [1]. Emerging applications include medical usage in e.g. cancer tumour detection and treatment [2] and increased usage for safety features in cars [3]. While the majority of these commercial functionalities operate below 10 GHz, also the market for systems higher into the terahertz (THz) range, loosely defined as the range 0.1 - 10 THz, is expanding. The growth at these frequencies, before mainly limited to research in radioastronomy and spectroscopy, is largely from imaging security applications [4].

Common to all these systems is the need to receive and transmit information carried by high frequency signals. Fundamental components in any receiver include low noise amplifiers (LNAs) and frequency down-converting mixers, while a transmitter requires up-converting mixers and power amplifiers (PAs). Virtually all microwave amplifiers are designed using solid-state devices, either bipolar junction transistors (BJTs) or field effect transistors (FETs) whereas mixers are often implemented using FETs.

1.1 Microwave transistors

The advent of microwave transistors began in 1967 with a GaAs metal-semiconductor FET (MESFET), having a a cut-off frequency $f_T = 3$ GHz [5]. While the usage of GaAs MESFETs is limited to $f < 50$ GHz, the introduction of the GaAs high electron mobility transistor (HEMT) in 1980 [6] enabled the race towards terahertz frequencies. With the state-of-the-art technology today, InP HEMTs, a maximum frequency of oscillation $f_{max} > 1$ THz [7] and 10 dB small-signal gain MMIC amplifiers at 650 GHz have been demonstrated [8]. The output power is limited to 1.7 mW for an eight stage TMIC (terahertz monolithic integrated circuit) amplifier and 3 mW when power combining two such circuits, which can be compared to Figure 1.1. Also, the InP heterojunction bipolar transistor (HBT) reach $f_{max} \approx 1$ THz [7] allowing for 8 dB small-signal MMIC amplifier circuits at 300 GHz [9].

Although other factors influence when gate length down-scaling is performed, carrier mobility and saturation velocity are closely related to the high-speed and noise performance of FETs, where Si metal oxide semiconductor FETs (MOSFETs) and GaAs MESFETs are surpassed by the high mobility 2D electron gas in GaAs HEMTs, which in turn is outperformed by the InP HEMTs.

1.2 Graphene for terahertz transistors?

With the maturity of InP technology the microwave community is constantly exploring new materials with increasingly higher carrier mobility to further push the limits of FETs, such as InSb HEMTs reaching $f_{max} > 200$ GHz [10]. More exotic, new device concepts include InAs nanowire FETs which reach $f_{max} =$ 14 GHz [11] and carbon nanotube (CNT) FETs. Although a CNT FET with *intrinsic* $f_T = 80$ GHz has been reported it is largely hampered by parasitics, but has proven to provide 11 dB small-signal gain at 1.3 GHz [12].

Recently, with the first production and demonstration of the field-effect in graphene in 2004 [13], a new promising candidate was introduced. Graphene, a single sheet of carbon atoms, is a truly 2D material with a measured superior room temperature carrier mobility of 100,000 cm^2/Vs for both electrons and holes. Together with its high carrier saturation velocity, $v_{sat} = 4\cdot 10^7$ cm/s, this property predicts its suitability for high frequency and low noise FETs. Further, the thin channel is believed to suppress short channel effects and allow even higher speeds in graphene based FETs [14]. The ultimate aim certainly is to push microwave electronics to close the THz-gap in Figure 1.1.

In a short time the development of graphene FETs (G-FETs) has proven the potential, with *intrinsic* cut-off frequencies on the order of $f_T = 300$ GHz [15,16] and a record *intrinsic* $f_{max} = 44$ GHz [16]. Several frequency translating devices, mixers [17,18] and multipliers [19], and one occurrence of small-signal gain with 50 Ω loading [20] have all been demonstrated. Nevertheless, several issues remain to be solved, including the high contact resistance which results in a large discrepancy between the extrinsic and intrinsic results [14], and the choice of a stable gate oxide allowing for high mobilities in the G-FET channel [21]. A recent review of graphene in RF applications is given in [22].

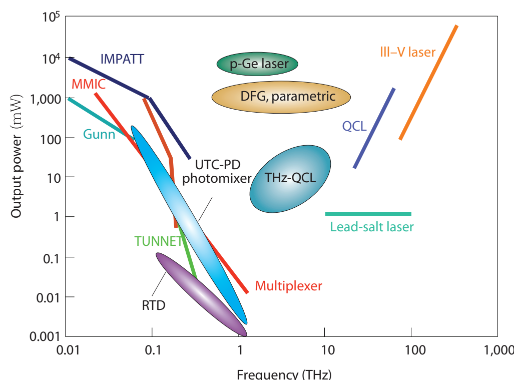

Figure 1.1: Illustration of the THz gap, where both the electronic and photonics fail to provide compact, room temperature sources with sufficient output power [4].

1.3 Scope

This master thesis deals with a further investigation of the future potential of G-FETs by measuring, for the first time, the microwave noise figure in two different applications; namely a novel G-FET amplifier [Paper A] and a subharmonic G-FET mixer [Paper B]. The work covers the complete manufacturing process, including graphene material production and patterning of G-FETs using electron beam (e-beam) lithography, as well as characterising the devices experimentally through DC and RF measurements. A key part is the design of the amplifier operating at 1 GHz which allows for accurate noise figure measurements. Finally, to further estimate the future achievable noise performance, noise modelling is utilised to predict the minimum noise figure in eliminating the noisy parasitic resistances.

This work is a continuation of the recent Licentiate Thesis [23] from the Terahertz and Millimetre Wave Laboratory, in which the original process was established. As such, the work investigates and takes the appropriate steps to adapt and develop the G-FETs to the requirements of noise figure measurements, i.e. to provide small-signal gain in amplifier applications, which is discussed in [Paper C].

The report, in turn, gives the background theory, method and results of this work. The next chapter starts with a noise treatment in microwave systems, then deals with the basic physics, DC, small-signal and noise behaviour of field effect transistors and concludes with a review of the graphene and G-FET fields to date. Finally, a section containing discussion and conclusion ends the report.

Chapter 2

Theory

This chapter first introduces the concept of noise in a microwave system. It then continues with a description of the properties of the field effect transistor. This is followed by a description of the intrinsic potential of graphene. It concludes with the performance of graphene field-effect transistors, G-FETs.

2.1 Noise

A treatment of noise in microwave systems relies on the concept of equivalent noise temperature. It is in turn based on the theory of thermal noise generated by random movement of carriers in any lossy component, as discovered experimentally by Johnson [24] and explained theoretically in more detail by Nyquist [25]. Consequently, it is illustrative to start a noise analysis with the noise properties of a resistor and then move on to microwave components.

2.1.1 Resistor noise and noise temperature

A resistor at physical temperature T can be modeled with a noiseless resistor in series with a voltage source that produces an RMS noise voltage according to

$$v_n = \sqrt{4kTR\Delta f} \qquad [\text{V}]. \tag{2.1}$$

This yields the maximum available noise power a resistor delivers to a matched load to be the well-known $N = kTB$, with $P_n = kT$ being the spectral density of available noise power from a resistor. More generally the spectral density of available thermal noise power from a resistor is given by $P_n = kT_n$ [W/Hz], where T_n [K] is the noise temperature. The distinction is that T_n may be different from the physical temperature, due to additional noise from vacuum fluctuations. The complete expression for resistor noise temperature is then given by the Callen-Welton expression [26] of (2.2).

$$T_n^{C-W} = T\left[\frac{\frac{hf}{kT}}{exp(\frac{hf}{kT}-1)}\right] + \frac{hf}{2k} \qquad [\text{K}] \tag{2.2}$$

However, when $hf \ll kT$ is a valid assumption, the Rayleigh-Jeans approximation that the noise temperature is equal to the physical temperature can be used with negligible error according to

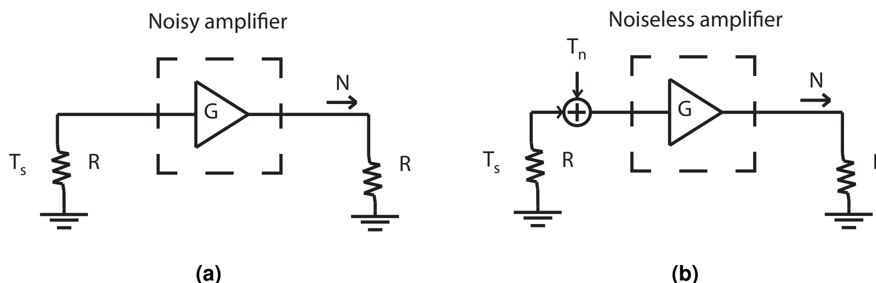

Figure 2.1: Illustration of equivalent input noise temperature with the output noise power N equal in both cases, since $T_n = T_L/G$, and given as; (a) $N = k\Delta f(GT_s + T_L)$ (b) $N = k\Delta f G(T_s + T_n)$.

$$T_n = T \qquad [\mathrm{K}], \tag{2.3}$$

as implied above. This yields a white noise process where the power in a certain bandwidth, B, is simply given by $N = kTB$. The range of frequencies for which the assumption is valid is dependent upon physical temperature. At a cryogenic temperature it corresponds to $f < 100$ GHz, while at room-temperature the acceptable region extends to $f = 1$ THz.

The noise of e.g. an amplifier, regardless of type including thermal noise, shot noise or 1/f noise, is typically modelled in a system perspective to be white thermal noise of a resistor at its input and the component itself is considered noiseless. Thus, the amplifier is described by its equivalent input noise temperature, T_n, which relates to its output noise temperature, T_L, as $T_n = T_L/G$. The situation is illustrated in Figure 2.1 [27].

2.1.2 Noise figure

It is convenient to introduce also the concept of noise figure, defined by Friis in [28] as the degradation in signal-to-noise ratio from the input to the output of a component (with an input termination at a physical temperature of 290K) as

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} > 1 \qquad [\mathrm{dB}]. \tag{2.4}$$

Further, Friis relates the noise figure to the equivalent noise temperature of an amplifier, T_A, as

$$F = 1 + T_A/T_N(290) \qquad [\mathrm{dB}]. \tag{2.5}$$

The current IEEE definition of noise figure uses instead an input termination with a noise temperature of 290K [26], which yields

$$F = \left[T_N(290) + T_A\right]/290 \qquad [\mathrm{dB}]. \tag{2.6}$$

Although the difference above 1 THz is distinct, at microwave frequencies, where $hf \ll kT$, both definitions reduce to the classical relation of (2.7), since $T_N(290) = 290$ according to the Rayleigh-Jeans approximation.

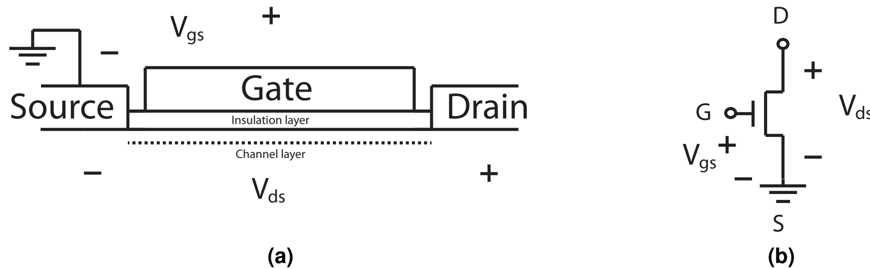

Figure 2.2: (a) Cross sectional view of a MOSFET. (b) Circuit symbol of a FET.

$$F = 1 + T_A/290 \qquad \text{[dB]} \tag{2.7}$$

2.2 Field Effect Transistors

By definition, a transistor is a component with three terminals, where one contact is used to control the electrical conductance between the other two. In a field-effect transistor (FET), capacitive control is employed to alter the conductivity via a transverse field, a concept attributed to Shockley at Bell Labs in 1952 [29]. Further, the current flows due to an electric field between the drain and source terminals. Thus the FET is operated by the two voltages V_{gs} and V_{ds}, respectively, with the source generally grounded as in Figure 2.2.

Mainly two different approaches to realise the gate capacitor are used [30]. Firstly, in a metal semiconductor FET (MESFET) the capacitor associated with the metal-semiconductor (Schottky) interface is used. Secondly, an insulating gate is realised, represented either by a large bandgap semiconductor layer as in a high electron mobility transistor (HEMT), or by a dielectric/oxide layer as in a metal oxide semiconductor FET (MOSFET).

Normally, FETs are distinguished to be either n-type (conducting electrons) or p-type (conducting holes) devices, and if they are enhancement mode (normally off) or depletion mode (normally on) devices.

2.2.1 Relevant semiconductor properties

A first indicator of the final device performance is the response of carriers in the channel due to the application of an electrical field. The following treatment assumes a semiconductor where carrier behavior is obtained by solving the Schrödinger equation.

For sufficiently low fields the carriers are set into motion with a drift velocity according to

$$v_{drift} = \mu E \qquad [cm^2/Vs], \tag{2.8}$$

where μ is the (field independent) carrier mobility [30]. The free motion of carriers is interrupted by different scattering mechanisms, where the resulting mobility is calculated by the Matthiessen rule as $\mu = (1/\mu_l + 1/\mu_i)^{-1}$. Here μ_l

Table 2.1: Effective mass, low-field mobility and saturation velocity (*peak) of typical bulk FET semiconductors. Values given at room temperature and low doping level.

Semiconductor	Si	GaAs	GaN	InAs	InSb
m_e^*/m_0	0.98	0.063	0.19	0.023	0.015
μ_e $[cm^2/Vs]$	1,400	8,000	1,600	33,000	80,000
v_{sat} $[10^7\ cm/s]$	1	1.5*	1.1	3.5*	5*

arises from acoustic phonons (lattice vibrations) and μ_i from charged impurities such as ionized donors or acceptors.

The mobility is directly related to the carrier effective mass, m^*, which is derived from the energy band structure, $E(k)$, of a semiconductor as in (2.9). Both mobilities, μ_l and μ_i, depend on the effective mass as $\mu_{l,i} \propto 1/m^*$.

$$m^* = \frac{1}{\hbar^2}\left(\frac{d^2E}{dk^2}\right)^{-1} \qquad [kg] \tag{2.9}$$

Increasing the field strength, the simple relation of (2.8) no longer holds. Instead the carrier drift velocity saturates to a certain temperature dependent value. This can be described by the empirical relation

$$v_{drift} = \frac{\mu E}{\left(1 + (\frac{\mu E}{v_{sat}})^x\right)^{1/x}} \qquad [cm/s] \tag{2.10}$$

where μ is the low-field mobility and x is a temperature dependent parameter extracted from experimental data [30]. Furthermore, many III-V semiconductors exhibit a peak drift velocity for a certain electric field strength, beyond which the drift velocity decreases with increasing field. Table 2.1 summarises carrier dynamics for some bulk semiconductor materials suitable for FETs.

2.2.2 Ideal DC characteristics

The DC behavior of an n-type enhancement mode FET is described by the transfer characteristic, $I_{ds}(V_{gs})$ for a fixed V_{ds} and the output characteristic, $I_{ds}(V_{ds})$ for a fixed V_{gs}. Basically, the transistor can be operated in a linear region or in current saturation, for $V_{ds} < V_{dsat}$ and $V_{ds} > V_{dsat}$, where V_{dsat} is the drain-source voltage where current saturation sets in, Figure 2.3a. The following treatment exemplifies using a silicon MOSFET with a channel long enough for velocity saturation to be negligible [30]. Similar relations apply also to HEMTs and MESFETs with slight modification.

The transfer characteristic is described by (2.11) for a fixed V_{ds}, where C_{ox} $[F/cm^2]$ is the gate capacitance per area and V_T [V] the threshold voltage, which is the minimum gate voltage for a conductive channel.

$$I_{ds} = k\left((V_{gs} - V_T)\frac{V_{ds}}{2}\right)V_{ds} \quad for \quad V_{ds} < V_{dsat} \quad [\text{A}] \tag{2.11a}$$

$$I_{dsat} = \frac{k}{2}(V_{gs} - V_T)^2 \quad for \quad V_{ds} > V_{dsat} \quad [\text{A}] \tag{2.11b}$$

$$k = \frac{W}{L}\mu C_{ox} \qquad [A/V^2] \tag{2.11c}$$

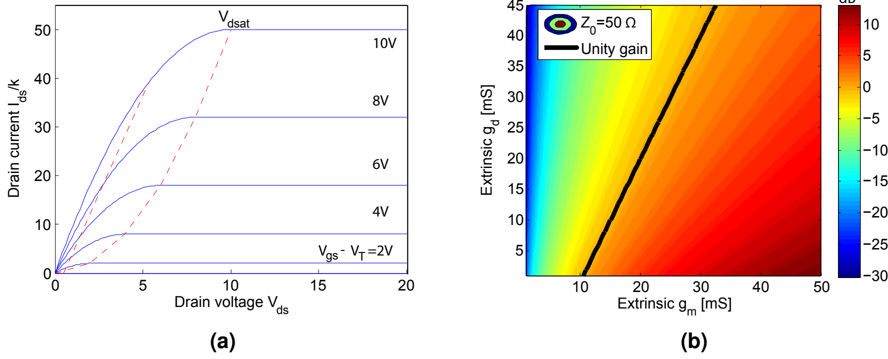

Figure 2.3: (a) Output characteristics illustrating ideal current saturation in drain voltage. The dashed lines indicate the linear and quadratic regimes in gate voltage. (b) Low frequency small-signal gain with 50 Ω terminations from (2.15).

The slope of the $I_{ds}(V_{gs})$ curve is the transconductance, g_m [S], defined and calculated in (2.12). It is proportional to V_{ds} in the linear region, V_{gs} in the saturation region and increases with transistor parameter k.

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=constant} \qquad [\mathrm{S}] \tag{2.12a}$$

$$g_m = kV_{ds} = \frac{W}{L}\mu C_{ox}V_{ds} \qquad for \qquad V_{ds} < V_{dsat} \quad [\mathrm{S}] \tag{2.12b}$$

$$g_m = kV_{gs} = \frac{W}{L}\mu C_{ox}V_{gs} \qquad for \qquad V_{ds} > V_{dsat} \quad [\mathrm{S}] \tag{2.12c}$$

The output characteristic is divided into the linear, non-linear and current saturation regimes (Figure 2.3a), dependent upon the drain to source voltage, V_{ds}. For $V_{ds} << V_{dsat}$ the transistor acts basically as a resistor variable with the gate voltage, V_{gs}. Further, for intermediate V_{ds} a non-linearity appears, as predicted by (2.11a). Lastly, at $V_{ds} > V_{dsat}$ current saturation sets in, where the drain current is independent of V_{ds} and quadratic in V_{gs} (2.11b). The slope of the $I_{ds}(V_{ds})$ curve is the output conductance, g_d [S], defined in (2.13). An increase in V_{ds} towards complete saturation yields $g_d \rightarrow 0$. The dashed borderline in Figure 2.3a to the saturation region is given by equation (2.11b) since $V_{dsat} = V_{gs} - V_T$.

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=constant} \qquad [\mathrm{S}] \tag{2.13}$$

If instead, the device has a short channel to yield a sufficiently high field, velocity saturation will dominate the carrier transport [30]. As a consequence, the saturation current and transconductance are both proportional to v_{sat}, not the mobility μ, as were the case for low fields in long channels, e.g.

$$g_m = WC_{ox}v_{sat} \qquad [\mathrm{S}]. \tag{2.14}$$

The formation of ohmic contacts is a crucial step for a MOSFET, which is a metal-semiconductor junction with very low resistance. It must contribute

only a small fraction of the device resistance, thus yielding a voltage drop that is negligible compared to the voltage drop across the active region [30]. This is generally done via heavy doping of the semiconductor and choosing a contact metal with a low work function compared to the bandgap of the semiconductor.

2.2.3 Small-signal amplifier

The main application of FETs is as small-signal amplifiers, where the transistor operates at a certain DC bias point (V_{GS}, V_{DS}, I_{DS}). A small-signal $v_{gs} = V sin\omega t$ is superimposed on the gate-source voltage yields a current variation $i_{ds} = g_m v_{gs} = g_m V sin(\omega t)$. A high g_m is thus important to realise an amplifier, which decides the bias point. This gives a qualitative understanding of the amplifier operation, while the formal design is made using S-parameters measured at a certain bias point [31]. In order to simplify, the pad resistances R_s and R_d can be included into the intrinsic transconductance and output conductance and the frequency dependent elements in the FET are ignored. This yields a small-signal equivalent circuit according to Figure 2.4 containing the extrinsic values g_{me} and g_{de}. These are the corresponding quantities as found via the measured FET characteristics. At low frequencies the small-signal gain can then be calculated as

$$S_{21} = -\frac{2Z_0 g_{me}}{(Z_0 g_{de} + 1)} \qquad \text{[dB]}, \tag{2.15}$$

where Z_0 is the system characteristic impedance. Based on (2.15) the contour plot in Figure 2.3b clearly illustrates the importance of a high g_{me} and a low g_{de} (i.e. operation in current saturation) to have a high gain.

2.2.4 Complete small-signal model

At higher frequencies, the capacitors and inductors may not be approximated as open and short, but instead the model of Figure 2.5 is used. The model elements of a FET in are divided into intrinsic and extrinsic. The intrinsic part describes the inherent FET behavior, via a voltage controlled current source, and the capacitive nature of the component. On the other hand, the extrinsic portion of the circuit contains the parasitic effects which result from the contact pads. Generally, the intrinsic part is bias dependent, while the extrinsic part is bias independent. The small-signal equivalent circuit is important to understand the

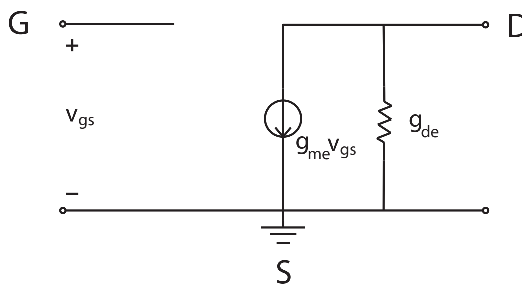

Figure 2.4: Small-signal model of a FET at low frequencies, with extrinsic g_m and g_d.

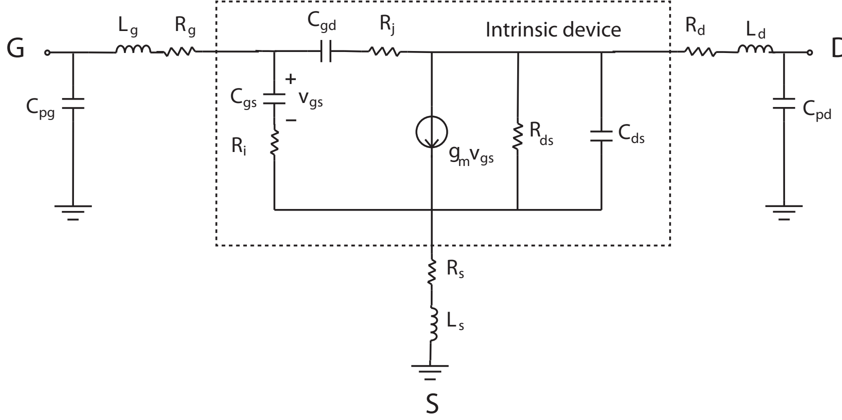

Figure 2.5: Complete small-signal model for a FET including frequency dependent parasitics. The intrinsic parameters are within dashed lines.

optimisation of FETs for them to operate at very high frequencies (Section 2.2.5) and a crucial building block in the noise modelling of FETs (Section 2.2.6).

The extraction of the model parameters starts with the determination of the parasitic elements from S-parameter measurements of the transistor structure when shorted and open. For HEMTs and MOSFETs the measurements are made at $V_{ds} = 0$ (cold-FET method [32]), altering the gate voltage to make the channel fully conductive or pinched off, respectively. Next, the measured S-parameters of the device at a desired bias point are de-embedded using the previously determined parasitic element values and two-port parameter conversions to find the intrinsic y-parameters of the transistor. Analytical expressions for the intrinsic y-parameters have been derived (reproduced in (2.16)), from which the intrinsic component model values can be calculated, as found in the literature (e.g. [32]).

$$y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega \left(\frac{C_{gs}}{D} + C_{gd} \right) \quad \text{[S]} \tag{2.16a}$$

$$y_{12} = -j\omega C_{gd} \quad \text{[S]} \tag{2.16b}$$

$$y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \quad \text{[S]} \tag{2.16c}$$

$$y_{22} = 1/R_{ds} + j\omega(C_{ds} + C_{gd}) \quad \text{[S]} \tag{2.16d}$$

$$D = 1 + \omega^2 C_{gs}^2 R_i^2 \quad \text{[-]} \tag{2.16e}$$

To relate the extrinsic, DC extracted quantities of (2.12) and (2.13) to the intrinsic counterparts in Figure 2.5, (2.17) and (2.18) are used [33].

$$g_{mi} = \frac{g_m^0}{(1 - (R_s + R_d) g_d (1 + R_s g_m^0))} \quad \text{[S]} \tag{2.17}$$

$$g_{di} = \frac{g_d^0}{(1 - R_s g_m (1 + (R_s + R_d) g_d^0))} \quad \text{[S]} \tag{2.18}$$

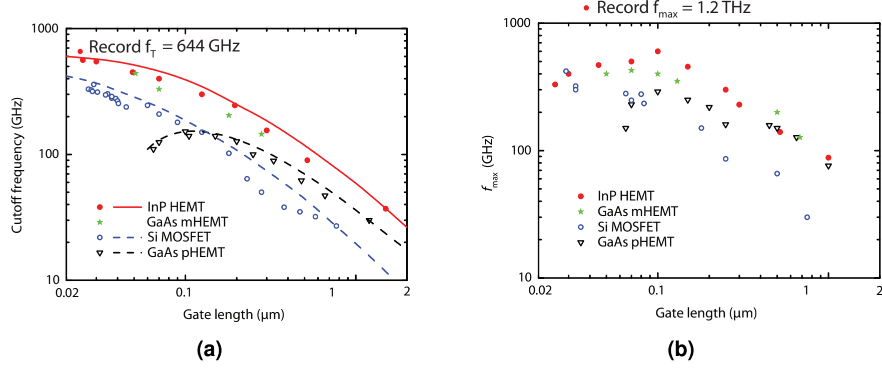

Figure 2.6: Reported gate length dependence for state-of-the-art FETs on (a) cutoff frequency, f_T, [34, 35] and (b) maximum frequency of oscillation, f_{max} [34, 36].

where $g_m^0 = \frac{g_{m,e}}{1-R_s g_{m,e}}$ and $g_d^0 = \frac{g_{d,e}}{1-(R_s+R_d)g_{d,e}}$. In mature HEMT and MOSFET technology the parasitic contact resistances are only a few ohms, resulting in $g_{mi} \simeq g_m$ and $g_{di} \simeq g_d$.

2.2.5 Figures-of-merit for a microwave FET

To benchmark the high frequency performance of transistors, where the parasitics reduce the gain compared to (2.15), mainly two different measures are used, the cut-off frequency, f_T, and the maximum frequency of oscillation, f_{max}. Importantly, neither a certain f_T or f_{max} guarantees the transistor to provide power gain with practical terminations. In addition, often the minimum noise figure is an important figure-of-merit of a microwave FET.

Cutoff frequency

The cut-off frequency occurs when the transistor has unity current gain, $f_T = f(|h_{21}| = 1)$. Generally, S-parameters are measured and the current gain calculated as

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} \qquad [\text{dB}] \tag{2.19}$$

An analytical expression for f_T has been derived [30], which is given here with reference to the notation of Figure 2.5

$$f_T = \frac{g_m}{2\pi\left((C_{gs}+C_{gd})\left(1+\frac{R_d+R_s}{R_{ds}}\right) + C_{gd}g_m(R_d+R_s) + C_{pg}\right)} \qquad [\text{Hz}]. \tag{2.20}$$

It is observed that in a region of current saturation (R_{ds} large) and for a mature technology with negligible parasitics, (2.20) reduces to the more simple form of an intrinsic FET

$$f_T \simeq \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{g_m}{2\pi C_g} \qquad [\text{Hz}]. \tag{2.21}$$

Thus, $C_g = C_{ox} \cdot W_g \cdot L_g$ [F], must be minimised while maintaining C_{ox} high to maximise g_m. This results in the well-known down-scaling principle to increase the cutoff frequency. Ideally, for a long channel MOSFET $f_T = \frac{\mu V_{gs}}{2\pi L_g^2} \propto 1/L_g^2$, while for a short-channel MOSFET $f_T = \frac{v_{sat}}{2\pi L_g} \propto 1/L_g$, which is illustrated in Figure 2.6a. Clearly the channel material mobility is important, as reflected with the increasing performance from Si, via $In_{0.2}Ga_{0.8}As$ of GaAs HEMTs to $In_{0.57}Ga_{0.43}As$ of InP HEMTs [34]. The ultimate cursor of high speed performance with aggressive gate length down-scaling, though, also includes the saturation velocity, as the electric field across the channel increases.

Nevertheless, Si MOSFETs reach a performance comparable with III-V HEMTs, despite the much lower mobility. This is due to easier avoidance of short-channel effects in FETs, e.g. lack of current saturation which counteract the improvement in C_g. This is mainly attributed to the possibility of realising a very thin barrier layer, gate oxide, between the gate and channel in a MOSFET which is important as L_g is decreased, and the higher density of states in Si as compared to III-V semiconductors [34].

In conclusion, for two technologies with the same device structure and resembling channel materials, the higher mobility and saturation velocity is the most advantageous, as illustrated by InP HEMTs outperforming GaAs HEMTs.

Maximum frequency of oscillations

The maximum frequency of oscillation occur when the unilateral power gain (Mason's gain [37]) equals unity, $f_{max} = f(U = 1)$. This is the highest frequency where the transistor provides power gain, if it is unilaterised, i.e. $S_{12} = 0$. Typically, U is calculated from measured S-parameters as [38]

$$U = \frac{|S_{12} - S_{21}|^2}{\mathbf{1} - \mathbf{SS}^*} \qquad \text{[dB]}. \tag{2.22}$$

An analytical expression to predict f_{max}, relative to f_T, is found in [30] to be

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_i + R_g + R_s}{R_{ds}} + 2\pi R_g C_{gd} f_T}} \qquad \text{[Hz]}. \tag{2.23}$$

In addition to the reasoning for the cutoff frequency, it is important to optimise the value of the gate resistance R_g for short gate length devices. This is typically addressed by fabricating a T-shaped mushroom gate for HEMTs or multigate fingers for MOSFETs.

Minimum noise figure

To quantify the noise performance of two-port FET amplifiers, the concept of noise figure is used, as introduced in Section 2.1.2. The noise figure is dependent upon the source admittance, Y_s, according to (2.24) [27].

$$F(Y_s) = F_{min} + \frac{R_n}{G_s} \cdot |Y_s - Y_{opt}|^2 \qquad \text{[dB]} \tag{2.24}$$

The equivalent noise resistance, R_n, is a measure of the rate at which the noise figure deteriorates with a deviation from the optimum source impedance, $Y_{opt} =$

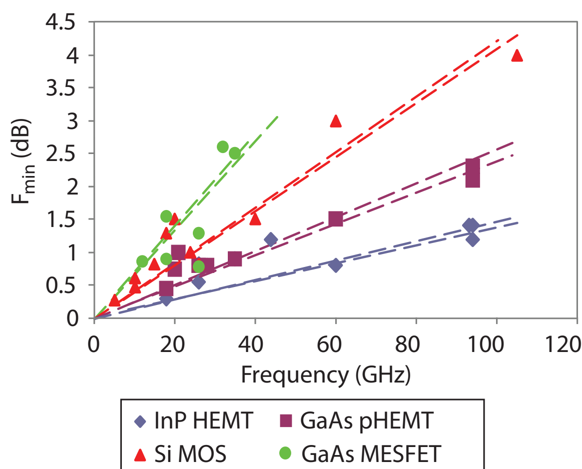

Figure 2.7: State-of-the-art F_{min} for four different FET technologies at RT [40].

$R_{opt} + jX_{opt}$, at which F_{min} is achieved. A set of noise parameters, including F_{min}, is only valid at the specific bias point at which they are measured. The best figure-of-merit is consequently to report the best F_{min} at the optimum DC current, I_{ds}. In addition, the corresponding available power gain, G_A, with source impedance Y_{opt} should be attached, which is also important for a low-noise amplifier (LNA) in a receiver chain. A high gain minimises the noise contribution cascaded components following the amplifier [27].

To understand the basic design principles for low noise figure of a FET, the relation of (2.25) [39] might be used as a first principle approach, with the small-signal equivalent circuit element notation of Figure 2.5, where $T_0 = 290$ K is the standard temperature.

$$T_{min} = (F_{min} - 1)\, T_0 \propto 2\frac{f}{f_T}\sqrt{(R_i + R_g + R_s)/R_{ds}} \propto \frac{\sqrt{I_{ds}}}{g_m} \qquad \text{[K]} \qquad (2.25)$$

A high g_m at a low I_{ds}, as well as low parasitic resistances, in general yields a low noise device. This relation is illustrated in Figure 2.7, which presents the state-of-the-art F_{min} at room temperature, where high f_T InP technology clearly outperforms Si MOSFETs and GaAs HEMTs in noise performance, which compares well to Figure 2.6.

2.2.6 Noise processes and modelling

Noise in FETs originates both from the intrinsic device and the parasitic elements. The extrinsic parts contributes mainly thermal noise from gate and source contact resistances, which is easily included when a model for the intrinsic noise is set up. Additionally, for FETs with large gate leakage current shot-noise and $1/f$ noise has to be included [40].

In long channel device, the intrinsic noise is thermal in origin. In a short-channel FET, on the other hand, where the carriers move at a saturated velocity, the noise is high-field diffusion noise [27]. Nevertheless, noise modelling in modern HEMTs and down-scaled Si MOSFETs derives from the original work by

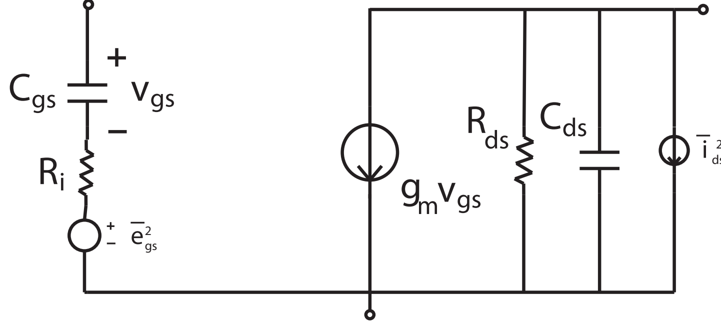

Figure 2.8: Intrinsic, uncorrelated FET thermal noise according to Pospieszalski, with a gate voltage source $\overline{e_{gs}^2} = 4kT_gR_i\Delta f$ and a drain current source $\overline{i_{ds}^2} = 4kT_dR_{ds}\Delta f$.

Van der Ziel [41] on thermal noise in FETs. Generally, the intrinsic noise is divided into drain thermal noise and induced gate noise. The PRC model of 1974 established the gate noise to be coupled from the channel via the gate capacitance and thus perfectly correlated [42]. Later, in 1989 Pospieszalski, interpreted the gate noise to be thermal and uncorrelated with the drain noise [43]. This approach is today widely used, and the model has been verified for both HEMTs and MOSFETs [40].

2.2.7 Pospieszalski's noise model

The Pospieszalski noise model takes as a starting point the intrinsic part of the small-signal circuit of Figure 2.5, with a voltage source representing gate noise and a current source representing the drain noise, according to Figure 2.8. It assigns two frequency independent equivalent noise temperatures, T_g of R_i and T_d of R_{ds}, to model the drain noise and gate noise, respectively. The model predicts all four noise parameters with closed form expressions in the equivalent noise temperatures, the intrinsic small-signal elements and frequency, where low frequency $1/f$ noise is negligible. The general expression for T_{min} is given by (2.26), where $f_T = \frac{g_m}{2\pi C_{gs}}$.

$$T_{min} = 2\frac{f}{f_T}\sqrt{(R_iT_gT_d)/R_{ds} + \left(\frac{f}{f_T}\right)^2 R_i^2T_d^2/R_{ds}^2} + 2\left(\frac{f}{f_T}\right)^2 R_iT_d/R_{ds} \quad \text{[K]} \tag{2.26}$$

In the frequency range where $\frac{f}{f_T} \ll \sqrt{\frac{T_gR_{ds}}{T_dR_i}}$ it reduces to

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{T_dT_gR_i/R_{ds}} \qquad \text{[K]}. \tag{2.27}$$

The model temperatures scales down accordingly with operation at cryogenic temperatures. Typically, the gate temperature $T_g \approx T_a$, which reduces the model to one unknown parameter. The drain temperature, T_d, also reduces

at low temperatures, but not to the same extent as T_g. This supports the assumption that the gate noise is not directly induced by the drain noise.

Noise temperature extraction and validity

An algebraic method for treating temperature based noise models has been developed [44] and utilised to derive direct extraction methods for the one parameter [45] and two parameter [46] Pospieszalski model. The effect of parasitic resistances at ambient temperature, T_a, is taken into account when calculating the intrinsic contributions T_g and T_d. The two parameter model requires two measurements of noise figure at the same frequency, but with different source impedance, while for the one parameter counterpart a single noise figure measurement is enough.

An assertion of the model validity can be made if accurate measured values of G_{opt}, R_n and T_{min} are available, with the inequality of (2.28) satisfied at all frequencies of interest.

$$1 \leq \frac{4G_{opt}R_nT_0}{T_{min}} < 2 \tag{2.28}$$

2.2.8 Resistive FET mixers

In addition to the small-signal application of FETs as amplifiers, it might also be operated in a large signal manner, which includes frequency translation. A FET mixer can utilise either the nonlinear resistance (resistive mixer) or the nonlinear transconductance (active mixer) of the transistor [1]. In either mode, the mixer operates by applying a local oscillator (LO) large signal at frequency f_{LO} to the gate terminal, which is typically biased close to the threshold voltage. As a consequence, the transistor switches between high and low transconductance or channel conductance, which yields waveform of $g_m(t)$ or $G_{ds}(t)$, respectively.

For a resistive mixer operation the RF signal is applied to the drain terminal [47]. This yields a multiplication according to $G_{ds}(t) \cdot V_{RF}sin(\omega_{RF}t)$. Since $G_{ds}(t)$ may be expressed as a Fourier series in f_{LO}, the product will contain $sin(\omega_{LO}t) \cdot sin(\omega_{RF}t)$, which can be rewritten as the sum $sin((\omega_{RF} + \omega_{LO})t) + sin((\omega_{RF} - \omega_{LO})t)$. The desired intermediate frequency, f_{IF}, is either the sum or difference depending on whether an up- or down-conversion is performed. The included frequencies and relative power levels are illustrated in Figure 2.9. A mixer is defined to be either single-sideband (SSB) or double-sideband (DSB) depending on whether it converts RF signals on only one side-band relative to the LO or both. This defines the image frequency f_{IM} which might result in an unwanted response the same as from f_{RF} for a DSB mixer.

Since the resistive mixer is a passive component it always results in a conversion loss (CL) as defined by

$$CL = \frac{P_{RF}}{P_{IF}} > 1 \qquad \text{[dB]}. \tag{2.29}$$

For a resistive mixer it is valid that $CL \propto 1/(\Gamma_{max} - \Gamma_{min})$ [48]. The proportionality constant depends on the wave shape of $G_{ds}(t)$, with a square wave of 50 % duty cycle the most favourable. On the other hand, the noise figure is generally lower than that of a diode mixer with the same conversion loss. The

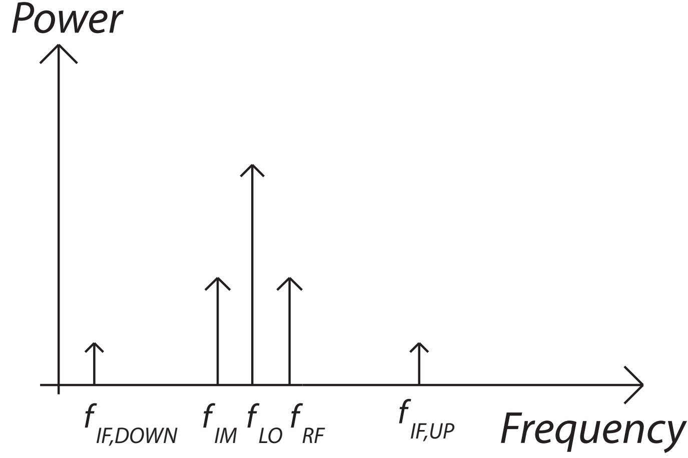

Figure 2.9: Spectra and relative powers in a mixer frequency translation. The frequencies are related as; $f_{IF,DOWN} = f_{RF} - f_{LO}$ and $f_{IF,UP} = f_{RF} + f_{LO}$. Ideally the image frequency, f_{IM}, yields the same output as the RF frequency, f_{RF}.

reason is the absence of shot noise when the gate leakage current is low. This makes the attenuator noise model [27]

$$T_{SSB} = T_a \cdot (CL - 2) \qquad [\text{K}], \tag{2.30}$$

where T_a is the ambient temperature, a suitable choice for a resistive mixer.

The most convenient mixer noise figure definition is different from (2.7) and given by

$$F_{SSB} = 2 + \frac{T_{SSB}}{T_0} \qquad [\text{dB}], \tag{2.31}$$

which yields $F_{SSB} = CL$ at room temperature where $T_a = T_0$, as verified experimentally in [47]. It also conserves the property that $F_{DSB} = F_{SSB}/2$ just like $T_{DSB} = T_{SSB}/2$, assuming exactly equal sideband loss.

2.3 Graphene

Graphene consists of a single-layer of carbon atoms organised in a honeycomb lattice, Figure 2.10a. The thickness is $d \simeq 0.3nm$, making it a truly 2D material, and the lattice constant is $a = 1.42$ Å. It is the basic building block of graphite flakes, which consists of several millions of graphene layers stacked on top of each other. Often, two layers are referred to as bilayer graphene, while without a prefix the underlying assumption is that of a single layer.

The electronic properties of graphene are found by solving the Dirac equation, rather than the Schödinger equation. The result for large area graphene shows a zero bandgap semiconductor, semimetal. It has conical (linear if restricted to a plane) conduction and valence bands crossing at points called Dirac points. As a consequence, the carriers close to the Dirac point have *zero* mass. By limiting the width of graphene in one dimension a nanoribbon is formed, in

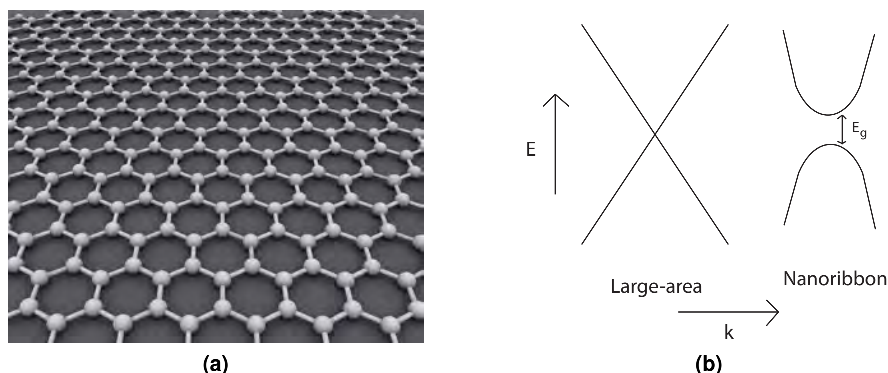

Figure 2.10: (a) Honeycomb crystal structure of a graphene sheet. (b) Dispersion relation close to the Dirac-point of a large-area graphene flake and a nanoribbon [14].

which a measurable bandgap can be detected with a size up to 200 meV [14], although the band curvature results in a higher carrier mass. The two cases are reproduced in Figure 2.10b.

2.3.1 Electronic properties

The potential for manufacturing high frequency, microwave and possibly terahertz range, field effect transistors from graphene stem from its high intrinsic mobility and saturation velocity. The utilisation of these properties are hindered by the choice of substrate and top gate dielectric, which yields lower extrinsic values. A unique property of graphene is that the electron and hole mobilities are very similar, whereas other semiconductors typically have $\mu_e >> \mu_h$ [30].

Mobility and saturation velocity

The predicted intrinsic room temperature mobility of graphene for a carrier density of $10^{12} cm^{-2}$ range from 100,000 $cm^2V^{-1}s^{-1}$ in [49] to 200,000 $cm^2V^{-1}s^{-1}$ in [50], as limited by the acoustic phonons of the graphene lattice. On the other hand, for graphene on SiO_2, the main scattering mechanism for carriers is from charged impurities introduced by the substrate, so called Coulomb scattering [51], which limits the maximum mobility of graphene on SiO_2 to about 10,000 $cm^2V^{-1}s^{-1}$ [52]. Comparing with reported experiments, by entirely removing the effect of the substrate a mobility of 100,000 $cm^2V^{-1}s^{-1}$ has been measured for suspended graphene [14].

Replacing SiO_2 ($\kappa \simeq 4$) with a high-κ dielectric screens the charged impurities, promising higher extrinsic mobility [52]. This is also the case for low temperatures where a fourfold improvement is possible. At room temperature, on the other hand, an additional scattering mechanism is introduced, surface-optical (SO) phonon scattering, which erases the improvement. Nevertheless, choosing AlN or SiC (intermediate-κ dielectrics) mobilities of about 15,000 $cm^2V^{-1}s^{-1}$ can be attained. Another possibility which has been successfully explored to achieve a higher mobility is atomically flat BN, where values of 25,000 $cm^2V^{-1}s^{-1}$ have been demonstrated [21].

A comparison with the conventional FET materials in Table 2.1 shows that graphene clearly has an advantage with respect to mobility. Furthermore, it is not only the substrate, but also the top gate dielectric of a graphene FET which affects the mobility, which is treated in Section 2.4.

Concerning the saturation velocity, theoretical studies suggest that for graphene the intrinsic v_{sat} can reach values of $4 \cdot 10^7 cm/s$ [14]. The peak is not as distinct as for III-V semiconductors, whereby the high carrier velocity is maintained for higher fields, making it yet more favourable compared to the materials in Table 2.1. Furthermore, an experimental study for graphene on SiO_2 indicate that the saturation velocity is highly carrier density dependent, varying in the range of $1 - 2 \cdot 10^7 cm/s$, which again suggests the substrate to be limiting the performance of graphene in FETs [53].

Residual carrier density

Since graphene does not have a bandgap, a FET channel is impossible to turn off, due to thermally generated carriers, where $n_{th} = 8 \cdot 10^{10} cm^{-2}$ at room temperature. These carriers provide a non-zero conductivity even at the Dirac point, which is the point of minimum conductivity. Measured conductivity for graphene on SiO_2, though, has shown that an additional parameter is required in order to explain the behavior at the Dirac point, usually referred to as the residual carrier density, n_0 [54]. These carriers are supplied by the aforementioned charged impurities, which form electron-hole puddles in the graphene layer. The available residual carrier density at the Dirac point lies typically in the range $n_0 = 10^{11} - 10^{12} cm^{-2}$, depending on the cleanliness of the sample.

2.4 Graphene Field Effect Transistors

Graphene field effect transistors (G-FETs) are categorised as MOSFETs, where the gate controls the channel conductivity via the capacitance of an oxide or dielectric. In addition to the persuasive mobility and saturation velocity of graphene as an intrinsic material, the most distinctive property is the ability to have both electron (n-channel) and hole (p-channel) conduction in the same device [13], as illustrated in Figure 2.11a.

2.4.1 DC characteristics

The simple model of (2.32) [55] may be used to fit the electron and hole branches of the channel resistance, in order to have a quantitative understanding how the different parameters influence the device behavior.

$$R_{ds} = 2R_c + \frac{L}{Wq\mu_{e,h}\sqrt{n^2 + n_0^2}} \qquad [\Omega] \tag{2.32a}$$

$$n = \frac{C_{gate}(V_{gate} - V_{dirac})}{q} \qquad [cm^{-2}] \tag{2.32b}$$

$$C_{gate} = \left(\frac{1}{C_{ox}} + \frac{1}{C_q}\right)^{-1} \qquad [F/cm^2] \tag{2.32c}$$

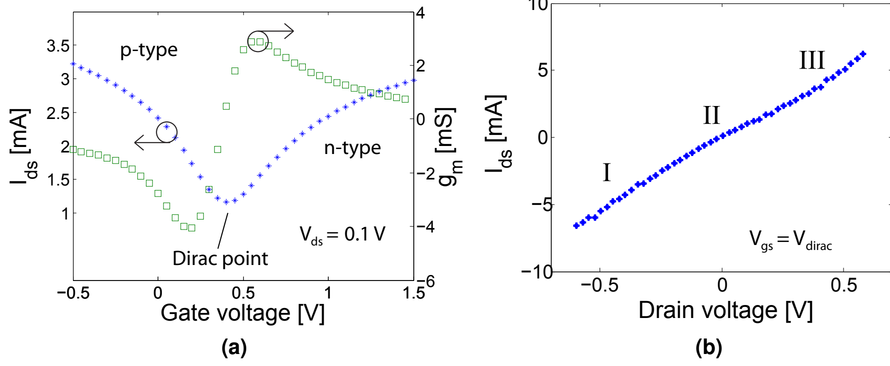

Figure 2.11: (a) Typical G-FET transfer characteristic and transconductance, with a change from electron to hole conduction at the Dirac point. (b) G-FET output characteristics with onset to current saturation and a second linear region.

The on-off ratio is influenced by mainly two parameters, the residual carrier density for the off-state, n_0, and the contact resistance, R_c, for the on-state. Furthermore, the slope is determined by the the carrier mobilities, $\mu_{e,h}$, and the gate capacitance per area C_{ox} $[F/cm^2]$. One should be careful in defining $C_{gate} = C_{ox}$ except when $C_{ox} << C_q$, the quantum capacitance of graphene [56].

The characteristic of Figure 2.11 illustrates also two unwanted phenomena in G-FETs. Firstly, the Dirac point is shifted away from $V_{gate} = 0$ V, which is attributed to unintentional doping of the graphene layer during the fabrication process. Secondly, there is an asymmetry of the electron and hole sides of the transfer characteristic around the Dirac point. This is caused by charge transfer from the metal contact to the graphene channel [57], which is minimised by a proper choice of contact metalisation. The extra resistance originates from pn-junction formation at the channel ends closest to the contacts.

2.4.2 Performance bottlenecks

As has already been outlined in Section 2.4.3, the intrinsic potential for graphene in amplifier applications is high, while the extrinsic performance is still limited by the high contact resistances and mobility degradation from substrates and top-gate dielectrics.

Contact resistance

The high sheet resistivity ρ_s $[\Omega/\square]$ of graphene, particularly close to the Dirac point where the density-of-states (DOS) is low [57], yields a large contact resistance, $R_c = R_A + R_{m-g}$. The access resistance, $R_A = \frac{L_A}{W_A}\rho_s$, originates from the ungated region between contact and channel and R_{m-g} from the metal-graphene interface. Experimental investigation of different metalisations [57] and simulations to understand the metal-graphene interface [58] has been conducted in order to develop a process that provides good ohmic contacts. Theoretical considerations suggest doping the graphene under the contact, but still no reliable doping process has been presented.

Table 2.2: Reported resistivities of several different contact metallisation stacks on single-layer graphene. Values are given as R_cW [$\Omega\mu m$] (* self-aligned structure).

Metal	Ni [57]	Ti/Au [60]	Cr/Au [57]	Ti/Pd/Au [18]	Ti/Pd/Au* [59]
R_cW	1,000	800	10,000	600	540*

It has been shown that the current transfer from metal to graphene occurs only at the edge of the contact [57]. Thus R_{m-g} scales with the width of the contact rather than the area and the correct measure of contact resistivity is R_cW in [$\Omega \cdot \mu m$], where W is the contact width. Available values of contact resistivity for single-layer graphene are presented in Table 2.2. In order to reach the level of established technologies, the contact resistivity needs to be reduced an order of magnitude [57]. Reducing the access region distance makes R_A less detrimental, where a self-alignment process is the limiting case [59], while another option is to dope also the access part to reduce ρ_s.

Mobility degradation from top-gate dielectric

The first G-FET with a top-gate, where the graphene channel is sandwiched between two dielectric materials, used SiO_2 [61]. The mobility degradation was severe, almost ten times, after the formation of the top-gate. Several alternative dielectrics have been suggested since, whereof a handful from literature are presented in Table 2.3, together with extracted carrier mobility. For completeness, the dielectric constants, κ, of the gate dielectrics or achieved gate oxide capacitance are stated where reported, which relates to the possibilities of having a high g_m .

High κ-dielectrics are typically grown by atomic layer deposition (ALD), after natural oxidation of a thin nucleation layer [55, 62]. Exfoliated graphene on SiO_2 is used in all examples of Table 2.3, except one sample on hexagonal boron nitride (hBN), which is back-gated with the gate recessed under the gate dielectric [63]. Using a proper choice of top-gate dielectric and deposition method the maximum mobility value for graphene on SiO_2 is approached. Regarding, hBN a bilayer BN/graphene/BN device has shown a mobility of 15,000 $cm^2/(Vs)$ [64] and further development is required to reach the promising values in [21] for single-layer device channels.

Table 2.3: Top-gate dielectrics produced by; a) ALD b) Natural oxidation c) PECVD d) Exfoliation. Relative dielectric constants refer to the thin gate dielectric films. All data refer to exfoliated single-layer graphene in FET channels.

Dielectric	μ [$cm^2/(Vs)$]	κ	C_{ox} [$\mu F/cm^2$]
SiO_2 [61]	700	-	-
Al_2O_3 $^{a)}$ [55]	8,600	6.4	0.3
Y_2O_3 $^{b)}$ [65]	5,400	10	1.5
HfO_2 $^{a)}$ [62]	$<$ 5,000	15	-
Si_3N_4 $^{c)}$ [66]	3,800	4.4	-
hBN ^{d} [63]	3,300	-	-

2.4.3 State-of-the-art RF devices

Single-layer graphene material can be prepared using several different methods, including chemical vapor deposition (CVD), thermal decomposition of SiC and mechanical exfoliation from natural graphite. The different methods yields varying quality, specifically regarding mobility and homogeneity of the material.

Thus far, the suitability for electronics is largest for exfoliated graphene where a transistor channel mobility on the order of 8,000 $cm^2/(Vs)$ has been extracted [55]. In addition, an intrinsic cutoff frequency f_T = 300 GHz for a gate length L_g = 144 nm, is achieved using exfoliated material [15]. The most commonly used substrate for exfoliated graphene is 300 nm SiO_2 on a Si wafer, which facilitates optical confirmation of the number of layers via the reflectance of green light [67], as can be seen in Figure 2.13. The drawback of exfoliated graphene is the scalability, as the largest flakes measure 10 $\times$ 30 μm^2.

Graphene may be grown by CVD techniques on a metal, such as nickel or copper. The advantages include large scale production and subsequent transfer to a wide variety of substrates, not limiting it to SiO_2. The mobilities for CVD graphene grown on Ni and Cu are in the range of 1,000 $cm^2/(Vs)$ [68] and 4,000 $cm^2/(Vs)$ [69], respectively. Recently, a cutoff frequency (intrinsic), f_T = 300 GHz for a gate length L_g = 40 nm, has been achieved using graphene grown on copper by this method [16].

Finally, epitaxially grown graphene exhibit mobilities up to 3,000 $cm^2/(Vs)$ on the Si face, whereas a cutoff frequency (intrinsic), f_T = 350 GHz for a gate length L_g =40 nm, has been reported [16].

The discrepancy between above mentioned intrinsic values and the extrinsic counterparts is still large. This is attributed mainly to the high contact resistances, even if the parasitic pad capacitance influences according to (2.20). The highest reported extrinsic cutoff frequency, f_T = 55 GHz, is achieved using CVD grown graphene on a glass substrate [70]. Otherwise, typical extrinsic f_T are in the range 10-20 GHz [16, 63, 66].

Recently, the correspondingly reported values of (de-embedded) f_{max} have increased with the ratio $f_{max}/f_T \approx 1$ at longer gate lengths [20]. The best reported value for the CVD graphene transistors is f_{max} = 44 GHz at L_g = 140 nm [16]. Moreover, graphene on SiC can reach f_{max} = 42 GHz at L_g = 140 nm. The achievement of current saturation, higher R_{ds}, and realisation of a low gate resistance, R_g, are important to improve f_{max}, according to (2.23).

A comparison of the intrinsic high frequency performance of graphene FETs, where both figure-of-merits were given, with mature CMOS and HEMT technologies is presented in Figure 2.12. In summary from literature, there is still a huge gap for G-FETs to bridge, especially in f_{max} but also in extrinsic f_T.

Frequency translation applications

The applications of G-FETs have been mainly limited to frequency multiplication [19], fundamental [17] and subharmonic resistive [18] mixing. The latter operates by biasing the G-FET at the Dirac point and applying an LO signal at f_{LO} to the gate. The resulting time varying drain to source resistance is at $2f_{LO}$. The multiplication with an RF signal at f_{RF} achieves a down-conversion to the intermediate frequency at $f_{IF} = |f_{RF} - 2f_{LO}|$. A state-of-the-art CL of 24 dB for G-FET mixers is accomplished by this method.

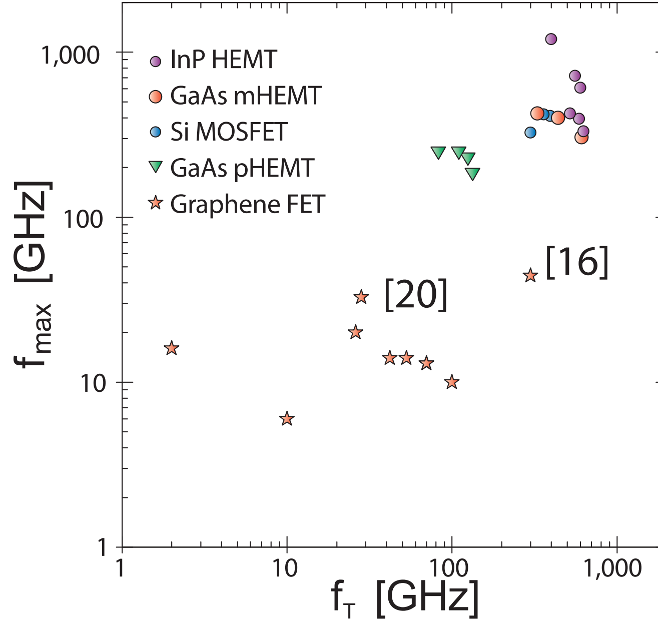

Figure 2.12: Intrinsic performance of G-FETs, where both f_T and f_{max} data were readily available, versus mature CMOS and HEMT technologies [16, 20, 71].

Small-signal power amplifier

The electron, hole duality of graphene is a fundamental requirement for the subharmonic mixer in [18], but it is a limitation in designing a small-signal amplifier. Again from Figure 2.3b small-signal gain requires a high g_m and a low g_d. For conventional, unipolar n-channel FETs operation in the current saturation regime assures a low g_d, while an appropriate V_{gs} yields a high g_m.

In G-FETs, on the other hand, g_m is not monotonically increasing with V_{gs}, but instead has well-defined max and min with a zero at the Dirac-point. Changing the drain bias shifts the peaks in g_m, which makes a G-FET operating at optimum transconductance to exhibit weak current saturation, as investigated also in [63]. To maximise g_m, the off-state must be distinct via a low n_0, while R_c must be minimised to have $g_{me} \approx g_{mi}$, from (2.17). Typically, as in Figure 2.11b, a G-FET enters a second linear regime in the output characteristics as the channel changes from one carrier type (region I), to pinch-off (region II) and finally to the other carrier type (region III). As a consequence of (2.15), the reported values in the literature are $|S_{21}| < 1$, with one occurrence of gain, e.g. $|S_{21}| > 1$ in [20].

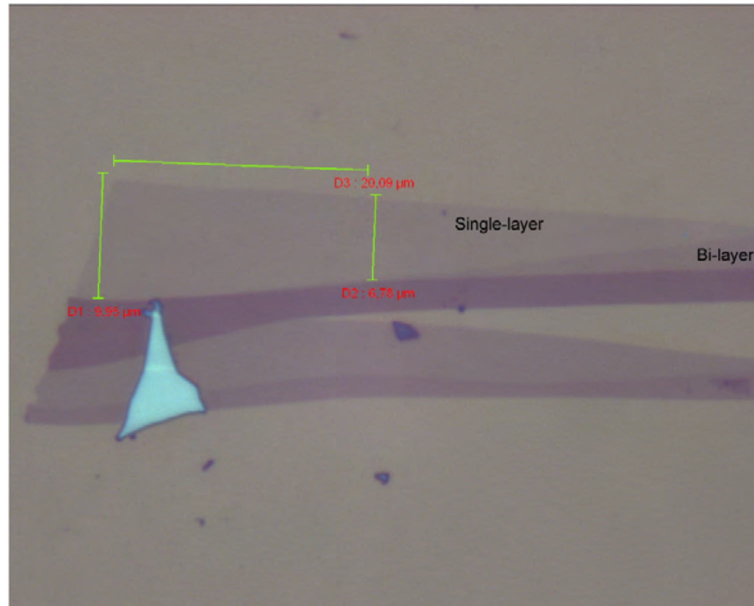

Figure 2.13: Illustration of the optical recognition of single-layer graphene from the bi-layer dito on chip after mechanical exfoliation for a relatively large flake.

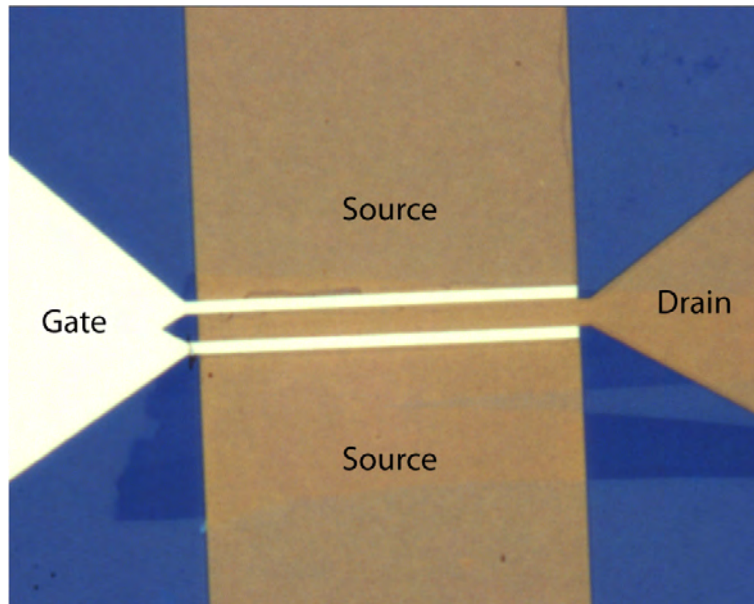

Figure 2.14: The same flake with a two-finger 60 μm wide, 1 μm gate length G-FET on top. The graphene is visible as a difference in nuance under the drain and source pads, which are covered by Al_2O_3, while the gate pad is on top of the oxide.

Chapter 3

Method

This chapter introduces the principles used in the manufacturing, characterisation, parameter extraction and modelling of the G-FETs and applications.

3.1 Fabrication

The manufacturing procedure is described in steps I-V below, each with an associated cross-sectional illustration shown in Figure 3.1.

I. Exfoliation of graphene on 300 nm SiO_2 from natural graphite, see Figure 2.13, which ensures a uniform and high quality material. The substrate limited mobility is still comparable to available synthesized graphene.

II. Electron beam lithography (EBL) patterning of drain and source contacts, using double resist layers consisting of MMA EL10 (500 nm) and ZEP520 1:1 Anisole (150 nm) to facilitate lift-off of metal evaporated by e-gun. A metal stack of Ti/Pd/Au (1 nm/15 nm/60 nm) is used, as motivated by the compilation in Table 2.2 to have low contact resistivity of 600 $\Omega \mu m$. The thin layer of Ti is used for adhesion only, while Pd is beneficial to have a small charge transfer and symmetric transfer characteristics.

III. Allover electron beam evaporation of metal and subsequent oxidation on a hot-plate. Usually 3 times 2 nm aluminum to form an Al_2O_3 oxide, which compares well in Table 2.3, with an approximate final thickness of 8 nm. This yields a gate oxide capacitance $C_{ox} \approx 0.5$ $\mu F/cm^2$ and results in mobilities for both electrons and holes $\mu \approx$ 2,000 $cm^2/(Vs)$.

IV. EBL patterning of a gate electrode, metallisation by e-gun evaporation and lift-off. Similar to drain and source consisting of Ti/Pd/Au, but with a metal thickness increased to 0.5 μm (MMA EL10 thickness increased to 1 μm) for amplifier applications to have a lower gate resistance, R_g, and thus improve noise performance. The access distances from gate electrode to drain/source pads are 100 nm, which is close to self-aligned. The gate length is $L_g = 1$ μm to have efficient channel modulation and thus as high transconductance, g_m, as possible, despite the large contact resistances.

V. Removal of oxide on top of contact pads with a wet etchant consisting of HF (buffered oxide etch). A resulting G-FET is shown in Figure 2.14.

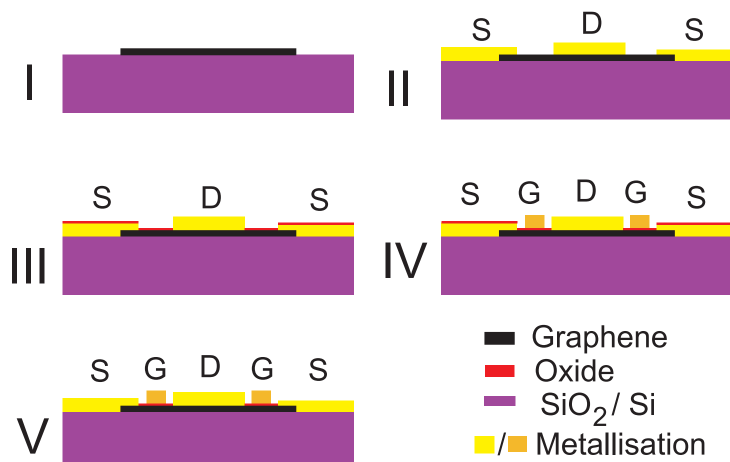

Figure 3.1: Step-by-step fabrication of a G-FET, described in detail in Section 3.1.

3.2 Amplifier design

To design a small-signal amplifier with the fabricated G-FET, the S-parameters in Figure 3.2 were measured at $V_{gs} = 0.25$ V and $V_{ds} = -\ 1.25$ V (see Figure 4.1). The device exhibits extrinsic $f_T = 5$ GHz and $f_{max} = 7$ GHz from Figure 3.6. A design frequency of 1 GHz was chosen and the conventional design method in [31] was utilised. Calculating the stability parameters from the S-parameters the G-FET is unconditionally stable, with stability factor $K > 1$ and stability measure $b > 0$. Thus any source- and load reflection coefficients, Γ_s and Γ_L respectively, can be presented without the risk of oscillations. The approach of a unilateral design was disregarded, since the estimated error of about 1 dB was considered unacceptable. Due to the low frequency, S_{11} is close to open and the largest gain improvement is achieved by matching at the input. Consequently, the available power gain, G_A, circles [72] are the logical starting point, as illustrated in Figure 3.3, where $G_{A,max} \approx 10$ dB at $\Gamma_{M,s} = 0.9\angle 29\,°$.

At 1 GHz on a Si substrate, $\varepsilon_{Si} = 11.7$, matching stubs are impractically long since $\lambda_{TEM} \approx 8.8\ cm$. This motivates lumped matching networks, used in combination with coplanar waveguide (CPW) transmission lines. Clearly, from Figure 3.3, a single series inductor is enough to match the input and enhance the gain substantially. With the available inductance values (Coilcraft 0402CS series) $L = 36$ nH was chosen, which corresponds to the source reflection coefficient $\Gamma_s = 0.9\angle 23\,°$ in Figure 3.3. The predicted available power gain is consequently $G_A \approx 9$ dB, where the uncertainty originates from the specified inductor tolerance of 5 %. The actual amplifier gain is the transducer power gain, $G_T = |S_{21}|^2$ [dB]. To have $G_A = G_T$ the output of the transistor must be conjugately matched, as $\Gamma_L = \Gamma_{out}^* = 0.3\angle 54\,°$. Keeping the output at 50 Ω, the gain is $G_T \approx G_A - 0.5$ dB. Consequently, having a simple circuitry with easy DC biasing is prioritised over an otherwise small gain improvement.

A photo of the resulting amplifier, with a soldered inductor on the gate, is shown in Figure 3.4 with the G-FET encircled and presented in Figure 3.5.

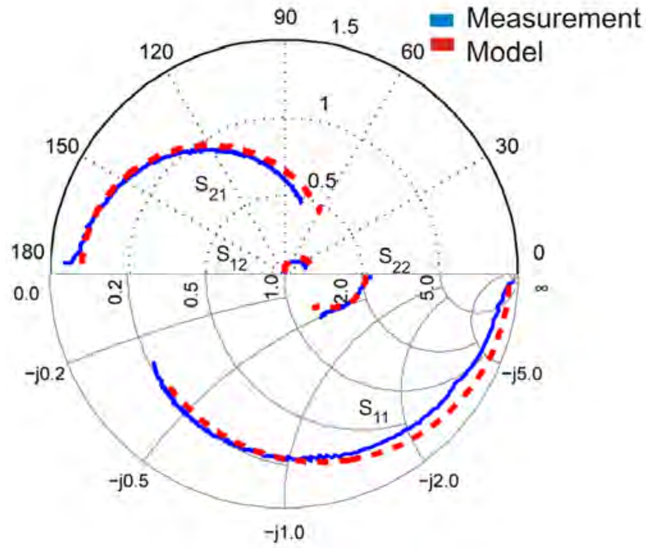

Figure 3.2: Measured and modelled G-FET S-parameters from 10 MHz to 10 GHz at the bias point $V_{gs} = 0.25$ V and $V_{ds} = -1.25$ V. Importantly, small-signal power gain with 50 Ω terminations is possible for $f \leq 3.3$ GHz.

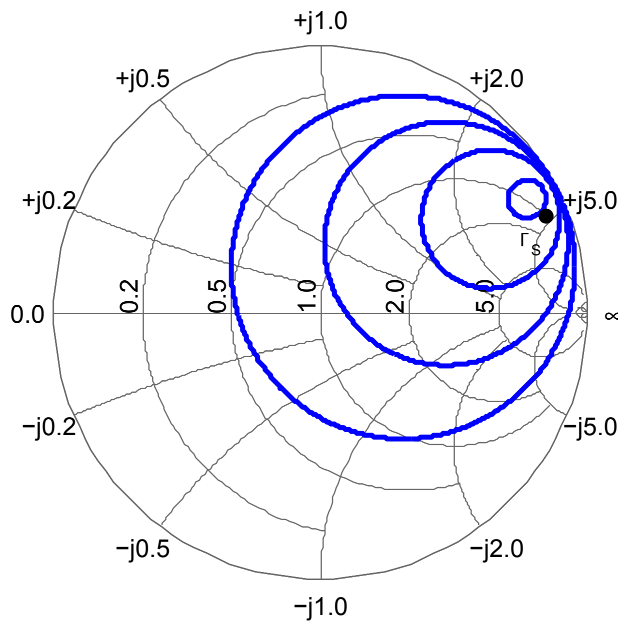

Figure 3.3: Available gain circles of the G-FET from 0.1 dB to 9.1 dB in steps of 3 dB, while $G_{max} \approx 10$ dB. The chosen source reflection coefficient, Γ_s, is also included.

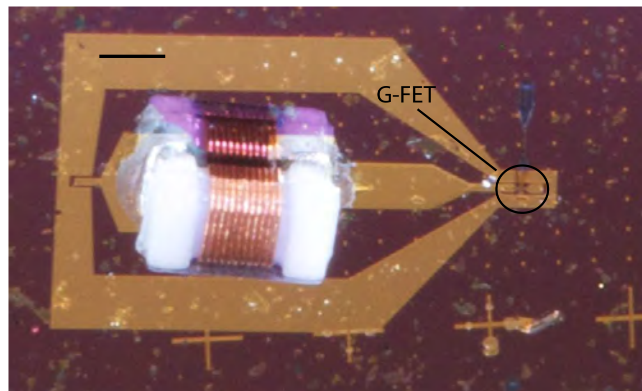

Figure 3.4: Photo of the manufactured amplifier, including the CPW transmission lines, the soldered inductor and the G-FET. The scale bar is 400 μm.

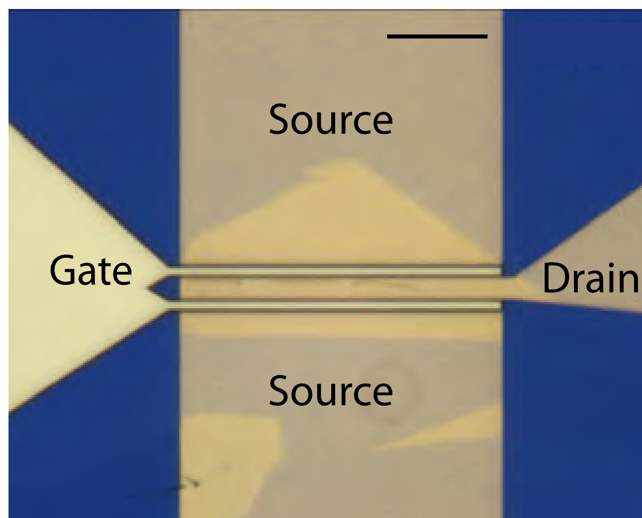

Figure 3.5: Close-up photo of the fabricated G-FET, with the graphene flake clearly visible underneath the drain and source contact pads. The gate length is 1 μm and the channel width is 60 μm divided equally in two fingers. The scale bar is 10 μm.

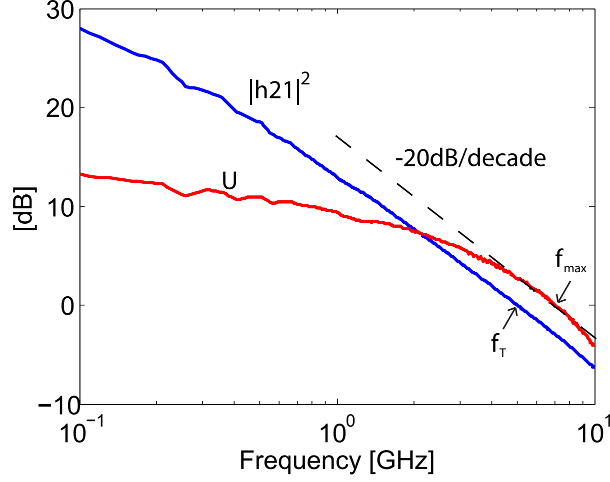

Figure 3.6: Derivation of extrinsic f_T and f_{max} from measured S-parameters for the G-FET at the bias point of $V_{gs} = 0.25$ V and $V_{ds} = -1.25$ V.

3.3 Noise measurements - the Y-factor method

The Y-factor method is a relative measurement technique utilising a cold and a hot load, presenting noise temperatures T_C and T_H, respectively. The resulting output powers from the device under test (DUT), with unknown input noise temperature T_n, are thus calculated as $P_{LC} = k\Delta f G(T_C + T_n)$ and $P_{LH} = k\Delta f G(T_H + T_n)$. The ratio is defined as the Y-factor and given by

$$Y = \frac{P_{LH}}{P_{LC}} = \frac{T_H + T_n}{T_C + T_n} \qquad [-], \tag{3.1}$$

from which the DUT input equivalent noise temperature is calculated as

$$T_n = \frac{T_H - YT_C}{Y - 1} \qquad [\mathrm{K}]. \tag{3.2}$$

Typically, a standard termination at $T_0 = 290$ K is used, while the other can have either a lower or higher temperature depending on the DUT noise temperature, since for best accuracy the difference should be $T_H - T_C \approx T_n$ [27]. For some measurements a cold load at liquid nitrogen temperature, $T = 77$ K, is sufficient, but for higher noise temperatures commonly diode noise sources are used as a hot load. These are specified with their excess noise ratio (ENR) defined in (3.3). Diodes with an ENR value of 15.2 dB are readily available.

$$ENR = 10 \cdot \log\left(\frac{T_n - T_0}{T_0}\right) \qquad [\mathrm{dB}] \tag{3.3}$$

Actual measured noise figure is the cascade of the corresponding quantities of the DUT and the receiver system used to measure the powers, according to the cascade formula

$$F_{meas} = F_{DUT} + \frac{F_{rec} - 1}{G_{DUT}} \qquad [\mathrm{dB}]. \tag{3.4}$$

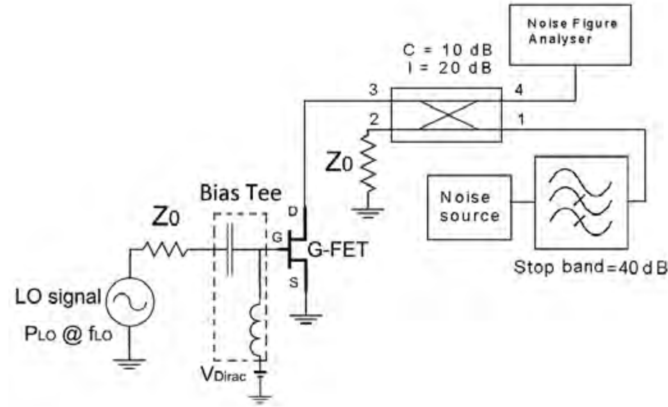

Figure 3.7: Schematic of the mixer noise measurement setup.

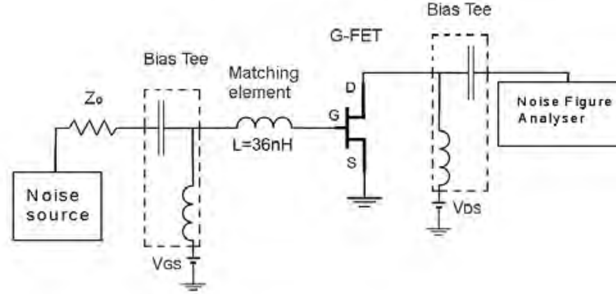

Figure 3.8: Schematic of the noise measurement setup used for the amplifier.

For a DUT with a high gain it is thus safe to assume $F_{DUT} \approx F_{meas}$, while otherwise a correction is required where F_{DUT} is solved from (3.4). This makes a simultaneous measurement of the DUT gain necessary, which in its most simple form is given by (3.5) [73]. The primed noise powers are measured with the DUT inserted, while the unprimed are the noise powers of the hot and cold sources themselves.

$$G_{DUT} = \frac{P'_H - P'_C}{P_H - P_C} \qquad \text{[dB]} \tag{3.5}$$

The complete procedure is implemented in a noise figure analyser (NFA), which calibrated with a commercial diode noise source, simultaneously displays gain and noise figure of a DUT.

The main uncertainties arises from mismatches of the DUT, quantified by S_{11} and S_{22}, which is especially deteriorative when the gain and noise figure are simultaneously low [74]. Furthermore, uncertainties arise from a high noise figure and mismatch of the NFA, as well as mismatch and ENR uncertainty of the noise source.

3.3.1 Noise measurement setups

The Y-factor and noise figure of the G-FET subharmonic mixer and amplifier were measured with an Agilent N8975A NFA and on-chip probing. The procedures are illustrated in Figure 3.7 and Figure 3.8. The mixer has a 1-18 GHz 10 dB directional coupler to separate the RF and IF signals at the drain. This setup uses also an additional low-pass filter with 40 dB attenuation in the stopband, to ensure good isolation and minimum leakage from the noise source to the NFA. A high ENR noise source, 15 dB ± 0.1 dB, is utilised to increase the Y-factor and thus decrease the measurement uncertainty in this case.

3.4 Modelling of G-FETs

This section starts with the procedures in large- and small-signal modelling of G-FETs and continues with its utilisation in noise figure modelling.

3.4.1 Parameter extraction

There are some major differences in the large- and small-signal modelling of G-FETs compared to other FETs, arising from the fact that graphene is a zero bandgap material. First, since the device has no pinch-off the cold-FET method needs modification and, secondly, the duality in electron-hole transport must be considered for a DC model. The relevant procedures are outlined below, as adapted from the semi-empirical large signal model proposed in [75].

The model presents a single closed-form expression for $I_{ds}(V_{gs})$, predicting both the difference in mobilities and asymmetry for electrons and holes, given μ_e, μ_h, R_c, R_{ext}, n_0 and C_{ox}. Especially, if $|V_{ds}/V_{gs}| \ll 1$ and $|V_{ds}/V_{gd}| \ll 1$, the expressions simplifies such that the total drain to source resistance may be expressed according to

$$R_{ds} = 2R_c + 2R_{ext} + \frac{\alpha_{\mu_e}}{1 + (V_{gs}/V_0)^2} \qquad [\Omega], \tag{3.6}$$

for $V_{gs} \gg V_{dirac}$ and

$$R_{ds} = 2R_c + \frac{\alpha_{\mu_h}}{1 + (V_{gs}/V_0)^2} \qquad [\Omega], \tag{3.7}$$

for $V_{gs} \ll V_{dirac}$, assuming hole doping of the channel from the contacts. Since $\alpha_{\mu_{e,h}} = L/(W\mu_{e,h}qn_0)$, $V_0 = qn_0/C_{ox}$ and $C_{ox} = (C_{gs} + C_{gd})/(LW)$ all parameters are extracted by curve fitting once the intrinsic capacitors are known. These are found from de-embedded S-parameters of the G-FET.

To find the parasitic components of Figure 2.5, S-parameters of separate and identical open- and short structures without graphene channel [15] are measured, which enables the extraction of the pad capacitances and pad inductors plus the gate resistance, respectively, according to Figure 3.9. The components of the open structure (Figure 3.9a) are found by identifying it is a π-network, while the short structure components (Figure 3.9b) are organised as a T-network, with the capacitors removed. The major part of the contact resistances, R_s and R_d, are due to the metal graphene interface and access resistances (Section 2.4.2) and are thus not correctly given by the short structure values R_s' and R_d', but instead found from (3.7) with $R_s = R_d = R_c$.

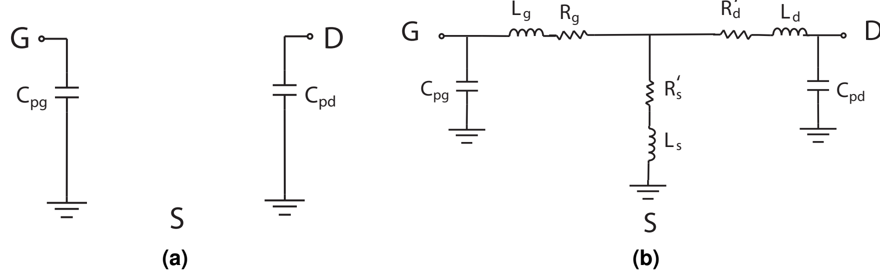

Figure 3.9: (a) Open structure small-signal circuit, where the gate-drain parasitic capacitance, C_{pgd}, is neglected. (b) Short structure small-signal circuit, where R'_s and R'_d are the metal contributions to R_s and R_d.

The expressions of (3.8) apply to the elements of the open structure.

$$Im(y_{11}) = \omega C_{pg} \qquad [S] \tag{3.8a}$$
$$Im(y_{22}) = \omega C_{pd} \qquad [S] \tag{3.8b}$$

The expressions of (3.9) apply to the elements of the short structure.

$$z_{11} = R'_s + R_g + j\omega(L_s + L_g) \qquad [\Omega] \tag{3.9a}$$
$$z_{12} = z_{21} = R'_s + j\omega L_s \qquad [\Omega] \tag{3.9b}$$
$$z_{22} = R'_s + R'_d + j\omega(L_s + L_d) \qquad [\Omega] \tag{3.9c}$$

3.4.2 Noise figure modelling procedure

The G-FET noise figure is measured when presented to a single Γ_s, while according to Section 2.2.5 the appropriate figure-of-merit for noise performance is F_{min}. In order to extract this quantity the one temperature Pospieszalski noise model was utilised, assuming $T_g = T_a$, as described in Section 2.2.7. The small-signal model of Figure 2.5 was used with the extracted component values presented in Table 3.1, which yields the modelled S-parameters in Figure 3.2. Several soldered inductors were measured to deduce the actual Γ_s, which differs slightly from the designed ideal inductor. Furthermore, for the noise analysis, the value of R_g includes $R_{series} = 5\ \Omega$ of the inductor with $Q \approx 44$ at 1 GHz. The remaining parameter T_d was extracted via a least square fit to the measured noise figures where the gain was $G_T > 5$ dB.

Table 3.1: Small-signal parameters for the G-FET noise model.

C_{ds}	C_{gs}	C_{gd}	g_m	R_g	R_i	R_{ds}
30 fF	0.5 pF	0.1 pF	56 mS	8 Ω	3 Ω	38 Ω
C_{pg}	C_{pd}	L_s	L_d	L_g	R_s	R_d
0.14 pF	10 fF	30 pH	50 pH	60 pH	17 Ω	17 Ω

Chapter 4

Results

This section presents the results divided into the two different applications considered for the G-FETs, in an amplifier and as a subharmonic resistive mixer. The former considers a novel G-FET amplifier and its noise performance by measurement and modelling [Paper A], while the latter considers a noise characterisation of the resistive mixer [Paper B].

4.1 G-FET small-signal amplifier

The DC characteristics of the fabricated device are presented in Figure 4.1 to illustrate the selected bias point, $V_{gs} = 0.25$ V and $V_{ds} = -1.25$ V. Small-signal parameters under these operating conditions for the G-FET are a transconductance value of $g_m = 22$ mS and an output conductance equal to $g_d = 10$ mS, which is not in optimum current saturation, as previously investigated in [63].

The associated S-parameters are presented in Figure 3.2 and clearly the device has small-signal gain when presented to 50 Ω impedances up to 3.3 GHz. Further, the fabricated amplifier exhibits a performance close to the designed value, with a discrepancy mainly attributed to the inductor tolerance of ± 5% and non-ideal Q $< \infty$. Most importantly, the resulting gain at 1 GHz is, from Figure 4.2, $G_T = 9.6$ dB which is slightly more than the designed value of $G_T \approx 8.5$ dB, while the overall maximum gain is 10 dB at 950 MHz. Thus, the fabricated amplifier has a source impedance closer to $\Gamma_{M,s}$. The related VSWR at both the input and output ports is low, as represented by $|S_{11}| < -10$ dB (Figure 4.3) and $|S_{22}| < -10$ dB at the design frequency. Finally, the reverse isolation is excellent with $|S_{12}| < -20$ dB. Also the modelled small-signal gain and return loss (RL)are plotted in Figure 4.2 and Figure 4.3, respectively.

In addition, the measured amplifier noise figure, as found in Figure 4.2, is 6.4 dB ± 0.4 dB at 1 GHz. The extracted frequency independent, Pospieszalski model equivalent drain temperature is $T_d = 23{,}100$ K. Since the measurement is done at room temperature the gate temperature is set to $T_g = T_a = 297$ K. The resulting modelled amplifier noise figure versus frequency is represented by the dashed line of Figure 4.2. The corresponding modelled G-FET noise figures, of the device itself as opposed to the amplifier circuit, are presented in Figure 4.4. As reference values, the estimated minimum extrinsic and intrinsic noise figures at 1 GHz are $F_{min,ex} = 3.3$ dB and $F_{min,in} = 1$ dB, respectively.

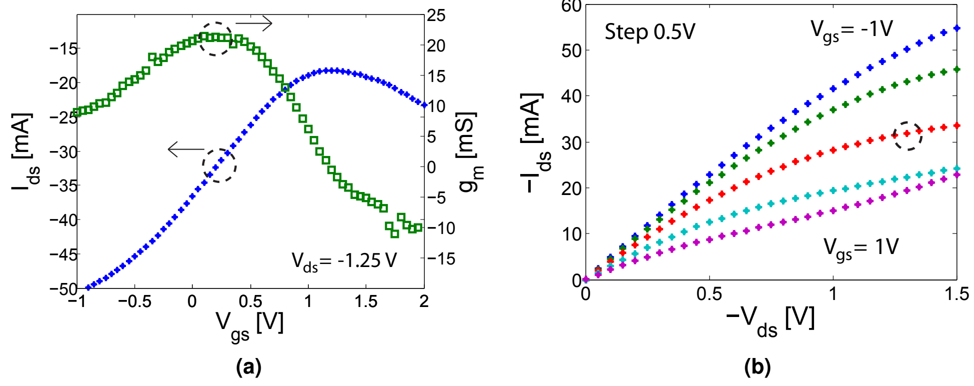

Figure 4.1: (a) Transfer characteristics and transconductance of the G-FET used in the amplifier at $V_{ds} = -\ 1.25$ V. (b) Output characteristics of the G-FET used in the amplifier from $V_{gs} = -1$ V (top) to 1 V (bottom). Dashed circles indicate the bias point used for the amplifier.

4.2 Noise of G-FET subharmonic resistive mixer

The fabricated G-FET mixer is operated at a gate bias of $V_{gs} = V_{dirac}$ and with zero drain voltage. Due to the thin gate dielectric a voltage swing of only $\pm$1V is required to sweep the transfer characteristics of Figure 4.5, corresponding to $P_{LO} = 0$ dBm in the 50 Ω system. Under these bias conditions there is an associated gate leakage current of $I_g < 20$ pA throughout the complete used voltage span, which is beneficial to keep the shot noise at a negligible level [27]. The symmetric transfer characteristics is important for the subharmonic mixing functionality. The small shift in the Dirac point assures little unintentional doping of the graphene layer from the contacts and is advantageous for the mixer to operate at zero gate voltage, where the leakage current is minimised.

The measured mixer single-sideband room temperature conversion loss and noise figure under these operating conditions are presented in Figure 4.6 versus RF signal frequency. The measurement frequency was set to $f_{IF} = 100$ MHz, double-sideband and a 3 dB correction applied to convert to single-sideband quantity. The conversion loss varies in the range 20-22 dB ($\pm$ 1 dB) throughout the complete frequency span, with a close relation to the noise figure. For verification, also the conversion loss measurement performed with the NFA was verified at $f_{RF} = 2$ GHz using a spectrum analyser.

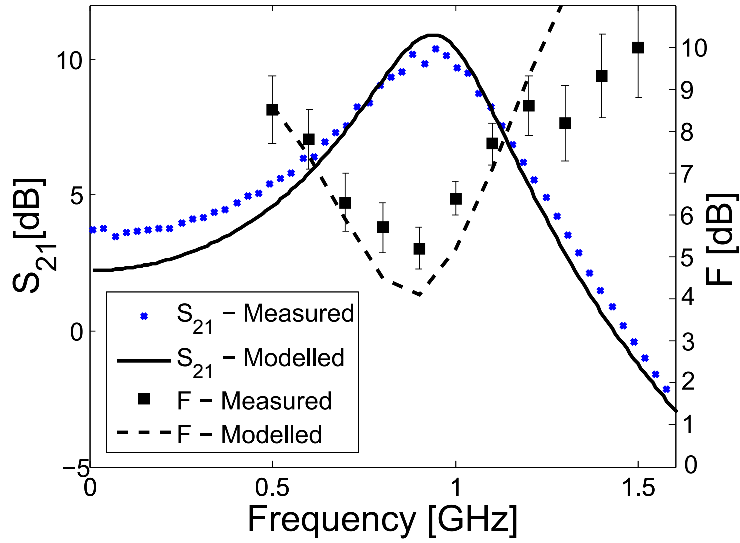

Figure 4.2: Measured and modelled gain for the amplifier from 10 MHz to 1.5 GHz. Measured and modelled noise figure of the amplifier from 500 MHz to 1.5 GHz.

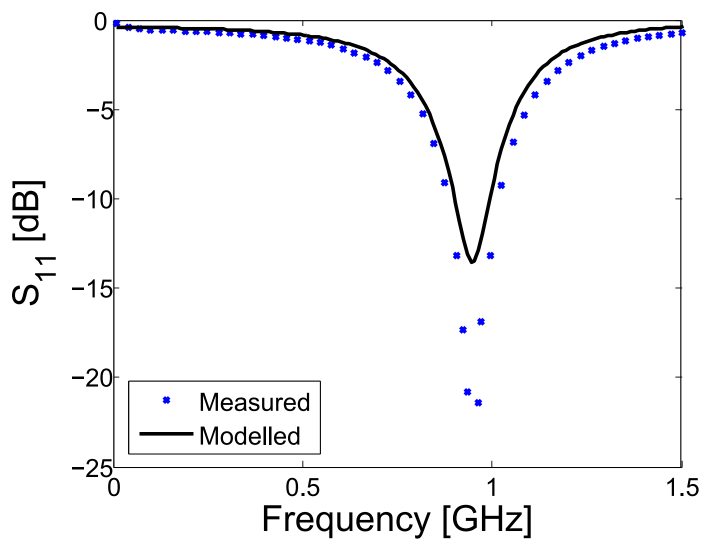

Figure 4.3: Measured and modelled return loss (RL) from 10 MHz to 1.5 GHz.

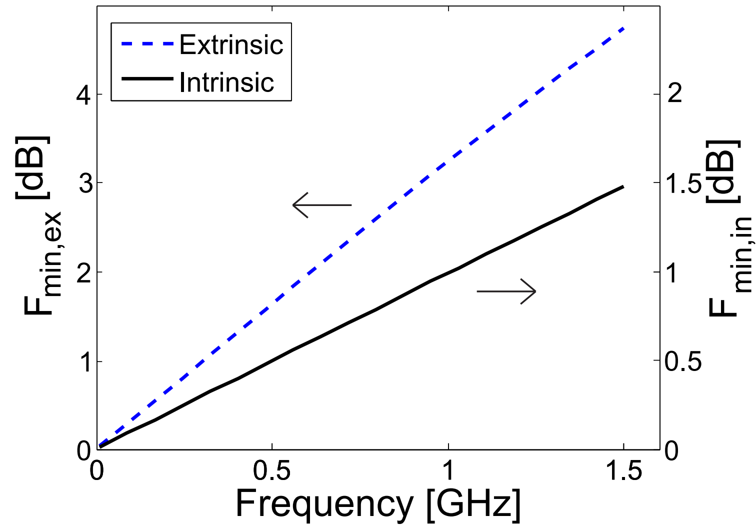

Figure 4.4: Minimum noise figure of the G-FET with and without parasitics from 10 MHz to 1.5 GHz calculated from Pospieszalski one temperature noise model [43].

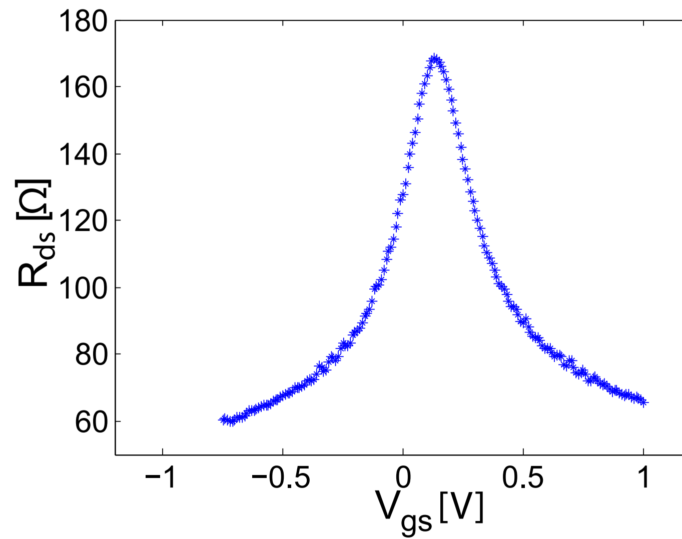

Figure 4.5: Drain to source resistance versus gate source voltage at $V_{ds} = 0.1$ V. This corresponds to the resistance swept by the LO in subharmonic mixer operation.

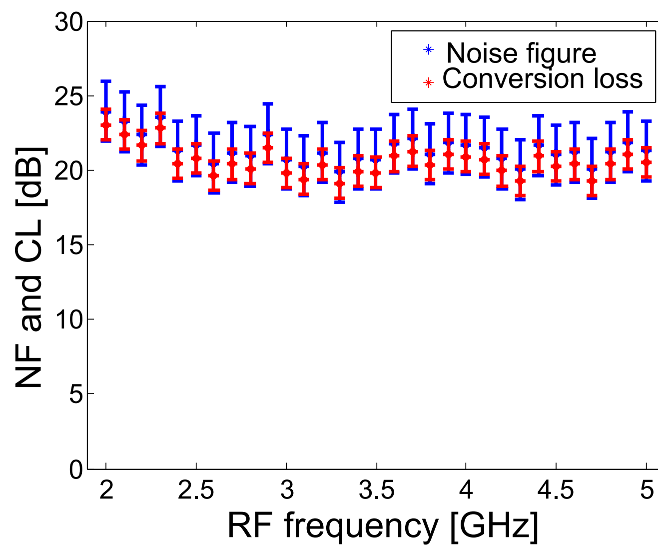

Figure 4.6: Measured conversion loss and noise figure for the G-FET the subharmonic mixer in the RF frequency interval f_{RF} = 2-5 GHz.

Chapter 5

Discussion and conclusion

This section initially discusses the G-FET performance in this thesis, compared to state-of-the-art GaAs and InP III-V HEMT technology and Si MOSFETs, as well as GaAs MESFET results. Finally, a conclusion of the work is drawn.

5.1 Discussion

Considering the subharmonic mixer, despite the measurement uncertainty, there is clearly a close relation with $F_{mixer,SSB,RT} \simeq CL$. According to the analysis in Section 2.2.8 the measured G-FET subharmonic mixer noise is thermal in its origin. Consequently, the most general route to lower noise figure is an improvement in conversion loss. This includes an increased on-off ratio, as well as the introduction of a bandgap in single-layer graphene to alter the shape of the time varying $R_{ds}(t)$. This yields a square wave shape with an increased off-state time, which is beneficial [48]. This is the case for HEMT mixers, where a GaAs HEMT fundamental resistive mixer achieves a conversion loss of 5.3 dB at $f_{RF} = 5$ GHz [48] and a subharmonic GaAs design 6.5 dB at 10 GHz [76]. Also, the noise being thermal makes it promising for cryogenic applications.

While the analysis is fairly simple for the mixer case, it is more complex for the G-FET in amplifier operation. Table 5.1 was compiled to benchmark the state-of-the-art room temperature noise figure results for leading FET technologies, given in Figure 2.7, with the modelled F_{min} of the G-FET fabricated in this work, as presented in Figure 4.4. It benchmarks the extrinsic and intrinsic F_{min} at 1 GHz, as well as the frequency where the extrinsic transistor exceeds $F_{min} = 1$ dB. Note that for the four mature technologies, the difference between intrinsic and extrinsic is negligible. In this comparison, the G-FET is far from the promises of the intrinsic properties of graphene as a material. The worse noise performance is reflected in the extracted value of T_d, which is ~ 4 times higher than in HEMTs [43, 46]. This is reflected in the $F_{min}(f)$ characteristics as a rapid increase, since $T_{min} \propto \frac{f}{f_T}\sqrt{T_d}$. In this framework, though, it is also interesting to compare to early results of established technologies before processing methods were optimised. A novel GaAs MESFET achieved a relatively modest $F_{min} = 4$ dB at 1 GHz, with $f_T = 3$ GHz [5]. On the other hand, an early GaAs HEMT already accomplished $F_{min} = 1.4$ dB at 12 GHz, with $f_T =$ 30 GHz [77].

Table 5.1: Benchmark of state-of-the-art microwave low-noise FETs at RT. Noise figures presented are at $f = 1$ GHz. For the mature technologies $F_{min,ex} \simeq F_{min,in}$ is valid.

Technology	$F_{min,ex}$	$F_{min,in}$	$F_{ex,1dB}$	L_g	f_T
G-FET [Paper A]	3.3 dB	1 dB	300 MHz	1 μm	5 GHz
GaAs MESFET [78]	0.4 dB	-	35 GHz	0.11 μm	88 GHz
GaAs pHEMT [79]	0.1 dB	-	40 GHz	0.1 μm	120 GHz
InP HEMT [80]	0.1 dB	-	75 GHz	0.15 μm	150 GHz
Si MOSFET [81]	0.1 dB	-	24 GHz	65 nm	160 GHz

Based on the directions followed by todays state-of-the-art low noise FETs, from these early results, the most fundamental issues to approach the competitors may be identified. Addressing the high contact and access resistances of the G-FET yields a double contribution. Firstly, eliminating the extrinsic noise contributions and, secondly, enabling a gate length down-scaling with maintained gain capabilities, that is reducing C_g while preserving g_m. This makes it possible to actually increase extrinsic f_T, thus enhancing the extrinsic F_{min}. Although a high f_T is important, in comparing Si MOSFETs and InP HEMTs from Table 5.1, clearly better dynamic properties of the carriers in the channel are essential to reach low noise performance especially at higher frequencies. The superior mobility of graphene must consequently be better utilised in G-FET channels, in which e.g. BN gate dielectrics and substrate is an interesting approach to minimise carrier scattering. Also, the ability to operate with high f_T at a drain current as low as possible has proven important, from (2.25), and concluded in [82]. A future direction is to characterise also $F_{min}(I_{ds})$ for G-FETs.

An advantage of the 2D electron gas in a HEMT channel is the dramatical increase in mobility at cryogenic temperatures. An observed mobility enhancement for graphene on substrate at low temperatures, e.g. [83], is promising in this context, although suspended graphene show competitive mobilities already at near room temperature [14]. Future work thus should include complete source-pull analysis versus ambient temperature and drain current, $F(I_{ds}, T_a, \Gamma_s)$. This allows for extraction of the noise parameters Γ_{opt} and R_n, making a formal validation of the Pospieszalski noise model for G-FETs possible according to (2.28).

5.2 Future outlook

Judging from the current performance G-FETs are probably not a future candidate for extremely low noise applications or LNAs at higher frequencies. Further consolidation requires a study with de-embedded source-pull measurements to extract the intrinsic F_{min} by modelling. Doing this versus gate length, L_g, reveals the potential with current mobilities, in eliminating the contact resistances. Still, to compete in low noise applications with HEMTs, it is of utmost importance to address the other performance bottleneck in low channel mobility in top-gated G-FETs on a substrate and reach the levels of e.g. InAs. Presently, graphene seems more likely to be an inexpensive alternative outperforming Si at lower and moderate microwave frequencies or complementary integrated with Si. This preferably uses CVD grown graphene directly on insulating substrate with mobilities surpassing those of Si, which are not yet achieved [84].

5.3 Conclusion

In this master thesis the first study of noise performance of graphene FETs at microwave frequencies has been conducted. Two applications have been considered, namely as a subharmonic resistive mixer and in a small-signal amplifier. The dominating noise generating process in the subharmonic resistive mixer was established to be thermal in origin, with $F_{SSB,mixer} \simeq CL =$ 20-22 dB for $f_{RF} =$ 2-5 GHz. Also, the noise figure of the amplifier could be described by thermal noise of the channel and parasitic resistances, with the Pospieszalski equivalent noise temperature model. General FET procedures has thus proven useful also for understanding the performance of the G-FETs in this work.

As a consequence of the low 50 Ω gain in G-FETs, a G-FET amplifier was designed as a part of this work, with a reported state-of-the-art small-signal transducer power gain $G_T \simeq 10$ dB at $f = 1$ GHz. This represents an 8 dB improvement compared to earlier reports. The achieved gain was high enough to allow for a relatively accurate noise figure measurement, with the main result being $F = 6.4 \pm 0.4$ dB at $f = 1$ GHz. Finally, utilising the Pospieszalski model, based on the extracted small-signal equivalent circuit, the minimum extrinsic and intrinsic noise figures of the G-FET were calculated. The results were $F_{min,ex} = 3.3$ dB and $F_{min,in} = 1$ dB at 1 GHz, respectively.

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Paper A

A 10-dB Small-Signal Graphene FET Amplifier

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Paper B

Noise Figure Characterization of a Subharmonic Graphene FET mixer

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Paper C

Towards Practical Graphene Field Effect Transistors for Microwaves

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