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Quantitative Evaluation of High Speed Microwave Modem

Master's Thesis in the program Communication Engineering

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Gothenburg, Sweden 2011
Master's Thesis EX058/2011

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Abstract

With advent of the 4th Generation (4G) mobile network and bandwidth thirsty applications, system operators have been employing different techniques to balance the bandwidth demand. To fulfill the bandwidth requirement, high bandwidth backhaul links are required. Fiber optic can address the bandwidth requirement but at cost of network infrastructure deployment. In order to cut cost microwave radio links are used by wireless network providers. However, the bandwidth of current microwave radio will become a bottle neck for the upcoming high speed wireless standards.

Ericsson AB in collaboration with BitSim AB is moving forward to achieve the 10 giga bits per second (Gbps) microwave Link. The work on digital portion is carried out at BitSim AB. In this thesis the digital part of the 10Gbps microwave modem is discussed and much focus is put on the modulation and detection of the symbol. The microwave modem is designed for the E-BAND region of the spectrum at 70/80 GHz. At such high frequency local oscillator mismatch at the transmitter and receiver can introduce high phase noise. Further the Analog to digital converter at such high speed should be much more precise. For countering the phase noise effect, circular 16 Quadrature Amplitude Modulation (QAM) is chosen as the modulation scheme of choice. In this thesis the chosen scheme's performance is tested under phase noise, additive white Gaussian noise (AWGN), quantization noise and is compared with rectangular QAM.

Acknowledgements

At last the day has arrived in the middle of spring in which I have completed my thesis work. Initially, I want to thank Almighty Allah, who has given me the strength and courage to complete the thesis work.

I want to thank Tryggve Matheison for supervising me during the whole thesis time. Being a digital Guru he has helped me in understanding "how it is done in FPGA". Dr. Hani Mehrpouyan and Dr. Michail Matthaiou, the former being my advisor came to my help in developing the theory of the modulation scheme and noise models. I got stuck at one moment in formulating but their eagle eyes did not let me to get stuck and corrected me wherever I got wrong. Not forgetting Dag Mortensen who helped me in implementing and understanding the design in the FPGA environment. I want to thank my examiner Tommy Svensson, whose valuable comments were of keen importance during thesis.

Prayers of my family and friends were with me at every moment of this whole time. They were the motivation and energy to move further.

Muhammad Assad Tariq, Göteborg 28/04/11

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Acronym

ADC analog to digital converter
AGC automatic gain control
ALU arithmetic logic unit
AWGN additive white gaussian noise
BS base station
BSC base station controller
BTS base transceiver system
CLB configurable logic block
CPRI common public radio interface
DAC digital to analog converter
DDR double data rate
EDGE enhanced data rates for GSM evolution
FEC forward error correction
FPGA field programmable gate array
GGSN gateway GPRS Support Node
GPRS general packet radio service
IF intermediate frequency
LO local oscillator
LTE long term evolution

LVDS low voltage differential signalling

MSC master switching center

OBSAI open base station architecture initiative

PDN public data network

PN phase noise

PLL phase locked loop

PSTN public switched telephone network

QAM quadrature amplitude modulation

QPSK quadrature phase shift keying

RAN radio access network

RAM radio access memory

ROM read only memory

SGSN serving GPRS support Node

SNR signal to noise ratio

VCO voltage controlled oscillator

1

Introduction

IN recent years mobile communication has proven itself an effective means of transferring voice as well as high speed data. The demand for high bandwidth data services continue to escalate with the evolution of third generation (3G) and fourth generation (4G) cellular networks [11]. The increase in user throughput results in the increase of base station (BS) throughput requirements, which in turn increases the rate of base station controller (BSC) and master switching center (MSC). The Backhaul links are backbone of any cellular network as they serves the medium to carry traffic from BS to the core network via BSC.

During the last decade cellular networks have been carrying more and more data traffic compared to voice. Increase in the use of bandwidth hungry devices have forced the operators to increase their bandwidth. In addition, advancements in internet and related services in terms of social networking, high definition (HD) streaming, online banking, online gaming, and video call services have fueled the usage of even larger data traffic. It is estimated that global mobile data traffic will reach 6.3 exabytes per month by 2015 [12].

1.1 Background

The whole cellular network is a composite of wired and wireless infrastructure. A typical cellular network compromises of BS, BSC and master switching center (MSC), which are interconnected either through wired or wireless medium. Figure 1.1 is an illustration of a typical mobile infrastructure. The user communicates to the network through BS. The BS provides the air interface to the user terminal to transmit and receive data. A typical BS looks like the one shown in Figure 1.2. The data carrying capacity of each BS varies with area and location. For example, if the BS is located in a densely populated area, it would have much more call carrying and data capacity as compared to the one located in a rural area. Each BS is connected to BSC normally via a microwave link as

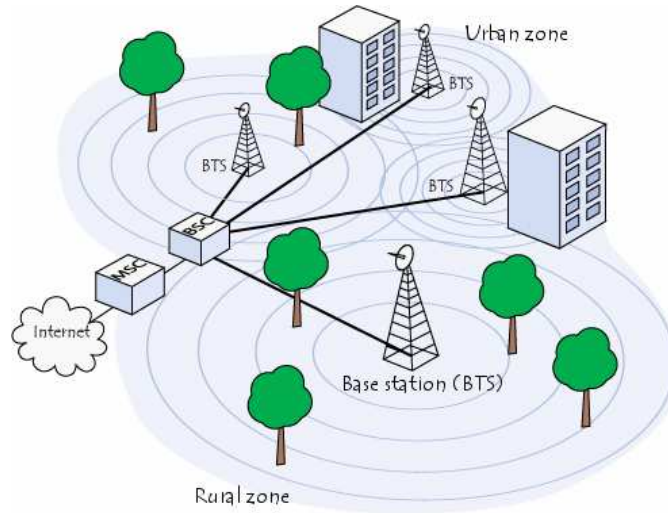


Figure 1.1: Typical cellular network infrastructure[1]

it is feasible for the operator to connect remotely positioned site. Another approach is through the use of leased line (E1/T1) from wire-line service providers. BSC controls the functionality of BS, manages traffic and user requirement. In addition, to the mentioned functionalities, it also routes the data from BS to MSC and vice versa and controls the handover procedure from one BS to another BS. The MSC act like the brain of the cellular network, it holds and controls all calls and data management functionalities. Along with MSC, the packet service is managed by serving GPRS support Node (SGSN) and gateway GPRS Support Node (GGSN). The aforementioned names are used in 2G mobile network (GSM/CDMA), where as in the 3G and 4G mobile network these entities are renamed and are summarized in Table 1.1.

1.1.1 Backhaul Network

The mobile or wireless backhaul is the portion of a wireless mobile network that connects information travelling from a BS to a MSC. The inter MSC network is called the backbone network. One of the major expense for wireless operator is the backhaul traffic. Figure 1.3 shows the difference between backhaul and backbone portion of the cellular network. The most common method to carry traffic is by using E1/T1 leased circuits from local wireline carrier. It is estimated that 30% to 50% of the carriers recurring operational expenses is due to leasing E1/T1 lines [3]. Bandwidth demand of voice traffic is either saturated or growing slowly, but with the introduction of high speed data service in 3G and 4G, amount of data traffic to be backhauled has increased rapidly. Operating cost of aforementioned backhaul technology increases with increasing capacity and it will become of least interest for network providers to deploy it if they have to lower operational expenditure (OPEX).

Table 1.1: RAN components and functionality for different different technologies[9]

Mobile Technology Generation	Type	Radio Access Components	Role
2G	GSM	BTS	Communication between air interface and BSC
		BSC	Controls multiple BS
		MSC	Handle Voice calls and SMS
2.5G	GPRS	BTS	Communication between air interface and BSC
		SGSN	Mobility management and data delivery to and from user terminal
		GGSN	Gateway to external data network
3G	UTRAN	BSC+PCU	Controls multiple BS and processes data packets
		NodeB	Performs functions similar to BTS
		RNC	Performs functions similar to BSC
		MSC	Handle Voice calls and SMS
4G	LTE	eNodeB	Routing and forwarding of user data, mobility anchoring
		SGW(serving gateway)	
		MME(mobility management entity)	Tracking idle user devices, handoff management
		PDN Gateway	Gateway to external data network



Figure 1.2: A typical base station having a set of transceiver antennas for communication between user terminal and network. Along with the transceiver is the microwave link, which carries the user data from the BS to BSC. Both the antennas are mounted either on a pole or tower at a specific height[2]

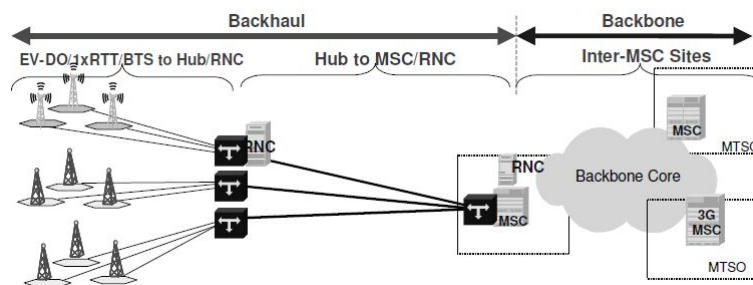


Figure 1.3: Backbone and backhaul in a cellular network[3]

Microwave radios as alternative to leased lines and are cost effective. It is no coincidence that 50% of the world's mobile base station are connected using point-to-point microwave links [13]. For over 20 years the microwave has been the primarily solution for rapid deployment of mobile backhaul infrastructure. Microwave can be deployed rapidly and cost effectively enabling services to be established quickly. Furthermore, microwave transmission systems are much more secure than cable network in terms of theft and vandalism.

Common frequency bands used for microwave radio transmission are 7, 18, 23 and 35GHz. Lower bands are preferred due to better radio propagation characteristics. However these frequencies have less bandwidth due to present usage and are more prone to long range interference. Gigabit capacity can be achieved in traditional band by means of higher modulation schemes, spatial multiplexing and polarization, which results in higher degree of complexity [14]. Recent release of E-Band, which lies around 70GHz

(71-76GHz) and 80GHz (81-86GHz) spectrum has opened up new dimension for point-to-point microwave links. The availability of 10GHz of bandwidth in this spectrum allows the use of low order modulation schemes and simple receiver implementations.

A traditional microwave link looks like the one shown in Figure 1.4. The point-

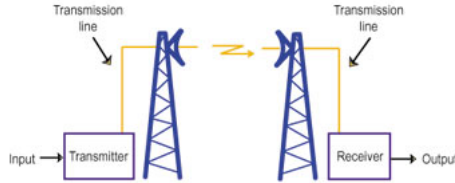


Figure 1.4: A typical microwave link

to-point microwave link has a pair of parabolic antennas, which are located on both end of the link. Microwave antennas transmit and receive electromagnetic signals and convert electrical signal to electromagnetic wave and vice versa. The transmitter and receiver are placed in housing that is co-located with the tower, which also includes the antenna. These units are made up of digital and analog circuitry that are responsible for handling digital data and extract data from the received signal. Major components that make up the transmitter and receiver are oscillators, amplifiers, modulator, demodulator, frequency up-down converters, timing and frequency lock, etcetera.

1.2 Thesis Layout

Chapter 2 deals with the formulation of symbol error probability for the 16 quadrature amplitude modulation (QAM) circular constellation. Noise models have been discussed that will be used to test the constellation and system performance. Furthermore, performance of circular-QAM is compared with the constellation discussed in the literature [15, 16, 7].

Chapter 3 deals with the framing protocol that is proposed for the project.

Chapter 4 describes basic structure for the digital part of the 10G microwave modem. An overview of the hardware functionality is given. Furthermore, FPGA implementation of the modulation scheme is discussed and the chapter is concluded with the hardware simulation results.

Chapter 5 gives the summary of the thesis work with conclusion.

1.3 Limitations

Limited time has been a key factor for the thesis. This project work was in development phase during the time of thesis. Moreover, in the allocated time frame, it was not possible to discuss the whole microwave link. The work has been limited to design and testing

of the modulator and demodulator because without modulation and demodulation it is impossible to achieve high data rate transmission. Furthermore, it is supposed that link is synchronized and the signal is sampled at the correct time instant.

2

Theory

2.1 Communication System

The basic elements of a digital communication system is shown in Figure 2.1. Every

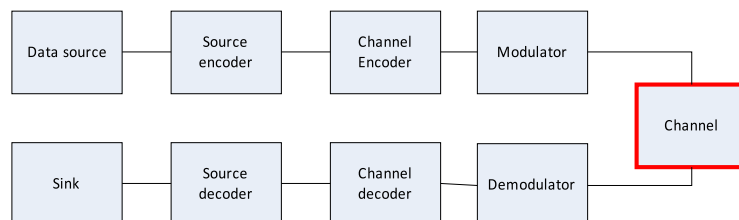


Figure 2.1: Digital communication system

communication system starts with a source of data that needs to be transmitted. The *source encoder* converts the input data, which could be either analog or digital, into a sequence of binary data. The binary data is passed through a *channel encoder* which adds redundancy to the data. This is required to overcome the effects of noise added by the channel. Ratio of redundancy to data is dependent on the type of communication system. For a system having high level of noise, it would require more redundant information so as to help the receiver decode and correct the received data. If k denotes the number of inputs bits to the channel encoder and n is the output bits then the rate of the encoder is given by k/n . There are different types of channel coding schemes which are broadly classified into *block codes*, *convolutional codes*, and *turbo codes*. After adding up redundant data bits, the sequence of bits are mapped onto signal waveforms by the modulator block. Based on mode of transmission channels are distinguished into two main groups: channels based on guided propagation and free propagation. The first

group includes fiber optic, coaxial cable, and telephone channels. The second group includes wireless broadcast channels, mobile radio channels and satellite channels. Each of these channel types have their specific characteristic and effect of noise is different for different channels [17]. The receiver obtains the signal from antenna and samples it. At the receiver based on received sample and type of constellation, it is decided which symbol was transmitted by the transmitter. The symbol detected, which was encoded by the channel encoder is decoded by the channel decoder. As previously discussed, channel decoder detects, and corrects errors that are due to the channel. After successful decoding, source decoder converts the digital signal into a form at which can be used by the user.

For every communication system, the data needs to be transformed in such way that it can be effectively transmitted. The modulator block has a key role in communication system. It modifies the message signal into a form that is suitable for transmission over the channel. Modulation is achieved in three ways: loading information either on changing amplitude, frequency and phase or a combination of these. Digital modulation is achieved by mapping bits onto finite levels of any of these dimensions. The type of digital modulation schemes can be summarized as follows.

- **Amplitude shift keying (ASK):** bits are mapped onto finite set of amplitude levels. The number of levels depends on how many bits are mapped.
- **Frequency shift keying (FSK):** in this modulation type, there are finite sets of frequency levels.
- **Phase shift keying (PSK):** there are finite levels of phases on which bits are mapped.

2.2 Quadrature Amplitude Modulation

Quadrature amplitude modulation (QAM) is generated by changing both the phase and amplitude of signal. The bits are mapped to two analogue signals by changing the amplitude and phase. The two analogue signal (sinusoid) are out of phase with each other by 90° , making them orthogonal. The modulated signals are summed up and the resulting waveform is the combination of both PSK and ASK.

Based on structure of the constellation diagram, different types of QAM exists. QAM having a rectangular structure are denoted by rectangular-QAM, likewise circular symmetry constellations are called circular-QAM. Each constellation performs differently under different channel conditions. In Figure 2.2 performance of different levels of QAM is compared with other various modulation schemes.

Table 2.1 shows the relationship between the bandwidth and modulation scheme in an ideal case and it can be seen that with a higher modulation scheme and lower bandwidth higher data rates can be achieved.

Rectangular-QAM is much easier to modulate and demodulate due to its regular structure, which is generated by amplitude modulations in phase and quadrature. On

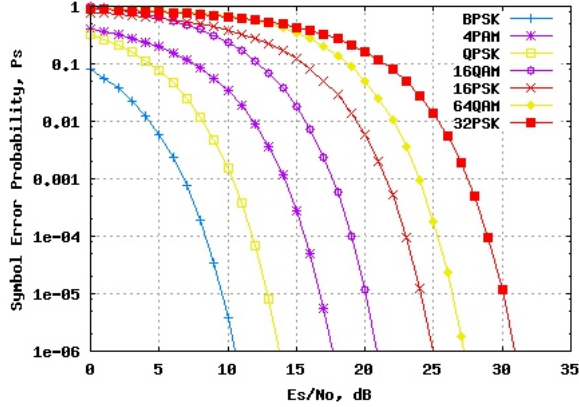


Figure 2.2: Comparison of various modulation schemes in terms of symbol error rate and $E_s N_o$ [4]

Table 2.1: Maximum capacity of different modulation scheme from 2.5GHz to 10GHz bandwidth[10]

Available Bandwidth(Ghz)		2.5	5	10
	BPSK	1.25	2.5	5
	QPSK	2.5	5	10
Maximum Capacity(Gbps)	16 QAM	5	10	20
	32 QAM	10	20	40

the other hand, circular-QAM has the advantage of performing better in channels effected by phase noise, which will be discussed, in section 2.4.1. Furthermore, with help of digital signal processing it is now possible to implement such schemes.

2.3 Simulation Model

The simulation model is shown in Figure 2.3. From this simulation model, effect of the additive white Gaussian noise (AWGN), phase noise and quantization noise over both rectangular and circular constellations are observed. The transmitter generates complex symbols which are passed through the channel. AWGN noise is generated by the hardware components. Oscillator phase noise is due to the result of the local oscillator mismatch and the quantization noise is generated by the digital to analog converter (DAC) and analog to digital converter (ADC) when having poor quantization levels. Out of these three noise sources AWGN and quantization noise are additive in

nature [16][5] and phase noise is multiplicative [18]. Figure 2.3 illustrates the baseband system model for the communication link. It is assumed that the system is only effected by the aforementioned noises under coherent detection. If S_t is the transmitted signal affected with n_{phase} , $n_{quantization}$ and n_{AWGN} which are defined later in this chapter, then the received signal, y , can be written as (2.1)

$$y = (S_t \times n_{phase}) + n_{AWGN} + n_{quantization} \quad (2.1)$$

where

$$\begin{aligned} n_{phase} &= e^{j\theta} \\ n_{quantization} &= U_i + jU_Q \\ n_{AWGN} &= n_i + jn_Q \end{aligned}$$

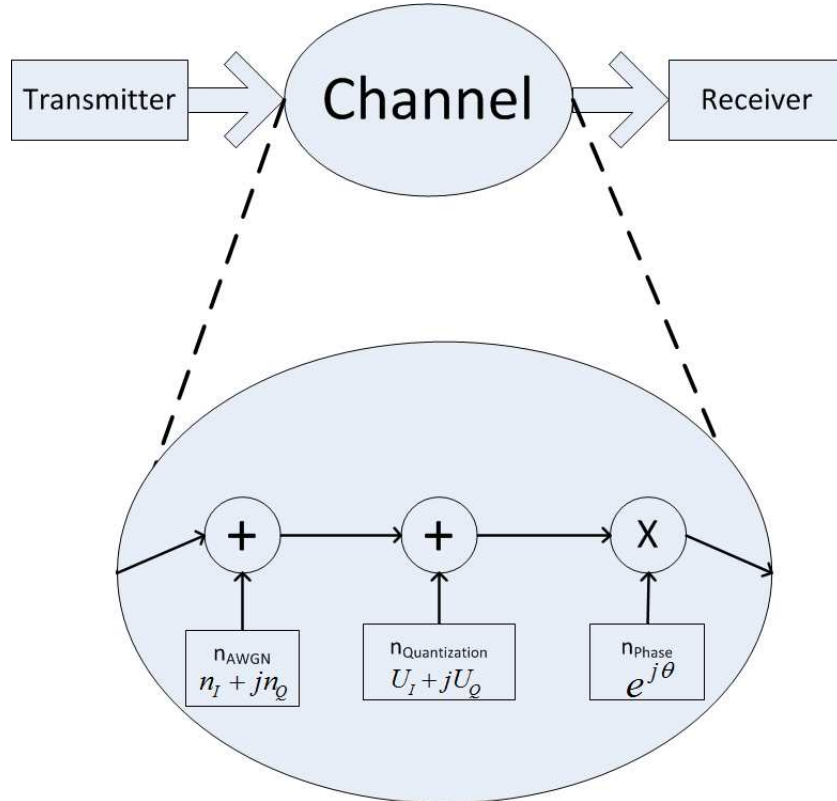


Figure 2.3: Equivalent Baseband system model

2.4 Probability of Error Formulation

2.4.1 Circular-16QAM

Figure 2.4 illustrates the constellation of circular 16QAM. Each ring is equally spaced by distance a , this locates the rings at radii a , $2a$, $3a$ and, $4a$. Four symbols lie on each ring with phase difference of 90° . The symbols on the odd rings lie at phases “ 0° , 90° , 180° and 270° ” whereas the symbols on the even rings lie at “ 45° , 135° , 225° and 315° ”. Mapping of the symbols on the IQ-plane is tabulated in Table 2.2. IQ-plane is a graphical representation of the signal in cartesian coordinate system. Where I and Q planes represent the x and y-planes respectively. Each point on the IQ-plane represent a specific amplitude and phase of the signal in time domain. The calculation of the symbol error

Table 2.2: Symbol Mapping on the IQ-Plane

Symbol Number	Location	Symbol Number	location
1	$(a \cos(0), a \sin(0))$	9	$(3a \cos(0), 3a \sin(0))$
2	$(a \cos(90), a \sin(90))$	10	$(3a \cos(90), 3a \sin(90))$
3	$(a \cos(180), a \sin(180))$	11	$(3a \cos(180), 3a \sin(180))$
4	$(a \cos(270), a \sin(270))$	12	$(3a \cos(270), 3a \sin(270))$
5	$(2a \cos(45), 2a \sin(45))$	13	$(4a \cos(45), 4a \sin(45))$
6	$(2a \cos(135), 2a \sin(135))$	14	$(4a \cos(135), 4a \sin(135))$
7	$(2a \cos(225), 2a \sin(225))$	15	$(4a \cos(225), 4a \sin(225))$
8	$(2a \cos(315), 2a \sin(315))$	16	$(4a \cos(315), 4a \sin(315))$

probability (SEP) is based on the union bound formula (2.2) [5]. Euclidean Distance between symbol s_m and s_n is given by (2.3) and (2.4) and gives the formula of ring radius ratio a with respect to average symbol energy E_s .

$$P_e \leq \frac{1}{M} \sum_{m=0}^{M-1} \sum_{\substack{n=0 \\ m \neq n}}^{M-1} Q \left(\sqrt{\frac{d_{s_m, s_n}^2}{2N_o}} \right) \quad (2.2)$$

$$d_{s_m s_n} = \sqrt{(m_1 - n_1)^2 + (m_2 - n_2)^2} \quad (2.3)$$

where $s_m = (m_1, m_2)$ and $s_n = (n_1, n_2)$

$$a = \sqrt{\frac{2E_s}{15}} \quad (2.4)$$

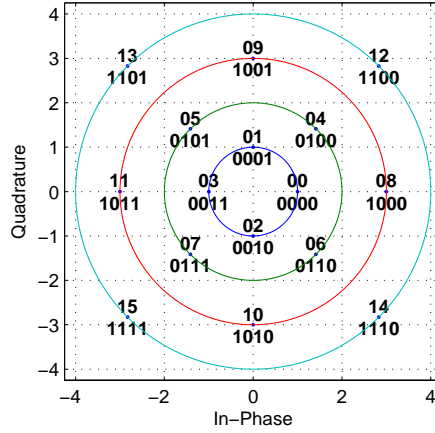


Figure 2.4: 16 QAM Circular Constellation

The application of (2.2) is carried out in steps of rings. It is separately applied over each ring and then the sum of the individual error probabilities is replaced in (2.5). With this assumption (2.2) can be written as

$$P_{ring} \leq P_{ring1} + P_{ring2} + P_{ring3} + P_{ring4}. \quad (2.5)$$

$$P_e \leq \frac{1}{16} P_{ring}. \quad (2.6)$$

Evaluating (2.5) over Figure 2.4 gives the equations (2.7), (2.8), (2.9) and (2.10). After replacing values in (2.5) and (2.6), final expression for the error probability is derived which is given in (2.11).

$$\begin{aligned}
 P_{ring1} = & 8Q \left(\sqrt{\frac{4a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{2a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{10a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{16a^2}{2N_o}} \right) \\
 & + 8Q \left(\sqrt{\frac{(5+2\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(5-2\sqrt{2})a^2}{2N_o}} \right) \\
 & + 8Q \left(\sqrt{\frac{(17+4\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(17-4\sqrt{2})a^2}{2N_o}} \right) \quad (2.7)
 \end{aligned}$$

$$\begin{aligned}
P_{ring2} = & 8Q \left(\sqrt{\frac{8a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{20a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{16a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{4a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{36a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(13 + 6\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(13 - 6\sqrt{2})a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(5 + 2\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(5 - 2\sqrt{2})a^2}{2N_o}} \right) \tag{2.8}
\end{aligned}$$

$$\begin{aligned}
P_{ring3} = & 4Q \left(\sqrt{\frac{4a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{18a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{10a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{16a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{36a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(13 + 6\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(13 - 6\sqrt{2})a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(25 + 12\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(25 - 12\sqrt{2})a^2}{2N_o}} \right) \tag{2.9}
\end{aligned}$$

$$\begin{aligned}
P_{ring4} = & 8Q \left(\sqrt{\frac{20a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{32a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{4a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{64a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{36a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(17 + 4\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(17 - 4\sqrt{2})a^2}{2N_o}} \right) \\
& + 8Q \left(\sqrt{\frac{(25 + 12\sqrt{2})a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{(25 - 12\sqrt{2})a^2}{2N_o}} \right) \tag{2.10}
\end{aligned}$$

$$\begin{aligned}
P_e \leq & \frac{1}{16} \left(8Q \left(\sqrt{\frac{2a^2}{2N_o}} \right) + 20Q \left(\sqrt{\frac{4a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{10a^2}{2N_o}} \right) + 12Q \left(\sqrt{\frac{16a^2}{2N_o}} \right) \right. \\
& + 8Q \left(\sqrt{\frac{8a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{20a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{18a^2}{2N_o}} \right) + 8Q \left(\sqrt{\frac{32a^2}{2N_o}} \right) \\
& + 12Q \left(\sqrt{\frac{36a^2}{2N_o}} \right) + 4Q \left(\sqrt{\frac{64a^2}{2N_o}} \right) \\
& + 16Q \left(\sqrt{\frac{(25 + 12\sqrt{2})a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{(25 - 12\sqrt{2})a^2}{2N_o}} \right) \\
& + 16Q \left(\sqrt{\frac{(13 + 6\sqrt{2})a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{(13 - 6\sqrt{2})a^2}{2N_o}} \right) \\
& + 16Q \left(\sqrt{\frac{(17 + 4\sqrt{2})a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{(17 - 4\sqrt{2})a^2}{2N_o}} \right) \\
& \left. + 16Q \left(\sqrt{\frac{(5 + 2\sqrt{2})a^2}{2N_o}} \right) + 16Q \left(\sqrt{\frac{(5 - 2\sqrt{2})a^2}{2N_o}} \right) \right) \quad (2.11)
\end{aligned}$$

N_o denotes the noise spectral density and is called the noise per unit of bandwidth. Since the Q-function is monotonically decreasing [19] and exponentially decreases with increasing coefficient value, terms in (2.11) having relatively high coefficient values can be eliminated at high SNR, γ_s . Thus, (2.11) is reduced to (2.12)

$$P_{e_{union}} \approx 2Q \left(\sqrt{\frac{a^2}{N_o}} \right) + Q \left(\sqrt{\frac{(5 - 2\sqrt{2})a^2}{N_o}} \right) \quad (2.12)$$

Replacing (2.4) in (2.12) and $\gamma_s = \frac{E_s}{N_o}$, the final formula for the symbol error probability for circular-16QAM can be approximated by (2.13) at high SNR and acts as a lower bound at other SNR.

$$P_{circ16QAM} = P_{e_{union}} \approx 2Q \left(\sqrt{\frac{2\gamma_s}{15}} \right) + Q \left(\sqrt{\frac{(5 - 2\sqrt{2})\gamma_s}{15}} \right). \quad (2.13)$$

Throughout this thesis (2.13) will be used to verify the simulation under AWGN noise.

2.4.2 Rectangular 16QAM

Symbol error probability of error for rectangular-16QAM, at high SNR, shown in Figure 2.5 is given by [5]

$$P_{rect16QAM} = 3Q \left(\sqrt{\frac{E_s}{5N_o}} \right) = 3Q \left(\sqrt{\frac{\gamma_s}{5}} \right). \quad (2.14)$$

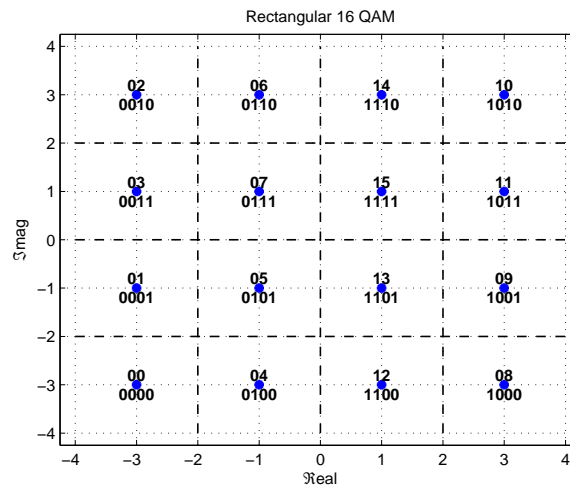


Figure 2.5: Constellation Plot of Rectangular 16QAM showing the decision region for each symbol

2.4.3 Simulation

The receiver used for the simulation is maximum likelihood (ML) receiver. An ML receiver in AWGN minimizes the Euclidean distance between the received symbol and constellation. It picks up the symbol in the constellation which has the least distance. The received symbols are decoded based on the region where they lie in, which are based on the decision region shown for circular and rectangular QAM in Figures 2.6 and 2.5, respectively. The drawn decision region are optimal, keeping in view the inter-symbol distance. Corner of each symbol's region is the intersection of vertical bisector for the line joining two neighbouring symbols.

The derived symbol error probability equation (2.13) for circular-16QAM and (2.14) for rectangular-16QAM are verified by simulation results which are illustrated in Figure 2.7.

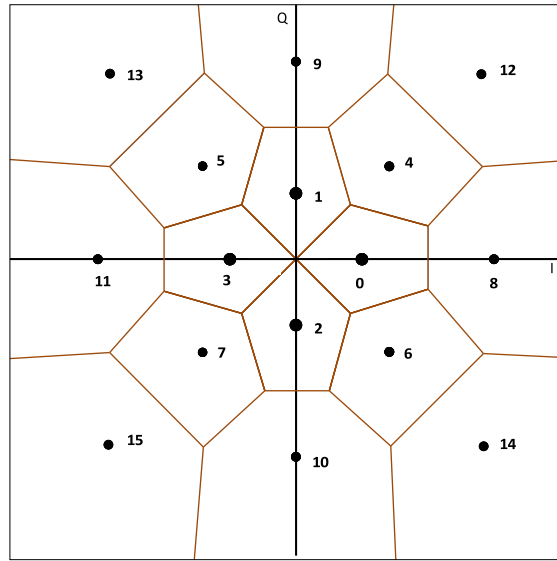


Figure 2.6: Decision region for circular-16QAM

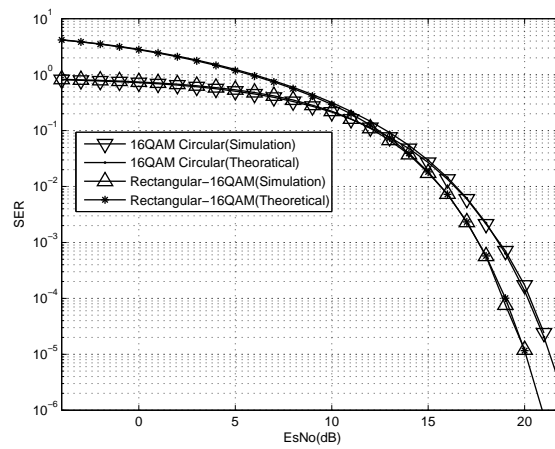


Figure 2.7: Comparison of performance between circular and rectangular -16QAM

2.5 Noise Model

The received signal is subjected to three types of noise sources.

- Additive white Gaussian noise (n_{AWGN}),

- Quantization noise ($n_{\text{quantization}}$) and
- Oscillator phase noise (n_{phase})

Out of these three types of noise sources the first two are additive in nature where as the last one is multiplicative in nature. Furthermore, due to the complex nature of the baseband signal the noise sources are also complex.

2.5.1 Additive White Gaussian Noise (n_{AWGN})

It is the simplest model of the communication channel. This type of noise is generated by the electronic components at the receiver, e.g. amplifier. If the noise is introduced by electronic components and amplifiers at the receiver, it can be characterized as thermal noise. This type of noise is characterized statistically by a *Gaussian process* [5]. AWGN channel model constitute of a transmitted signal $s(t)$ and an additive noise process $n(t)$ as shown in Figure 2.8.

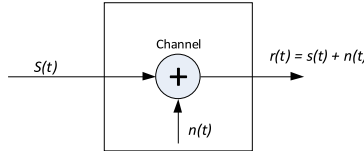


Figure 2.8: AWGN channel model [5, p.10]

2.5.2 Effect of AWGN on circular and rectangular-16QAM

From the curves in Figure 2.7 it is observed that rectangular-QAM performs 2dB better at SER of 10^{-5} . Rectangular-QAM has an equal space distribution for each symbol whereas in circular-QAM, inner symbols have a tighter region compared to the outer symbols. The result of these tight region is more contribution of error by these symbols because noise will displace them to region of neighbouring symbols.

2.5.3 Quantization Noise ($n_{\text{quantization}}$)

Quantization noise occur due to the difference between the original value and the quantized value. It is also called the quantization error. Quantization error is directly related to the number of quantization levels used. The fewer the quantization levels, the higher is the quantization error and quantization noise. The quantizer employed in this thesis is a scalar uniform quantizer. From [20] it is known that the distribution of the quantization noise is uniform. Therefore, random variables U^I and U^Q are uniformly distributed between $\pm b$ with noise variance $\sigma_{U^I}^2 = \sigma_{U^Q}^2 = \sigma_U^2$ [16], where I and Q are the in-phase and quadrature phase respectively. From [20] it is known that the parameter b

is related to the noise variance via $b = \sqrt{3 \cdot \sigma_U^2}$. Furthermore, if ADC is operating within the voltage scale of $\pm V_s$, the variance of quantization noise can be written as

$$\sigma_U^2 = \frac{V_s}{3 \cdot (2^{2N_{ADC}})}, \quad (2.15)$$

where N_{ADC} is the number of bits which define the quantization levels. By setting $V_s = 1$ the parameter b can be written in term of N_{ADC} as

$$b = 2^{-N_{ADC}}. \quad (2.16)$$

2.5.4 Effect of Quantization Noise

Within the channel discussed in the simulation model, quantization noise is also taken into consideration. As already discussed, lower quantization level will contribute more to the noise as compared to the ADC having larger quantization levels. The quantization levels are changed by changing the number of bits, i.e., N_{ADC} which will in the model changes the variance of the quantization noise. Furthermore, the range of the ADC, V_s , is set to ± 1 . The signal is assumed to be within the range of ADC and there is no saturation or clipping. From the curves in Figure 2.9, it is observed that increasing the precision of the ADC decreases the effect of noise.

2.5.5 Phase Noise n_{phase}

Oscillator on both ends of the link are assumed to be free running. A slight mismatch between the carrier frequency and the local oscillator at intermediate frequency (IF) stage can add phase shift to the received symbol. This would displace the sampled symbol to another decision region resulting in an error. To keep local oscillator locked to carrier frequency, phase locked loop (PLL) are employed. PLL calculates the phase difference between received and output signal. The difference is then applied to the voltage controlled oscillator (VCO) which changes the oscillating frequency in order to minimize or completely remove the difference. Moreover, the oscillator itself does not generate true sine waves and its operation is affected by the electronic circuitry used. Noise generated by oscillator circuit results in distortion of amplitude and phase of the oscillating frequency. This phase distortion is called the oscillator phase noise.

The phase noise (PN) model adopted in this thesis work is based on [21, 22, 23]. This phase noise model has been accepted as a reference in the European digital terrestrial television broadcasting project. The PN output in baseband notation can be written as (2.17)

$$n_{phase} = e^{j\theta(t)} \approx 1 + j\theta(t). \quad (2.17)$$

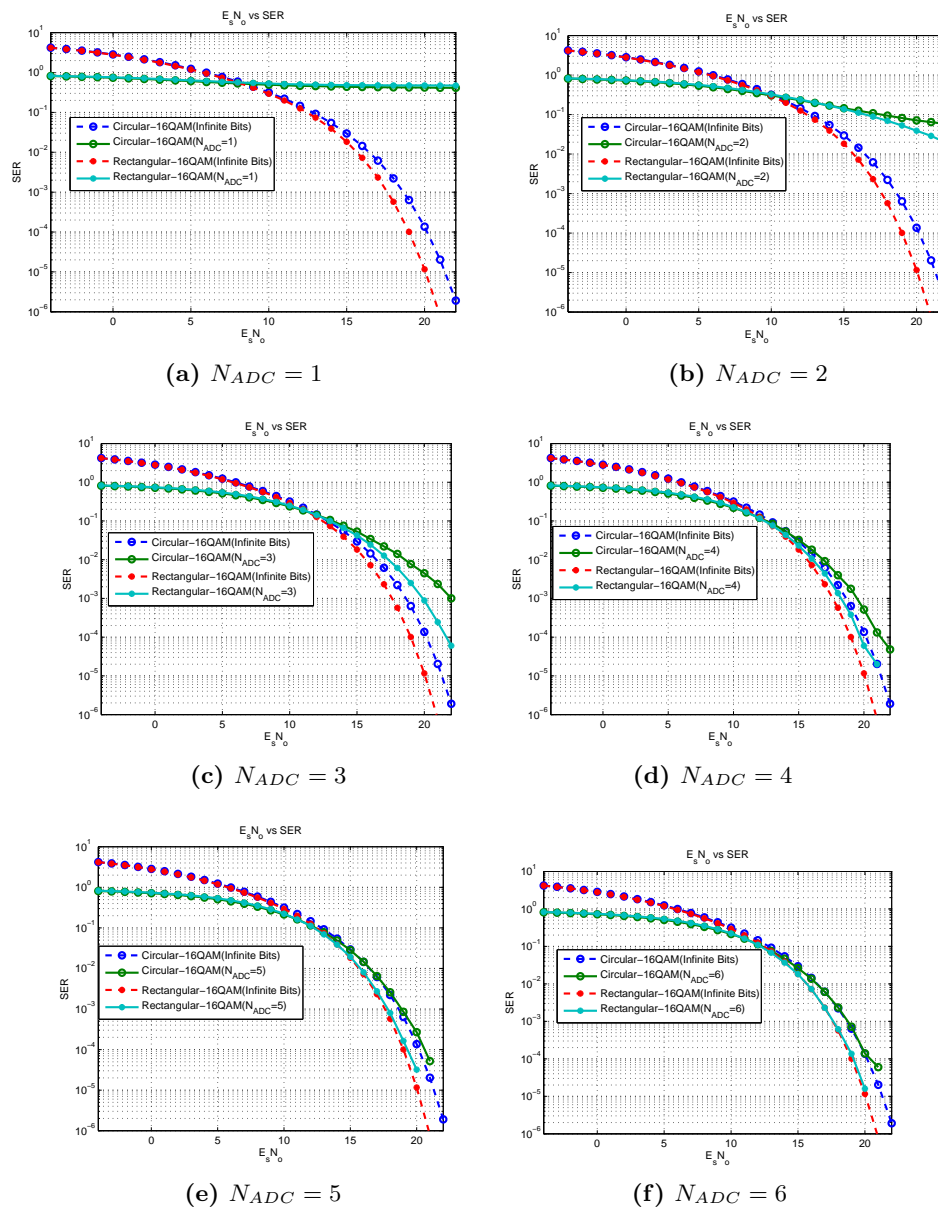


Figure 2.9: Effect of varying N_{ADC} on SER

If PN process is slowly varying, it can be assumed that the phase change is constant over the symbol period [18]. After sampling the PN process becomes discrete in time and can be modeled as a discrete time Wiener process [24, 25]. The PN updates can be written as

$$\theta_t = \theta_{t-1} + \Delta_t, \quad (2.18)$$

where Δ_t is modeled as a Gaussian distributed random variable with zero mean and variance $\sigma_{\Delta}^2 = 2\pi BT$ [25]. BT is called the PN rate and is the product of PN bandwidth (B) and modulated symbol period (T). From Figure 2.10 it is observed that the nature of the updates of phase noise follow random walk, where k is the time realization ($k=t$).

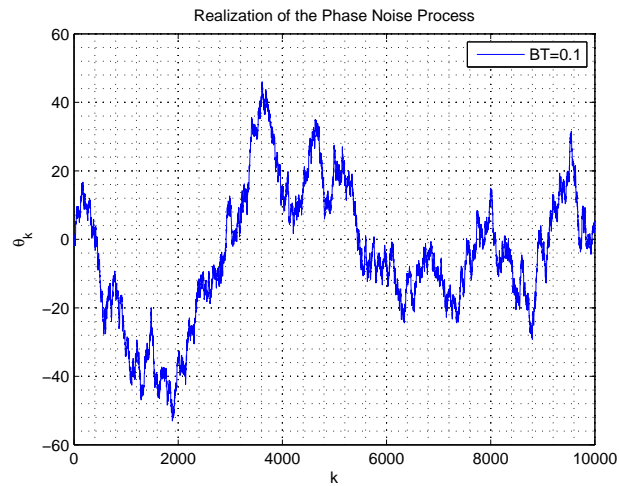


Figure 2.10: Realization of discrete time Wiener process

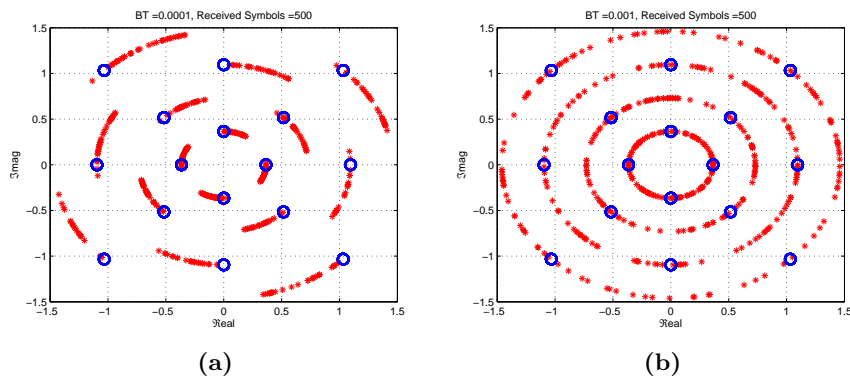


Figure 2.11: Effect of phase noise on circular-16QAM

When PN is applied to the constellation of 16QAM circular, it will cause each symbol to rotate along its axis. Degree of rotation is dependent on the severity of the mismatch between oscillator and carrier frequency. If the variance of PN is high, this would rotate the symbol much more as compared to smaller variances, as illustrated in Figure 2.11. In addition, the phase instabilities can cause havoc in the communication system if left unaddressed. With passage of time, the unaddressed phase noise results in erroneous decoding as illustrated in Figures 2.12. Figure 2.12a shows the received symbol is not affected by any phase instabilities. Figure 2.12b and 2.12c illustrates how phase noise distorts the received symbols.

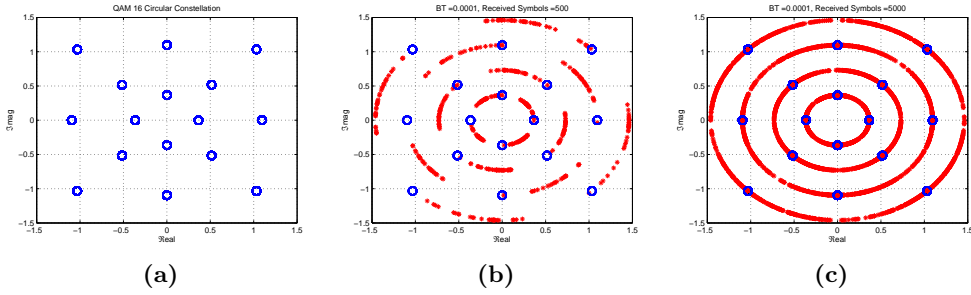


Figure 2.12: Effect of unaddressed phase noise

2.5.6 Performance of modulation schemes with phase noise

Before evaluating the performance of modulation schemes under phase noise, symbol error probability (SEP) is derived for binary phase shift keying (BPSK) and quadrature phase shift keying (QPSK) with phase noise which is given in (2.19) and (2.20) (for derivation refer to Appendix A).

$$P_{BPSK_\theta} = \frac{1}{2} \operatorname{erfc} \left(\operatorname{real}(e^{j\theta}) \sqrt{\frac{E_s}{N_o}} \right) \quad (2.19)$$

$$P_{QPSK_\theta} = \frac{1}{2} \operatorname{erfc} \left((\cos \theta - \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) + \frac{1}{2} \operatorname{erfc} \left((\cos \theta + \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) \\ + \frac{1}{4} \operatorname{erfc} \left((\cos \theta + \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) \operatorname{erfc} \left((\cos \theta - \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) \quad (2.20)$$

The curves in Figures 2.13 are obtained by varying SNR and the phase noise rate, BT, for BPSK and QPSK. As it can be seen in the Figures 2.13a and 2.13a, both the simulation and theoretical curves overlap with one another. This result validates the correctness of the simulation setup.

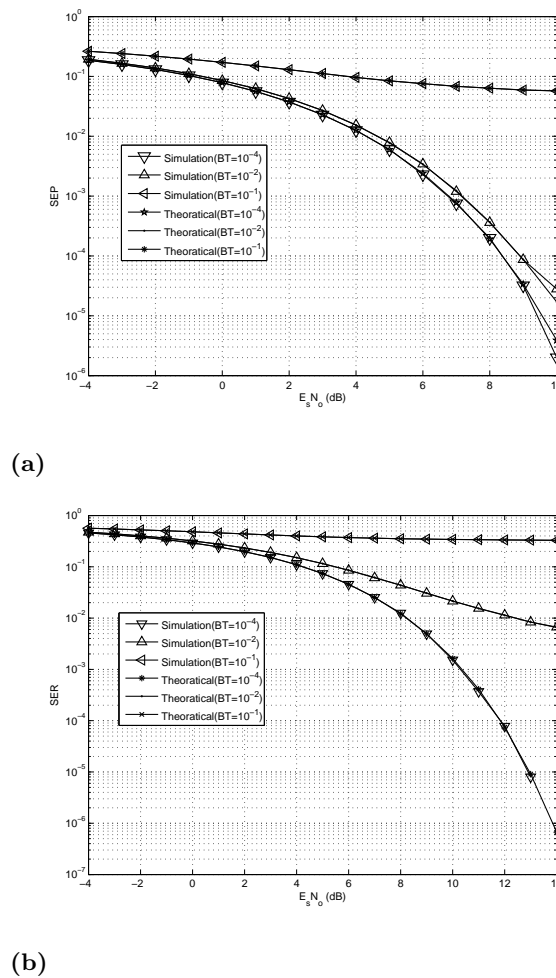


Figure 2.13: SER vs $E_s N_o$ under varying phase noise

2.5.7 Circular-16QAM and phase noise

Continuing with the noise effect on the modulation schemes, effect of phase noise in addition with AWGN is analysed. Figure 2.14 is a result of performing Monte Carlo simulations on the aforementioned model over circular-16QAM and rectangular-16QAM. Variance of PN is varied by changing the phase noise rate BT . It is observed that circular-16QAM performs better than its rectangular counterpart. It is also observed that circular-16QAM performs 4dB better than rectangular-16QAM at intermediate PN rate, BT . Rectangular-16QAM curve does not improve by increasing SNR near SER of 10^{-4} at $BT = 10^{-3}$ whereas circular-16QAM continues to perform better.

It is noted in Figure 2.15 that circular-16QAM has a wider and equal phase free region

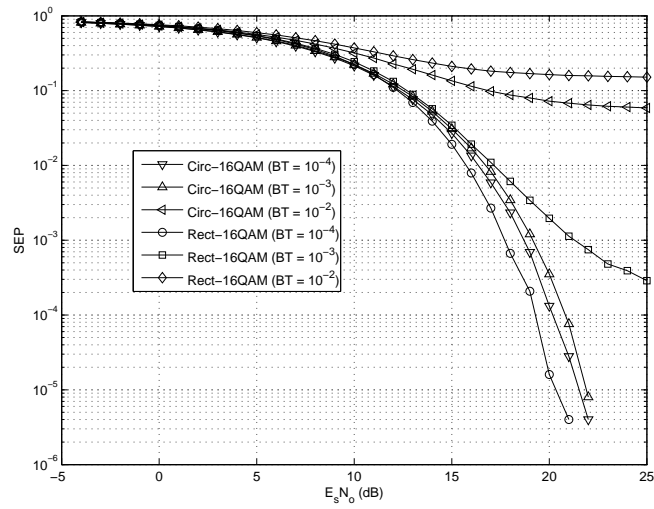


Figure 2.14: Comparison of performance between Rectangular and Circular 16QAM under phase noise

for each symbol phase (each symbol is 90° apart from adjacent symbols). Furthermore, it can be noted that in the case of rectangular-16QAM the phase difference between the symbols on the center rectangles have a smaller phase difference compared to the most inner and outer rings and significantly contribute to the SER in the presence of PN.

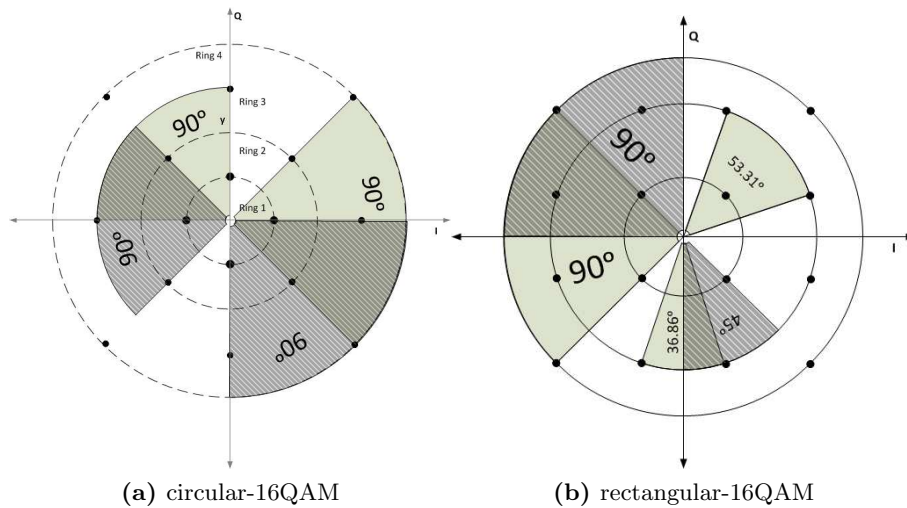


Figure 2.15: Phase difference between symbols

The inherent wider phase distribution in circular-16QAM allows it to perform better than rectangular-16QAM. In addition to wider phase distribution, the circular-16QAM in Figure 2.16 performs better than the circular constellation [26, 15, 7] which are optimized for AWGN only. Simulations have shown that circular-16QAM outperforms the optimal_{AWGN} [6] and (4,12) circular-16QAM [7] at intermediate PN rate BT and are illustrated in Figure 2.16a and 2.16b respectively.

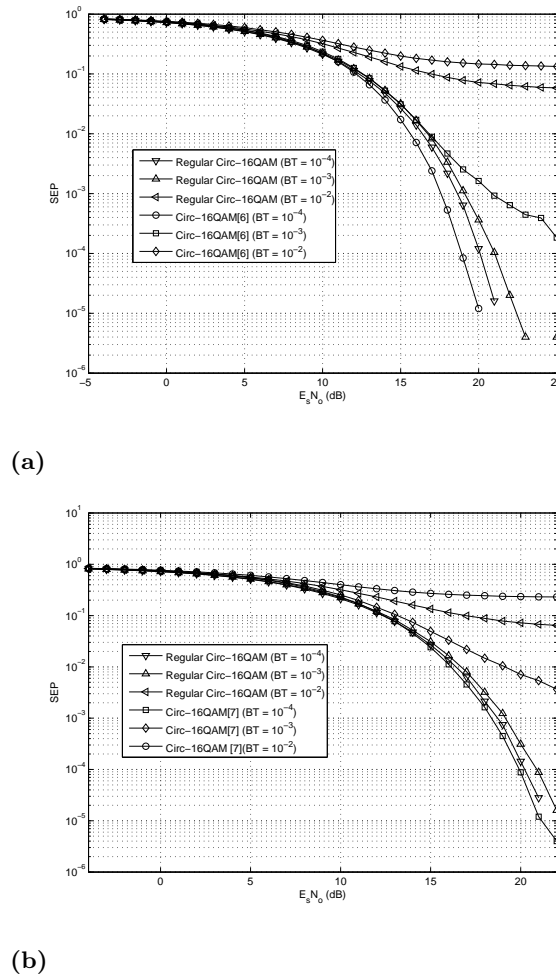


Figure 2.16: Comparison between the circular-16QAM with optimal circular_{AWGN}-16QAM[6] and (4,12)circular-16QAM[7] in terms of phase noise.

3

Frame Structure

Frame structure has been adopted from the common public radio interface (CPRI) ver 4.2 [8]. The CPRI standard defines the interface of base stations between the radio equipment controllers in the standard, to local or remote radio units, known as radio equipment. The companies involved in defining the specification are Ericsson AB, Huawei Technologies Ltd., Nokia Siemens Networks and Alcatel-Lucent. Nortel had been a part of CPRI for initial specification development but left in late 2009 [27]. CPRI has focused on hardware dependent layer (layer 1 and layer 2). The CPRI standard ensures the technology evolution with independence and little hardware adaptation. CPRI focuses on a radio base station design that divides the radio base station into a radio and a control part and by specifying one new interface - the only and unique radio driven interconnect point within base stations.

The reason for choosing CPRI is the availability of intellectual property (IP) block [28]. This reduces the time for implementing it in hardware. Furthermore, in built synchronization capabilities makes it suitable for adding time and frame synchronization. Finally CPRI is scalable which is an added benefit. Depending on the scenario, line rate can be changed making it possible to operate in different data rate conditions.

The reason behind defining the frame structure is to have a uninterrupted, structured and monitored running link. This chapter is organized to give an overview of the structure defined for 10Gbps microwave link under the CPRI format [8]. A bottom to top approach is used. Basic frame structure is firstly defined then the discussion is ended by the hyper frame structure and link control parameters.

3.1 Frame Terminology

The frame terminologies are the same as defined in [8]. Word number within a frame is denoted by W , each bit within W is given by B . Each BYTE in a word is addressed by index Y . For basic frame number X will be used and the hyper frame number is denoted

Table 3.1: Word Length and Control Word Position[8]

Line Rate [Mbit/s]	Word Length [Bit]	Control Word Position
614.4	T=8	Z.X.0
9830.4	T=128	Z.X.0, Z.X.1, Z.X.2, Z.X.3, Z.X.4, Z.X.5, Z.X.6, Z.X.7, Z.X.8, Z.X.9, Z.X.10, Z.X.11, Z.X.12, Z.X.13, Z.X.14, Z.X.15

by Z. When addressing a specific frame within a hyper frame, Z, the address Z.X.Y will be used.

3.2 Basic Frame Structure

CPRI model has parameters designed for the universal mobile telecommunication system (UMTS) . The basic frame structure has a length of 260.41267ns. Each basic frame consists of 16 words. Out of 16 words, 15 are data words ($\mathbf{W} = 1, 2, \dots, 15$) and one is the control word ($\mathbf{W} = 0$). Thus 1/16 of the basic frame duration is dedicated to control word and the rest for data. The length of each word varies with different line rate.

For this thesis, line rate of 9830.5 Mbit/s is used for this with a word length of 128 bits. This higher line rate is derived by scaling the basic line rate of 614.4 Mb/s sixteen times. With the increase of the line rate, length of the word is increased accordingly. Table 3.1 summarizes the basic line rate and proposed line rate with word length and control word information. During transmission a control word is sent first followed by the IQ data words. Each word is 8b/10b encoded for tracking of error during transmission. For maintaining DC balance on the transmission wire, scrambling is used in order to avoid long runs of 1's and 0's.

Table 3.2: CPRI line rate with frame positions

CPRI line Rate [Mbits/s]	Z	X	W	Y	B
614.4				0	0,1,...,7
1228.8	0,1,2,...,149	0,1,2,...,255	0,1,2,...,15	0,1	0,1,...,15
9830.4				0,1,2,...,15	0,1,...,127

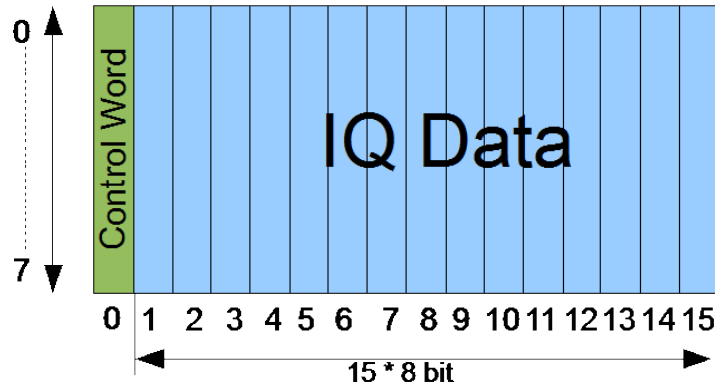


Figure 3.1: Basic Frame Structure[8]

The basic frame structure for the 9830.4Mbit/s line rate is shown in Figure 3.4. The dot on the right side of the image represent each byte of the frame. Furthermore this also shows the transmission of the bytes at one instance of time. Thus at first instance of time all the control words are transmitted and then followed by the data bytes.

3.3 Hyper Frame Structure

Hyper frame consists of 256 basic frames. Formation of hyper frame ease the tracing of the control words which is further used for monitoring the link. A hierarchical frame distribution from 10ms CPRI frame to basic frame is shown in the Figure 3.2. Each

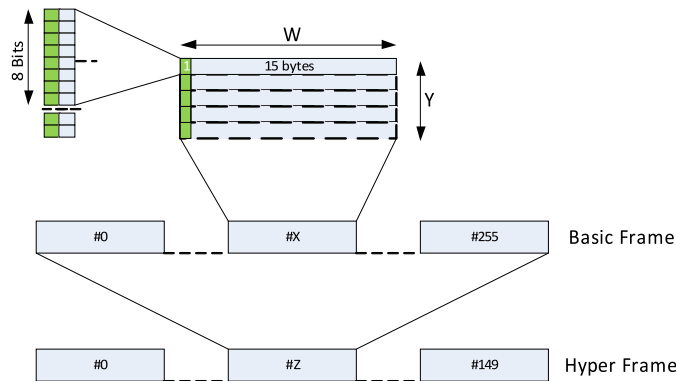


Figure 3.2: Illustration of the frame hierarchy

control words in the hyper frame is assigned different functionality for maintaining and acquiring the information of the link, which can be categorized as:

- Synchronization: it includes the data required for the frame synchronization and time alignment. It comprises of specific sequence of 1s and 0s from which the timing information can be extracted. Then based on this information the sampling point can be shifted to the optimal sampling point. It also helps in locating the start and end of each frame.
- L1 In band Protocol: It includes the signalling information required to keep the link in a running condition. This information includes the radio signal strength, frame loss, and link start up.
- Control and Management Data: This entity consists of the control and management information between the radio equipment, radio equipment controller, and is shared with higher layers.

The 256 control word of the hyper frame is arranged into 64 sub channels having 4 control word each. If N_s is the sub channel number and its value ranges from 0 to 63, index of the control word is denoted by X_s and the value ranges from 0 to 3. As a result the control word in the hyper frame indexed by X is given by $X = N_s + 64 * X_s$. Figure 3.3 illustrates the sub channel in a hyper frame. Furthermore, the legend shows the category of each control word. With help of the characterization, specific control word can be addressed at any time of the transmission.

Ns	Xs			
	0	1	2	3
0	0	64	128	192
1	1	65	129	193
2	2	66	130	194
3	3	67	131	195
4	4	68	132	196
5	5	69	133	197
6	6	70	134	198
7	7	71	135	199
8	8	72	136	200
9	9	73	137	201
10	10	74	138	202
11	11	75	139	203
12	12	76	140	204
13	13	77	141	205
⋮	⋮	⋮	⋮	⋮
62	62	126	190	254
63	63	127	191	255

Legend	
Comma Byte	
Synchronization and timing	
Slow C & M link	
Extended IQ Data	
L1 Inband Protocol	

Figure 3.3: Sub channel Within a Hyper Frame[8]

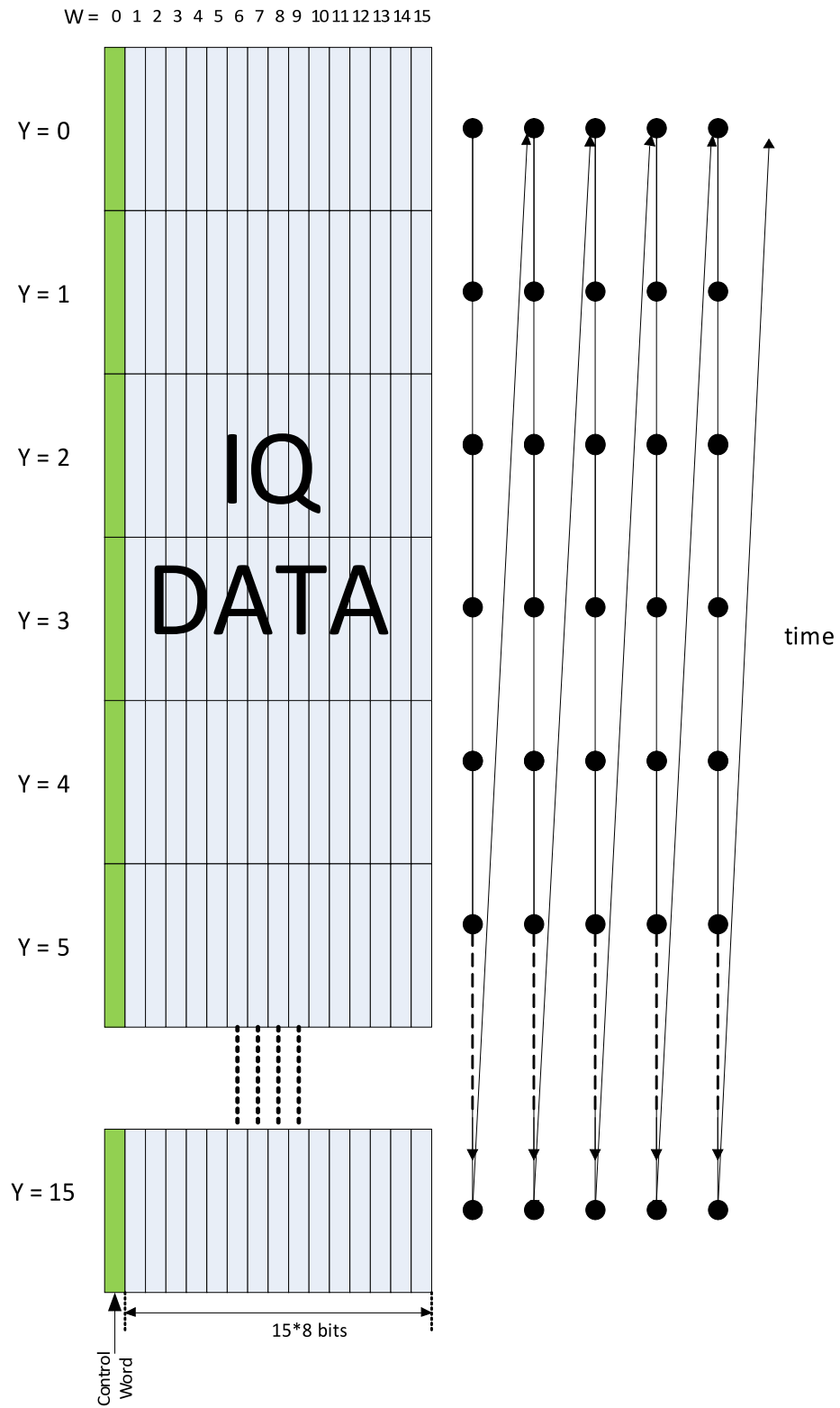


Figure 3.4: Frame Structure for Line rate 9830.4Mbit/s[8]

4

System Design

4.1 Field Programmable Gate Array

Field programmable gate arrays (FPGA) are programmable semiconductor devices that are based around a matrix of configurable logic blocks (CLB) connected by means of programmable interconnects. A general FPGA structure has three types of resources:

- Logic blocks,
- I/O blocks for connecting pins to the package,
- Interconnection wires and switches and
- Look up table

Logic blocks are arranged in a matrix form and the interconnection wires are organized as horizontal and vertical routing channels between row and columns of logic blocks. The routing channels contain wire and programmable switches which allow the logic block to be connected in different ways. Programmable connection also exists between the input/output (I/O) blocks and interconnections wires. The actual number of programmable switches and wires in FPGA varies with type. A look up tables (LUT) differentiates FPGA's from application specific integrated circuits (ASIC). Look up table is a memory unit which has a one bit output, which is result of a certain input logic. These LUTs are the key components of FPGAs having 4-6 bit input which can be programmed by the user. Programming is achieved either by hardware programming language such as very high speed integrated circuit (VHSIC) hardware description language (VHDL), Verilog, or by computer aided design tools like LabVIEW and Simulink. The design tools translate the hardware descriptive language (HDL) code to routing map of FPGA built in blocks. In fact the development of design tools has allowed designers to use C language for implementing logic functions in FPGA.

The inherent parallelism of the logic resources on an FPGA allows for considerable computational throughput even at a low MHz clock rate which has made FPGA's the designer choice for high speed application. FPGA's have a wide range of application in areas of digital signal processing, image processing, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation, radio astronomy, metal detection and a growing range of other areas [29]

In this thesis Xilinx's Virtex 5 ML505 FPGA and Spartan 3A DSP development kits are used to perform proof-of-concept test as shown in Figure 4.1.

Table 4.1: FPGA Specification

Kit	Virtex 5 ML505	Spartan 3A DSP
FPGA	XC5VLX50T	XC3SD1800A
Clock	differential 200 MHz	125 MHz LVTTL SMT oscillator

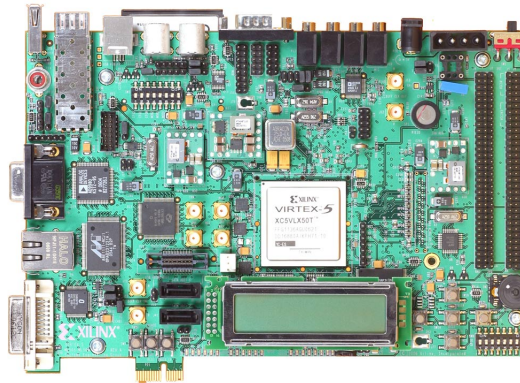
4.2 Development Design Flow

The design flow for the development of the modulator and demodulator is based on the approach from theoretical simulation to FPGA implementation. For simulation purpose Matlab and Simulink are used. Xilinx system generator is used for translating the Simulink design onto FPGA. FPGA design flow is shown in Figure 4.2. If at any stage an unprecedented result is observed, one has to step back to find the cause and revise the design. The process is repeated until correct results are observed at hardware testing stage.

4.3 Transmitter Design

Data handling is done in digital domain, and this requires very high speed ADC and DAC. The system setup has DAC and ADC working at 2.5 Gsamples/sec having dynamic input voltage. Furthermore, the hardware employing the transmitter and receiver has a maximum clock of 500MHz. If the system runs at double data rate (DDR) then the maximum rate the system can address is 1Gbps, which is quite far from the 10Gbps mark. Another advantage of using FPGA is that it uses the pipe-lining for the processing. This gives the power of parallel processing. By converting the input data to parallel streams of data, one can effectively reduce the line rate within the FPGA while preserving the original line rate. Converting input bits to words of 4 bits, then passing through 8 parallel streams reduces the line rate to $\frac{10G}{4*8} = 312.5MHz$. Using this approach the clock limitation is easily addressed.

Block diagram of the transmitter is shown in the Figure 4.3. Transmitter is composed of three parts



(a) Virtex 5 ML505[30]



(b) Spartan 3A DSP[31]

Figure 4.1: FPGA Board use in project

- Framer,
- Forward error correction encoder and
- Symbol Mapper.

4.3.1 Forward Error Correction

The FEC encoder is added at this stage to introduce additional redundancy to the data. This will help in detecting errors. As previously discussed, within the hardware, data is paralleled to 8 streams, and for each stream an individual FEC encoder generates encoded data. The FEC encoder runs on 4 bit input data and gives 16 bit data as output. Polynomial of depth 16bit is xored with 4 bits of data to generate a 16 bit code which is appended to the data. After encoding the data is passed to the symbol mapper or the modulator and FEC is reset to get new blocks of data.

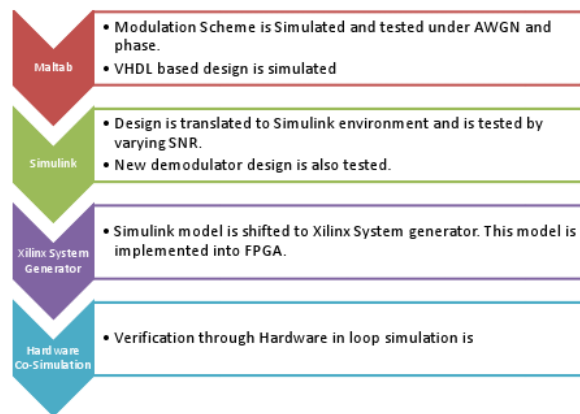


Figure 4.2: FPGA design work flow

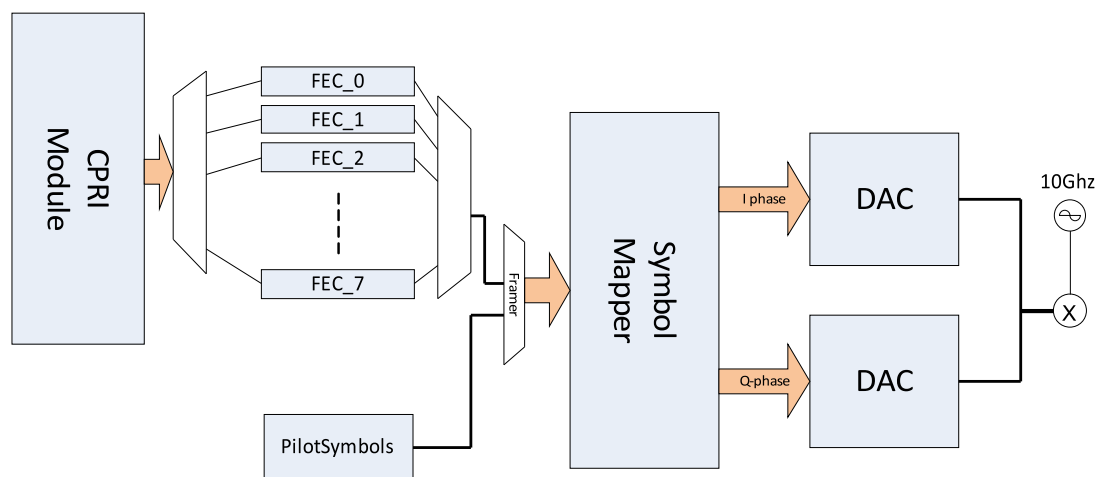


Figure 4.3: 10G Microwave Modem Transmitter Block Diagram

4.3.2 Framer

The framer adds pilot symbols to the incoming data. The pilot symbols are known both to the transmitter and receiver. This helps the receiver to estimate the channel condition and also to perform initial frame synchronization. For one set of 8 streams, 4 words are appended with sequence of symbol No. '8' and '9' by the framer. The transition from

symbol '8' to '9' represent physical transition from I to Q [32]. This helps in finding the midsync value. The final formatted data at one stream in frame format is illustrated in Figure 4.4.

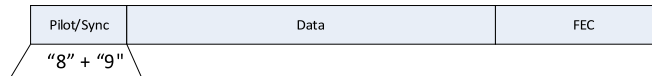


Figure 4.4: Framer Formatted data for one stream

4.3.3 Modulator

Circular-16QAM modulation has been used as a modulation scheme for this thesis. Much detail is provided in section 2.4.1 about the performance of this modulation. The modulator based on the symbol position, generates 6 bits and drives the DAC. Using double data rate and 4:1 mux output helps to limit the internal clock frequency to 1/8 of the symbol transmission frequency. After 4:1 mux, symbol rate is 2.5GSps which is the running speed of DAC. Each stream of 4:1 mux is running at 0.625GSps using DDR low voltage differential signalling (LVDS). There are a total of 2 DACs, each working for the I- and Q-phases.

4.4 Receiver

The receiver consists of the demodulator, FEC decoder, de-rotator, and synchronization loops. Block diagram for the receiver is given in Figure 4.5.

4.4.1 Demodulator

Function of the demodulator is to decode the symbol that is transmitted by the transmitter. Equipped with the demodulator is the de-rotator. The function of the de-rotator is to counter the effects of the phase noise which might have rotated the symbol. As discussed in 4.3.2 the pilot symbols are known to the receiver. Thus the de-rotator calculates the phase shift encountered by the pilot symbol and applies the counter phase shift to the coming block of the data. It is supposed that the phase shift remains the same for each frame block. To assist the pilot symbol, de-rotator is also equipped with a table for phase region of the constellation. This works on the symbol by symbol basis and phase change is counteracted by a complex multiplier.

The decision region drawn in section 2.4.3 is translated into the digital domain. The whole region is sectored to form a matrix. The value of the cell is determined by the region of the symbol. This matrix is called the decoding matrix and is shown in Figure

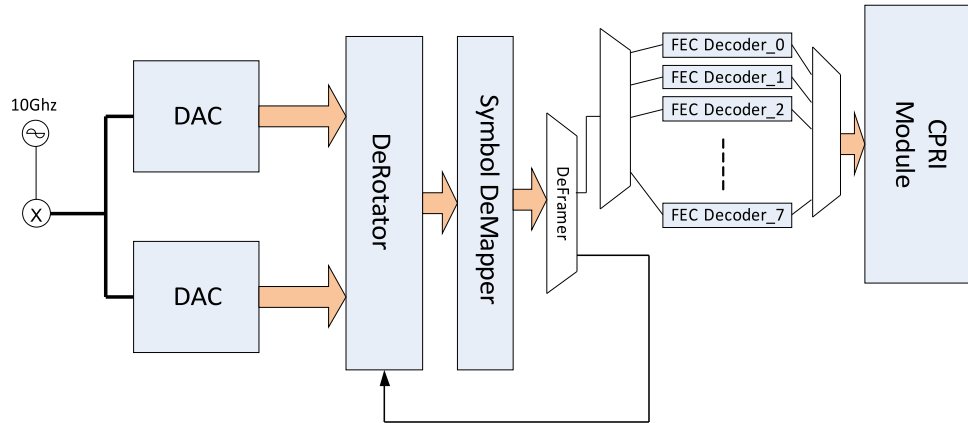


Figure 4.5: Block Diagram of Receiver

4.6. This matrix is used in the design for decoding the symbols. Selecting an effective matrix is a design challenge. The matrix is stored in the system memory. Memory required by the matrix can be obtained as 2×2^{bits} . Multiplication of 2 is because of the addressing the rows and columns and in the memory the matrix is mapped as a 1-dimensional array. It has been observed that 5bits is sufficient for the resolution for identifying the IQ-symbol. With help of decoding matrix, information regarding amplitude and phase error can be extracted. Regions are defined around the symbol which shows the displacement of the incoming symbol sample. If displacement of the received sample symbol is along the symbol then it will result in an amplitude error and if the displacement is along the curvature of the symbol then it will result in a phase error. The extra information can be used to log statistics and/or control amplitude and phase drift.

4.4.2 FEC Decoder

The FEC decoder calculates the syndrome based on the symbols received and compares it with the appended FEC code. If there is a valid match then it is concluded that the data bits are flawlessly received. Moreover, the FEC gets information about how many bits are in error, from which the error correction criteria can be developed in the future.

4.5 Simulation and Implementation

4.5.1 Simulink Model

A Simulink model is developed, in which modulator and demodulator is only considered and is shown in Figure 4.7. A Bernoulli binary generator is used for generating random

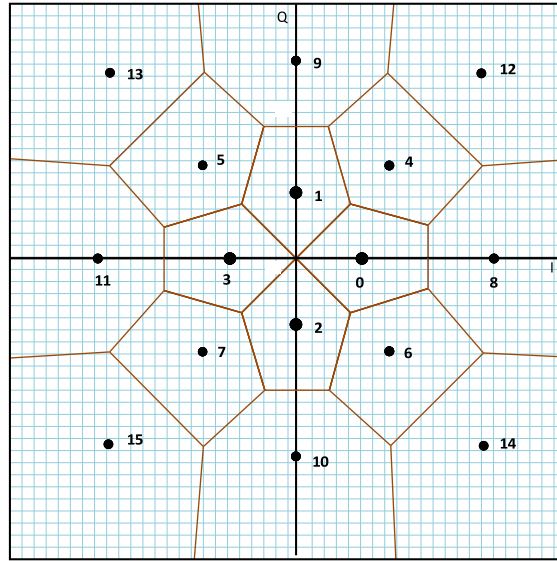


Figure 4.6: Circular-16QAM decision region in form of Matrix Grid

binary bits. These bits are converted to four bit integers which are used by the modulator to generate IQ symbols. Each integer is linked to a specific address in the read only memory (ROM) of the FPGA where the IQ values are stored. IQ Symbols are input to the receiver after passing through the channel. Amplitudes of the received symbols are controlled with a gain which sets it to be within the range of the ADC. Any amplitude lying outside the range of the ADC will be clipped off and the ADC would go into saturation. For the current scenario hit and trial methods have been used to get the signal within the range. This value should be such so as the received constellation does not collapse in terms of amplitude. This will lead to link loss. The demodulator described in previous section is implemented by help of ROM and the arithmetic logic unit (ALU). Finally, the decoded symbol is compared by the transmitted symbol for checking of error. The FEC only detects the error for the current setup.

4.5.2 System Generator Setup

After defining the design in the Simulink environment, it is transformed into the digital domain with the help of Xilinx System generator toolbox [33]. The block diagram of the transformed system is shown in the Figure 4.8.

Monte Carlo simulation is carried out on both models. Phase noise rate is kept constant at 10^{-3} and SNR is varied by changing the noise power keeping signal power at a constant level. The results are illustrated in form of curves shown in Figure 4.10. It is seen that both models perform equally well with little degradation in system generator setup curve, which is due to the quantized value of the input signal because of fixed

point notation.

4.6 Hardware in Loop Simulation

Xilinx system generator tool box provides basic elements for implementing the design into hardware with less complexity and optimized performance. System Generator provides abstractions that allows one to design for an FPGA largely by thinking about the algorithm that needs to be implemented. System Generator is particularly useful for algorithm exploration, design prototyping, and model analysis [34].

System Generator provides hardware co-simulation, making it possible to incorporate a design running in FPGA directly into a Simulink simulation. “Hardware Co-Simulation” compilation targets automatically create a bitstream and associate it to a block. When the design is simulated in the Simulink, results for the compiled portion are calculated in hardware, in our case is FPGA. This allows the compiled portion to be tested in actual hardware and can speed up the simulation dramatically.

4.6.1 Hardware Setup in loop

First step is to setup the hardware platform. The hardware used is Xilinx Spartan-3A DSP 1800A Starter Platform shown in Figure 4.1, which is connected to the host pc with either JTAG [35] cable or ethernet cable. After configuring the hardware using the system generator hardware co-simulation block is created which incorporates the model developed in Simulink. Hardware co-simulation block is shown in Figure 4.9.

During simulation, a hardware co-simulation block interacts with the underlying FPGA platform, automating tasks such as device configuration, data transfers, and clocking. A hardware co-simulation block consumes and produces the same types of hardware co-simulation blocks signals that other System Generator blocks use. When a value is written to one of the block’s input ports, the block sends the corresponding data to the appropriate location in the hardware. Similarly, the block retrieves data from hardware when there is an event on an output port. To enhance the data transferring capacity, host pc and hardware are connected through point to point ethernet link. This allows the high data transmission which is limited by the JTAG serial link. Simulation shows that the modulator and demodulator in the hardware performed equivalent to the system generator model, which is evident by looking at the symbol error count at specific SNR.

4.6.2 Resource Utilization

The hardware resources that the aforementioned design utilizes is tabulated in Table 4.2. Comparing the used and available resources in spartan 3A DSP 1800 board, the design utilizes a small amount of the resource, which shows that the above design of modulator and demodulator design is not hardware intensive. One thing to notice is that the resource shown is only for the modulator and demodulator, other components

Table 4.2: Resource Utilization by Design

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	38	33,280	1%
Number of 4 input LUTs	223	33,280	1%
Number of occupied Slices	122	16,640	1%
Number of Slices containing only related logic	122	122	100%
Number of Slices containing unrelated logic	0	122	0%
Total Number of 4 input LUTs	235	33,280	1%
Number used as logic	212		
Number used as a route-thru	12		
Number used as Shift registers	11		
Number of bonded IOBs	36	519	6%
Number of BUFGMUXs	1	24	4%
Number of DSP48As	1	84	1%

have not been simulated. Actual resources would be known when the whole system is implemented in hardware.

4.7 Simulation Results

Monte Carlo method is also performed on hardware simulation and the results are illustrated in Figure. 4.10. The degradation of the FPGA curve compared to the theoretical in the current scenario is first due to the quantization error and the resolution of the decoding matrix. The fixed point notation used in the FPGA limits the number of digits after the decimal point, which results in a quantized value of the received sampled signal and in turn adds quantization noise to the overall system. In addition, the resolution of the decoding matrix outlined in Section 4.4.1 affects SER. However, if the resolution of decoding matrix is increased this will increase the number of bits required to address the memory, which in turn increases the latency and complexity of the demodulator implemented on the FPGA.

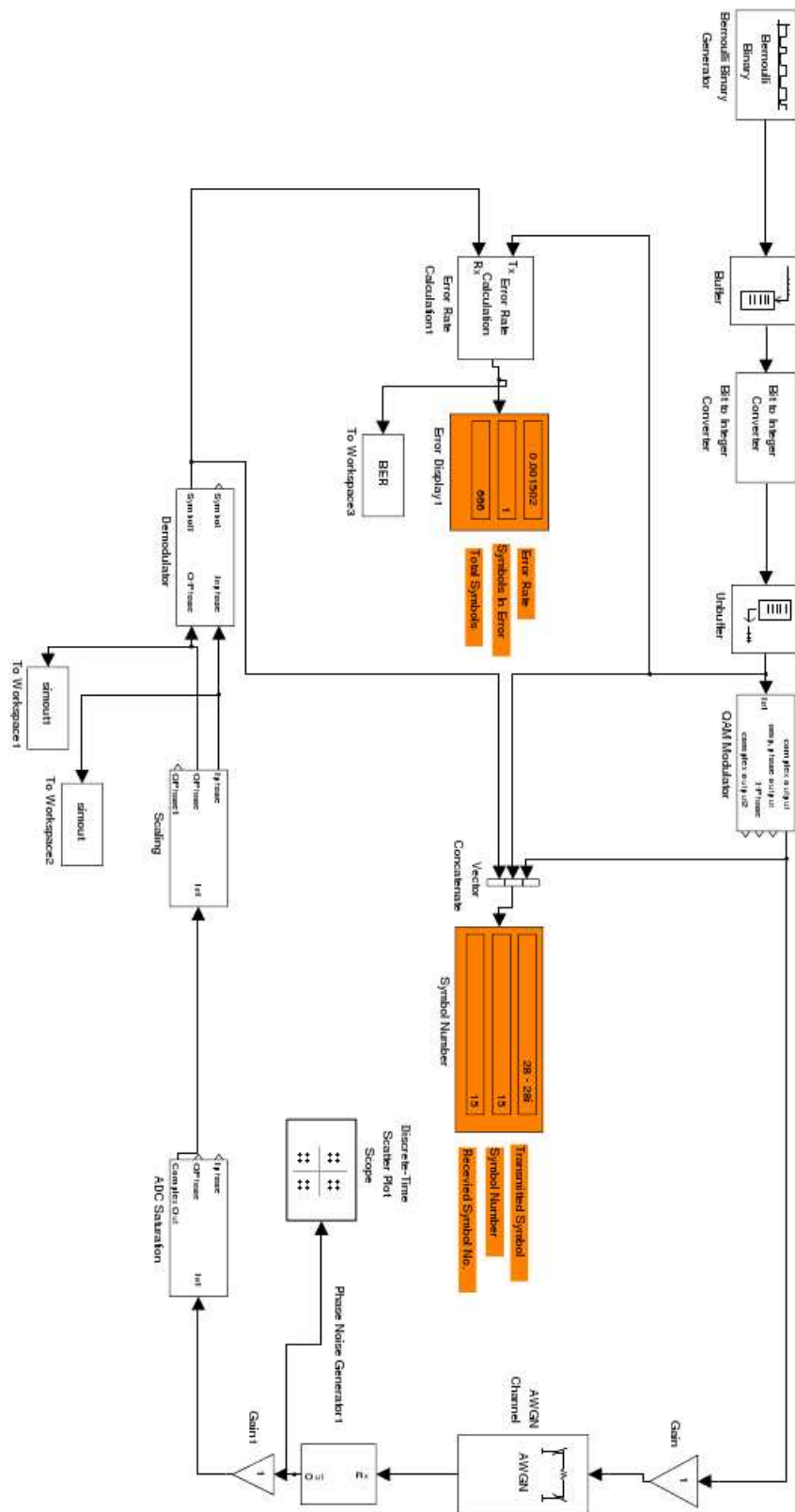


Figure 4.7: Simulink Model of Transceiver

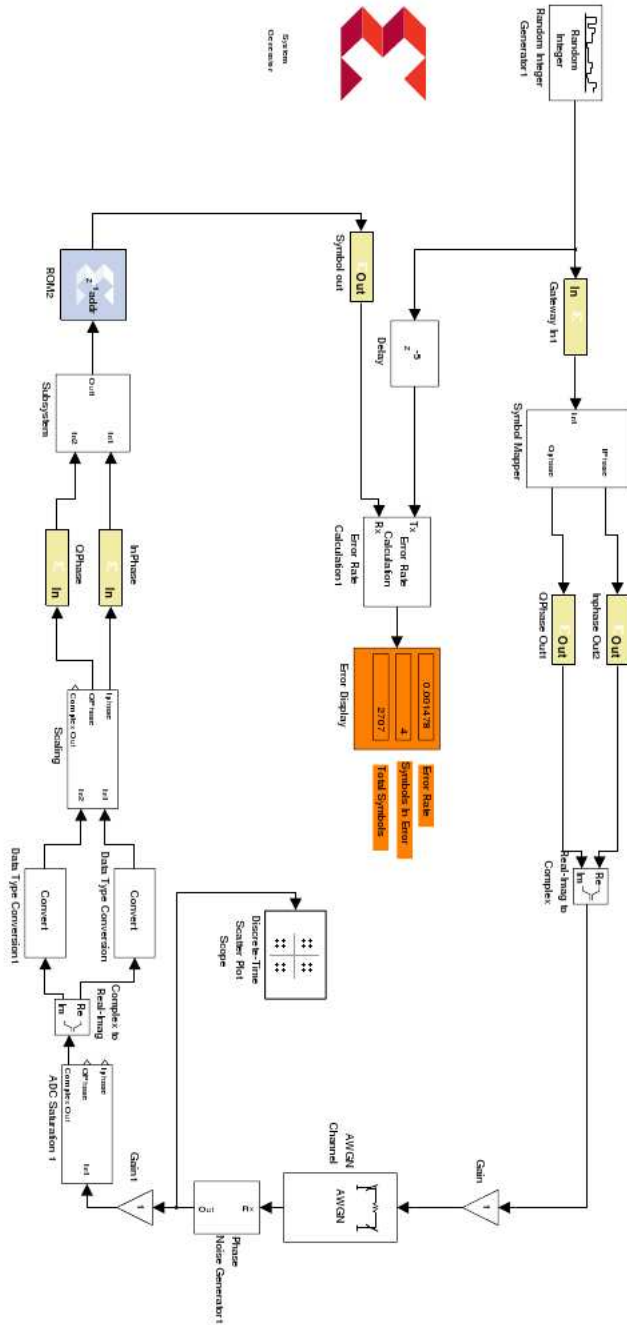


Figure 4.8: System Generator Implementation of the Transceiver

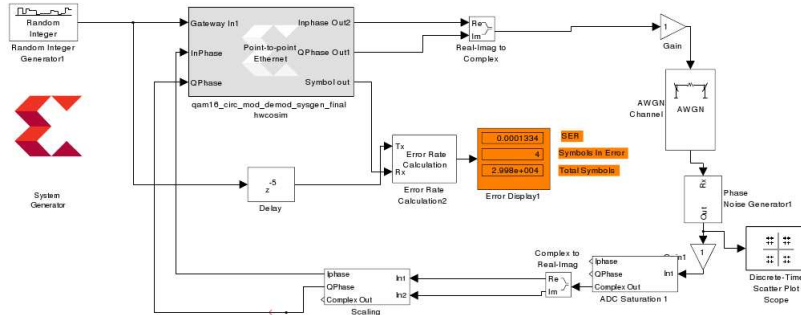


Figure 4.9: Co Hardware Simulation model in Simulink

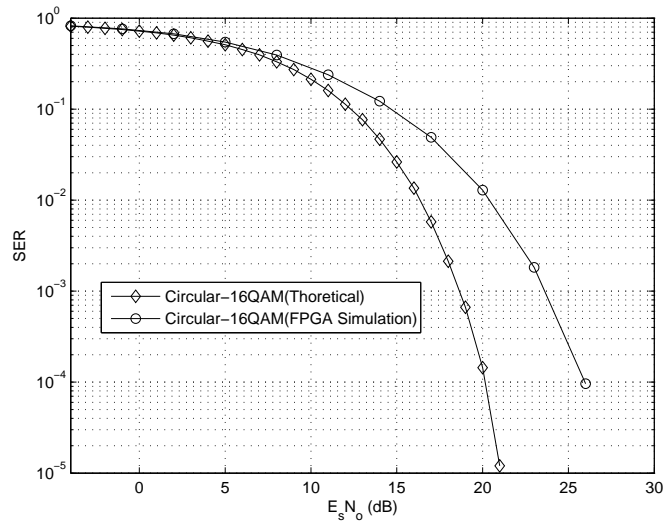


Figure 4.10: SER vs SNR curves for the Simulink model and hardware in loop simulation

5

Summary

5.1 Discussion

Circular-16QAM is a good alternative to rectangular-16QAM when phase noise is a limiting factor. It has been indicated by simulation that phase distribution of symbols in constellation is important design parameter when phase noise is a limiting factor. Further more oscillators need to be very accurate at E Band frequency, since slight jitter in the oscillator circuitry can introduce drift to the received signal. In addition the PLL needs to track the phase noise fast enough to control the phase drift.

As described in section 4.3, the ADC and DAC are working at sampling frequency of 2.5Gsamples/sec. Such a high sampling rate is achieved by limiting the outputs of the quantizer. In other words there is a trade off between quantizer's resolution and the ADC's sampling frequency. Furthermore, this also limits the chance to oversample the incoming signal to find the best sampling point. At this point, the sampler is working at a sampling frequency which is equal to the baud or symbol rate, and the chance of detecting an error increase as only one sample is taken. When one observes the eye diagram, the best sample point is the place where there is a maximum eye opening. If during transmission, at regular interval extra samples of the signal are recorded by delaying or advancing the sample point could be helpful in obtaining the best sampling point. In the thesis it was assumed that the received signal is within the range of the ADC, but in practical settings this is not the case. If at any time the power increases at the transmitter this will in turn increase the signal amplitude at receiver or noise in the receiver. The result would be an increase in the signal amplitude at receiver and the ADC will go into saturation region. Once the signal reaches the the saturation region it will be clipped off, causing loss of data. Therefore, to keep the signal within the range of the ADC, automatic gain control (AGC) should be used. AGC adjusts the gain of the power amplifier at the receiver and maintains a constant signal level at the input of the ADC. To monitor the power of the signal an averaging filter that average outs the

signal power can be employed. This filter has high memory and takes large samples on which an average is obtained. Based on the output of averaging filter, AGC's gain can be controlled so as to keep the amplitude within the range. Furthermore, the decoding matrix discussed in section 4.4.1 can be used to simplify this process. Each symbol region can be further distinguished into amplitude error and error free regions.

5.2 Conclusion

In this thesis, circular 16QAM has been discussed, which is a candidate for the modulation scheme for 10Gbps microwave link. Analytical results show that circular-16QAM perform better than its rectangular counterpart under phase noise. Further it also outperforms the other circular constellation that have been discussed in the literature. Quantization noise can also become a limiting factor, so when designing the system it should be also mitigated. Further more, advancement in digital signal processing techniques in FPGA has enabled the implementation of a digital modulation scheme with little complexity.

5.3 Future Work

Currently 10Gbps microwave link is under development and considering the whole transmission link much work can be done.

- Theoretical model can be developed which can handle other channel models and also including the FEC.
- Every link requires synchronization where as in the thesis perfect synchronization is assumed. Work can be carried out on how to perform synchronization when we have limited sample of data, which is running at such high speed. Time synchronization, frame synchronization and phase synchronization can be good topic to work on.
- Algorithm or criteria can be developed for how the AGC should be working.

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A

Appendix A

A.1 SEP in presence of Phase Noise

A.1.1 Binary Phase Shift Keying

As discussed in earlier in thesis, modulation can be achieved either by mapping bits onto changing amplitude or phase or frequency of the signal. If one bit is used to alter one of the aforementioned characteristics of a signal then it is called a binary shift keying, and if it is used to alter the phase then it gives us BPSK. Observing the IQ plot Figure A.1 of BPSK, it is found that the symbol lie on the I-plane and Q-plane.

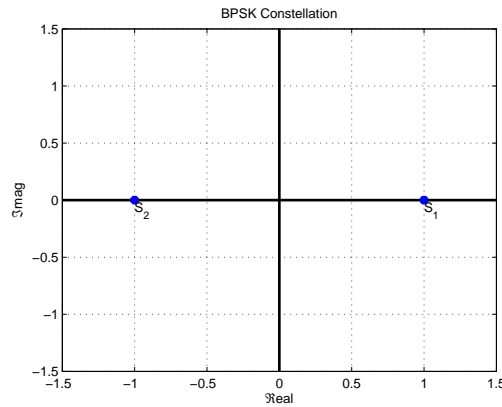


Figure A.1: BPSK IQ Plot

Pdf of gaussian function is given in (A.1) where $\mu = 0$ & $\sigma^2 = \frac{N_o}{2}$. Under AWGN noise the received signal is written as $y = s_1 + n$ & $y = s_2 + n$. Based on the received

signal it can be said that the mean of the original gaussian function is shifted to S_1 & S_2 and the conditional PDF can be written as (A.2) & (A.3) respectively.

$$p(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \quad (\text{A.1})$$

$$p(y|S_1) = \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_1)^2}{N_o}} \quad (\text{A.2})$$

$$p(y|S_2) = \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_2)^2}{N_o}} \quad (\text{A.3})$$

Conditional probability can be written as

$$P_e(y|S_1) = \int_{-\infty}^0 \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_1)^2}{N_o}} dy \quad (\text{A.4})$$

$$P_e(y|S_2) = \int_0^{\infty} \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_2)^2}{N_o}} dy \quad (\text{A.5})$$

With AWGN noise the received symbol is also affected with phase noise. Phase noise rotates the symbol by θ and can be written as multiplication with transmitted symbol. Thus the received symbol can be written as $y = S_1 e^{j\theta} + n$ & $y = S_2 e^{j\theta} + n$. As it is known that in BPSK there is no complex part so it can be assumed that only the real part of phase noise effect received symbol and can be written as $y = S_1 \text{real}(e^{j\theta}) + n$ & $y = S_2 \text{real}(e^{j\theta}) + n$. Now using this assumption and replacing in (A.4) and (A.5) will give us (A.6) and (A.9) respectively.

$$P_e(y|S_1) = \int_{-\infty}^0 \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_1 \text{real}(e^{j\theta}))^2}{N_o}} dy \quad (\text{A.6})$$

$$P_e(y|S_2) = \int_0^{\infty} \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_2 \text{real}(e^{j\theta}))^2}{N_o}} dy \quad (\text{A.7})$$

now solving (A.6)

$$\begin{aligned}
P_e(y|S_1) &= \int_{-\infty}^0 \frac{1}{\sqrt{\pi N_o}} e^{-\frac{(y-S_1 \operatorname{real}(e^{j\theta}))^2}{N_o}} dy \\
z &= \frac{(y - S_1 \operatorname{real}(e^{j\theta}))}{\sqrt{N_o}} \\
dy &= \sqrt{N_o} dz \\
\text{change of limits will be } &(-\infty \frac{S_1 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}}] \\
&= \frac{1}{\sqrt{\pi}} \int_{-\infty}^{\frac{S_1 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}}} e^{-z^2} dz \\
&= \frac{1}{\sqrt{\pi}} \int_{\frac{S_1 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}}}^{\infty} e^{-z^2} dz \\
P_e(y|S_1) &= \frac{1}{2} \operatorname{erfc} \left(\frac{S_1 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}} \right) \tag{A.8}
\end{aligned}$$

similarly solving for S_2 will give (A.9)

$$P_e(y|S_2) = \frac{1}{2} \operatorname{erfc} \left(\frac{-S_2 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}} \right) \tag{A.9}$$

Probability of error for BPSK can be written as

$$P_b = p(S_1)p(y|S_1) + p(S_2)p(y|S_2) \tag{A.10}$$

$$p(S_1) = p(S_2) = \frac{1}{2}$$

$$P_b = \frac{1}{2} (p(y|S_1) + p(y|S_2)) \tag{A.11}$$

$$P_b = \frac{1}{2} \left\{ \operatorname{erfc} \left(\frac{S_1 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}} \right) + \operatorname{erfc} \left(\frac{-S_2 \operatorname{real}(e^{j\theta})}{\sqrt{N_o}} \right) \right\} \tag{A.12}$$

$$S_1 = \sqrt{E_S}, S_2 = -\sqrt{E_S} \text{ This gives us}$$

$$P_b = \frac{1}{2} \operatorname{erfc} \left(\operatorname{real}(e^{j\theta}) \sqrt{\frac{E_S}{N_o}} \right) \tag{A.13}$$

A.1.2 Quadrature Phase Shift Keying

BPSK being a one dimensional modulation scheme is only effected by the real part of the phase noise. Where as QPSK is two dimensional modulation scheme thus both components of phase noise play a contribution to the received signal. the way probability

of error had being solved for BPSK similar approach is taken for QPSK. But the difference is that the symbol decision is broken down to Real and Imaginary components. The Symbol Error Probability for QPSK in presence of phase noise is formulated and is given in (A.14).

$$\begin{aligned}
 P_b = & \frac{1}{2} \operatorname{erfc} \left((\cos \theta - \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) + \frac{1}{2} \operatorname{erfc} \left((\cos \theta + \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) + \\
 & \frac{1}{4} \operatorname{erfc} \left((\cos \theta + \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) \operatorname{erfc} \left((\cos \theta - \sin \theta) \sqrt{\frac{E_s}{2N_o}} \right) \quad (\text{A.14})
 \end{aligned}$$