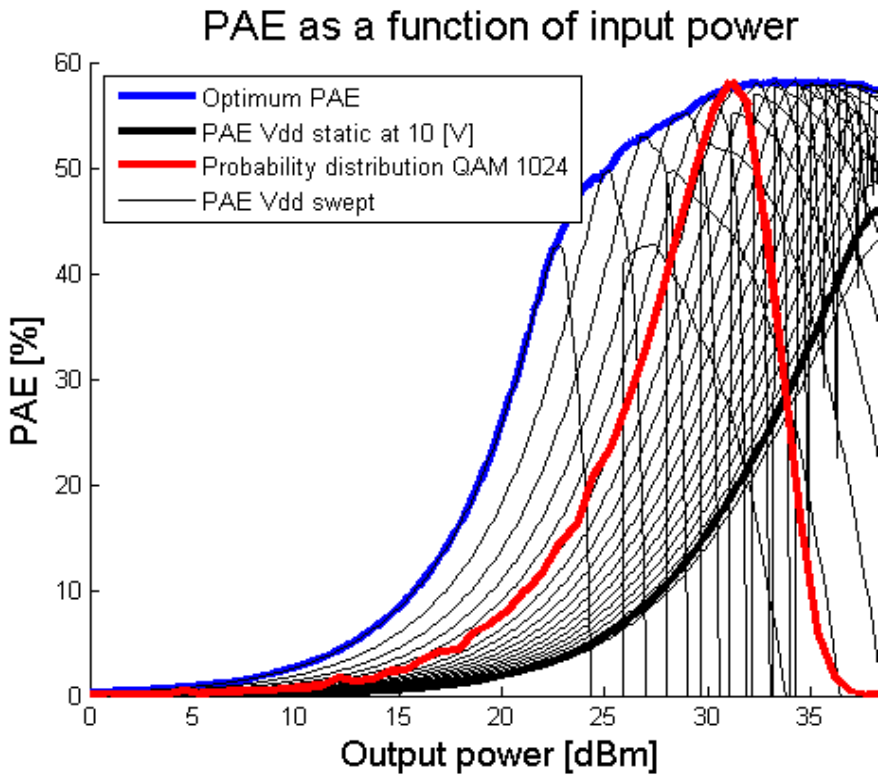
CHALMERS



Supply modulation study for Ericsson MINI LINK

Master of Science Thesis in Wireless and Photonics Engineering

BJÖRN HERRMANN

Department of Microtechnology and Nanosciency
Division of Microwave Electronics Laboratory
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden, 2011

Abstract

This report presents a feasibility study of envelope tracking for Ericssons radio link system. The analysis is done based on a model of an existing 7 GHz GaAs Power amplifier. From the on the model based analysis the theoretical PAE was found to be 50% compared to the 15% achieved through static biasing.

The high capacity radio links which were the basis of this study requires bandwidths up to 100 MHz. Implementing envelope tracking on such a systems introduces problems both for linearization and supply modulation efficiency. By introducing an iterative peak tracking low pass this report shows that the PAE still can be improved by at least 5% with a low efficiency supply modulator. Widening the study and investigating the effect of modulating the supply of the whole amplifier chain showed a potential improvement of 10%

The trade off between, reduced PAE improvement in the PA and efficiency improvement in the supply modulator when reducing the bandwidth reduction, was evaluated by simulating a simple envelope amplifier. Using lumped elements the maximum bandwidth achieved was 40 MHz.

Table of Contents

Abstract 1
Table of Contents 2
1 Abbreviations 3
2 Introduction 4
2.1 Dynamic supply modulation 5
2.2 Ericsson MINI LINK system 7
3 Characterization of Power Amplifier 8
3.1 Calculation of supply modulation signals 11
3.2 Input signal calculation 12
3.3 Analysis of PAE improvement potential 13
3.3.1 Dynamic drain bias modulation PAE improvement potential 13
3.3.2 Dynamic gate bias modulation PAE improvement potential 15
3.3.3 Switched drain bias modulation PAE improvement potential 15
4 Peak tracking bandwidth reduction 17
4.1.1 PAE vs EA bandwidth trade off 18
5 Linearity evaluation 19
5.1 DPD performance 19
5.2 Input spectrum 21
6 Verification of PAE potential calculations 22
6.1 Verification of PAE improvement calculations 22
7 Complete PA chain PAE 24
8 Envelope amplifier 26
8.1 Implementation 26
8.2 Choosing components 29
8.2.1 Components 29
8.3 Simulations 30
8.4 EA simulation results 30
9 Conclusions 33
10 Future work 34
11 References 35

1 Abbreviations

PA	(Power Amplifier)
PAE	(Power Added efficiency)
DLM	(Dynamic Load Modulation)
DSM	(Dynamic Supply Modulation).
ADS	(Advanced Design System)
DPD	(Digital predistortion)
QAM	(Quadrature amplitude modulation)
PAR	(Peak to average ratio)
DAC	(Digital to analog converter)
RF	(Radio Frequency)
DC	(Direct current)
MSE	(Mean Squared Error)
FET	(Field Effect Transistor)
EER	(Envelope elimination and restoration)
ET	(Envelope tracking)
EA	(Envelope amplifier)
2DLUT	(2 dimensional look up table)
CW	(Constant Wave)
LPF	(Low Pass Filter)
DAC	(Digital to analog converter)

2 Introduction

In all electronic devices the need for managing power consumption is ever present. Two important factors contributing to this demand are the cost and heat dissipation associated with high energy consumption. An important parameter in determining the maximum distance between two radio links in the transmitter output power, which in turn is limited by internal heat dissipation in the PA (Power Amplifier). By increasing the efficiency of the PA it is possible to increase radio link separation and or reduce the power consumption.

The history of PA development is rich in various methods for increasing the PAE (Power Added Efficiency), Most of these methods are focused on manipulating the gate bias and recovering the signal through filtering in the load network. In recent years state of the art performance has been achieved using Doherty, DLM (Dynamic Load Modulation) or DSM (Dynamic Supply Modulation).

The scope of this project is focused on investigating the feasibility of introducing the efficiency wise very promising DSM.

The aim of this project is to through simulations and numerical calculations to evaluate the feasibility and potential of introducing DSM in the radio link units manufactured by Ericsson.

Conceptually DSM is very simple where it seeks to dynamically change the transistor supply voltage to the PAE optimal level. What this means in practice is that for low output power we would like to lower the DC supply voltage and increase it for higher output power. By not having an unnecessary high bias voltage the power dissipation is decreased.

As a scheme for optimizing the PAE of power amplifiers, supply modulation has recently become recognized as a strong candidate for the next generation wireless standards [1].

2.1 Dynamic supply modulation

When designing a statically biased PA the bias voltages are set to manage the highest output powers. In order to support the highest output powers the bias current is unnecessarily high for signals below the peaks. This wasted energy is the theoretical background behind the concepts of EER (Envelope elimination and restoration) and ET (Envelope tracking), where the supply bias is controlled by the envelope of the RF signal via an EA (Envelope amplifier) as can be seen in Figure 1.

EER means separating the phase and amplitude information in the RF signal. The phase modulated, constant amplitude signal is then sent into the PA while the amplitude information is encoded through supply modulation. In ET the input RF signal is also amplitude modulated. It is this input amplitude which is being measured and fed to the EA supply modulator.

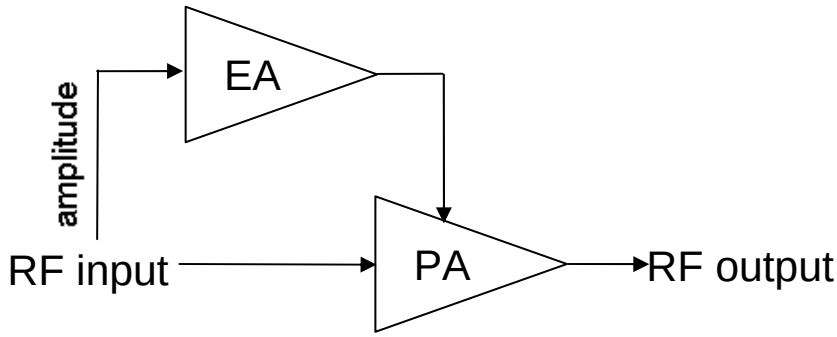


Figure 1. Envelope tracking architecture.

In this project it is assumed that the baseband signal is computed digitally using an ASIC (Application Specific Integrated Circuit). Digital signal processing allows for a nonlinear mapping of signal amplitude to supply signal. This in turn enables continuously driving the amplifier at its maximum PAE. In addition the digital processing of supply signals means the supply signal level can be fed to the predistorter. See Figure 2 for a description of the envelope tracking system considered in this work.

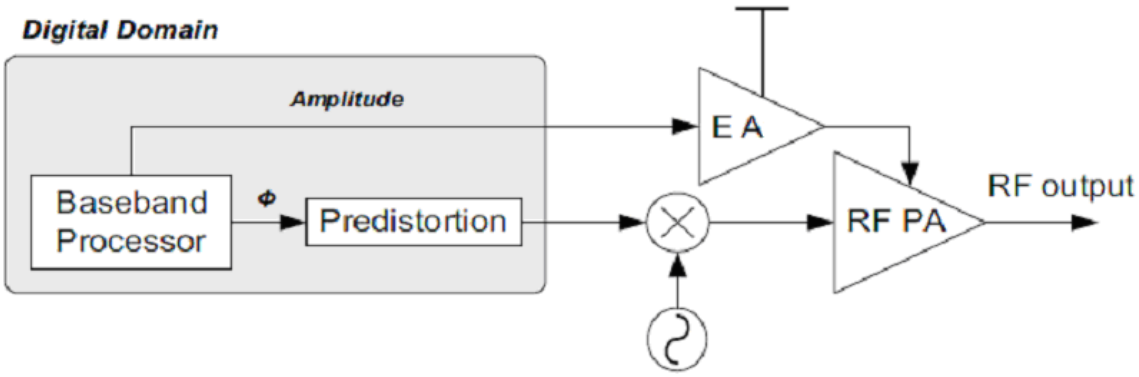


Figure 2. Basic concept of digitally controlled Envelope tracking.

From this general concept three specific cases have been chosen for evaluation. The feasibility of implementing them on the specific requirements of the Ericsson radio link system will be presented. The concepts are: Dynamic Gate Bias Modulation, Dynamic Drain Bias Modulation and Switched Drain Bias Modulation. They have different advantages and possibilities in terms of feasibility and potential PAE improvement.

From a PAE perspective dynamic drain bias modulation is the best solution. By directly controlling the drain voltage the dissipated power can be significantly reduced. Switching between discrete levels is merely a simplification where the deviation from the dynamic case is limited by the number of levels and switch speed. In Figure 3 a time domain description of a switched and continuous drain modulation is seen. The origin of this envelope signal is a QAM-1024 modulated carrier. High orders of modulations have implications for the probability distribution, where the highest peaks become increasingly rare. For such signals switched solutions could have an increased potential. Another simplification from the full optimum signal of Figure 3 is a peak tracking bandwidth reduced version. In this case of course the bandwidth has to be traded for PAE improvement.

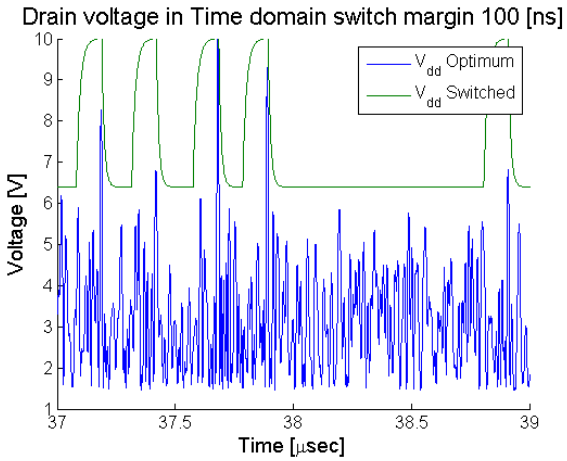


Figure 3. Example of drain voltage signal comparing optimum dynamic drain bias modulation and a switched taking rise and fall time into account.

For dynamic gate bias modulation the bias current for low RF input power is lowered. This might have implications on transistor gain, which have to be compensated for by predistortion. The drain current control is not as strong as when modulation the drain voltage directly, this lowers the maximum PAE improvement potential. The up side with gate modulation though is that the DC bias current entering the gate is virtually zero and thus significantly simplifies the modulator implementation compared to envelope tracking through the drain supply voltage.

2.2 Ericsson MINI LINK system

This study will be conducted by evaluating DSM applied to a system that exhibits the very unique requirements of a Radio Link system. Specifically a well behaving ADS (Advanced Design System) model of a 7GHz PA will be the subject of the study. This PA is designed to operate in class AB operation with $Id_{quiescent}$ set at 15.5% of Id_{ss}. At 7 GHz this amplifier has a gain of 10dB and a saturated output power of 39 dBm with a gain saturation of 5 dB.

The DPD (Digital predistorter) currently employed for the 7 GHz PA uses polynomials which are the inverse of the system. This DPD can not handle gain expansion and high orders of intermodulation. The systems on which DSM could be employed will most likely need a more sophisticated DPD because of the non linearity presented when the bias varies. With the present polynomial DPD the PA can support a 28dBm average output power and 9dB PAR (Peak to average). For this study it was decided that the averaged output power was going to be set to 30 dBm, since efficiency is increased for higher output powers. The PAE improvement to be evaluated is to be compared with the static performance at which the PAE is 15%.

Driving the amplifier beyond the point of compression of course means a loss of gain. This is compensated for by the DPD, the DPD can compensate for a maximum of 6 dB loss of gain. Allowing for higher DPD swing would require a DAC with larger dynamic range which in turn would have negative efficiency implications. This thereby becomes the maximum allowed system gain compression.

The back haul solutions for transporting information between base stations and network hubs require very high data rates. Achieving high data rates is often times done using high orders of modulation as well as a high symbol rates. In present Ericsson radios QAM (Quadrature amplitude modulation) signals with a modulation order up to 256 are used. With ever growing demands on link capacity these requirements will continue to increase. For that reason this study has been done with a 1024-QAM signal. The symbol rate was chosen to be 85% of the 112MHz channel spacing in question which is 95.2MHz.

An important signal characteristic is the PAR (Peak to average ratio). It is usually specified in dB and sets the maximum peak output power in relation to the average output power. In this study a 9 dB PAR limit was chosen, this because it was assumed to be close to what can be expected in future MINI LINK systems.

A study of current research literature in envelope amplifiers concluded that the highest bandwidth achieved is 20MHz [2]. In Figure 4 the spectrum of the QAM-1024 signal can be seen. The signal envelope does not have a well defined bandwidth but could be estimated to around 100MHz. The conclusion being that either the EA bandwidth has to be increased or this signal bandwidth reduced. This project aims to do both of those, while investigating interesting trade offs in terms of PAE and signal distortion. In almost all DSM research the main focus has been base station applications. The main differences between base station and Radio link PA's is that base stations have a higher output power and lower envelope bandwidth. This project will investigate if the higher modulated envelope bandwidth can be accomplished for the relatively low output power in radio links.

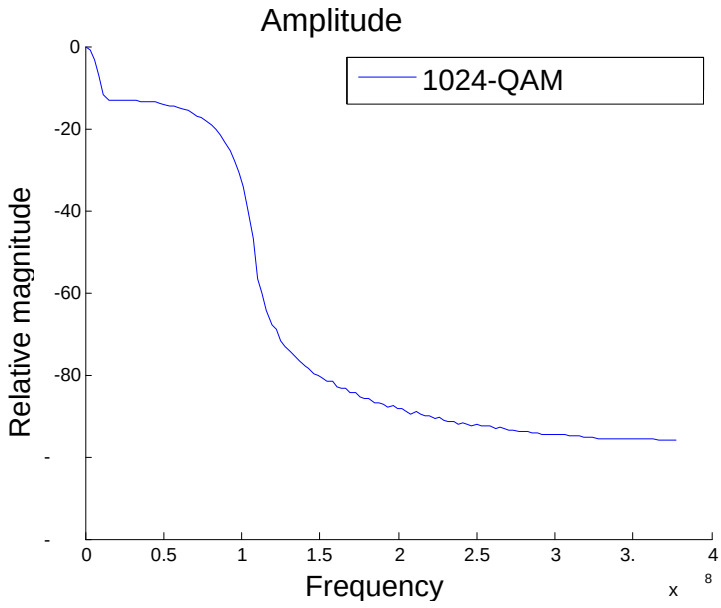


Figure 4. QAM-1024 envelope bandwidth.

An ideal DPD produces a signal that is the inverse of the system it is meant to linearize. From a frequency point of view this means an identical spectrum. This could pose a problem if the bandwidth in the DAC (Digital to analog converter) is limited, because frequency components outside the sampling range of the DAC causes aliasing. In this study the DAC bandwidth has been set to 500 MHz, to avoid aliasing the signal is filtered with an anti aliasing filter that has a cut off frequency of 170MHz. Since spectral broadening of the RF signal is expected for DSM this limit will be studied carefully.

3 Characterization of Power Amplifier

In order to calculate the PAE improvement potential a model of the 7 GHz PA was simulated in ADS. The transfer characteristics were retrieved by sweeping Gate/Drain Voltage and CW (Continuous Wave) input Power, while measuring output power and DC power consumption.

The simulations were done using harmonic balance simulation with an RF frequency of 7 GHz including 5´th order harmonics. In order to accurately predict the performance with some head room for a 1024-QAM signal P_{in} was swept between -40 dBm to 41 dBm and V_{dd} respectively between 1V and 12V. In order to prevent input mismatches from affecting the measurements an ideal isolator was placed at the input port of the PA.

For newer radio generations it is expected that the PA will be run with a lower conduction angle. Therefore the drain bias sweep was done at two different quiescent drain currents. The PA was designed for a gate voltage bias of -0.685V giving a quiescent drain current of to 400mA or 15.5% of Id_{ss}. By reducing the gate voltage to -0.810V $Id_{quiescent}$ was lowered to 200mA which is 6.7% of Id_{ss}.

The PA transfer characteristics were retrieved from harmonic balance simulations in ADS. The result of these simulations with the drain bias voltage swept between 1 V and 10 V can be seen in Figure 5 and Figure 6. It can here be seen that for relatively high input powers the dominant phenomena is self biasing resulting in very similar behavior for both bias points. We can in the figures also see a very sharp decline in gain when the contours go from horizontal to vertical.

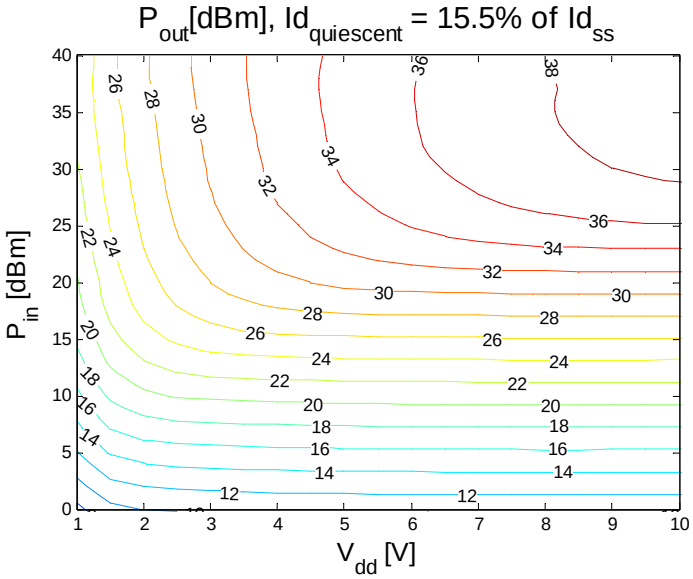


Figure 5. P_{out} as a function of V_{dd} and P_{in} simulated with $Id_{quiescent}$ = 15.5% of Id_{ss}.

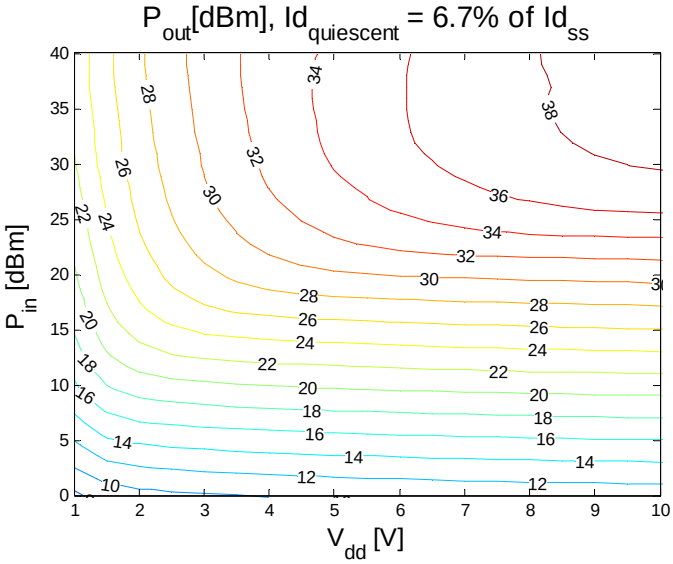


Figure 6. P_{out} as a function of V_{dd} and P_{in} simulated with $Id_{quiescent}$ = 6.7% of Id_{ss}.

In Figure 7 and Figure 8 the PAE contour plots for both bias points can be found. From these graphs we see that the PAE behavior is similar when both drain voltage and input power is high. For both lower drain voltages and lower input powers the PAE is increased in the deeper PAE case. Again the self biasing effect is seen from the fact that the top PAE region and above is very similar for both figures.

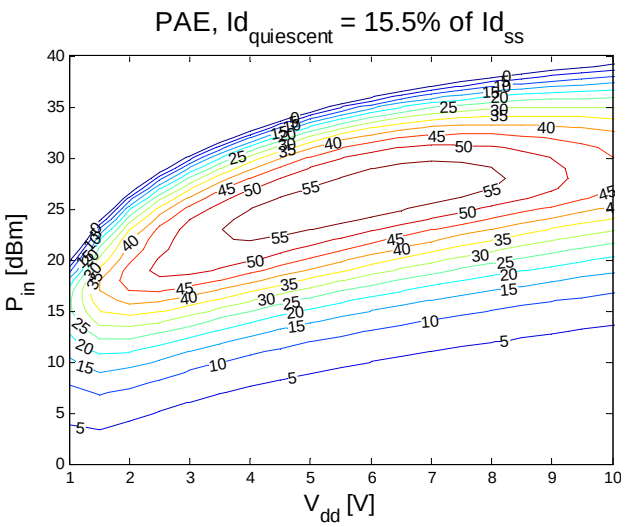


Figure 7. PAE as a function of V_{dd} and P_{in} simulated with $Id_{quiescent}$ = 15.5% of Id_{ss}.

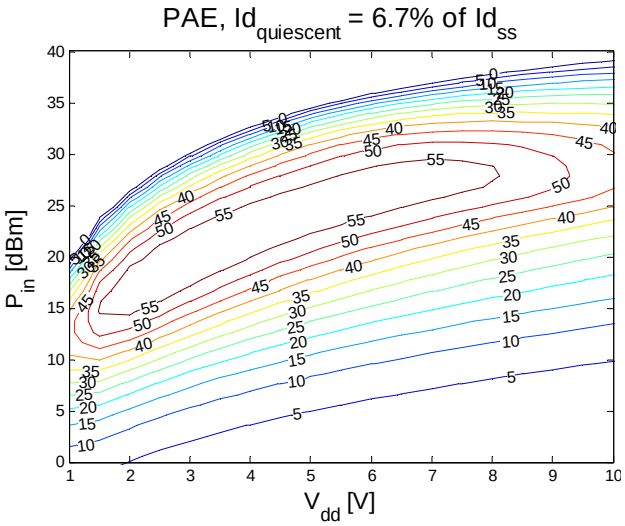


Figure 8. PAE as a function of V_{dd} and P_{in} simulated with $Id_{quiescent}$ = 6.7% of Id_{ss}.

In Figure 9 and Figure 10 the transfer characteristics with the gate swept between -1.5 V and -0.5 V are seen. We can see that for high power levels the gain is dependent upon gate voltage, with about 4 dB/V, while for small signals the transistor shuts down under -1V. For a swept input power the maximum PAE is found to always be over -1V which is before the transistor shuts down.

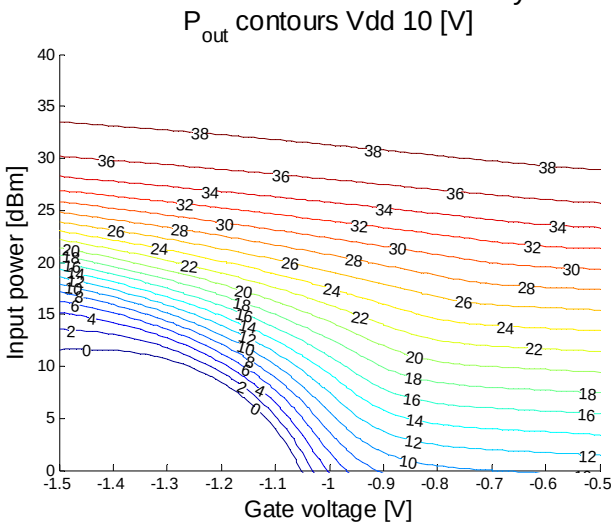


Figure 9. P_{out} as a function of V_{gs} and P_{in} simulated with V_{dd} = 10V.

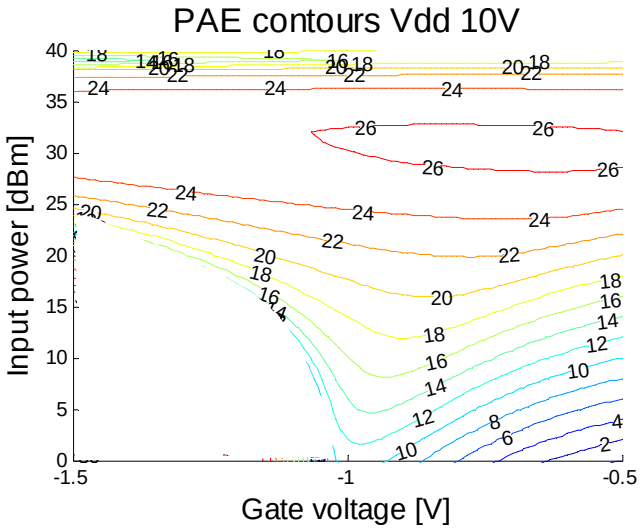


Figure 10. PAE as a function of V_{gs} and P_{in}.

Recalling that the average input signal power is below 20 dBm wee see that the potential PAE improvement is very small.

3.1 Calculation of supply modulation signals

Knowing the desired output signal, we can calculate the set of supply bias and input signal that produces not only the correct output but also maximizes the PAE. From the PA transfer characterization constant contour plots were calculated using MATAB resulting in Figure 11 and Figure 13. Numerically the point on each constant output power contour in Figure 11 that maximizes PAE was chosen, resulting in the black curve seen in both figures. Since this curve is not monotone at some points and also irregular it would make a poor mapping function. For that reason a polynomial fit of this black curve was used to calculate the full bandwidth control signals. To constrain the mapping functions appropriately a minimum gain and a minimum drain voltage was set. The minimum gain requirement was set to 5 dB since this is comparable with the performance of the DPD employed today. Examples of such a mapping function can be seen in Figure 12. As described in the next section a DPD is implemented using a 2DLUT, the DPD calculated Pin that corresponds to each output value via the Vdd polynomial is shown in Figure 14.

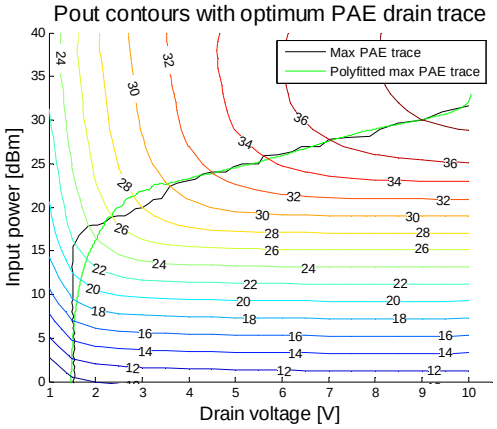


Figure 11. Optimum PAE trajectory and polynomial fit on top of with constant P0out contours.

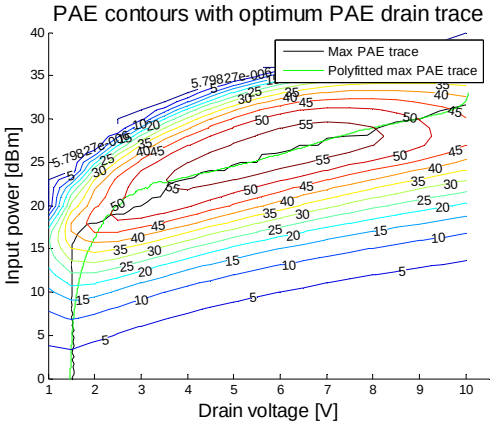


Figure 13. Optimum PAE trajectory and polynomial fit on top of constant PAE contours.

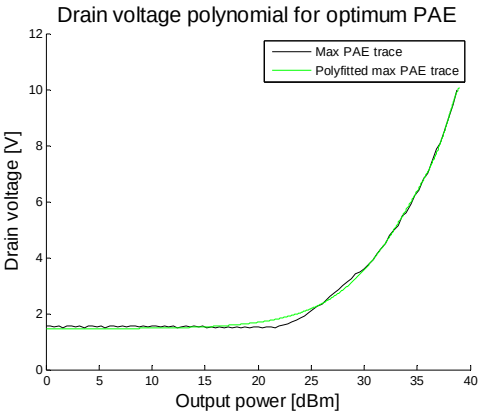


Figure 12. Example of drain voltage polynomial fitted onto the optimum trajectory.

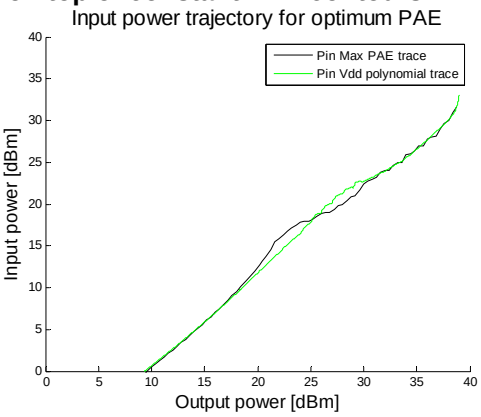


Figure 14. Example of Pin trajectory calculated from the V_{dd} polynomial.

3.2 Input signal calculation

In Ericsson MINI LINKS system the PA phase and amplitude distortion is compensated for by a polynomial DPD. These polynomials are calculated as the inverse of the amplitude and phase shift as a function of output power, commonly referred to as AM/AM and AM/PM. This polynomial predistortion could theoretically be employed also for a supply modulating system given that the memory effects are minor.

In this report special attention has been given to bandwidth reduction. Bandwidth reduction means there no longer exists a 1:1 relation between signal amplitude and supply signal. The input signal now has to be calculated using either a 2DLUT or a 2 dimensional polynomial. The implementation chosen for this study consisted in 2 2DLUTs (2 dimensional look up table) which represent the inverse of the PA and therefore through interpolation delivers the input signal that cancels the nonlinearities of the modulated PA.

Calculating this inverse 2DLUT was done using the data produced by the PA characterization. The sets of P_{in} and V_{dd} that produces constant P_{out} seen in Figure 15 were interpolated onto a mesh grid comprised of the desired V_{dd} and P_{out} range. This resulted in the 2DLUT seen in Figure 16 which is defined for all points below unit gain.

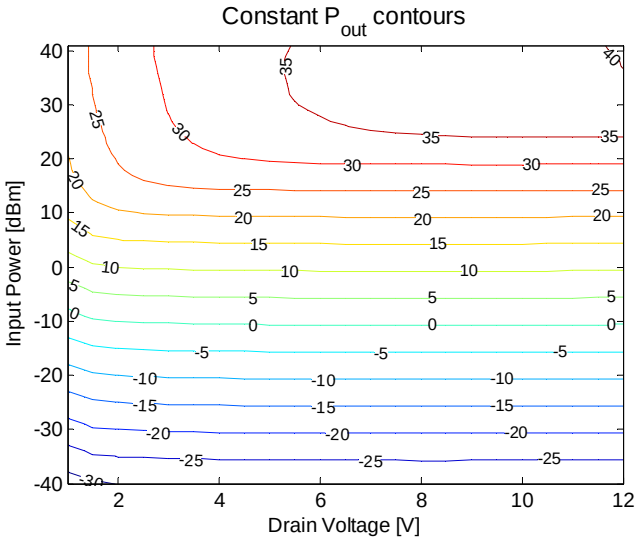


Figure 15. Constant Pout contours produced using the data from the PA characterization.

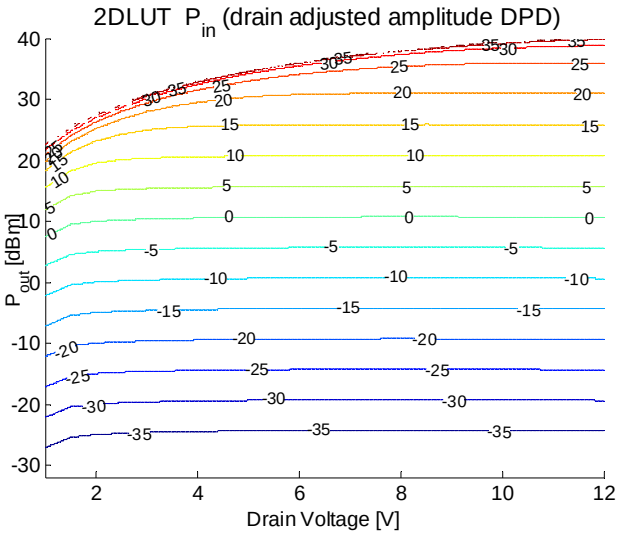


Figure 16. 2DLUT PAE as a function of Vdd and Pin simulated with Idquiescent = 6.7% of Idss.

What is important to consider when calculating the inverse 2DLUT is where the amplifier is intended to operate. Supply modulation means in the end to drive the PA in compression over a large portion of the amplitude range. This means that accuracy in the area close to the non defined zone is of great importance. By up sampling the mesh grid and also the Pout contour density for high output powers this issue can be resolved.

3.3 Analysis of PAE improvement potential

The PAE improvement potential has been evaluated numerically in MATLAB using the model created by the PA characterization. This was done by employing the following process:

1 Compute random 1024-QAM IQ signal.
2 Control RF bandwidth using raised cosine filter with a roll off factor of 0.17.
3 Normalize to desired output signal power.
4 Map output power to supply signal.
5 Through 2DLUT interpolate to find input signal.
6 Using a LUT model of the PA the DC power consumption was calculated.

Based on the PA characterization the possible PAE performance was estimated for the three modulation schemes. In the sections that follow the theoretical average PAE, for various signal powers is calculated. All evaluations in this section are done with a 1024-QAM signal with PAR limited to 9 dB. These calculations were done in MATLAB and without taking envelope amplifier efficiency into account.

3.3.1 Dynamic drain bias modulation PAE improvement potential

Using data from the PA characterization the PAE as a function of output power for various drain voltage levels is plotted in Figure 17. Note that the gate bias is set to 15.5% of $Id_{ss.}$ The dynamic range over which the PAE can be increased by controlling the drain voltage is compared with the probability distribution of a 1024-QAM signal. We see that the probability distribution is well covered within the V_{dd} range between 1V and 10V. From this information we can infer that further reducing the gate controlled $Id_{quiescent}$ will not substantially affect the maximum achievable PAE.-

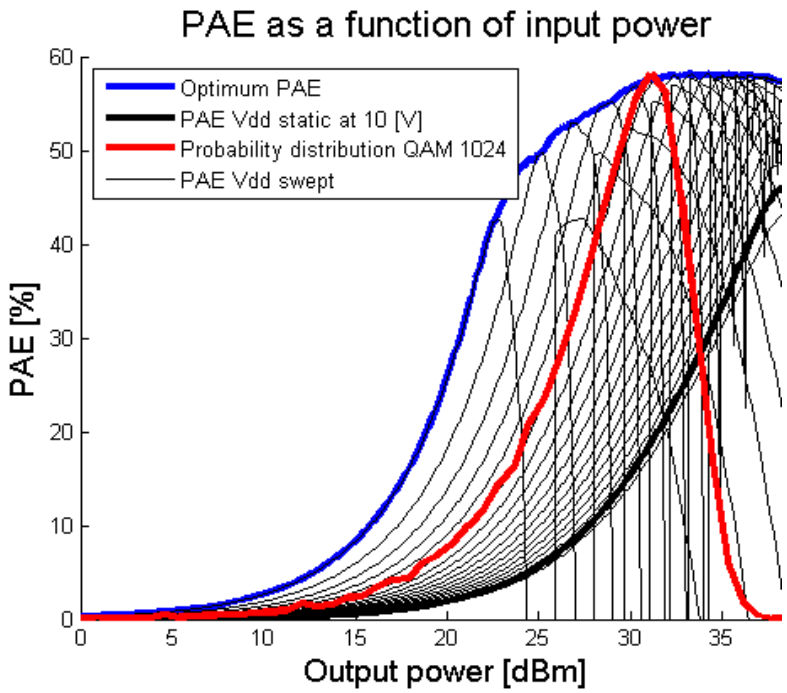


Figure 17. PAE as a function of output power for various drain voltage supply levels. Comparing the dynamic range for drain modulation with the probability distribution of a 1024-QAM signal. Vdd range from 1V to 12V, with gate bias set to 15.5% of Id_{ss}.

From the optimum PAE trajectory a polynomial fit was calculated. This polynomial was then applied to the RF signal where after the PA characterization was used to predistort the input signal and estimate the PAE. The result of these simulations can be found in Table 1. These PAE numbers refer to the PA PAE not taking the envelope amplifier into account.

Table 1. Simulated maximum PAE for dynamic drain bias modulation.

Average P_{out}	Average PAE
30dBm	53.6%
28dBm	51.1%
26dBm	47.1%

3.3.2 Dynamic gate bias modulation PAE improvement potential

In Figure 18 the dynamic range of gate modulation can be found. This shows the same message as seen earlier that the maximum average and peak PAE is much lower than for the drain modulation. But apart from that it becomes evident that the improvement potential, which is showed as the area between the blue and black line is very minor.

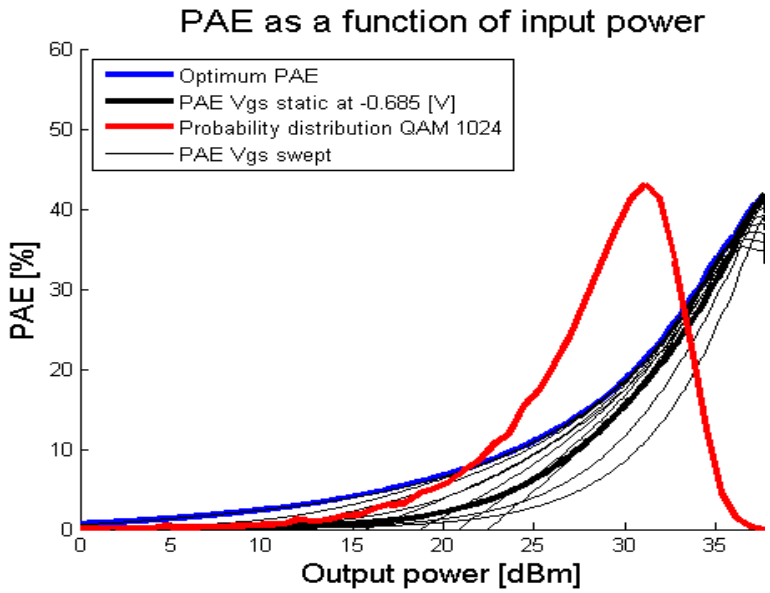


Figure 18. PAE as a function of output power for various gate voltage supply levels. Comparing the dynamic range of gate modulation with the probability distribution of a 1024-QAM signal. V_{gs} from -1.5V to -0.5V.

The PAE simulation showed that the maximum average PAE using gate modulation on this 7 GHz PA for a 1024 QAM signal is 18%.

3.3.3 Switched drain bias modulation PAE improvement potential

In instead of dynamic modulation the drain supply it was switched between two or more discrete levels. In

Figure 19 the PAE potential of such an implementation is found. The drain voltage levels are computed to within 0.25V be the PAE wise optimum set of levels. Since it is required to reach the highest peak one of the levels must always remain at 10V. From this simulation we see that an improvement to a PAE between 25% and 30% is possible given that it is possible to liberalize the distortion caused by switching.

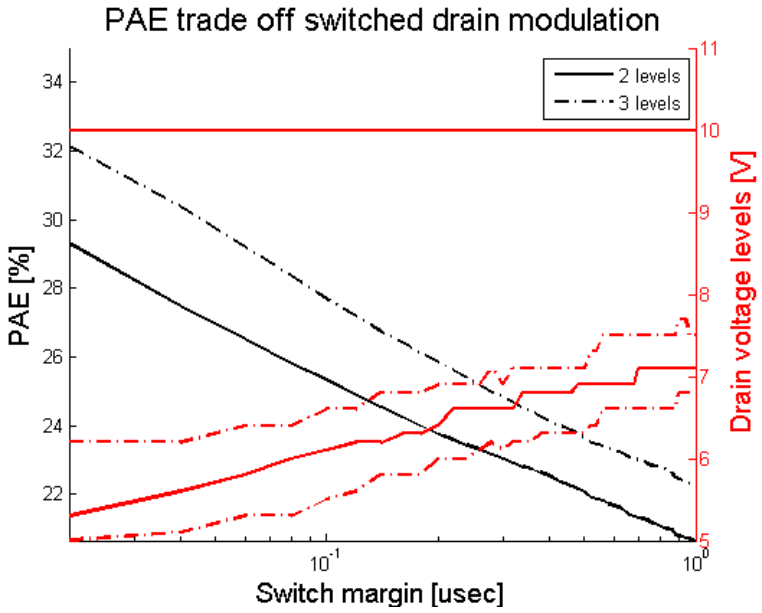


Figure 19. PAE improvement potential estimation for switched drain modulation. The term switch margin refers to the time between when a switched is set on and the value is reached.

The evaluation of the three different modulation methods led to the conclusion that the dynamic drain modulation was going the be the main focus. Specifically the bandwidth reduction schemes and their implications is the focus for the remainder of the study.

4 Peak tracking bandwidth reduction

For transistors in general, the dissipated power is increased with the operating frequency. Envelope amplifiers specifically follow the same relationship showing efficiency degradation and also linearity issues for higher signal bandwidths. This is one of the limiting factors for supply modulation [1]. It is with this knowledge in mind the idea of reducing the supply modulation signal bandwidth arises. Filtering however is not as straight forward as simply applying a FIR LPF, since the top supply voltage is needed in order to maintain gain and linearity for the peaks. This leads to the conclusion that a PTLPF (Peak Tracking Low Pass Filter) is needed.

In [1] the iterative filter described by Figure 20 was found. The principle of operation is to add the positive difference between the original polynomially calculated Vdd signal and its low pass filtered version. For every iteration the peaks will approach the desired level and thus produce the PAE optimized supply signal for a given cutoff frequency.

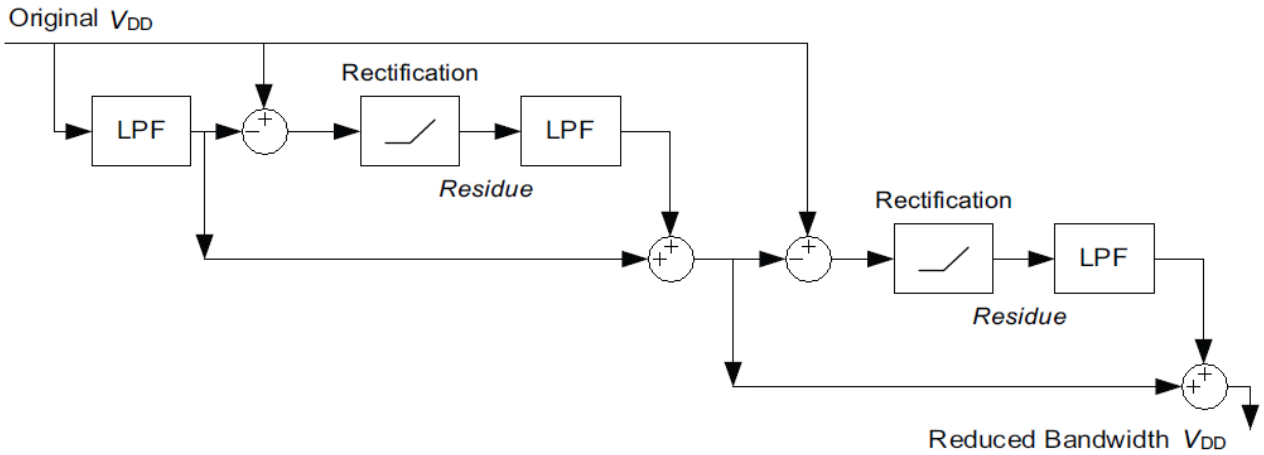


Figure 20. Schematic description of the iterative peak tracking low pass filter.

The design of this filter has the interesting characteristic stemming from the super positioning of the filtered signals. If the slope of the LPF applied to the residual signal is not steep enough the stop band content will add up. Letting these high frequency components propagate though to the EA would most likely cause linearity issues related to mismatches between supply and RF signal. During this master thesis project this problem has been solved by implementing the LPFs with 10´th order elliptical FIR filter which ha a very steep cutoff frequency and a very non linear phase response. The phase linearity issues were not addresses but rather ignored by using the “filtfilt” function in MATLAB, which lets the signal run through the filter in both forward and reverse direction resulting in a constant phase response.

Recalling from the conceptual description we could note that time alignment between supply and RF signals is crucial for the linearity and to a certain extent also efficiency. This is of course also an important consideration in the filter design, since frequency dependent delay would cause poor synchronization which in worst case means undesired compression and nonlinearities.

The peak tracking property is necessary while the level of the lower areas is a trade off between an increase in PAE and reduced gain and linearity.

4.1.1 PAE vs EA bandwidth trade off

Employing the peak tracking low pass filtering algorithm described in the method section resulted in the data presented in Figure 21. The result is a trade off number of filter iterations and the low pas filter cut off frequency. The limiting factor for number of filter iterations is the time delay it is translated into when implementing the filter. Low pass filter is in turn traded against efficiency in the EA achievable

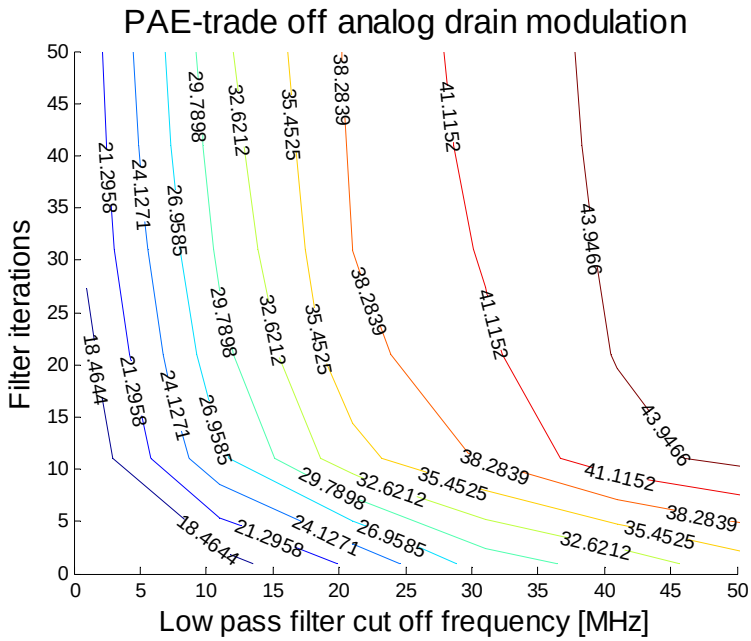


Figure 21. Trade off between LPF cut off frequency and number of filter iterations for bandwidth reduced dynamic drain modulation.

From Figure 21 we can conclude that this bandwidth reduction scheme requires more than 30 filter iterations. Further for filter cut off frequencies over 25 MHz the PAE dependence is not as strong.

5 Linearity evaluation

5.1 DPD performance

The DPD performance is evaluated in terms of the ability to adjust for the distortion in the PA. A common way to view the distortion is by looking at the AM/AM and AM/PM behavior. For a few selected envelope bandwidths this can be seen in Figure 22 and Figure 23. As can be seen in the figures, the static and infinite bandwidth lines constitute mapping functions between output power and control signals. But for the bandwidth reduced cases they turn into more of a statistical cloud. Already the non linear and non monotonic behavior of the infinite bandwidth curves would be a challenge for the DPD. This also leads to the conclusion that maybe there is a different way to calculate the optimum trajectory that minimizes that gain and phase variations.

For the AM/AM case the infinite and static lines set the boundaries for the probability clouds of the bandwidth reduced ones. The relation between the lines and clouds is slightly different for the AM/PM the case, instead the clouds become more similar to the static line for low frequencies and vice versa for high frequencies.

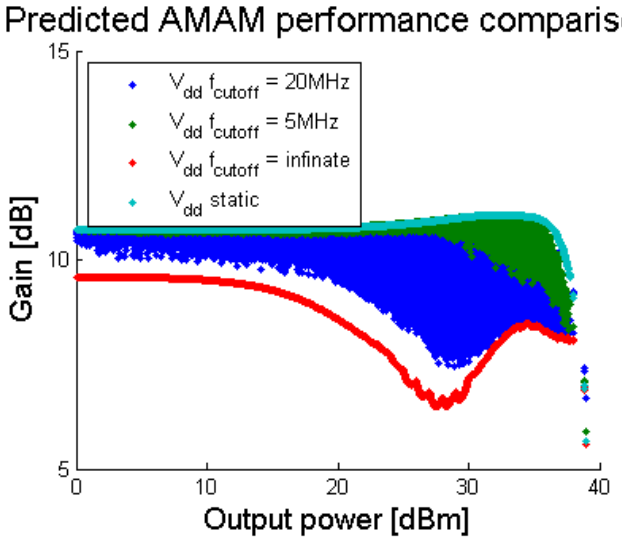


Figure 22. Predicted AM/AM behaviour when empoyeding DSM.

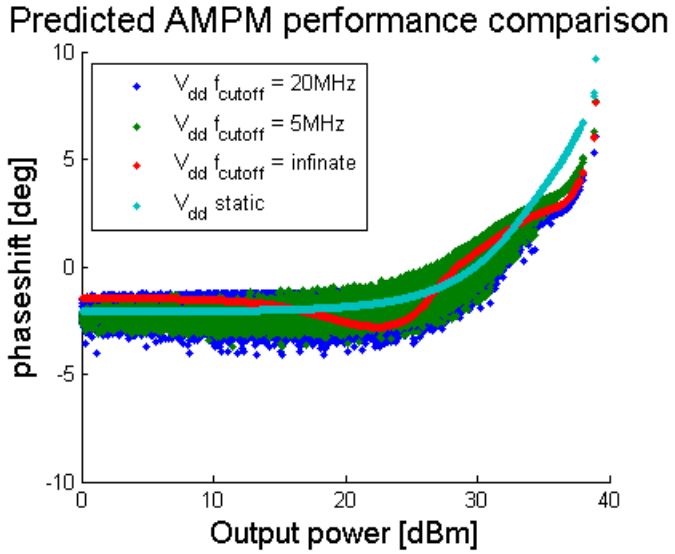


Figure 23. Predicted AM/PM behaviour when employing DSM.

One way of describing the DPD performance is to look at the RF frequency spectrum. In Figure 24 the RF frequency response with the DPD turned off is seen. This can be compared with Figure 25 where the DPD is deployed. Recalling that the DPD is an inverse 2DLUT of the PA characterization this result is to be expected verifying that the DPD in fact is an accurate inverse.

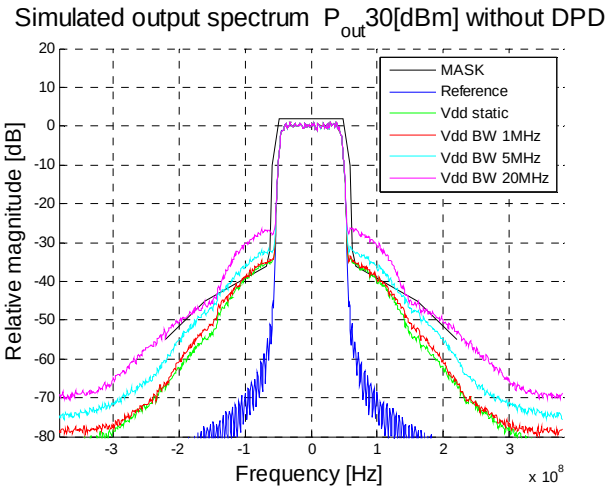


Figure 24. MATLAB simulation comparing desired output signal with simulated response for an output power of 30dBm.

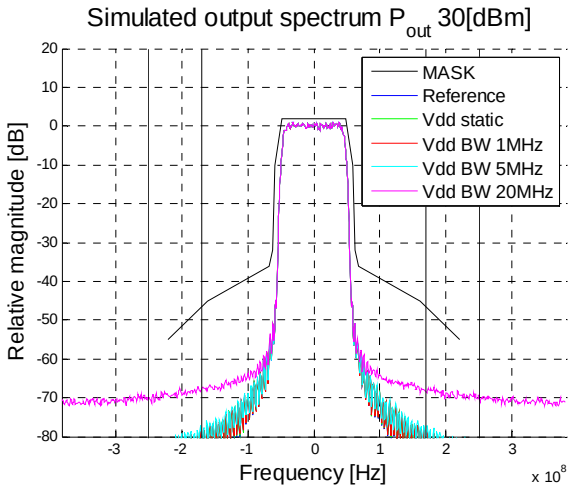


Figure 25. MATLAB simulation comparing desired output signal with simulated predistorted response for an output power of 30dBm.

Another way of evaluating DPD performance is through the MSE(Mean Squared Errror). In Table 2 the MSE for output powers of 28dBm and 30dBm at different level of supply modulation is found. In this table as in the spectrum pictures we can clearly see that the DPD is accurate for static drain voltages and then gradually degrading for increasing modulation bandwidth. For drain voltage modulation above the RF signal envelope bandwidth the EVM will improve.

Table 2. MSE for different output power and modulation bandwidth.

	Vdd static	**Vdd BW 1MHz**	**Vdd BW 5 MHz**	**Vdd BW 20 MHz**
P_{out} = 28dBm	-82.1 dB	-68.3 dB	-54.2 dB	-45.7 dB
P_{out} = 30dBm	-70.3 dB	-68.7 dB	-60.3 dB	-48.5 dB

5.2 Input spectrum

In Figure 26 and Figure 27 the input spectrum to the DAC (Digital to analog converter) is seen. As expected the spectrum is similar to that of the output spectrum without DPD in Figure 24.

The input spectrum does not have to conform with the spectrum mask as the output does. Instead the input spectrum is not allowed to spread further than the DAC converter bandwidth. For a DAC bandwidth of 500MHz the spectrum is required to be lower than -55dBc at 170MHz away from the center frequency. If the DAC instead has 800MHz of bandwidth this limit is shifted to lower than -55dBc at 250 MHz away from the center frequency. The 4 vertical black lines are positioned at 170MHz and 250 MHz away from the center frequency. From the figures we see that the spectrum width requirement for the 500 MHz DAC is not satisfied for any other than the static drain voltage. On the other hand they all fit nicely inside the 800 MHz DAC spectral requirements.

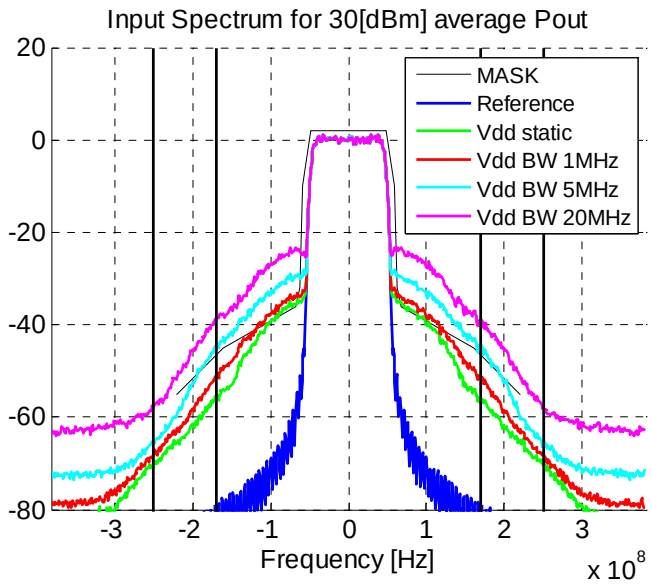


Figure 26. Spectral growth of input spectrum with DSM for 30dBm average Pout.

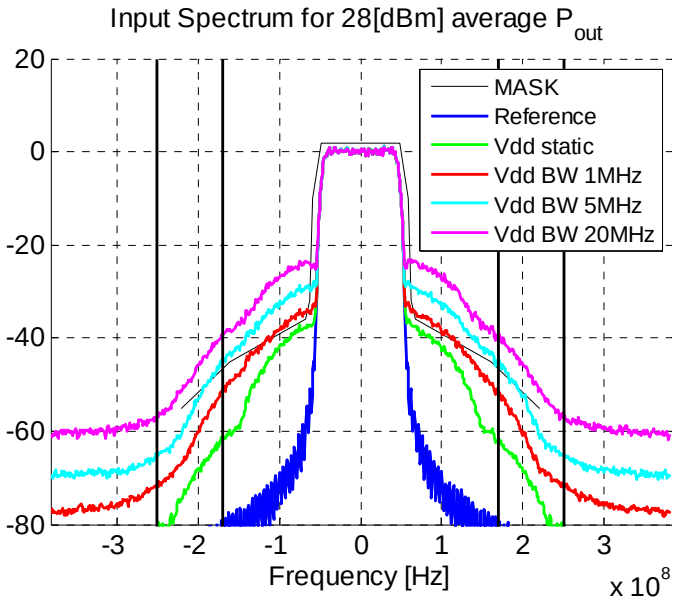


Figure 27. Spectral growth of input spectrum with DSM for 28dBm average Pout.

6 Verification of PAE potential calculations

The PAE improvement potential evaluation algorithm implemented in MATLAB has to be verified by simulating a PA controlled by the calculated signals. This was done using the MALAB co simulation package ADS Ptolemy. The PA was fed with a modulated drain voltage and a predistorted RF carrier signal voltage. Both of these signals were computed in MATLAB and via ADS Ptolemy fed to PA. During the simulation the RF output and DC power consumption was measured to compare linearity and DC power consumption.

6.1 Verification of PAE improvement calculations

By simulating the PA model in ads, with the MATLAB calculated signals the hope was to evaluate the validity of the MATLAB calculations. This was unfortunately unsuccessful since the simulations turned out as noise as can be seen in the figure below. What could be evaluated though was the PAE estimation which if compared with the MATLAB calculation in Figure 21 can be seen to match up to simulated values of Table 3.

Table 3. PAE improvement verification

	Figure 28	**Figure 30**	**Figure 29**	**Figure 31**
Vdd – BW	0 MHz	0 MHz	20 MHz	20 MHz
PAE	14.8 %	14.9 %	37 %	38 %
DPD-state	ON	OFF	ON	OFF
Average Pout	30 dBm	30.04 dBm	30.05 dBm	30.22 dBm

In the figures below the stochastic behavior for higher output powers can be seen where the PA reaches compression early. We can note that the gain at all times is kept above 9 dB when the DPD is turned of. This tells us that the DPD range is not a limiting factor.

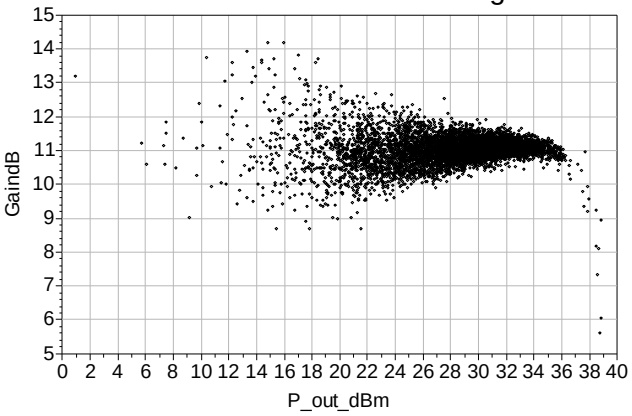


Figure 28. ADS verification, VDD static DPD ON.

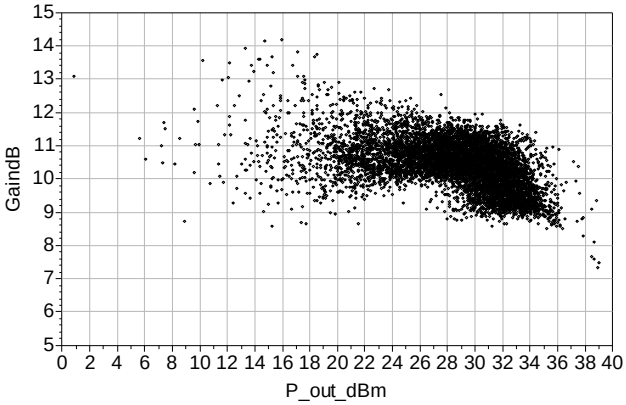


Figure 29. ADS verification, Vdd 20 MHz DP ON.

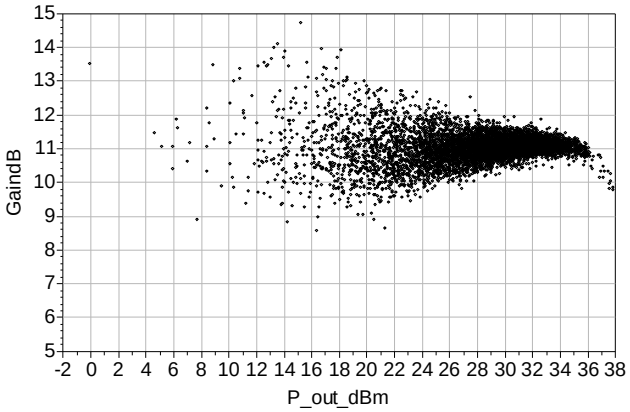


Figure 30. ADS verification, Vdd static NO DPD.

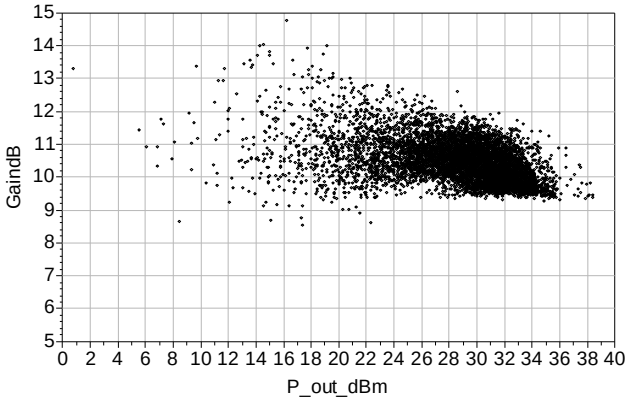


Figure 31. ADS verification, Vdd 20 MHz No DPD.

7 Complete PA chain PAE

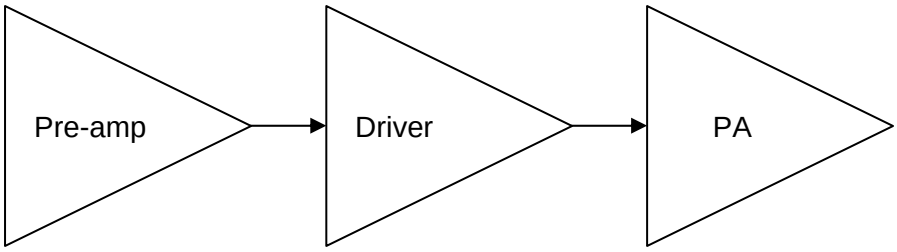


Figure 32. Transmitter amplifier stages.

The complete PA chain in this study consists of 3 consecutive stages in series. These are seen in Figure 32 and are the preamplifier, driver and PA. The ADS model that was characterized is of the last stage which is the PA. Since models for the proceeding stages where not available they were approximated by the PA model with downscaled bias voltages. The preceding stages have approximately the same gain but are backed off from the 1dB compression further point to improve linearity. Non linearity in early stages would otherwise be amplified in the later ones. The drawback of this is poor efficiency, but since their output power is much lower the system loss is less affected.

Table 4. Amplifier back off relative to the PA of the 3 steps in the amplifier chain.

	Pre amplifier	**Driver**	**PA**
Relative amplifier back off	10 dB	3 dB	0 dB

Modulating the drain voltage of the PA implies operating it closer to the point of compression for a large part of the $P_{in,RF}$ range. When the PA goes into compression gain is lost, this means more power has to be delivered by the linear and inefficient preceding stages.

By approximating the DC characteristics and transfer function as a scaled version of the final stage PA, the DC power consumed in of the preceding stages could be calculated. This was done using the relative back off of each amplifier as follows:

(η_{EA} denotes envelope amplifier efficiency)

$P_{in.\ relative}(dB)$ = $P_{in,PA}(dB)$ - relative amplifier back off(dB)

PAE = $PAE_{2DLUT,\ estimator}\{ P_{in.\ relative}(dB) \}$

$P_{out.\ relative}(dB)$ = $P_{out,\ 2DLUT,\ estimator}\{ P_{in.\ relative}(dB) \}$

$P_{DC,\ estimated.}(W)$ = $(P_{out.\ relative}(dB) - P_{in.\ relative}(dB)) / PAE / \eta_{EA}$

In Table 5 the complete PA chain PAE with different EA efficiencies and different number of PA stages modulated is seen. The modulation evaluated here is 10MHz dynamic drain modulation.

By introducing supply modulation on the last PA stage only the individual stage PAE increases by 13 percentage units but the total PAE is still only increased by 4.5%. But, if we introduce modulation also on the driver stage an additional 7.5% is increased in the total PA PAE.

Also recall here that modulating the supply of the Driver and Pre-driver will introduce additional non linearity and loss of gain.

Table 5. PAE for compete and individual gain stages in PA, with and without drain modulation. V_{dd} bandwidth 10 MHz.

			Number of stages with modulated supply			
			0/3	1/3	2/3	3/3
Individual PAE (not considering EA efficiency)	Pre-driver		1.3%	1.4%	1.7%	18.2%
	Driver		2.9%	3.2%	22.3%	22.3%
	PA		15.6%	28.5%	28.5%	28.5%
Total PAE	EA efficiency	80%	10.6%	13.3%	18.6%	20.3%
		90%	10.6%	14.2%	20.6%	22.8%
		100%	10.6%	15.1%	22.64%	25.32%

8 Envelope amplifier

A conceptual envelope amplifier design was chosen after studying literature and consulting the Power department at Ericsson. Apart from efficiency, good linearity over the desired bandwidth is important in order to provide the PA with the desired modulated supply voltage. The chosen design that provides both high efficiency and high bandwidth, is comprised of a low speed high efficiency switching stage and a high speed linear amplifier in parallel. See Figure 33.

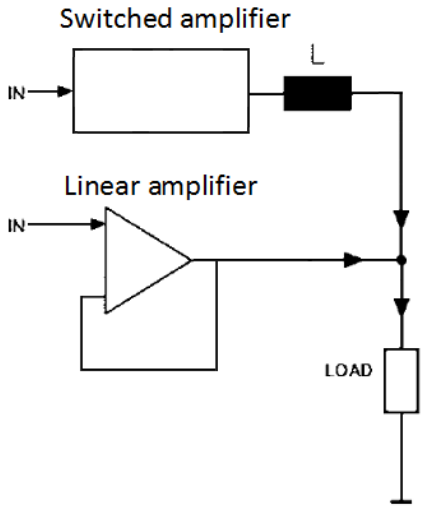


Figure 33. Conceptual description of the Envelope amplifier.

The switching stage is usually a very efficient buck converter switching stage that is followed by a large inductor. This inductor together with the load resistance serves as a LPF (Low Pass Filter) blocking high frequency distortion generated in the switch. From the collaboration with Ericsson power it was found that their implementations used 16 μH series inductors. For this simulation the PA was modeled as a 10 ohm resistor. This 10 Ohm resistor in series with the 16uH Inductor yields a cut off frequency ~100 KHz. This is too low to have any impact from a DSM point of view.

In the static bias case the drain voltage is provided with a similar kind of DCDC converter and since the efficiency of those is comparable the switch stage efficiency will not be investigated or accounted for in this study.

8.1 Implementation

The linearity and bandwidth performance is limited by the linear amplifier, while efficiency requires both stages to have low power dissipation. The EA design presented by Ericsson power was designed for base station applications, this means lower bandwidth and higher power compared to the MIN ILINK EA in this study.

The linear amplifier has to accurately track the desired drain voltage, operating like an ideal variable voltage source. The PA drain current is the purely set by the drain source impedance controlled by the RF input signal and bias. Since the linear stage output voltage must be able to swing both up and down a push pull configuration inside an Op-amp feedback loop was chosen as basic design. The push pull stage consists of a pair of complementary bipolar transistors, which has the best performance for high frequency, high current applications. See Figure 35 for a description of the feed back loop.

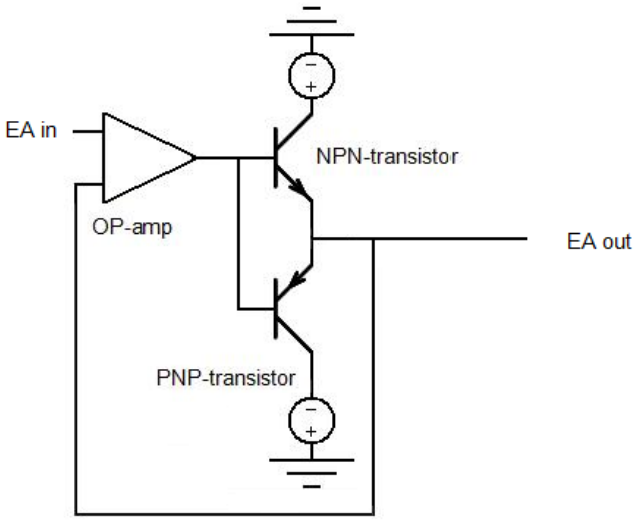


Figure 34. Basic push pull feedback loop.

The base emitter voltage drop in a BJT causes a “knee” in the transfer function of the amplifier in Figure 35. This has to be compensated for in order to get a linear behavior. By placing two diode coupled transistors between the bases of the two transistor this is taken care of, but only for high output currents. In order to provide a constant voltage drop that is independent of the op-amp output a current mirror stage is placed as can be seen in Figure 35. In this figure we also see two current buffers on the base of both BJTs. A current buffer is a unit voltage gain amplifier boosting the current. The reason for having such buffers is that better frequency performance in the BJTs can be achieved, if devices with lower gain are chosen.

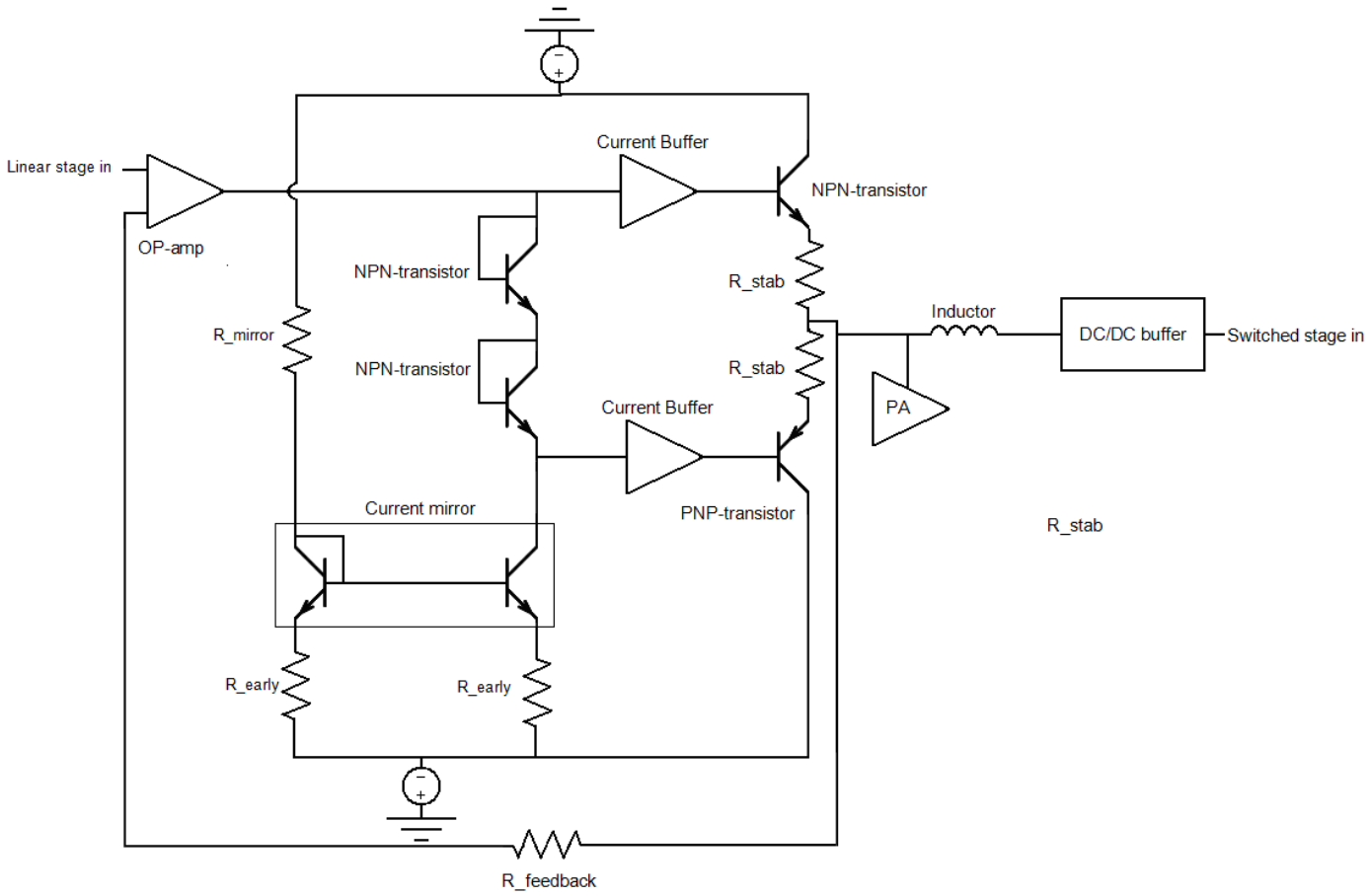


Figure 35. Envelope amplifier conceptual layout.

There are 4 sets of resistors in this circuit; these are the R_mirror, R_early, R_stab, R_feedback. R_mirror has the functionality of setting the current mirror current together with the normally much lower R_early which has the function of reducing V_{CE} dependence on the current in the current mirror. R_stab was found to solve an initial problem of oscillation between the PNP, NPN transistors. Finally we have the R_feedback which is the most sensitive design parameter of the linear amplifier as it sets the feedback speed and thereby cutoff frequency. Setting it too low though will result in an unstable circuit.

The PA model provided has a high complexity and was therefore initially modeled by a resistor. From the MATLAB simulations it was found that the DC input impedance at the PA drain port has an average of 10 ohm for a 10MHz modulated drain signal. A 10 ohm resistor was therefore selected as a simplified PA model. For final testing off course this resistor was replaced by the complete PA ads model.

8.2 Choosing components

The optimization of the linear amplifier is a trade off between, linearity, energy consumption, bandwidth, voltage swing and current swing. The major challenge lies in achieving a high bandwidth without causing instability, distortion and major power dissipation. Voltage swing is determined by the DC supply level, this sets the minimum DC supply level and apart from some design head room a higher level is rarely desirable, since it will increase the dissipated power. In turn the current swing is set by Ic_{max} in the BJT´s, it is therefore desired to choose a sufficiently large transistor. But for BJT´s there exists an approximate inverse relation between ft, f_{max} and Ic_{max}. This implies that a too large transistor size degrades the frequency performance. In addition to this the current gain of the BJT´s has to trade against output current from the OP-amp and current buffer.

8.2.1 Components

The Operational amplifier in the circuit is from Texas instruments and the model number is THS3001 which has a 3dB bandwidth of 420 MHz and a maximum output current of 175 mA. This meets the requirements of the EA with head room.

A bandwidth wise critical part of the circuit was the current buffers. The performance wise best buffer found was the HA-5002 from Intersil. This Buffer has a bandwidth of 110MHz and an output power of ±200mA.

The most sensitive part of the linear amplifier is the output stage NPN PNP transistors. This part has to be chosen together for maximum predictability. The two components chosen were model NJT4030p and NJT4031n from ON semiconductor. They featured a maximum collector current of 5 A and an f_T of 160 MHz and 215 MHz respectively.

The knee compensating diode coupled NPN transistors have the model number 2n3904 and is available from STMicroelectronics. The specification for the transistor is mainly to have a high f_T which for this model was 250 MHz.

In the current mirror two identical transistors are placed that need only have low power dissipation and stable operation. These transistors were chosen from STMicroelectronics and the model BC547C.

8.3 Simulations

Using ADS, a simulation model of Figure 35 was designed and optimized. In order to cut simulation time while designing a few simplifications were made. The switched BUCK stage was in the simulation replaced with a voltage source followed by an RF choke.

As mentioned before the PA was initially simulated with an ideal resistor. The value of this resistor was selected from the average value of the drain source impedance with a 10 MHz dynamic supply modulation.

8.4 EA simulation results

The EA design procedure consisted in several steps involving various ADS simulation engines. The final design though was evaluated using transient simulation in order to make sure the design was stable for all frequencies.

InTable 6 a display of the complete PAE of the final stage PA and EA combined is shown. This shows how the increased power dissipation in the EA for higher frequency still is outweighed by the increased PAE of the PA.

Table 6. EA power dissipation for increasing bandwidth.

Vdd bandwidth	1 MHz	5 MHz	10 MHz	20 MHz	30 MHz	40 MHz
DC power consumed by PA W	4,8	3,4	2,7	2,6	2,26	2,0567
DC power dissipated in Linear EA W	1,2	1,7	1,9	1,9	2,1	2,1
Pin W	0,1	0,1	0,1	0,1	0,1	0,1
Total dissipated power W	6,1	5,1	4,6	4,5	4,4	4,2
Pout W	1,0	1,0	1,0	1,0	1,0	1,0
PAE PA	19,0%	24,0%	31,0%	38,0%	40,0%	43,0%
PAE EA+PA	15,2%	18,0%	19,6%	19,9%	20,4%	21,2%
PAE reference without DSM	15,6%					

In addition to trading the linear EA efficiency performance against PA PAE the EA linearity is of great concern. In Figure 36 the MSE as a function of frequency swept between 1 and 101 MHz is seen. What can be seen here is that the performance starts to degrade severely after around 40 MHz.

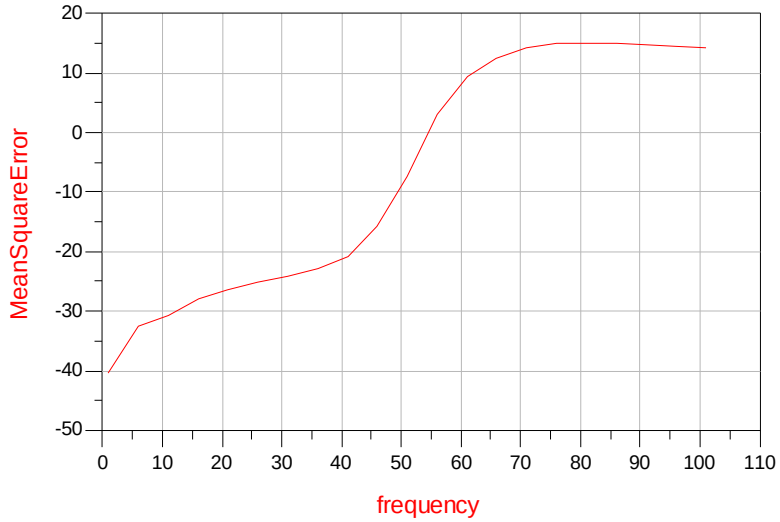


Figure 36. Linear Envelope amplifier MSE as a function of frequency.

The linear amplifier has a predictable and desired response for frequencies up to 40 MHz. An example of the time domain response can be seen in Figure 37. Comparing this figure with a simulation where the resistor is replaced with the real PA model yields the result seen in Figure 38. The high frequency noise stems from the RF envelope frequency controlling the drain current. The drain current variations that are outside the bandwidth of the EA will cause the drain voltage to deviate from the desired causing the RF signal to be distorted.

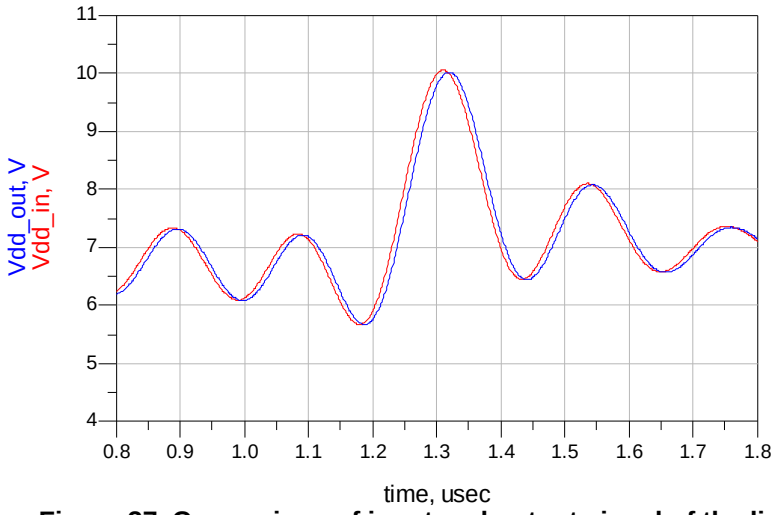


Figure 37. Comparison of input and output signal of the linear amplifier for a QAM-1024 modulated drain voltage signal bandwidth reduced to 5 GHz simulated with a resistive load.

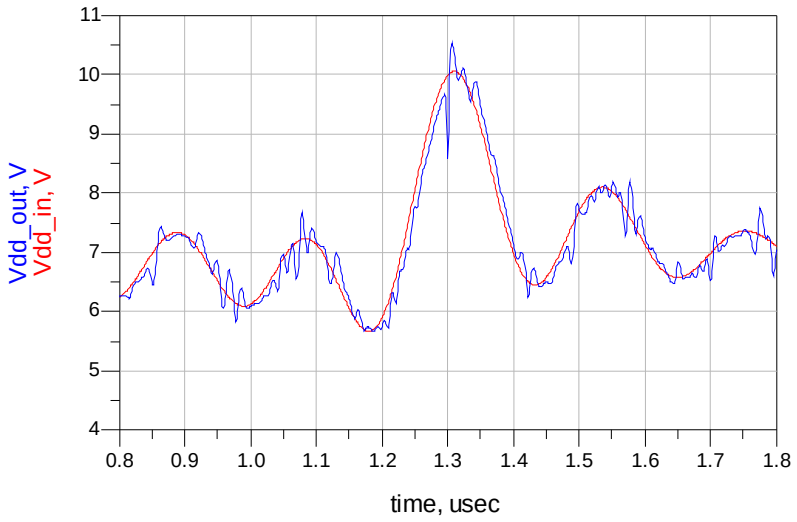


Figure 38. Comparison of input and output signal of the linear amplifier for a QAM-1024 modulated drain voltage signal bandwidth reduced to 5 GHz simulated with an ADS model PA as load.

An attempt at resolving this issue was made by placing a LPF between the EA and PA and thereby isolating them for high frequencies. The idea was to lower the drain signal bandwidth down to around 10 MHz and place the cut off frequency of the LPF below the bandwidth of the linear amplifier at around 20-30 MHz. By having this overlap between the EA bandwidth and the LPF it was assumed that good isolation could be achieved. Unfortunately these attempts were unsuccessful and this seems to be an area where continued investigations are needed.

9 Conclusions

The PAE improvement achieved in this project shows a potential improvement of the final stage PA from 15% to 20%. This number takes efficiency of the inefficient EA into account. Simulations of the entire amplifier chain indicate that the complete amplifier PAE can be improved from 10% to 20% with an EA efficiency of 80%.

The polynomial mapping signal envelope to drain voltage should not only be optimized for maximum PAE. By choosing the polynomial carefully large gains in linearity can be achieved.

From the PA characterization it was found that the potential PAE improvement with gate modulation is much lower than with drain modulation.

Driving the amplifier in compression over a wider range of signal amplitudes causes spectral growth. The heavily distorted signal poses difficulties not only for the DPD, but also for the DAC. Spectral growth in the non predistorted signal is when applying predistortion translated into spectral growth of the signal going into the DAC. Aliasing caused by input signal broadening was for this PA found to be a problem requiring a wideband DAC.

Bandwidth reduction introduces the possibility of supply modulator bandwidth lower than the RF signal envelope bandwidth. For such a system termination of RF envelope induced drain current variations is important and must be taken care of through a filter between EA and PA.

For radios with such high envelope bandwidths as in this project the main bottleneck is modulator bandwidth. The discrete components used in the envelope amplifier in this study limits the maximum operating frequency.

Dynamic supply modulation remains an interesting alternative for enhancing the efficiency of low power PA´s, though very high signal bandwidths are a hard obstacle to overcome.

10 Future work

Further investigation into envelope amplifier architectures that has increased bandwidth and improved efficiency is the key to feasible envelope tracking. For high frequency radio links operating a lower power levels the main advantage is the low bias voltage that should enable smaller devices with lower parasitics.

The tradeoff between linearity and PAE for the drain voltage polynomial should be evaluated further.

The problem of envelope induced current ripple in the drain supply bias for low bandwidth supply modulators has to be solved in order to implement the bandwidth reduction scheme.

Since linearity is very critical in amplifier design it is important that a simulation test bench is developed.

11 References

[1] J. Jeong, D. F. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. M. Asbeck, “Wideband envelope tracking power amplifiers with reduced bandwidth power supply waveforms and adaptive digital predistortion techniques,” IEEE Trans. Microwave Theory Tech., vol. 55, no. 12, pp. 2757–2765, Dec. 2007

[2] F. Wang, D. Kimball, J. Popp, et al., "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," in Proceedings of the Microwave Symposium Digest, pp. 645-648, La Jolla, Calif, USA, June 2005.

[3] E. Cipriani, P. Colantonio, F. Giannini, R.Giofre, L. Piazzon, ”Effects of Envelope Tracking Technique on an L-band Power Amplifier” IEEE Mediterranean Electrotechnical Conference, pp. 348 - 352 , April 2010