



S-Parameter Characterisation of Sub-Millimetre Membrane Circuits

Thesis for the degree of Master of Science in Wireless and Photonics Engineering

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Terahertz and Millimetre Wave Laboratory Department of Microtechnology and Nanoscience CHALMERS UNIVERSITY OF TECHNOLOGY Göteborg, Sweden, 2011 Thesis for the degree of Master of Science in Wireless and Photonics Engineering

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Abstract

In this thesis, a thru-reflect-line (TRL) calibration technique enabling full Sparameter characterisation for membrane circuits has been demonstrated in the WR-03 waveguide band (220 to 325 GHz). The designed membrane TRL kit is packaged in E-plane split blocks. An improvement of beam lead to ground connection was utilized by recessing the block surface. The proposed calibration provides the reference planes right at device under tests, thus reduces an extra de-embedding step. Membrane circuits such as stub filter, thin film resistors, thin film capacitor were characterised by applying the presented method. The simulated and measured results agree well, showing the validity of this approach. Furthermore, the measurement uncertainties such as temperature variation, time drift, system noise, power level fluctuations, connection repeatability and assembly tolerance were systematically investigated. For the connection repeatability study, the amplitude response of transmission coefficient varies within ± 0.1 dB while that of reflection coefficient is below -30 dB across the frequency band. In addition, the result of the membrane circuit is not sensitive to circuit mounting tolerance. These analysis prove that this technique is applicable in the WR-03 band. However, it is also very crucial to have a setup with good cables because of the significant impact of the cables on the characterisation result.

Keywords: Membrane circuit, TRL calibration, S-parameter, VNA measurement, Terahertz (THz) technology.

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Acronyms and Abbreviations

ADS	Advanced Design System
DUT	Device Under Test
GHz	Gigahertz
HFSS	High Frequency Structure Simulator
MMICs	Microwave Monolithic Integrated Circuits
OML	Oleson Microwave Lab
TFR	Thin Film Resistor
TFC	Thin Film Capacitor
TMICs	Terahertz Monolithic Integrated Circuits
VNA	Vector Network Analyzer

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Chapter 1 Introduction

TeraHertz (THz) radiation locates in the spectrum between microwaves and far infrared region. It is usually referred to a frequency range from 100 GHz to 10 THz although there is no specific definition [1]. THz technology has become a very hot research field in recent years, which was initially driven by astrophysics for space science mission applications. Nowadays, THz technology has shown potentials in a wide range of applications from remote sensor, THz imaging to medical diagnostic systems [2,3].

For the THz applications, as the working frequency increases, the circuit assembly will become more difficult to realize due to the decrease of chip dimensions. Moreover, the dielectric loss from the support substrate due to the moding effect is another factor which limits the operating frequency of the circuits. The membrane supported terahertz monolithic integrated circuits (TMIC) technique has been proposed as a solution to reduce these limitations [4, 5]. In this method, the thick semiconductor substrate is removed and the circuit is supported by a very thin (a few microns) insulating membrane. Additionally, the use of beam leads simplifies the assembly as they can also be designed for mechanical support and electrical connections. Figure 1.1 shows schematic pictures of a membrane supported mixer circuits and the cross section of membrane circuits mounted on half waveguide block. Up to date, numerous membrane MICs operating in the THz frequency region have been performed [4-8]. For example, high performance fundamental balanced mixer based on monolithic GaAs membrane diodes in the frequency bands of 520 -590 GHz [7] and 835 - 900 GHz [8] have been demonstrated. However, to the best of our knowledge, no research work about the Vector Network Analyzer (VNA) measurement enabling full S-parameter characterisation of membrane cicruits has been reported, which is very important for design verification and device modeling.



Figure 1.1: Schematic picture of a membrane supported mixer circuits and the cross section (cut at A - A') of membrane circuits mounted on half block.

On wafer probing measurement [9], see Figure 1.2 (a), is commonly used to characterise S-parameters of microwave components. However, at the submillimetre frequencies, new probe interfaces, for example membrane tip probes [10–12], and the new standards for waveguide flange interfaces [13] are required for the on-wafer probing technique. Besides, the difficulties of probing repeatability, contacting tolerances of probes, radiation and coupling between probes pose a challenge to the traditional on wafer probing and it is unsuitable for measuring the fragile membrane circuits. A waveguide-embedded VNA measurement enabling characterising MIC at millimetre wave frequencies has been proposed in the Niculea and Pisani's research [14]. In this method, a waveguide to planar transition is placed in a fixture that connect the device to the flange interface of VNA, and a thru-reflect-line (TRL) calibration removes all the systematic errors coming from the embedding structure.

In our previous work, a membrane TRL calibration kit is developed and demonstrated by S-parameter characterisation of membrane circuits in the WR-03 frequency band (220-325 GHz) [15, 16]. The 3 μ m thick membrane TRL standards are packaged in E-plane split blocks for TRL calibration. Figure 1.2 (b) shows a membrane circuit mounted on a half waveguide E-plane split block. The circuits will be clamped with another symmetric half block that the blocks connect to the VNA flange interface for measurements. This waveguide embedded structure does not need soldering, wire bonding and probing and thus becomes a suitable solution for the characterisation of the membrane circuits at submillimetre wave frequencies. The proposed membrane TRL calibration allows S-parameter characterisation of the membrane circuits without the need for extra de-embedding [17] because the reference planes are set directly inside the membrane circuits.

Based on our previous work [15, 16], further investigations have been made in this thesis including: (1) ground connection of the membrane circuits are improved by recessing the block surface; (2) new membrane device under tests (DUTs) are characterised such as membrane stub filter, membrane thin film capacitor (TFC) and membrane thin film resistors (TFRs) and the measurement results agree well with HFSS simulations; (3) some random errors coming from the test setup such as connector repeatability, time drift, temperature variation and mounting tolerance are studied.



Figure 1.2: Photos of (a) On wafer probing measurement and (b) Waveguide embedded structure enabling S-parameter characterisation of the membrane circuit. The circuits will be clamped with another symmetric half block that the blocks connect to the VNA flanges for measurements.

This thesis is organised as follows. Chapter 2 presents the theory of the TRL calibration technique. The design, fabrication and assembly of the membrane circuits are shown in chapter 3. Chapter 4 shows the measurement results and the investigations of measurement uncertainties such as connection repeatability, time drift and assembly tolerance. Finally, conclusions and possible work in the future are summarized in the last chapter.

The main results of this work is based on the published paper in the Appendix A.

Chapter 2

Theory of TRL calibration technique

In this chapter, two-port VNA calibration technique is introduced. The purpose of the calibration is to get rid of systematic errors in the VNA measurement. The theory of the most interested calibration technique, TRL calibration technique, is described.

2.1 N-port electrical network

An N-port microwave electrical network is illustrated in Figure 2.1 [18].



Figure 2.1: An N-port electrical network.

At the terminal planes, there are incident waves V_i^+, I_i^+ and reflected waves V_i^-, I_i^- . The total voltage and total current at the n^{th} reference plane are given as follows

$$V_n = V_n^+ + V_n^- (2.1)$$

$$I_n = I_n^+ - I_n^-$$
 (2.2)

The impedance matrix (Z matrix) at the reference planes is defined by the voltages related to the currents

$$[V] = [Z] \cdot [I] \tag{2.3}$$

with

$$Z_{ij} = \frac{V_i}{I_j}\Big|_{I_k=0, k\neq j} \tag{2.4}$$

The admittance matrix (Y matrix) is defined by

$$[I] = [Y] \cdot [V] \tag{2.5}$$

with

$$Y_{ij} = \frac{I_i}{V_j} \Big|_{V_k = 0, k \neq j} \tag{2.6}$$

The total voltages and currents cannot be measured directly at high frequencies. However, both the magnitude and the phase of the reflected waves and the incident waves are easily measured. The scattering matrix (S matrix) which describes the relationship between incident waves and reflected waves is defined as follows

$$\begin{bmatrix} V^{-} \end{bmatrix} = \begin{bmatrix} S \end{bmatrix} \cdot \begin{bmatrix} V^{+} \end{bmatrix}$$
(2.7)

with

$$S_{ij} = \frac{V_i^-}{V_{j^+}} \Big|_{V_k^+ = 0, k \neq j}$$
(2.8)

The S-parameter can be measured directly using a VNA. S-parameter can be used to characterise an electrical network, because it relates directly to some interesting figure of merits such as gain, transmission loss and return loss, and it can be converted easily to other network parameters, for example Z-parameter, Y-parameter, etc.

2.2 Vector network analyzer

VNA is an instrument which is used to measure both amplitude and phase properties of network parameters of an electrical network. S-parameter is commonly measured because both reflection coefficient and transmission coefficient of an electrical network can be easy to measure at high frequencies.

2.3 Error terms

There are some significant errors that will affect VNA measurements and must be addressed [19].

- Systematic errors: caused by imperfections in connectors and test fixture, etc. These are repeatable errors.

- Random errors: due to some unpredictable variables which change with time such as noise, connection repeatability [20], etc.

- Drift effects: due to the changes inside the system because of some environmental variables such as temperature, humidity, etc.

Random errors and drift effects can not be removed. However, they can be minimized in a stable environment. Calibration of a VNA can largely remove the effect of systematic errors. Many calibration techniques have been developed [21–24] which are listed below:

- Open, Short, Match (OSM)
- Thru, Open, Match (TOM)
- Thru, Reflect, Match (TRM)
- Thru, Reflect, Line (TRL)
- Line, Reflect, Line (LRL)
- Thru, Open, Short, Match (TOSM)
- Short, Open, Load, Thru (SOLT)

During the calibration, a series of known standards are measured. And the influences of systematic errors are determined by the difference between the measured responses and actual characteristics of the standards [25]. By this way, the errors can be extracted from the actual measurements of DUT. The accuracy of the measurement depends not only on the measurement setup such as cable, connectors, etc., but also on the calibration technique being used. For one-port VNA measurement, the OSM calibration is commonly used. The TOM, TRM, TRL, LRL, TOSM and SOLT calibrations are used for two-port VNA measurements in different cases. The TOM technique requires complete knowledge about the characteristics of all standards. TRL calibration is useful for planar structures in a test fixture because some characteristics of the TRL standards can be unknown and the system impedance can be implemented easily by the geometry. However, the length of the line standard will be very long at low frequencies. TRM uses the match standard instead of the line standard, but the perfect match standard is very difficult to fabricate. LRL is another variation of TRL where another line standard is used to replace the thru standard. However, an extra step is needed to set the reference planes to the desired position. TOSM and SOLT require the OSM (or OSL) measurements at each port and a thru measurement between two ports. They are developed to solve the problem in which the thru standard can be partly known. In this project, the TRL calibration for two-port VNA measurement is used because it is easily implemented for planar structures of membrane DUTs.

There are several error models developed such as 3 error term, 7 error term, 12 error term and 16 error term models [26]. The 3 error term model is used for one port calibration and the OSM technique. The two-port calibration can use the 7 error term model (TRL, TRM, LRL techniques) or the 12 error term model (TOSM, SOLT techniques). There is a 16 error term model as well. More details can be found in references [24, 25, 27, 28].

2.4 7 error term model

The 7 error term model is presented in this section. A general mathematical model for the effect of systematic errors using S-parameters (or ABCD parameters) is constructed as shown in Figure 2.2 [19].



Figure 2.2: General model for the effect of taking in account systematic errors.

 S_m is defined as the actually S-parameters measured by the VNA. These include all of the errors. The S-parameters of error boxes A and B are defined as S_A and S_B . The S-parameters of the DUT is called S_{DUT} which are desired to know. The measurement planes are at the interface between the VNA and the exterior setup. The reference planes are dependent on the calibration technique and are usually set right up to the DUT. The purpose of VNA calibration is to determine the numerical values of all S parameters in the error boxes at each interested frequency [19]. Then the real responses of the DUT can be obtained by extracting the error boxes from the actual measurements.

Based on the general model, a 8 error term model is established as in Figure 2.3 [26].



Figure 2.3: Mathematical model with 8 error terms.

where a_1, b_1, a_2, b_2 are the raw measurements at the measurement planes of the VNA. a'_1, b'_1, a'_2, b'_2 are the incident wave and reflect wave at port 1 and port 2, respectively, at the reference planes. $e_{00}, e_{01}, e_{10}, e_{11}$ are the S-parameters of the error box A, $e_{22}, e_{23}, e_{32}, e_{33}$ are the S-parameters of the error box B

2.4. 7 ERROR TERM MODEL

and $S_{11}, S_{12}, S_{21}, S_{22}$ are the S-parameters of the DUT that we need to know. These S-parameters will be converted to the cascade T-parameters because the measured results are easily calculated using T-matrix.

S-parameter and T-parameter are defined in (2.9) and (2.10)

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = S \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$
 (2.9)

$$\begin{pmatrix} b_1\\a_1 \end{pmatrix} = T \cdot \begin{pmatrix} a_2\\b_2 \end{pmatrix}$$
 (2.10)

S-parameters of the error boxes A and B are converted to T-parameters.

$$T_1 = \frac{1}{e_{10}} \cdot \begin{bmatrix} -\Delta_1 & e_{00} \\ -e_{11} & 1 \end{bmatrix}$$
(2.11)

where

$$\Delta_1 = e_{00}e_{11} - e_{10}e_{01} \tag{2.12}$$

$$T_2 = \frac{1}{e_{32}} \cdot \begin{bmatrix} -\Delta_2 & e_{22} \\ -e_{33} & 1 \end{bmatrix}$$
(2.13)

where

$$\Delta_2 = e_{22}e_{33} - e_{32}e_{23} \tag{2.14}$$

Similarly for DUT

$$T_{DUT} = \frac{1}{S_{21}} \cdot \begin{bmatrix} -\Delta_{DUT} & S_{11} \\ -S_{22} & 1 \end{bmatrix}$$
(2.15)

where

$$\Delta_{DUT} = S_{22}S_{11} - S_{12}S_{21} \tag{2.16}$$

The measured T parameters can be expressed as

$$T_m = T_1 \cdot T_{DUT} \cdot T_2 \tag{2.17}$$

where

$$T_m = \frac{1}{S_{21m}} \cdot \begin{bmatrix} -\Delta_m & S_{11m} \\ -S_{22m} & 1 \end{bmatrix}$$
(2.18)

and

$$\Delta_m = S_{22m} S_{11m} - S_{12m} S_{21m} \tag{2.19}$$

Combining (2.11), (2.13), (2.15) and (2.17), we have

$$T_m = \frac{1}{e_{10} \cdot e_{32}} \begin{bmatrix} -\Delta_1 & e_{00} \\ -e_{11} & 1 \end{bmatrix} \cdot T_{DUT} \cdot \begin{bmatrix} -\Delta_2 & e_{22} \\ -e_{33} & 1 \end{bmatrix}$$
(2.20)

According to equation (2.20), to know the S_{DUT} , seven identified error terms need to be determined. There are 3 terms at port 1 (Δ_1, e_{00}, e_{11}), 3 terms at port 2 (Δ_2, e_{22}, e_{33}) and $e_{10} \cdot e_{32}$ can be regarded as one term. So the 8 error terms are reduced to 7 error terms.

A calibration technique will require enough calibration standards to build at least 7 independent equations so that 7 error terms above can be resolved.

2.5 TRL calibration technique

The most commonly used calibration technique for two-port VNA measurement of non-coaxial devices using 7 error term model is the TRL calibration technique. During the calibration, a series of thru, line and reflect standards are measured.

2.5.1 Thru standard

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The thru standard is normally a transmission line. It is usually used to set the reference plane of the measurement. A zero length thru is the best solution. However, a non-zero length thru is also acceptable. In this case, the electrical length must be defined when it is used to set the reference plane. If the time delay of the non-zero length is set to be zero, the reference plane is set in the middle of the thru standard. A mathematical model of a zero-length thru standard is shown in Figure 2.4 [19].



Figure 2.4: Mathematical model of the zero-length thru standard.

The S-parameters of the zero length thru can be written as

$$S_t = \begin{bmatrix} 0 & 1\\ 1 & 0 \end{bmatrix} \tag{2.21}$$

The equations from (2.22) to (2.25) are obtained from the thru's model. The measured S-matrix defined as S_{mt} in Figure 2.4 can be derived by

$$S_{mt11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = S_{11A} + \frac{S_{12A}S_{21A}S_{11B}}{1 - S_{22A}S_{11B}}$$
(2.22)

$$S_{mt22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = S_{22B} + \frac{S_{12B}S_{21B}S_{22A}}{1 - S_{22A}S_{22B}}$$
(2.23)

$$S_{mt12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} = \frac{S_{12B}S_{12A}}{1 - S_{22A}S_{11B}} \tag{2.24}$$

$$S_{mt21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} = \frac{S_{21B}S_{21A}}{1 - S_{22A}S_{11B}} \tag{2.25}$$

2.5.2 Reflect standard

The reflect standard is considered as a load that produces a large reflection as shown in Figure 2.5 [19]. The optimal value of the magnitude of the reflection coefficient Γ_L is 1, but it is unnecessarily known. The values of Γ_L at two ports are ideally the same. An open or a short is usually chosen as reflect standard. It can be also used to set the reference plane. In that case, the phase response of the reflect standard must be specified.



Figure 2.5: Mathematical model of the reflect standard.

The S-parameters of the reflect standard are

$$S_r = \begin{bmatrix} \Gamma_L & 0\\ 0 & \Gamma_L \end{bmatrix}$$
(2.26)

Two equations (2.27)-(2.28) are built as follows

$$S_{mr11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = S_{11A} + \frac{S_{12A}S_{21A}\Gamma_L}{1 - S_{22A}\Gamma_L}$$
(2.27)

$$S_{mr22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = S_{22B} + \frac{S_{12B}S_{21B}\Gamma_L}{1 - S_{11B}\Gamma_L}$$
(2.28)

in which S_{mr} is defined as the measured S matrix in Figure 2.5.

Since two ports are isolated, then

,

$$S_{mr12} = S_{mr21} = 0 \tag{2.29}$$

2.5.3 Line standard

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The line standard is a transmission line whose length doesn't need specified and the line may be lossy, see Figure 2.6 where l is the length of the transmission line and γ is called propagation constant [19]. The optimal length of line is $\lambda/4$ longer than that of the thru standard at the center frequency. The characteristic impedance of the line standard is set as the reference impedance of the measurement. And the characteristic impedance of the line standard must be the same as the thru standard. The phase difference between the thru and the line standards should range from 20 degree to 160 degree to minimize some measurement uncertainties.



Figure 2.6: Mathematical model of the line standard.

The S-parameters of the line standard are given as follows

$$S_l = \begin{bmatrix} 0 & e^{-\gamma l} \\ e^{-\gamma l} & 0 \end{bmatrix}$$
(2.30)

Four equations (2.31)-(2.34) are given as below

$$S_{ml11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = S_{11A} + \frac{S_{12A}S_{21A}S_{11B}e^{-2\gamma.l}}{1 - S_{22A}S_{11B}e^{-2\gamma.l}}$$
(2.31)

$$S_{ml22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = S_{22B} + \frac{S_{12A}S_{21A}S_{22A}e^{-2\gamma.l}}{1 - S_{22A}S_{11B}e^{-2\gamma.l}}$$
(2.32)

$$S_{ml12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} = \frac{S_{12A}S_{12B}e^{-\gamma.l}}{1 - S_{22A}S_{11B}e^{-2\gamma.l}}$$
(2.33)

$$S_{ml21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} = \frac{S_{21A}S_{21B}e^{-\gamma.l}}{1 - S_{22A}S_{11B}e^{-2\gamma.l}}$$
(2.34)

where S_{ml} is defined as the measured S matrix in Figure 2.6.

Now, by measuring three standards, ten equations from (2.22) to (2.25), (2.27)-(2.28), (2.31)-(2.34) are built to solve ten unknown variables. They are eight S-parameter terms in the error boxes A and B, $e^{-\gamma l}$ and Γ_L . That is why the values of $e^{-\gamma l}$ and Γ_L don't need to be specified in TRL calibration. At this point, the S-parameters of DUT are de-embedded from the measured S-parameters.

It is worth to mention, the TRL solution will give two roots for both $e^{-\gamma l}$ and Γ_L . Since only one root is chosen, the problem now is which one will be chosen. For $e^{-\gamma l}$, it is the transmission coefficient of the line standard, so its magnitude have to be less than or equal to 1 and its phase should be continuous. Based on that, one of two roots can be selected. Concerning Γ_L , the solution gives two roots equal in the amplitude but out of phase. The root selection for the Γ_L is given in reference [29].

Another solution for the TRL calibration based on the analysis of the T parameters is given in the reference [30]. Alternative ways to choose the root are presented in detail in references [31]- [32].

2.6 Switch correction

In section 2.5, the error correction model assumes a perfect balanced test setup system between two ports. However, it is not the case in practice where two error boxes in section 2.4 are not equal [25]. Therefore, an additional correction called switch correction is needed by getting the raw data at two ports for each standard.



Figure 2.7: General model with switching correction.



Figure 2.8: Mathematical model after doing the switch correction.

At port 1, the forward excitation is given by

$$\begin{pmatrix} b_f^1 \\ b_f^2 \end{pmatrix} = \begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} \cdot \begin{pmatrix} a_f^1 \\ a_f^2 \end{pmatrix}$$
(2.35)

Similarly, the reverse excitation at port 2 is shown as follows

$$\begin{pmatrix} b_r^1 \\ b_r^2 \end{pmatrix} = \begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} \cdot \begin{pmatrix} a_r^1 \\ a_r^2 \end{pmatrix}$$
(2.36)

Equations (2.35)-(2.36) can be combined as follows

$$\begin{pmatrix} b_f^1 & b_r^1 \\ b_f^2 & b_r^2 \end{pmatrix} = \begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} \cdot \begin{pmatrix} a_f^1 & a_r^1 \\ a_f^2 & a_r^2 \end{pmatrix}$$
(2.37)

After that, the waves are normalized to a channel on the excitation side as below

$$\begin{pmatrix} \frac{b_f^1}{a_1^r} & \frac{b_r^1}{a_r^2} \\ \frac{b_f^2}{a_1^r} & \frac{b_f^2}{a_r^2} \\ \frac{b_f^2}{a_1^r} & \frac{b_f^2}{a_r^2} \end{pmatrix} = \begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} \cdot \begin{pmatrix} 1 & \frac{a_r^2}{a_r^2} \\ \frac{a_f^2}{a_1^1} & 1 \end{pmatrix}$$
(2.38)

Equation (2.38) is simplified by the label given by

$$\begin{pmatrix} s'_{11} & s'_{12} \\ s'_{21} & s'_{22} \end{pmatrix} = \begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} \cdot \begin{pmatrix} 1 & a_{12} \\ a_{21} & 1 \end{pmatrix}$$
(2.39)

Finally, the raw uncorrected S-parameters are obtained as follows

$$\begin{pmatrix} S_{11raw} & S_{12raw} \\ S_{21raw} & S_{22raw} \end{pmatrix} = \begin{pmatrix} s'_{11} & s'_{12} \\ s'_{21} & s'_{22} \end{pmatrix}^{-1} \cdot \begin{pmatrix} 1 & a_{12} \\ a_{21} & 1 \end{pmatrix}$$
(2.40)

After doing the switch correction, these uncorrected data are valid to use the 7 term error model above to calculate the corrected S-parameters as shown in Figure 2.8.

The general model with switch correction in Figure 2.7 is used in the stability investigation.

Chapter 3

Design, fabrication and assembly

In this chapter, the design, fabrication and assembly of the membrane circuits are described.

3.1 Membrane TRL kit design

The membrane TRL standards and all DUTs are designed by using Ansoft's High Frequency Structure Simulator (HFSS) and Agilent's Advanced Design System (ADS) softwares [33].

3.1.1 Waveguide to membrane transition

A single waveguide to microstrip transition structure is designed and simulated in HFSS over the WR-03 waveguide band of 220-325 GHz, see Figure 3.1.

The WR-03 rectangular waveguide has a width of 432 μ m and a height of 864 μ m. The cut-off frequency of the dominant mode TE_{10} appears at 173 GHz. The waveguide probe will provide the coupling from the waveguide dominant mode TE_{10} to the planar circuit. The shape and the dimensions of both the waveguide probe and the waveguide backshort are optimised together to get almost 100 percent coupling efficiency over the WR-03 frequency band. The planar circuit structure is coplanar waveguide type. E-plane split blocks are used which gives the lowest loss since the currents of the waveguide mode are not broken [34]. The simulated value of the reflection coefficient S_{11} and the transmission coefficient S_{12} of the waveguide to membrane transition are shown in Figure 3.2. The simulated S_{11} is better than 15 dB over the frequency range.



Figure 3.1: HFSS simulation of waveguide to microstrip transition.



Figure 3.2: S-parameters of the waveguide to microstrip transition simulation, without considering the losses.



The E-field distribution of the dominant mode TE_{10} is presented in Figure 3.3.

Figure 3.3: E-field distribution of the waveguide TE_{10} mode.

The air channel is designed to have a width of 300 μ m and a height of 250 μ m so that the second mode and the third mode will appear around 410 GHz and 495 GHz, respectively, see Figure 3.4, β is the phase constant.

3.1.2 Membrane TRL standards

The length of the membrane thru standard and the membrane line standard are 600 μ m and 850 μ m, respectively, see Figure 3.5. The membrane thru is designed to be as short as possible so that there are still space for other circuits in the integrated structure, but not too short to avoid the influences of avanescent modes. The membrane line standard is designed to be 250 μ m longer than the membrane thru standard so that the phase difference between them is 90 degrees at 300 GHz.

The width of the transmission line is 64 μ m, corresponding to a characteristic impedance of approximately 100 Ω [15] as shown in Figure 3.6.

An open standard was chosen as the reflect standard because of its good response characteristic compared to a short standard. Moreover, the open standard is usually less sensitive and more reliable because it depends slightly on the ground connection and mounting tolerance [16]. All TRL standards have the same waveguide to planar interface at each end [15]. The length of all standards and DUTs are the same except the membrane thru standard so that the number of different mechanical block types is minimized.



Figure 3.4: Phase constant β as a function of frequency showing cut-off frequencies of higher order modes.



Figure 3.5: Schematic picture of membrane TRL standards.



Figure 3.6: Characteristic impedance as a function of frequency for a 64 μm width signal line.

3.2 Fabrication

A flow chart for the fabrication of the membrane circuit is shown in Figure 3.7 [35].

Figure 3.7 (a) describes the epitaxy structure of the membrane fabrication. In the beginning of the process, the top two n doped GaAs layers are etched away. After that, the individual chips are defined by etching through the GaAs membrane layer down to the bottom AlGaAs layer (Figure 3.7 (b) and (c)). Next, the passive circuits and the beam lead are patterned and plated (Figure 3.7 (d)). The beam leads are fabricated on the top AlGaAs layer extending out onto the bottom AlGaAs layer. The thickness of plated Au is 2 μ m, with a root mean square (RMS) surface roughness of 21 nm by atomic force microscopy (AFM). After finishing these top side process, the circuit is mounted upside down, to a Silicon wafer using wax (Figure 3.7 (e)). Then, it is lapped mechanically down to 50 μ m (Figure 3.7 (f)). Chemical selective etchants are used to remove the GaAs layer and the bottom AlGaAs layer (Figure 3.7 (g)). Finally, the individual chips are collected after dissolving the wax with acetone. The microscope pictures of the fabricated membrane TRL kit are shown in Figure 3.8.



Figure 3.7: The flow chart of membrane circuit fabrication.



Figure 3.8: Microscope picture of the fabricated membrane TRL kit.

3.3 The assembly

In this section, the way to mount a membrane circuit in a waveguide of the E-plane split block is described as follows.

1. Put a little bit of water in the air channel of a half waveguide block.

2. A chosen membrane circuit is flipped down and placed in the air channel. Water will help the circuit stick to the channel.

3. The chip position is adjusted under microscope so that it is aligned in the air channel.

4. The half waveguide block with circuit mounted inside is placed on the heater to evaporate the water.

5. In the final step, two symmetric waveguide blocks are clamped and fastened and the circuit now is ready to measure.

The schematic pictures of top view and cross section of the membrane circuits in the E plane split blocks with all detailed dimensions and and a photo of a real 3 μ m membrane circuit mounted in a half split block are shown in Figure 3.9 and Figure 3.10, respectively.



Figure 3.9: Schematic pictures of top view and cross section of membrane circuit in block.

In Figure 3.9, it is clearly seen that the beam leads are clamped in the blocks and they are used as ground connection. In previous work, the channel is designed to be 40 μ m wider than the membrane circuit [15]. In this work, the alignment tolerance is decreased to 20 μ m to improve the alignment. The membrane circuit is designed to have self-aligned structure with almost the same length of the beam lead and the air channel, see Figure 3.10, permitting a small mounting tolerance. Moreover, new E plane split blocks with recessed surface were manufactured to improve the beam lead to the ground connection as shown in Figure 3.11.



Figure 3.10: Photo of a membrane circuit mounted in a half of waveguide block.



Figure 3.11: Photo of a E-plane split block with recessed surface.

Chapter 4

Measurement results

In this chapter, waveguide calibration using Oleson Microwave Labs (OML) TRL standards are first performed to verify the membrane TRL design. Next, the proposed membrane TRL calibration technique is applied to characterise the S-parameters of some membrane passive circuits such as membrane stub filter, membrane thin film capacitor (TFC), membrane thin film resistors (TFRs). Moreover, some measurement uncertainties such as connection repeatability, drift related to time, temperature variation and alignment tolerance are investigated as well.

4.1 Measurement setup

S-parameter characterisation of membrane circuits are done with VNA measurements at high frequency. Two OML V03VNA2-T/R frequency extension modules are connected to an Agilent E8361 VNA to extend the 50 GHz test set to the WR-03 frequency band (220-325 GHz). The E-plane type split blocks with the membrane circuits in between are connected directly to the flanges of the two frequency extension modules. A schematic picture and a photo of the WR-03 measurement setup are shown in Figure 4.1.

For the VNA set up, the power of all ports is set at -10 dBm. Both the power slope (dB/freq) and the attenuation (dB) are set at zero. An IF bandwidth of 1 kHz is used and the sweep type is linear. TRL calibration program inside the VNA is used for the calibration.



Figure 4.1: Schematic picture (a) and a photo (b) of the WR-03 measurement setup.

4.2 TRL kit design verification

First of all, the OML waveguide TRL standards are used to do the calibration which is called waveguide calibration. The OML thru standard is a non-zero length thru. Therefore, the OML thru is specified to have zero time delay so that the reference plane is set in the center of the OML thru standard in the waveguide calibration. A photo of the OML waveguide standards are given in Figure 4.2.



Figure 4.2: A photo of OML waveguide standards.

For assemble the membrane thru, a 26 mm long reference waveguide is designed to evaluate the losses of the waveguide, see Figure 4.5 . In this work, the recessed E-plane split blocks which are designed to improve the beam lead to ground connection are used.



Figure 4.3: Photo of one waveguide thru half block. The half together with another symmetric half are used to assemble the membrane thru



Figure 4.4: S_{12} and S_{11} of the reference waveguide thru in old block and recessed block.

In the Figure 4.4, a comparison of loss in reference waveguide between old block and recessed block is shown. $|S_{12}|$ of the reference waveguide thru in the two cases are approximately -0.7 dB and -0.3 dB, respectively. An improvement of 0.4 dB in the reference waveguide of recessed block is observed compared to that in the old block, probably thanks to better ground connections. The magnitudes of S_{11} in the reference waveguides of both blocks are well below -15 dB.

Then, the membrane thru, line and the open standards are mounted in the recessed E-plane split block to verify their design. The magnitude of S_{12} of the membrane thru and the membrane line are approximately -0.6 dB and -0.9dB, respectively, see Figure 4.5. Compare S_{12} of the reference waveguide and the membrane thru, the loss in a 2 mm long membrane circuit is approximately 0.3 dB. Higher loss at high frequencies (around 300 GHz) is observed for all membrane thru, membrane line and reference waveguide, may be due to the resonance frequency. The S-parameters of the membrane line agree well with the HFSS simulation results. This simulation includes the loss of surface resistance of Au already.



Figure 4.5: S_{12} and S_{11} of the reference waveguide, the membrane thru, the membrane line and HFSS simulation of the membrane line measured at reference plane of waveguide calibration.

For the membrane open, S_{11} is around -0.6 dB and S_{21} is below -40 dB showing a good isolation between two ports as seen in Figure 4.6. The membrane TRL kit with low losses in the membrane thru and the membrane line standards and high reflection in the membrane open standard verifies that these standards can be use as TRL calibration standards. The best circuits with lowest loss and highest reflection in each batch are selected for the membrane TRL calibration.



Figure 4.6: S-parameters of the membrane open measured at the reference plane of waveguide calibration.

4.3 Applications

After showing that the quality of the membrane TRL standards are good in the section 4.2, the membrane TRL calibration is performed. After the TRL calibration, the reference planes are set in the center of the membrane thru standard, see Figure 3.5. Then, S-parameter measurements of some membrane passive circuits are characterised such as membrane shorted stub filter, membrane TFR and membrane TFC. Reference [36] (or Appendix A) is referred for more information about the design and the fabrication of the membrane shorted stub filter, the membrane TFR and the membrane TFC.

The membrane stub filter is designed to check the clamping of the ground connection which has the electrode connected to ground via the beam lead, see Figure 4.7 (a). Figure 4.7 (b) shows the characterisation of the stub filter calibrated by using the old blocks [16] and the recessed blocks. The result of using recessed blocks fit better to the HFSS simulation with surface roughness loss. Compared to the simulation, small frequency shifts of 3 GHz are observed in the measurements, probably due to simulation, manufacturing and assembly errors.

Moreover, a comparison of using the proposed membrane TRL calibration and the waveguide TRL calibration is also performed in Figure 4.8. Compared to the waveguide TRL calibration (the dash grey curve), the membrane TRL calibration (the black curve) gives a better agreement to the HFSS simulation (the green curve) because the reference planes are set directly at passive circuit.



Figure 4.7: (a) A microscope picture of membrane stub filter (b) S-parameters characterisation of the membrane stub filter using recessed blocks (wine curve), old membrane blocks (blue curve) and HFSS simulation (black curve).



Figure 4.8: S-parameters characterization of the membrane stub filter using the membrane calibration and the waveguide calibration.

Another membrane passive circuit is the membrane TFC which is designed for DC bias application in future TMICs applications. It has the capacitors whose top electrode is connected to the beam lead via an air bridge [36], see Figure 4.9 (a). It has a similar structure with the membrane stub filter. The size for each side of the membrane TFC is 20 μ m x 60 μ m with the thickness of 320 nm SiN dielectric layer, corresponding to a value of 0.2 pF in DC measurement. Its S-parameter characterisation is shown in Figure 4.9 (b) which agrees quite well with the simulation result. Compared to the membrane stub filter, the TFC has similar response showing that it can be used for the separation of DC and RF signals. The frequency shift of 3 GHz is obtained compared to the simulation result, probably due to simulation, manufacturing and assembly errors.



Figure 4.9: (a) A microscope picture of membrane TFC (b) S-parameter characterisation of the membrane TFCs using the membrane calibration.

The S-parameter measurement of two types of the membrane TFR are also performed [36]. One membrane TFR has the resistor connected in series between two transmission lines and the other has resistors connected in parallel via the beam lead, see Figure 4.10 (a) and Figure 4.11 (a). The sizes of the series TFR and each side of the shunt TFR are 64 μ m x 125 μ m and 20 μ m x 75 μ m, respectively, with a 60 nm thick NiCr thin film. The DC characterisation gives a resistance of 90 Ω for the series configuration TFR and 180 Ω in each side of the shunt configuration TFR. The results of S-parameter characterisation of two types of the membrane TFRs are shown in Figure 4.10 (b) and Figure 4.11 (b). They agree with the HFSS simulation results. The ripple in the results of both types of TFRs is probably due to the imperfection in the waveguide to membrane transition.



Figure 4.10: (a) Microscope picture of a series membrane TFR (b) S-parameter characterisation of the series membrane TFR using the membrane calibration.



Figure 4.11: (a) Microscope picture of a shunt membrane TFR (b) S-parameter characterisation of the shunt membrane TFR using the membrane calibration.

4.4 Connection repeatability

To evaluate the accuracy of the membrane TRL calibration, the connection repeatability is investigated in this section. In the TRL calibration procedure, the membrane thru is the last standard, so the S-parameters of the membrane thru in calibration without the reconnection are recorded. The magnitude of S_{11} and S_{22} of membrane thru in calibration are below -40 dB while the transmission between two ports S_{12} and S_{21} are approximately 0 dB as shown in Figure 4.12 (a) with black curves. The phase of S_{12} and S_{21} are approximately 0.5 degree, see Figure 4.12 (b) (the pink and blue curves).



Figure 4.12: The magnitude of S_{12} and S_{11} (a) and phase response of S_{12} and S_{21} (b) for the membrane thru in calibration and after reconnection.

The connection repeatability of the membrane thru after reconnection is checked, as shown in Figure 4.12. There is a very small variation in the amplitude between the membrane thru in calibration and after the reconnection. The phase of S_{12} and S_{21} of the membrane thru ranges between 0 and 1 degree after the reconnection (the red and black curves).

By re-measuring the membrane thru without reconnection over 3 hours, the effect of time drift is also observed. The magnitude now is decreased a little bit, around -0.05 dB, and the phase is shifted 4 degree compared to the membrane thru reconnection case, see Figure 4.13 (a) and Figure 4.13 (b), respectively.



Figure 4.13: The magnitude of S_{12} and S_{11} (a) and phase response of S_{12} and S_{21} (b) for the membrane thru after reconnection and after 3 hours.

The connection repeatability of the membrane line is performed as well. There are very small changes in amplitude of S_{12} and S_{11} of the membrane line standard with different connections. The magnitude of S_{12} is -0.1 dB and the amplitude of S_{11} is always under -30 dB with different connections as seen in Figure 4.14 (a). The phase of the membrane line varies less than 5 degree



among different connections, see Figure 4.14 (b).

Figure 4.14: The magnitude of S_{12} and S_{11} (a) and phase response of S_{12} and S_{21} (b) for the membrane line with different connections.

The membrane open standard after reconnection has a good isolation between two ports ($|S_{21}|$ and $|S_{12}|$ are below -40 dB) and high reflection ($|S_{11}|$ and $|S_{22}|$ are below -0.2 dB) as shown in Figure 4.15.

In summary, by reconnecting all membrane TRL standards after the membrane TRL calibration, there are small variations in both magnitude and phase response observed for all membrane standards over the WR-03 frequency band.



Figure 4.15: S-parameters of the membrane open after the membrane TRL calibration.

4.5 Stability of the system

In this section, the drift related to time and temperature variation are studied. The set up for WR-03 drift measurement is shown in Figure 4.16. Four temperature sensor are used to monitor the changes of the temperature. Sensor 1 is placed on the table, sensor 2 is placed on the flange of one extender, sensor 3 is taped to one extender and sensor 4 is taped to the other as indicated in Figure 4.16. An extra computer is used to record the raw data at the VNA. A sweep is set to collect measurement data every third minute.



Figure 4.16: Drift measurement setup with four-port VNA-X N5242A.

In the first case, a OML thru is used to investigate the drift in transmission factor. The whole system is left over 15 hours. During the sweep, the raw data of $\frac{b_1}{a_1}, \frac{b_2}{a_1}, \frac{a_2}{a_1}, \frac{b_1}{a_2}, \frac{b_2}{a_2}$, and $\frac{a_1}{a_2}$ are taken and the raw S-parameters $(S_{11}, S_{12}, S_{21}, S_{22})$ are computed from this data using switch correction in section 2.6. To study the drift of transmission measurement, the ratio of $q = \frac{S_{12}}{S_{21}}$, which is the reciprocity correction factor in an unknown thru calibration, is computed. To have a good

reciprocity between two ports, this factor should be equal to 1 and should be stable.

The drift in q factor at some different frequencies is plotted versus the sweep time in three different formats: dB, magnitude and phase, see Figure 4.17.



Figure 4.17: Transmission coefficient at some frequencies versus the sweep time with different formats.

The amplitude of the transmission factor q does not change too much while the phase fluctuates from 0 degree in the beginning to roughly 10 degree at the end of sweep time.

Figure 4.18 illustrates the temperature variation during the sweep time. As shown in Figure 4.18, there are very small variations of temperature in two extenders (temperature sensor 3 and temperature sensor 4), indicating that the measurement happened in a quite stable environmental conditions.



Figure 4.18: Temperature variation versus the sweep time in four temperature output sensors.

The second transmission drift measurement is repeated for a long time of 70 hours. At the time of 17.5 hour, the cables are bent in around 10 minutes to check the effect of the cable to system's change. In Figure 4.19, it can be seen clearly that the drift in q factor are affected a lot when the cables are bent, especially in phase. The phase is decreased to -30 degree at the bent time. It takes time to recover (approximately 5 hours), but it can not obtain the previous value due to the drift. The cables have a significant effect on the stability of the system, so a home-made carries for the cables will be fixed for the future measurement.



Figure 4.19: Transmission coefficient at some frequencies versus the sweep time with different formats.

In the third case, the reflection drift measurement is done. Two OML short standards are connected to the flanges at the two ports. The system is left over night, around 15 hours. All raw data of the reflection measurement are taken as well. Based on these data, two reflection coefficients of two ports $\Gamma_1 = S_{11}$ and $\Gamma_2 = S_{22}$ are computed and they also should be stable. The drift in reflection coefficients at the two ports are plotted in Figure 4.20 in dB scale, linear scale and phase, respectively. The solid curves are of Γ_1 and the dash curves are of Γ_2 . They look stable over the sweep time except the phase deviation of port 2 in the first 2 hours and the last 2 hours. This is probably caused by the change in the incident wave of port 2 in those two time intervals, see Figure 4.21. Overall, the reflection drift results look more stable than the transmission drift, probably because it just depends on one port setup instead of two-port



setup in transmission drift measurement.

Figure 4.20: Reflection coefficients at two ports at some frequencies versus the sweep time with different formats.

In summary, the time drift effect in both the transmission coefficient and the reflection coefficient are performed during the stability investigation. There are variations in phase during both the thru and the reflect measurements. This phase shift may be caused by the change inside the VNA, the extenders or the cables. But it is difficult to say exactly it happened in which part of the system. Therefore, more investigations are needed to figure out this problem.

4.6 Assembly tolerance

The alignment tolerance which is the distance between the membrane and the air channel is decreased from 20 μ m in previous work to 10 μ m in this work. However, according to the measurement results of new membrane TRL standards, there is insignificant improvement compared to previous work [15]. Therefore, an investigation of circuit mounting tolerance in block which affects the waveguide to membrane transition are performed by simulation in this section. The misalignment of the membrane line circuit is simulated in HFSS with 5 μ m shift in block in different directions, including the waveguide embedded structure, see Figure 4.22.



Figure 4.21: Power drift in two ports and the drift in q factor at some frequencies versus the sweep time.



Figure 4.22: HFSS simulation of misalignment of membrane line circuit.

There are four possibilities of membrane line circuit misalignment in the waveguide block: right, left, up and down. However, it can be reduced to two cases because of the symmetric structures of the circuit and the block. More serious cases of circuit misalignment in block such as 5 μ m left-up shift and 5 μ m right-up shift are also considered. The misalignment will affect the magnitude of the reflection coefficients of two ports of the membrane line and makes them different compared to the well aligned case. The biggest difference is observed when membrane line circuit is shifted 5 μ m in both left and up directions, see Figure 4.23, but this difference are not significant.



Figure 4.23: Membrane line circuit is shifted left of 5 μ m and up of 5 μ m in block.

The phase response of S_{12} in the perfect mounting case is different of 1 degree compared to the perfect mounting case, see Figure 4.24. However, the phase responses of the S_{11} are different between two cases.

In general, misalignment of circuit in block doesn't affect significantly the magnitude, but it affects the phase responses of the refection coefficients at two ports.



Figure 4.24: Phase of S_{12} and S_{11} in the alignment and misalignment cases.

Chapter 5 Conclusion

In this work, the membrane standards for TRL calibration technique have been developed to characterise the S-parameter of membrane circuits in WR-03 frequency band. Using this method, the reference planes are set directly on the membrane circuit, thus reducing the need of extra de-embedding procedure. The characterised S-parameters of some membrane DUTs such as the membrane TFR, the membrane TFC and the shorted stub filter, agree with the HFSS simulations, validating the feasibility of this technique.

Compared to previous work [15, 16], the new E-plane split blocks with recessed surface give better results than the old ones due to better beam lead to ground connection. Moreover, investigation on the repeatability of the waveguide connection shows that this technique is applicable in WR-03 band. During the study about measurement errors coming from of the test setup, the time drift and temperature variation are investigated. The study indicates that the measurement result is sensitive to moving cables. Therefore, the carriers are necessary to fix the cables. Additionally, the mounting tolerance of the membrane line circuit in manufactured in house block is simulated and evaluated as well. There is insignificant influence of the assembly tolerance on the result of the membrane line standard.

Although a lot of work has been done, there is still more work that can be continued. This technique can be applied to characterise more membrane DUTs, not only passive components but also active components such as membrane diode, etc. Currently, the membrane Schottky diode for TMIC is being processed and evaluated at Chalmers University of Technology [34]. Furthermore, an averaged calibration approach can be considered to reduce the calibration error. In addition, it is difficult to determine from which part of whole setup the phase shift originates. It may happen in the VNA, the extender or even cables. Thus, further investigation on the stability of the whole system can be pursued.

The designed waveguide embedded TRL calibration based on membrane circuits has been developed for two-port devices, but it is possible to develop this technique further in the near future to characterise S-parameters of fourport networks such as directional coupler, rat race, etc. Because the frequency extender is commercially available up to 1 THz now, this technique can move up to higher frequency. Thus, a new membrane TRL kit for higher frequency applications can be modified and fabricated in the future.

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REFERENCES

Appendix A

Paper A

Characterization of thin film resistors and thin film capacitors integrated on GaAs membranes for submillimeter wave circuit applications

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Characterization of thin film resistors and capacitors integrated on GaAs membranes for submillimeter wave circuit applications

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Abstract

In this paper we describe the fabrication and characterization of thin film resistors and capacitors integrated on a 3 µm thick GaAs membrane. The thin film resistors and capacitors are based on NiCr and SiN_x materials respectively. Onwafer probing DC characterization of these thin film components was performed before removing the GaAs substrate. The corresponding high frequency characterization in the WR-03 frequency band (220-325 GHz) was demonstrated utilizing a membrane-based two-port TRL calibration technique. The measurement results have shown a good agreement with the simulation.

1 Introduction

There is a strong need for development of highly integrated THz-electronics based on GaAs Schottky diodes for earth observation instruments as well as THz imaging systems. Several planned missions and applications will require increased functionalities (e.g. sideband separation) involving more complex circuits. For high frequency applications, membrane supported Terahertz Monolithic Integrated Circuits (TMICs) have shown advantages such as easy assembly and low loss in substrate [1]. In this approach, the semiconductor substrate is removed and the circuits are supported by an ultra thin (i.e. a few microns thick) semiconductor membrane. Up to date, high performance GaAs Schottky mixers based on this technique have been demonstrated [1-3]. To increase the design flexibility and to achieve multifunction performance on a MIC chip, compact circuit components of thin film resistors (TFRs) and thin film capacitors (TFCs) are commonly used for DC bias network or to separate DC and RF signals.

For TFR applications, materials like TiN [4], Ta_xN [5], and NiCr [6] are commonly used. For TFC applications, variety of materials such as Ta₂O₅, Al₂O₃, SiO₂, SiN_x [7] and ferroelectric materials like barium strontium titanium (BST) [8] can be used. In this work, the TFRs and TFCs are fabricated using NiCr and SiN_x materials respectively, because of the high resistivity and low temperature coefficient of resistance (TCR) exhibited by NiCr and high breakdown voltage exhibited by SiN_x.

For a complex membrane TMIC design, S-parameter characterization of each building component is very useful to get the input values and to verify the design. However, at high frequencies traditional on-wafer probing S-parameter measurements are challenging due to contacting tolerances of probes, radiation and coupling effects, and are unsuitable for fragile membrane circuits. Instead, Sparameter characterization of membrane circuits in the WR-03 frequency band (220-325 GHz) utilizing the TRLcalibration technique has been developed [9]. In this work, TFRs based on NiCr and TFCs based on SiN_x were fabricated on a 3 µm thick GaAs membrane. High frequency characterization of the TFRs and TFCs in the WR-03 frequency band is demonstrated utilizing the developed membrane-based two-port TRL calibration technique.

2 Membrane thin film resistor and capacitor design

The membrane TFR and TFC circuit design was performed using a three-dimensional electromagnetic simulator (Ansoft HFSS) and a microwave circuit simulator (Agilent ADS). All of the membrane circuits are designed to have the same waveguide to planar transitions at both ends. The simulated return loss is better than 15 dB over the WR-03 band for a single waveguide transition. In order to minimize variations of the mechanical blocks, the membrane length for all the membrane TFRs and TFCs are the same. In this work, two types of TFRs were investigated, see Fig.1. One has the resistor connected in series configuration between two transmission lines. The other type has the resistors connected in a shunt configuration via the beam lead ground.

The TFC has the capacitors with top electrode connected with the beam leads ground via an air-bridge. As a comparison, a grounded stub filter with the stub width same as the top electrode width of the capacitor was designed. The fabricated TFC and the stub filter are shown in Fig.2. More simulation results will be presented together with the measurement results in section 5.



Figure 1 Microscope pictures of two types of membrane TFRs.



Figure 2 Microscope pictures of the membrane TFC and the membrane grounded stub filter.

3 Membrane thin film resistor and capacitor fabrication

The epitaxy structure for the membrane TFRs and TFCs was grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE). The structure includes a 400 nm thick $Al_{0.7}Ga_{0.3}As$ layer followed by a 3 µm thick GaAs layer, which are used as the etch stop layer and the membrane layer respectively.

Fig.3 shows schematics of the membrane TFR and the membrane TFC. The TFR was formed by resistive evaporating a 60 nm thick NiCr film followed by a lift off process. An interconnection metal of 10 nm/300 nm Ti/Au was then deposited, and the membrane was defined. Before sputtering an Au seed layer for electroplating, the NiCr thin film area was protected by e-beam resist PMGI.

The transmission lines and beam leads were then gold plated to achieve the final thickness of approximately 2 μ m after the Au seed layer removal.

The Ti/Au interconnection layer was introduced to avoid disconenction between the transmission line and the NiCr thin film. Because a misalignment can introduce a small gap between the plated transmission line and the PMGI pattern. The NiCr thin film in the small gap without PMGI protection will be removed during an ion milling of the Au seed layer.

The fabrication of the TFC started with depositing a bottom electrode pad. This is followed by the deposition of a low stress SiN_x layer using the plasma enhanced chemical vapor deposition (PECVD) technique. In the subsequence step, the SiN_x in the transmission line and beam lead area was removed. Then, the area between the top electrode and the transmission line was covered by PMGI before sputtering the Au seed layer. Next, the beam leads and the top electrode with connection of the transmission line were plated. An air bridge structure was formed after dissolving the PMGI.

After fabricating the TFR and TFC structures on the topside, the wafer was mounted topside down on a Si wafer using wax. Then the substrate was mechanically lapped down to 50 μ m. The remaining substrate was removed using selective wet etching which stopped at the AlGaAs layer. Then AlGaAs layer was selectively etched away using a dilute HF. Finally, the individual membrane circuits were released and collected on filter paper after dissolving the wax.



Figure 3 Schematics of (a) the membrane TFR and (b) the membrane TFC.

4 DC characterization

In order to check the reliability of the process and the edge contamination effect [10], test structures with simple electrodes in series connected with different sizes of TFRs and TFCs were also fabricated, see the insets of Fig. 4 and Fig. 5. As shown in Fig. 4, the resistance of the TFR increases linearly with the length-to-width ratio for a 60 nm thick NiCr film, indicating a sheet resistance of around 46 Ω/\Box . For TFCs with a 320 nm SiN_x film, a value of 180 pF/ mm² is extracted from the linear size dependent capacitance, see Fig. 5. The linear size dependence of the

resistance and capacitance indicate the edge contamination effect can be neglected in our process.

For the membrane TFCs and TFRs, DC characterizations were also performed before the backside process. The resistance is around 90 Ω for series configuration T FR and 180 Ω for each side of shunt configuration TFRs, corresponding to a 64 μ m x 125 μ m size and a 20 μ m x 75 μ m size of the NiCr thin film respectively. The capacitance of a 20 μ m x 60 μ m size TFC is around 0.2 pF.



Figure 4 DC resistance as a function of length-to-width ratio for the TFRs with a 60 nm thick NiCr film, the inset shows test structure of a TFR.



Figure 5 DC capacitance as a function of size for the membrane TFCs with a 320 nm thick SiN_x film, the inset shows test structure of a TFC.

5 S-parameter characterization

The membrane circuits were mounted in E-plane split blocks for the S-parameter characterization. The WR-03 setup consists of the Oleson Microwave Labs (OML) V03VNA2-T/R frequency extension modules with an Agilent E8361A PNA S-parameter test set. Further details of the waveguide embedding structures, measurement setup, and membrane TRL calibration can be found in [9]. Fig. 6 (a) and (b) show the result of S-parameter characterization of the membrane TFRs. The unsmooth response of S_{11} in both types of TFRs is probably due to imperfect repeatability in waveguide to membrane transitions.

Fig.7 (a) and (b) show the S-parameter characterization of the membrane TFC and the membrane stub filter, respectively. A 3 GHz frequency shift both for the membrane TFC and the membrane stub filter were observed between the simulation model and circuit measurements. This small frequency shift is probably due to either modelling error or manufacturing tolerances. Since the simulation doesn't include any loss such as the surface roughness of the Au, a difference between measured S_{12} and the simulation was observed in both cases.

Compared with the membrane stub filter, the membrane TFC has less reflection at the resonace frequency and broader response in the reflection, which is due to either a broader bottom electrode width or an extra loss from the dilectric SiN_x layer.



Figure 6 S-parameter characterization and HFSS simulation of the (a) series configuration (b) Shunt configuration membrane TFRs.





Figure 7 S-parameter characterization and HFSS simulation of the (a) membrane TFC and (b) membrane stub filter.

6 Conclusions

We have developed a membrane TFR and TFC process, based on NiCr and SiN_x materials respectively. DC characterization of the TFRs and TFCs shows linearly sizedependent resistance and capacitance, indicating the process is reliable. Utilizing the developed membrane TRL calibration technique, S-parameter characterization of the TFRs and TFCs was demonstrated in the WR-03 frequency band. The measurement results agree with the HFSS simulation. Both the DC characterization and the high frequency responses of the membrane TFRs and TFCs provide useful input for the membrane TMIC design.

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