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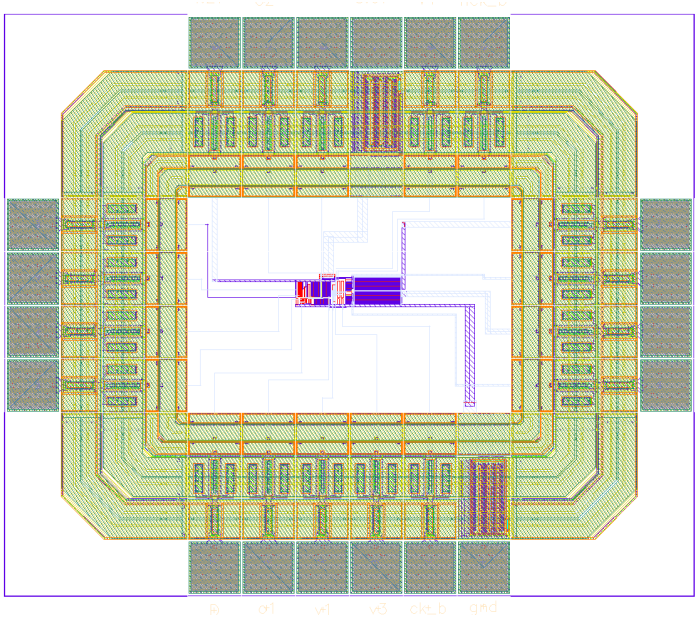

Ultra Low Power Low Voltage ASIC Design and Implementation

For a Novel Bone Conduction Implant (BCI) System

Master of Science Thesis in Integrated Electronic System Design (MPIES), Computer Engineering

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Göteborg, Sweden, May 2011

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To Sara…

Ultra Low Power Low Voltage Application-Specific Integrated Circuit (ASIC) Design and implementation for a Novel Bone Conduction Implant (BCI) System

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Abstract

Patients who are suffering from conductive hearing loss, single sided deafness and mixed hearing loss, cannot be rehabilitated by conventional air conduction hearing aids due to the functionality losses in the middle ear. Since in these hearing impairments, the cochlea functions perfectly, a bone conduction hearing aid is used for transmitting sound data to the cochlea. Today, percutaneous Bone Anchored Hearing Aid (BAHA) is an important alternative for such individuals. These devices use a percutaneous snap coupling and bone anchored implant that incurs skin infections, requires a life-long commitment of care every day, and there is a risk for implant damage due to trauma.

A novel Bone Conduction Implant (BCI) system is designed as an alternative to the percutaneous system, because, it leaves the skin intact. The BCI system comprises digital and analog signal processing units and applying amplitude modulation technique, sound information is transmitted to a permanently implanted transducer via an inductive link system through the intact skin. A coupling insensitive efficient inductive power and data link is designed that can deliver maximum force output to the transducer.

The BCI system uses a 1.3 volt standard hearing aid battery that provides power to the entire electronics and the transducer. In the process of designing and implementing the electronics of the BCI, the most critical, challenging and interesting focus is to have a very high efficiency system. Using ultra low power low voltage electronics circuit design and implementation with matured technologies, the power dissipation can be reduced and the whole device will be high efficient and the battery lifetime will be increased. The power amplifier design is another important part of the electronics that must be designed very efficiently. The proposed high efficiency switching power amplifiers are Class-D and Class-E. Studying and designing an application-specific integrated circuit for BCI system that covers all the demands on the power and efficiency is the main goal of this project.

This Project has been divided into two different parts. In the first Part, Two different prototypes which use Class-D and Class-E as their Power Amplifier have been designed and implemented. The results proved Class-D amplifier as a better topology for this specific application with current consumption bellow 4mA which is significantly lower than 22mA which is consumed by Class-E for similar RF load. Spartan 3 board has been used as FPGA board to produce Clock signal and Pulse-density-Modulation (PDM) to Pulse-Width-Modulation conversion.

In the second part, integrated version of proved circuit was designed in 0.35um Standard CMOS Technology and it was submitted for fabrication in SOIC 20 standard die frame.

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Contents

1. Introduction

1.1. Bone Conduction Implant (BCI) System

For patients who are suffering from conductive hearing loss, Bone Conduction implant (BCI) is an important method to restore hearing ability. The percutaneous Bone Anchored Hearing Aid (BAHA) is the conventional type of bone conduction hearing aid which is anchored to the skull bone by a titanium fixture [1]. Since the titanium fixture needs to be screwed into the skull bone, BAHA suffers from drawbacks such as skin infections, accidental or spontaneous loss of the bone implant, and patient refusal for treatment due to stigma [2]. The transcutaneous BCI is a good alternative to the fixture type: it leaves the skin intact and puts the transducer permanently under the skin [2].

The BCI is a wireless biomedical device which produces the energy for the implanted part remotely. In a wireless biomedical device, a safe and effective method of delivering energy must be used. An inductively coupled RF link is a common method to deliver energy to implanted biomedical devices [3]. Figure 1-1 shows a typical block diagram of the BCI system.

The BCI consists of two separate parts: external and internal parts to the body which are separated by the skin. The external part samples the sound, processes, amplifies and delivers the proper signal via a tuned RF link. The internal part receives the signal and converts it to a mechanical vibration with a transducer.

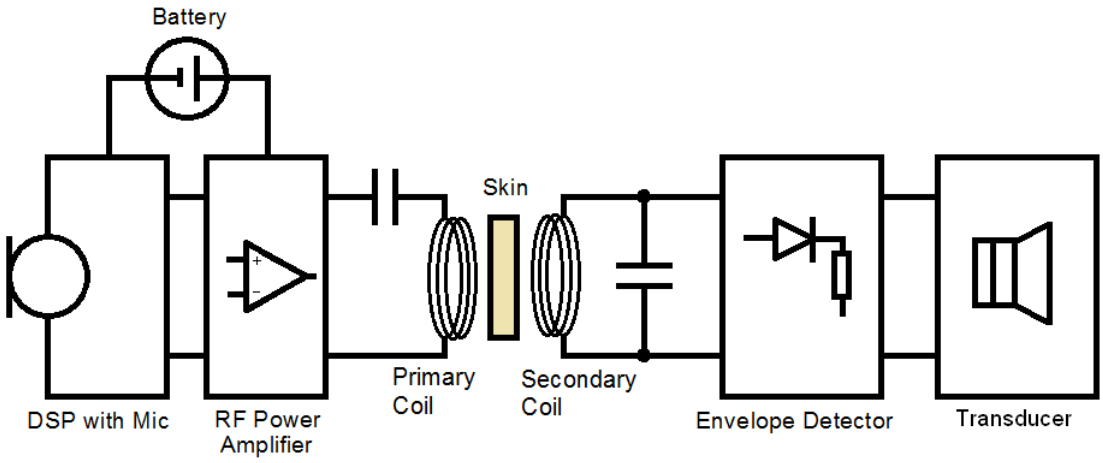

Figure 1-1: Block diagram of the BCI system

1.2. The scope of this project

The main aim in this project is to design a high performance RF power amplifier to deliver the required amount of energy from low voltage battery. Two common topologies as power amplifiers (Class-D and Class-E) have been studied and tested as discrete circuits; the results are presented in next chapter.

1.3. Restrictions of the scope of this project

In the first stage of BCI, the sound should be sensed and processed by microphone and Digital Signal Processing units respectively. In this project, GA3285 DSP model from SOUND DESIGN TECHNOLOGIES® LTD has been used [4].

As the inductive link for wireless transmission, RF inductive link designed by Taghavi [1] has been used. Since the RF link is tuned to 120 kHz, this frequency must be used as the operating frequency of the RF power amplifier.

2. Discrete Circuit Design

2.1. Digital Signal Processor Model

In this project, discrete circuit level design was started by studying the GA3285 DSP operation and output waveform. The important parameters of the DSP in this project are supply voltage, output frequency and type of output signal.

The GA3285 DSP can work with a supply voltage between 0.95 V and 1.5 V [4]. The output signal of the DSP is a 1-bit PDM (pulse density modulation) data stream. According to its nature as low impedance and differential output voltage, the DSP output signal is suitable for driving zero-biased hearing aid receivers [4].

Figure 2-1 shows the DSP output waveform. GA3285 uses a 2.048 MHz sampling rate. Thus, the minimum pulse width at the output is 488ns. One frame of output PDM bistream consists of nine sampling frequency pulses (corresponding to a frame rate of 227.5 kHz).

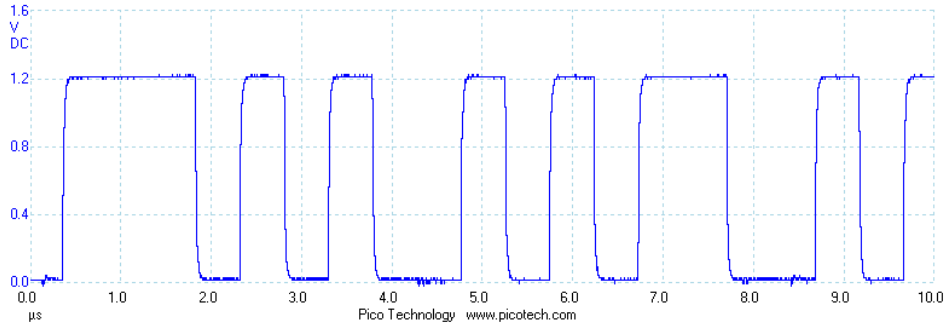

Figure 2-1: Output waveform of GA3285

2.2. PDM to PWM Conversion

Since the DSP output signal is inherently PDM, it uses oversampling technique to represent the input signal in digital domain with higher frequency. Higher frequency is more expensive in terms of power consumption. In addition, due to higher switching rate, PDM makes more switching noise in frequency domain than PWM. To reduce the switching noise, PDM to PWM conversion must be done [5].

Figure 2-2 shows an example of a PDM bitstream and its PWM related signal. The total pulse widths in one frame in both signals are the same, but in PDM, the pulse width is a multiple number of oversampling frequency which is much higher than clock frequency in PWM. The important factor in conversion that must be obeyed is the size of the frame which is the same in both PDM and PWM signals. The important point in PDM and PWM is that in both bitstream starts with level "1" which is useful for extracting PDM and its related PWM code.

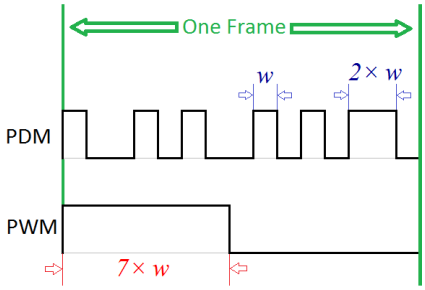

Figure 2-2: PDM vs PWM in one frame.

Before converting PDM to PWM, the size of the frame must be defined. Since the size of PDM frame is already defined, PWM frame must be identical. In this project, a Xilinx Spartan-3 FPGA was used for digital signal processing and clock generation [6]. Spartan-3 uses 50 MHz as the main clock frequency. Selecting a proper frequency is one of the obstacles in digital implementation, because on one hand, the frequency should be close to 227.5 kHz to minimize the error for PDM to PWM conversion, but on the other hand, it should be related to 120 kHz to which the RF link is tuned. As a trade-off between two above cases, a 240 kHz frame was selected for PWM representation. To keep the error between PDM and PWM frames at minimum, the end of each PWM frame is synchronized with the beginning of next PDM frame by 50 MHz sample clock.

Based on DSP output waveform observation, PDM code and its PWM code were extracted as figure 2-3. Based on what mentioned above there is a small difference between PDM and PWM frames that is not shown in figure 2-3.

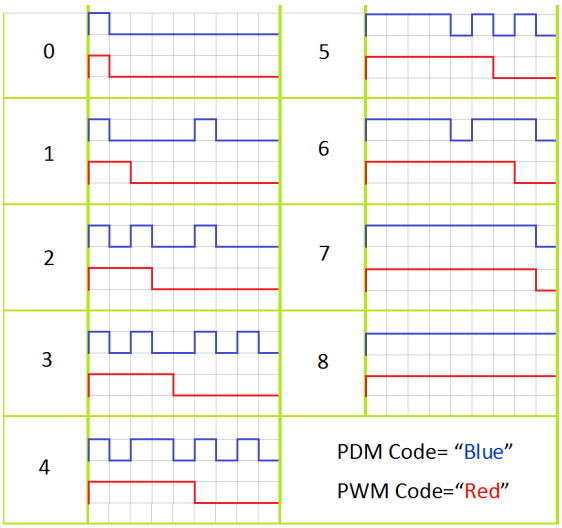

Figure 2-3: PDM and PWM codes in a 9-pulse width frame.

The Spartan-3 FPGA board cannot read the DSP outputs directly. An interface circuit is needed to feed the DSP output to the FPGA board. Here a simple circuit with a BC107 BJT transistor is used to connect the DSP with the FPGA board (Figure 2-4).

Figure 2-5 shows the PDM to PWM conversion at the output of FPGA board. There are some spikes in switching periods which is due to interface circuit and weakness of grounding.

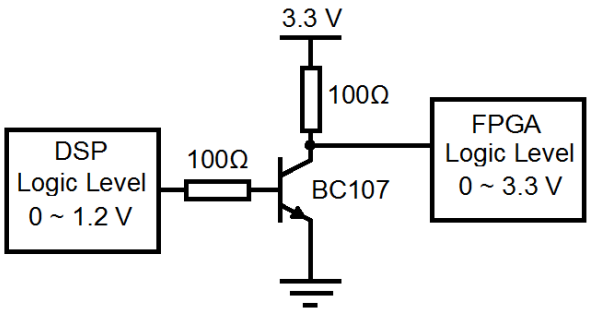

Figure 2-4: Interface Circuit between DSP and FPGA Board.

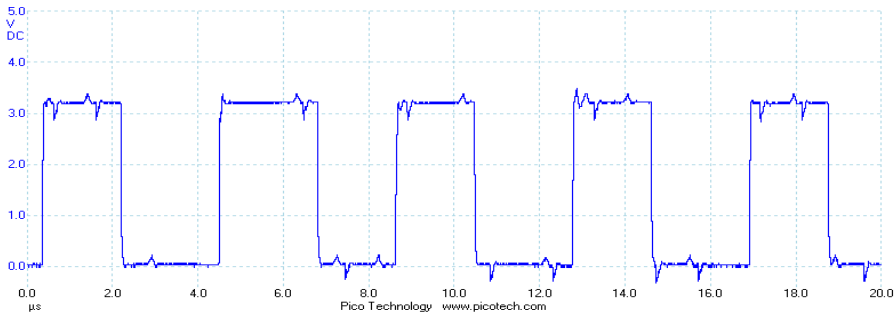

Figure 2-5: PWM bitstream at the output of FPGA Board.

2.3. Clock generation

Clock pulse generation is necessary for both Class-E and Class-D RF power amplifiers (PA) as a carrier signal for modulation. The Spartan-3 FPGA board can produce accurate 120 kHz from 50 MHz main clock frequency. Figure 2-6 shows two overlapped complementary clock pulses generated by Spartan-3 board. The reason of using overlapped clock pulses will be described in chapter 3 (part 3.2).

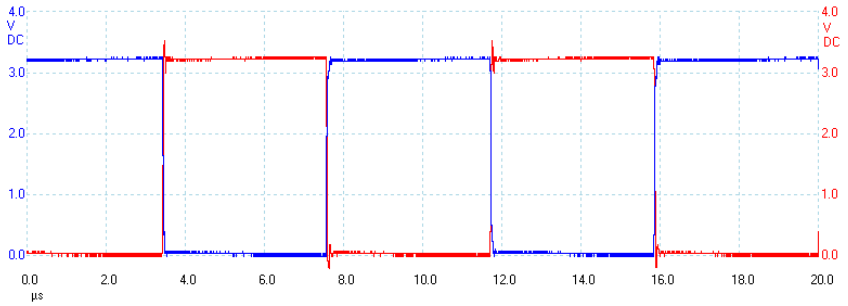

Figure 2-6: 120 kHz Complementary clock pulses generated by Spartan-3 FPGA board.

2.4. Inductive RF Link

An inductive RF link is the media to deliver data and power to the implanted part of medical device under the skin. The RF link used here was designed and implemented by Taghavi[1]. The main goal of this project is to drive the link with maximum efficiency. Figure 2-7 shows the electrical model of the RF link.

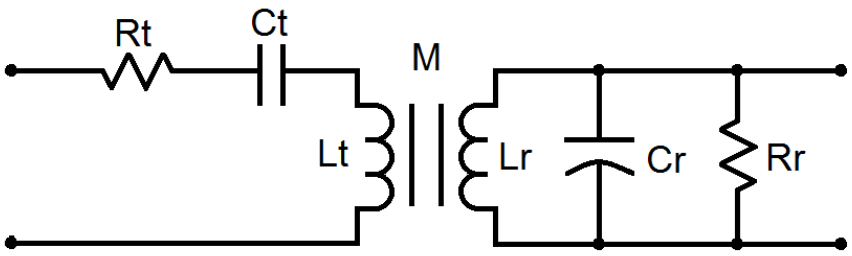

Figure 2-7: Electrical model of inductive RF link.

Since all electrical parameters of the RF link have already been designed, the only factor we can play with in design is coupling coefficient (k) which describes the mutual inductance which occurs between transmitter and receiver coils.

$$k = \frac{M}{\sqrt{L_t \cdot L_r}} \tag{2.1}$$

The coupling coefficient is a dimensionless quantity and $0 \le k \le 1$ [1]. A simplified model for the RF link can be obtained by considering the effect of secondary coil on primary coil (Figure 2-8).

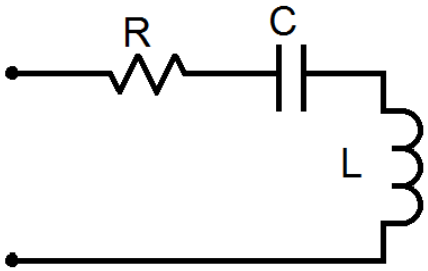

Figure 2-8: Simplified electrical model of inductive RF link.

The new values for R, C and L of the model can be extracted from figure 2-9. Figure 2-9 is a simulation result of implemented inductive RF link. The horizontal axis in both curves is the coupling coefficient which depends on the distance between the two coils. The upper curve shows the total load resistance (Ω) seen in the primary coil as a function of the coupling coefficient.

The lower curve shows the total load inductance (μH) seen in the primary coil as a function of the coupling coefficient. The related capacitance of the RF link can be obtained from (2.2) and (2.3).

$$f = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{2.2}$$

$$f = 120kHz$$

$$C = \frac{1}{4\pi^2 \cdot L \cdot f} \tag{2.3}$$

Three points in each curve are shown to demonstrate the related values in 0 mm, 4 mm and 8 mm distance between the coils.

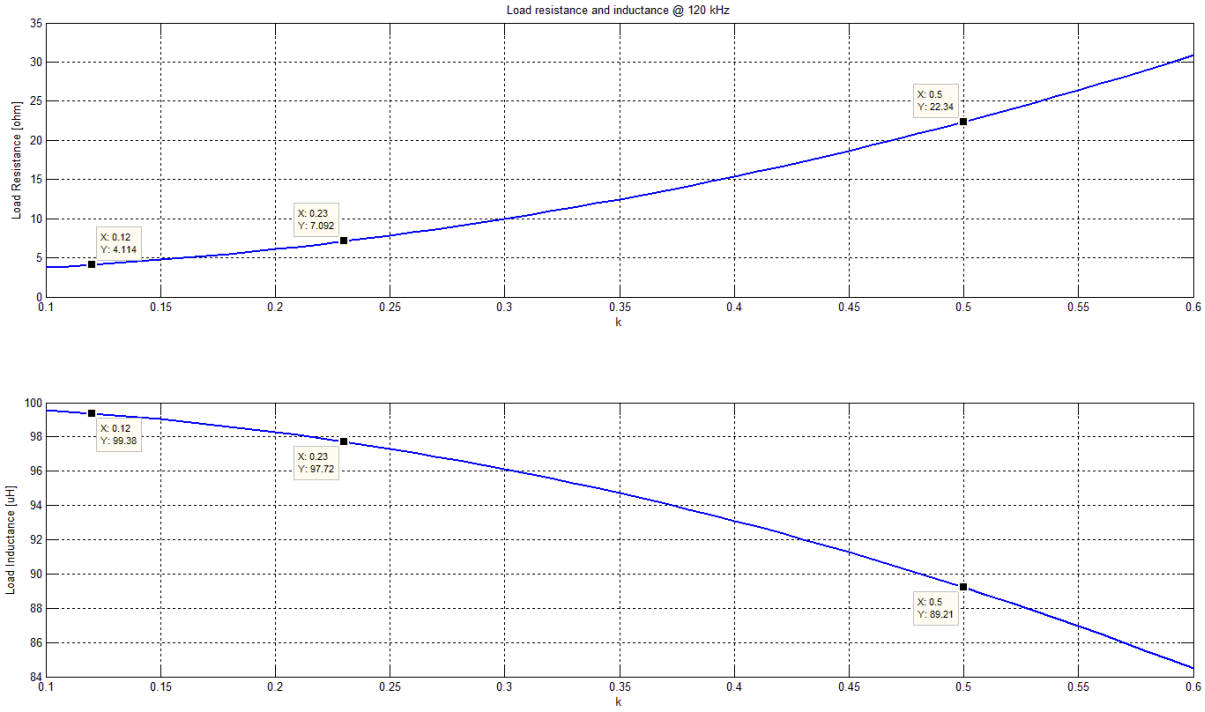

Figure 2-9: The simulation result of the RF link based on coupling coefficient (*k*).

2.5. Class-E Power Amplifier

The Class-E power amplifier is a switching-mode power amplifier, introduced by Sokal in 1975 [7]. In most RF power amplifiers, the main part of power is consumed in the active device(s). Thus, if the product of voltage and current of switching device are minimized, the maximum efficiency in term of power consumption will be obtained. Allocating the maximum voltage and current across the switch transistor at different times is the main goal of the Class-E power amplifier (Figure 2-10)

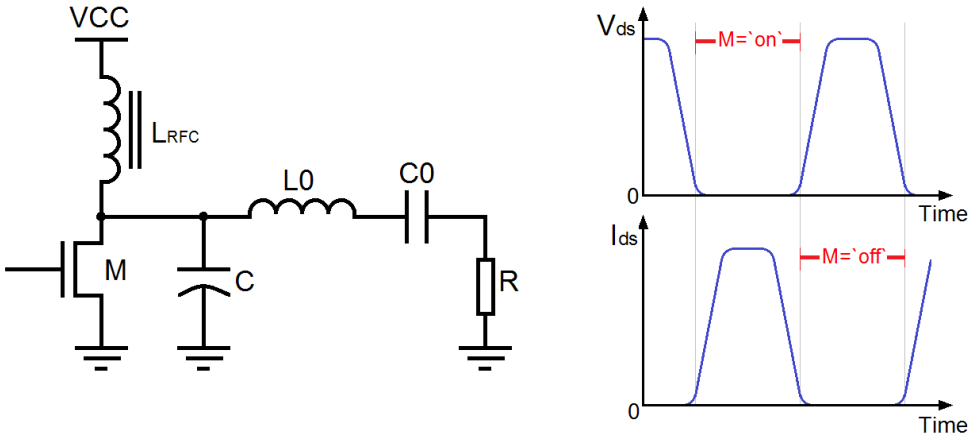

Figure 2-10: A typical circuit for Class-E Power Amplifier with the desired voltage/current waveforms of power transistor.

Obtaining high efficiency in a Class-E amplifier does not rely on a certain circuit configuration or parameters, but [7, 8, 9] define three main requirements:

- The voltage across the switch must be zero at switch turn-on time
- The time derivative of the switch voltage must be zero at switch turn-on time
- The shunt capacitor must delay the rise of the switch voltage until after the transistor is Off

Fulfilling these requirements is not easy, because a real transistor has nonzero On resistance and consequently the switch voltage cannot be brought back to zero completely. Furthermore, non-ideal components in tuned circuit (L0 and C0) with output capacitor of transistor will influence the tuned circuit.

Based on previous discussion, RF modulation is needed to deliver the power and data in a wireless medium. In this project, amplitude modulation is used for transmitting data. Figure 2-11 shows the designed RF Class-E power amplifier. A schottky diode (D) is used after PDM/PWM conversion to protect the FPGA board from negative voltage. An N-Channel transistor [10] was selected as the switch transistor (M). To make AM modulation, the PWM bitstream is applied on top of L_{RFC}. Besides the main function of L_{RFC} as a current source, its combination with C_1 can also make an L-C filter. Thus, an analog signal through L_{RFC} is applied to the drain of transistor M, where a 120 kHz clock pulse is applied to the gate of M. Figure 2-12 shows the output RF signal at the primary coil (V_P) in unloaded situation. The maximum 7.8 V peak-to-peak output signal was obtained. This circuit consumes 15 mA without digital signal processing part.

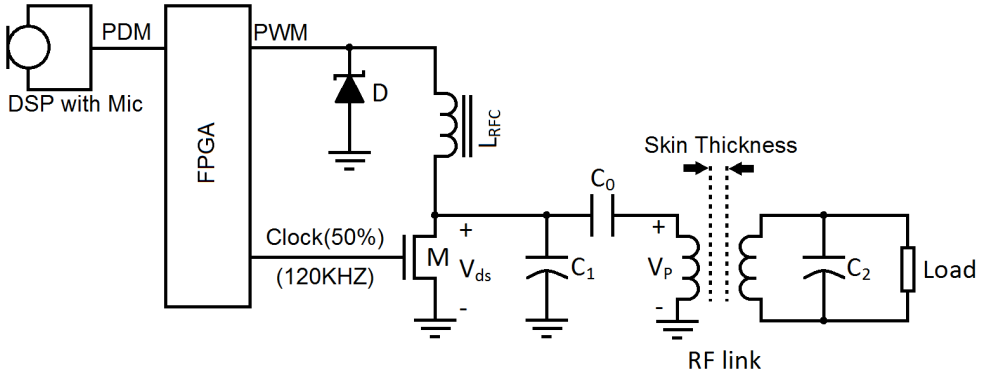

Figure 2-11: RF Class-E Power Amplifier Circuit.

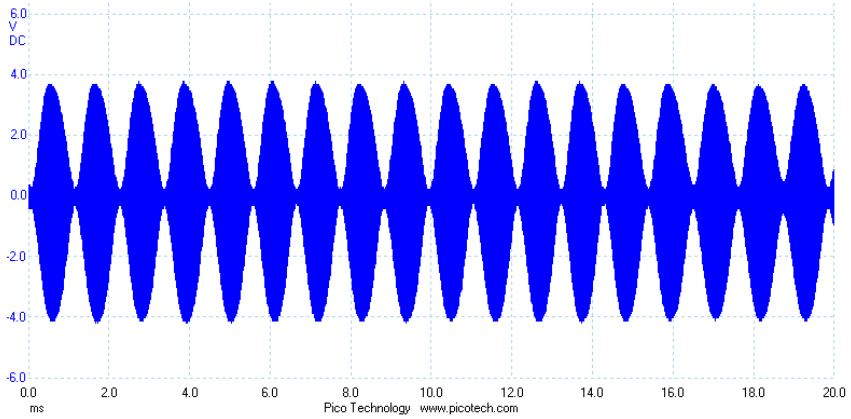

Figure 2-12: RF output signal (V_P) @ 4 mm distance (optimum position).

Figure 2-13 shows the RF output signal (V_P) at three different distances between coils. At unloaded situation (8 mm), the maximum output voltage level is obtained (7.8 V p-p). When the amplifier is loaded, the output level signal decreases (4.5 V p-p). At minimum distance, the minimum output voltage is obtained (2.5 V p-p). As is clear from figure 2-13, all three waveforms have some distortion; the worst case happens at minimum distance. There are some sources of distortion which are: non-ideal RF choke, un-tuned LC tank (since we cannot use any arbitrary values for L and C) and the output capacitor of the switch transistor which influences the resonance circuit.

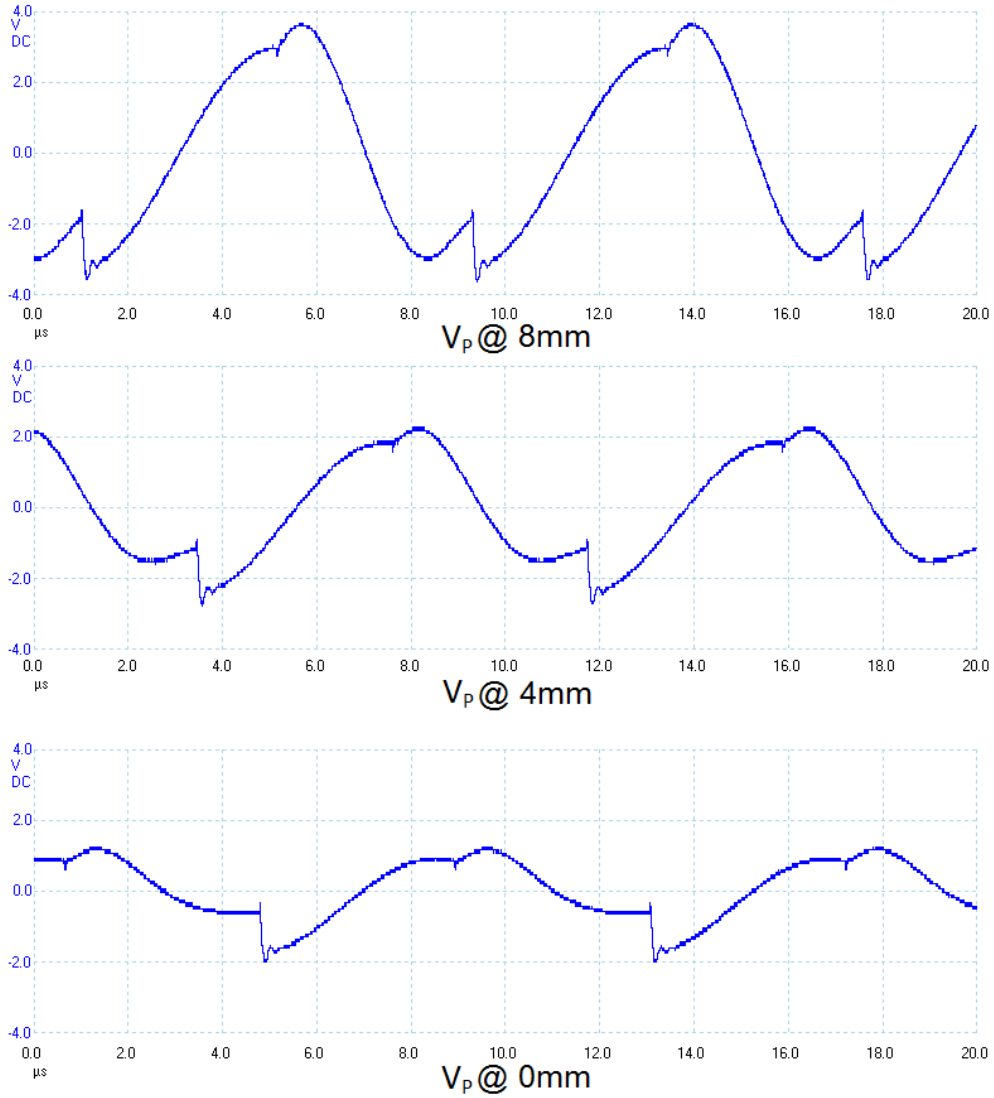

Figure 2-13: Class-E RF output Signal at different distances.

Figure 2-14 shows the drain voltage of transistor in Class-E amplifier at different distances. The effect of changing in resonance components is shown in figure 2-15 [11].

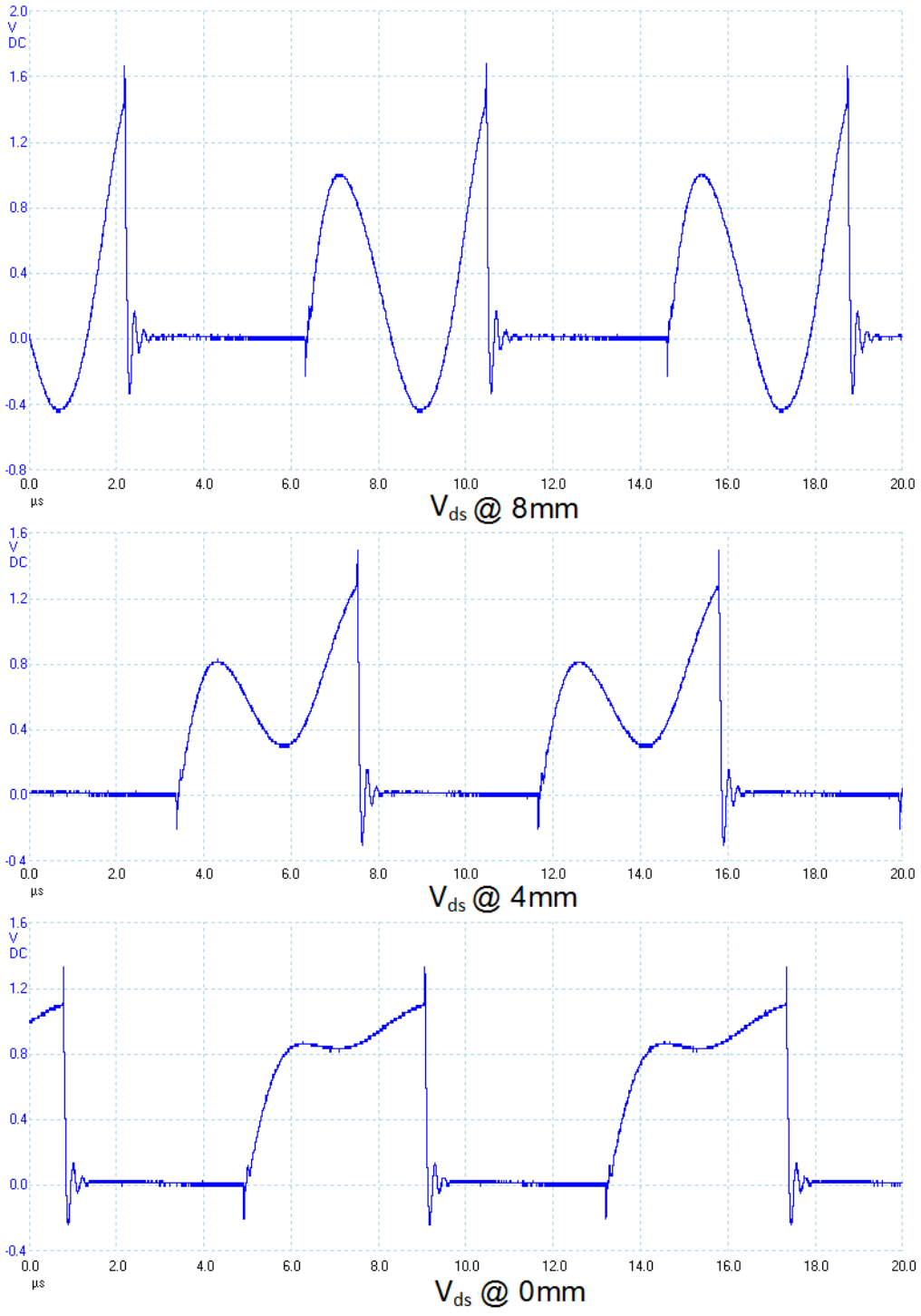

Figure 2-14: Class-E drain voltage of power transistor at different distances.

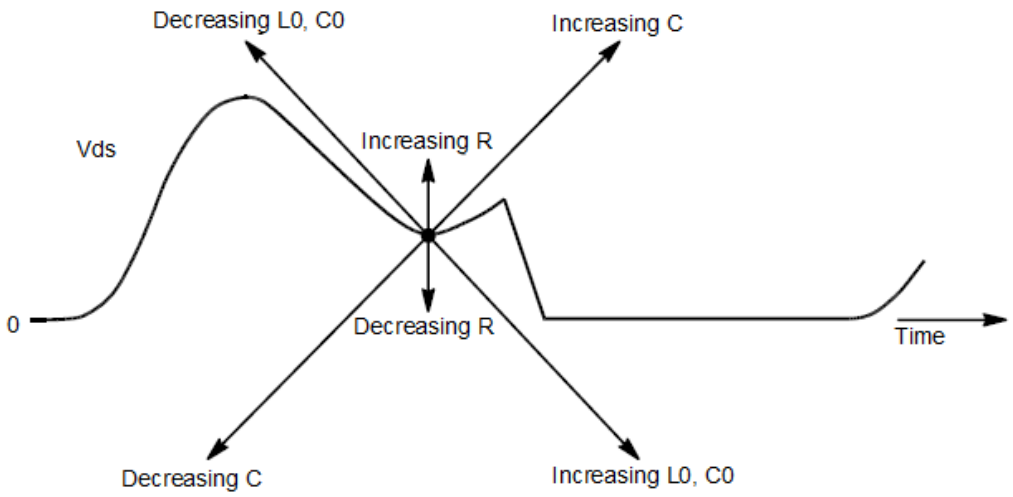

Figure 2-15: Effects of Changing Components in Class-E Amplifier [11].
L0, C0, C and R refer to figure 2-10.

Finally, the Class-E amplifier supply current and RF link output voltage at different distances are listed in table 2-2. The applied signal to DSP is a baseband signal with the amplitude of 0.6 V and the frequency of 1 kHz.

Distance (mm)	*Current Consumption (mA)*	*RF link output voltage (V)*
0 mm	*22*	*2.5*
4 mm (optimum)	*15*	*4.5*
8 mm (unloaded)	*11*	*7.8*

Table 2-2: Current consumption and output voltage (p-p) of RF Class-E Amplifier at different distances

2.6. Class-D Power Amplifier

At the desired frequency of this project (120 kHz), Class-D PA might be more beneficial in terms of the timing control of switches and power consumption [9]. The same transistor and serial resonance tank, used in Class-E, have been used in a Class-D design. Figure 2-16 shows the schematic of the Class-D PA. After converting the PDM to PWM by FPGA, the signal is applied to a LC low-pass filter which has a high cut-off frequency at 8 kHz (baseband frequency of speech). Two transistors are used as switches in Class-D PA and work in opposite phases. Figure 2-17 shows the measurement of the AM modulated signal of 1 kHz sine wave, applying to the RF link at 4 mm distance between coils.

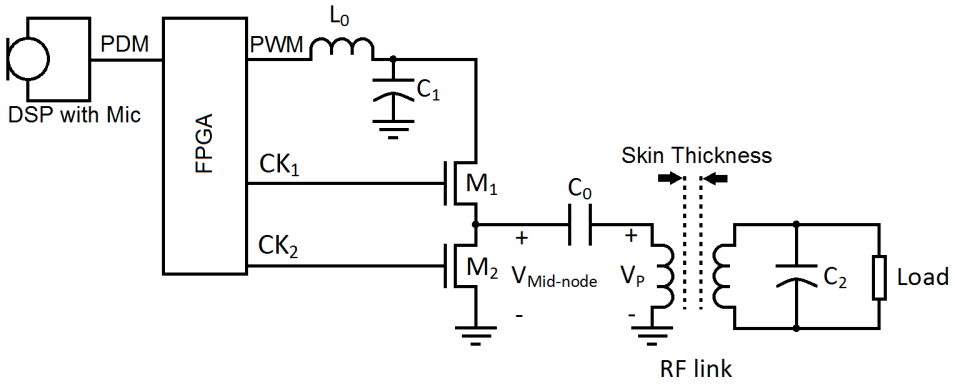

Figure 2-16: RF Class-D Power Amplifier Circuit.

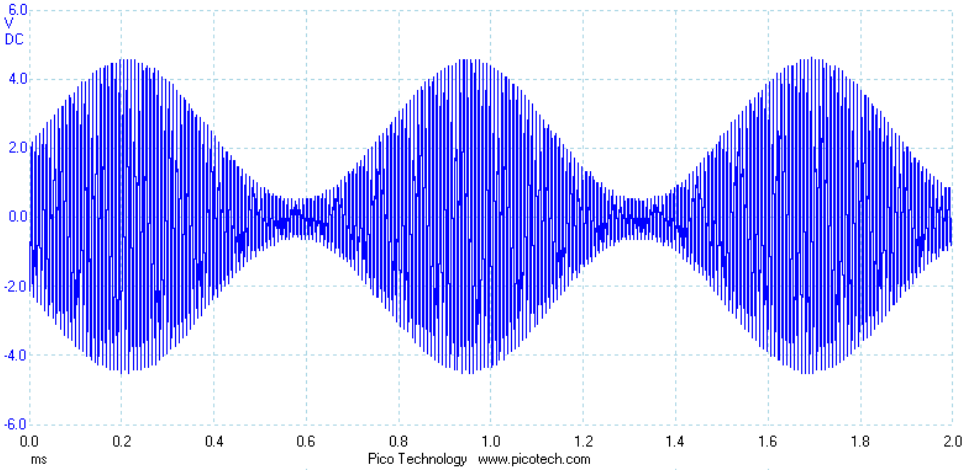

Figure 2-17: PA output Signal @ 4 mm.

Figure 2-18 shows the output signal of Class-D PA when it is unloaded. The signal illustrates the AM modulation of arbitrary voice signal. The maximum RF signal up to 16 V p-p with 7 mA current consumption is obtained.

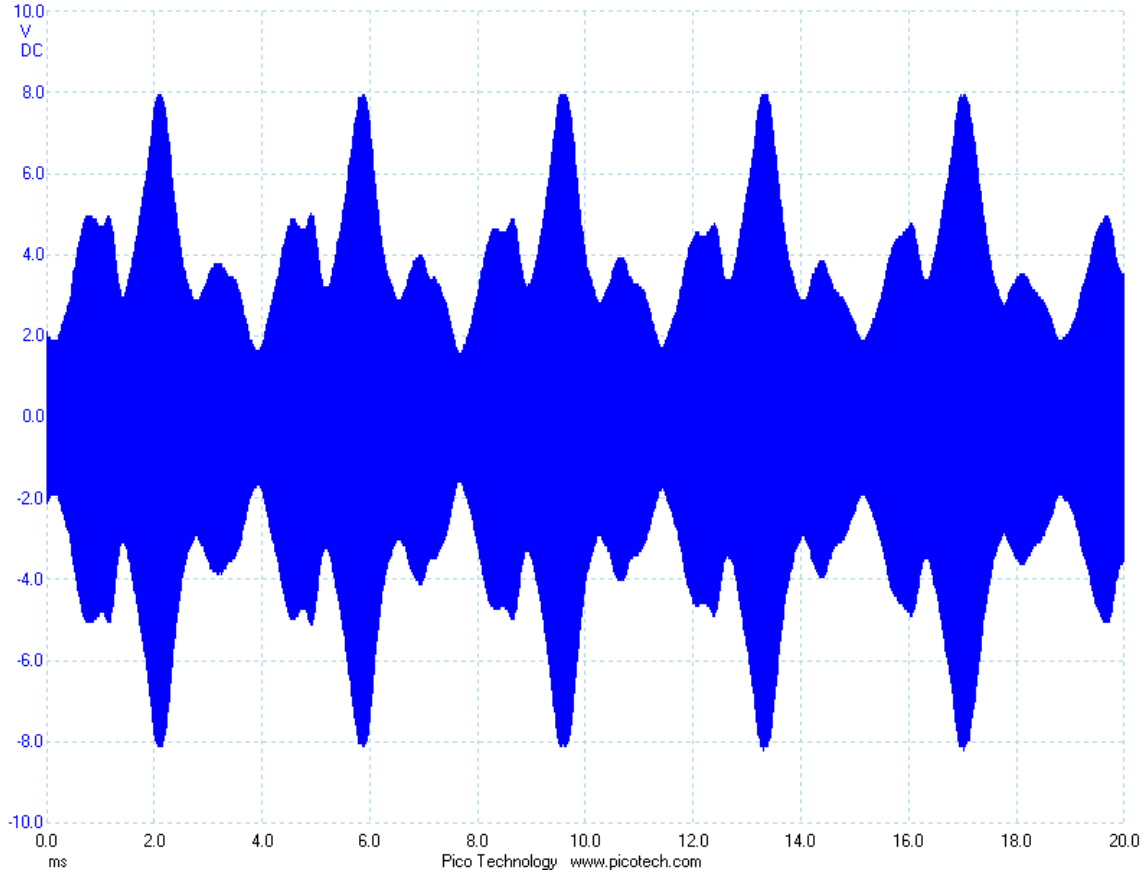

Figure 2-18: PA output signal @ unloaded situation.

Figure 2-19 shows the carrier of Class-D RF signal at different distances. At unloaded position, 8mm, the maximum output voltage is obtained. The minimum output voltage relates to fully loaded situation (0 mm) which is 4 V p-p. As is clear from figure 2-19, at all distances there is some distortion on the carrier signal. This distortion (jump) is because of the RLC series tuned circuit connected to the Class-D amplifier when the coil voltage is being observed.

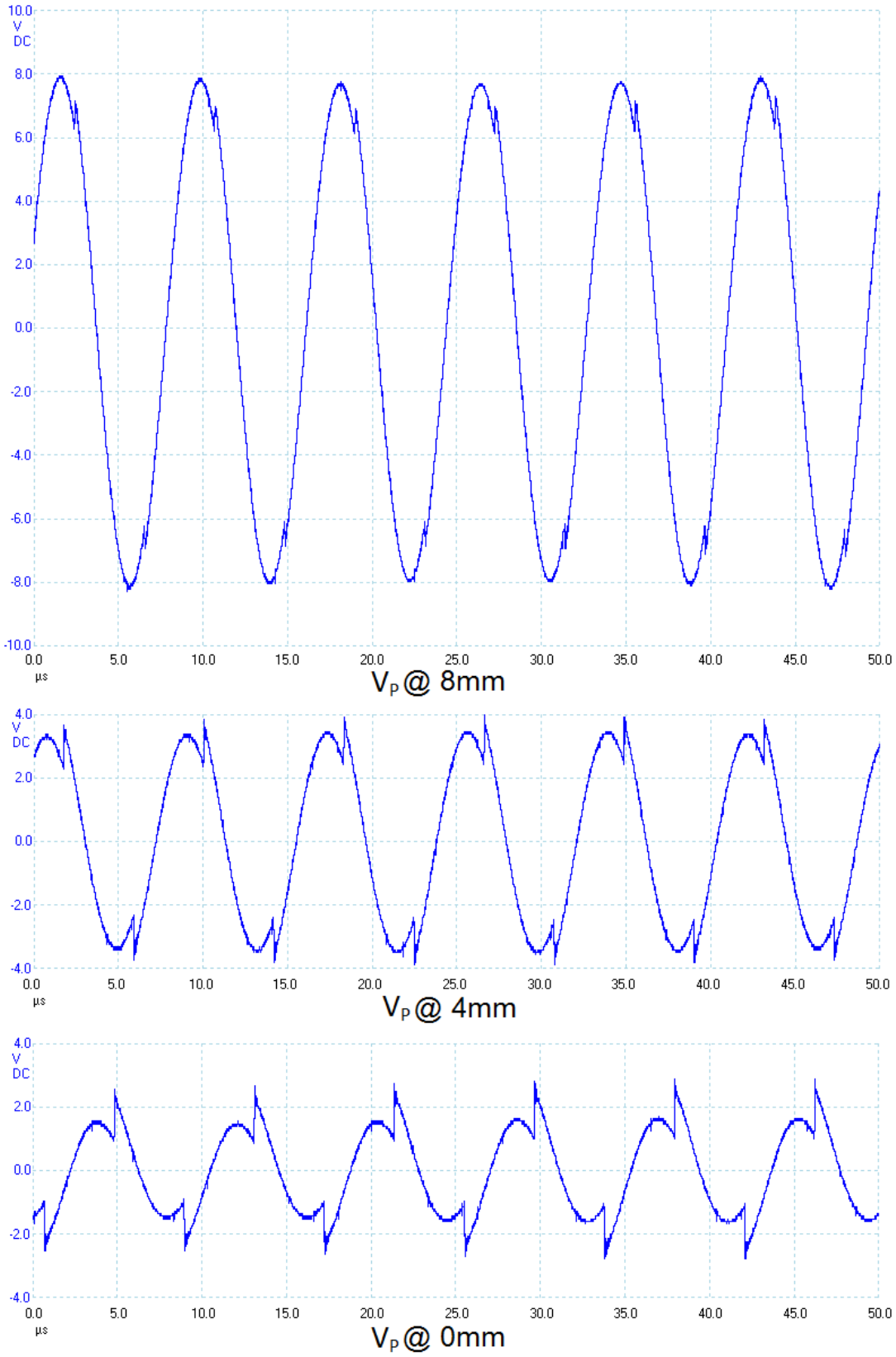

Figure 2-19: Class-D RF output signal at different distances.

Output switch voltage is an important factor in switching type power amplifiers. In ideal case, in 'On' state, there shouldn't be any voltage across the switches. Figure 2-20 shows the voltage of mid-node of Class-D at optimum distance (4 mm). As is clear from figure 2-20, there is some bend on the wave form which is because of transistor linear voltage in 'On' state ($R_{on} \times I_d$). This voltage will reduce efficiency due to transistor power consumption ($R_{on} \times I_d^2$). In contrast, we cannot see the same phenomenon at the lower transistor (M_2), because the source node of M_2 is connected to ground and consequently there is no increasing of the threshold voltage. In the upper transistor, the source is not connected to the ground and the threshold voltage of M_1 increases during 'On' state of M_1. As a result, the lower transistor (M_2) is better switch than the upper one (M_1) because of source-bulk difference voltage across them.

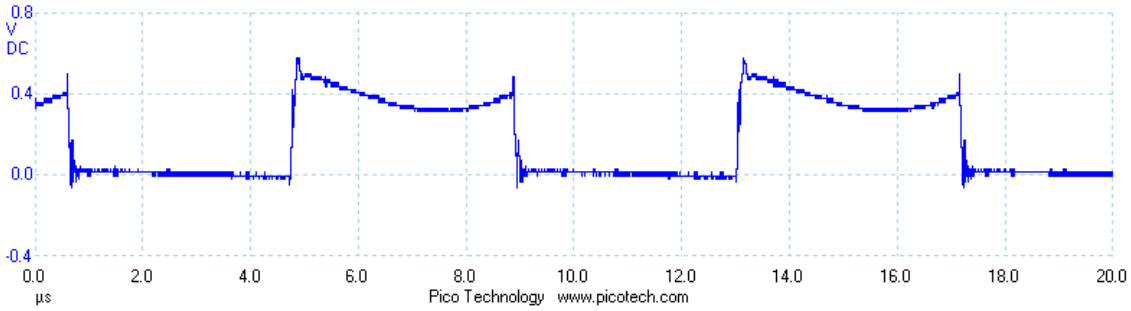

Figure 2-20: Class-D mid-node voltage at 4 mm distance.

Finally, the consuming current by Class-D amplifier and RF link output voltage at different distances are listed in table 2-3.

Distance (mm)	*Current Consumption (mA)*	*RF link output voltage (V)*
0 mm	*3*	*4.5*
4 mm (optimum)	*5*	*7.8*
8 mm (unloaded)	*7*	*16*

Table 2-3: Current consumption and output voltage (p-p) of RF Class-D amplifier at different distances

3. Integrated Circuit Design

3.1. ASIC Architecture and sub-blocks

The main purpose of the prototype design (chapter 2) was identifying the most suitable RF switching power amplifier topology: either the Class-E or the Class-D amplifier. The results (5 mA current consumption in Class-D vs. 15 mA current consumption in Class-E) showed that Class-D would be the best architecture for this project.

A second result of the prototype design was finding out the maximum peak-to-peak output voltage (saturated output). At this voltage, the maximum stimulus can be applied to the transducer. This maximum voltage is the main quality measure in the integrated circuit design.

The result showed the same saturated output voltage for both designs, in the range of 15 V p-p. Figure 3-1 shows the block diagram of integrated circuit (ASIC) designed in this project. The ASIC consists of three main sub-blocks:

- Clock divider & Buffer drivers
- Level shifter & Gate drivers
- Power Amplifier

The main consideration of the design is based on the last block (power amplifier) and all other parts of the circuit are designed in term of last block parameters. As a rule, all integrated circuit designs will be labelled with ASIC for rest of this report.

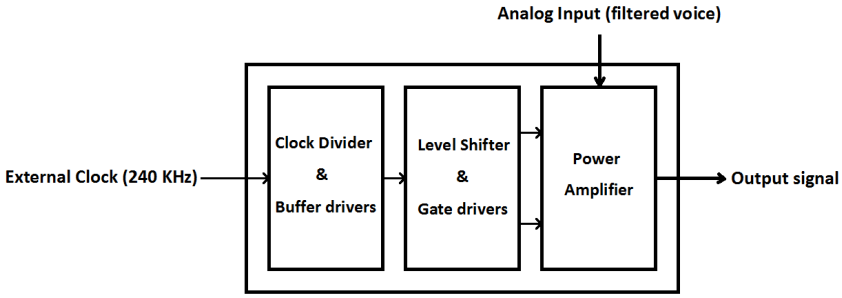

Figure 3-1: Block diagram of ASIC and its sub-blocks.

3.2. ASIC-Power Amplifier

According to chapter 2, the Class-D topology is selected for this project. In design of the Class-D amplifier, three parameters should be determined:

- The size of transistors in the Class-D amplifier
- The type of the Class-D amplifier
- Timing control of the Class-D amplifier

3.2. 1.The size of transistors in the Class-D Amplifier

The first step of integrated circuit design is defining the size of MOS output transistors.

Figure 3-2 shows a typical Class-D amplifier. The important parameter is the maximum current flow through each transistor. Assume that the link (L) is tuned with capacitor C to the desired frequency and that the link is lossless ($R_L \approx 0$) which will yield the maximum current. The maximum output voltage based on previous measurement in discrete circuit design is above 15 V (p-p). By considering 50% pulse width for the clock, we can write:

$$i_L(t) = i_1(t) = i_2(t - T/2) \tag{3.1}$$

$$v_L(t) = v_1(t) = v_2(t - T/2) \tag{3.2}$$

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{3.3}$$

$$i_L(t) = \frac{1}{L}\int v_L \cdot dt \tag{3.4}$$

$$v_L(t) = V_{\max} \cdot \sin(2\pi \cdot f \cdot t) \tag{3.5}$$

We can rewrite:

$$i_L(t) = \frac{1}{2\pi f \cdot L} \cdot V_{\max} \int_0^{T/2} \sin(2\pi \cdot f \cdot t) \cdot dt = \frac{1}{2\pi f \cdot L} \cdot V_{\max} \cdot (1 - \cos(\pi \cdot f \cdot T)) \tag{3.6}$$

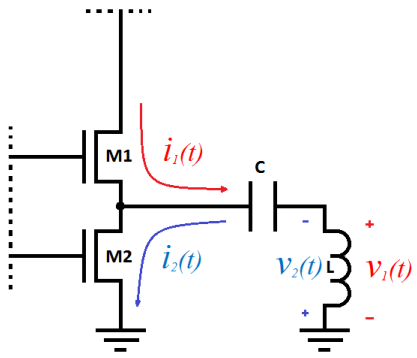

Figure 3-2: Typical Class-D amplifier with tuned RF link.

In Class-D amplifier, both transistors are considered as On/Off switches. Therefore, transistors should be in linear region. For simplicity assume that both transistors are NMOS (in CMOS Class-D amplifier, I_D of PMOS should be scaled up by the ratio of: $\frac{\mu_n}{\mu_p}$)

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_{th}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS}) \tag{3.7}$$

The simplified version of (3.7) is:

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_{th}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{3.8}$$

In 0.35µm standard CMOS technology (AMS c35b4), $\mu_n \cdot C_{ox} = 115 \frac{\mu A}{V^2}$ and $V_{th} \approx 0.48V$.

Since we are calculating the maximum size of transistors, we have to use as small as possible value for $(V_{GS} - V_{th})$; $V_{GS} - V_{th} \approx 1.2V$. Using the minimum value for $(V_{GS} - V_{th})$ also compensates the body effect at the upper transistor of the Class-D amplifier.

As a main concern we have to keep the drain capacitance of the Class-D amplifier as small as possible, otherwise it can influence the tuned RF tank. Based on what mentioned, we have used the smallest possible size for length of transistors ($L = 0.35\mu m$). Based on the maximum output voltage of RF link and above equations: $W_1 = W_2 = 1500\mu m$.

3.2. 2.The type of the Class-D Amplifier

Next step of ASIC-power amplifier is selecting a proper type for Class-D. There are three different types that are commonly used in Class-D amplifiers based on power, frequency and application as: Inverter Class-D, CMOS Class-D and NMOS Class-D (figure 3-3)

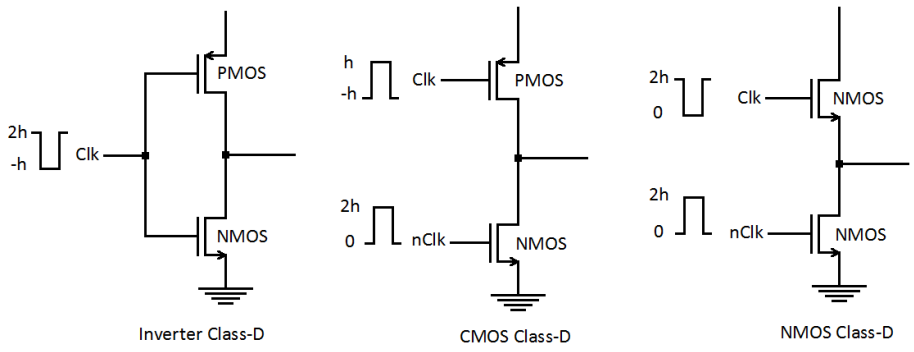

Figure 3-3: Three different types for Class-D amplifier.

In CMOS and Inverter Class-D types, both PMOS and NMOS transistors are used but there is a difference between them according to transistors gate connection. In inverter Class-D, the gates of two PMOS and NMOS are connected together. So for turning On/Off transistors, a negative voltage level for turning on PMOS transistor (-h) and for turning on NMOS transistor a positive voltage level (2h) are required.

In CMOS Class-D, two different clock pulses (Clk & nClk) are used for driving the gates of PMOS and NMOS transistors. For PMOS transistor in CMOS Class-D, the level low (-h) is the critical level to turn On the PMOS, while in NMOS the level high is critical (2h). Since both transistors in NMOS type are the same, we can drive them with the same voltage level (but in complementary phase). If we apply insufficient voltage level (positive or negative) as clock pulse, transistors will not be turned On (Off) completely and there will no longer be in linear region. Figure 3-4 shows a test bench circuit in Cadence-Virtuoso ADE to simulate a CMOS Class-D type.

The size of NMOS transistor is $\frac{W_n}{L_n} = \frac{1000\mu m}{0.35\mu m}$ and for PMOS, $\frac{W_p}{L_p} = \frac{2700\mu m}{0.35\mu m}$.

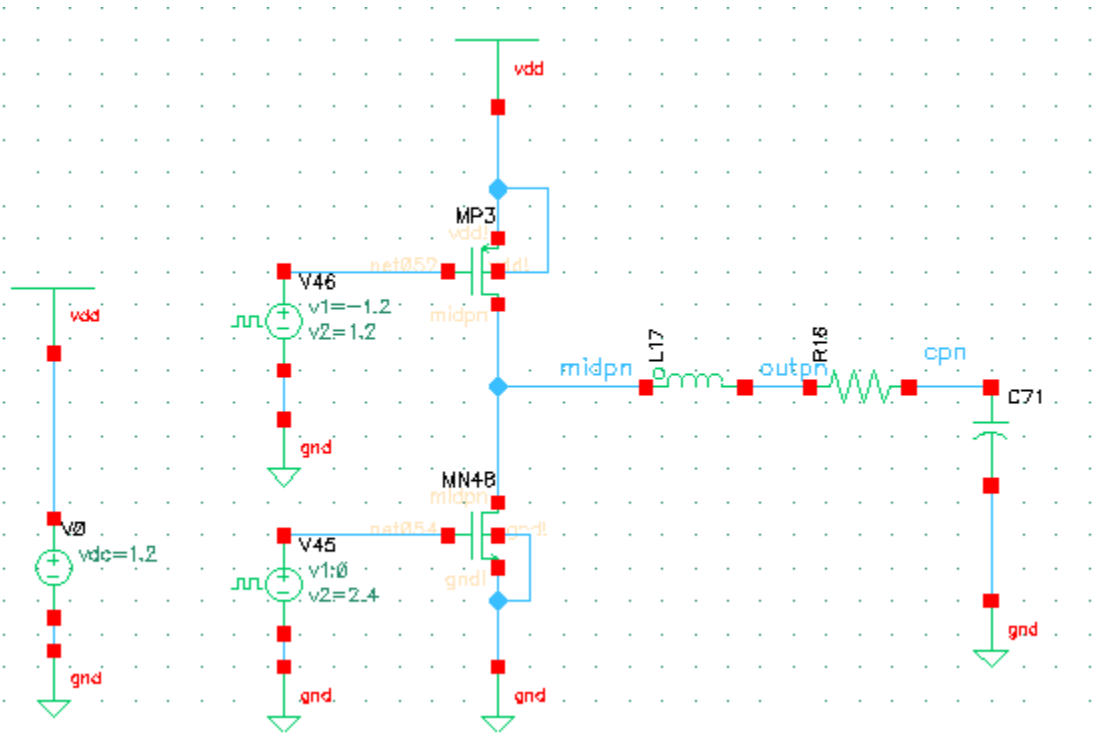

Figure 3-4: Test bench circuit of CMOS Class-D.

At first, a clock pulse between 0V and 2.4V was applied to PMOS transistor and another clock pulse with the same level but in opposite phase was applied to NMOS transistor.

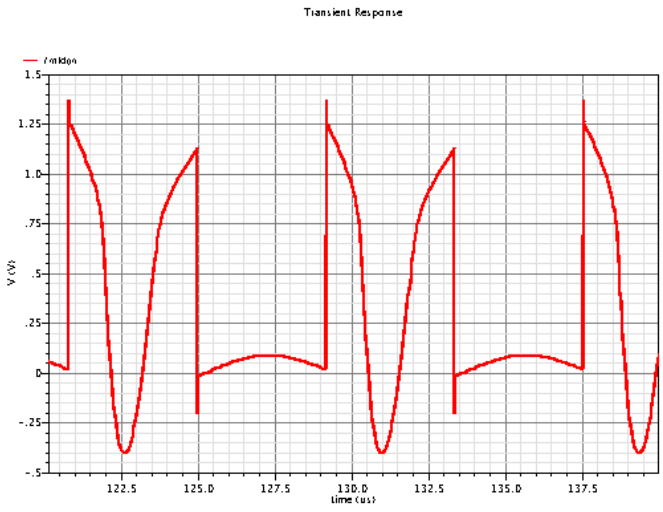

Figure 3-5: The mid-node voltage of CMOS Class-D when improper clock pulse is applied.

The mid-node voltage is shown in figure 3-5. As is clear in figure 3-5, when we apply a pulse voltage which is not sufficient to turn PMOS On properly ($0 < V_{PULSE} < 2.4$ V), we have a quite large resistance in On period. The Class-D amplifier consumes much power in this time. However, when we apply a proper voltage (-1.2 V $< V_{PULSE} < 1.2$ V), we can see the Class-D amplifier works properly (fig.3-6). Note that the pulse that is used to sufficiently turn on the PMOS has a negative voltage level. Generating such voltage needs another gate drive circuit design.

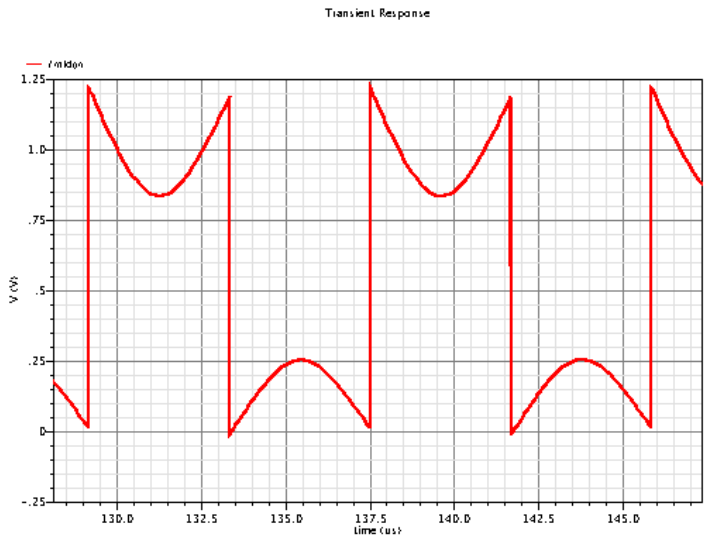

Figure 3-6: The mid-node voltage of CMOS Class-D when proper clock pulse is applied.

Figure 3-7 shows a test bench circuit to compare three different Class-D types. The left one is the Inverter, the middle one is the CMOS and the right one is the NMOS. The size of NMOS transistors for all three types are 1500µm (based on previous calculation) and PMOS transistors in Inverter and CMOS Class-D are scaled up by the factor of $\frac{\mu_n}{\mu_p} \approx 2.7$ (4050 µm =1500 µm×2.7). The applied clock pulse frequency for all of them is 120 kHz. The clock pulse for Inverter is between −1.8 V ~ 3.6 V; for PMOS transistor in CMOS Class-D, the clock pulse is between −1.8 V~1.8 V and for NMOS is 0 V ~ 3.6 V; for both transistors in NMOS Class-D, the clock pulse is between 0 V ~ 3.6 V.

The mid-node (the node between two transistors in each type) for all three types are shown in figure 3-8.

As is clear from figure 3-8, when PMOS transistors (in inverter and CMOS topologies) are On, more voltage drops across them in compare with NMOS transistor and more dropped voltage across transistors means more power consumption in the Class-D amplifier. Figure 3-9 shows the output voltage of three types. Since in inverter and CMOS class-D the current that can be delivered to the load is slightly smaller than NMOS Class-D, the output voltage amplitude of NMOS Class-D is slightly larger than two other types.

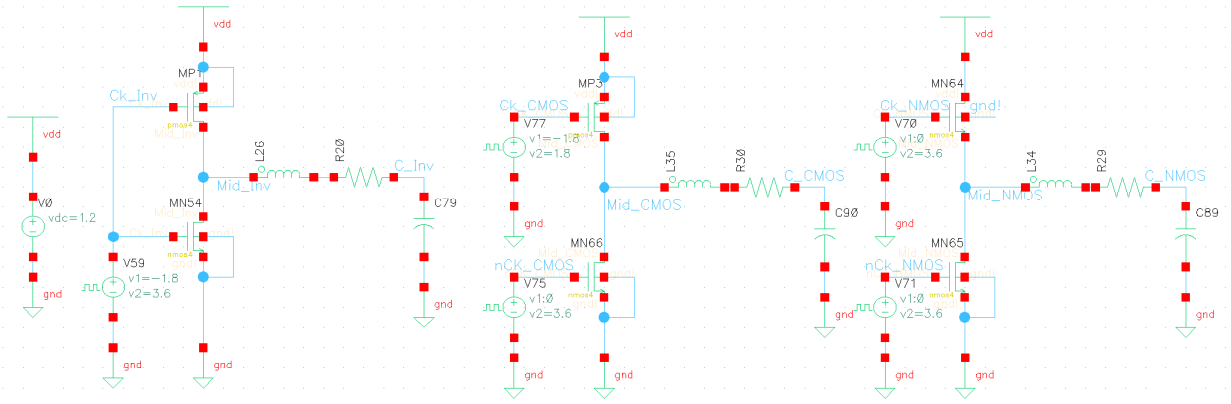

Figure 3-7: Test bench circuit to compare 3 different Class-D amplifiers.

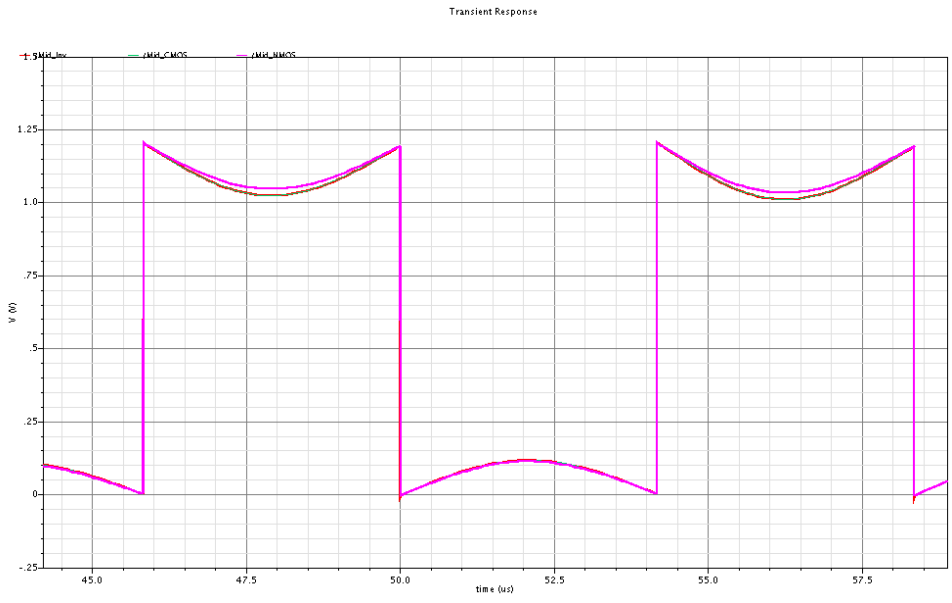

Figure 3-8: Mid-node voltage of three types (Inverter: red, CMOS: green and NMOS: pink).

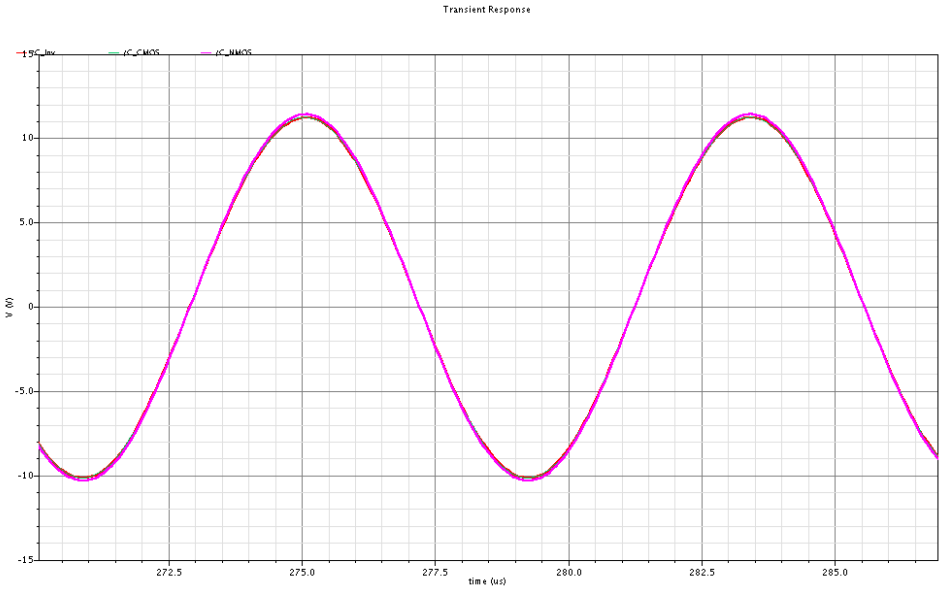

Figure 3-9: Output voltage of three types (Inverter: red, CMOS: green and NMOS: pink).

Another parameter that should be compared is output internal dominant capacitors in each type. Figure 3-10 shows the schematic of CMOS and NMOS Class-D output stages with their respective capacitances (Inverter topology has the same output capacitance as CMOS type). It should be mentioned that this comparison of output internal capacitors is just another factor to help finding out the best type. Instead of precise calculation, here the rough estimation was made to compare all Class-D types. Thus, I neglected C_{GD} capacitors which are much smaller than C_{GS}, C_{DB} and C_{SB} in each type.

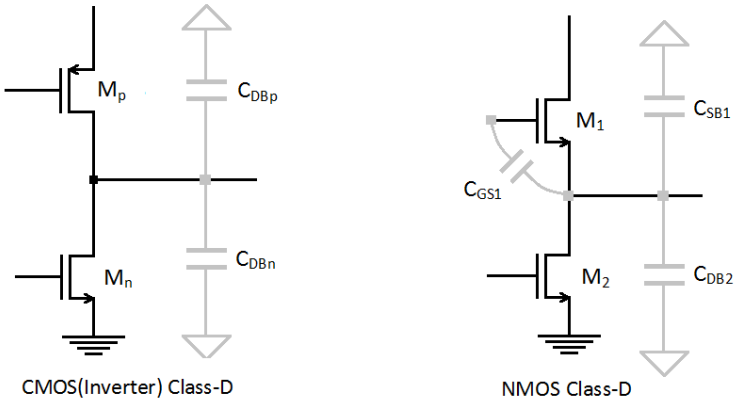

Figure 3-10: Output internal dominant Capacitors in three types. CMOS (Inverter) type in the left hand and NMOS type in the right hand.

According to [13]:

$$C_{GS} = \frac{2}{3} \cdot C_{ox} \cdot W \cdot L + C_{gd0} \cdot W \tag{3.9}$$

$$C_{XB} = \frac{C_j \cdot A_X}{(1 - \frac{V_{BX}}{V_j})^{m_j}} + \frac{C_{jp} \cdot P_X}{(1 - \frac{V_{BX}}{V_{sw}})^{m_{sw}}} \tag{3.10}$$

Which in (3.10): X is Source or Drain of transistors, A_x is Source/Drain area, P_x is Source/Drain perimeter and V_{BX} is potential from bulk to Source/Drain. According to AMS c35b4 CMOS process (Appendix A):

$$C_{ox} = 4.6 \frac{fF}{\mu m^2}, C_{jn} = 0.93 \frac{fF}{\mu m^2}, C_{jnp} = 0.28 \frac{fF}{\mu m^2}, C_{jp} = 1.42 \frac{fF}{\mu m^2},$$

$$C_{jpp} = 0.38 \frac{fF}{\mu m^2}, C_{gd0} = 0.21 \frac{fF}{\mu m}, V_{jn} = V_{swn} = 0.69V, V_{jp} = V_{swp} = 1.02V,$$

$$m_{jn} = 0.31, m_{jp} = 0.55, m_{swn} = 0.19, m_{swp} = 0.39$$

Also based on what I calculated for the size of PMOS and NMOS transistors and Geometric Design Rule for 0.35µm CMOS technology (Appendix B), the area of Source/Drain transistors are:

Minimum diffusion length in 0.35µm CMOS technology, $E = 0.85\mu m$

Assume that the lengths of P and N diffusion are the same.

$A_{Dn} = A_{Sn} = W_n \times E = 1500 \times 0.85 = 1275 \mu m^2$

$P_{Dn} = P_{Sn} = 2 \times (W_n + E) = 3001.7 \mu m^2$

$A_{Dp} = W_p \times E = 4050 \times 0.85 = 3442.5 \mu m^2$

$P_{Dp} = 2 \times (W_p + E) = 8101.7 \mu m^2$

$V_{BDn} = V_{BSn} = -V_{BDp} \approx -0.6V$

$C_{GSn1} = \frac{2}{3} \times 4.6 \times 1500 \times 0.35 + 0.21 \times 1500 = 1925 fF$

$$C_{DBn} = C_{DBn2} = C_{SBn1} = \frac{0.93 \times 1275}{(1+\frac{0.6}{0.69})^{0.31}} + \frac{0.28 \times 3001.7}{(1+\frac{0.6}{0.69})^{0.19}} = 1723 fF$$

$$C_{DBp} = \frac{1.42 \times 3442.5}{(1-\frac{0.6}{1.02})^{0.55}} + \frac{0.38 \times 8101.7}{(1+\frac{0.6}{1.02})^{0.39}} = 12315 fF$$

$$C_{CMOS} \approx C_{DBp} + C_{DBn} = 12315 + 1723 \approx 14 pF$$

$$C_{NMOS} \approx C_{DBn2} + C_{SBn1} + C_{GSn1} = 1723 + 1723 + 1925 \approx 0.5 pF$$

Based on above calculation, we can see the output capacitor in CMOS and Inverter types are roughly 28 times greater than output capacitor in NMOS Class-D type. In practice the difference of the output capacitor between CMOS (Inverter) and NMOS types are bigger, because in NMOS Class-D amplifier (figure 3-10) the source of upper transistor can be merged with the drain of the lower transistor.

The summary of comparison of the types is listed below.

- For PMOS transistor in CMOS/Inverter types, negative voltage level is needed.
- Although PMOS transistor is scaled up, but it has slightly bigger resistance in comparison with NMOS transistor, which leads to more power consumption.
- Since PMOS transistor should be scaled up, the occupied area in CMOS and Inverter types is roughly 2 times bigger than in the NMOS type.
- The output capacitance in CMOS/Inverter is roughly 28 times bigger than NMOS type which may influence the tuned RF link frequency and reduce its quality factor.

Based on above considerations, NMOS Class-D amplifier was selected for this project.

3.2.3. Timing control of the Class-D Amplifier

Another important parameter that should be considered in switching amplifiers is the timing of clock pulses which drive the gates of transistors. The performance and power transmission of Class-D amplifier are dependent on overlapped or non-overlapped of clock pulse(s). Although it

seems that the best performance should be when non-overlapped clock pulses are used, in this project after simulation in Cadence-Virtuoso-ADE, we have come to a different conclusion.

To find the best timing of clock pulse, we applied 3 different pulse-width with the same frequency (120 kHz) and with the same rise/fall time (10 ns) to the Class-D amplifier (figure 3-11); pulse-width of 4.1566 µs relates to two clock pulses that exactly have the same On and Off pulse-widths and cross each other in the mid-level of rise(fall) time; pulse-width of 4.1466 µs relates to two clock pulses that don't cross each other, but there is no delay between start (stop) of one to stop (start) of another clock pulse; pulse-width of 4.1366 µs relates to two clock pulses that don't cross each other, and there is a delay of 10ns between start (stop) of one to stop (start) of another clock pulse.

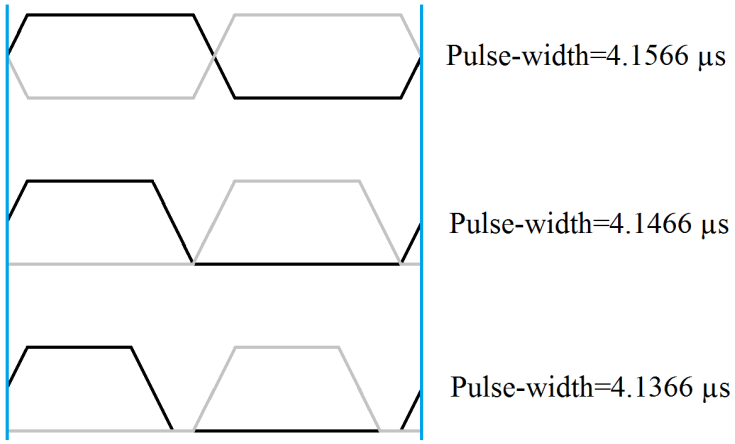

Figure 3-11: Three different sets of clock pulses which were applied to Class-D amplifier.

The current waveforms of three different duty cycle states are shown in figure 3-12 and figure 3-13. What is traditionally mentioned as the best-applied clock pulse is based on Drain current of MOS transistors in Class-D. As is clear from figure 3-13, when we apply overlapped clock pulses (pulse-width=4.1566 µs), some spikes will be appeared on the current curve. It means in switching period, both transistors in Class-D are On for a short time and this phenomenon influence the performance of Class-D. However, it not the full story, because in this project besides performance of Class-D, the output voltage waveform is important too.

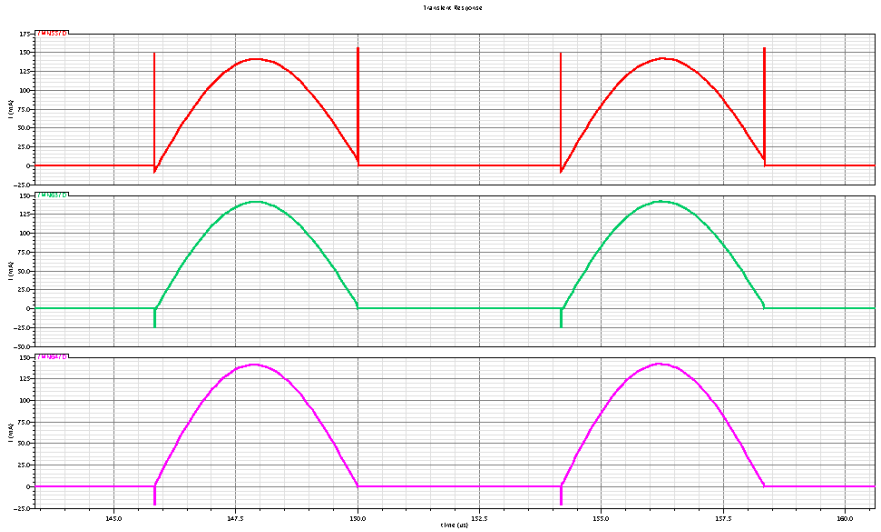

Figure 3-12: Drain Current waveforms of NMOS transistors in Class-D amplifier(NMOS Class-D type in figure 3-10) with three different pulse-widths (Red: 4.1566 µs, Green: 4.1466 µs, Pink: 4.1366 µs).

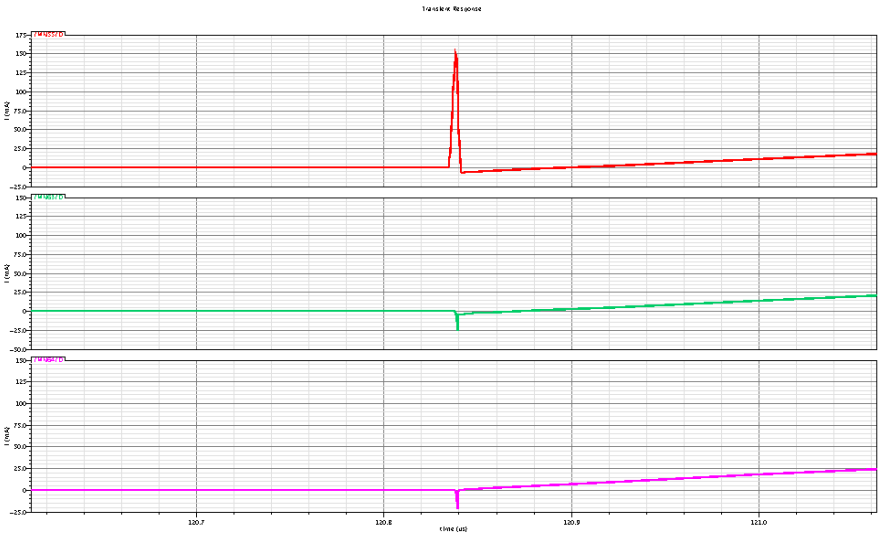

Figure 3-13: Zoomed version of figure 3-12

The mid-node voltages of three different duty cycle states are shown in figure 3-14 and 3-15. The curve which is related to overlapped clock pulse (pulse-width=4.1566 µs) does not have any spikes, but the two other curves (non-overlapped clock pulse) have spikes that will be copied on output voltage (figure 3-16). As was discussed in previous paragraph, the shape of output voltage is very important in this design, because the envelope will be used in voice detecting application and any spikes on the output will be suffering for patients.

If we multiply the current for each pulse-width set to its related mid-node voltage and take the RMS in a period, the power consumption of each state will be defined. Thanks to calculator toolbar in Cadence-Virtuoso-ADE, following results were obtained:

- Power Consumption for each transistor in 4.1566 µs clock pulse-width=63.32µW
- Power Consumption for each transistor in 4.1466 µs clock pulse-width =63.3µW
- Power Consumption for each transistor in 4.1366 µs clock pulse-width =63.33µW

According to the results above, when we use non-overlapped clock pulses (pulse-width=4.1466 µs) the less power consumption will be obtained, but on the other hand there will be big spikes on the output waveform which is crucial problem for this application. As a trade off between power consumption and shape of output voltage, it seems that overlapped clock pulses (pulse-width=4.1566 µs) will be the best candidate in this project.

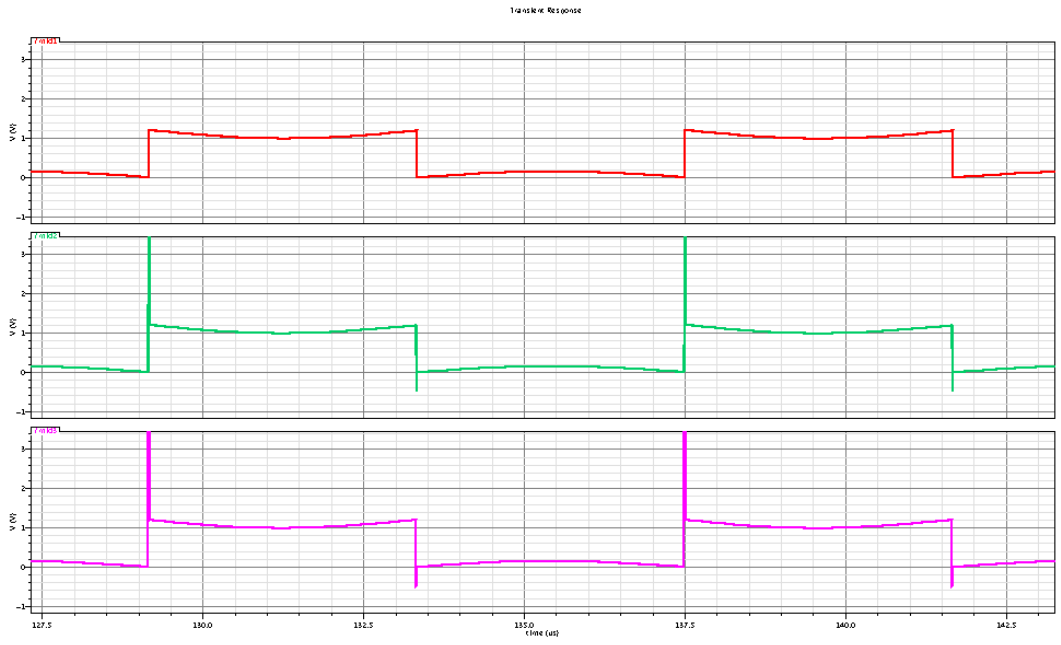

Figure 3-14: Mid-node voltages of three different pulse-widths (Red: 4.1566 µs, Green: 4.1466 µs, Pink: 4.1366 µs).

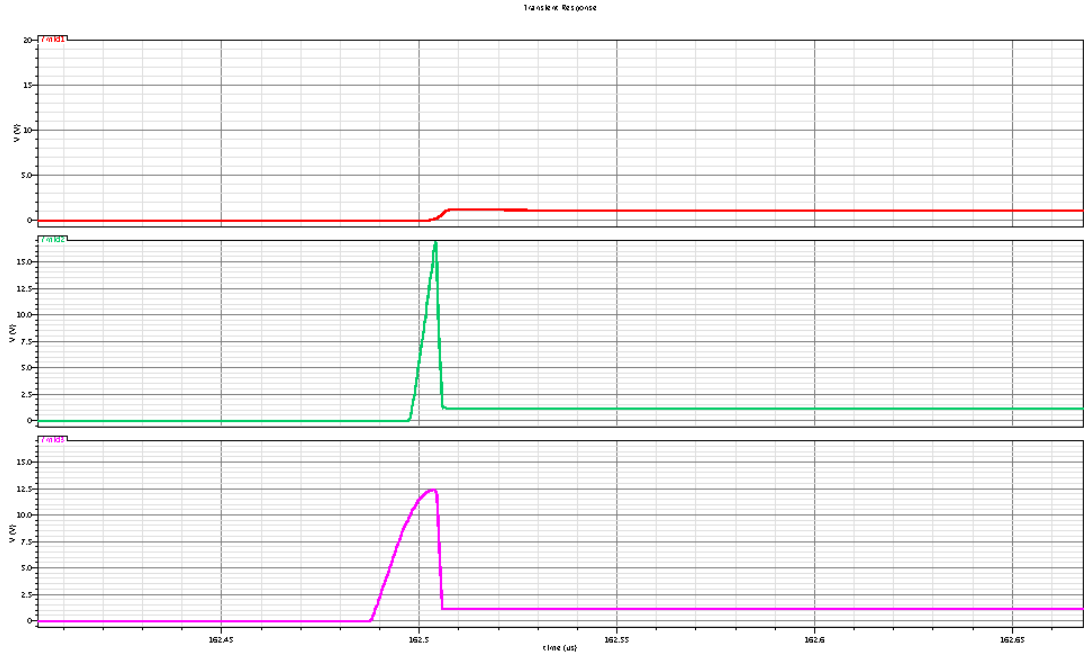

Figure 3-15: Zoomed version of figure 3-14

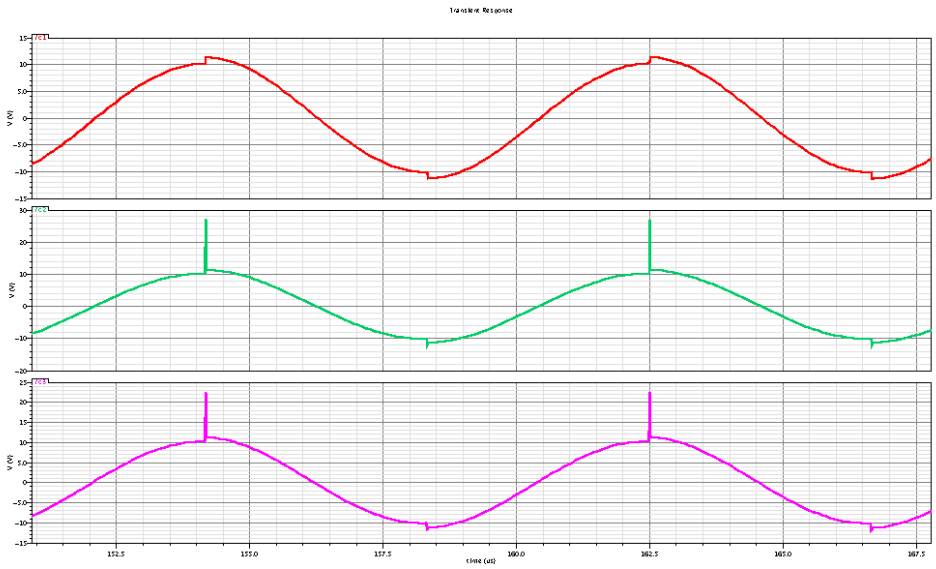

Figure 3-16: Output voltages of three different pulse-widths (Red: 4.1566 µs, Green: 4.1466 µs, Pink: 4.1366 µs).

3.3. ASIC-Level Shifter & Gate Drives

The 1.2 V battery that is the voltage supply of this project is not high enough to drive the gate of transistors in Class-D amplifier. Figure 3-17 shows the related voltages of transistors in Class-D amplifier. The minimum requirement voltages to turn transistors On/Off are defined as below.

In linear region for NMOS transistor:

$$V_{GT} = V_{gs} - V_{th} \geq 0 \tag{3.11}$$

$$\left.\begin{aligned} &V_{GT1} = V_{G1} - V_{th} - V_{Mid-Node} \\ &V_{th} \approx 0.5V \\ &V_{Mid-Node}(\max) \approx 1.2V \end{aligned}\right\} \rightarrow V_{G1} \geq 1.7V \tag{3.12}$$

According to simulation, 1.7 V is not enough to guarantee complete switching in Class-D and at least 2 V is needed to be sure that the circuit works properly. In the other hand if we design based on minimum gate voltage, the Class-D amplifier will not be so efficient because the output conductance of transistors is in the minimum value according to (3.13). In other words, the output resistor is in maximum value which degrades the performance of Class-D due to power consumption.

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th} - V_{DS}) \tag{3.13}$$

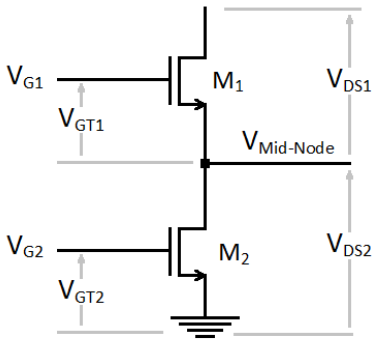

Figure 3-17: The related voltages of transistors in Class-D amplifier.

Figure 3-18 shows the simulation result of two different cases: when we apply 2 V clock pulses to the gates and when we apply 3.6 V to them. It clearly shows when we apply the minimum voltage level (2 V) to the gates-due to power consumption in transistors- less output voltage can be delivered (13.88V @ 2 V clock pulse versus 21.26 V @ 3.6 V clock pulse).

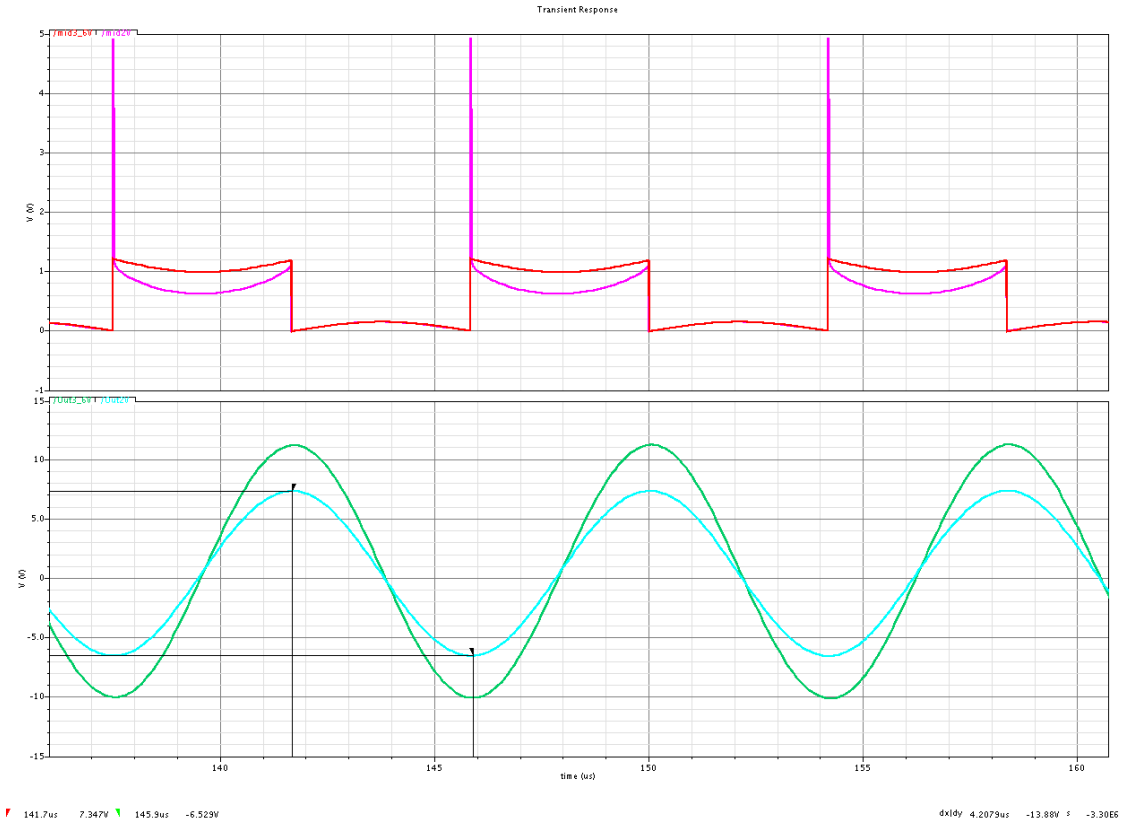

Figure 3-18: The simulation result of two different clock pulse levels. The upper curves relate to mid-node of Class-D when we apply 0 ~ 2 V (the pink one) versus 0 ~ 3.6 V clock pulse (the red one). The lower curves relate to output voltage of Class-D when we apply 0 ~2 V (the blue one) versus 0 ~ 3.6 V clock pulse (the green one).

We decided to use the 3.6 V as a high level of clock pulses. To produce this voltage level from 1.2 V, different circuits were studied and simulated in Cadence-Virtuoso-ADE; some of them will be presented next.

3.3.1.Supply and clock booster circuit

The first considered charge pump circuit has been designed by Ay [14]. It is a supply and clock booster circuit. The circuit consists of two inverters, a booster capacitor (C) and three transistors (figure 3-19). The bulk of M2 and M3 are connected to V_b for improving efficiency of boosting. When the CLK is low, the capacitor C is charged from M3 and M4 to V_{dd}. When the CLK goes high, the previous charge of the Capacitor is added to V_b.

Ideally this circuit can produce $2V_{dd}$ at V_b and consequently double the high level of CLK to $2V_{dd}$, but when a load Capacitor (C_L) is connected to V_b the boosted supply voltage becomes:

$$V_b = V_{dd} + \frac{C}{C + C_L} \cdot V_{dd} \tag{3.14}$$

This circuit is suitable for memories that don't consume so much current, but in this project it does not work properly due to big transistors in Class-D amplifier. In addition, to get 3.6 V, we have to cascade this circuit which degrades the boosting efficiency because it is very sensitive to increasing the load capacitance in node V_b.

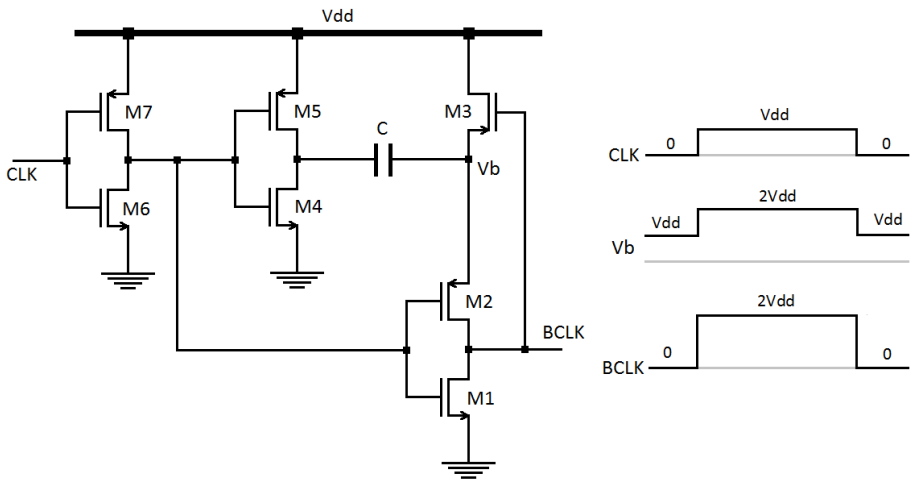

Figure 3-19: Supply and clock booster [14] and its ideal waveforms.

3.3.2. The Dickson charge pump circuit

The Dickson charge pump is the most well known circuit for generating higher voltages [15].A schematic diagram of a 4-stage Dickson charge pump is shown in figure 3-20. The Dickson charge pump consists of capacitor stages connected by diodes and driven in parallel by two anti-phase clocks. When implementing the circuit in standard CMOS technology, NMOS transistors are used as diode connections. The charges are delivered from one stage to the next through the NMOS transistors and consequently higher DC voltage at the output will be produced. If we disregard the threshold drops, the value of increasing voltage at each node can be presented as:

$$\Delta V = V_{dd} \cdot \frac{C}{C + C_S} - \frac{I_O}{f \cdot (C + C_S)} \tag{3.15}$$

Where C is the pumping capacitor in each stage, C_S is the stray capacitance at each node, I_O is the output current and f is the frequency of the clocks. If C_S is much smaller than C and also I_O is small enough, then $\Delta V \approx V_{dd}$. At each node, the Dickson charge pump can add V_{dd} to previous voltage value. Since NMOS transistors are connected as diode-connection, the voltage equal to V_{th} drops across each transistor when it is On. Therefore, the output voltage of Dickson charge pump is reduced to:

$$V_{out} = \sum_{N} (V_{dd} - V_{th}(N)) \tag{3.16}$$

Where $V_{th}(N)$ is the threshold voltage of N_{th} stage. In single n-well standard CMOS technology, the bulk of NMOS transistors is connected to ground. The voltage at later stages (V_3, V_4) of the charge pump is higher and consequently the difference between source and bulk nodes is higher. Therefore, the body effect causes higher V_{th} in later stages. Thus, the performance of the charge pump is degraded when the numbers of stages are increased.

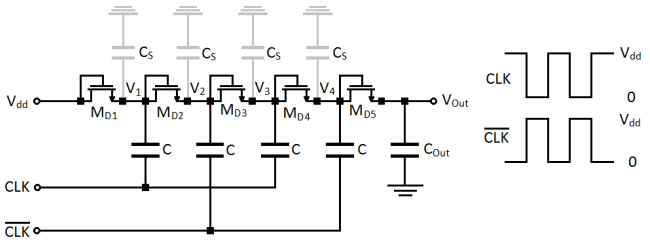

Figure 3-20: 4-stage Dickson charge pump circuit.

3.3.3. NCP-2 charge pump circuit

To solve the problems in Dickson charge pump, different approaches have been used. For example, Wu[16] designed the NCP-2 charge pump circuit to compensate for the V_{th} drop in each stage. The circuit uses dynamic charge transfer switches (CTS) (figure 3-21). CTS's are NMOS transistors (M_S's) in parallel with diode-connected transistors. Each CTS is controlled by the pass transistors M_N's and M_P's. The aim of using CTS is to transfer charges from one stage to the next without any V_{th} drop across diode-connected transistors. The idea is implemented by controlling the CTS in each stage by higher voltage from next stage.

When CLK is low, the voltage at node 1 is V_{dd} and the voltage at node 2 is $3\times V_{dd}$ ($V_{dd}+V_{C1}+V_{C2}$). The transistor $M_{N1}$is turned off because $V_{gs}=V_1- V_{dd}=0$, while M_{P1} is turned on. Therefore, M_{S1} is turned on completely and transfers charge from V_{dd} to node 1. When CLK is high, M_{P1} is turned off and M_{N1} is turned on and consequently makes M_{S1} to be turned off completely. The rest of the circuit works similar to the first stage.

Although NCP-2 charge pump can solve the problem of Dickson charge pump, it is quite complicated and some other methods with less complexity should be considered.

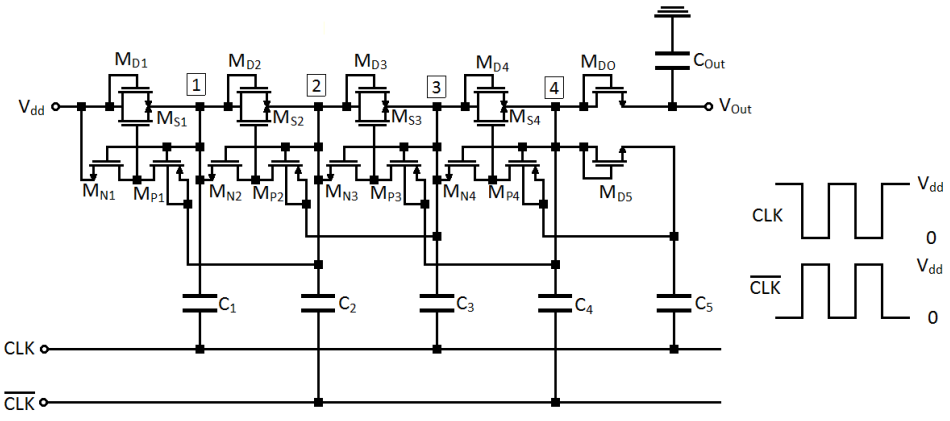

Figure 3-21: 4-stage NCP-2 charge pump circuit.

3.3.4. Cross-coupled charge pump circuit

A more simple solution for Dickson charge pump was designed by Nakagome[17]. The circuit is based on two cross-coupled NMOS transistors (figure 3-22). The voltage drop of the cross-coupled charge pump is equal to the source-drain voltage which is in the range of 100 mV, while the voltage drop in Dickson charge pump in each stage is equal to V_{th} of that stage. Another benefit of cross-coupled charge pump is its automatically reverse bias of the junctions [18].

Usually, the bulk nodes of NMOS transistors are connected to ground, but in some designs they are connected to V_{dd} [19]. Connecting the bulk nodes of NMOS transistors to V_{dd} is not feasible in single n-well standard CMOS technology and at least double n-well is needed.

The problem in cross-coupled charge pump is that to obtain a double DC voltage, serial switch at the outputs are necessary. The only way to make this DC doubled voltage is using PMOS transistors to avoid the voltage V_{th} [19] (figure 3-23). Using PMOS transistors at the output is not for free and it has its disadvantage due to reverse bias junction. To overcome the reverse bias junction problem, C_{OUT} must be a big capacitor.

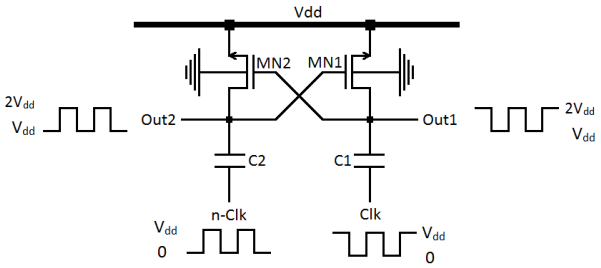

Figure 3-22: Cross coupled charge pump circuit.

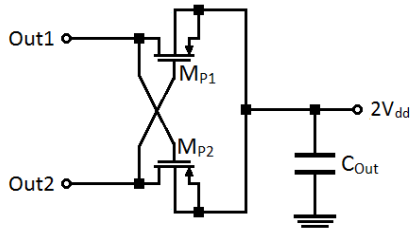

Figure 3-23: Serial PMOS switches with the outputs of cross-coupled charge.

3.3.5.The proposed voltage tripler circuit

To produce 3.6 V from 1.2 V, a voltage tripler circuit based on cross-coupled charge pump has been designed (figure 3-24). The proposed voltage tripler consists of two stages cross-coupled charge pump and one stage clock boosting.

M_{N1}, M_{N2}, C_1 and C_2 make the first cross-coupled charge pump to shift up Clk and n-Clk by V_{dd}. So V_1 and V_2 are between V_{dd}~$2V_{dd}$ now. The combination of M_{N3}, M_{N4}, C_3 and C_4 makes the second cross-coupled charge pump, but instead of applying Clk and n-Clk directly, boosted clock signals are applied to second cross-coupled charge pump. M_{P1} and M_{N5} make an inverter that by applying n-Clk to that, thanks to boosted V_1, BClk can be produced which is between 0~$2V_{dd}$.

Since n-Clk and V_1 are anti-phase, there is no need to make a doubled DC voltage for clock boosting, because when n-Clk is low, V_1 is high ($2V_{dd}$), M_{N5} is turned off, M_{P1} is turned on and $2V_{dd}$ will be appeared at the BClk node. When n-Clk is high (V_{dd}), V_1 is low (V_{dd}), M_{N5} is turned on, $M_{P1}$is turned off and consequently BClk node becomes low (0 V). The function for boosting n-Clk is the same but in different clock cycle. Thanks to boosted clock signals (BClk and n-BClk), V_3 and V_4 at the outputs of second cross-coupled charge pump are between V_{dd}~$3V_{dd}$, so by placing two inverters at the outputs, we can get the pulses between 0~ 3.6 V at Out_1 and Out_2. The bulk nodes of all NMOS transistors are connected to ground, while the bulk nodes of PMOS transistors are connected to their source terminal.It should be mentioned that all are off-chip. The circuit was simulated in Cadence-Virtuoso-ADE and the result was shown in figure 3-25.

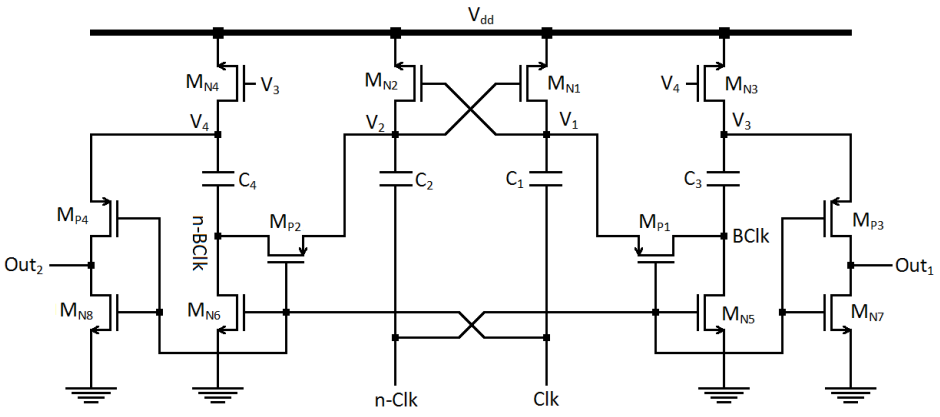

Figure 3-24: The proposed voltage tripler.

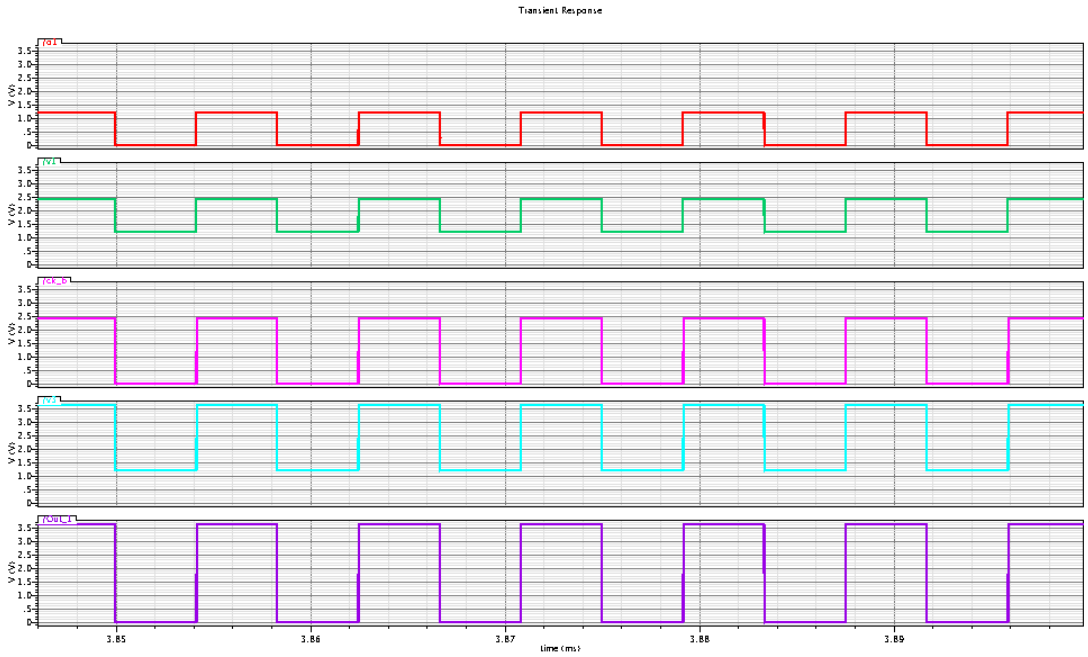

Figure 3-25: Simulation result of the proposed voltage tripler. (Red: Clock signal 0 ~ 1.2 V, Green: V_1 1.2 V ~ 2.4 V, Pink: Boosted Clock 0 ~ 2.4 V, Blue: V_3 1.2 V ~ 3.59 V, Violet: Output 0 ~ 3.59 V)

Although the proposed voltage tripler does not need doubled DC voltage, but due to ESD (electrostatic discharge) protection which should be done in pad connection to the layout, a DC voltage in the range of 3.6 V has been produced (figure 3-26). The output voltage is shown in figure 3-27 and figure 3-28 shows the ripple of this produced DC voltage. The ripple of DC voltage is 47 μV which is acceptable, because we just use this DC voltage for ESD protection.

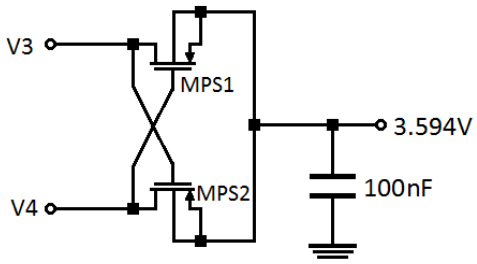

Figure 3-26: The circuit to make 3.6V DC voltage for ESD protection.

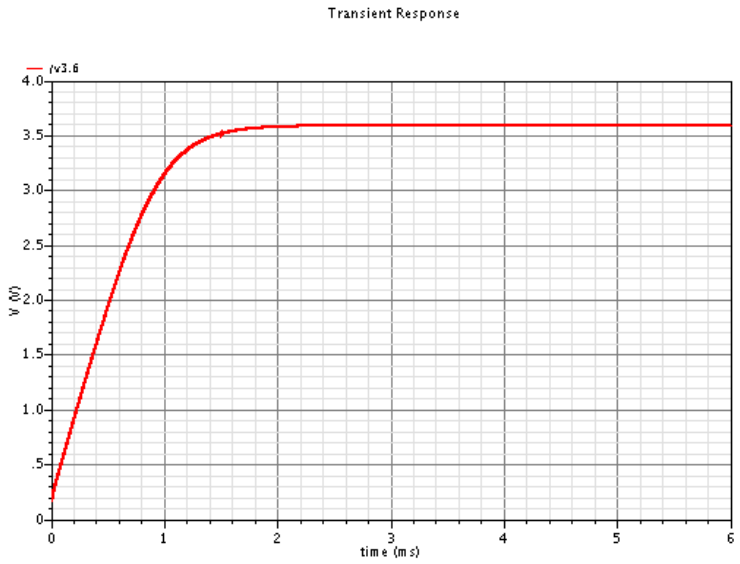

Figure 3-27: Output DC voltage for ESD protection (2 ms is settling time).

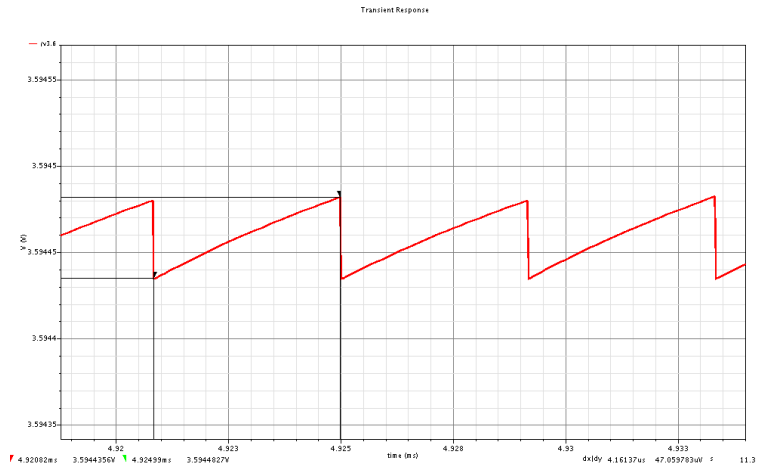

Figure 3-28: The ripple of output DC voltage for ESD protection (47 µV).

3.4. ASIC-Clock divider & Buffer Drives

Two sub blocks have been designed in this part: one for dividing external clock frequency and other for making two simultaneously anti-phase signals from divided clock pulse.

3.4.1 ASIC-Clock divider

In this project an external crystal with standard 240 kHz frequency has been used. To convert this signal to 120 kHz, a divider circuit is necessary. The usual way to divide clock frequency is using D flip-flop and make feedback from negative output to its input (figure 3-29). There are different ways to implement D flip-flop in CMOS technology. A wisely designed circuit which is dynamic logic is TSCP (true single clock phase). This circuit proposed by Yuan[20] and became popular in integrated circuits due to its simplicity and its low of transistor count compared with static D flip-flop (10 transistors in TSCP vs. 16 transistors in a typical CMOS D flip-flop [20]).

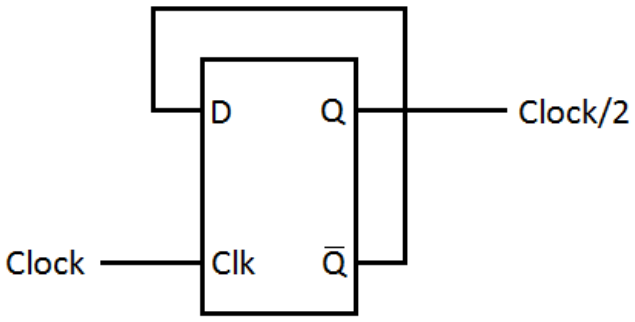

Figure 3-29: Using D-Flip-flop as a traditional way of clock division.

The designed TSCP divider is shown in figure 3-30. The circuit has an input inverter as a buffer of external clock and has three stages. The circuit works as an edge triggered D flip-flop. The bulk nodes of all PMOS transistors are connected to V_{dd}, while in NMOS transistors they are connected to ground. At the output of TSCP two stages of inverter are used to drive next block (ASIC-Buffer Drivers).

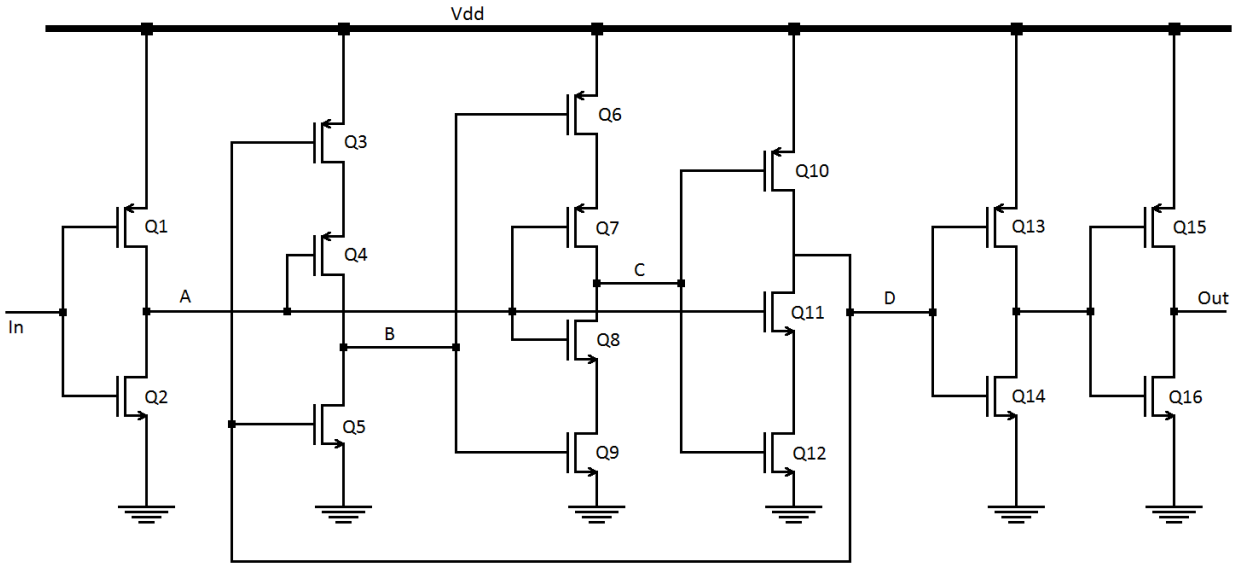

Figure 3-30: TSCP (true single clock phase) divider with buffered input.

Figure 3-31 shows the voltage wave forms of TSCP divider. The node A acts as an enable signal for three stages, when is goes from high to low, stage one (Q4) and half upper side (Q7) of stage two are enabled. When node A goes from low to high, the lower part (Q8) of stage two and the last stage (Q11) are enabled. When A is low or high, no change happens at the output [20].

At node A transition high to low, if current state of node D is low, node B becomes high and if current state of node D is high, then node B becomes low and node C becomes high (low state of node D propagates in stage one, while high state of node D propagates in stage one and upper half of stage two).

At node A transition low to high, when current state of node D is low, node B propagates to node C and node C propagates to node D. When current state of node D is high, only node C propagates to node D.

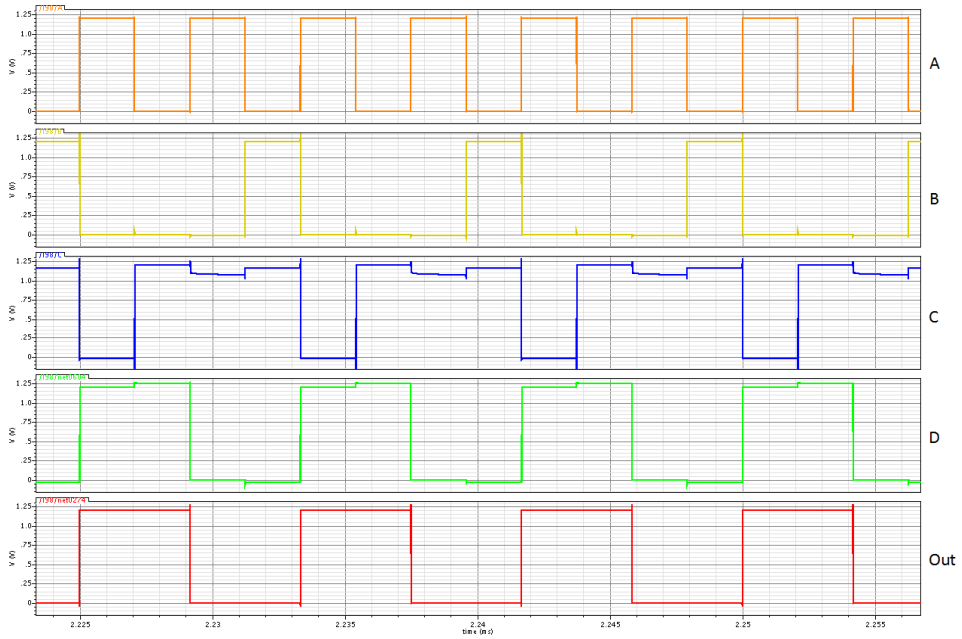

Figure 3-31: Waveforms of TSCP circuit.

3.4.2 ASIC-Buffer drivers

As was mentioned previously, two anti-phase clock signals are needed for applying to gates of Class-D amplifier (after boosting). To produce these signals from 120 kHz (that is already made from external 240 kHz by TSCP divider), we have to build two separate paths with the same delay (figure 3-32).

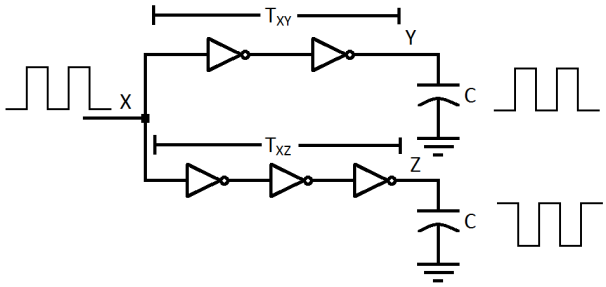

Figure 3-32: Two separate paths with the same delay (T_{XY}= T_{XZ}).

Figure 3-33 shows a simple model of a CMOS inverter [21]. Based on V_{in}, output is connected to V_{dd} or ground via R_G, R_G is resistor of MOS transistors (assume that we sized the transistor which R_N= R_P= R_G). If this inverter drives another inverter, propagation delay will be [21]:

$$t_d = 0.7R_G(C_P + C_L) \tag{3.17}$$

Where C_L is the gate capacitance of next inverter. We can rewrite (3.17) as below:

$$t_d = \tau_{inv}.(p + h) \tag{3.18}$$

Where, $\tau_{inv} = 0.7 \times R_{inv} \times C_{inv}$ is a delay of a reference inverter (which is constant in each standard CMOS technology), R_{inv} and C_{inv} are the resistance and gate capacitance of a reference inverter respectively. $p = \dfrac{R_G.C_P}{R_{inv}.C_{inv}}$ is the relative parasitic delay and $h = \dfrac{C_L}{C_G}$ is electrical effort.

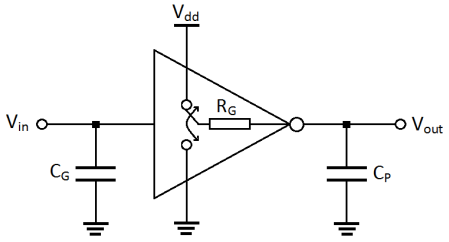

Figure 3-33: Simple model of CMOS inverter.

Figure 3-34 represents figure 3-32 with delay and electrical effort for each inverter. Shoji [22] has shown that if the delays of the second inverter in each of the two paths are equal (T_2=T_b, but not necessarily equal to the delays of the other inverters), the two paths will have the same delay in all four process corners. Process corners relate to NMOS and PMOS if they are slow or fast, so we have 4 process corners: S/S, S/F, F/S, F/F [25].

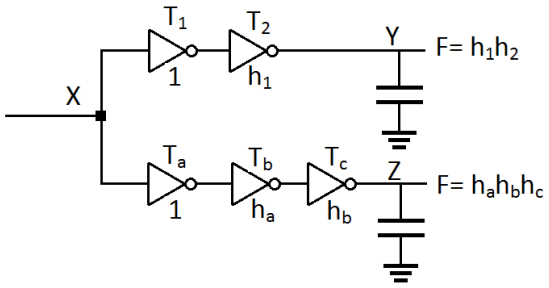

Figure 3-34: Two separate paths with the same delay (figure 3-32 with labels).

To determine the size of transistors based on [22], first the optimum loading factors (electrical factors) should be calculated.

$$\left.\begin{aligned} &T_1 + T_2 = T_a + T_b + T_c \\ &F = h_1.h_2 = h_a.h_b.h_c \\ &T_2 = T_b \end{aligned}\right\} \Rightarrow h_1 = h_a + h_c + p \;\&\; h_1 = h_a.h_c \tag{3.19}$$

For simplicity, we assume that electrical effort of inverter *a* and *c* have the same electrical effort.

$$h_a = h_c = h \tag{3.20}$$

Therefore, we can rewrite equation (3.19) as:

$$h^2 = 2h + p \Rightarrow h = 1 + \sqrt{1+p} \tag{3.21}$$

With p=1.25 [21] we have:

$$h_a = h_c = 2.5$$
$$h_1 = 6.25$$
$$h_2 = h_b = \frac{F}{6.25}$$

After electrical efforts' calculation, to define the size of inverters, we replaced output capacitors in figure 3-34 with two similar inverters (figure 3-35) and started from last stage. The size of replaced inverters at the output can be selected arbitrarily, but for driving pumping capacitors in charging pump circuit, the size of PMOS and NMOS transistors are selected as:

$$W_n = 100\mu m, W_p = 270\mu m, L_n = L_p = 0.35\mu m$$

Therefore, by scaling down the size of transistors from the last stage based on the h of each stage, we can calculate the size of all transistors (for all transistors: $L = 0.35\mu m$).

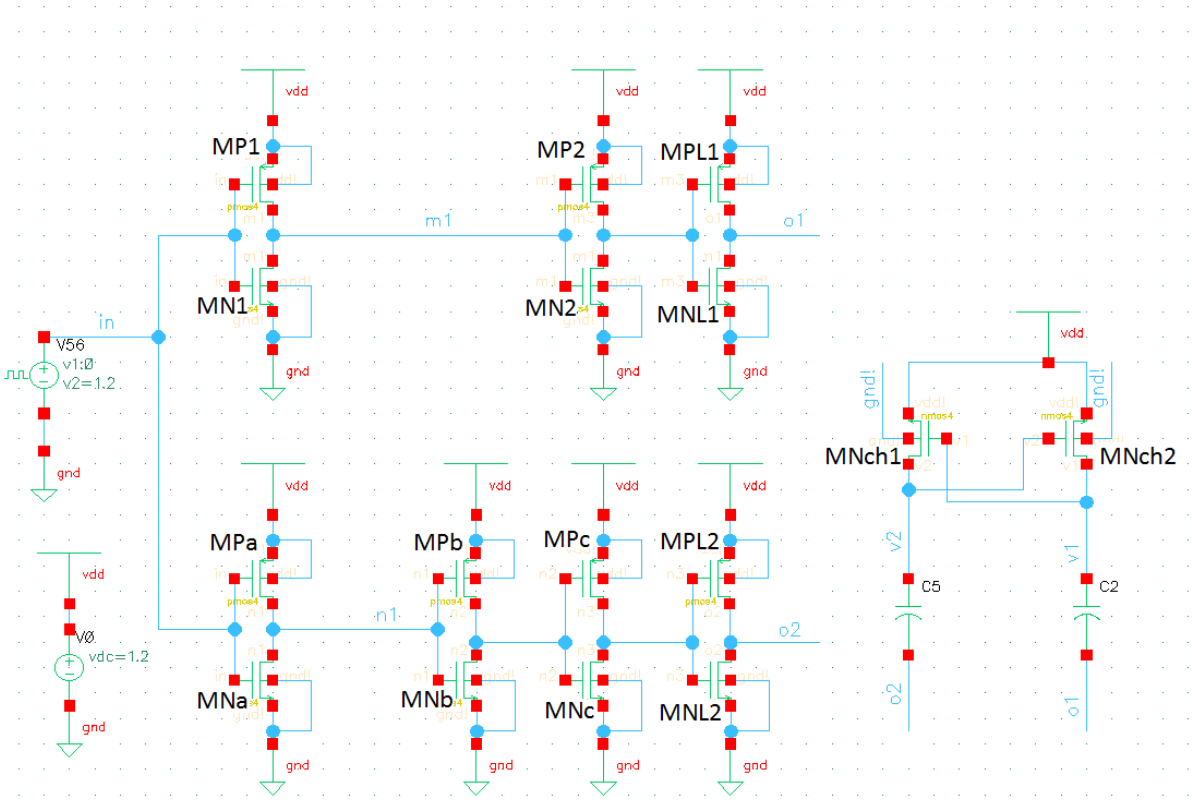

Figure 3-35: The circuit of ASIC-Buffer & drivers.

The simulation result in Cadence-Virtuoso-ADE is shown in figure 3-36.

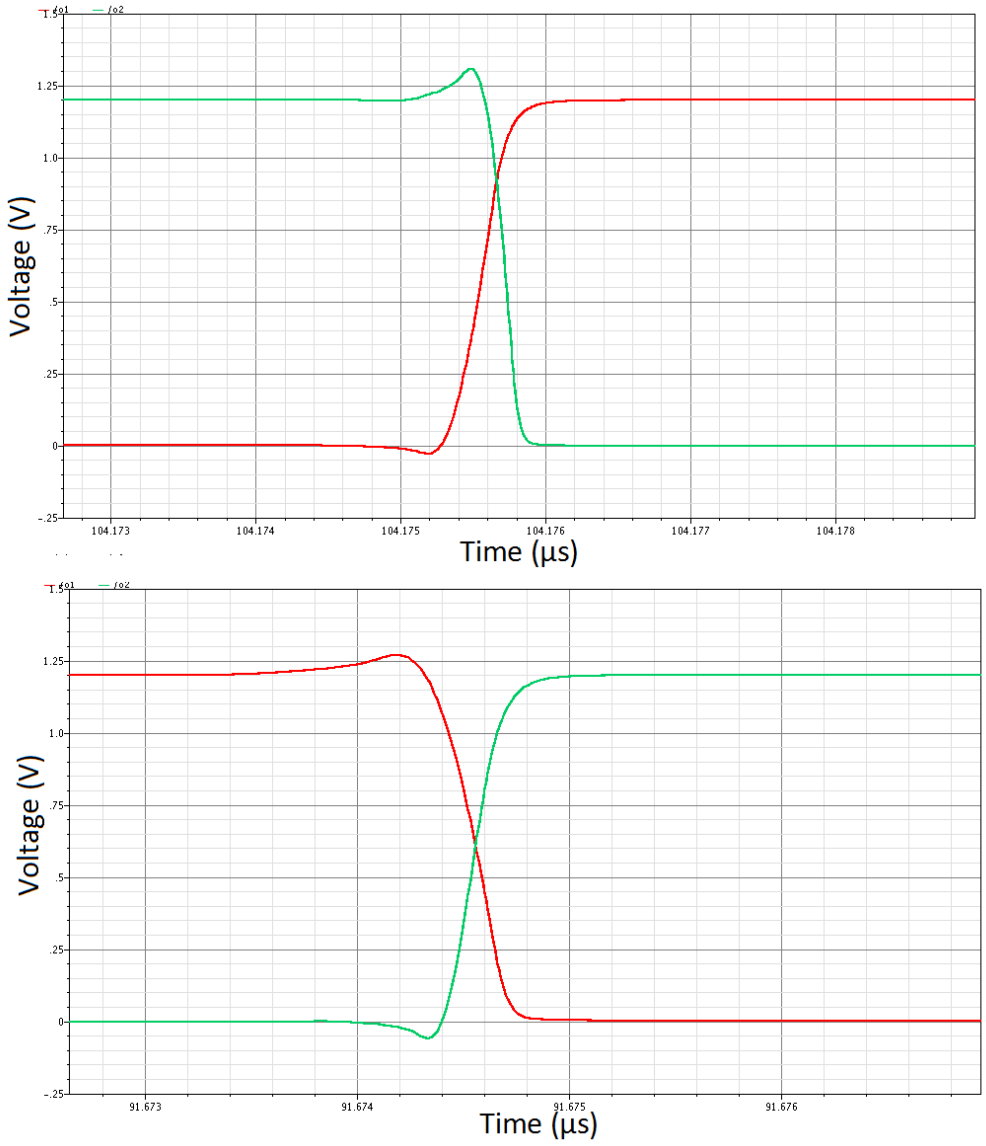

Figure 3-36: Transition switching in ASIC-Buffers& drivers circuit (voltage waveform of o1 and o2 in figure 3-35).

3.5. ASIC-Layout

Figure 3-37, shows the layout of the whole circuit and figure 3-38 shows the circuit in standard SOIC 20 die frame. Although we could use a frame with less number of pins (for example SOIC 14), for ease of testing of the internal nodes, the SOIC 20 die frame was selected.

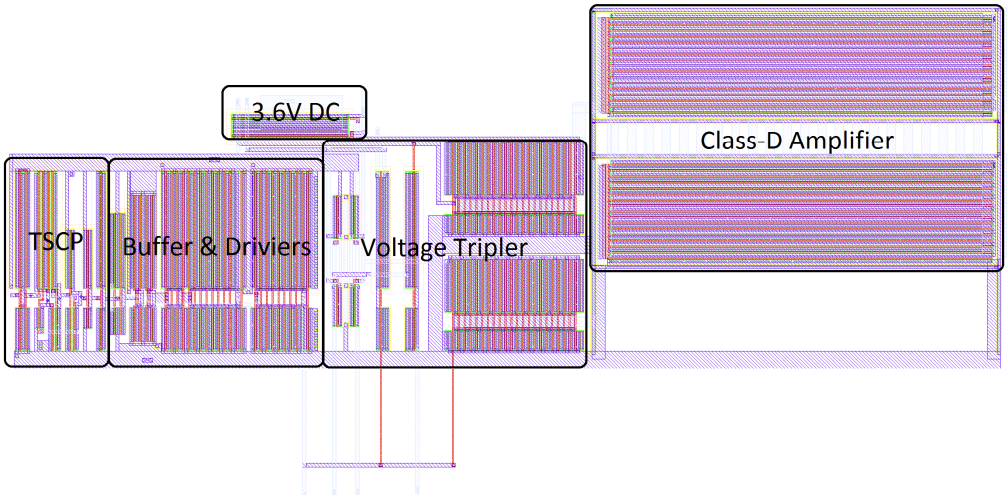

Figure 3-37: The layout of whole ASIC design without pads.

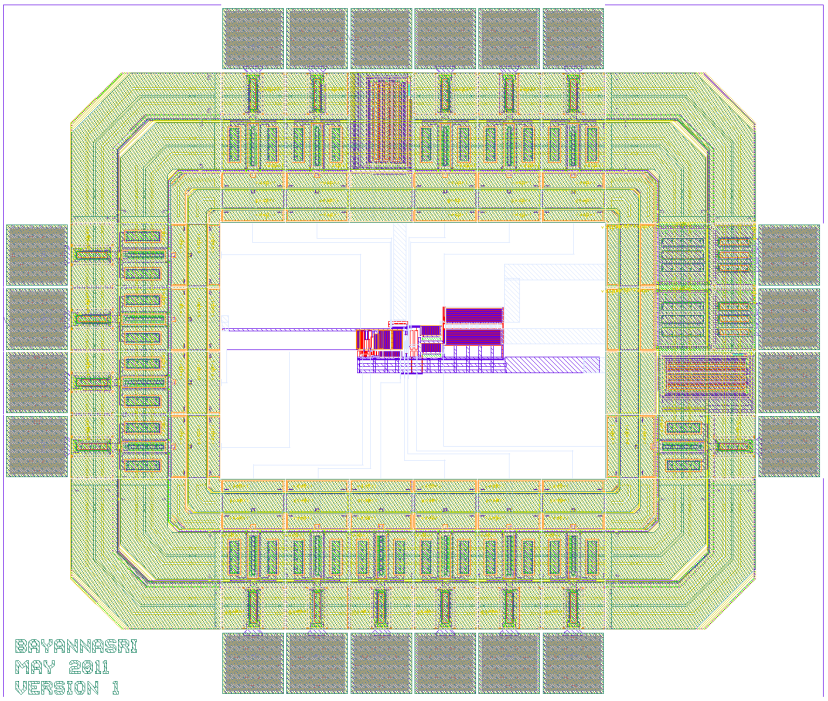

Figure 3-38: The layout of whole ASIC design in SOIC 20 Die frame.

3.6. Design Verification and Results

After designing the layout, a DRC (Design Rule Check) was carried out, then an LVS (Layout Versus Schematic) check was performed to verify that the layout view and the schematic view were identical. The last step in design verification is a post-layout simulation. For post-layout simulation, a test bench circuit was made (figure 3-39) and used for simulating both the schematic and layout with identical inputs and loads. The results of all pins (voltages and currents) are identical except the pin which produces 3.6V DC (figure 3-40). Figure 3-40 shows that the pin in schematic configuration reaches to steady state (3.59 V) 20µs before the same pin in layout configuration. This difference is caused due to parasitic capacitors in layout that are not considered in schematic simulation.

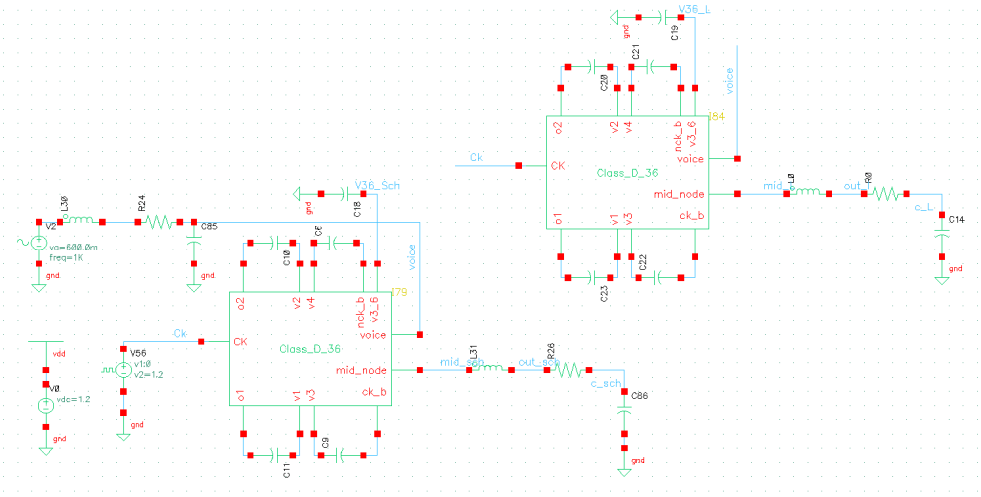

Figure 3-39: Test bench circuit for post-layout simulation.

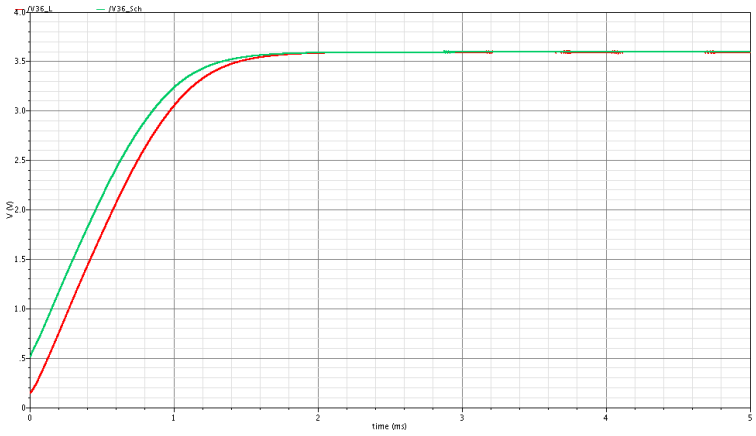

Figure 3-40: Difference between layout and schematic of the circuit on 3.6 V pin.

To assess the performance of the circuit, a test bench like figure 3-41 was used. The voice is modeled with a 0~1.2 V and 1 kHz Sine wave voltage supply. The RF link in the figure 3-41 is shown as a serial connection of a resistor with an inductor. The RF link is tuned with a capacitor of 20 nF. The circuit was tested in three different configurations to simulate three distances between transmitter and receiver.

According to figure 3-41, the total power which is consumed from the battery is:

$$P_S = P_{Vdc} + P_{V\sin} + P_{Ck} \tag{3.22}$$

In comparison with P_{Vdc} and P_{Vsin} , we can neglect P_{Ck} because it is in the range of nW.

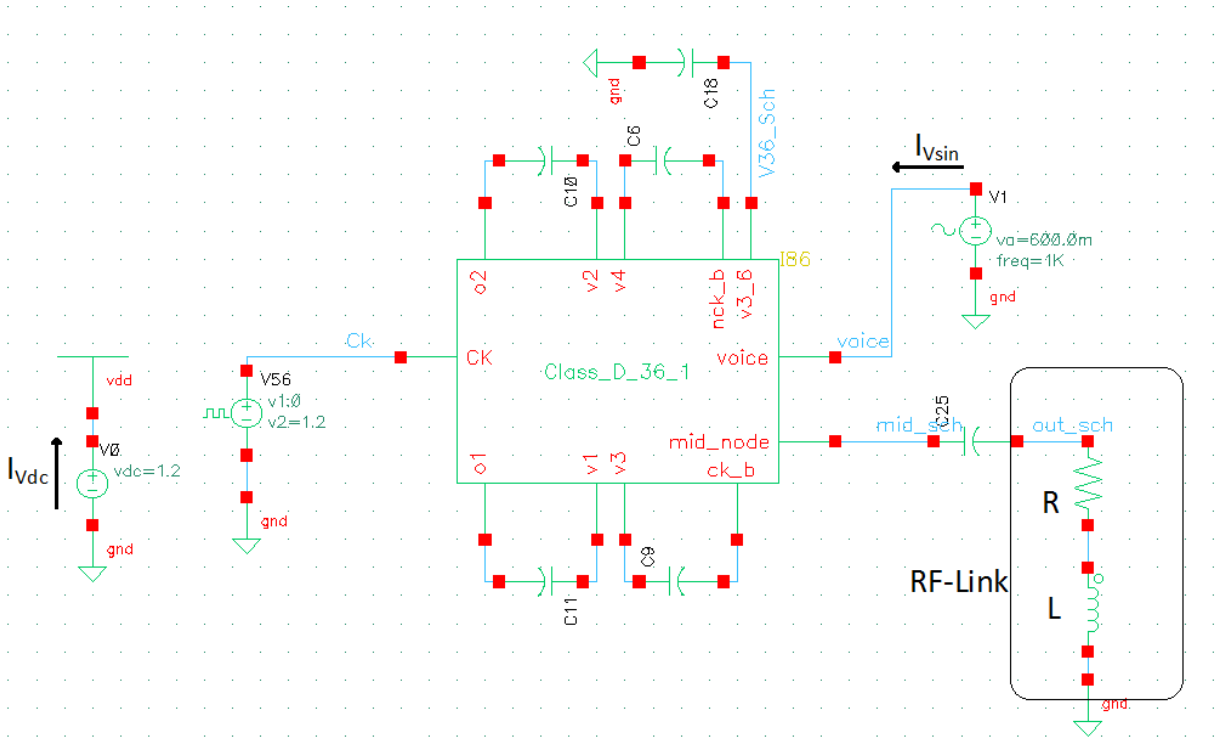

Figure 3-41: Test bench circuit for measurement.

Figure 3-42 shows the boosted clock pulses for driving the gates of Class-D amplifier. In contrast with figure 3-36 (which is related to ideal input signal), figure 3-42 has more symmetric property in term of level of transitions (2.14V and 2.24V).

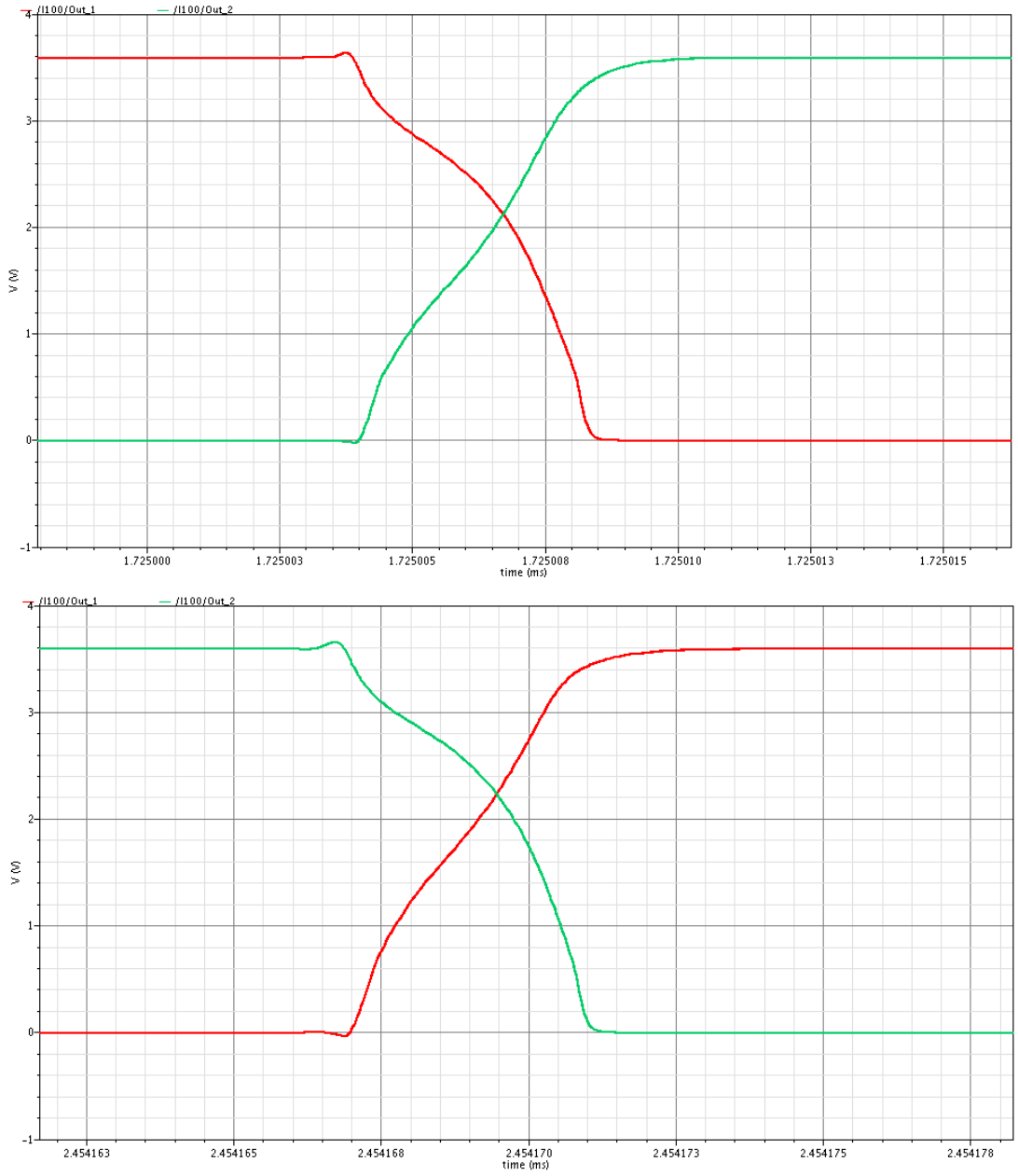

Figure 3-42: The boosted clock pulses for driving the gates of Class-D amplifier.

3.6.1. Simulation results at 8 mm distance (unloaded state)

The simulation result for average P_{Vdc} and P_{Vsin} are 0.25 mW and 14.35 mW respectively. Thus, the total power consumption taken from the battery is: P_S=14.6 mW.

Figure 3-43 shows the mid node voltage (node mid_sch in figure 3-41). It is clear that during the initial transient, the mid node voltage can reach up to 18 V. Mid node voltage is one of important factors to evaluate the performance of Class-D amplifier. The zoomed version of figure 3-43 is illustrated in figure 3-44. The mid node voltage swings as a pulse between -80 mV and 1.29 V. The more similarity of mid node with an ideal pulse (square waveform with the same voltage levels), the better performance of Class-D can be obtained.

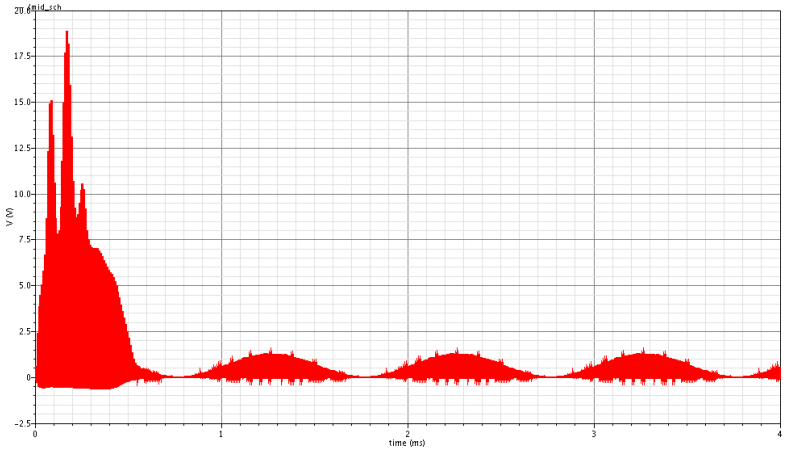

Figure 3-43: The mid node voltage of Class-D amplifier @ 8 mm distance.

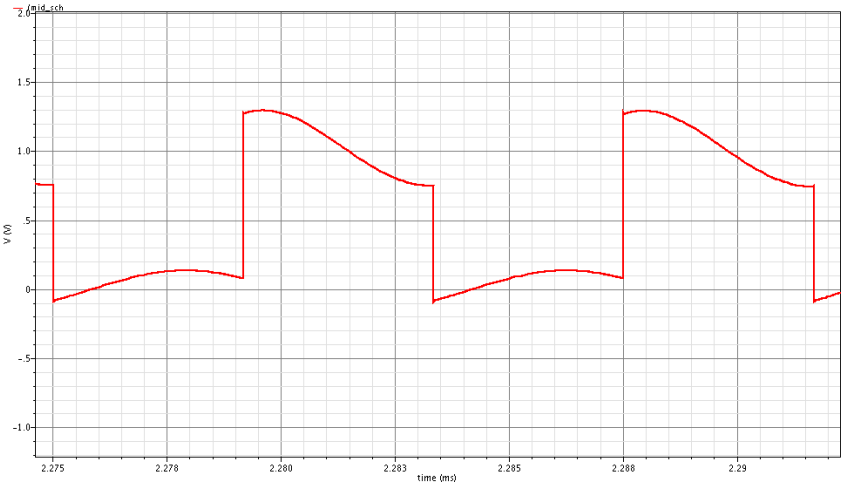

Figure 3-44: Zoomed version of figure 3-43.

Figure 3-45 shows the currents of transistors in Class-D amplifier. As was mentioned before, the spikes on current waveforms are because of using overlapped clock pulses. These spikes can reach to 285 mA but in a short time (20 ns). The maximum current is 128.6 mA that can be delivered to the RF link while the minimum current of −76.42mA can go back from the RF link to the transistor. Figure 3-45 also shows that the On/Off timing of transistors are not in the optimum position according to current level (the optimum position occurs when the current is in zero level), but this phenomenon is an advantage in term of output voltage that will be discussed in figure 3-47.

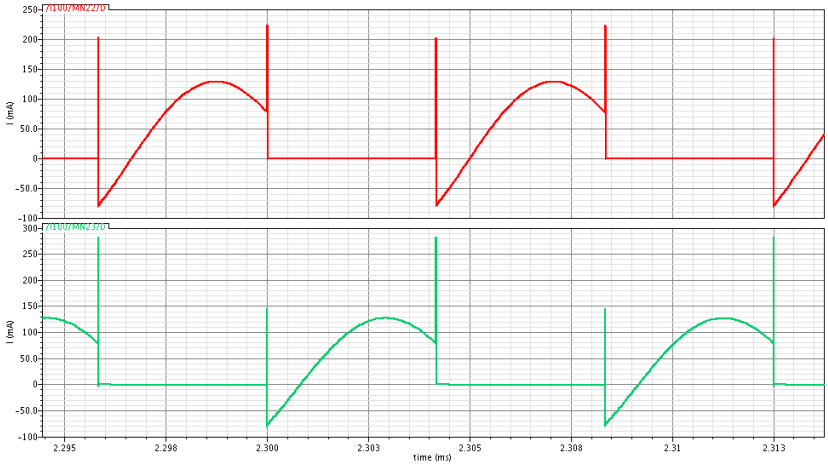

Figure 3-45: the currents of transistors in Class-D amplifier @ 8mm distance.

The voltage drops on RF link can reach to 22 V during the initial transient (figure 3-46). The peak-peak voltage of RF link is 18.45 V (–9.12 V ~ 9.33 V).

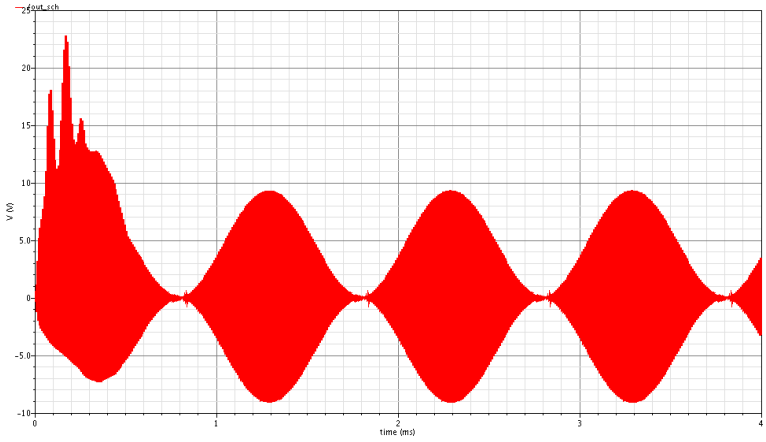

Figure 3-46: The voltage drops on RF-Link @ 8mm distance.

The zoomed version of figure 3-46 is shown in figure 3-47. As was mentioned before, the current switching does not happen at the optimum position, but it has advantage for RF link voltage. In figure 3-47 it is clear that the switching isn't at the maximum or minimum nodes of voltage.

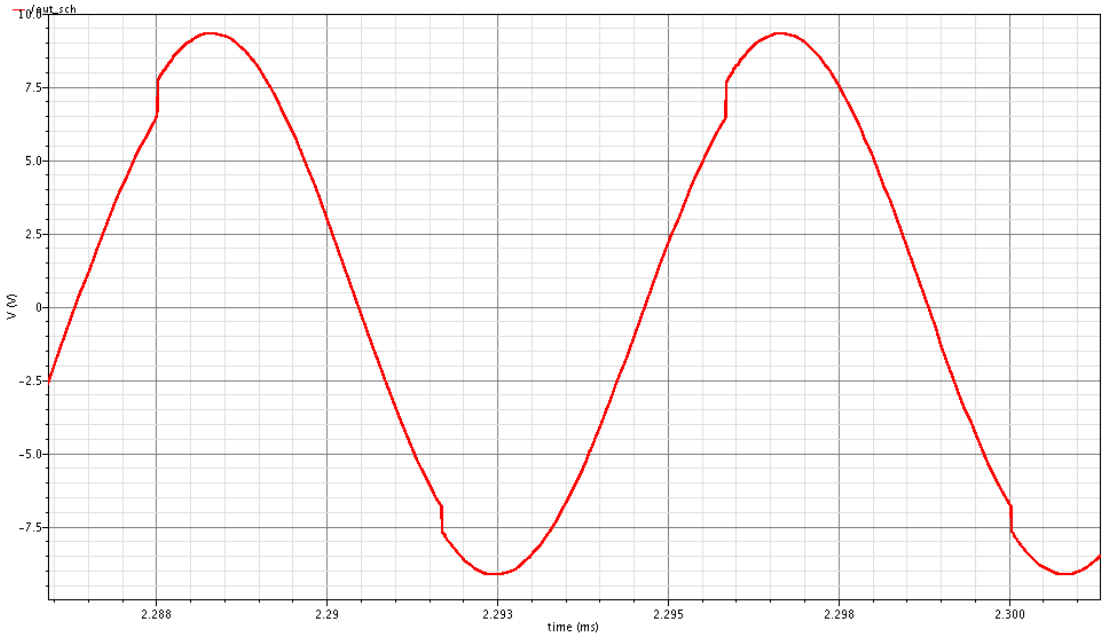

Figure 3-47: The zoomed version of figure 3-46

In audio applications, THD is used to measure the total distortion of the system. The total harmonic distortion, THD, is the ratio of the sum of the power of all harmonic components to the power of the fundamental frequency.

$$THD = \frac{\sum_{i=2}^{\infty} P_i}{P_1} \tag{3.23}$$

Where P_i is the power of harmonic i and P_1 is the power of fundamental frequency.

By using the predefined function *THD*, in Cadence-ADE-Calculator the *THD* of the RF link voltage at 8 mm distance is $THD = 3.9\%$. It should be mentioned that the *THD* value does not say anything about the sound quality as it is only the measure of the carrier not the envelope.

By multiplying the RF link voltage to its current, we can get the Power waveform that can be delivered to the load through RF link (figure 3-48). The maximum power that can be delivered to the RF link is 609 mW and its average is 8.5 mW.

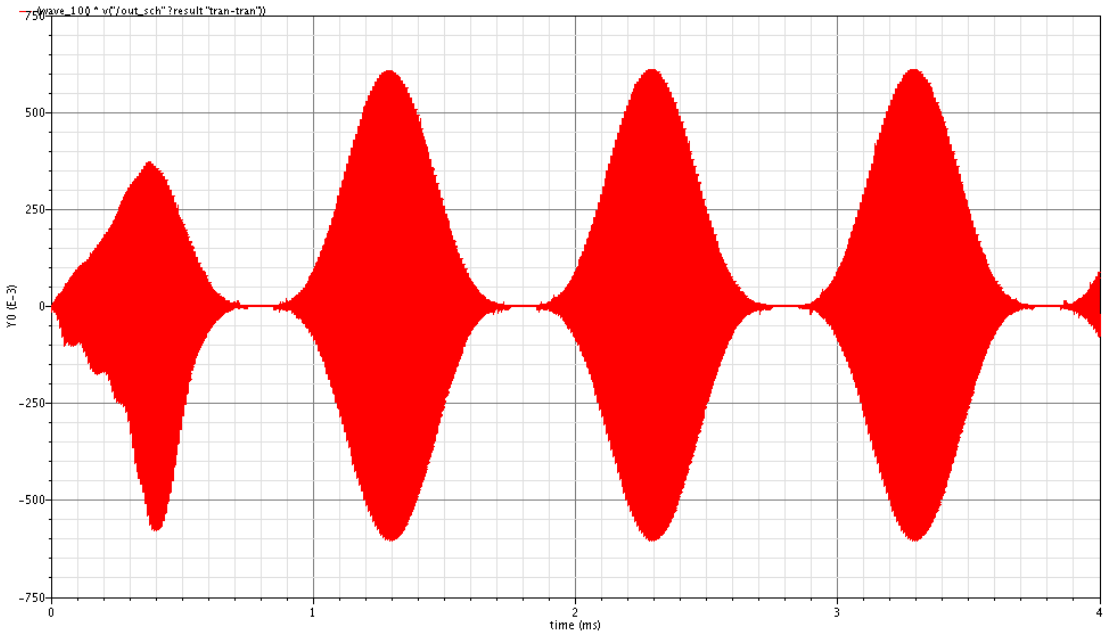

Figure 3-48: The power that can be delivered through RF link @ 8 mm distance.

One of the important parameters in Class-D amplifiers is power dissipation in switches of Class-D amplifier. By definition, power dissipation in switching amplifiers is consists of two terms: signal and spike power dissipation [24] as below:

$$P_{Signal} = V_{dd}.I_{ds} \tag{3.24}$$

$$P_{Spike} = C.V_{ds}^{2}.f \tag{3.25}$$

Where V_{dd} is supply voltage, I_{ds} is a drain current of transistor, C is the total output node capacitance, V_{ds} is the drain-source voltage of transistor and f is switching frequency.

Figure 3-49 shows the total power dissipation in one of the Class-D NMOS transistors which is the product of mid node voltage (V_{ds} of lower NMOS) and drain current of related NMOS transistor. The spikes in the figure 3-49 relates to dynamic power dissipation of transistor. Thanks to Cadence-Virtuoso-ADE calculator, the average power dissipation of each transistor is obtained as: $P_{NMOS} = 1.6mW$.

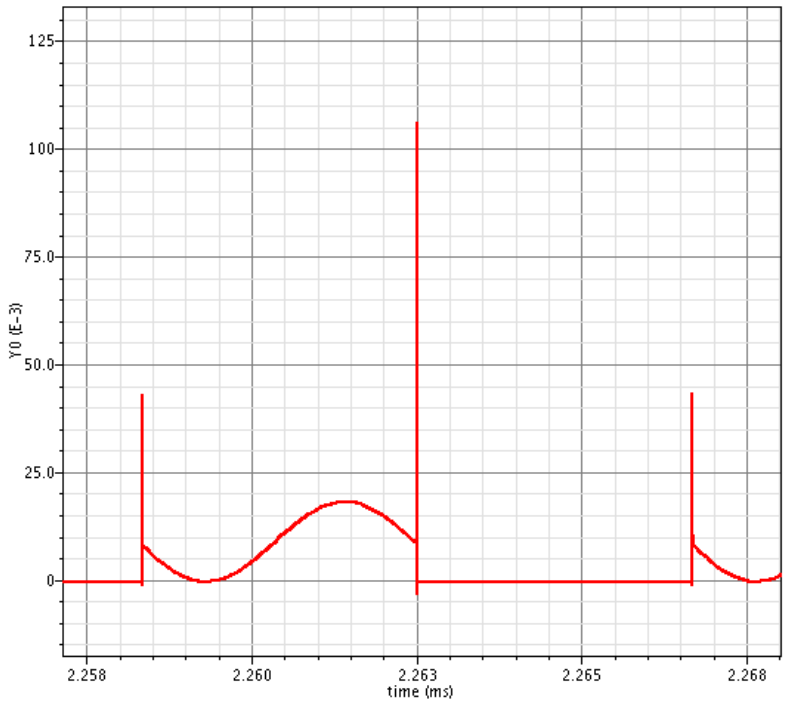

Figure 3-49: Power dissipation (mW) for each NMOS transistors in Class-D amplifier @ 8 mm distance (unloaded).

The total power taken from battery is: P_S=14.6 mW. The average power that can be delivered to the RF link is: P_{load}=8.5 mW

So the performance of the ASIC at 8 mm distance can be calculated as below:

$$\eta = \frac{P_{load}}{P_{Source}} = 58\%$$

3.6.2. Simulation results at 4 mm distance (optimum state)

The simulation result for average P_{Vdc} and P_{Vsin} are 0.25 mW and 11.75 mW respectively. Thus, the total power consumption taken from the battery is: P_S=12 mW.

Figure 3-50 shows the currents of transistors in Class-D amplifier at 4mm distance. The maximum of spikes is 258mA. The maximum current is 88.78 mA that can be delivered to the RF link. Figure 3-45 also shows that the On/Off timing of transistors are in the optimum position according to current level.

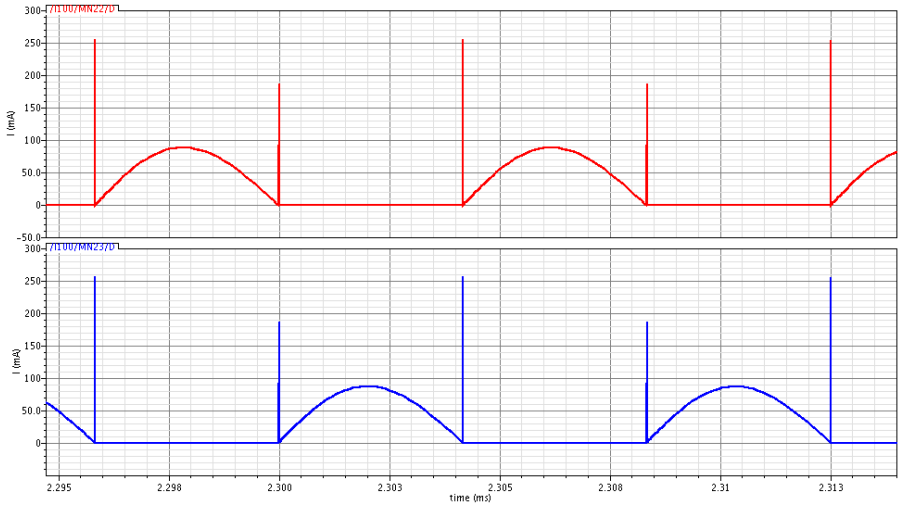

Figure 3-50: The currents of transistors in Class-D amplifier @ 4 mm distance.

Figure 3-51 shows the mid node voltage at 4 mm distance. During the initial transient, the mid node voltage can reach up to 6V. The zoomed version of figure 3-51 is illustrated in figure 3-52. The mid node voltage swings as a pulse between 0V and 1.22V.

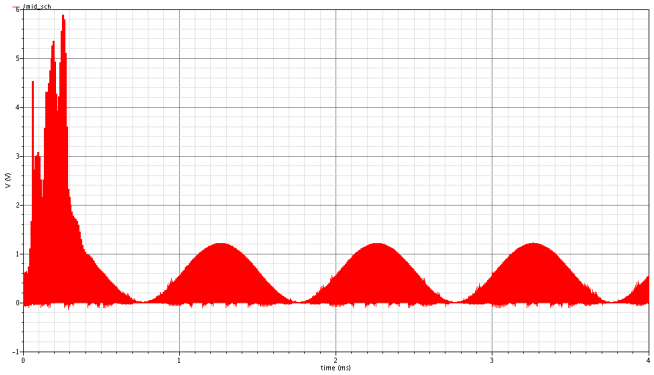

Figure 3-51: The mid node voltage of Class-D amplifier @ 4 mm distance.

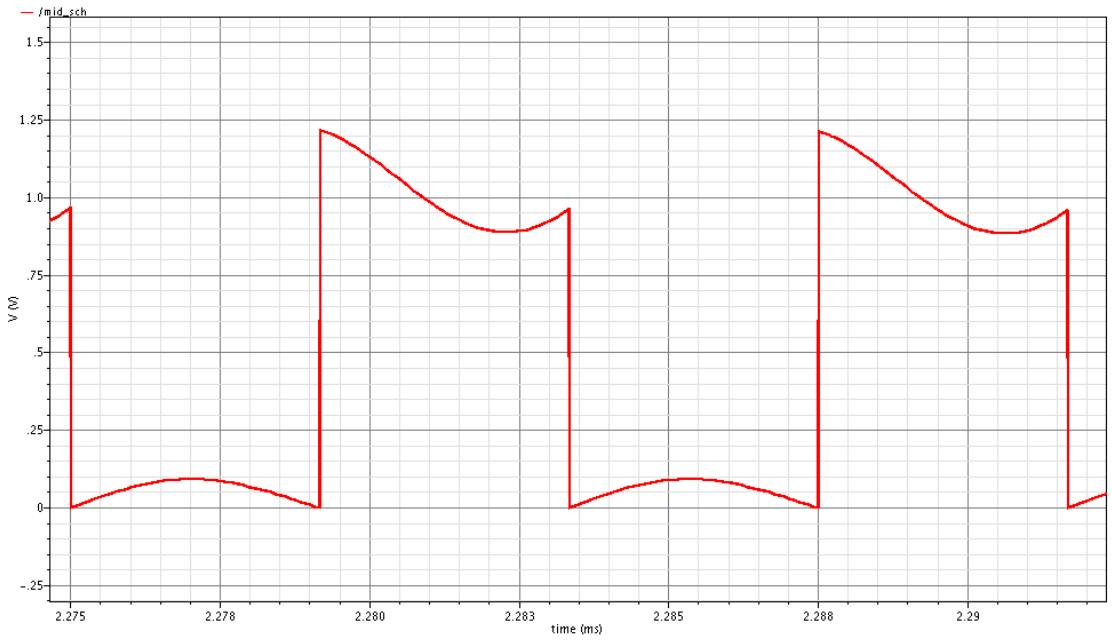

Figure 3-52: Zoomed version of figure 3-51.

At 4 mm distance, the voltage drops on the RF link can reach to 8 V during the initial transient (figure 3-53). The peak-peak voltage of the RF link is 18.45V (−6.36 V ~ 6.52 V).

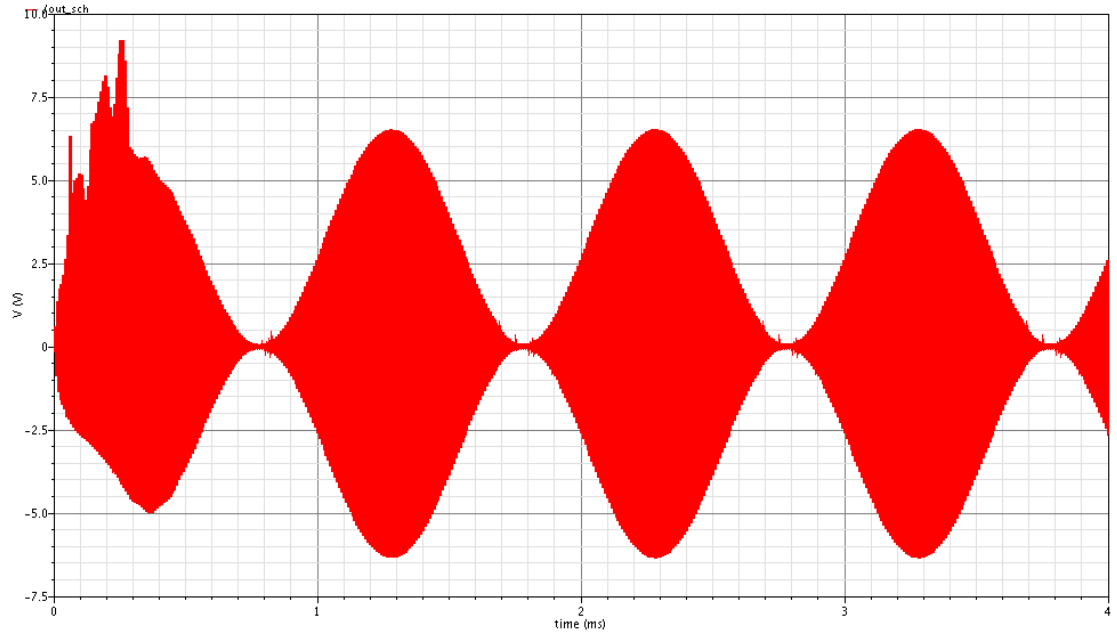

Figure 3-53: The voltage drops on the RF link @ 4 mm distance.

The zoomed version of figure 3-53 is shown in figure 3-54. In contrast with figure 3-46 (8 mm distance), the current switching is at the maximum or minimum nodes of voltage.

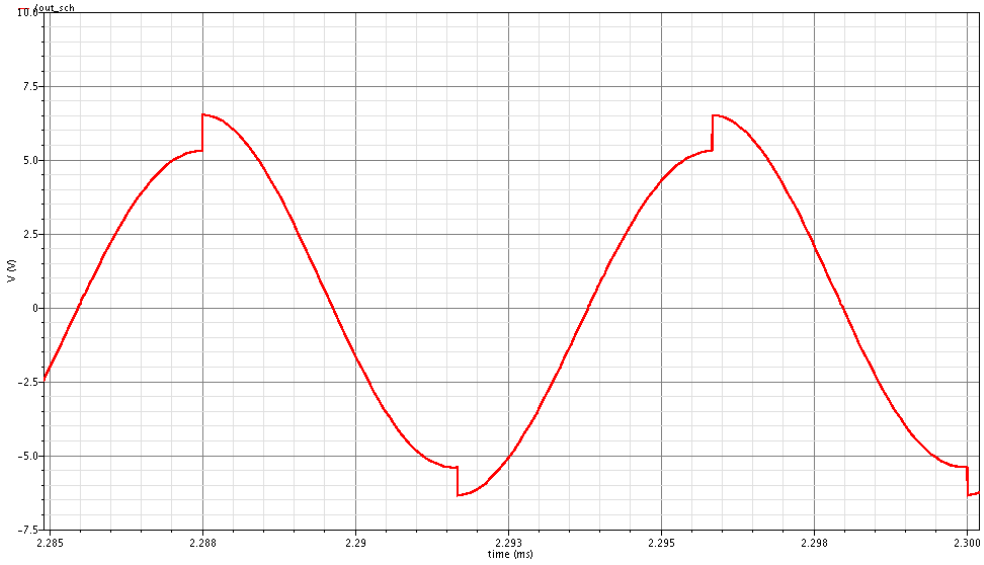

Figure 3-54: The zoomed version of figure 3-53.

The maximum distortion at 4 mm distance was measured as: $THD = 6.216\%$. The power waveform of the RF link at 4 mm distance is shown in figure 3-55. The maximum power is measured as 301.49 mW and its average is 8.632 mW. Although the maximum transferred power to the RF link is higher at 8 mm distance, the average of transferred power to the RF link is higher at 4 mm distance.

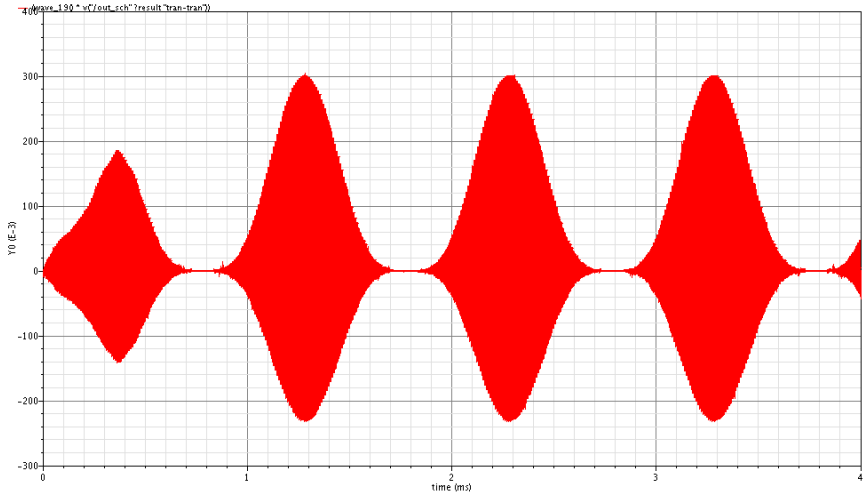

Figure 3-55: The power that can be delivered through RF link @ 4 mm distance.

Figure 3-56 shows the total power dissipation in one of the Class-D NMOS transistors at 4mm. The average power dissipation of each transistor is obtained as: $P_{NMOS} = 0.7578mW$.

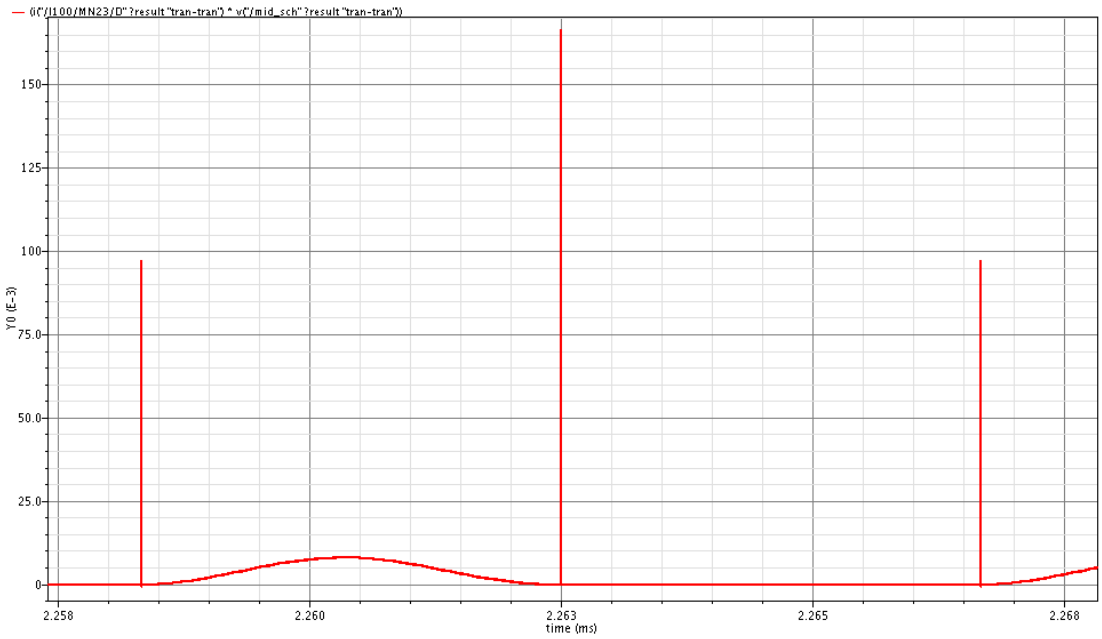

Figure 3-56: Power dissipation (mW) for each NMOS transistors in Class-D amplifier @ 4 mm distance (optimum position).

The total power taken from battery is: P_S=12 mW. The average power that can be delivered to the RF link is: P_{load}=8.63 mW

So the performance of the ASIC at 4 mm distance can be calculated as below:

$$\eta = \frac{P_{load}}{P_{Source}} = 72\%$$

3.6.3. Simulation results at 0 mm distance

The simulation result for average P_{Vdc} and P_{Vsin} are 0.25 mW and 5.9 mW respectively. Thus, the total power consumption taken from the battery is: P_S=6.15 mW.

Figure 3-57 shows the currents of transistors in Class-D amplifier at 0mm distance. The maximum of spikes is 252mA. The maximum current is 44.24mA that can be delivered to the RF link while the minimum current of −4.14mA can go back from the RF link to the transistor.

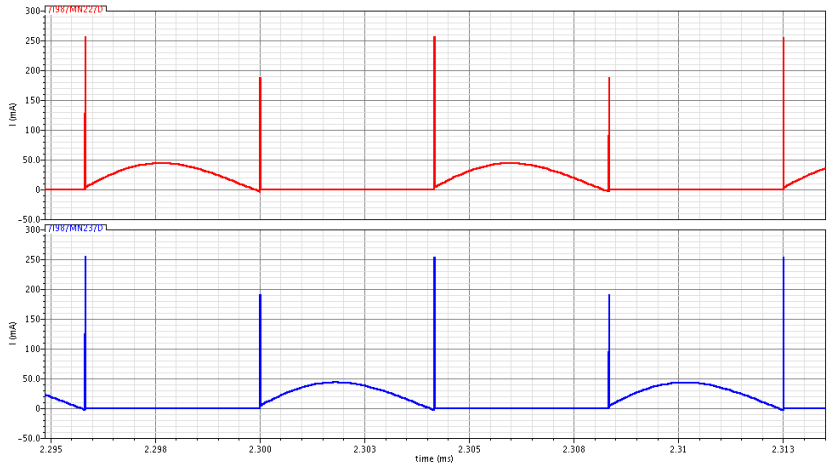

Figure 3-57: The currents of transistors in Class-D amplifier @ 0 mm distance.

Figure 3-58 shows the mid node voltage at 0 mm distance. During the initial transient, the mid node voltage can reach up to 3.8 V. The zoomed version of figure 3-58 is illustrated in figure 3-59. The mid node voltage swings as a pulse between −4.18 mV and 1.21 V.

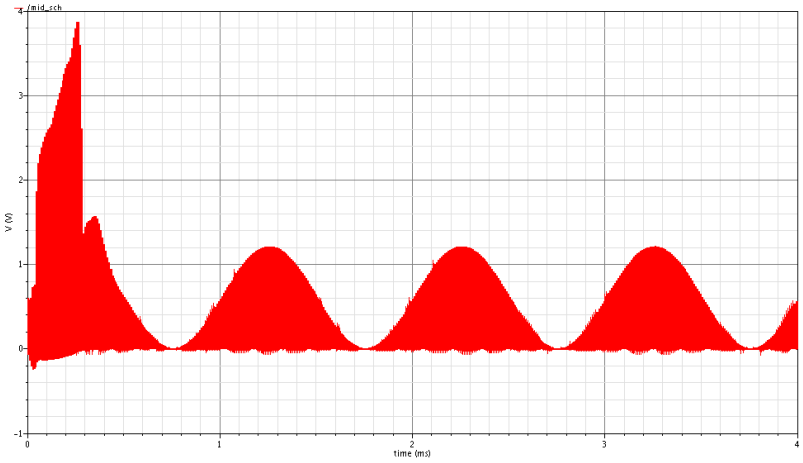

Figure 3-58: The mid node voltage of Class-D amplifier@ 0 mm distance.

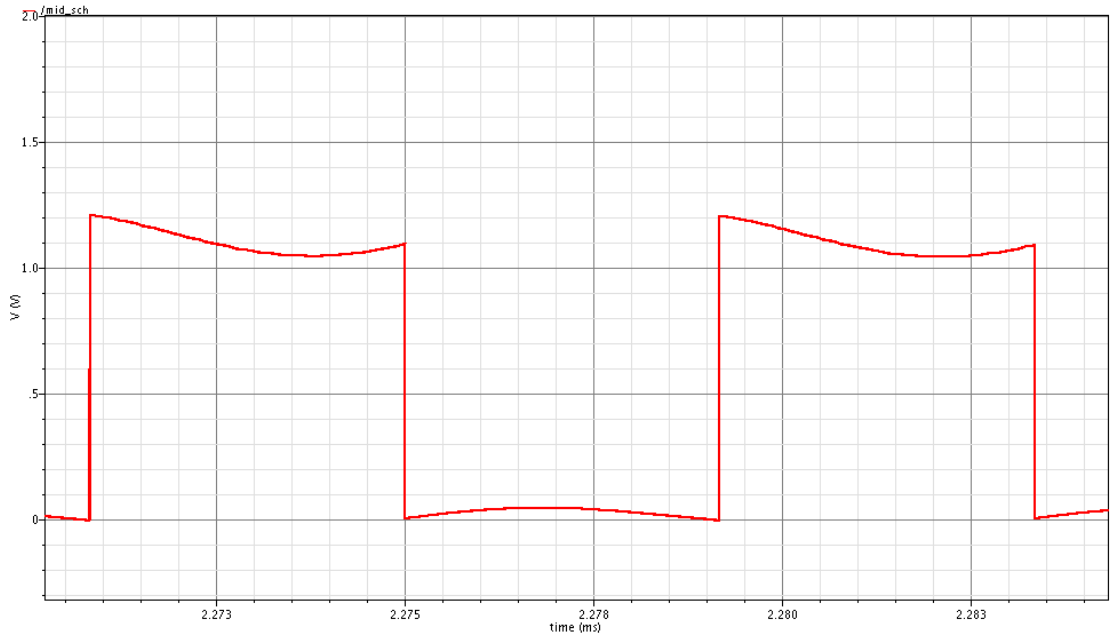

Figure 3-59: Zoomed version of figure 3-58.

At 0mm distance, the peak-peak voltage of RF link is 18.45V (−3.43 V ~ 3.52 V).

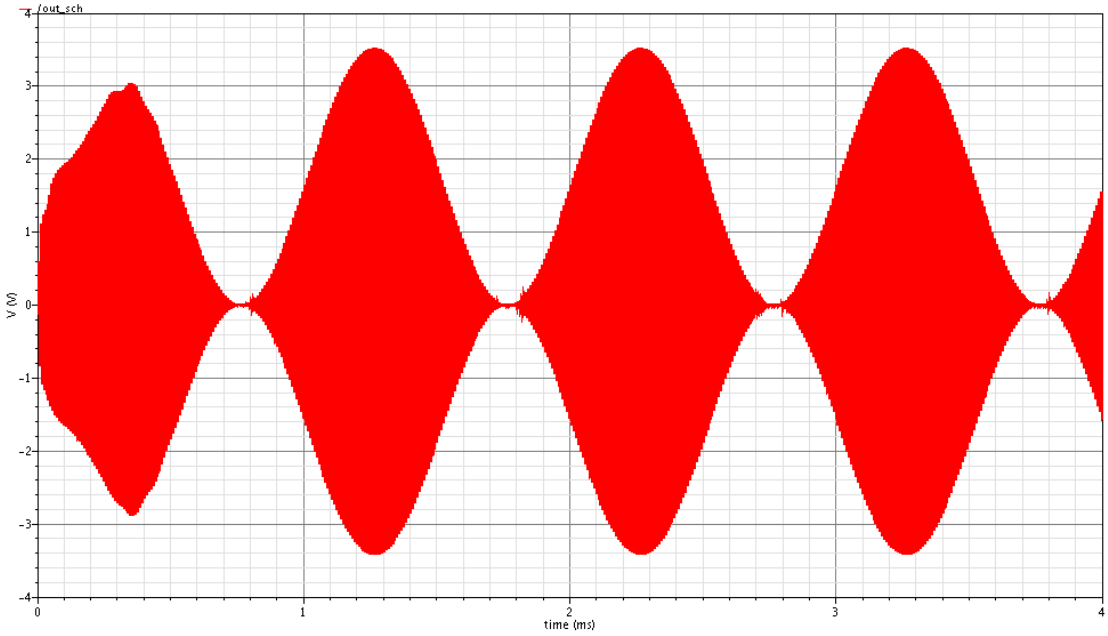

Figure 3-60: The voltage drops on RF link @ 0 mm distance.

The zoomed version of figure 3-60 is shown in figure 3-61.

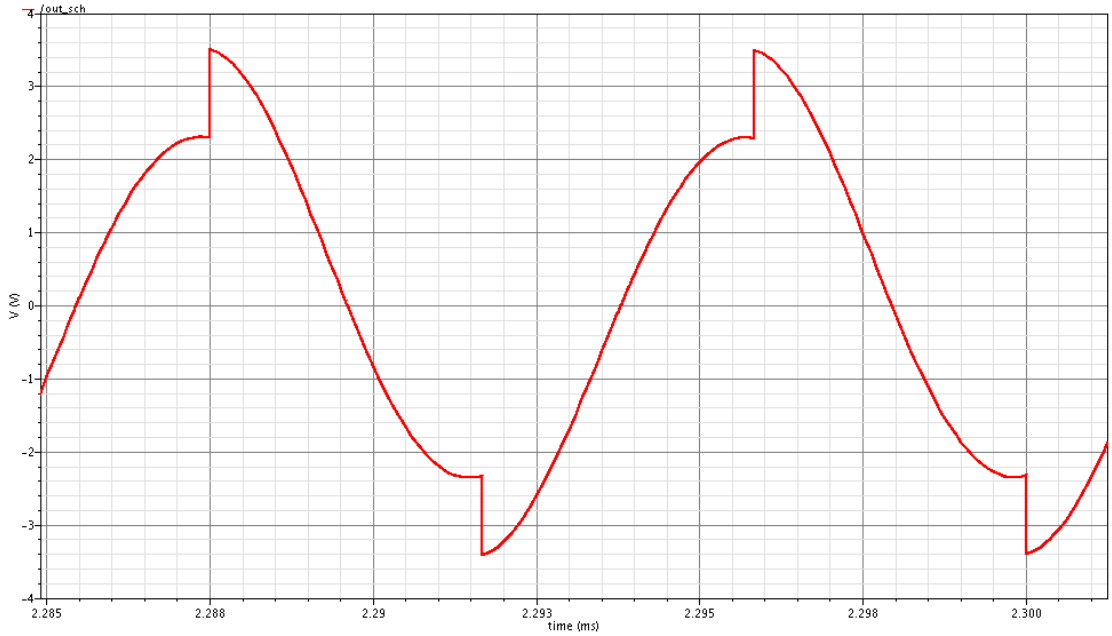

Figure 3-61: The zoomed version of figure 3-60.

The maximum distortion at 0mm distance was measured as: $THD = 13.13\%$.

The power waveform of RF link at 0 mm distance is shown in figure 3-62. The maximum power is measured as 86.4 mW and its average is 5 mW.

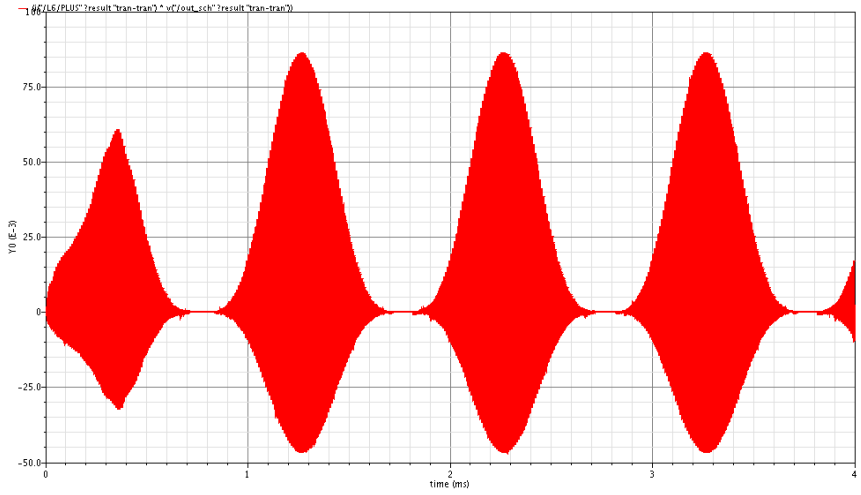

Figure 3-62: The power that can be delivered through RF link @ 0 mm distance.

Figure 3-63 shows the total power dissipation in one of the Class-D NMOS transistors at 0 mm. The average power dissipation of each transistor is obtained as: $P_{NMOS} = 0.2012mW$.

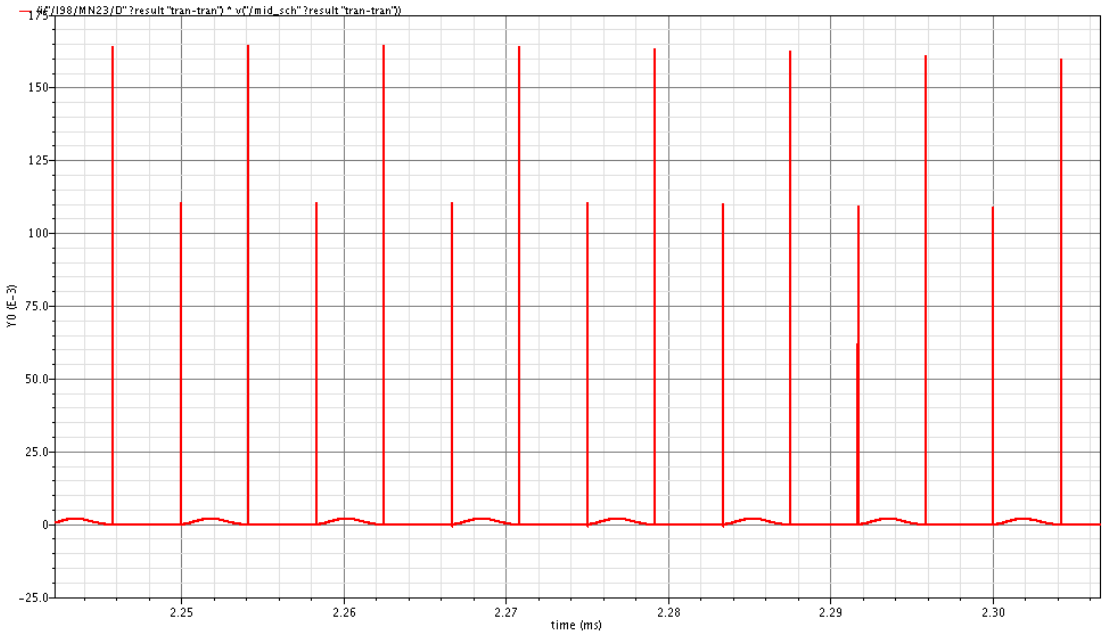

Figure 3-63: Power dissipation (mW) for each NMOS transistors in Class-D amplifier @ 0 mm distance.

The total power taken from battery is: P_S=6.15 mW. The average power that can be delivered to the RF link is: P_{load}=5 mW

So the performance of the ASIC at 0 mm distance can be calculated as below:

$$\eta = \frac{P_{load}}{P_{Source}} = 81\%$$

4. Conclusion

In this project, a low power low voltage ASIC for Bone Conduction Implant has been designed. The project was started from system level and implementation in discrete circuit design to visualize the comparison between two well-known switching amplifiers, Class-D and Class-E. The benefit of discrete circuit design besides helping to select the proper Class of amplifiers for the project is find out the power requirement for RF-link and consequently the stimulation of transducer. The results of discrete circuit design showed that Class-D amplifier has better performance due to pre-defined clock frequency and power consumption.

In the next part of the project, the ASIC version of the circuit was designed in 0.35µm standard CMOS technology. The ASIC design was designed by studying and simulating different architectures for each sub-block such as clock division circuits, gate drivers, level shifters and Class-D amplifier. After schematic design, the layout was designed in Cadence-Virtuoso-Suite. Since this is the first prototype, it is a good idea to test all internal nodes within the circuit. So the SOIC20 ceramic package (Appendix C) was selected. The standard voltage supply for 0.35µm standard CMOS technology is 3.3V or 5V, but this project was designed based on 1.2V. So for ESD protection a 3.6V DC voltage is generated.

The layout was verified due to Design Rule Check (DRC) and Layout Versus Schematic (LVS) check. It should be mentioned that LVS check was done before pad connection, because pads in Cadence-Virtuoso-Suite are defined as cell libraries which need extra rule check that are not supported by non industrial version of Cadence-Virtuoso-Suite layout design. The simulation results are listed in table 4-1.

Parameter	0 mm distance	4 mm distance	8 mm distance
Maximum output voltage (V)	3.52	6.53	9.33
Maximum power of RF-Link (mW)	86.4	301.49	609
THD (%)	13.13	6.216	3.9
ASIC performance (%)	81	72	58

Table 4-1: The simulation results at three different distances.

5. Future work

Adding smart control to the ASIC: Design a circuit to turn the ASIC to the idle mode when there is no sound, helps to improve the power consumption of the whole circuit. This can be done by adding an analog circuit to the output of DSP.

Using higher operating frequency: Since the RF link is designed to work with 120 kHz, we have to use a clock pulse with the same frequency. If the RF link be modified to work with a higher frequency in the range of MHz, there will be some advantages for the ASIC. First, the size of pumping capacitors which are already off-chip, will shrink and they can be implemented within the chip. Second, the size of the RF link and its series capacitor will shrink. Thus, the total area of the circuit (on-chip/off-chip) will be reduced. Finally, using an operating frequency in the range of MHz, gives the opportunity to make the PDM/PWM conversion within the ASIC.

Design an internal oscillator: Instead of external crystal as a clock generator, using an internal oscillator can help the project according to occupied area. Furthermore, internal control can be done in generating clock pulse by using PLL or VCO circuits.

Changing the CMOS technology: Although 0.35 µm standard CMOS technology (which was used in this project) is more convenient in analog integrated circuit (according to the maximum delivering current to the load), its standard supply voltages are 3.3 V and 5 V that are higher than battery voltage level (1.2 V) which is the main supply voltage of this project. These standard supply voltages are important in ESD protection. In this project, we had to design extra circuit to produce a proper DC voltage (3.6 V) for ESD protection. However, if we move through 130 nm CMOS technology, there is no need to use extra circuit for ESD protection, because the standard supply voltage of 130 nm CMOS technology is 1.2 V which is match with the battery voltage level. In addition, the threshold voltage of NMOS and PMOS transistors in 130 nm CMOS technology are smaller than 0.35 µm. Thus, we do not need to use a voltage tripler circuit and a voltage doubler circuit might be enough to drive the gates of Class-D amplifier.

6. References

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Appendix A

AMS C35B4 CMOS Process Parameters

Electrical Parameters

Transistor					
	N-type		P-type		Unit
Gain factor (datasheets)	KP_n	175	KP_p	58	$\mu A/V^2$
Gain factor (simulated)	KP_n	115	KP_p	40	$\mu A/V^2$
Threshold voltage (W/L=10/10)	V_{tn0}	0.46	V_{tp0}	-0.60	V
Threshold voltage (W/L=10/0.3)	V_{tn0}	0.48	V_{tp0}	-0.60	V
Effective channel length (0.3 μm)	$L_{eff,03,n}$	0.40	$L_{eff,03,p}$	0.53	μm
Effective channel length (0.6 μm)	$L_{eff,06,n}$	0.50	$L_{eff,06,p}$	0.50	μm
Body effect factor (W/L=10/10)	γ_n	0.58	γ_p	-0.45	$\sqrt{V}$
Bulk potential	ϕ_{bn}	0.79	ϕ_{bp}	-0.77	V
Resistance, active region (sim.)	r_{ds_n}	55	r_{ds_p}	55	$\Omega A/\mu m$
Saturation current (0.3 μm)	I_{sat_n}	540	I_{sat_p}	-240	$\mu A/\mu m$
D-S breakdown volt. (0.3 μm)	V_{brn}	> 8	V_{brp}	> -8	V

Capacitances (layer to substrate)	Area fF/μm^2		Perimeter fF/μm	
gate capacitance	C_{ox}	4.60		
gate-diff overlap			C_{gd0}	0.21
gate-bulk overlap			C_{gb0}	0.11
n^+ diffusion (0 V)	C_{jn}	0.93	C_{jnp}	0.28
p^+ diffusion (0 V)	C_{jp}	1.42	C_{jpp}	0.38
$N_{well} - bulk(0V)$	C_{jw}	0.11	C_{jwp}	0.53
poly1	C_{p1}	0.119	C_{pp}	0.052
metal1	C_{m1}	0.032	C_{m1p}	0.046
metal2	C_{m2}	0.012	C_{m2p}	0.036
metal3	C_{m3}	0.008	C_{m3p}	0.037
metal4	C_{m4}	0.006	C_{m4p}	0.033
poly1-poly2	C_{poly_s}	0.86	C_{poly_p}	0.082

Sheet resistance		
Layer		$\Omega/\square$
metal4	R_{sm4}	0.05
metal3	R_{sm3}	0.05
metal2	R_{sm2}	0.08
metal1	R_{sm1}	0.08
poly1	R_{sp}	6
poly2	R_{sp2}	50
n^+ diff.	R_{sdn}	80
p^+ diff.	R_{sdp}	150
n-well	R_{nw}	1000

Max. current density		
Layer	mA/μm	
metal4	J_{m4}	1.6
metal3	J_{m3}	1.0
metal2	J_{m2}	1.0
metal1	J_{m1}	1.0
poly1	J_p	0.5
poly2	J_{p2}	0.3

Max. contact current		
0.4 μm×0.4 μm contact		
0.5 μm×0.5 μm via, via2, via3		
Layer-layer		mA
metal4-metal3	I_{via3}	0.96
metal3-metal2	I_{via2}	0.60
metal2-metal1	I_{via}	0.60
metal1-poly1/diff	I_{cp}	0.94

Contact resistance		
Layer-layer	Ω/cnt	
metal4-metal3	R_{via3}	3
metal3-metal2	R_{via2}	1.5
metal2-metal1	R_{via}	1.5
metal1-poly1	R_{cp}	5
metal1-n^+ diff.	R_{cdn}	40
metal1-p^+ diff.	R_{cdp}	90

Diode data		N	P
Area junc. pot.	V_j	0.69 V	1.02 V
Sidewall junc. pot.	V_{sw}	0.69 V	1.02 V
Area grading coeff.	m_j	0.31	0.55
Sidewall grading coeff.	m_{sw}	0.19	0.39

Structural and geometrical parameters		
Gate oxide thickness	t_{ox}	7.5 nm
Poly1-poly2 oxide thickness	t_{pox}	41 nm
Field oxide thickness	t_{fox}	290 nm
Poly1-metal1 oxide thickness	t_{pox}	645 nm
Metal1-metal2 oxide thickness	t_{mox}	1.00 μm
Metal2-metal3 oxide thickness	t_{mox2}	1.00 μm
Metal3-metal4 oxide thickness	t_{mox3}	1.00 μm
Passivation thickness	t_{prot}	900 nm
Poly1 thickness	t_p	282 nm
Metal1 thickness	t_{m1}	665 nm
Metal2 thickness	t_{m2}	640 nm
Metal3 thickness	t_{m3}	925 nm
Metal4 thickness	t_{m4}	925 nm
n^+ and p^+ junction depth	x_j	200 nm
n-well junction depth	x_w	2.0 μm

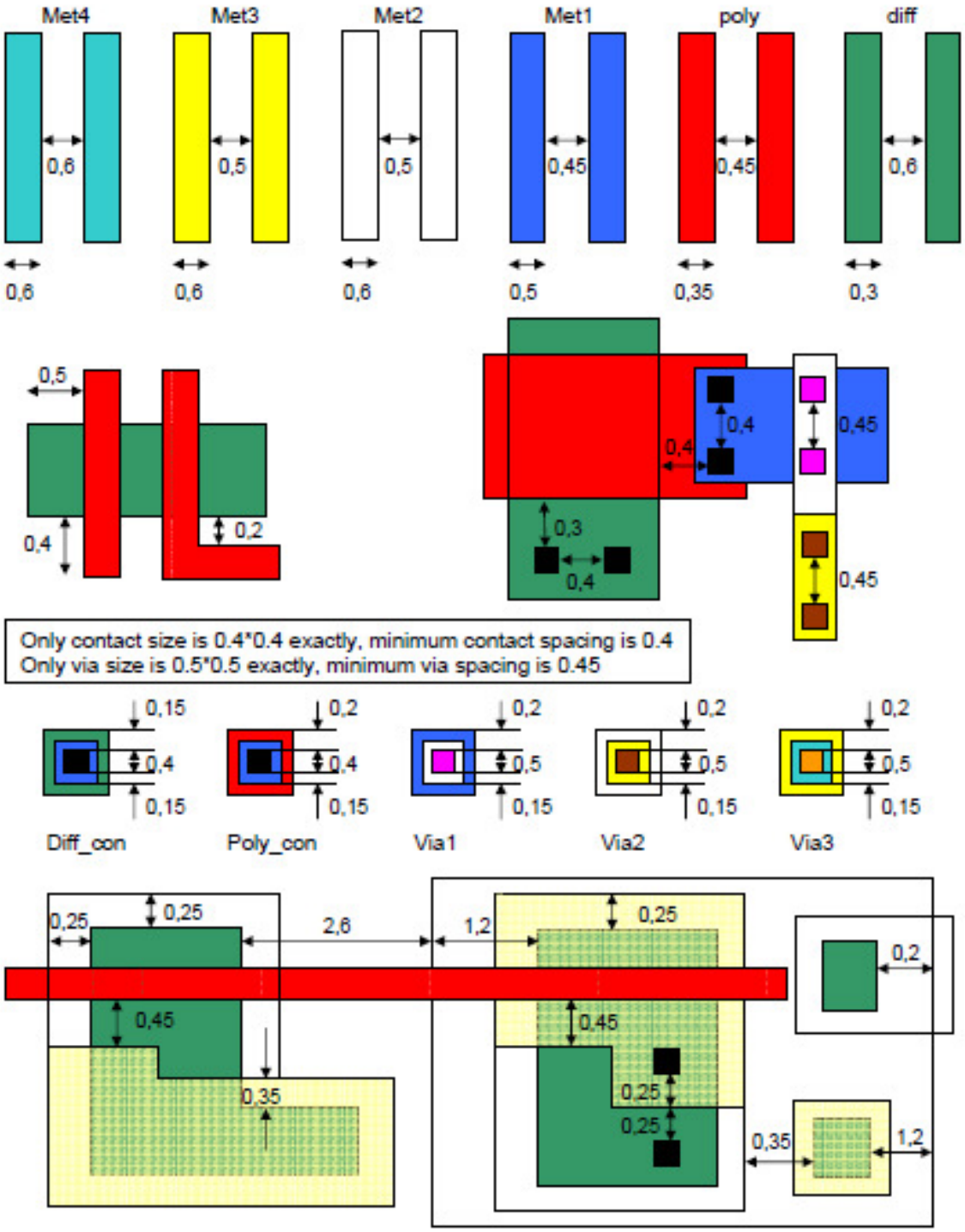
Latch-up prevention

1. All wells must have at least one contact connected to V_{dd}.
2. Place well and substrate contacts wherever possible.
3. Max. spacing between well/substrate contacts: 50 μm.

Note: The design rules and electrical parameters presented in this document are representative for the AMS c35b4 CMOS process, and they are intended for teaching purpose only.
By Johan Wernehag

Appendix B

Geometric Design Rule for 0.35µm CMOS Technology



Well (HOT_NTUB)

NWS1	spacing (different potential) (min notch 1.0)	3.0
NWW2	width	3.0

Active (DIFF)

ODW2	Width	0.3
ODS1	Spacing	0.6
ODC1	NTUB enclosure of NDIFF	0.2
ODC3	NDIFF to HOT_NTUB spacing	2.6
ODC4	NTUB enclosure of PDIFF	1.2
ODC5	PDIFF to NTUB spacing	1.2
ODC6a	PDIFF to NGATE spacing	0.45
ODC6b	NDIFF to PGATE spacing	0.45

Poly (POLY1)

POW2	GATE length of NMOS	0.35
POW3	Width	0.35
POS1	Spacing	0.45
POC1	POLY to DIFF spacing	0.2
POC2	DIFF extension of GATE	0.5
PO01	POLY extension of GATE	0.4

N-Select (NPLUS)

NPE1	NPLUS extension of DIFF	0.25
NPC1	NPLUS to DIFF spacing	0.35
NPC2	NPLUS to PGATE spacing	0.45
NPC3	NPLUS extension of NGATE	0.45
NPW1	NPLUS width	0.6
NPS1	NPLUS spacing	0.6

P-Select (PPLUS)

PPE1	PPLUS extension of DIFF	0.25
PPC1	PPLUS to DIFF spacing	0.35
PPC2	PPLUS to NGATE spacing	0.45
PPC3	PPLUS extension of PGATE	0.45
PPW1	PPLUS width	0.6
PPS1	PPLUS spacing	0.6

Contacts (CON)

COW1	Fixed CONT width	0.4
COS1	CONT spacing	0.4
M1E1	MET1 enclosure of CONT	0.15

Contact to active (DIFFCON)

COC1	DIFFCON to GATE spacing	0.3
COE1	DIFF enclosure of DIFFCON	0.15
COE3	PPLUS enclosure of PDIFFCON	0.25
COE4	NPLUS enclosure of NDIFFCON	0.25

Contacts to POLY (POLYCON)

COC2	POLYCON to DIFF spacing	0.4
COE2	POLY enclosure of POLYCON	0.2

Metal (MET1, MET2, MET3, MET4)

M1W1	Width	0.5
M1S1	Space	0.45
M2W1	Width	0.6
M2S1	Space	0.5
M3W1	Width	0.6
M3S1	Space	0.5
M4W1	Width	0.6
M4S1	Space	0.6

Via1, Via2 and Via3:

VIA1W1	Fixed VIA1 width	0.5
VIA1S1	Spacing to VIA1	0.45
VIA1E1	MET1 enclosure of VIA1	0.2
M2E1	MET2 enclosure of VIA1	0.15
VIA2W1	Fixed VIA2 width	0.5
VIA2S1	Spacing to VIA2	0.45
VIA2E1	MET2 enclosure of VIA1	0.2
M3E1	MET3 enclosure of VIA2	0.15
VIA3W1	Fixed VIA3 width	0.5
VIA3S1	Spacing to VIA3	0.45
VIA3E1	MET3 enclosure of VIA3	0.2
M4E1	MET4 enclosure of VIA3	0.15

Appendix C

SOIC 20 Ceramic Package Lead frame