Comparison of bandwidth reduction schemes in dynamic load modulation power amplifier architectures

Comparison of Bandwidth Reduction Schemes in Dynamic Load Modulation Power Amplifier Architectures

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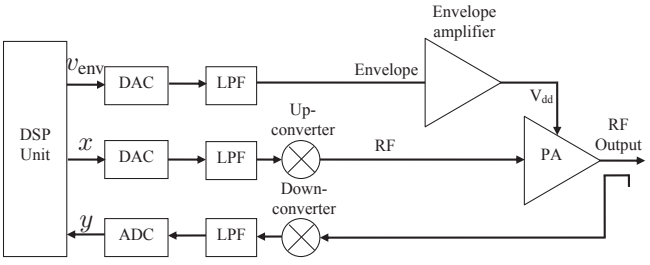
***Abstract*—This paper compares bandwidth reduction schemes for baseband control signals used in high efficiency power amplifier (PA) architectures, such as envelope tracking and dynamic load modulation (DLM). The baseband control signal used in such architectures usually has 3-4 times wider bandwidth than the modulated radio frequency (RF) signal. Such a wideband signal brings challenges for practical hardware design. In this paper, two bandwidth reduction schemes originally used in envelope tracking are applied on a DLM PA. The performance of both schemes are investigated by simulation. The results show that the bandwidth of the baseband control signal can be effectively reduced from 12.5 MHz to 4 MHz, while at the same time, maintaining a 49% average power-added and acceptable linearity.**

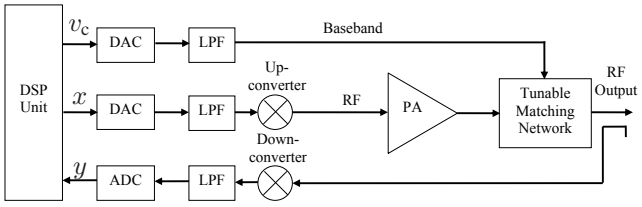
I. Introduction

Recently, different novel power amplifier (PA) architectures have been introduced to improve the average power-added efficiency (PAE). Envelope elimination and restoration (EER) [1], envelope tracking (ET) [2] and dynamic load modulation (DLM) [3] are some of the most promising examples. The basic principle of these PA architectures is to keep the operating point of the PA close to saturation by manipulating the power supply (ET and EER) or load impedance (DLM), for a wide range of power levels. The efficiency can therefore maintain high over a wider output power range and thus result in an improved average PAE also for signals having large peak-to-average power ratio (PAPR). At the same time, in order to compensate for the distortion introduced in these architectures, dedicated digital predistortion techniques [4], [5] have been proposed.

Envelope signal has wider bandwidth than RF signal itself which is 3-4 times in practice. Since the envelope is used to control the DC/DC converter in ET/EER or the load modulation network in DLM, its wide bandwidth creates challenges in hardware implementation. Simplified block diagrams for ET and DLM PA architectures are shown in Fig. 1, where x is the modulated RF signal and v_{env} and v_{c} are the baseband supply voltage and load control signals, respectively. It should be noted that although the architectures have different hardware implementations, they are quite similar from the signal processing point of view.



(a) Envelope tracking [4]



(b) Dynamic load modulation [5]

Fig. 1. Simplified block diagram of high efficiency power amplifier architectures.

In [6] and [7], two different techniques have been applied to reduce the bandwidth of the baseband control signal in ET PA architectures. Their experimental results showed the bandwidth of the baseband control signal can be effectively reduced almost to that of the modulated RF signal, while the average PAE can be kept relatively high.

In this paper, the bandwidth reduction schemes in [6], [7] are evaluated with a DLM PA [5]. The RF input signal is a 3.84 MHz WCDMA signal with 7 dB PAPR and the target reduced-bandwidth of the baseband control signal is chosen as 4 MHz. In principle, however, the bandwidth can be reduced arbitrarily. Simulation results show that both techniques can reduce the bandwidth of the baseband control signal to 4 MHz while the average power efficiency is kept more than 49%.

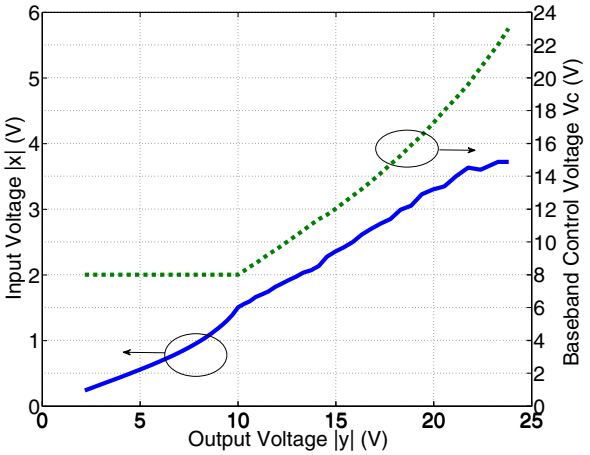


Fig. 2. Efficiency-optimized control function for dynamic load modulation PA architecture.

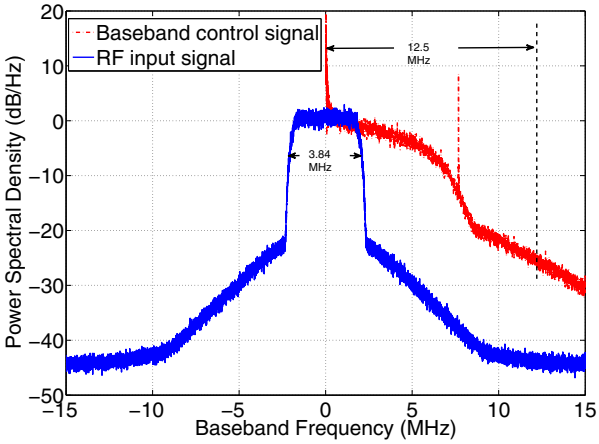


Fig. 3. Power spectra for the optimal baseband control signal v_c and RF input signal x.

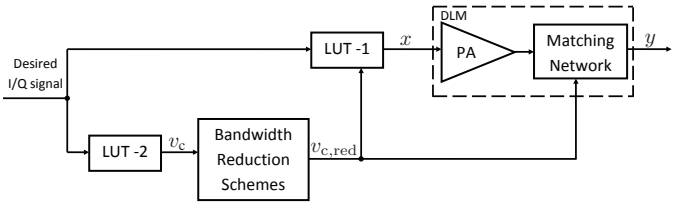


Fig. 4. DLM PA architecture with bandwidth reduction schemes.

II. Overview

A. Background for Dynamic Load Modulation PA Architecture

Similar to the ET architecture, the DLM PA architecture has two inputs, namely an RF input and a baseband control input. By co-controlling these two inputs, higher average PAE is possible to obtain. Given a desired output signal, the efficiency-optimized co-control of the baseband control voltage, v_c, and the RF input signal, x, can be derived from a single-input-dual-output polynomial fitting model [8]. The model is constructed from static measurements at which all combinations of the two input signals for a given desired output signal are first recorded, and only the combination which gives the highest efficiency is then selected [9]. The efficiency-optimized relationship of the desired output signal and the two input signals is shown in Fig. 2. From these static measurements combined with the desired WCDMA signal statistics, the maximum average PAE is estimated to be 54%.

The power spectra of the two optimal input signals is shown in Fig. 3. We can see that the bandwidth of the baseband control signal v_c which is defined by 99.99% of the signal energy is 12.5 MHz, and the bandwidth of the RF input signal x is 3.84 MHz. This wideband property of the baseband control signal is very challenging for hardware design. Bandwidth reduction schemes are thus needed for the baseband control voltage v_c.

B. General Design Considerations for The Reduced-Bandwidth Baseband Control Signal

The reduced-bandwidth baseband control signal can cause undesired distortion at the RF output and degrade the overall efficiency of the PA architectures. Therefore, when designing such a signal, some considerations need to be taken into account. First, the distortion introduced by the reduced-bandwidth control signal should be possible to be compensated for by appropriate predistortion techniques. This can be viewed as a design constraint for the baseband control signal [6] and is given by

$$v_{c,red} \geq v_c \tag{1}$$

where $v_{c,red}$ and v_c are the reduced-bandwidth and original baseband control signal, respectively. In addition to the requirements on distortion, the power efficiency should be maintained as high as possible when the signal bandwidth reduces.

III. Bandwidth Reduction Schemes

In this section, the two different bandwidth reduction schemes in [6], [7] are presented. Both schemes have been previous successfully applied to the ET PA architectures. In this paper, we investigate the general effectiveness of these schemes by applying them on the DLM PA architecture.

A general block diagram of the efficiency-optimized DLM PA architecture with bandwidth reduction schemes is shown in Fig. 4, where LUT-2 is the efficiency-optimized function for the baseband control signal v_c as shown in Fig. 2. The bandwidth reduction schemes applied after the LUT-2 are used to construct the reduced-bandwidth baseband control signal $v_{c,red}$. LUT-1 is a two-dimensional static look-up table which is derived from static power sweep measurements of the baseband control signal and RF input signal. Given the reduced bandwidth baseband control signal $v_{c,red}$ and the desired I/Q signal, LUT-1 can simply be seen as the inverse function of the PA.

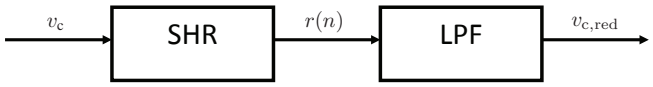


Fig. 5. Shift register method in [7]. SHR and LPF represent shift register and low-pass filter, respectively.

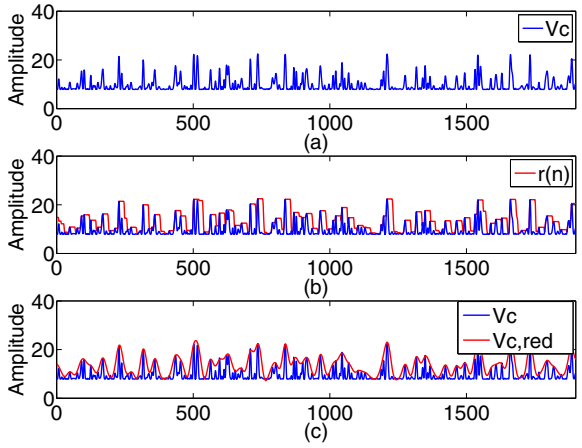


Fig. 6. Reduced-bandwidth baseband control signal $v_{c,red}$ with shift register method in [7].

The first bandwidth reduction scheme was proposed in [7] and is shown in Fig. 5. In this scheme, a shift register with delay D is implemented as a maximum filter and used to predict the peaks of the original baseband control v_c, which can be written as

$$r(n) = \max\left[v_c(n), v_c(n+1), v_c(n+2)\cdots v_c(n+D)\right] \quad (2)$$

where $r(n)$ is the reference signal at the output of the shift register. It operates on blocks of D samples and is constant for every D samples. The order D needs to be chosen carefully and the resulting reduced-bandwidth baseband control signal can thus satisfies (1). The reference signal $r(n)$ is then applied to a low-pass filter (LPF) to produce a slow time-varying signal, which is the reduced-bandwidth baseband control signal $v_{c,red}$. Note that, when using this bandwidth reduction method, the same delay D needs to apply at the RF branch before LUT-1 in Fig. 4 in order to synchronize both the RF and baseband control signals. The time domain waveforms for the original and reduced-bandwidth baseband control signal and the reference signal are shown in Fig. 6. As shown in Fig. 6, the reduced-bandwidth baseband control signal is larger than the original baseband control signal for all the samples which satisfies (1).

The second bandwidth reduction scheme was also proposed for the ET PA architecture. The bandwidth of the baseband control signal is reduced from 20 MHz to 5 MHz, and the overall PAE is about 50% [6]. The block diagram for this scheme is shown in Fig 7. The original baseband control signal v_c is first low-pass filtered and then subtracted from itself to get the difference signal $v_{c,diff}$. This difference signal

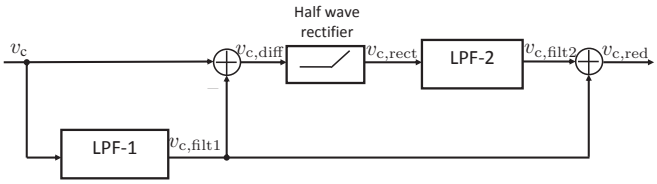


Fig. 7. Rectifier-based method in [6]. LPF-1 is a low-pass filter with cut-off frequency R MHz and LPF-2 is a low-pass filter with cut-off frequency $2R$ MHz.

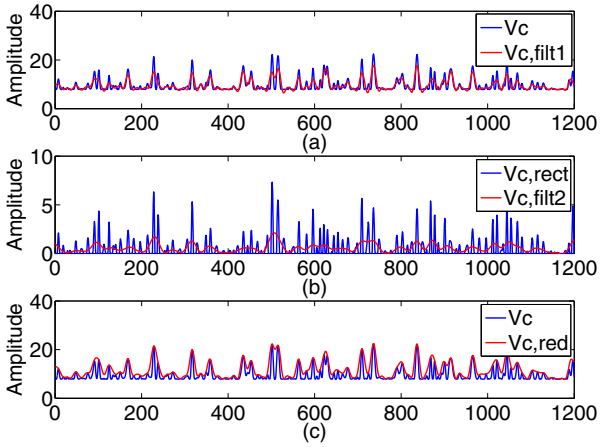


Fig. 8. Reduced-bandwidth baseband control signal $v_{c,red}$ with rectifier-based method in [6] after 10 iterations.

is then passed through a half-wave rectifier. The rectified residue signal $v_{c,rect}$ is low-pass filtered again and this filtered signal $v_{c,filt2}$ is added back to the filtered baseband control signal $v_{c,filt1}$ to produce the reduced-bandwidth control signal $v_{c,red}$. However, the reduced-bandwidth signal derived from this process still cannot satisfy (1), and several iterations are therefore needed until the reduced-bandwidth signal $v_{c,red}$ does not violate (1) [6]. In our case, 10 iterations are needed. The signals in different stages of the scheme are shown in Fig. 8.

IV. Simulation Results and Complexity Discussion

A. Simulation Results

Both bandwidth reduction schemes [6], [7] have been verified by simulation in Matlab®. The simulation setup is shown in Fig. 4 where the DLM block is represented by static measurements collected from the DLM PA architecture [5]. The maximum output power of this DLM PA architecture is around 7 W. As mentioned in Section II, in order to maximize the efficiency and minimize the distortion at the output, the RF input signal x needs to be modified according to the reduced-bandwidth signal $v_{c,red}$. In this case, given the reduced-bandwidth baseband control signal $v_{c,red}$ and the desired output signal, a two-dimensional interpolation is used to derive the new predistorted RF input signal x. In principle, based on this new predistorted input signal x and the reduced-bandwidth

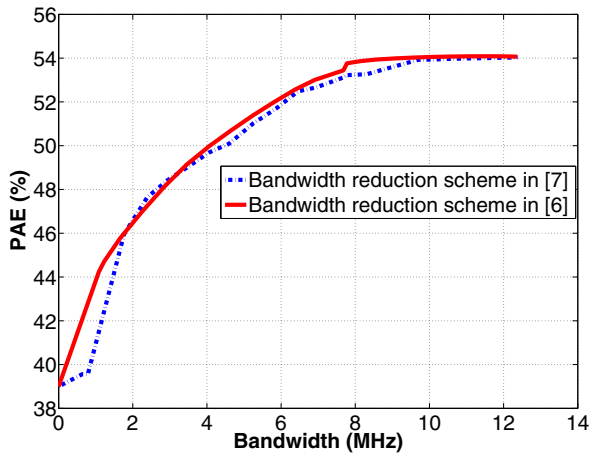


Fig. 9. Average PAE versus different baseband control voltage bandwidths for the two bandwidth reduction schemes.

baseband control signal $v_{\mathrm{c,red}}$, the nonlinear distortion at the output should be very little and can be ignored.

Since the linearity in the simulation is almost perfect, we are only interested in the effects of bandwidth reduction on the average PAE. The average PAE comparison is shown in Table. I. The bandwidth reduction scheme in [6] gives 0.5% higher PAE for the same envelope bandwidth reduction.

More importantly, according to the statement earlier, the bandwidth reduction scheme should have as small average PAE degradation as possible when the bandwidth of the baseband control signal reduces. Fig. 9 shows the average PAE comparison vs. different reduced baseband control signal bandwidths. From 8 MHz to 12.5 MHz, the PAE remains almost the same for both schemes. Down to 4 MHz, the average PAE is kept over 49 %. The PAE only drops dramatically under 2 MHz. Note that, the zero-bandwidth case can be seen as the traditional PA architecture case where the load impedance is fixed (no load modulation), and the PAE is just 39%.

TABLE I
EFFICIENCY COMPARISON WHEN THE BASEBAND CONTROL SIGNAL BANDWIDTH IS REDUCED TO 4 MHZ.

Methods	Average PAE [%]
Bandwidth reduction scheme in [7]	49.5
Bandwidth reduction scheme in [6]	50

B. Complexity Discussion

In practice, the reduced-bandwidth signal should be updated in real-time. It is therefore important that the bandwidth reduction schemes have low computational complexity. The scheme in [7] employs a shift register. The order calculation of this shift register may involve very high complexity, as the step size of the order is incremented in small steps. At each step the reduced bandwidth signal needs to be compared with the original control signal to verify if it satisfies (1). The scheme in [6] needs iteration to satisfy (1), however, each iteration involves very low complexity. In our application, it is noticed that the scheme in [6] has overall less complexity.

V. CONCLUSION

This paper has investigated two existing bandwidth reduction schemes for use in DLM PA architectures. The results showed they can be used to reduce the bandwidth of the baseband control signal effectively without much PAE degradation, and the scheme in [6] shows better results with less complexity.

ACKNOWLEDGMENT

This research has been carried out in the GigaHertz center in a joint research project financed by the Swedish Governmental Agency of Innovation Systems (VINNOVA), Chalmers University of Technology, Ericsson AB, Infineon Technologies AG, and NXP Semiconductors BV.

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