Aging- and annealing-induced variations in Nb/Al–AlO_x/Nb tunnel junction properties

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In this paper, we present studies of room temperature aging and annealing of Nb/Al–AlO_x/Nb tunnel junctions with the size of 2–3 μm^2. We observed a noticeable drop of junction normal resistance R_n unusually combined with increase in subgap resistance R_j as a result of aging. Variation in both R_n and R_j are subject to the junction size effect. An effect of aging history on the junction degradation after consequent annealing was discovered. Discussion and interpretation of the observed phenomena are presented in terms of structural ordering and reconstruction in the AlO_x layer, driven by diffusion flows enhanced due to stress relaxation processes in the Al layer interfacing the AlO_x layer. © *2011 American Institute of Physics*. [doi:10.1063/1.3532040]

I. INTRODUCTION

For many years, since introduction of superconducting Nb/Al–AlO_x/Nb tunnel junctions,[1,2] variation in their properties under room temperature aging and annealing at elevated temperatures has been extensively discussed.[3–10] The interest to this subject was constantly supported by applications[11,12] and related to that life-time and reliability questions. An increase in the junction normal state resistance R_n (decrease in critical current I_c) followed by further degradation of its characteristics at even higher temperatures, seemed to be a commonly agreed trend. General understanding behind the increase in the normal state resistance of Nb/Al–AlO_x/Nb junctions is that during the annealing at lower temperature range, below 250…275 °C, the tunnel barrier gets thicker either due to (additional) oxidation of the Al layer by chemisorbed oxygen,[7,13] or by adsorbed water molecules (hydroxyl groups).[3,14–16] This was supported by Raman spectroscopy study,[17] showing decay of Al–OH peak and corresponding rise of Al–O peak as a result of Nb/Al–AlO_x/Nb junction annealing. At higher annealing temperatures, above 250…275 °C, AlO_x barrier apparently grows due to diffusion of oxygen through the junction's counter electrode.[3,4]

However, there are experimental facts, which do not fit the suggested trend and cannot be explained within the same approach. In the number of studies, unusual drop of R_n value of Nb/Al–AlO_x/Nb (Refs. 8–10) and Al/Al–AlO_x/Al (Refs. 15, 18, and 19) junctions with annealing or aging has been observed.

In this study, we experimentally observed a reduction in R_n of Nb/Al–AlO_x/Nb junctions with aging similarly to Refs. 8–10. Unusually, this R_n reduction was accompanied with an increase in the subgap resistance, R_j. Furthermore, we observe the junction size affecting the R_n and R_j changes with aging. In addition, we experimentally detect a difference in persistence of the Nb/Al–AlO_x/Nb junctions recently fabricated and long time aged at room temperature. These phenomena hardly could find explanation within the concept of further oxidation of AlO_x barrier layer with adsorbed oxygen or water vapor. Below, we present a discussion in attempt to interpret all mentioned effects related to aging and annealing in terms of diffusion and stress-related processes in the vicinity of the tunnel barrier.

II. EXPERIMENT

The Nb/Al–AlO_x/Nb junctions studied in this work have been processed using dedicated equipment placed in class 100 clean-room environment. The junctions used in this studies were fabricated at the different stages of the superconductor/insulator/superconductor (SIS) mixer development for the APEX Band 3 (385…500 GHz) receiver, which has recently been installed at the APEX telescope.[20,21] The nominal junction areas were $A=3$ μm^2 (wafers R5.1, R6.1, R7.1, R8.2, and D1.2) and $A=2$ μm^2 (wafer D1.2), with the ±10% typical spread of the junction size due to the processing-specific variation. The Nb/Al–AlO_x/Nb trilayer growth and processing parameters were the same for all wafers discussed in the paper.

The tunnel junctions were fabricated on 1 in. square z-cut crystal quartz substrates. All of the junction structure layers were deposited in a cluster magnetron sputtering system, having two deposition chambers connected to the vacuum load-lock through a transport module. The four vacuum chambers of the sputtering system are pumped by turbo pumps backed by multistage Roots pumps, providing dry vacuum environment at the base pressure level below 1×10^{-7} Torr. The sample transfer between the chambers is complemented by Argon gas counterflow at about $5\times10^{-2}…1\times10^{-1}$ Torr, which "rinses" the sample on its loading path, ensuring minimum water vapor and oxygen content in the sputtering chamber.

Etching of the Nb and Al–AlO_x layers were carried out in a dual-chamber reactive ion etching (RIE) system, where each etching chamber was dedicated to either fluorine or chlorine plasma chemistries. Base pressure in the both etching chambers was at the level below 4×10^{-7} Torr.

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The $Nb/Al-AlO_x/Nb$ trilayer was grown in single vacuum run by means of dc magnetron sputtering. All patterns were defined by conventional contact photolithography. The base Nb electrode, 200 nm thick, was deposited at 0.9 nm/s rate followed by about 7 nm Al deposited at 0.3 nm/s rate. The fresh Al surface was exposed to pure oxygen at room temperature and at a pressure of 1.7×10^{-2} mbar for 15 min to form the AlO_x tunnel barrier. Finally, 100 nm thick Nb counter electrode was deposited under the same conditions as the base electrode. The base electrode pattern has been etched through the $Nb/Al-AlO_x/Nb$ trilayer by a sequence of CF_4+O_2 for Nb and Cl_2 for $Al-AlO_x$ RIE, correspondingly. The junction pattern was defined by RIE process with a stop at $Al-AlO_x$ layer. Anodization[22] with voltage up to 13 V was followed by a deposition of 250 nm thick SiO_2 by means of reactive rf magnetron sputtering; the SiO_2 layer was lifted-off forming interlayer insulation. A 400 nm thick Nb wiring layer was deposited by dc sputtering and followed by RIE. The contact pads were formed by lift-off of the Nb (100 nm)/Pd (150 nm) bilayer.

Each fabricated wafer contained 203 SIS mixer chips, out of which, 30 where connected to the wafer external contact pads, allowing dc characterization of the junctions before dicing wafer into single mixer chips. Each chip had a pair of junctions connected in parallel.[20] In this work, for junction characterization, we measured their current-voltage characteristics (IVC) at 4.2 K. Analyzing the recorded IVCs, we extracted the values of junction normal resistance, R_n, which corresponds to the resistance of normal electrons tunneling through AlO_x barrier at bias voltage higher than the junction superconducting gap voltage, V_g. Another important parameter is the subgap resistance R_j, which corresponds to the resistance of quasiparticles tunneling through the barrier at bias voltages below V_g. Normal state resistance R_n is considered as a measure of transparency of the tunnel barrier transparency. There are very little of quasiparticles in niobium at 4.2 K. Therefore, the R_j value is very sensitive to the presence and quantity of the tunnel barrier defects and hence used as an indicator of the $Nb/Al-AlO_x/Nb$ tunnel junction quality. We estimated R_n as an average resistance measured in the range of 0.9 $V_{max}\ldots V_{max}$, where V_{max} is the maximum bias voltage value during recording of IVCs (in this work, typically 6…8 mV); R_j as an average resistance measured in the range of 0…1.7 mV at the subgap branch of the IVC.[23]

As fabricated, all wafers demonstrated high-quality of the junctions and yield of about 90%. The junction parameters are $R_nA\simeq 20\ \Omega\ \mu m^2$, $R_j/R_n\simeq 15\ldots25$, and the superconducting gap voltage $V_g\simeq 2.87$ mV.

The aging of the wafers carried out in a controlled environment at room temperature 19…23 °C in an air-conditioned laboratory room. The wafers were stored in standard antistatic trays and no additional measures were taken to protect the wafers from environmental factors during the storage period. The junction IVCs were recorded and changes in their R_n and R_j values due to aging were analyzed as a function of their area. Assuming the AlO_x barrier of $Nb/Al-AlO_x/Nb$ trilayer is uniform across the wafer area, the measure for the junction area is the recorded as-fabricated values of the R_n.

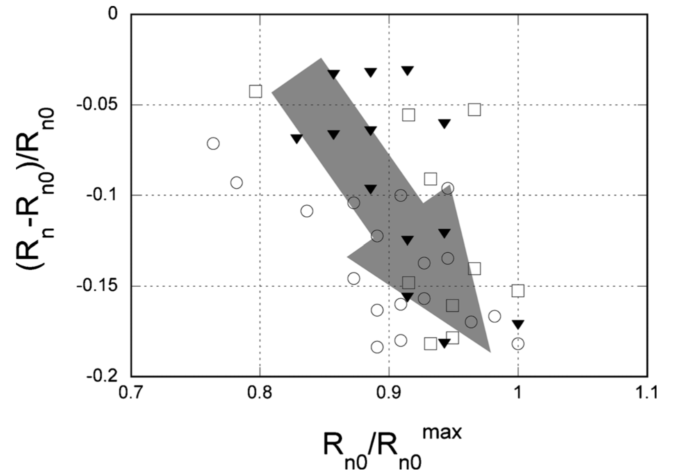

FIG. 1. Room temperature aging effect on the normal resistance of the junctions from wafers R5.1 (*circles*, aged for 655 days), R6.1 (*squares*, 597 days), and R7.1 (*triangles*, 428 days). R_{n0}, R_{n0}^{max}, and R_n-junction normal resistance as-deposited, maximal for the given wafer and after aging, correspondingly. Gray arrow illustrates the trend and guides eye.

The junction annealing experiments were performed as a sequence of hot-plate baking steps at the range of temperatures 120…250 °C for 1 h in the atmosphere of room air with $42\pm-2\%$ relative humidity, with the temperature increased by a 10 °C of increment at each step. Each baking step followed by recording of the junction IVCs.

III. RESULTS AND DISCUSSION

Junctions from different wafers experience similar type of changes after long aging at room temperature. The normal state resistance of the junctions decays, which agrees with results reported in Refs. 8–10. Furthermore, we have observed the junction size effect on R_n aging behavior, similar to that, reported in Ref. 10. Figure 1 depicts relative changes in the junction normal resistance, defined as $(R_n-R_{n0})/R_{n0}$, versus their normalized values of as-fabricated normal resistances R_{n0}/R_{n0}^{max} normalized by R_{n0}^{max}; here R_{n0}^{max} is maximum R_{n0} for the given wafer. There is a noticeable tendency that the more resistive junctions experience higher relative drop of the normal resistance. That indicates that the smaller area junctions exhibit relatively stronger decrease in their normal resistance due to aging as compared to the junctions of a bigger size on the same substrate.

The reduction in R_n due to aging and the junction size effect are attempted to be explained in Refs. 8–10 by suggesting out-diffusion of hydrogen, trapped in the niobium electrodes during the junction fabricating. It was speculated[10] that "the Nb work function increases due to the hydrogen inclusion, resulting in the increase in the barrier height." Following this explanation, one should expect similar behavior of the junction subgap resistance R_j with aging. However, we observe the tendency just opposite to the R_n changes: R_j increases with aging (Fig. 2). Figure 3 shows a summary of the relative changes in junction subgap resistance, defined as $(R_j-R_{j0})/R_{j0}$, versus normalized as-fabricated normal resistances R_{n0}/R_{n0}^{max}. The wafers R5.1, R6.1, and R7.1 demonstrate a similar tendency of the R_j increasing and the results are earlier presented in Ref. 24. It is worth to notice that the

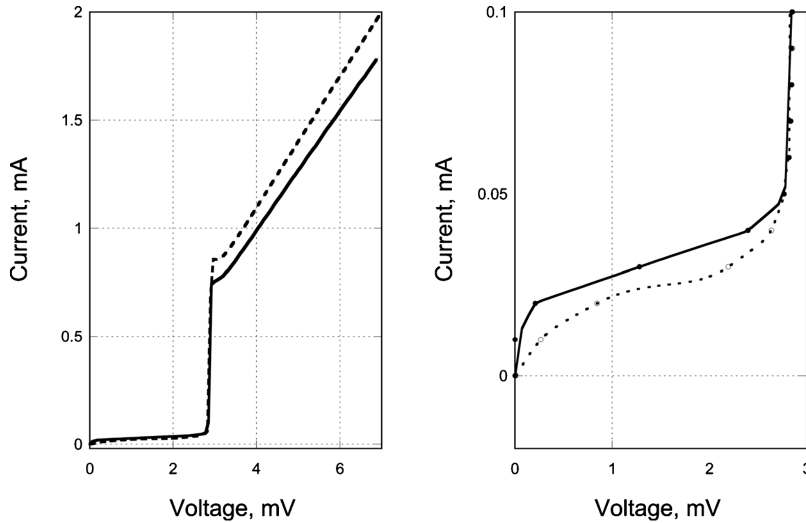

FIG. 2. Current-voltage characteristic of a tested junction before (*solid line*) and after aging for 63 days (*dotted line*), wafer D1.2, chip 16 (nominal junction size 3 μm^2). Plot to the right shows subgap branch of the IVC at a higher magnification.

wafer D1.2 (measurements at Fig. 3) experienced about an order shorter aging, compared to the wafers R5.1, R6.1, and R7.1 (measurements at Fig. 1). While aging effect on R_j is clearly seen at the moderate aging times, the R_n changes are nearly not noticeable at shorter aging time. However, being exposed to annealing at 120 °C for 30 min, the junction normal resistance R_n changes, Fig. 4, showing the similar junction size effect and very much alike as after the long room temperature aging (Fig. 1). This points out to the fact that aging processes affecting R_j occur at a shorter time scale than those, causing R_n changes, and that fact could hardly be explain within the concept of hydrogen-induced aging effects.

After room temperature aging, the junctions were annealed at elevated temperatures, which affects their normal and subgap resistances as presented in Fig. 5. The results are partially presented in Ref. 24. The changes, both for R_n and R_j, follow the same trend for the junctions experienced room temperature aging with different durations (batches R8.2 and D1.2). However, depending on the aging history, the junctions were able to survive annealing up to different temperatures. Figure 6 compares the fraction of the failed junctions with respect to the annealing temperature for the wafers that were subject to preaging with different duration. Under the term "failed junction," we consider either a short-circuited junction or a junction with sufficiently degraded IVC. From this plot, we could suggest that the junctions subjected to a longer room temperature aging survive higher annealing temperature. Compared to the earlier presented data,[3,4,6,7] the longer preaged junctions (batch R8.2) demonstrate similar ability to persist annealing conditions. Worth mentioning though, the junctions used in the present work have substantially thinner tunnel barrier, then those reported in Refs. 3, 4, 6, and 7. This makes the junctions more susceptible to the intrinsic stress. This is discussed in more detail further in the paper.

In attempt to explain the observed connection between the aging and the annealing behavior of Nb/Al–AlO_x/Nb junctions, we would like to look at the tunnel barrier structure and its evolution at atomic scale. Any direct studies of the processes in AlO_x tunnel barrier and adjacent to it layers

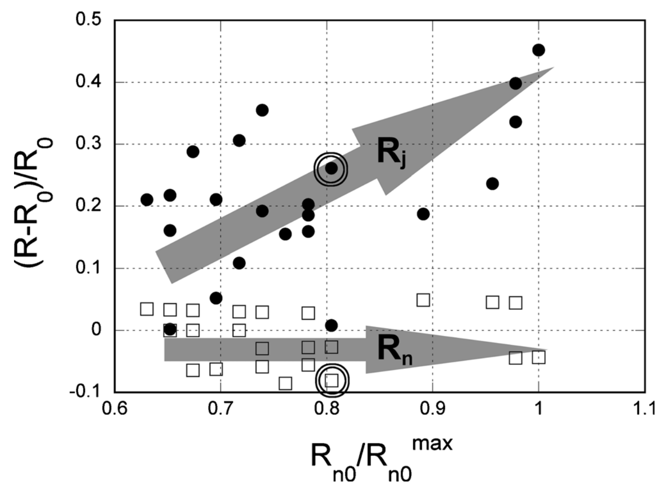

FIG. 3. Room temperature aging effect on the subgap (*circles*) and normal resistance (*squares*) of the junctions from the wafer D1.2 (aged for 63 days). R_{n0}^{max}, and R_n-junction normal resistance as-deposited, maximal for the given wafer and after aging, correspondingly. Gray arrows illustrate the trend and guide eye. The data points marked with rings correspond to the junction, which current-voltage characteristic presented at the Fig. 2.

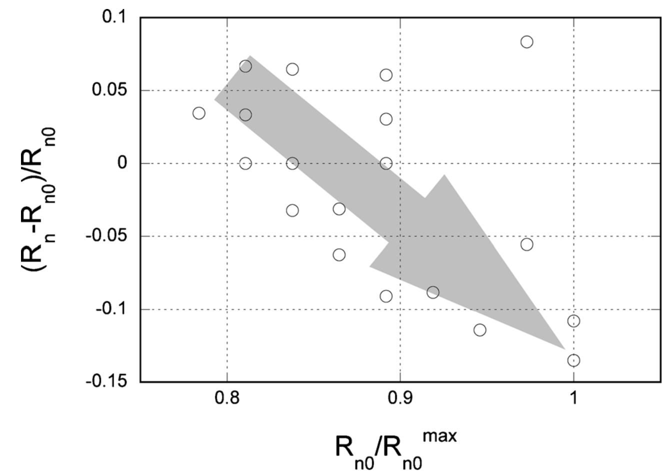

FIG. 4. Effect of annealing at 120 °C on the normal resistance of the 3 μm size junctions from the wafer D1.2 (aged for 63 days before annealing). R_{n0}^{max} and R_n-junction normal resistance as-deposited, maximal for the given wafer, and after aging, correspondingly. Gray arrow illustrates the trend and guides eye.

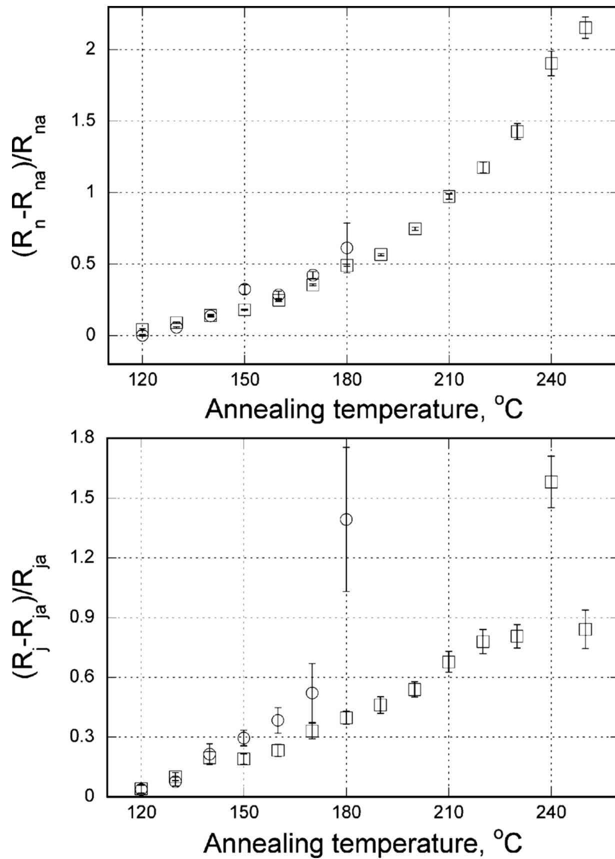

FIG. 5. Annealing effect on the normal and subgap resistance of the junctions from the wafer D1.2 (aged for 63 days before annealing, *circles*) and the wafer R8.2 (aged for 391 days before annealing, *squares*). R_{na}, R_n, and R_{ja}, R_j-junction normal and subgap resistance after room temperature aging and consequent annealing.

are extremely difficult, as it is a structure of about one nm thick, sandwiched in between rather thick (200…500 nm) layers of niobium. However, in this discussion, we could greatly benefit from the recent results on *in situ* studies of the growth kinetics and crystal state of the ultrathin oxide film over the atomically clean single-crystal Al surfaces at the low temperatures between 80 °C and 380 °C, Refs. 25–27.

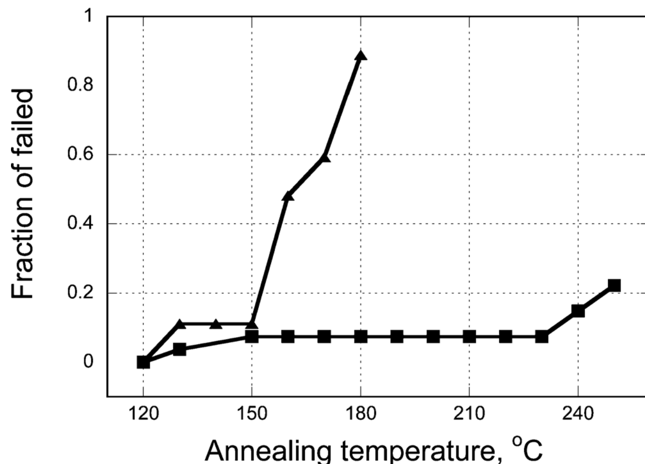

FIG. 6. Annealing temperature effect on the fraction of failed junctions, which experience long room temperature aging (wafer R8.2, aged for 391 days, *squares*), compared to that of junctions, experienced shorter aging (wafer D1.2, aged for 63 days, *triangles*).

The conditions of the Al-oxide film growing in Refs. 25–27 largely resemble the conditions and thus the properties of the AlO_x tunnel barrier grown over the Al layer during fabrication of $Nb/Al-AlO_x/Nb$ junctions. The authors of these papers conclude that various processes of structural ordering in the oxygen sublattice of AlO_x, namely, an annihilation of the vacancy-type defects and even crystallization of initially amorphous oxide layer,[25,27] occur in the above mentioned interval of temperatures and AlO_x thickness about 1 nm. Furthermore, the reduction of the number of the electronic defect states within the oxide band gap takes place at the same interval of temperatures and AlO_x thickness of about 1 nm.[27] Applying these conclusions to the $Al-AlO_x$ layer of the tunnel barrier, we speculate that the same processes should certainly cause a decrease in the "leakage" component of the subgap current. This could explain the observed increase of R_j after room temperature aging. From the other hand, the structural ordering reduces the material volume,[25,27] and consequently causes thinning of the tunnel barrier and hence could explain a decrease of the R_n after a long aging.

Within the very same concept, the difference in the time scales of changes for both R_j and R_n could also be explained. The process of curing of minor structural defects that should lead to a raise of R_j, requires relatively little diffusion to occur, as discussed above. Whereas decreasing of R_n requires sufficient rearrangement of the film structure and diffusion processes in the AlO_x film being developed in a very much longer time scale.

The studied room temperature aging of the $Nb/Al-AlO_x/Nb$ junctions occurs at noticeably lower temperature as compared to the conditions of ultra-thin oxide film growth presented in Refs. 25–27. Nevertheless, we believe that even the aging effects could be explained through the AlO_x layer structure ordering. However, in the case of the room temperature aging, a nonthermal enhancement of diffusion and consequent curing of the structural defects should exist. An indication of such nonthermal diffusion enhancement mechanism comes from observed dependence of R_n and R_j on junction area. The fact that the smaller junctions demonstrate a stronger aging effect points out to the intrinsic stress that always is accumulated in Nb film of the wiring layer during its growth. Our fabricating process is calibrated in such way that the wiring layer Nb film typically characterized by slight compressive stress of about 100 MPa.

In order to understand how the stress affects the tunnel junction, we assume perfect adhesion at the $Nb/Al-AlO_x/Nb/Nb_{wiring}$ interfaces and account that the yield strength value is 100…200 MPa for a deposited Al material,[28] that is comparable with the intrinsic stress of the niobium film. For Al, the room temperature corresponds to a moderate homologous temperature $\Theta_{Al}=T/T_m^{Al}\simeq 0.32$, where T_m^{Al} is melting temperature of Al. Altogether, this leads to a conclusion that the intrinsic stress in Nb wiring layer could be partly relaxed via creep deformation (stress relaxation process) of the aluminum layer of $Nb/Al-AlO_x/Nb$ trilayer at room temperature. This hypothesis is supported by an experimental observation of the stress relaxation in a free-standing microstructures made of sputtered Al films occurred at room temperature, when originally loaded with a 50 MPa

stress.[29] Furthermore, whatever mechanism of stress relaxation process takes place in Al layer of Nb/Al–AlO_x/Nb trilayer, either diffusion creep,[30,31] or dislocation climb creep,[31,32] it should be associated with diffusional flows of vacancies in the Al layer. Vacancy flow in the vicinity of the AlO_x layer provides an additional diffusion path that in a nonthermal way enhances diffusion needed for structural ordering of AlO_x barrier layer.

Moreover, following the same concept, the difference in temperature dependence of the failed junctions ratio after annealing could be explained. The diffusion ordering of the AlO_x layer is far more slower than deformation (stress relaxation) of the Al layer. At higher annealing temperature, the Al layer deformation occurs quicker and tears AlO_x layer out, whereas the diffusion reconstruction cannot catch up creep of Al layer. Alternatively, a very long room temperature aging allows the major part of the Al layer relaxation to happen at low deformation speed, making the AlO_x layer reconstruction able to follow. Consequently, the annealing at elevated temperatures does not lead to tearing oxide layer out up to noticeably higher temperatures.

A noticeable data points' scattering in Figs. 1, 3, and 4 can be attributed to the stochastic character of the diffusion process for each junction. We assume that at further stages of the diffusion aging, it should converge to some more pronounced common dependence. Certainly, possible local nonuniformities in distribution of the defects and intrinsic stress in the vicinity of the junction should contribute to the scattering of the data points.

We believe, the suggested junction aging mechanism should be applicable to any system like Nb/Al–AlO_x/Nb tunnel junctions. However, specific details of fabricating process (film stress, composition of residual gas in the deposition system, etc.) largely define a balance between aging driven by the diffusion ordering and annealing effects caused by further oxidation of the AlO_x barrier by the adsorbed oxygen or hydroxyl groups. In particular, low residual water content (see the description of the deposition system above) is crucial to be able to observe relatively advanced diffusion ordering stage for the fabricated junctions, as presented in the paper.

IV. CONCLUSION

We have studied room temperature aging of Nb/Al–AlO_x/Nb junctions of a 2…3 μm^2 size. We observe reduction in the normal resistance R_n and increase in the subgap resistance R_j of the tested junctions as a result of room temperature aging. Changes in R_j occur at sufficiently shorter time scale than that of R_n. Aging effects for both R_n and R_j are subject to the junction size effect. Finally, we observed effect of aging history on the temperature dependence of the junction failure after consequent annealing.

We suggest that the observed junction aging and annealing behavior could be explained by diffusional ordering and structural reconstruction in the AlO_x layer. The diffusion driving the structural ordering and reconstruction of the AlO_x tunnel layer is enhanced due to the intrinsic stress relaxation (creep) processes in the underlying Al layer.

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