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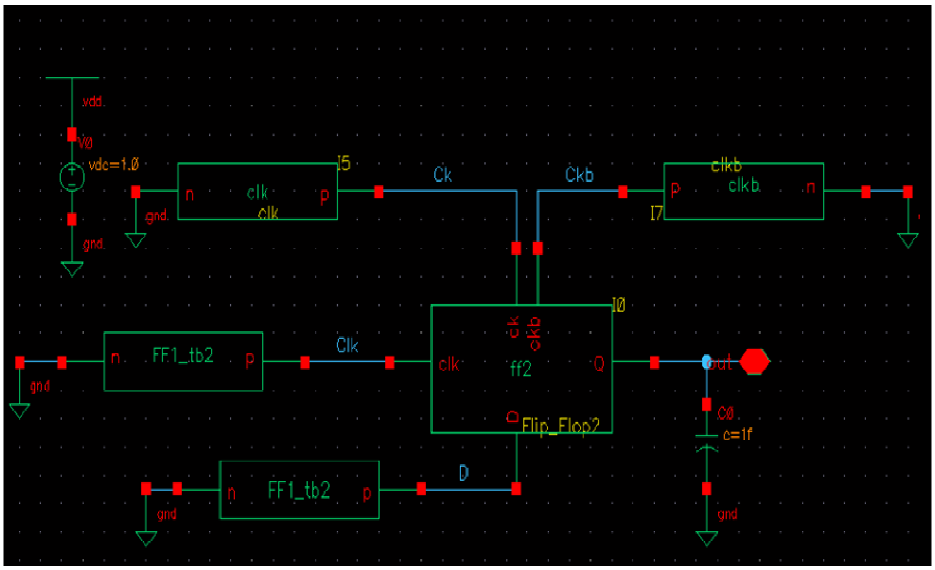

Logic Gates Switching Harmonics

Master of Science Thesis in Integrated Electronic System Design

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Göteborg, Sweden, August 2010

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Cover:
Test bench of Modified C^2MOS Latch

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Abstract

This report deals with the study of spectrum generation from logic circuits, in order to better understand how to suppress the generation of high harmonics, especially in a given frequency band. It is well known that signals with fast edges contain more energy at higher-frequency spectral components [3]. However, existing closed-form expressions become increasing unwieldy to cover high order harmonics (10th harmonic and above) [1]. Furthermore, circuit simulations of such waveforms are difficult, and certain insights are needed to correctly interpret the simulation results.

For tool setup simulations of simple inverter were performed with Cadence Spectre simulator using 65 nm and 130 nm process technologies and data points were transferred to Matlab to plot the FFT spectrum of switching waveforms.

Three different flip-flop structures PowerPC 603 Master-Slave Latch, modified C^2MOS Latch, hybrid-latch flip flop (HLFF) were also designed and simulated using 130nm process technology. Comparison between three flip flop structures was also done in terms of time delay, power dissipation and FFT spectrums of switching waveforms. Performance of hybrid-latch flip flop (HLFF) was best as compared to other two structures

Keywords: BSIM transistor Model, Cadence Spectre, PowerPC 603 Master-Slave Latch, modified C^2MOS Latch, hybrid-latch flip flop (HLFF)

Acknowledgments

First I would like to thank Professor Lars Svensson for giving me the chance to work on this project and for all the help and support he has given me along the way. I would also like to extend my appreciation for his patience guidance in various problems in my thesis. I would also like to thank Lars Kollberg for his work in tool set-up during my thesis.

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1 Introduction

IC designs are getting complex with time and number of transistors on a small silicon chip area is increasing day by day. When we simulate a logic circuit based on CMOS technology, a large number of transistor parameter like body effects, short channel effects, DIBL (Drain induced barrier lowering) effects, leakage currents, capacitances inside different terminals and many other parameters affect the simulation results. Modern IC design tools model all these parameter to provide the accurate simulation results and fortunately as designers we don't need to know all these parameters. Highly integrated wireless communication systems require accurate estimation of harmonic contents because radio performance is influenced by the switching harmonics from the digital parts. Quality of transistor model and nature of input signal influences the estimation of harmonic contents of switching waveforms. Switching noise is a complex problem in integrated circuits and thus harmonic contents of switching waveforms are an important study in digital integrated circuits designs and are helpful in accurate estimation of the noise contents of signal.

1.1 Thesis Focus

The main focus of this thesis is the study of influence of transistor model quality and nature of input signal on harmonic contents of the spectrum of three different CMOS Flip flop structures PowerPC 603 Master-Slave Latch, modified C^2MOS Latch, hybrid-latch flip flop (HLFF) logic waveforms. A comparison between these three Flip flop structures was also done in the form of time delays, power dissipation and roll off in the spectrum of logic switching waveforms. Input signal is also important in getting steeper roll off in the spectrum switching waveforms. A comparison between 65 nm and 130 nm process technologies was also made on the basis of spectrum of logic switching waveforms. 65 nm process technology uses BSIM3 transistor model while 130 nm process technology uses BSIM4 transistor model. BSIM4 model is an extended version of BSIM3 model.

1.2 Limitations

Spectre is an accurate and reliable tool for simulations and Matlab allows more flexible spectrum analysis. So data points were transferred from Cadence Spectre to Matlab for spectrum analysis.

1.3 Report disposition

This report is mainly divided into three parts. First part is based on the theoretical background for simulations and flip flops study. Second part is based on simulations and results and third part is based on discussion and conclusions.

1.4 Report target group

The intended reader for this master thesis report is a student or an engineer with basic background in electronics and simulation software like Cadence Spectre and Matlab.

2 Circuit Simulations

For circuit simulations the availability of accurate, reliable and fast circuit simulation tools is necessary. Spice circuit simulator was the first computer-aided design (CAD) tool which got the world wide attention [5]. SPICE was developed at University of California at Berkeley. University of California at Berkeley developed three different versions of Spice simulation tools over the years and they are called Spice-1, 2 and 3. Nowadays very high accuracy circuit simulation tools are available in market like Eldo, Spectre etc. Several other tools were also developed like PSPICE or HSPICE for industrial and university use. New tools are based on the modern programming techniques and new algorithms and they have very high accuracy and better performance [5]. In my thesis, I used Cadence Spectre for circuit simulation purposes. Some simulations were performed using 65 nm process and major part of the simulations was performed using 130 nm process.

2.1 Properties of Circuit Simulation

Following properties of circuit simulators have been observed.

- Circuit simulators represent the voltage and current signals as sequence of time value pairs.
- In transient analysis, time looks like a continuous variable but in actual digital computers there are only few points and other points are obtained by interpolation.
- Transient analysis means the solution of differential algebric equations at every time point.

2.2 Transistor Model Quality

A large variety of MOS transistor Models provide the high quality simulation results. Level 1, Level 2 and Level 3 Models are important just for historical point of view but they cannot provide the accurate simulation results. BSIM models are standard nowadays and are used for industrial and university research purposes, but there are some companies who rely on their own models.

2.2.1 Level 1 Models

Level 1 model is based on square law and implements Shichman-Hodges models [5]. This model is based on the derivation of long channel expressions. This model doesn't include the short channel effects.

$$\frac{I_d}{K} = \begin{Bmatrix} 0, \quad V_{gs} < V_t \\ (V_{gs} - V_t)^2 - (V_{gd} - V_t)^2, \; V_{gs} > V_t, \; V_{gd} > V_t \\ (V_{gs} - V_t)^2, \; V_{gs} > V_t, \; V_{gd} < V_t \end{Bmatrix} \tag{2.1}$$

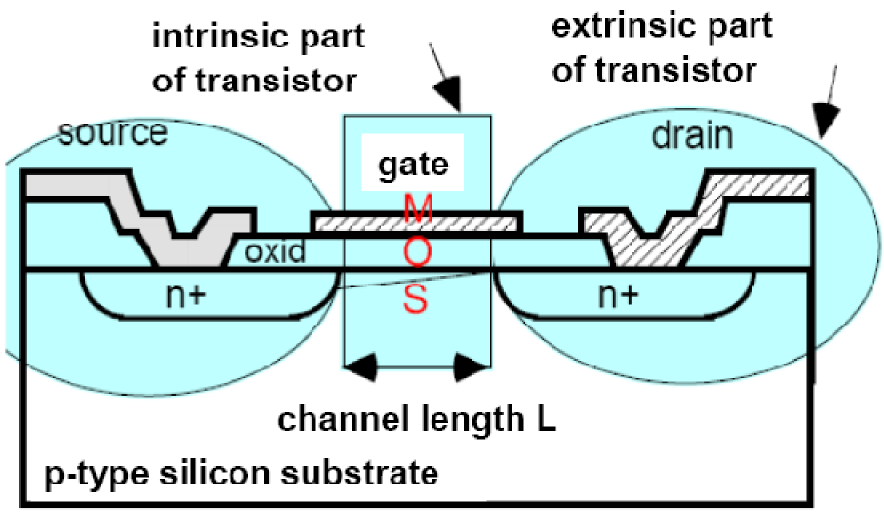

Figure 2.1: A simple transistor Model [5]

2.2.2 Level 2 Models

Equations of Level 2 Models are derived from the detailed device physics and are based on geometry [5]. Level 2 model is based on Grove-Frohman equations. Level 2 model is more accurate than Level 1 model and also handles the second order effects like mobility degradation, DIBL (Drain induced barrier lowering), sub threshold conduction, velocity saturation. However problem with this model is complexity due to including submicron process advanced 3D effects in physics based models.

2.2.3 Level 3 Models

This model consists of empirical and analytical expressions [5]. This model is good for channel length down to 1 micron meter and it determines its main parameters by using measured device data. This model is also called semi empirical. Level 3 models have almost same accuracy, better convergence and faster simulation time as compared to level 2 models. Level 3 models are not the standard in today's industry because they don't fit well into modern transistors I-V characteristics curves.

2.2.4 BSIM Models

Some of the semiconductor manufacturing companies rely on their own transistor model and claim that the model developed by them is best in the world, so this situation makes it difficult to choose the best. Fortunately, BSIM (Berkeley short channel IGFET model) was developed in 1990's at university of California at Berkeley. BSIM stands for Berkeley short channel IGFET model. BSIM models are very accurate, reliable and are standard in today's industry. These models best fit into the I-V characteristics of modern transistor. BSIM 3 model includes over than 200 parameters. Fortunately as IC designers, we don't need to know about all model parameters. These parameters usually model the second order effects. Although BSIM models are considered most reliable in digital integrated circuits simulations, but still theses models don't model the leakage currents well. BSIM4 model is an extension of BSIM3 model. BSIM4 model is physics based, robust, most accurate, scalable and predictive transistor model for high accuracy in circuit simulations. BSIM models have sensitivity of transistor width and length to different parameters like threshold voltage Vt. These models have very detailed threshold models including DIBL (Drain induced barrier lowering) and body effects. These models have good convergence of I-V characteristics across sub threshold, linear and saturation regions. BSIM models have multiple gate capacitance models including diffusion capacitance and resistance models. BSIM models have detailed information about different effects like short channel effects, mobility degradation and velocity saturation. In BSIM models the temperature dependence is included in the model of diode junction capacitance. To avoid the bad values of certain parameters the parameter checking is also included in the model. BSIM 4 models also have support for gate leakage effect and very thin gates effects.

2.2.6 Caution

IC designers almost have religious faith on their simulation results. But it is also important to consider that the simulation results can deviate from reality because of many reasons like inaccuracies in transistor models, device parameters, parasitic capacitance and resistance. The predicted and actual behavior of a digital integrated circuit can also be different due to process variations over the die or temperature variations. So there should be a substantial margin between the simulation results and design constraints.

3 Flip-Flops and Latches

Flip flop is a data storing device that has the capability to store one bit of data either 1 or 0. Flip flop has two stable stages. A flip flop is a non-transparent device and is either edge triggered or clocked, while a latch is a transparent device. A flip flop is often controlled by either one or two control signals and a clock signal or gate signal. A latch is called positive latch when it passes input D to out Q when clock is high and similarly a latch is called negative when it passes input D to output Q when clock signal is low.

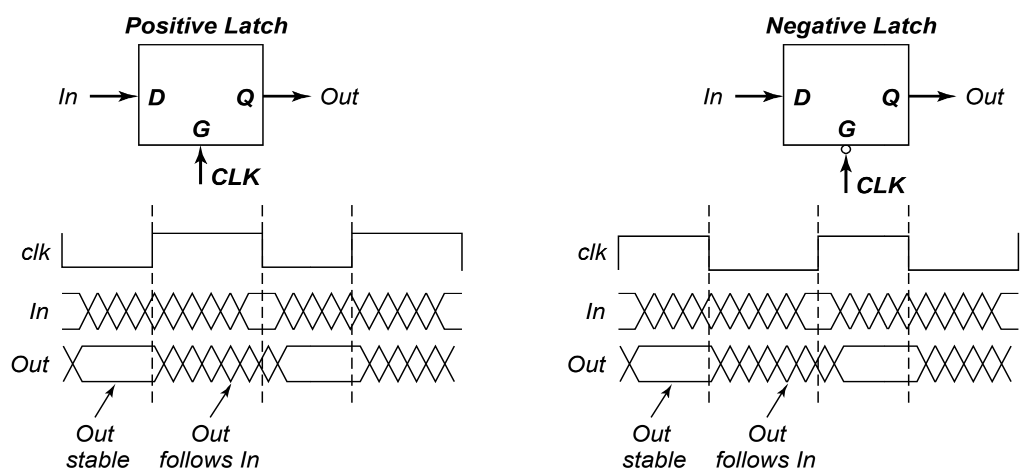

Fig3.1: positive and negative latch [5]

Flip-Flop is bistable component and is built by the cross coupling of gates. A positive edge triggered register samples data at the clock transition 0 →1 while a negatively edge triggered register samples data at the clock transition 1→0. A master slave latch can be built by cascading positive latch and a negative latch.

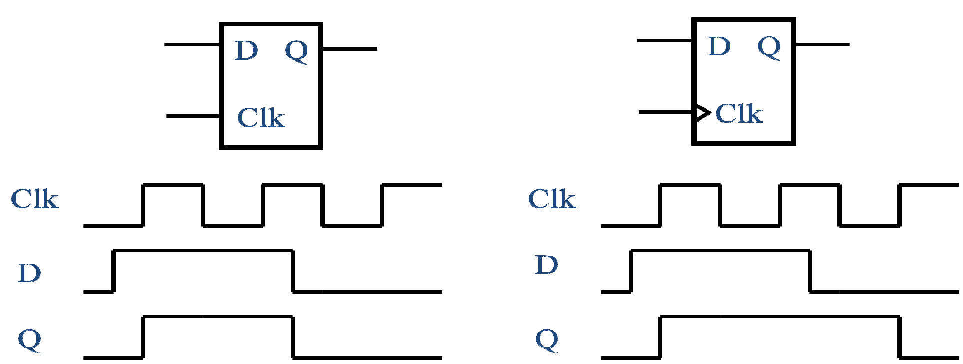

Fig3.2: Latch VS Register [5]

There are three parameters that are associated with the register and those are

- Setup time
- Hold time
- Propagation delay

Setup time:

Setup time is the time for which input must be valid before the clock transition (0→1 in case of positively edge triggered register).

Hold Time:

Hold time is the time for which input must remain valid after the clock edge.

Propagation delay:

Propagation delay is the length of time when input data is stable and valid and clock transition (0→1 in case of positively edge triggered register) to the time when output is stable and valid. Usually propagation delay is referred as the maximum time from input crossing 50% to the output crossing 50%.

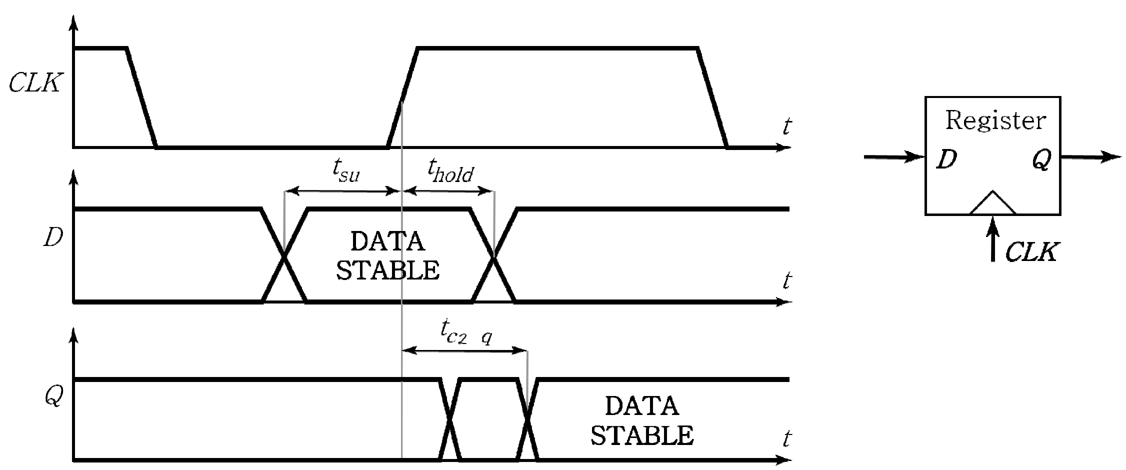

Fig3.3: setup time, hold time and propagation delay waveforms [5]

In this thesis, I used three different flip-flops topologies for analysis on 130 nm process and the target was to design the low power, fastest, robust and noise free flip flops. Increasing the performance usually increase the power dissipation. Methods of operation of these flip flop topologies and simulation results are attached in the simulation section.

4 Power Dissipation

Power dissipation is a major problem in digital integrated circuits. It decreases the performance and reliability of digital integrated circuits, so low power designs are major challenge for digital designers. In this topic, I will discuss power dissipation in CMOS integrated circuits.

The instantaneous power is given by [5]

$$P(t) = I_{dd} \bullet V_{dd} \tag{4.1}$$

The energy consumed is given by [5]

$$E = \int_0^T I_{dd}(t) \bullet V_{dd}(t)\, dt \tag{4.2}$$

The average power over this interval is given by the following relation [5]

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T I_{dd}(t) \bullet V_{dd}(t) dt \tag{4.3}$$

Power dissipation in CMOS digital integrated circuits is because of two components (Static and dynamic) [5]

$$P_{total} = P_{static} + P_{dynamic} \tag{4.4}$$

Static power dissipation is due to

- OFF transistors have Subthreshold conductions
- Gate oxide have tunneling currents
- Reverse biased diodes have leakage
- Ratioed circuits have contention currents

Static power dissipation in CMOS is give by the relation (4.5)

$$P_{static} = I_{static} \bullet V_{dd} \tag{4.5}$$

Dynamic power dissipation is due to [4]

- Charging and discharging of capacitances at load
- "Short-circuit" current while both pMOS and nMOS networks are partially ON

From equation (4.3), we can derive the relation for dynamic Power dissipation in CMOS

$$P_{dynamic} = C \bullet Vdd^2 \bullet f \tag{4.6}$$

From equation (4.6), we can see that the dynamic power dissipation in CMOS digital integrated circuits can be reduced by

- Reducing capacitance => Need to use short wires (Wire also cause capacitance)
- Reducing the supply voltage V_{dd}
- Reducing the clock frequency

5 Switching Noise

Switching noise is a complex issue in digital integrated circuits design. It can be divided into three different parts: first part is the circuit that generates noise called aggressor circuit; second part is the circuit that couple the noise from aggressor called victim circuit, and third part is the circuit that picks the noise from victim circuit. The total noise which received at victim circuit is the combination of noise from a lot of aggressor circuits. Circuit reduction techniques are important in noise generation. Reduced digital circuits generate less noise and large digital circuits generate more noise and we also require large computer and software resources to simulate.

It is important to study the harmonic contents of switching waveform spectrum to control the noise in digital integrated circuits. The spectrum of a signal is determined by its time-domain waveforms. According to rule stated by Lee [10]: "the spectrum of a signal will decay as $1/f^n$, where n is the number of derivatives of the signal required to yield an impulse". Discontinuities occur only in simulation domain and the presence of discontinuities in model distort spectra, so when we wish to study higher order harmonics, we need to avoid model discontinuities, otherwise we cannot trust the results.

As output waveforms approximate square waves, so there will be higher order harmonics in all switching waveforms, regardless of the shape of the input waveform. The main reason not to use $\sin$e waves is that the comparatively slow edges cause extra short-circuits power. These higher order harmonics are also expected when $\sin$e wave is amplified and limited. If we use square wave as input to digital circuits it will create discontinuity in the output switching waveform or its derivatives and it will decrease the roll-off in output switching waveform spectrum. So the best option is to use square like wave (Neither sinusoid nor square) as an input to digital circuits. In my thesis I used $\arctan(\sin)$ signal as input to make it sure that there is no discontinuity in the input signal because $\mathrm{tangent}$ and sine are continuous functions. The spectrum of output switching waveform can be evaluated by FFT. To plot the spectrum of the switching waveforms, I transferred the equidistant data points from Cadence Spectre to Matlab. Cadence is best for simulations but Matlab is best for plotting and spectrum analysis.

Transistor model quality is very important in the estimation of harmonic contents of switching waveforms. BSIM4 transistor models are extended version of BSIM 3 models and they provide steeper roll-off in the switching waveform spectrum and they don't have any discontinuity. BSIM3 transistor models also don't have any discontinuity. Roll-off in output switching waveform spectrum provided by level1, Level2, level3 transistor models is not considered good due to discontinuity.

Threshold voltage of a device is an important parameter. Devices with lower threshold yield higher subthreshold currents and turn on softly and yield a steep roll off [1]. So devices with lower threshold voltages are good for the highly integrated devices. But the problem with low threshold is that it causes leakage currents and hence idle power dissipation. Accurate estimation of harmonic contents of CMOS logic switching waveforms allow the designers and computer aided design (CAD) tools to control and minimize the production of switching noise in the design. Digital circuit designers also distribute the noise budget among the different blocks of the design and this technique is useful in minimizing the switching noise in the designs.

6 Fourier analysis

Fourier transform is developed by French mathematician Joseph Fourier. Fourier transform is one of the mathematical tools used by the engineers in spectrum analysis. It is not possible to analyze the spectrum without Fourier transforms and hence it is extensively used in circuit analysis and computer aided design simulation tools.

6.1 DFT

DFT is discrete fourier transform and is used for spectrum analysis. DFT takes the discrete signal in time domain and transform this signal into discrete frequency domain.

The discrete Fourier transform DFT is given by equation (6.1)

$$X(k) = \sum_{n=0}^{N-1} x(n)\, e^{-j2\pi kn/N} \ \ where\ k\ = 0, \dots N-1 \tag{6.1}$$

Where N is the number of samples, $X(k)$ is kth coefficient of DFT and $x(n)$ denotes the nth sample of the of the time series. We can also note that $X(k)$ is a complex number and $X(n)$ can be a complex number or real number.

The inverse of DFT can be calculated by the relation (6.2)

$$X(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k)\, e^{j2\pi kn/N}\ where\ n = 0, \dots N-1 \tag{6.2}$$

6.2 FFT

FFT is fast fourier transform and is faster implementation of discrete fourier transform (DFT). In 1965 Cooley and Tukey developed an efficient algorithm called FFT to compute the same thing as DFT. Radix-2 Cooley Tukey is the most famous implementation of this algorithm which requires that the number of points in the series should be a power of 2 [11]. Radix-2 FFT computation time is proportional to

$$N \bullet log_2(N) \tag{6.3}$$

The transform on 1024 points using FFT is 100 times smaller than using the DFT.

6.3 Sampling theorem

According to sampling theorem the sampling frequency of a continuous signal should be at least two times the frequency of the highest frequency in the signal.

It is possible to define a continuous signal $f(t)$ by samples of time period $1/f_s$, where f_s is sampling frequency. Suppose frequency spectrum $F(f) = 0$, for $f\ > f_s/2$. Where $f_s/2$ is known as the Nyquist frequency. During digitization of a continuous signal the Nyquist frequency puts the limit on the minimum sampling frequency [11].

A continuous signal $f(t)$ can be reconstructed from the samples $X(k)$ of time period $1/f_s$ but in this case the sampling theorem must be satisfied by [11]

$$f(t) = \sum_{k=-\infty}^{K=\infty} X(k)\ \mathrm{sinc}(t \bullet f_s - k) \tag{6.4}$$

Where

$$\mathrm{sinc}(x) = \frac{\sin(\pi \bullet x)}{\pi \bullet x} \tag{6.5}$$

Usually the signal to be digitized should be filtered before the sampling to eliminate the higher frequency components. If the sampling frequency is low and not high enough the signal will be corrupted, because in this case the higher frequency components will wrap around and appear in different locations in the discrete spectrum. [11].

Figure 6.1 represents a continuous signal in time and frequency domains.

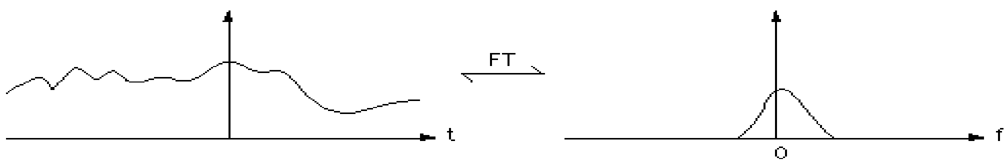

Figure 6.1: Continuous signal in time and frequency domain [11]

Signal of figure 6.1 can be sampled with sampling frequency f_s, where sampling period is $1/f_s$. This is similar to the frequency domain convolution by delta function train with a spacing of f_s [11].

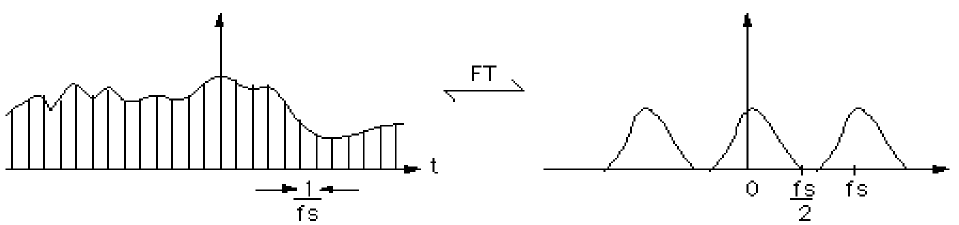

Figure 6.2: Sampling of signal with sampling frequency f_s [11]

The signal will be corrupted if the samples are too low because in this case the frequency spectrum will overlap the signal as shown in figure 6.3.

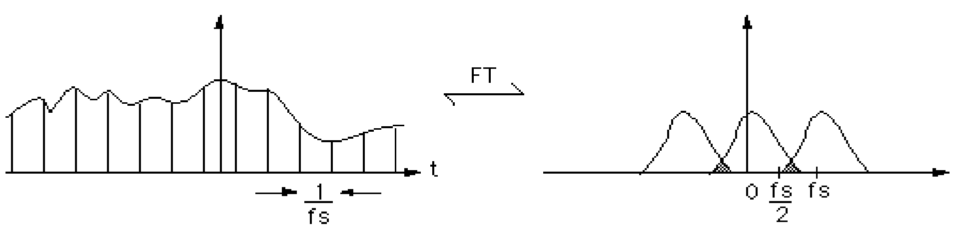

Figure 6.3: Frequency spectrum overlapping [11]

7 Comparison between 65nm and 130nm processes

All simulations were performed with Spectre simulator using 65nm and 130nm process technologies and for the Spectrum analysis equidistant data points were transferred from Spectre to Matlab. I simulated a simple inverter for tool set-up and comparison purposes between 65nm and 130nm process technologies.

7.1 Input signal in all Simulations

In all simulations, I used square like wave as an input signal, it is neither sinusoid nor a square wave. Square like wave was generated by taking $\arctan$ of a sinusoid wave and multiplying its argument by a number like 10 to change its sinusoid shape to square.

$$V = \mathrm{arc}\tan\left(10 \bullet \sin\left(x\right)\right) \tag{7.1}$$

So generated wave is having fast edges with no discontinuity. Spectre cannot do this, so I used VerilogA [6] to implement this function.

7.2 Simulations of an Inverter on 65nm

Simulation conditions in this experiment are:

- Process technology = 65nm
- Temperature = 27 °C
- Power supply voltage V_{dd} = 1V
- Clock frequency = 1 GHz

7.2.1 Schematics

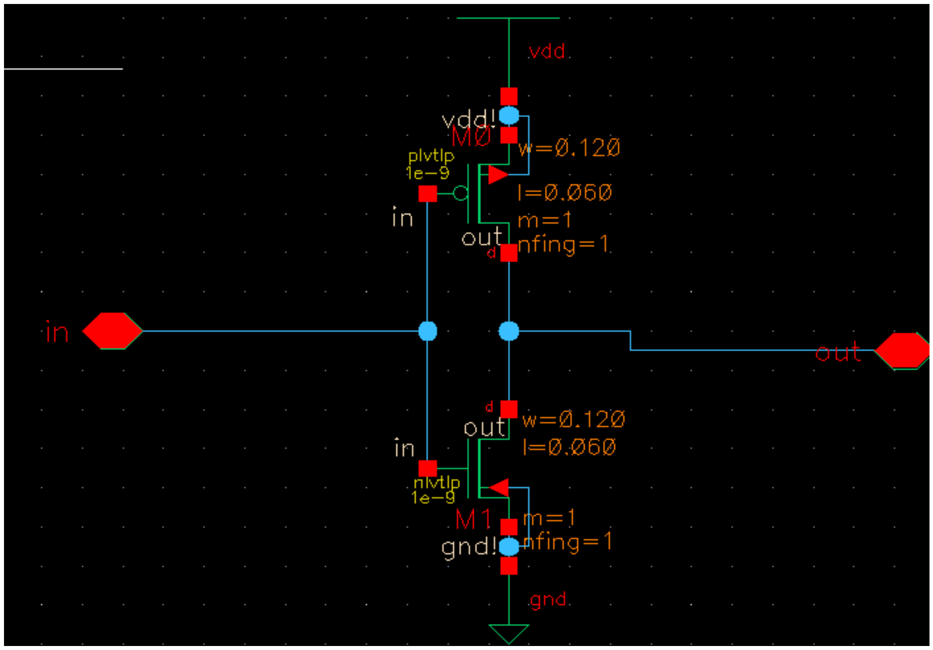

Figure 7.1: Schematics diagram of inverter using 65nm process

7.2.2 Test Bench

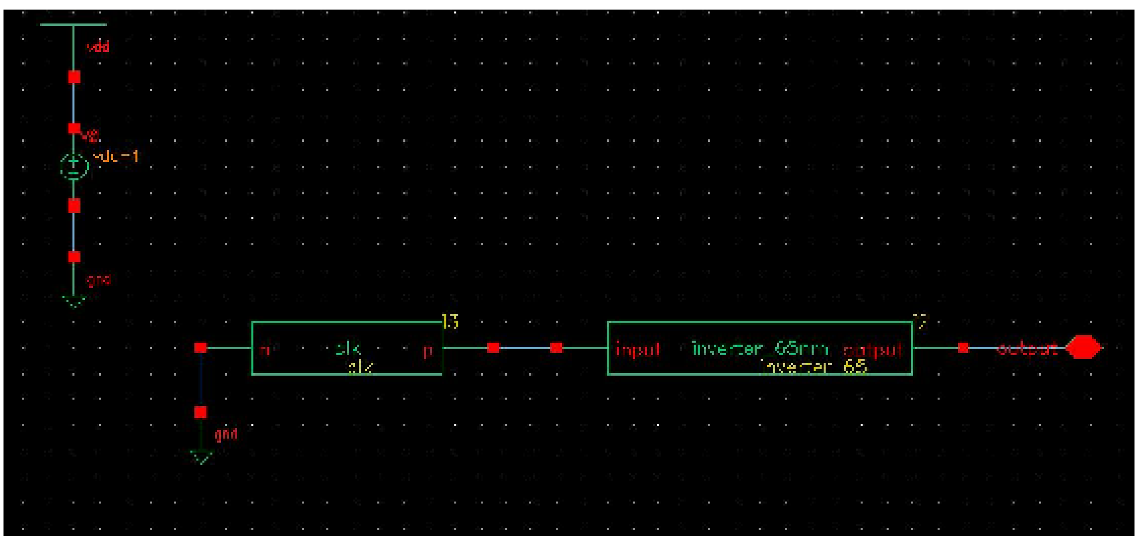

Figure 7.2: Inverter test bench

7.2.3 Cadence waveform

Figure 7.3 represents the waveform of simple inverter input and output. Input signal is square like wave and is generated by using VerilogA.

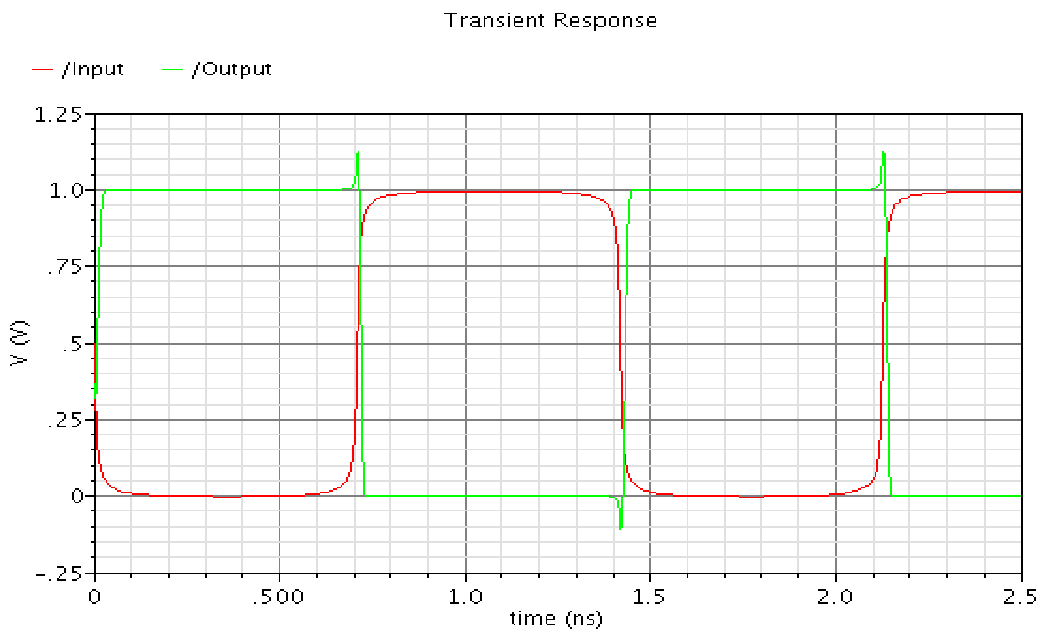

Figure 7.3: Input and output waveforms of inverter using 65nm process

7.2.4 Matlab Waveforms

After plotting waveform in Cadence Spectre I transferred data points to Matlab. Cadence Spectre is best tool for simulations but not for spectrum analysis, Matlab is a best tool for spectrum analysis. I used higher accuracy settings in Cadence Spectre to plot 5000 equidistant data points in specific cycle to see the clear view of data points in spectrum. After transferring data points to Matlab, I took one cycle of the whole waveform.

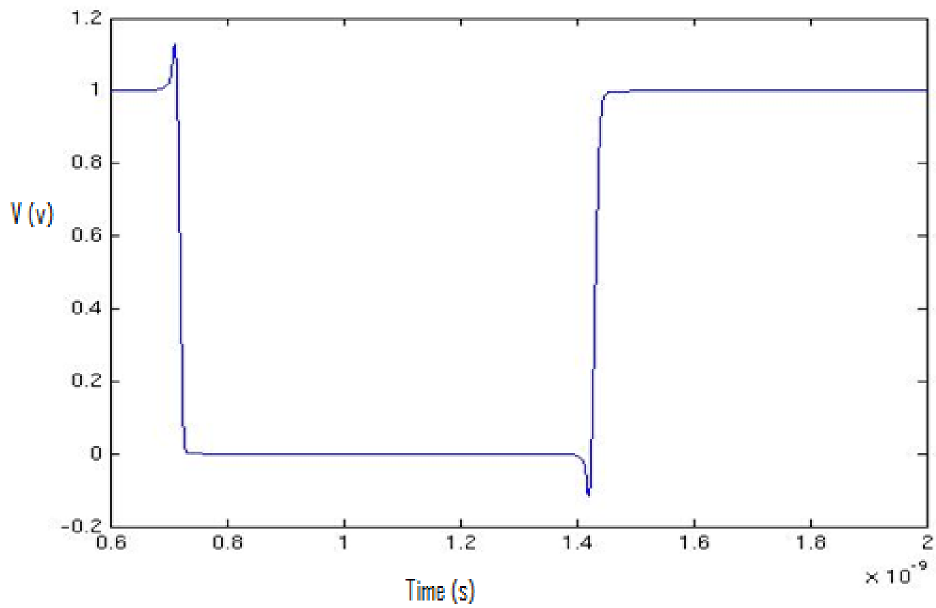

Figure 7.4: Inverter output plot (one cycle) on Matlab

7.2.5 Matlab Spectrum Plot

Figure 7.5 shows the spectrum of inverter's switching waveforms. Before knee frequency the spectrum roll-off is around 20 dB/decade, beyond knee frequency the spectrum roll-off is much faster than 20 dB/decade. At knee frequency, the spectral amplitude is down by half (-6.8 dB) below the natural 20 dB/decade roll-off [3]. Beyond knee frequency the spectrum roll-off is about 100dB/decade. Spectrum roll-off of 100 dB/decade shows that there is no discontinuity in first four derivatives of output signal. Input signal was square like wave generated by arctan of sinusoid wave to make it sure that there is no discontinuity in the input signal. Discontinuity decreases the spectrum roll-off and causes higher order harmonics so we avoid discontinuity. We want spectrum of switching waveform as steeper as possible to avoid higher order harmonics. To control noise in digital integrated circuits we need to have the correct estimation of harmonics.

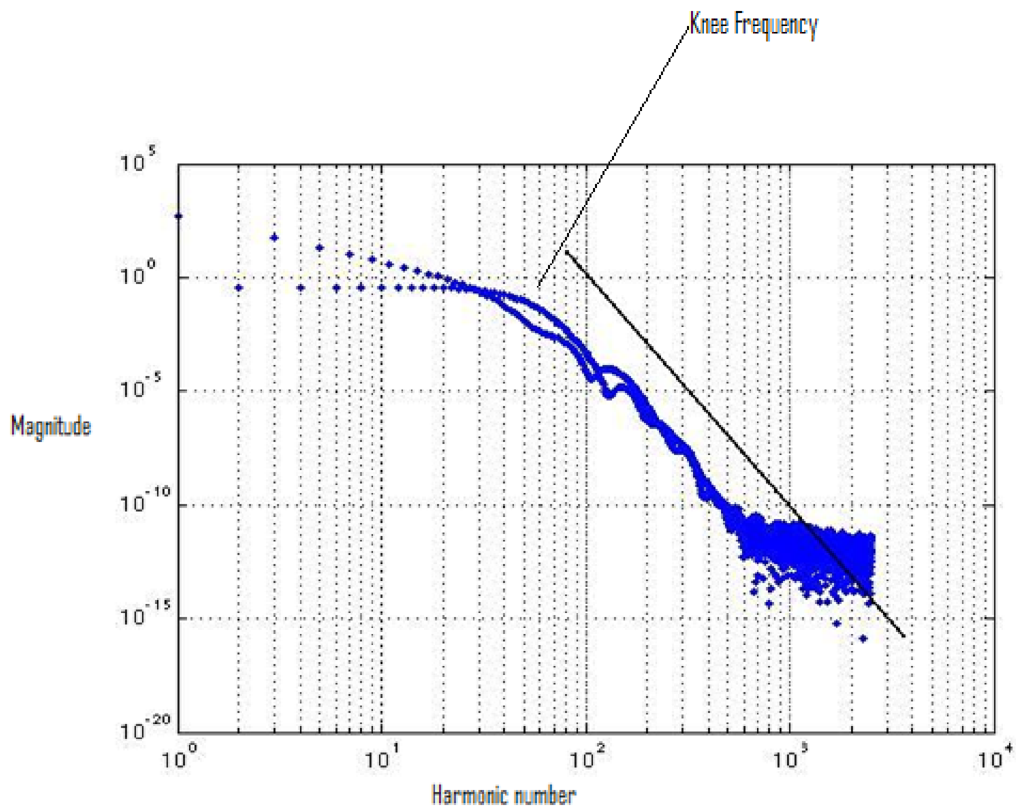

Figure 7.5: Spectrum plot of inverter switching waveform

7.3 Simulations of an Inverter on 130nm

Simulation conditions in this experiment are:

- Process technology = 130nm
- Temperature = 27 °C
- Power supply voltage V_{dd} = 1V
- Clock frequency = 1 GHz

7.3.1 Schematics

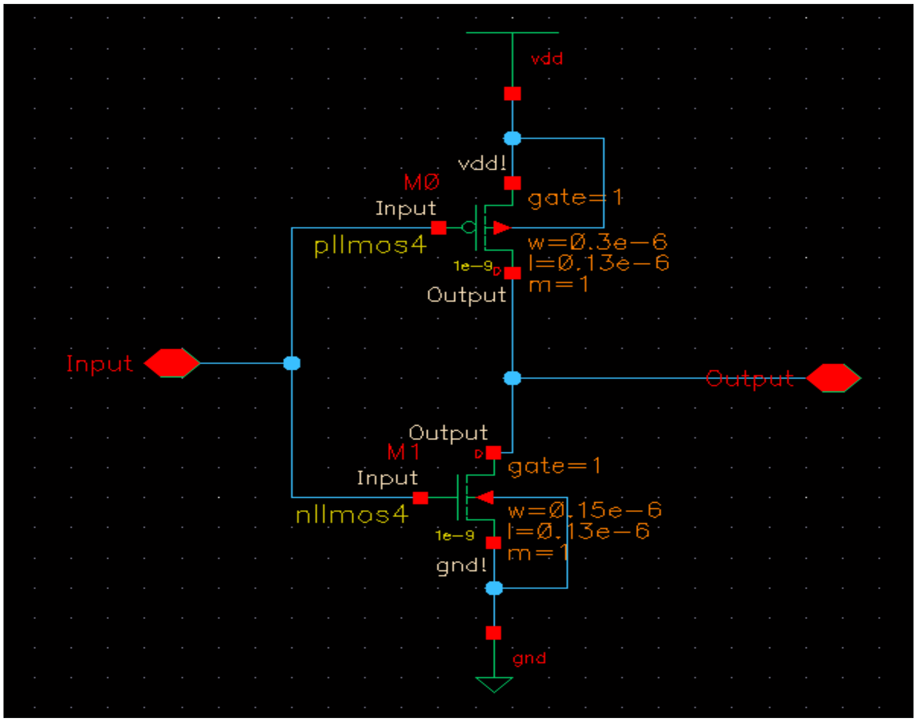

Figure 7.6: Inverter Schematics on Cadence Spectre

7.3.2 Test Bench

Figure 7.7 shows the test bench of inverter using 130nm process, where FF1_tb2 shows the verilogA symbol and it generates the square like wave.

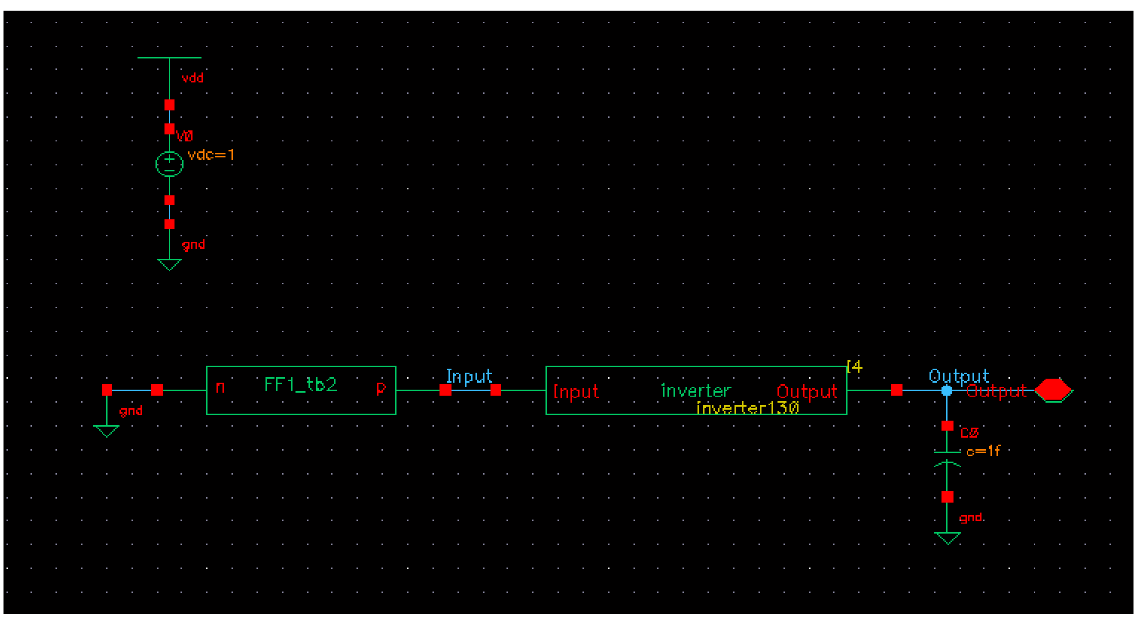

Figure 7.7: Inverter test bench

7.3.3 Cadence Waveforms

Figure 7.8 shows the input and output waveform of an inverter. In figure 7.8, the input voltage swings above 1V, this is because the input signal was generated by using arctan(Sin) function in VerilogA. Initially the input signal swing was much above than 1V, but I adjusted the swing very near to 1V by addition and division of arbitrary numbers in function. Fig 7.9 shows the VerilogA code to generate square like wave. Falling edges are steeper than the rising edges of inverter output this is because of input signal swing above 1V and n-channel device is turned on harder.

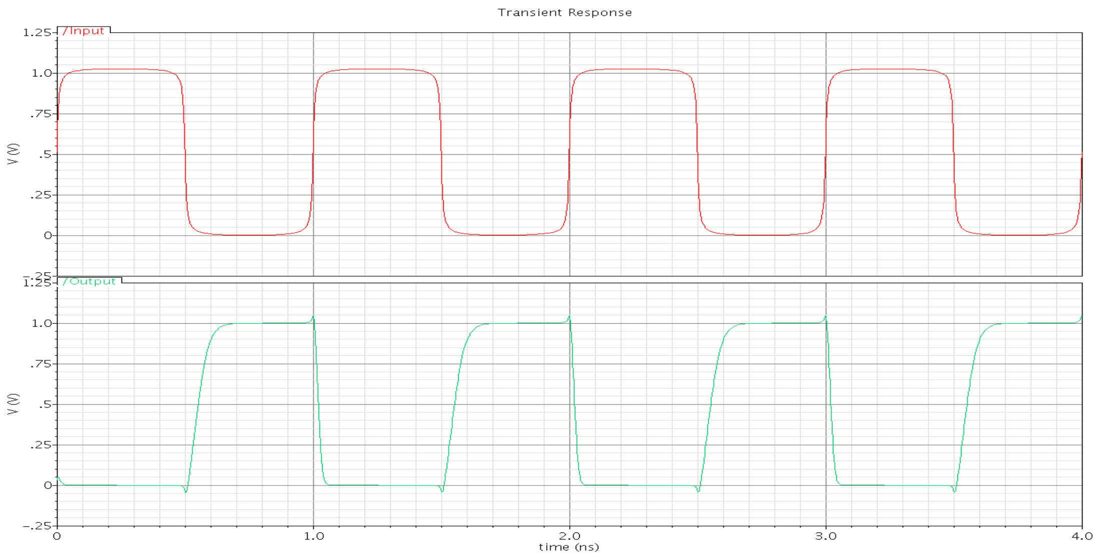

Fig 7.8: Inverter input and output plots on Cadence

```
//Verilog-AMS HDL for "clock1", "clock1" "verilogams"

`include "constants.vams"
`include "disciplines.vams"
module clock1 (p,n);
  parameter real amplitude = 1.0;
  parameter real freq = 1e9;
  parameter real phase = 0.0;
  inout p;
  inout n;
  electrical p;
  electrical n;

  analog begin
    @(initial_step)
      V(p,n) <+ 0.0 ;
    V(p,n) <+ (atan(10 *amplitude * sin(2.0 * `M_PI * freq
* $abstime + phase))+1.54)/3;
  end
```

Fig 7.9: VerilogA code to generate square like wave

7.3.4 Matlab waveforms

Figure 7.10 describes the inverter output using 130 nm process where first cycle contain 5000 equidistant data points.

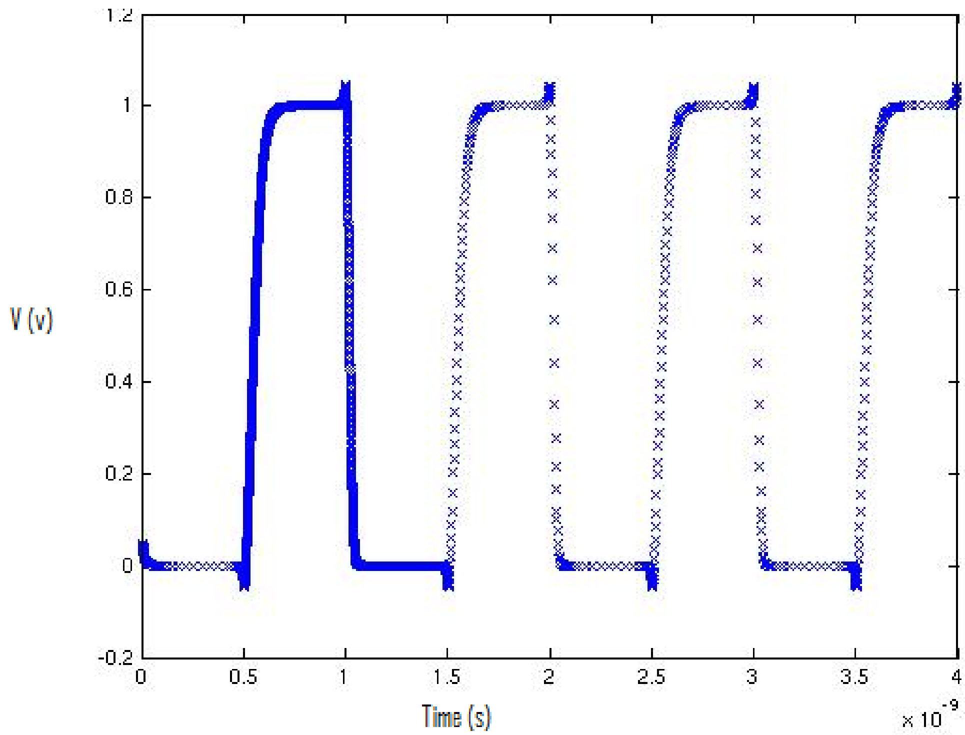

Fig 7.10: Inverter output plots on Matlab in which first cycle contain 5000 equidistant data points

7.3.5 One cycle

Figure 7.11 shows the plot of first cycle.

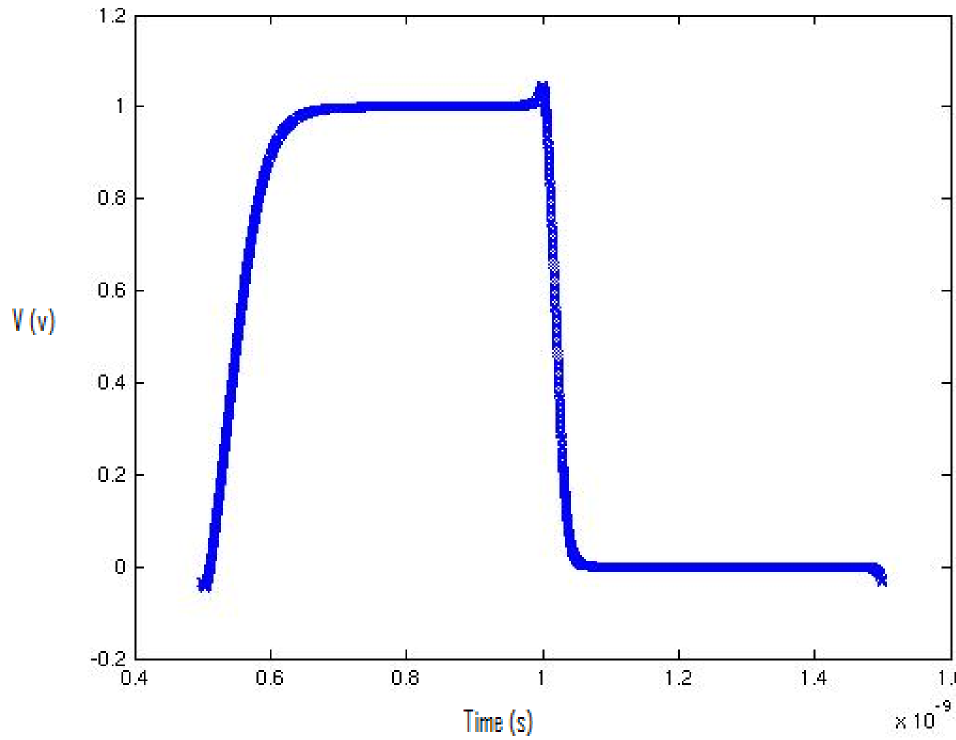

Fig 7.11: Inverter output plots (one cycle) on Matlab

7.3.6 Matlab Spectrum Plot

Figure 7.12 shows the Matlab spectrum plot of the first cycle of switching waveform of inverter. Spectrum roll-off is about 80 dB/decade.

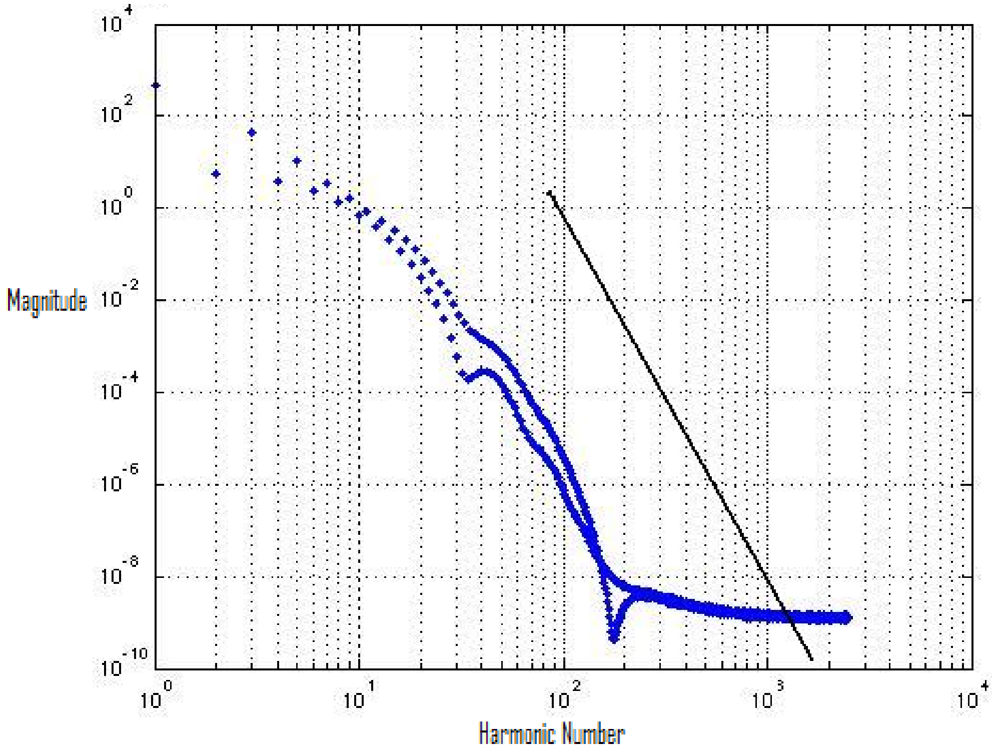

Figure 7.12: Spectrum plot of inverter switching waveform

7.4 Comparison between 65nm and 130nm

We can see that the roll-off of spectrum of switching waveforms plotted by using 65nm process is steeper than 130nm process. Spectrum roll-off obtained by using 65nm process technology is 100 dB/ decade while the spectrum roll-off obtained by using 130nm process technology is 80 dB/ decade. The capacitive load at the output of inverter using 130nm is 1 fF, whereas there is no capacitive load at the output of inverter using 130nm. The rise time of inverter output waveform using 65nm is 0.3 ns and the rise time of inverter output waveform using 130nm process is 0.7 ns. So the difference in slope of spectrum of these two process technologies may be because of process parameters itself, capacitive load at output and the rise time, delay times of switching waveforms. So we can see that the simulation results of 65nm process are improved than 130nm process in terms of rise time and spectrum roll-off of switching waveforms.

8 Flip Flop Topologies

In this chapter I will describe the design goals, simulations, spectrum analysis and results of three different flip flop structures PowerPC 603 Master-Slave Latch, modified C^2MOS Latch, hybrid-latch flip flop (HLFF). All simulations were performed with Spectre simulator using 130nm process technology.

8.1 Design Goals

In all three flip-flop structures the design goals were like this

- We like to apply
  I. A pulsed design
  II. Smaller as possible direct path
  III. Smaller as possible node swing
  IV. Smaller as possible clock load
  V. Feed back with low power
  VI. Master and slave both should be optimized
- We don't want
  I. Setup time as positive
  II. Clock skew and clock slope sensitive
  III. Dynamic and floating nodes
  IV. Master latch as dynamic
- Optimizations of energy and delay
- Less power dissipation
- Maximum delay can be calculated by clk-Q+setup time

8.2 Simulation conditions

- 130nm process technology
- Temperature = 27 °C
- Power supply voltage V_{dd} = 1V
- Clock frequency = 1 GHz
- Data clock frequency = 500 MHz
- Minimum width of transistor = 0.15 micron meter
- Maximum width of transistor = 2.06 micron meter

8.3 Flip Flop topology 1

First topology of flip flop selected was PowerPC 603 Master Slave Latch, this flip flop structure is with short direct path and low power feedback. All simulations were performed by with Spectre tool by using 130 nm process.

8.3.1 Power PC 603 Master slave Latch

A flip flop can be built by two phase clock with a master slave latch pair. Figure 8.1 shows the schematic of the PowerPC 603 with the transmission gate master slave latch pair [2]. Master Slave latches have two clock phases, its simulations were performed with Spectre tool by using 130 nm process. Properties of PowerPC 603 Master slave latch are [2]:

- Low power feedback
- Clock load is high
- Unbuffered Input
    - Wire length must be small as possible at the input
    - Input capacitance is dependent on phase of clock
    - Under shoots and over shoots with longer routes
- Small clock output delay
- Low power device

8.3.2 Schematics

Circuit diagram of PowerPC 603 Master Slave Latch is given by figure 8.1.

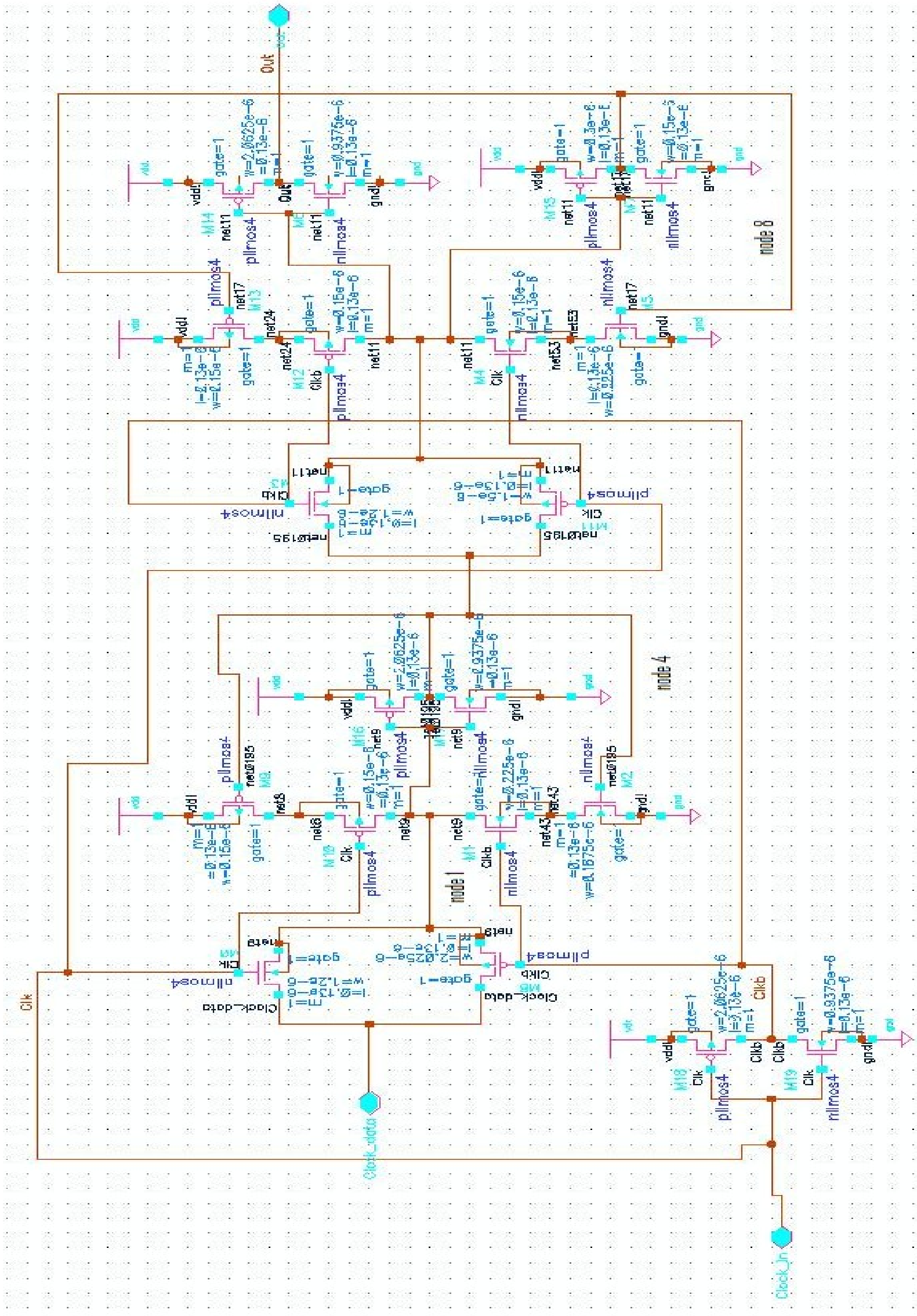

Fig 8.1: PowerPC 603 Master-Slave Latch Schematics

8.3.3 Test Bench

Figure 8.2 represents the test bench for the simulations of PowerPC 603 master slave latch.

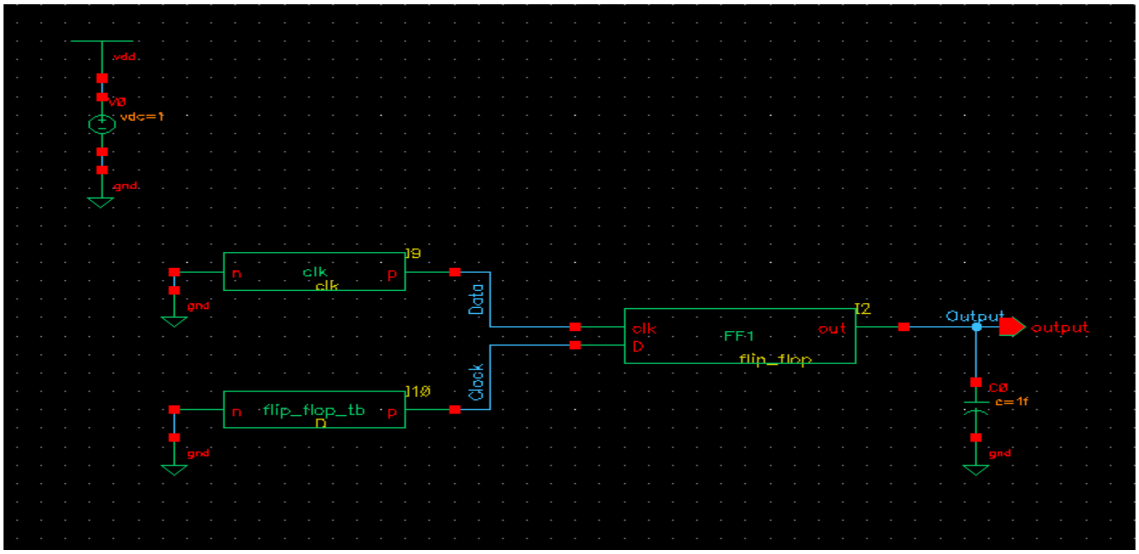

Fig 8.2: PowerPC 603 Master-Slave Latch test bench

8.3.4 Cadence Waveforms

Similarly as in the inverter simulations using 65nm and 130nm processes I generated the input square like wave using verilogA for the PowerPC 603 master slave latch simulations in 130nm process. Figure 8.3 shows the input and output waveform of PowerPC 603 master slave latch.

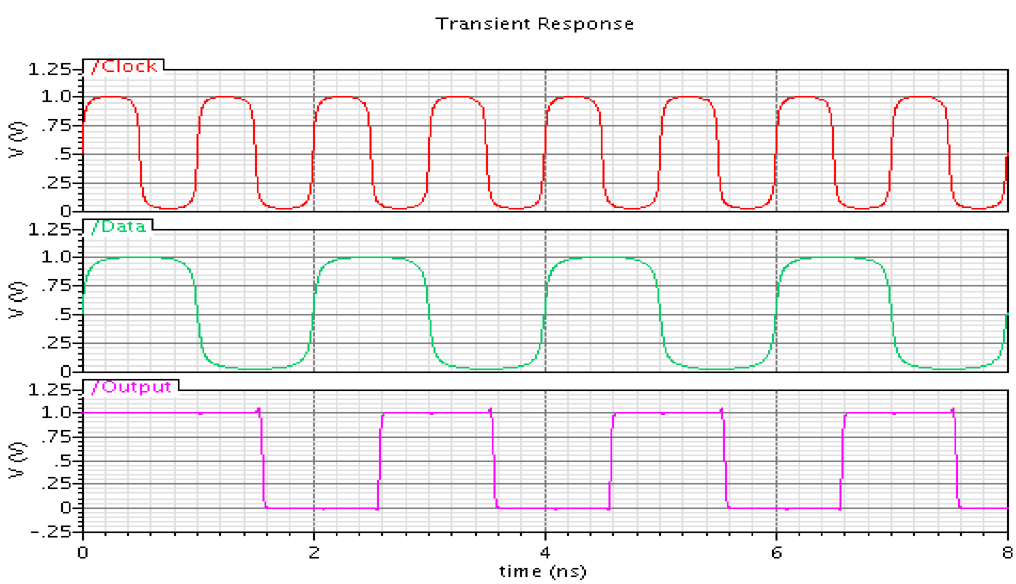

Fig 8.3: PowerPC 603 Master-Slave Latch input and output waveforms

Minimum set up and hold times are given by

Minimum set up time= 0.12 ns

Minimum Hold time = 0.14 ns

Clock to output delay = 0.07 ns

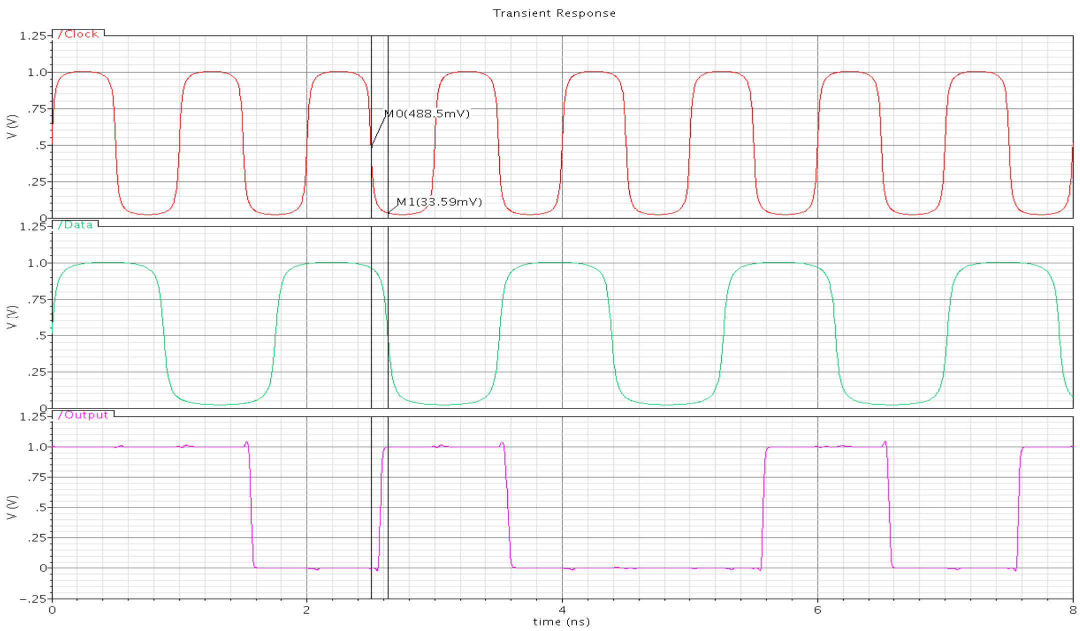

Fig 8.4: Minimum setup time calculations

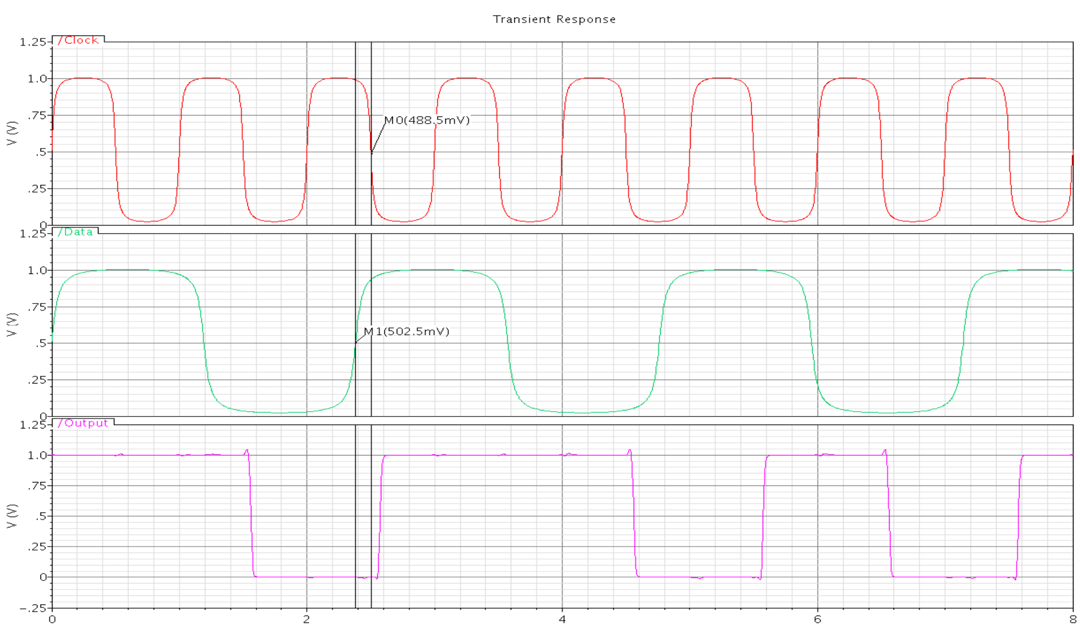

Fig 8.5: Minimum setup time calculations

8.3.5 Internal Node waveforms to check devices sizes

Fig 8.6 shows PowerPC 603 Master-Slave Latch internal node waveforms on Cadence Spectre. It is very important to check the internal node waveforms to verify the internal transistors sizes. We can see that the waveforms of internal nodes have steep rising and falling edges, so it means that the internal device sizes are reasonable.

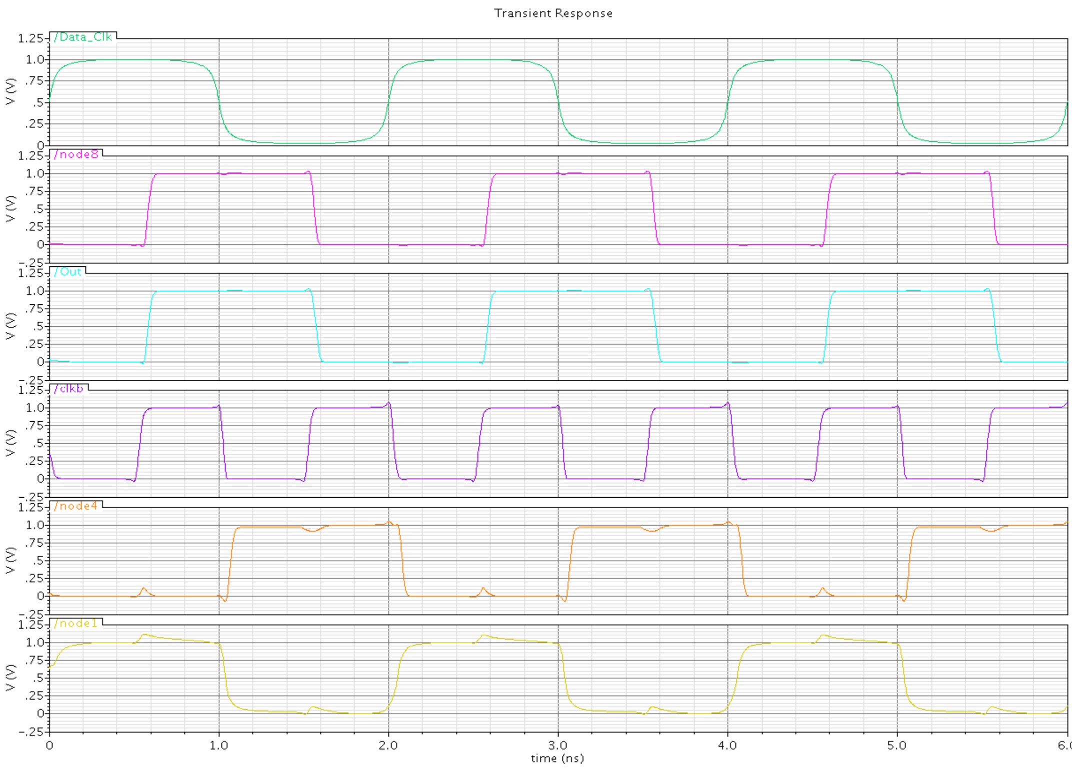

Fig 8.6: PowerPC 603 Master-Slave Latch internal node waveforms

8.3.6 Power plots

Power dissipation of a digital integrated circuit mostly depends on its structure and statistic of data applied. Figure 8.7 shows the plot of total power dissipation of PowerPC 603 Master-Slave Latch. Total power dissipation is sum of three power dissipations i.e. internal power dissipation of latch, local clock power dissipation and local data power dissipation. In figure 8.7, the pulse train like appearance of plot is because of switching activity. If no switching happens, the signal remains unchanged and the dynamic power is zero, but rapidly changing signals provoke plenty of switching and therefore dissipation. Supply voltage is 1V in this simulation. The average power dissipation of whole plot is 25.08 µW. In some intervals power doesn't go back to zero, this is because of static current flows or the capacitors are not fully discharged in that interval.

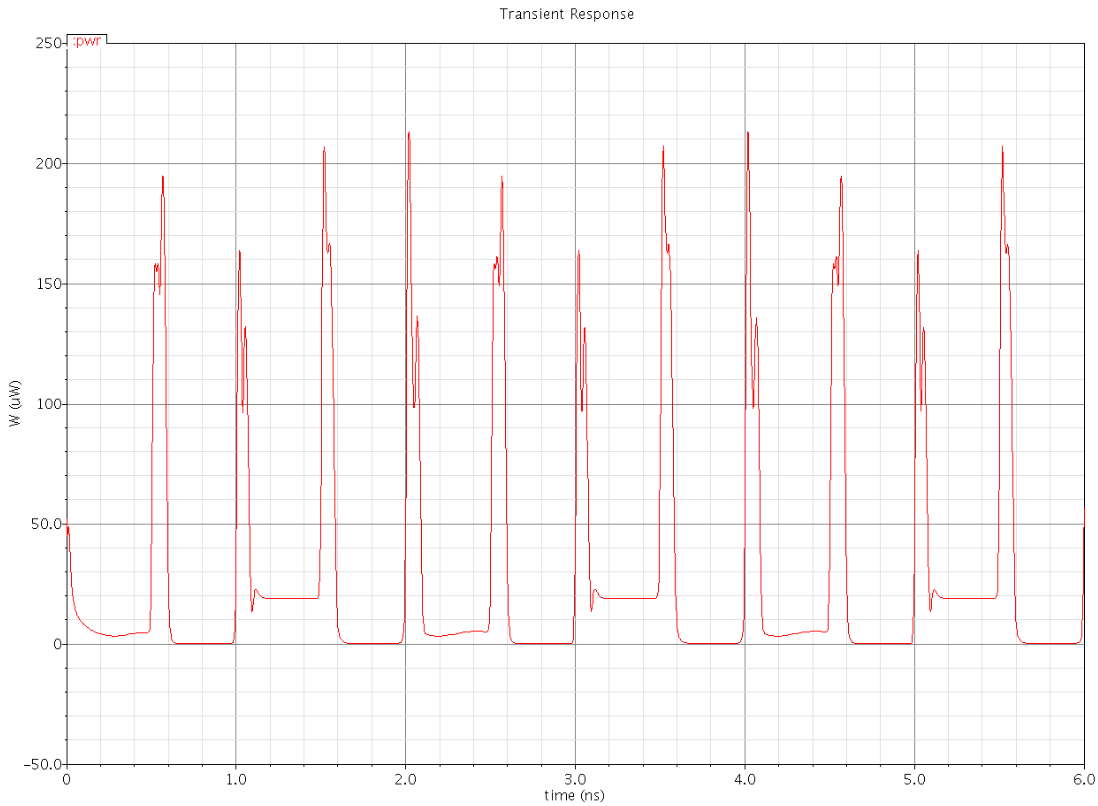

Fig 8.7: Waveforms of total power dissipation in PowerPC 603 Master-Slave Latch

8.3.7 Matlab Waveforms

Similarly as in 65nm process and 130nm process inverter design after plotting waveform in Cadence Spectre I transferred data points to Matlab.

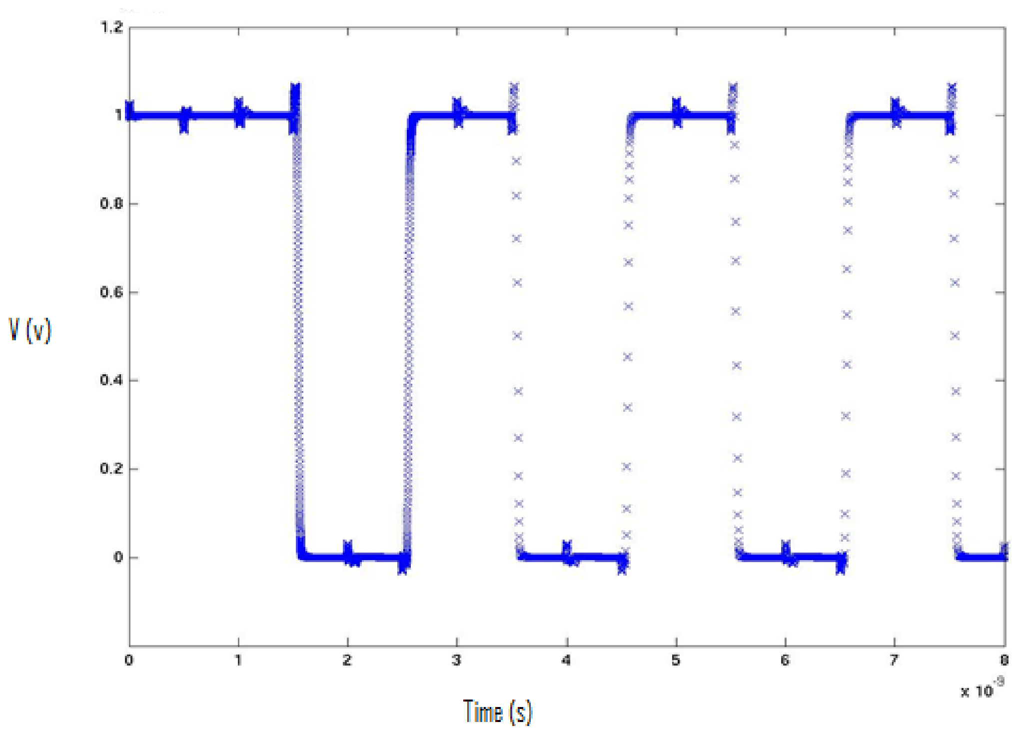

Fig 8.8: PowerPC 603 Master-Slave Latch output waveforms on Matlab

8.3.8 Matlab waveforms of one cycle

The plot of first cycle is given by the figure 8.9. It contained equidistant 5000 data points.

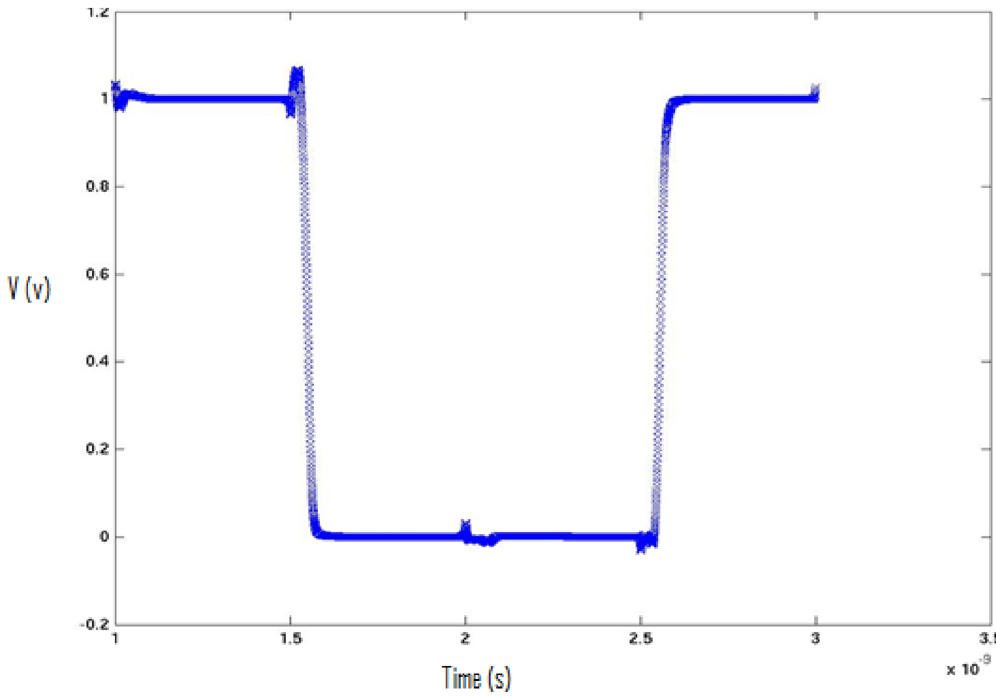

Fig 8.9: PowerPC 603 Master-Slave Latch output waveforms on Matlab (one cycle)

8.3.9 Matlab Spectrum Plots

Figure 8.10 represents the switching waveform spectrum plot of first cycle of PowerPC 603 Master slave latch. Spectrum roll-off is about 80 dB/decade, but there is bump that indicates that some harmonics have magnitudes about a factor of 10 larger than indicated, these are odd harmonics and are numbered as 101^{st}, 105^{th}, 109^{th}, 113^{th}, 117^{th} etc. Generation of these higher order harmonics is probably due to improper selection of time period of one cycle.

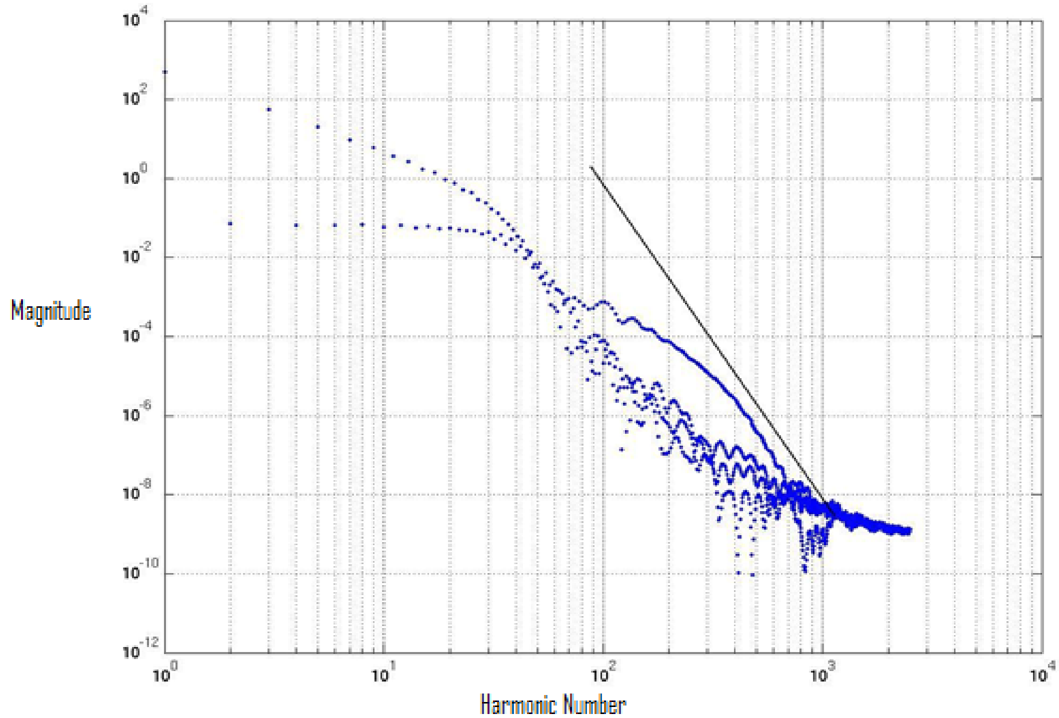

Figure 8.10: Spectrum plot of PowerPC 603 Master slave Latch switching waveform

8.4 Flip Flop 2 Topology

Second topology selected was modified C²MOS Latch, it is having low power feedback. Simulations of modified C²MOS Latch were performed with Spectre simulator using 130nm process technology.

8.4.1 Modified C²MOS Latch

C²MOS Latch is positive edge triggered register and is based on master slave concept like PowerPC 603 master slave latch. C²MOS stands for clocked CMOS (Complementary metal oxide semiconductor). C²MOS Latch samples data at only one edge of the clock i.e. either rising or falling edge. But in modified C²MOS Latch it is possible to sample data on both edges of the clock.

C²MOS Latch has following properties [2]:

- Weak driving capability
- Low power feedback
- Locally generated second phase
- Robustness to clock slope

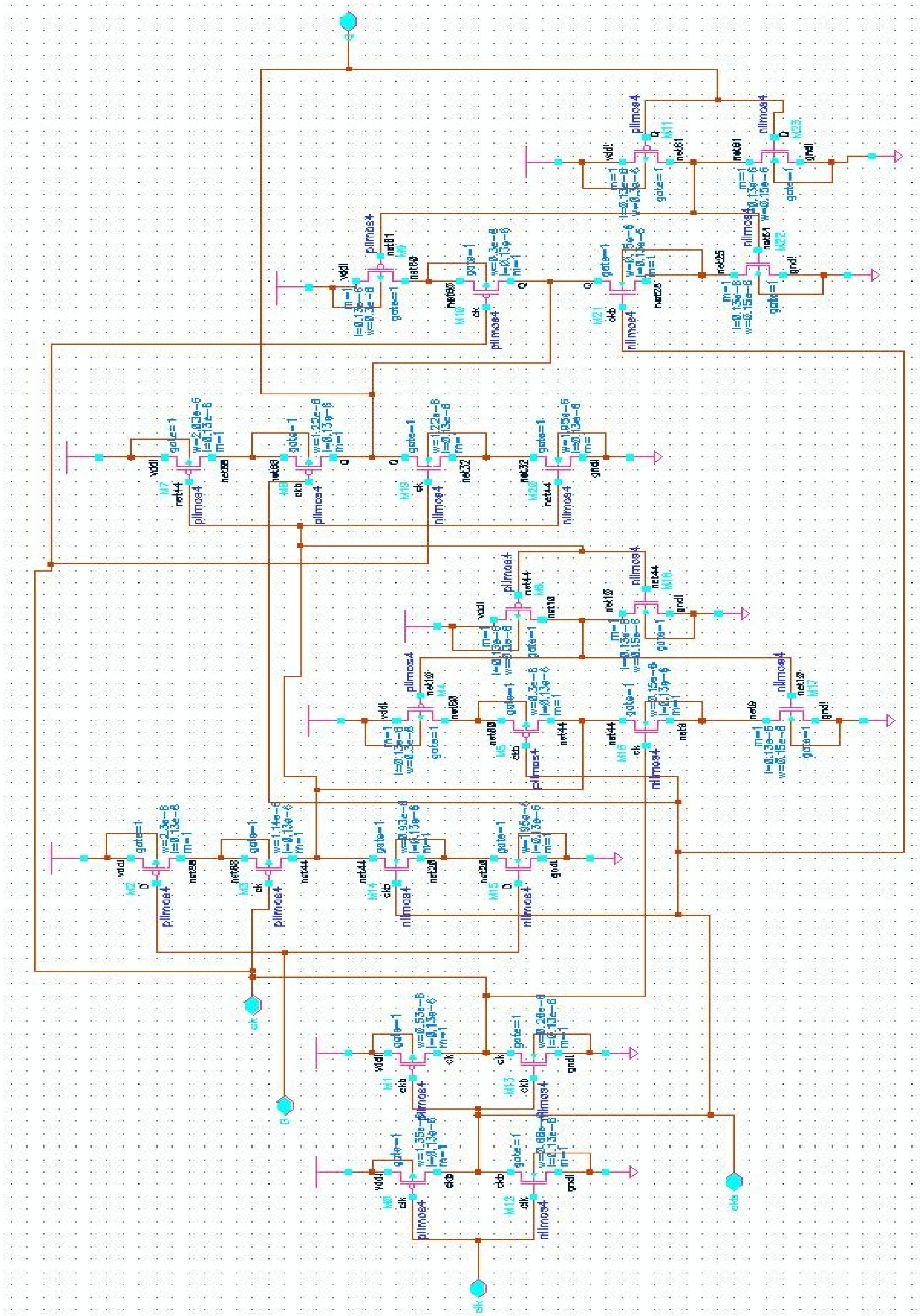

Fig 8.11: Modified C²MOS Latch Schematics

8.4.2 Test Bench

Figure 8.12 shows the test bench for the simulations of modified C²MOS Latch, where FF1_tb2 is data clock.

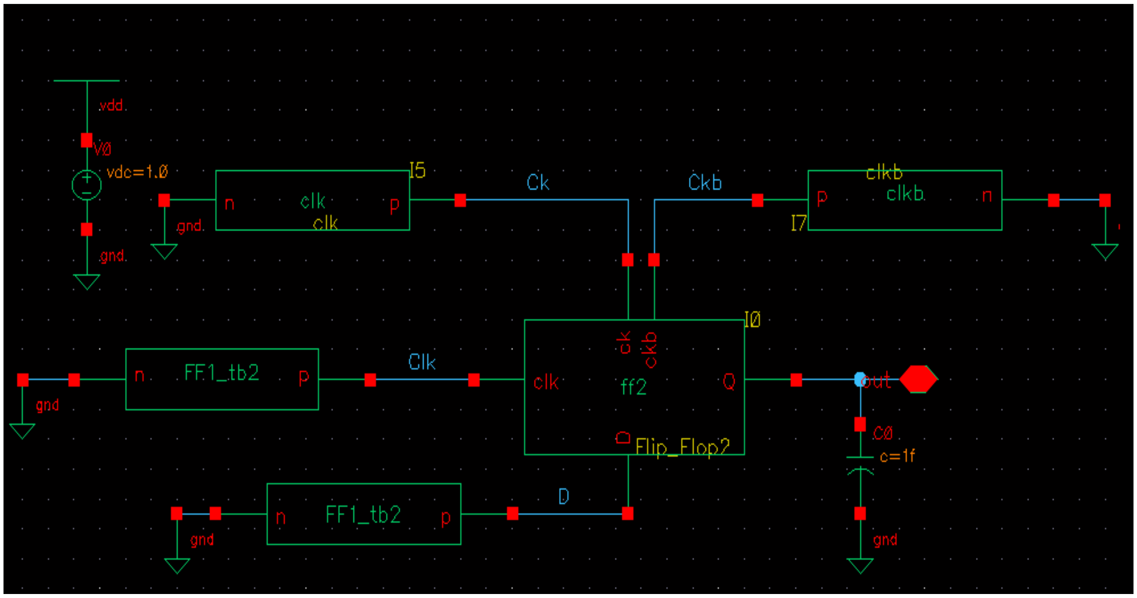

Fig 8.12: Modified C²MOS Latch test bench

8.4.3 Cadence Waveforms

Similarly as in the PowerPC 603 master slave latch simulations on 130nm process I generated the input square like wave using verilogA for the modified C²MOS latch simulations in 130nm process. Figure 8.13 shows the input and output waveform of modified C²MOS latch.

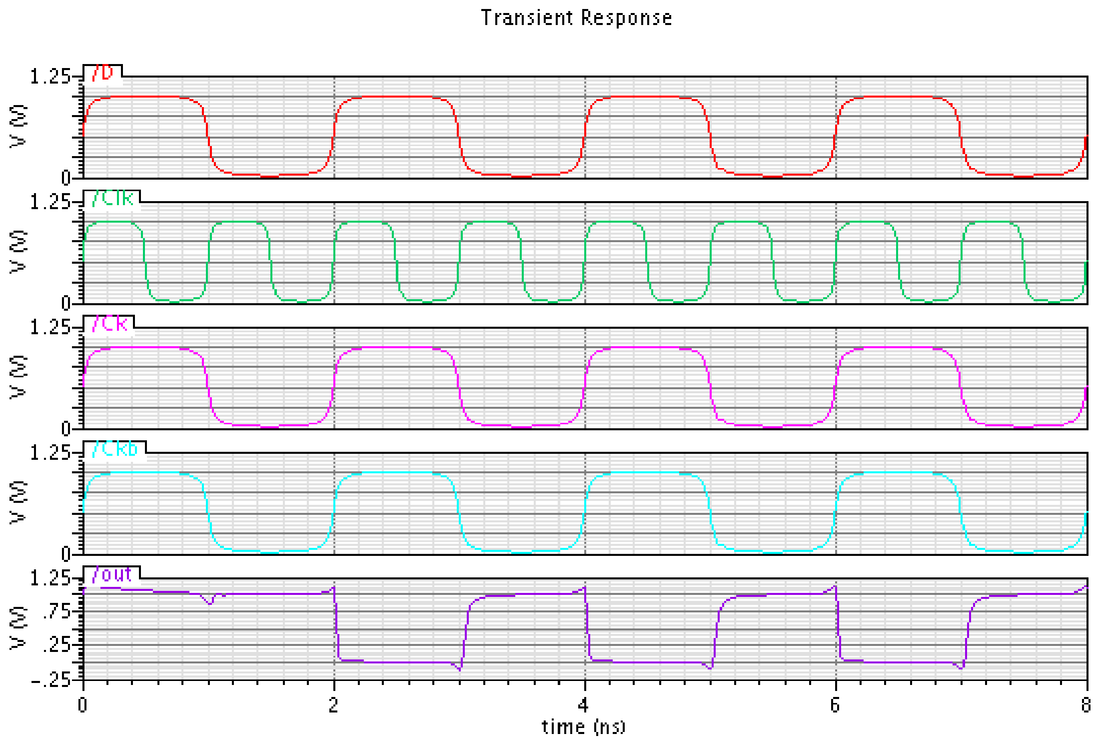

Fig 8.13: Modified C²MOS Latch input and output waveforms

Minimum setup, minimum hold and clock-Q delay are given below

Minimum set up time= 0.90 ns

Minimum hold time = 0.13 ns

Clock to output delay = 0.07 ns

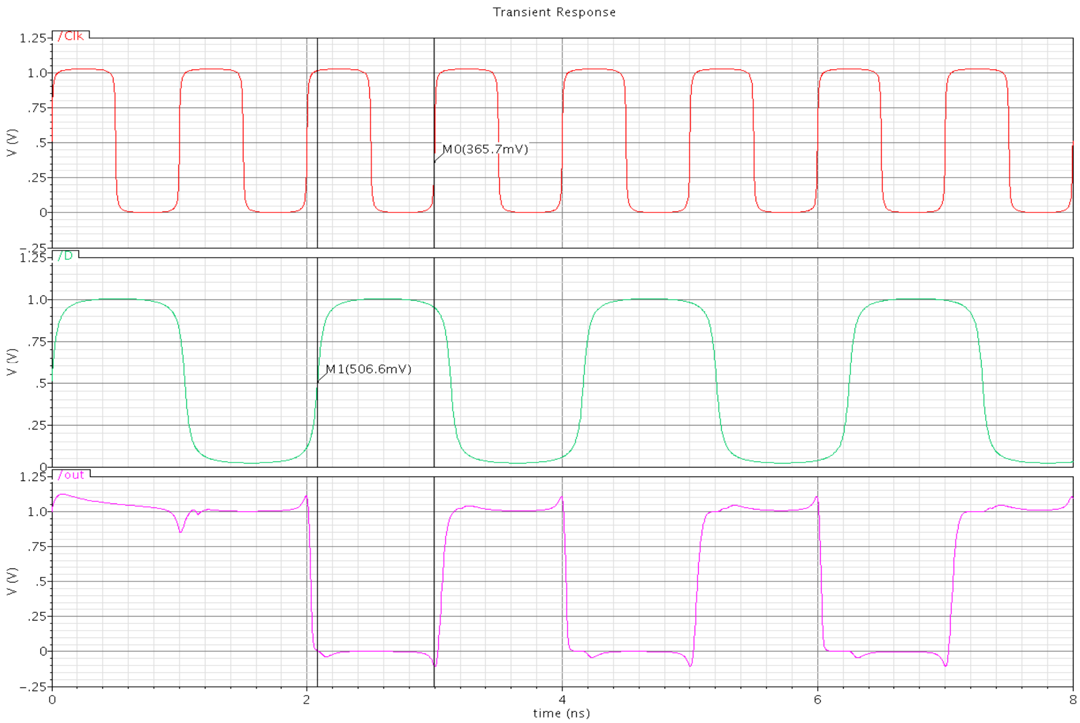

Fig 8.14: Minimum setup time calculations

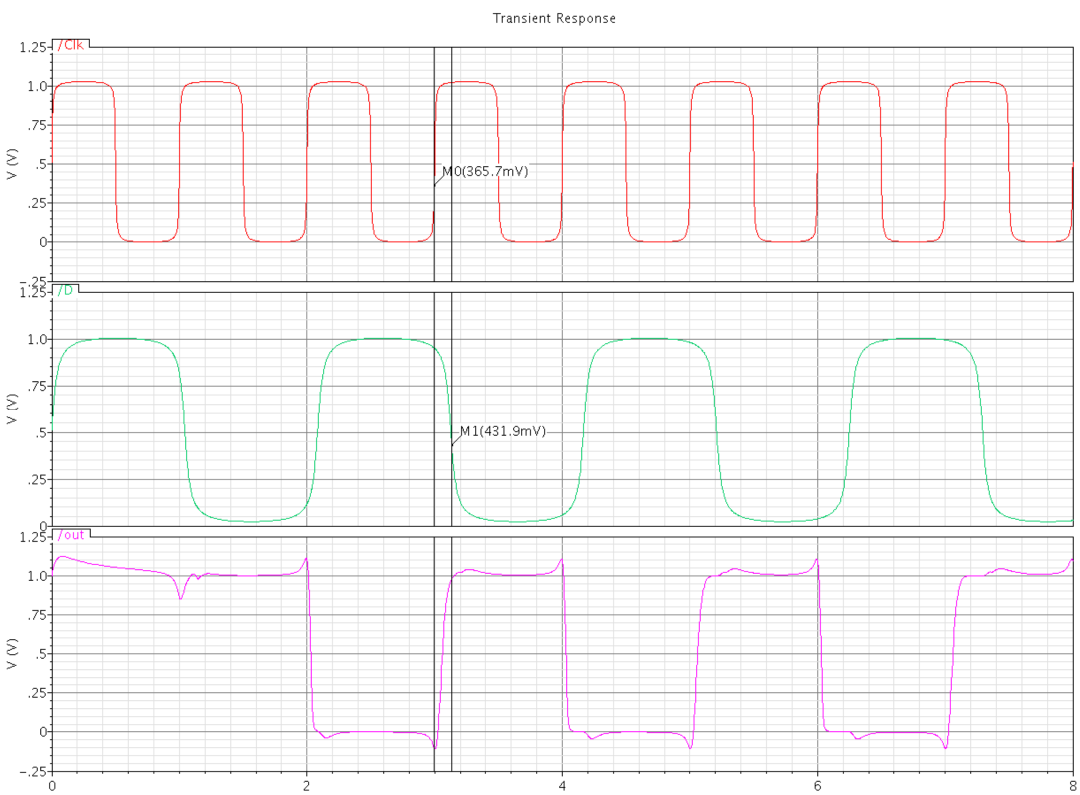

Fig 8.15: Minimum hold time calculations

8.4.4 Internal Node waveforms to check the device sizes

Figure 8.16 shows the waveforms of internal nodes as described in section 8.3.5.

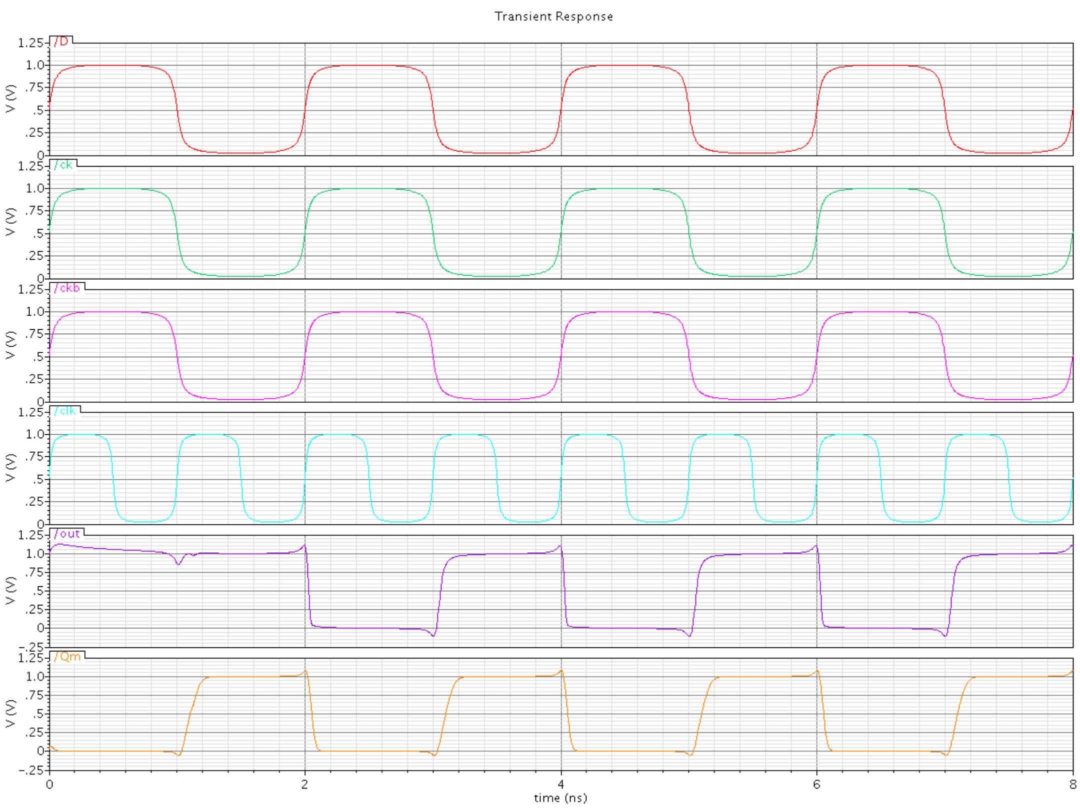

Fig 8.16: Modified C²MOS Latch internal node waveforms

8.4.5 Power waveforms

Total power dissipation waveform of modified C²MOS latch is given by the figure 8.17. Total power dissipation is sum of three power dissipations i.e. internal power dissipation of latch, local data and local clock power dissipations. Supply voltage in this simulation is 1V and the average power dissipation is 181.6 µW. The appearance of is like pulse train and is because of switching activity as described in section 8.3.6.

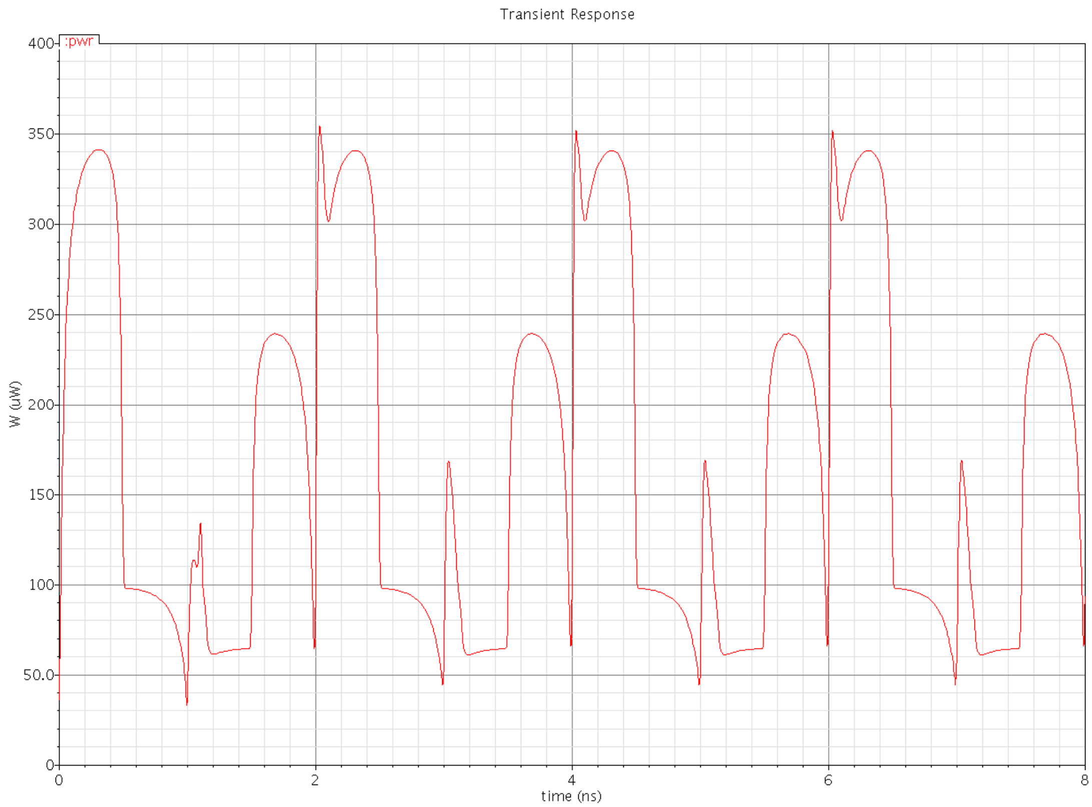

Fig 8.17: Waveforms of total power dissipation in modified C²MOS Latch

8.4.6 Matlab Waveforms

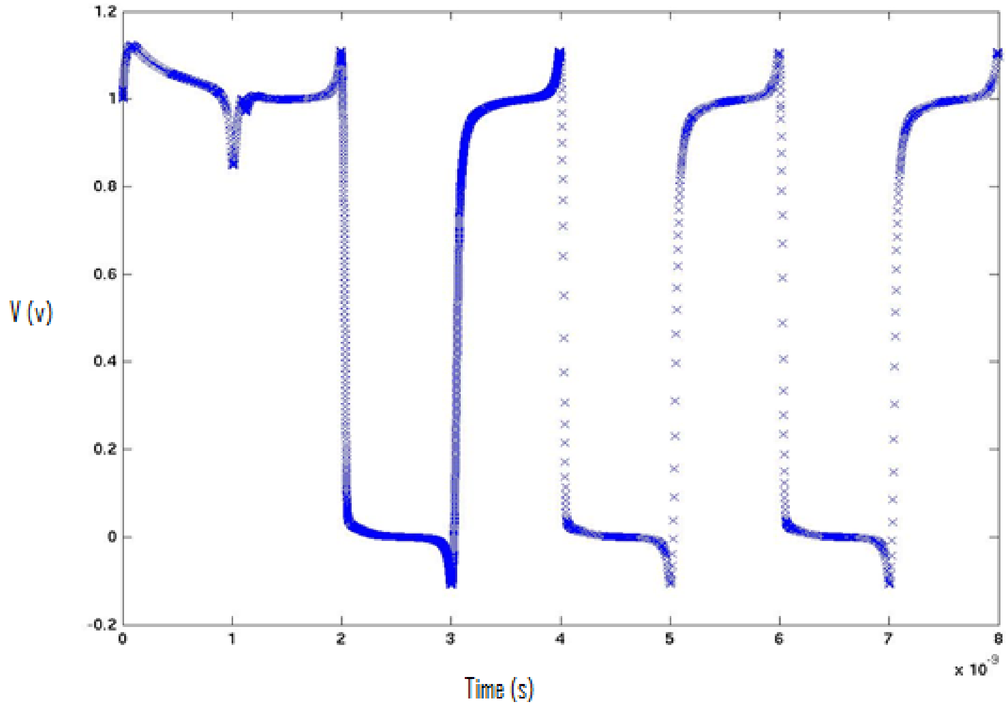

Fig 8.18: Modified C²MOS Latch output waveforms on Matlab

8.4.7 Matlab waveforms of one cycle

Matlab waveform of first cycle is given by the figure 8.19.

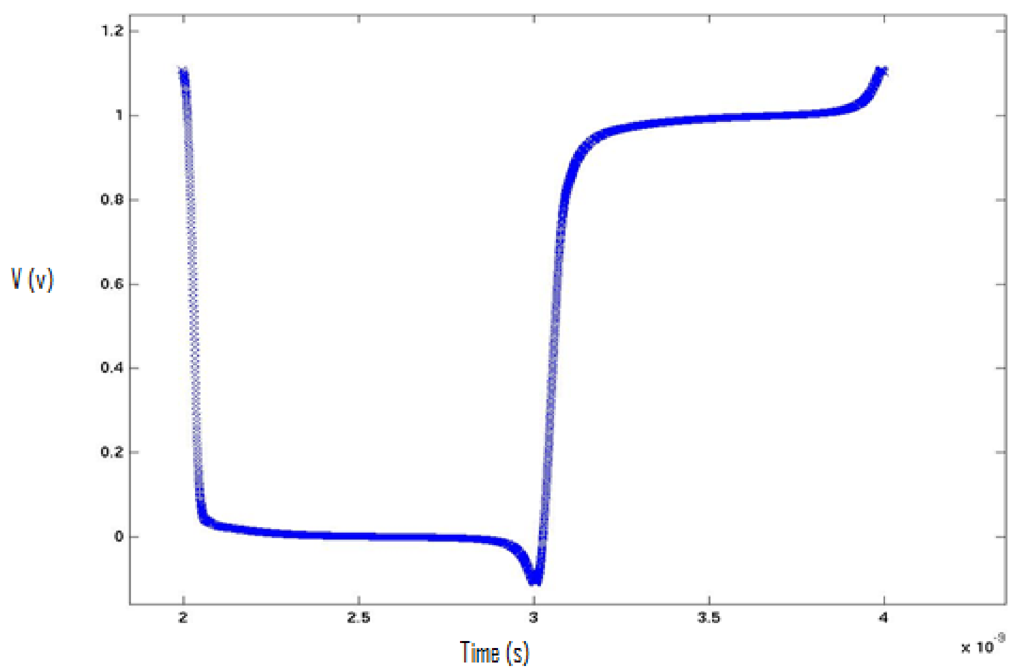

Fig 8.19: Modified C²MOS Latch output waveforms on Matlab (one cycle)

8.4.8 Matlab Spectrum Plot

Spectrum plot of switching waveform of modified C²MOS latch is given by the figure 8.20. Spectrum roll-off is about 70 dB/ decade.

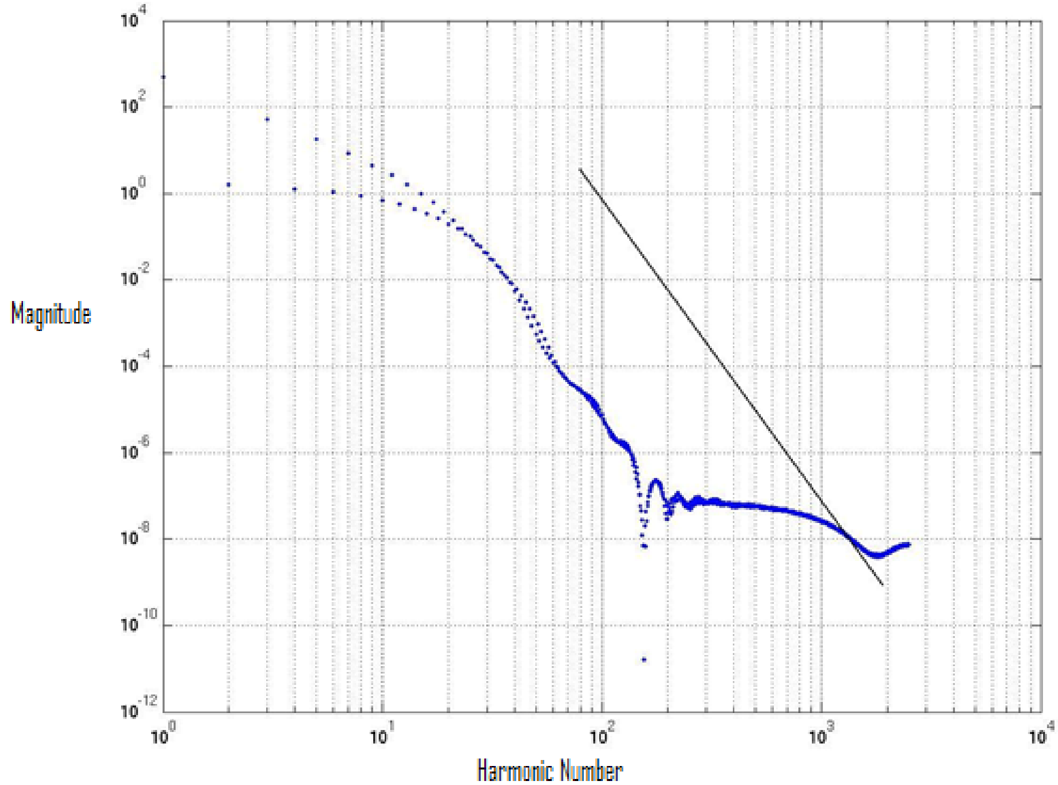

Figure 8.20: Spectrum plot of Modified C²MOS Latch switching waveforms

8.5 Flip Flop 3 Topology

Third flip flop topology which I simulated was Hybrid-Latch Flip Flop (HLFF). It is low power structure and its performance is better than other two structures. All Simulations were performed with Spectre simulator using 130 nm process.

8.5.1 Hybrid-Latch Flip Flop (HLFF)

First stage of hybrid-latch flip flop is a pulse generator that generates a pulse on the rising edge of the clock, while the second stage of HLFF is a latch that captures the pulse generated in the first stage of the HLFF circuit [2]. It is also important to note that the power is always consumed in clocked pulse generator.

HLFF structure has the following properties [2]:

- Flip flop is edge triggered on one edge of clock
- Single phase clock
- Latch has brief transparency and is equal to three inverter delays
- It is must to control the delay between the flip flops (HLFF delay is comparable to hold time)
- Fully static
- Possible to incorporate logic

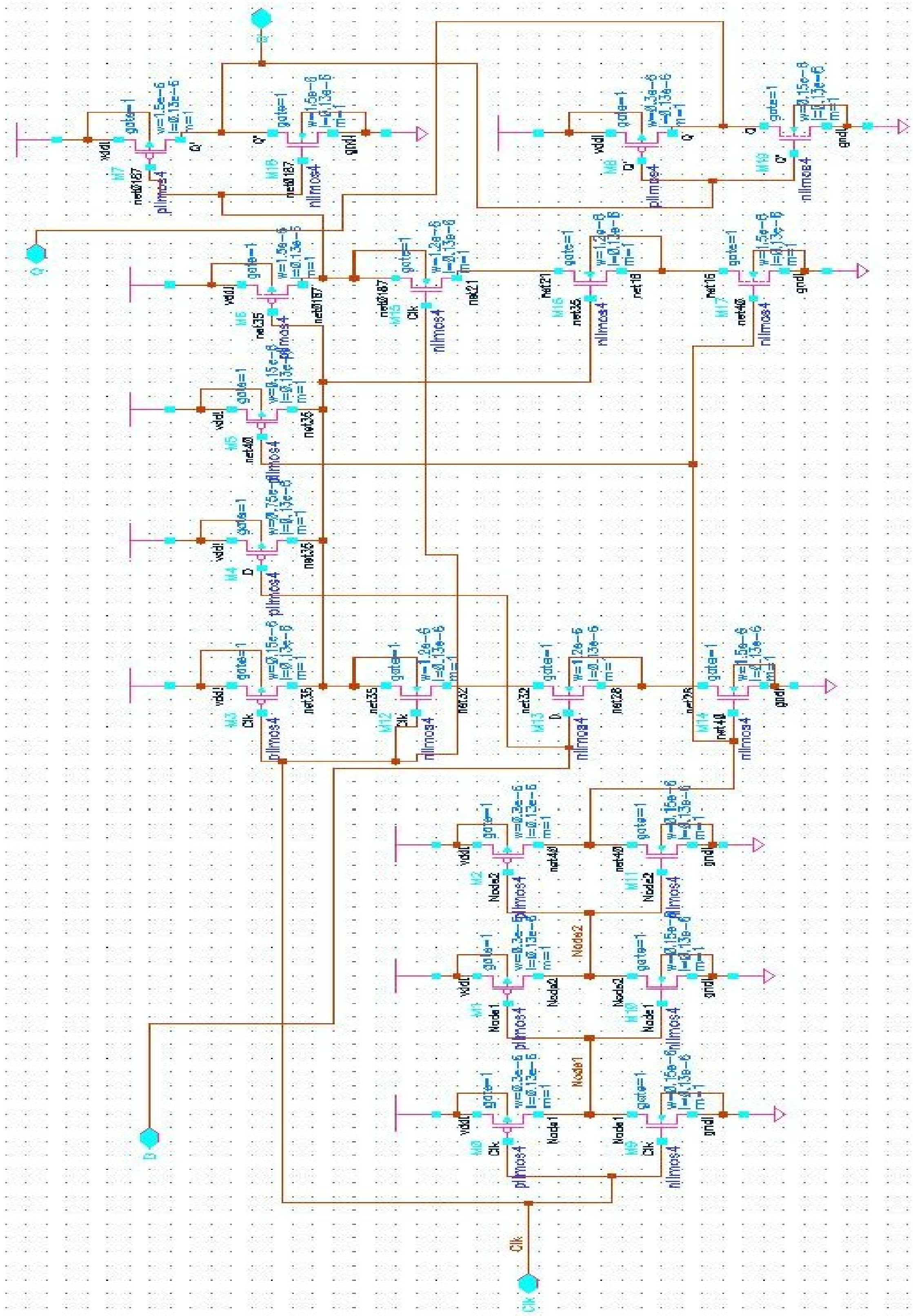

Fig 8.21: Hybrid-Latch Flip Flop (HLFF) Schematics

8.5.2 Test Bench

The test bench for the simulation of Hybrid-Latch flip flop (HLFF) is given by the figure 8.22.

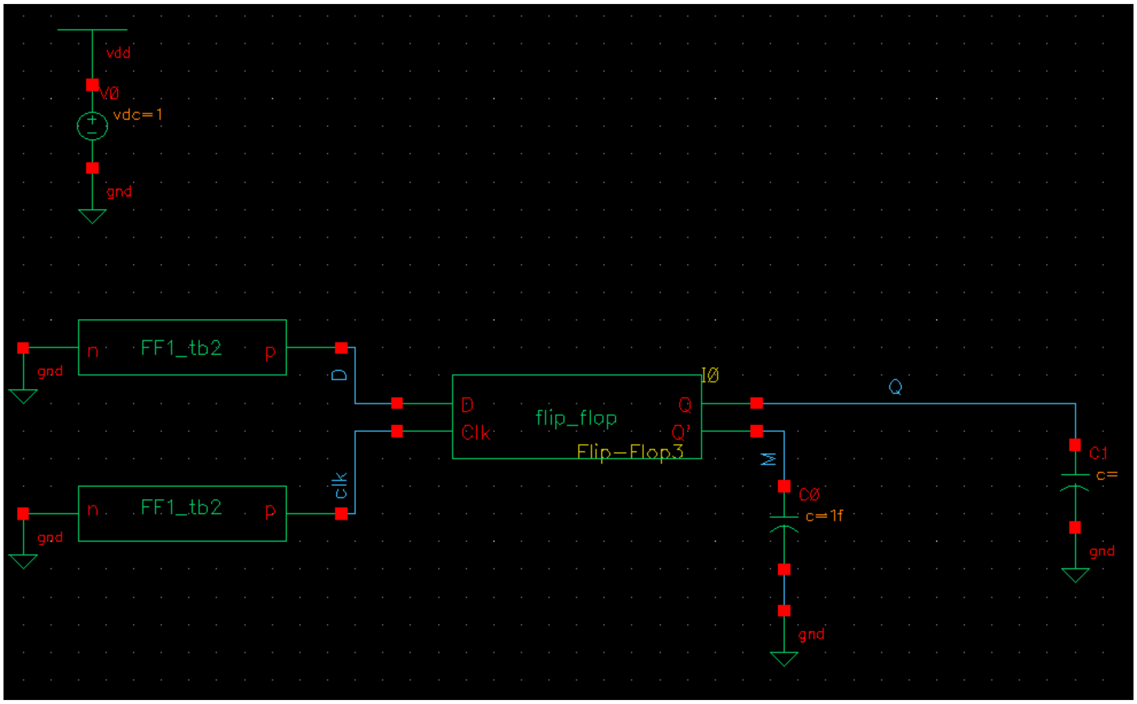

Fig 8.22: Hybrid-Latch Flip Flop (HLFF) test bench

8.5.3 Cadence waveforms

Similarly as in PowerPC 603 master slave latch and modified C^2MOS latch simulations; I generated the input square like wave using verilogA for the Hybrid latch flip-flop (HLFF) simulations. Figure 8.23 shows the input and output waveform of Hybrid latch flip-flop (HLFF).

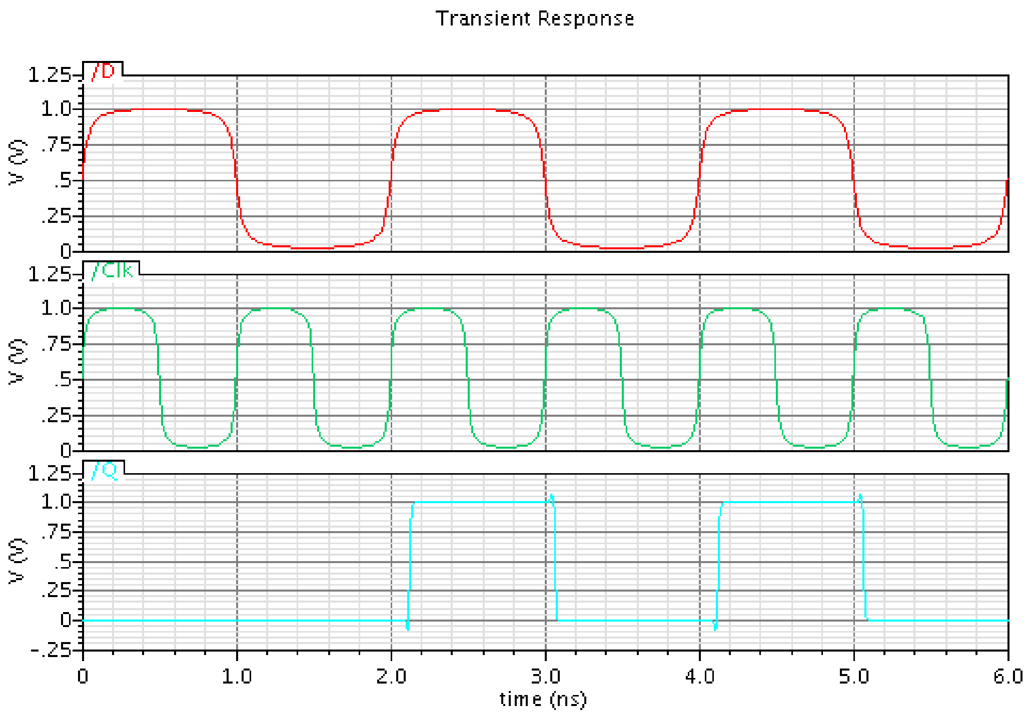

Fig 8.23: Hybrid-Latch Flip Flop (HLFF) input and output waveforms

Minimum setup, minimum hold and clock to output delay times are given by

Minimum set up time= - 0.071 ns

Minimum hold time = 0.21 ns

Clock to output delay = 0.12 ns

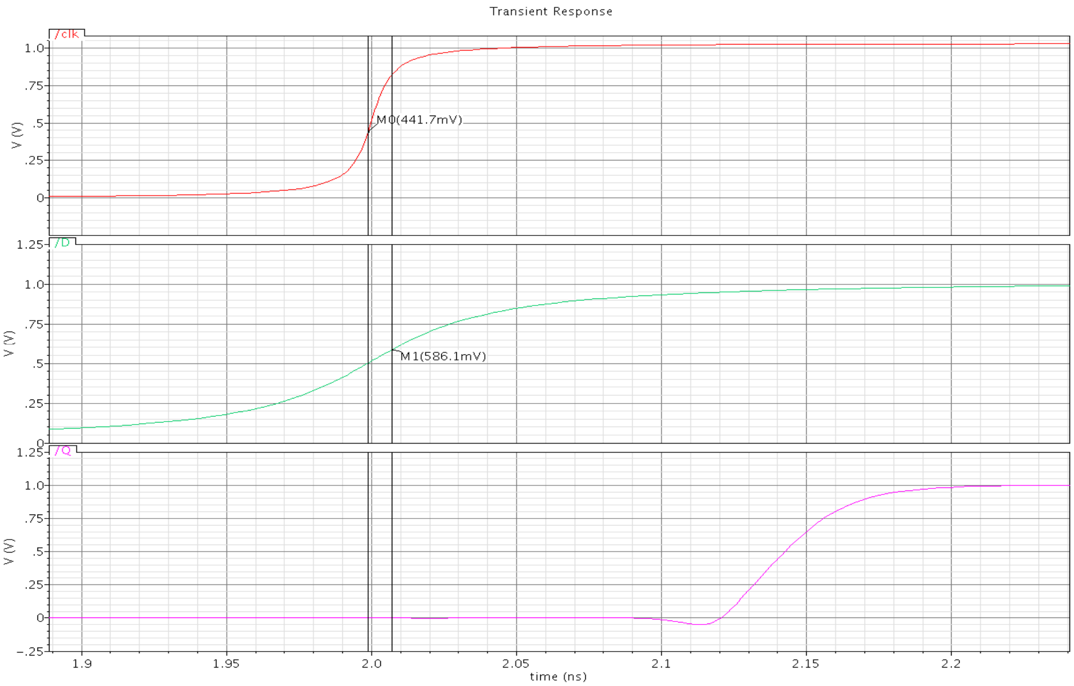

Fig 8.24: Minimum setup time calculations

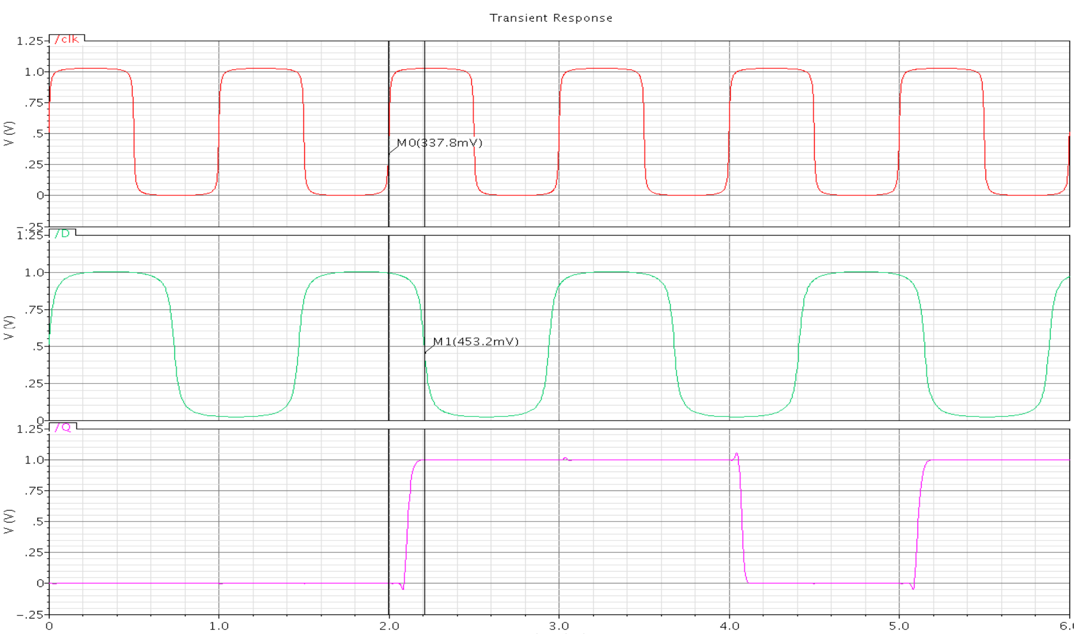

Fig 8.25: Minimum delay time calculations

8.5.4 Internal Node waveforms to check the device sizes

Figure 8.26 shows the waveforms of internal nodes of Hybrid-Latch Flip Flop (HLFF) as described in section 8.3.5.

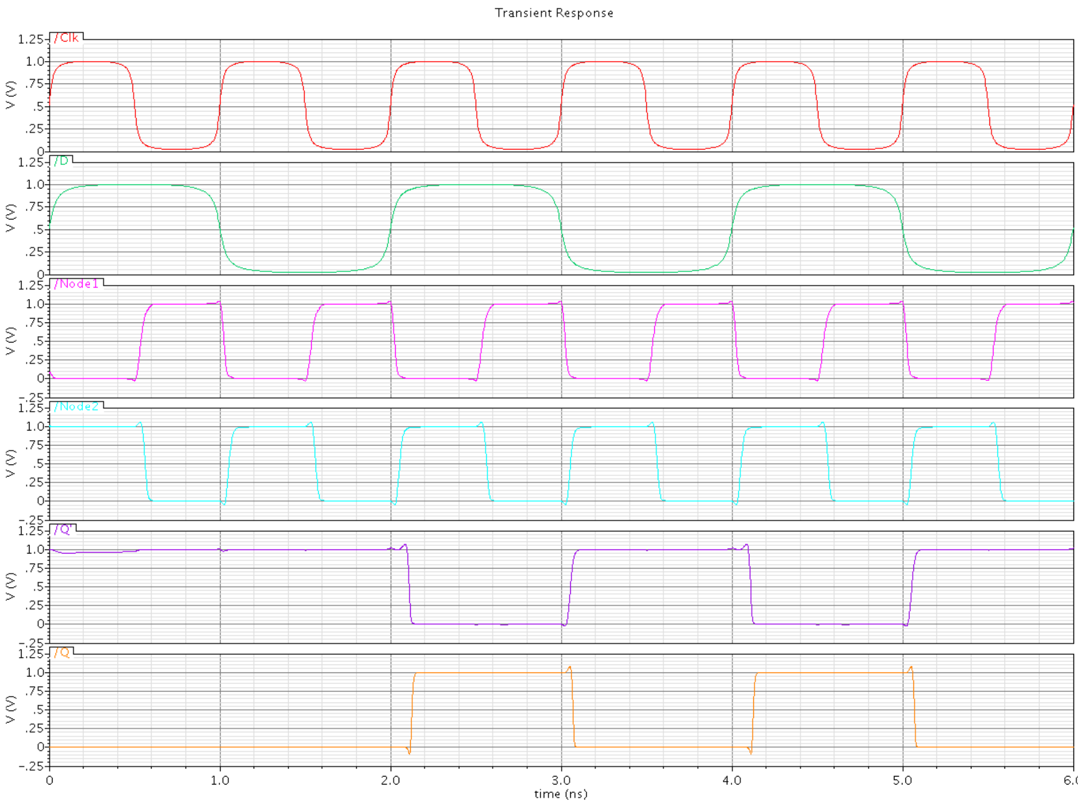

Fig 8.26: Hybrid-Latch Flip Flop (HLFF) internal node waveforms

8.5.5 Power waveforms

The total power dissipation waveform for the whole hybrid latch flip-flop (HLFF) is given by the figure 8.27. The appearance of plot is like pulse train and is because of switching activity as described in section 8.3.6. In some intervals power doesn't go back to zero and is because of static current flows or the capacitors are not fully charged. The supply voltage in this simulation is 1V and the average power dissipation of this plot is 21.19 µW.

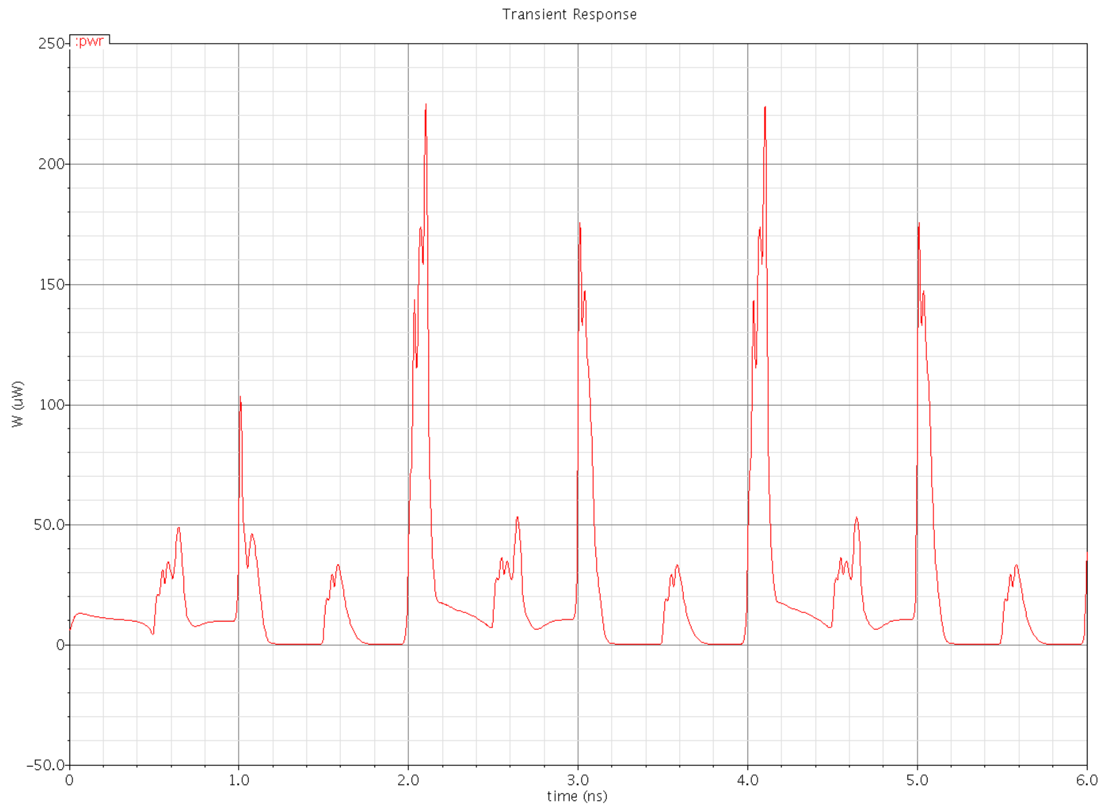

Fig 8.27: Waveforms of total power dissipation in Hybrid-Latch Flip Flop (HLFF)

8.5.6 Matlab Waveforms

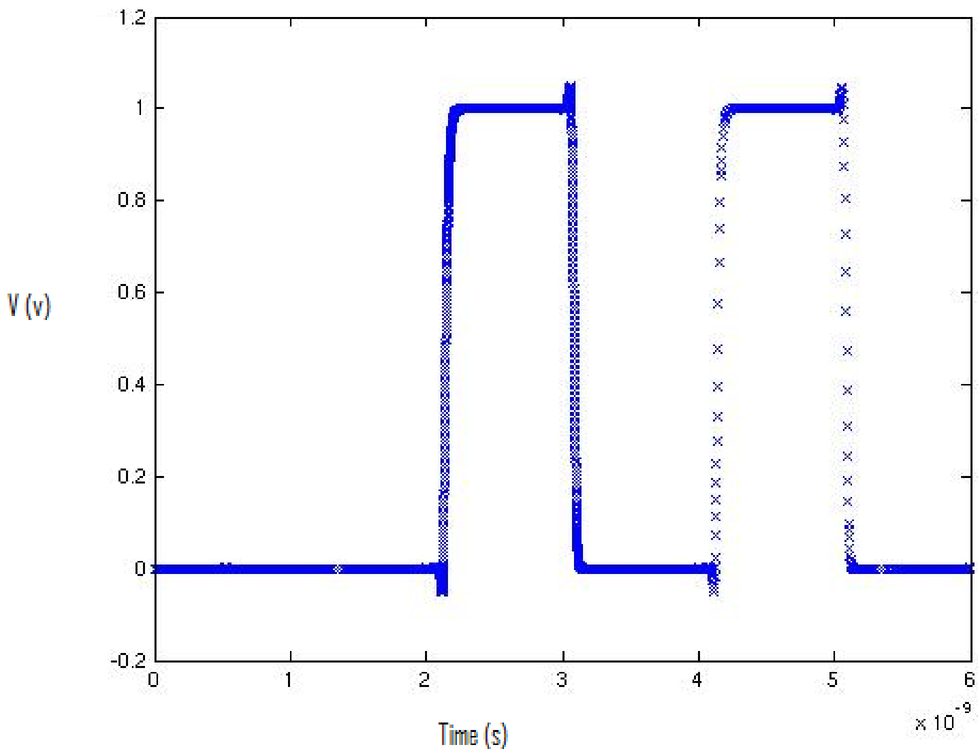

Fig 8.28: Hybrid-Latch Flip Flop (HLFF) output waveforms on Matlab

8.5.7 Waveform of one cycle

The Matlab waveform of first cycle is given by the figure 8.29.

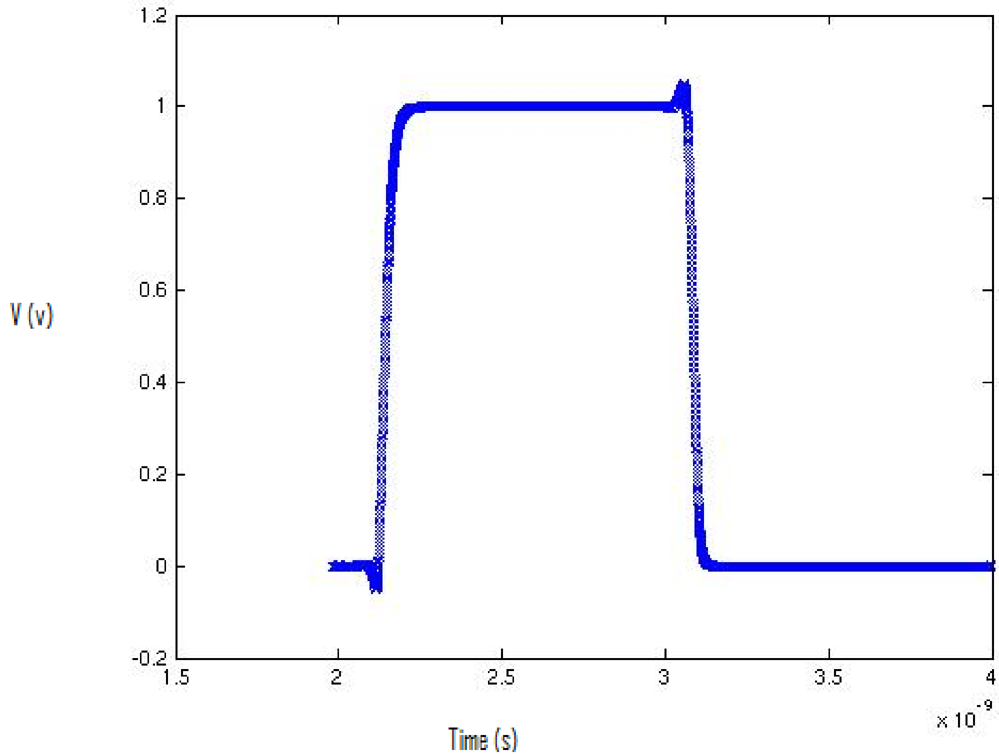

Fig 8.29: Hybrid-Latch Flip Flop (HLFF) output waveforms on Matlab (one cycle)

8.5.8 Matlab spectrum plots

Finally the Matlab spectrum of the switching waveform of HLFF is given by the figure 8.30. Spectrum roll-off is about 105 dB/decade.

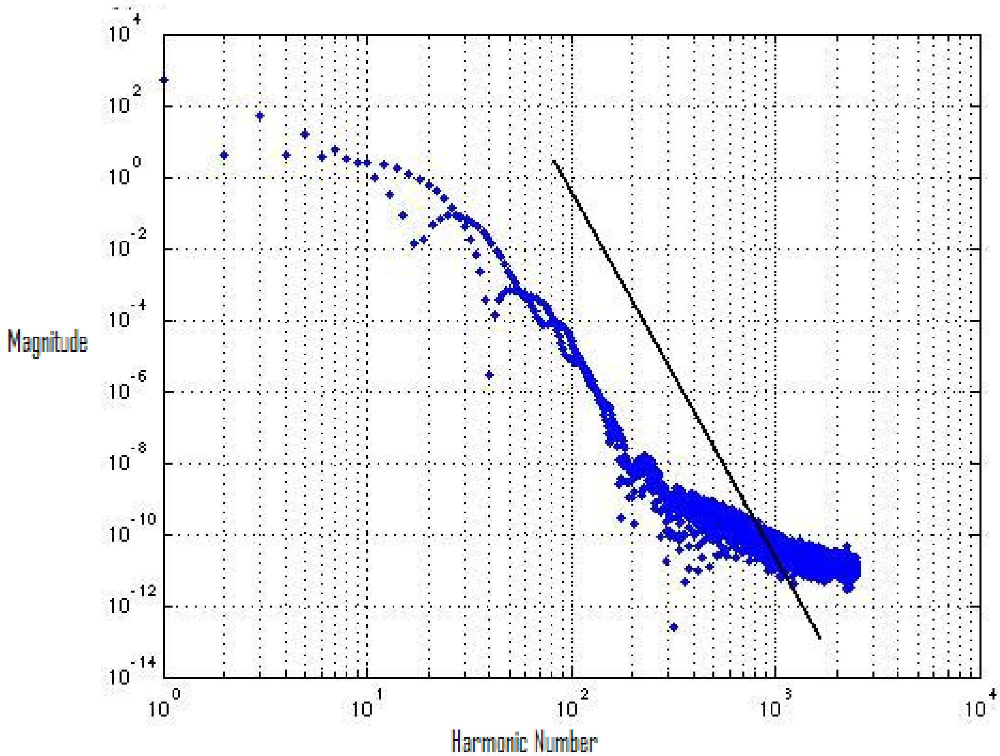

Figure 8.30: Spectrum plot of Hybrid-Latch Flip Flop (HLFF) switching waveforms

9 Comparison between Flip-Flop topologies

We can see that the less power dissipation occurs in hybrid latch flip-flop (HLFF) while modified C^2MOS latch dissipates maximum power and the power dissipation of PowerPC 603 master slave latch is between these two if we compare the readings of these three topologies power dissipation. We can also note that the power dissipation in PowerPC 603 master slave latch and hybrid latch flip-flop (HLFF) is not much different.

Table below shows the power dissipation values of three different flip-flop structures.

S/No.	Flip flop topology	Average power dissipation	Peak value of Power dissipation
1	PowerPC 603 Master slave latch	25.08 µW	210 µW
2	Modified C^2MOS latch	181.6 µW	352 µW
3	hybrid latch flip-flop (HLFF)	21.19 µW	222 µW

Table below shows the timing performance of all three flip flop topologies.

S/No.	Flip flop topology	Minimum Set up time (ns)	Minimum Hold time (ns)	Clock-Q delay (ns)
1	PowerPC 603 Master slave latch	0.12	0.14	0.07
2	Modified C^2MOS latch	0.90	0.13	0.07
3	hybrid latch flip-flop (HLFF)	-0.071	0.21	0.12

In switching waveform spectrum analysis we can see that the steeper roll-off is given by hybrid latch flip-flop (HLFF).

S/No.	Flip flop topology	Roll-off in Switch waveform spectrum
1	PowerPC 603 Master slave latch	80 dB/decade
2	Modified C^2MOS latch	70 dB/decade
3	hybrid latch flip-flop (HLFF)	105 dB/decade

So we can conclude the Hybrid Latch Flip Flop (HLFF) is best among the three flip flop topologies.

10 Conclusions

Transistor model quality is important in accurate estimation of harmonic contents. The input signal which I used in all simulations was a square like wave; it was neither a sinusoid nor a square wave. A sinusoid wave is with slower edges and causes extra short circuit power while the use of a square wave produces discontinuity in the output and its derivatives. Higher order harmonics generates noise contents while discontinuity decreases the switching waveform spectrum roll-off.

Comparison between 65nm and 130nm was also done on the basics of simulation results of inverter, roll-off of spectrum of switching waveforms using 65nm process was steeper than 130nm process and the rise time of inverter output wave using 65nm process was also less than 130nm process.

Simulations of three topologies of flip flop structures were done with Spectre simulator using 130 nm process. It is clear that the less average power dissipation occurs in hybrid latch flip-flop (HLFF) and it has switching spectrum roll-off of 105 dB/decade and timing delay is also less than other two topologies, while modified C^2MOS latch dissipates maximum average power and its switching spectrum roll-off is 70 dB/decade and timing delay is greater than the other two topologies and the performance of PowerPC 603 Master slave latch is between these two if we compare the readings of these three topologies in terms of average power dissipation, timing delay and spectrum roll-off. Spectrum roll off of PowerPC 603 Master slave latch is 80 dB/decade. We can also note that the power dissipation in PowerPC 603 master slave latch and hybrid latch flip-flop (HLFF) is not much different. So according to all the simulation results, HLFF was best among the three flip flops.

References

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