Investigation of the interface between silicon nitride passivations and AlGaN/AlN/GaN heterostructures by C(V) characterization of metal-insulator-semiconductor-heterostructure capacitors

M. Fagerlind,[1,a] F. Allerstam,[1] E. Ö. Sveinbjörnsson,[1,3] N. Rorsman,[1] A. Kakanakova-Georgieva,[2] A. Lundskog,[2] U. Forsberg,[2] and E. Janzén[2]
[1]*Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Göteborg, Sweden*
[2]*Department of Physics, Chemistry and Biology, Linköping University, SE-58183 Linköping, Sweden*
[3]*Science Institute, University of Iceland, 107 Reykjavik, Iceland*

(Received 15 February 2010; accepted 17 April 2010; published online 13 July 2010)

Capacitance-voltage [C(V)] measurements of metal-insulator-semiconductor-heterostructure capacitors are used to investigate the interface between silicon nitride passivation and AlGaN/AlN/GaN heterostructure material. AlGaN/AlN/GaN samples having different silicon nitride passivating layers, deposited using three different deposition techniques, are evaluated. Different interface state distributions result in large differences in the C(V) characteristics. A method to extract fixed charge as well as traps from the C(V) characteristics is presented. Rough estimates of the emission time constants of the traps can be extracted by careful analysis of the C(V) characteristics. The fixed charge is positive for all samples, with a density varying between 1.3×10^{12} and 7.1×10^{12} cm^{-2}. For the traps, the peak density of interface states is varying between 16×10^{12} and 31×10^{12} cm^{-2} eV^{-1} for the three samples. It is concluded that, of the deposition methods investigated in this report, the low pressure chemical vapor deposited silicon nitride passivation shows the most promising results with regards to low densities of interface states. © *2010 American Institute of Physics*. [doi:10.1063/1.3428442]

I. INTRODUCTION

Heterostructure surface passivation plays a crucial role in the GaN-based heterostructure field effect transistor (HFET) technology. The passivation has been shown to be necessary to reduce the influence of dispersion.[1] In this report capacitance-voltage [C(V)] measurements of metal-insulator-semiconductor-heterostructure (MISH) capacitors are utilized to characterize the interface between the heterostructure and the passivation layer.

A number of C(V) characterization techniques have been used for decades to investigate the oxide/silicon interface in silicon based metal oxide semiconductor structures.[2] C(V) analysis of metal-insulator-semiconductor (MIS) capacitors based on GaN and AlGaN have also been reported.[3–5] However it is more relevant to investigate MISH capacitors since they resemble the actual heterostructure used in HFETs. Chen *et al.*[6] investigate GaN-based MIS and MISH structures deposited with a SiO_2 passivation. Liu *et al.*[7] measure C(V) characteristics of a HfO_2 passivated AlGaN/GaN heterostructure. In a more recent report Miczek *et al.*[8] investigate MISH capacitors passivated with silicon nitride and Al_2O_3 dielectrics. In their study the interface state density at the passivation interface was deduced from C(V) in a bias region near depletion of the heterostructure. The investigation presented here is a more general study of the C(V) behavior of MISH capacitors. It is demonstrated that it is possible to classify interface traps at the passivation interface in terms of their effect on the C(V) characteristic. Furthermore, a method of extracting emission time constants and activation energies from the C(V) characteristics is demonstrated.

Three silicon nitride passivation layers, deposited using different deposition techniques, are evaluated. The deposition techniques are: low pressure chemical vapor deposition (LPCVD),[9] reactive sputtering (RS),[10] and plasma enhanced chemical vapor deposition (PECVD).[11]

II. EXPERIMENT

A. The MISH-capacitor structure

The MISH-capacitor structure and a schematic drawing of the energy bands as a function of depth into the device is shown in Fig. 1. The metal gate contact is isolated from the

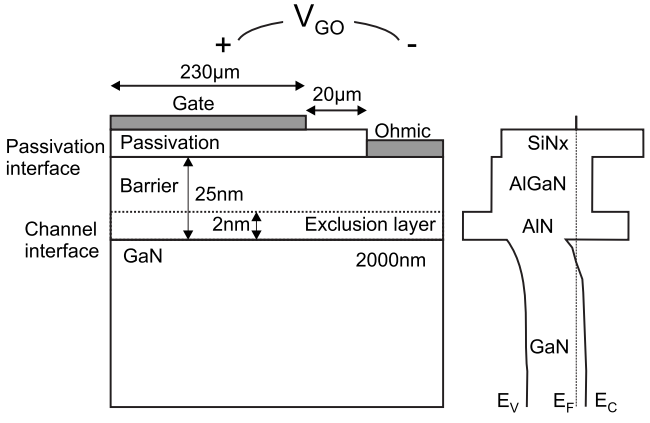

FIG. 1. Schematic drawings of the MISH-capacitor structure and the energy bands. V_{GO} is the voltage applied between the gate and Ohmic contact.

[a]Electronic mail: martin.fagerlind@chalmers.se.

semiconductor by a silicon nitride passivation layer. The Ohmic contact is providing a low loss resistive contact to the two-dimensional electron gas (2DEG) that is formed below the interface between the AlN and GaN layer. The gate contact is a square contact with dimensions $230 \times 230\ \mu m^2$.

The heterostructure material is epitaxially grown on a 3 inch semi- insulating SiC wafer. The growth was performed in a horizontal hot-wall metal-organic chemical-vapor deposition reactor.[12] The reactor is designed to reduce vertical and horizontal temperature gradients in order to obtain a high cracking efficiency of precursor gases and a reduction in bowing of the substrates during growth.[13,14] A high resistive buffer layer can be obtained by optimizing the V/III ratio during growth of the GaN buffer layer. Typical growth temperature was 1100 °C (AlN growth) and 1000 °C (GaN and AlGaN growth).[15] In this work an AlGaN/AlN/GaN heterostructure has been used. Inclusion of an AlN exclusion layer reduces the spreading of electrons into the barrier layer and results in higher electron mobility.[16] However, the method described in this paper is general and should be useful for characterization of interfaces between any heterostructure and a dielectric. After growth, an initial mercury-probe, C(V) measurement is performed. This measurement is used to extract 2DEG sheet carrier density, n_s, and the barrier layer thickness. For the material in this report the aluminum concentration in the barrier is 23% and the total barrier was measured to be 25 nm thick, out of which the exclusion layer is 2 nm.

In the discussion below the interface between the passivation and the barrier will be referred to as the *passivation interface*, while the interface between the barrier and the channel will be referred to as the *channel interface*.

B. MISH-capacitor fabrication

Fabrication starts with degreasing of the samples using acetone and isopropyl alcohol. The samples are then cleaned in RCA1 ($H_2O:NH_4OH:H_2O_2$) and RCA2 ($H_2O:HCl:H_2O_2$) solutions, both heated to 70 °C. Ohmic contacts are formed by deposition and rapid thermal annealing (RTA) of a Ti/Al/Ni/Au metal stack. A two-step RTA (30 s at 680 °C and 30 s at 830 °C in an N_2 atmosphere) of the samples results in a contact resistivity of $r_c = 0.3\ \Omega$ mm. Silicon nitride is deposited using three different deposition methods: LPCVD, RS, and PECVD. The three samples will be referred to as the LP, RS, and PE samples, respectively. The RS and PECVD nitrides are deposited after the RTA step. The LPCVD nitride has to be deposited before the Ohmic contact process in order to prevent metal contamination of the deposition furnace.

The LPCVD nitride is deposited in a tube furnace with the precursor gases H_2SiCl_2 and NH_3 at a flow ratio of 1:6. The temperature and pressure during deposition are 770 °C and 150 mTorr, respectively. The RS nitride is deposited by sputtering of a silicon target in a nitrogen ambient. The first RS process step is plasma cleaning of the surface (50 W in Ar ambient). During RS deposition the power is stepwise increased from 30 to 160 W, while the pressure is increased from 7 to 10 mTorr in two steps.[10] The PECVD nitride is deposited utilizing a dual frequency[11] (380 kHz and 13.56 MHz) plasma with SiH_4(2%) and NH_3 gases at a flow ratio of 200:3. The deposition temperature was 300 °C and the pressure was 250 mTorr. The passivation thicknesses were 52 nm, 63 nm, and 78 nm for the LP, RS, and PE nitrides, respectively. Silicon wafers have also been deposited with the same nitrides. Ellipsometer measurements on the these wafers show that the refractive indices of the nitrides where 2.01, 1.99, and 1.94 for the LP, RS, and PE nitrides, respectively, (ellipsometer wavelength was 632 nm).

An NF_3 based reactive ion etch is used to etch probe openings to the Ohmic contacts of the RS and PE samples. The same process is used to etch openings before deposition of Ohmic contacts on the LP sample. The gate electrodes are formed by electron beam evaporation of a Ni/Au bilayer.

C. Measurement procedure

C(V) characteristics have been measured using an HP4284A LCR meter. The data is presented using the parallel capacitance-conductance (Cp-G) model.[17] The bias sweep rate is approximately 0.1 V/s and the frequency of the small signal sinusoidal voltage (hereafter referred to as the *test signal*) is varied between 1 and 100 kHz. The bias voltage V_{GO} is first swept from a negative value to a value above 0 V (labeled as *forward sweep*) and then back to the starting bias (*reverse sweep*).

III. THEORY

A. Data interpretation

Figure 2 presents the forward sweep C(V) characteristic of the LP sample. Similar curves can also be found in other reports.[18,19] The characteristic can be split into three intervals. The small MISH structure in each interval of the characteristic schematically presents the depletion region (dashed region) and electron distribution (minus signs) in the structure. Starting from negative V_{GO}, the close to zero capacitance is due to depletion of the 2DEG channel under the gate metal. With increasing V_{GO}, electrons start to accumulate at the channel interface, thus forming the 2DEG. The peak in conductance is an effect of a large displacement current associated with filling of the 2DEG. The 2DEG accumulation

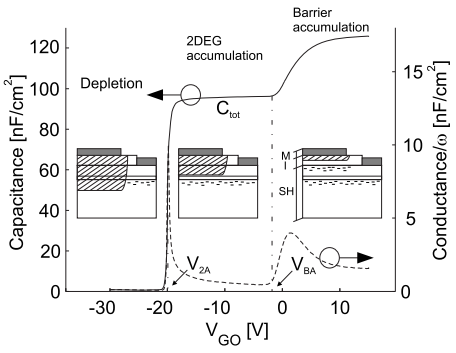

FIG. 2. 100 kHz C (V) curves for the LP MISH-capacitor, the solid curve is the capacitance and the dashed curve is the conductance divided by the angular frequency, ω. The characteristic can be split into three intervals, the depletion region and electron distribution is schematically presented for each interval.

region has a constant capacitance designated the total capacitance (C_{tot}). The situation can be approximated with a parallel plate capacitor using the 2DEG and the gate metal for conductive surfaces, with a dielectric containing both the barrier and the passivation.[7] The voltage where the capacitance is half of C_{tot} is arbitrarily chosen as the 2DEG accumulation voltage (V_{2A}). V_{2A} is correlated with the pinch-off voltage of a MISHFET device.[7,19]

At gate biases higher than the barrier accumulation voltage (V_{BA}) electrons will start to transfer into the barrier of the heterostructure. V_{BA} is arbitrarily chosen where there is a substantial increase in the slope of the capacitance curve. At a sufficiently large forward bias, electrons will start to accumulate at the passivation interface, at which stage a parallel plate capacitor with the capacitance of the passivation (C_{pass}) can be used as a model. The increase in conductance above V_{BA} is due to a displacement current associated with the charge redistribution. Electrons are moving in the barrier from the Ohmic contact region to accumulate at the passivation interface. However there are also electrons tunneling through the exclusion layer. Both conduction processes are associated with a larger series resistance than that of the filling of the 2DEG. The series resistance will result in a larger deviation from the Cp-G model, which in turn can result in frequency dispersion. The conductance curve is presented to show that it is behaving in a physically intuitive way, which indicates that the Cp-G model is a reasonable approximation of the structure. The information provided by the conductance curve is not further used for analysis of the samples.

From inspection of the MISH structure it can be concluded that C_{tot} is a series connection of C_{pass} and the capacitance of the barrier layer, C_{barr}

$$C_{tot} = \frac{C_{pass} C_{barr}}{C_{pass} + C_{barr}}. \tag{1}$$

It should be mentioned that the capacitance values calculated using the parallel-plate capacitor formula should be higher than those measured, since electrons in the real structure are not all located at the interfaces. The electron distribution is in reality extending deeper into the semiconductor material, resulting in an effectively thicker dielectric medium.

B. Passivation interface states

The C(V) characteristic is affected when states are introduced at the passivation interface. This work proposes that the passivation interface states are divided into two general categories, fixed charge and traps. The traps are then further classified according to their effect on the C(V) characteristic.

An ideal MISH structure is used for setting absolute numbers on the densities of the interface states. The ideal structure is assumed to have a reference sheet density, n_{ref}, at zero applied gate voltage. At positive gate bias, electrons of the ideal structure are starting to transfer to the barrier, i.e., $V_{BA}=0$ V. The implication is that: $V_{2A}=-qn_{ref}/C_{tot}$ for the ideal structure. The reference sheet density is obtained by Hall measurement on a piece of material before annealing, a material characterization method using nonannealed Ohmic contacts[20] was used. The reference value was measured to be $n_{ref}=9.7\times10^{12}$ cm^{-2} with a Hall mobility of 2170 cm^2/V s, resulting in a sheet resistance of 297 Ω/sq.

Fixed positive (negative) charge at the passivation interface will shift the curve in negative (positive) voltage direction. The voltage shift compared to the ideal characteristic is equal to $\Delta V=-qN_{fix}C_{pass}$, where N_{fix} is the number of fixed charges per unit area. Fixed charge at the passivation interface is extracted using Eq. (2)

$$N_{fix} = \left(-\frac{qn_{ref}}{C_{tot}} - V_{2A} \right) \frac{C_{pass}}{q}. \tag{2}$$

Traps have different emission and capture time constants. The trap carrier capture rate is determined by $n\ c_n$ with n and c_n are the electron density at the trap location and the capture coefficient, respectively. Time constants, τ_n, associated with electron emission of trapped electrons are described by Eq. (3)[21]

$$\tau_n = \frac{1}{e_n} = \frac{1}{\sigma_n v_{th} N_C} e^{E_a/k_B T}, \tag{3}$$

where e_n is the electron emission rate, σ_n is the electron capture cross- section, v_{th} is the thermal velocity, N_C is the effective density of states in the conduction band, k_B is the Boltzmann constant, T is the absolute temperature, and E_a is the activation energy of the trap.

The trap can be said to be either slow or fast. Which group it belongs to depends on if the time associated with trap capture and emission is longer or shorter than the period of the test signal. The emission time is assumed to limit the capture-emission process since trap emission is normally much slower than trap capture. If the trap has an emission time constant longer than the period of the test signal, the trap is defined as slow. Electrons trapped by slow traps cannot respond to the test signal. Hence, the effect of the slow traps is detected when V_{BA} is shifted compared to the ideal value. Traps of the slow type will be designated N_{slow} and are extracted using Eq. (4)

$$N_{slow} = \left[V_{BA,lf} - \left(V_{2A} + \frac{qn_{ref}}{C_{tot}} \right) \right] \frac{C_{pass}}{q}, \tag{4}$$

where $V_{BA,lf}$ is the barrier accumulation voltage for the lowest test signal frequency, which is 1 kHz in this investigation. The extraction of N_{slow} relies on the assumption that electrons start to transfer to the barrier as soon as the channel 2DEG has an electron sheet density that exceeds n_{ref}.

If τ_n of the trap is smaller than the period of the test signal (a fast trap) it will have time to capture and emit electrons during one period of the test signal. Even though the trap is fast compared to a given test signal, it can be slow compared to higher frequency test signals. Hence, traps of this kind can be responsible for dispersion between C(V) sweeps with different test signal frequencies. The trap will be designated N_{fdisp} (frequency dispersion) and the trap density is extracted using Eq. (5)

$$N_{\mathrm{fdisp}} = (V_{\mathrm{BA,hf}} - V_{\mathrm{BA,lf}})\frac{C_{\mathrm{pass}}}{q}, \tag{5}$$

where $V_{\mathrm{BA,hf}}$ is the barrier accumulation voltage for the highest test signal frequency, which is 100 kHz in this investigation. A trap with emission rate higher than the highest test signal frequency will not be detected during C(V) measurements.

Some traps are easily detected as hysteresis between forward and reverse sweep directions. Electrons that are captured during passivation accumulation will initially act like fixed negative charge by shifting the entire curve in the positive voltage direction, resulting in hysteresis in the region around V_{BA} (ΔV_{BA}). During the continued reverse sweep some of the captured electrons will emit, the result is a shift of $V_{2\mathrm{A}}$ ($\Delta V_{2\mathrm{A}}$) that is smaller than the shift of V_{BA}. N_{hyst2A} is the concentration of traps responsible for $\Delta V_{2\mathrm{A}}$ and N_{hystBA} are the remainder of traps responsible for ΔV_{BA}. Equations (6) and (7) are used to extract the densities of these traps

$$N_{\mathrm{hystBA}} = (\Delta V_{\mathrm{BA}} - \Delta V_{2\mathrm{A}})\frac{C_{\mathrm{pass}}}{q}, \tag{6}$$

$$N_{\mathrm{hyst2A}} = \Delta V_{2\mathrm{A}}\frac{C_{\mathrm{pass}}}{q}. \tag{7}$$

Table I presents a summary of approximate emission time constants for the traps. The time constants have also been converted to equivalent activation energies through Eq. (3). The calculation is performed using $N_C = 2.7\times10^{18}$ cm^{-3}, $v_{\mathrm{th}} = 2\times10^{7}$ cm/s (both calculated using data from Vurgaftman *et al.*[22]) and $\sigma_{\mathrm{n}} = 1\times10^{-16}$ cm^2.[8]

The error margins of the stated emission time constants should be considered to be at least one order of magnitude. The limits for N_{fdisp} traps are the inverses of the test signal frequencies. The lower limit of N_{slow} traps is the inverse of the lowest test signal frequency. The upper limit of N_{slow} traps is not well defined and overlaps the lower limit of N_{hystBA} traps. The lower limit of N_{hystBA} traps is related to the resolution of the sweep, each step in V_{GO} is 0.25 V and the sweep rate is approximately 0.1 V/s, i.e., there is approximately 2.5 s between each measurement point. The upper limit of N_{hystBA} traps is the sweep time of the gate bias, which is around 500 s. Traps with emission time constants longer than a week can, for all practical purposes be considered fixed charge, setting the upper limit of N_{hyst2A} traps to around 10^6 s.

TABLE I. Estimation of room temperature and trap electron emission time constants. The activation energies have been calculated using Eq. (3).

	τ_n (s)	E_a (eV)
N_{fix}	$10^6 < \tau_n < \infty$	$1.0 < E_a$
N_{hyst2A}	$10^3 < \tau_n < 10^6$	$0.8 < E_a < 1.0$
N_{hystBA}	$1 < \tau_n < 10^3$	$0.6 < E_a < 0.8$
N_{slow}	$10^{-3} < \tau_n < 1$	$0.4 < E_a < 0.6$
N_{fdisp}	$10^{-5} < \tau_n < 10^{-3}$	$0.3 < E_a < 0.4$

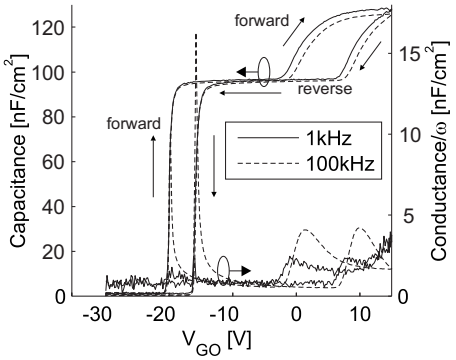

FIG. 3. 1 kHz and 100 kHz C(V)-sweeps for the LP sample. The reverse sweep is shifted to the right compared to the forward sweep.

IV. RESULTS AND DISCUSSION

A. Experimental C(V)

C(V) measurements of MISH-capacitors from the three samples are shown in Figs. 3–5.

Figure 3 presents the complete C(V) characteristic of the LP sample. There is some dispersion between sweeps with different test signal frequencies and there is a clear hysteresis between forward and reverse sweeps. Hence, the C(V) characteristics indicates presence of N_{slow} traps and that N_{hystBA} and N_{hyst2A} traps are being filled in the passivation accumulation interval. The V_{BA} of the forward sweep is below 0 V indicating some fixed positive charge at the passivation interface.

Figure 4 shows the C(V) characteristics for the RS sample. The lack of passivation accumulation at forward bias is interpreted as a shift of V_{BA} to a voltage higher than 10 V. The transient presented in the inset of Fig. 4 is the result of stepping the bias from $V_{\mathrm{GO}} = 10$ V to $V_{\mathrm{GO}} = -23$ V. The capacitance recovers from the depletion capacitance to its stable value in about 5 s. This indicates emission of electrons from traps with time constants less than a few seconds. Current will start to leak through the passivation at $V_{\mathrm{GO}} > 10$ V, preventing extraction of a definitive value of V_{BA}.

Figure 5 presents the C(V) characteristics for the PE sample. The large negative $V_{2\mathrm{A}}$, compared to a reference MISH-capacitor with the same C_{tot}, indicates a positive

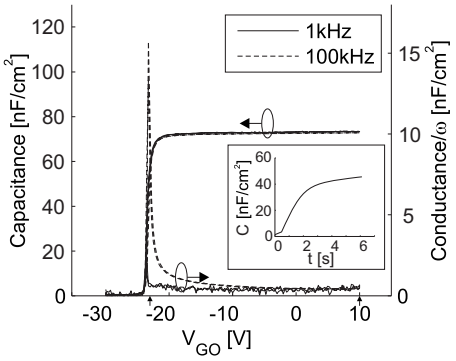

FIG. 4. 1 kHz and 100 kHz C(V)-sweeps for the RS sample. There is no hysteresis between forward and reverse sweeps. The graph in the inset shows the evolution of the capacitance after an instantaneous step from $V_{\mathrm{GO}} = 10$ V to $V_{\mathrm{GO}} = -23$ V (the relevant voltages are marked with arrows along the voltage axis).

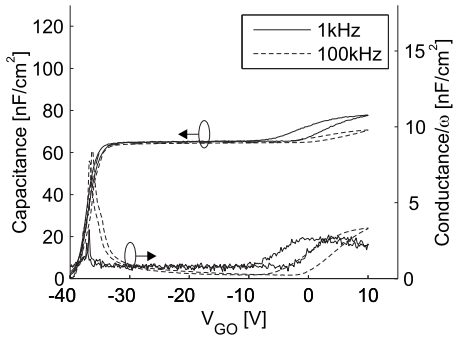

FIG. 5. 1 kHz and 100 kHz C(V)-sweeps for the PE sample. As for the LP sample the reverse sweep is shifted to the right compared to the forward sweep.

charge at the passivation interface. Hysteresis in both passivation accumulation and 2DEG accumulation intervals as well as frequency dispersion indicates a complete spectrum of interface traps for the PE sample.

B. Interface state extraction

From Figs. 3–5 it is seen that it is not possible to extract C_{pass} directly from the passivation accumulation capacitance. There are several reasons for this: traps, increased series resistance associated with electrons transferring from the channel region to the barrier, and electrons accumulating at other positions in the MISH structure. C_{pass} is necessary for extraction of all traps and the capacitance is, instead, calculated by rearranging Eq. (1). The calculated passivation capacitance ($C_{pass,c}$) is expressed as

$$C_{pass,c} = \frac{C_{barr}C_{tot}}{C_{barr} - C_{tot}}. \quad (8)$$

C_{barr}, the barrier layer capacitance, has been measured to approximately 320 nF/cm^2 using both mercury probe measurements and measurements of Schottky diodes. Forward and reverse Schottky diode C(V) characteristics, measured at 10 kHz, are presented in Fig. 6. There is no hysteresis between forward and reverse sweeps, and there is no frequency dispersion of the capacitance in the 1–100 kHz frequency range.

The parameters introduced in Secs. III B and III A are extracted from the experimental data and are presented in Table II. Equations (2) and (4)–(7) are then used to extract the interface state densities (Table III).

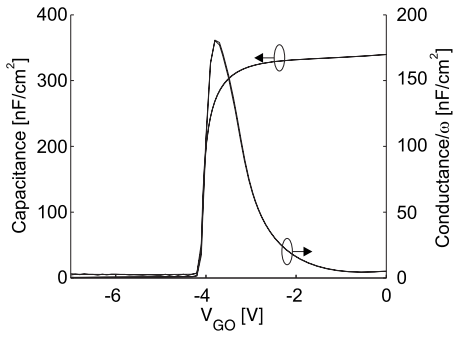

FIG. 6. 10 kHz C(V)-sweep for a Schottky diode.

TABLE II. Parameter extraction from the experimental C(V) data.

	LP	RS	PE
V_{2A} (V)	−20.0	−23.5	−37.2
$V_{BA,lf}$ (V)	−2.5	>10	−7.2
$V_{BA,hf}$ (V)	−1.4	x [a]	−5.0
C_{tot} (nF/cm^2)	96	73	66
$C_{pass,c}$ (nF/cm^2)	138	95	83
ΔV_{2A} (V)	4.1	0	0.5
ΔV_{BA} (V)	8.0	x [a]	5.8

[a]Not possible to extract from available data.

For the RS sample the high density of N_{slow} states results in Fermi-level pinning at the passivation interface, preventing any signs of barrier accumulation. Without a value for V_{BA} it is impossible to extract other trap types by the use of the methods described in this report. The choice of n_{ref} will influence the extracted N_{fix} and N_{slow} densities. In this case a lower n_{ref} would result in higher densities of N_{slow} traps and more positive fixed charges, for all samples. A higher n_{ref} would reversely result in lower N_{slow} and lower positive N_{fix}, the fixed charge density could even become negative.

It can be seen in Fig. 3 that the passivation interface is more strongly accumulated for the LP sample than for the RS and PE samples. Differences in how strongly the passivation interfaces have been accumulated results in that the interfaces can only be compared in certain intervals. For comparison with the RS sample only the N_{slow} value can be used. For comparison with the PE sample the values for N_{fdisp}, N_{slow}, and to some degree N_{hystBA} can be used. Hence, the higher total trap density for the LP sample is probably due to a more complete picture of the state distribution for this sample. The risk of electrons being captured by traps inside the silicon nitride[23] also increases with stronger accumulation.

A rough picture of the interface trap density, $D_{it} = N_{it}/\Delta E$, can be composed from the energy intervals presented in Table I and interface state densities (Table III).

The last row in Table IV presents the sum of all trap states divided by the investigated part of the band gap. These numbers can be used to compare the results in this report with other published results. The densities extracted in this report are substantially larger, one to two orders of magnitude, than some reported results for MIS[3,4] and MISH[8] structures with different passivations. The results are more in line with what is presented on Si_3N_4/GaN MIS capacitors by Swenson and Mishra[24] a report that also shows that different characterization methods can result in large differences in extracted D_{it}.

TABLE III. Summary of the passivation interface states. The values are given in units of ($\times 10^{12}$ cm^{-2}).

	LP	RS	PE
N_{fix}	3.4	1.3	7.1
N_{hyst2A}	3.5	x [a]	0.3
N_{hystBA}	3.4	x [a]	3.1
N_{slow}	1.4	7.2	3.1
N_{fdisp}	0.9	x [a]	1.3

[a]Not possible to extract using the presented method.

TABLE IV. D_{it} in units of ($\times 10^{12}$ cm^{-2} eV^{-1}) for different intervals of activation energy. The last row is the average D_{it} obtained by dividing the total amount of traps (i.e., excluding N_{fix}) with the investigated part of the energy band gap.

E_a (eV)	LP	RS	PE
0.3–0.4	9.0	x [a]	13.0
0.4–0.6	6.5	36.0	15.5
0.6–0.8	17.0	x [a]	16.0
0.8–1.0	18.0	x [a]	2.0
0.3–1.0	13.0	10.3	11.1

[a]Not possible to extract using the presented method.

V. DISCUSSION AND CONCLUSION

The surface passivation is an important step in the process of manufacturing GaN-based HFETs. In this paper a method to study the passivation interface using C(V) measurements has been described. The same method can be used to characterize interfaces between dielectrics and other types of heterostructures.

The analysis in this paper is simplified in the sense that traps are only allowed to be located at the passivation interface. The assumption of identical capture cross-section is also a simplification that will affect extracted D_{it} values (Table IV). At this stage the reported characterization method is most suited for comparing different passivations of the same heterostructure material.

From the discussion concerning the results in Table III it is concluded that where the nitrides are directly comparable, the LPCVD passivated sample has the lowest density of interface traps. When also considering the fixed charge the LPCVD sample is the sample that has the least amount of interface states.

Further experiments with manufacturing of HFET devices are required to investigate the effect of these traps on the operation of the HFET. It is not evident that the passivation showing the lowest amount of surface states is most suitable for transistor manufacturing. The gate contact of an HFET is a Schottky contact, with an electric field distribution that is different from that of the MISH capacitor. It is, however, intuitive to assume that a HFET having low interface state densities should offer more reliable and less dispersive operation, a property that is very favorable from application engineering perspective.

ACKNOWLEDGMENTS

This research has been carried out in the Microwave Wide Band gap Technology project financed by Swedish Governmental Agency of Innovation Systems (VINNOVA), Swedish Energy Agency (STEM), Chalmers University of Technology, Ericsson AB, Furuno Electric Co., Ltd., Infineon AG, Norse Semiconductor Laboratories AB, Norstel AB, NXP Semiconductors BV, and Saab AB. This work was also partially financed by Swedish Foundation for Strategic Research (SSF) in the research project "III-nitrides for UV and High-Frequency Applications."

[1]B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, IEEE Electron Device Lett. **21**, 268 (2000).
[2]E. Nicollian and J. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 2003).
[3]T. Hashizume, E. Alekseev, D. Pavlidis, K. S. Boutros, and J. Redwing, J. Appl. Phys. **88**, 1983 (2000).
[4]B. Gaffey, L. Guido, X. Wang, and T. Ma, IEEE Trans. Electron Devices **48**, 458 (2001).
[5]C. K. Wang, S. J. Chang, Y. K. Su, Y. Z. Chiou, T. K. Lin, C. C. Wong, H. L. Liu, S. P. Chang, and J. J. Tang, Phys. Status Solidi A **203**, 404 (2006).
[6]P. Chen, S. J. Chua, W. D. Wang, D. Z. Chi, Z. L. Miao, and Y. D. Zheng, J. Appl. Phys. **94**, 4702 (2003).
[7]C. Liu, E. F. Chor, and L. S. Tan, Appl. Phys. Lett. **88**, 173504 (2006).
[8]M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, J. Appl. Phys. **103**, 104510 (2008).
[9]J. Shealy, T. Prunty, E. Chumbes, and B. Ridley, J. Cryst. Growth **250**, 7 (2003).
[10]J. Y. Shiu, V. Desmaris, N. Rorsman, K. Kumakura, T. Makimoto, H. Zirath, and E. Y. Chang, Semicond. Sci. Technol. **22**, 717 (2007).
[11]W. Tan, P. Houston, G. Hill, R. Airey, and P. Parbook, J. Electron. Mater. **33**, 400 (2004).
[12]J. Zhang, U. Forsberg, M. Isacson, A. Ellison, A. Henry, O. Kordina, and E. Janzén, J. Cryst. Growth **241**, 431 (2002).
[13]O. Danielsson, C. Hallin, and E. Janzen, J. Cryst. Growth **252**, 289 (2003).
[14]A. Kakanakova-Georgieva, U. Forsberg, I. Ivanov, and E. Janzen, J. Cryst. Growth **300**, 100 (2007).
[15]U. Forsberg, A. Lundskog, A. Kakanakova-Georgieva, R. Ciechonski, and E. Janzen, J. Cryst. Growth **311**, 3007 (2009).
[16]R. S. Balmer, K. P. Hilton, K. J. Nash, M. J. Uren, D. J. Wallis, D. Lee, A. Wells, M. Missous, and T. Martin, Semicond. Sci. Technol. **19**, L65 (2004).
[17]Yokogawa-Hewlett-Packard, LTD, *Operation Manual, Model 4284A*, 1 edition, 1988.
[18]T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, J. Vac. Sci. Technol. B **21**, 1828 (2003).
[19]S. Arulkumaran, L. Z. Hong, N. G. Ing, S. L. Selvaraj, and T. Egawa, Appl. Phys. Express **2**, 031001 (2009).
[20]M. Fagerlind, H. Zirath, and N. Rorsman, Semicond. Sci. Technol. **24**, 045014 (2009).
[21]D. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, New York, 2005).
[22]I. Vurgaftman, J. Meyer, and L. Ram-Mohan, J. Appl. Phys. **89**, 5815 (2001).
[23]E. J. M. Kendall, Br. J. Appl. Phys., J. Phys. D **1**, 1409 (1968).
[24]B. L. Swenson and U. K. Mishra, J. Appl. Phys. **106**, 064902 (2009).