A Single-chip 64 Input Low Power High Speed Cross-Correlator for Space Application

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INTRODUCTION

Microwave sounding for weather and climate measurements has previously been done only from low earth orbit (LEO). One of the reasons for this is the large aperture required to perform such measurements from higher orbits. There are a number of advantages to achieve microwave sounding from geostationary earth orbit (GEO), such as spatial and temporal coverage. A satellite in GEO can continuously cover the area of interest, enabling a high temporal resolution.

Channels near 50 GHz are interesting for temperature sounding; assuming a desired resolution of 50 km at this frequency, the aperture needed from GEO would be over 6 m. Conventional parabolic antennas of this size are not easily deployed in space. An alternative to using conventional antennas is the use of synthetic aperture by interferometry. This method has been used for ground-based radio astronomical telescopes, such as the Very Large Array (VLA) [1], for a long time. A large aperture antenna is emulated by cross-correlating the signals from an array of smaller antennas.

The usage of interferometric aperture synthesis for earth observation was first proposed in the 1980s [2]. In November of 2009 the Soil Moisture and Ocean Salinity (SMOS) satellite was launched carrying a satellite-borne, 2-D, interferometric radiometer [3]. SMOS is the first polar orbiting satellite to carry such an instrument. Two microwave sounders using interferometric imaging, operating from GEO, are in development. The Geostationary Atmospheric Sounder (GAS) is an ESA project intended for nowcasting and short range forecasting [4]. It will carry a y-shaped rotating array of antennas. Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) is a weather and climate satellite being developed by NASA [5]. It will also carry a y-shaped array of antennas. For the 50 GHz band with a resolution of 50 km it will have approximately 300 receiving elements.

Previous and current ground-based cross-correlators, such as the ones used in VLA, are manufactured on multiple PCBs, each using multiple Application-Specific Integrated Circuits (ASICs). Since these cross-correlators are optimized for maximum computational performance, they are far from being portable and power-efficient enough for space application. Ever-shrinking process technologies, however, enable new ways to construct cross-correlators. The possibility has now emerged to fit a complete, large cross-correlator in a single-chip solution. This will enable powerful satellite-borne cross-correlators, where size and power dissipation are critical factors.

CROSS-CORRELATION

The cross-correlation of two signals describes the similarity between them. The continuous cross-correlation of two signals, f and g, is given by (1). The signals are multiplied and integrated, assuming a time delay τ is applied on one of the signals. The resulting cross-correlation is a function of this time delay.

$$(f * g)(\tau) = \int_{-\infty}^{\infty} f^*(t) g(t+\tau) dt \tag{1}$$

A schematic representation of digital cross-correlation is depicted in Fig. 1. A time-limited and discrete representation of the cross-correlation is performed. The signals are still multiplied and integrated; the integration time is limited by the memory depth of the integrator.

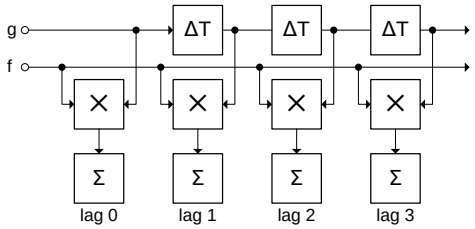

Fig. 1: Schematic of digital cross-correlation.

THE CROSS-CORRELATOR IMPLEMENTATION

A cross-correlator chip has been designed, implemented and manufactured as a first step towards future development of full-sized single-chip cross-correlators, built on previous cross-correlator experiences from Omnisys Instruments. The chip is manufactured in a 65-nm low-power process from ST Microelectronics. The nominal supply voltage is 1.0 V for both core and IO pins. All IOs are single-ended, and data and clock inputs can handle input swings at least down to 150 mV p-p at a 4-GHz clock frequency. A/D conversion is being handled externally, using 1-bit precision. The cross-correlator can be used either as a 32-input complex correlator, reaching bandwidths close to 4 GHz, or as a 64-input real valued correlator with half that bandwidth. Inputs are arranged in groups of eight, each group having its own clock input. All inputs should be synchronous. The cross-correlator operates in two modes, correlation and readout. The readout is performed through a scan chain using a serial readout interface.

The cross-correlator core is built up of an array of 2-input cross-correlators. This array is arranged in such a way that it allows for scaling to a larger number of inputs. The inputs are all routed to one side of the cross-correlator core using delay-matched paths; from there the data signals, each with its own clock, are routed sideways and forward to form a pattern illustrated in Fig. 2. Each row of cross-correlators is synchronous. The row-wise synchronization is maintained by synchronizing the clocks of the two incoming data signals in each 2-input cross-correlator.

The 2-input cross-correlators perform only zero-lag correlation, that is, no time delays between signals are applied.
The integrator depth is 30 bits, of which the 24 most significant bits are read out. At a clock frequency of 4 GHz, this means that integration times of at least 0.26 seconds can be achieved.

The layout of the chip, shown in Fig. 3, including pads, has a size of just above 3 mm^2. The compactness of the cross-correlator was one of the important issues for the layout phase. While 3 mm^2 in itself is not a big area, this chip is intended to demonstrate the possibility to implementing single-chip cross-correlators containing much more logic. A cross-correlator with 100 inputs and 1.5 bit precision, cross correlating with 32 lags, would for example have a core area 100 times larger than that of the current version, using a similar layout. With an increasing number of inputs that size ratio grows rapidly. This makes the area of the 64-input cross-correlator very important. Advanced technology nodes such as 65 nm or even 45 nm will be necessary, in order to stay with a single-chip solution for future correlators.

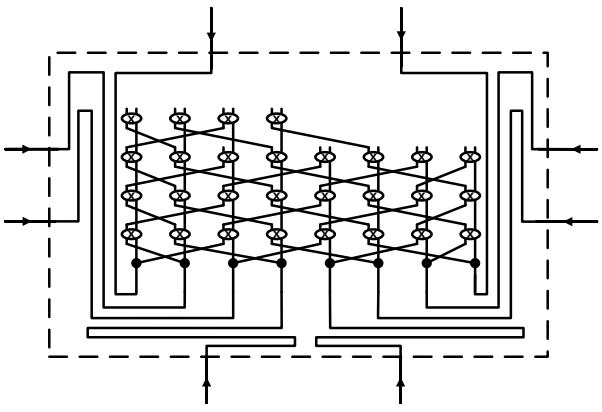

Fig. 2: 8-input example of the signal routing.

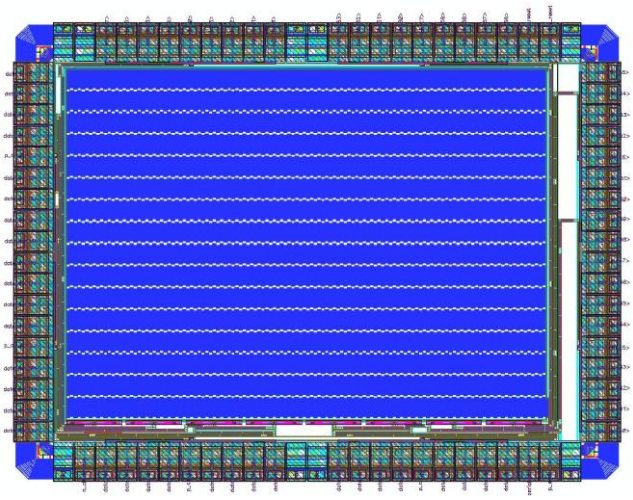

Fig. 3: The cross-correlator layout.

Another consideration when scaling to larger correlators is what number of IOs that can be handled on a single chip. This 64-input version uses single-ended signalling. Differential signalling on the other hand would offer advantages, such as common-mode rejection. For the previously mentioned example with 100 1.5-bit inputs, the number of pins using differential signalling would exceed 400. Using packaging techniques such as flip-chip BGA could very well accommodate more than 2,000 pins working at GHz frequencies [6].

PERFORMANCE

Operating at a clock frequency of 4 GHz, keeping signals synchronized is one of the major challenges. To verify that synchronization will be successfully handled, a simulation of the signal skew within the correlator was performed. The very regular structure of the design can be used to construct a simplified MATLAB simulation model, based on an RC-extraction of the layout. Timing of clock paths for 10,000 chips is randomly generated using this simplified model. For each of these chips, the worst skew between incoming clock signals to any 2-input cross correlator is saved. The result can be seen in Fig. 4. Most of the chips will have a worst clock skew below 0.3 clock periods at a clock frequency of 4 GHz. Simulations of the synchronisation logic has shown that it will be able to synchronize up to 0.32 clock periods of clock skew. This would give a yield of 99%. Since an ASIC of this type would only be manufactured in small numbers, the yield will be less important than the performance. Thus, minor discrepancies between simulation models and actual ASIC measurements will not be critical.

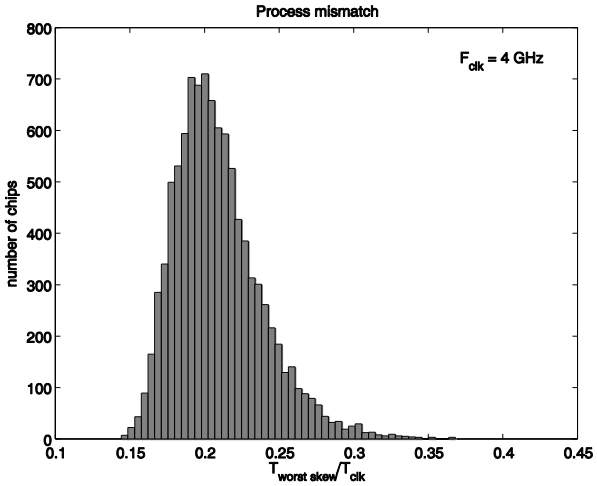

Fig. 4: Skew simulation results.

POWER

One of the main objectives in the development of this correlator was low-power dissipation; especially power per performance is an important figure of merit. Several low-power design techniques have been leveraged to achieve low power. To evaluate the power dissipation of the circuit, a simulation making use of the regularity of the correlator structure was carried out: Using random input signals, power was obtained for an RC-extracted netlist containing pads, routing and correlator core logic.

A comparison of the simulation result with a few other cross-correlators is displayed in Table 1. The FPGA-based correlator is a system developed by Omnisys Instruments. It has similar specifications to the ASIC-correlator, in terms of input precision and the number of lags and inputs. It has a power dissipation of around 5 W for the digital cross-correlator and a clock frequency of 330 MHz. The MIRAS CCU unit, the correlator on the SMOS satellite, has a stated power dissipation of 34 W working at 55.84 MHz with 72 1-bit IQ pairs being correlated [7]. A GeoSTAR cross-correlator is not yet in production, but it is estimated in [8] that a future cross-correlator will dissipate less than 20 W, performing 20 trillion multiplications per second.

Table 1. Comparison of cross-correlators.

Correlator	Performance (Mult/s)	Power (mW/ch/GHz)
ASIC	$8.1*10^{12}$	0.13
FPGA	$0.67*10^{12}$	7.5
SMOS	$0.57*10^{12}$	60
GeoSTAR	$20*10^{12}$	<1

CONCLUSION

Measurements on the ASIC remain to be done to verify the functionality, performance and efficiency of the chip. The simulations do however show some promising results. The power dissipation is greatly improved compared to current cross-correlators. The performance simulations indicate that the high, specified bandwidth is feasible. The entire design is fitted in a 3 mm^2 ASIC. All these aspects demonstrate the feasibility of producing larger single-chip cross-correlators meeting the requirements of future synthetic aperture radiometer satellite missions.

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