

THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

On Power Electronics Interface for Distributed  
Generation Applications and its Impact on System  
Reliability to Customers

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## Abstract

Distributed generation (DG) is being employed as a means of achieving increased reliability for electrical power systems as regarded by consumers. As the most of DG technologies utilize renewable sources, the power electronic interface plays a vital role to match the characteristics of a DG unit with the grid requirements.

In this thesis, a voltage source converter (VSC) is considered as a front end for a DG unit that utilizes a variable speed wind turbine. The control of the voltage/current is considered the most important part when implementing the interface. In order to obtain a high bandwidth, a vector current controller (VCC) is developed for the VSC connected to the grid through a filter inductor. The VSC system is simulated and examined in case of voltage dips. The VCC has proven to work adequately in case of balanced dips. However, most faults are unbalanced resulting in unbalanced voltage dips on the VSC terminals. Hence, the VCC had to be modified to give a better performance in case of grid voltage imbalance.

The dual vector current controller (DVCC) has been implemented to enhance the performance in case of unbalanced voltage dips. Two methods are proposed and compared to calculate the current references used by the controller. They depend on how the oscillating power, which is the power at double the fundamental frequency that is produced due to unbalanced faults, is compensated. The system is examined for all possible voltage dips. Design equations are derived to calculate the maximum current that the VSC switches should hold in case of different dips. Moreover, a case study is presented at which a design criterion, based on the knowledge of wind statistics at a specific site, is introduced to give the DG the capability to ride-through faults.

The controller is then modified to control a VSC connected to the grid through an inductor-capacitor-inductor (LCL-) filter, which has the advantage of eliminating the higher harmonics in the grid current. The VSC connected to a weak grid through an LCL-filter is also considered in the thesis. The voltage regulation limits are calculated and the controller is tested in case of the load connection/disconnection and balanced voltage dips.

**Keywords:** distributed generation, harmonics, L-filter, LCL-filter, power quality, strong grid, vector control, voltage dips, voltage regulation, VSC, weak grid.



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## List of Publications

- [1] F. A. Magueed, A. Sannino, and J. Svensson, "Transient Performance of Voltage Source Converter under Unbalanced Voltage Dips," in *Proc. of Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, 20-25<sup>th</sup> June 2004, pp.1163-1168.
- [2] F. A. Magueed, A. Sannino, and J. Svensson, "Design of Robust Converter Interface for Wind Power Applications," accepted to be published on *Wind Energy Journal*, special issue on Electrical Integration of Wind Power.
- [3] F. A. Magueed, J. Svensson, and A. Sannino, "Transient Performance of Voltage Source Converter Connected to Grid through LCL-Filter under Unbalanced Voltage conditions," accepted to be presented in *Proc of Power Tech Conference (PT'05)*, St. Petersburg, Russia, 27-30<sup>th</sup> June 2005.
- [4] F. A. Magueed, and J. Svensson, "Control of VSC Connected to the Grid through LCL-Filter to Achieve Balanced Currents," accepted to be presented in *the IEEE Industry Applications Society 40<sup>th</sup> Annual Meeting (IAS'05)*, Kowloon, Hong Kong, 2-6<sup>th</sup> October 2005.





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# 1. Introduction

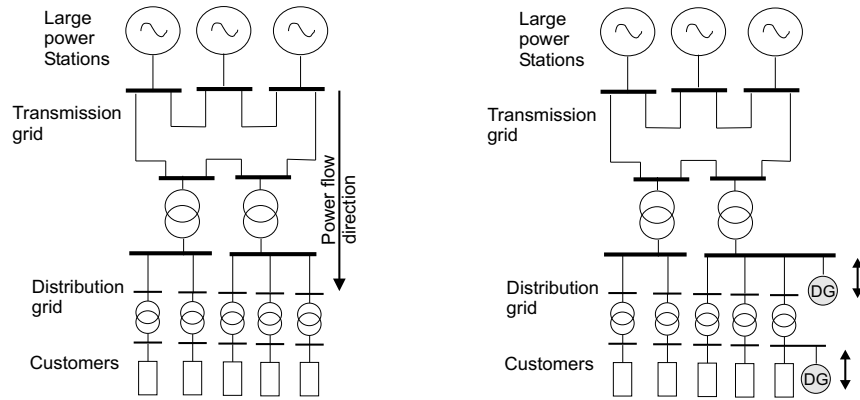
## 1.1 Background

One of the fundamental laws of physics states that the energy in a closed system is conserved but may transform from one form to another. The global increase in fossil energy consumption leading to environmental problems, such as greenhouse gas emission, is a direct proof for this law. Since the production of electrical energy consumes a large part of the total worldwide fossil energy reserve, the traditional power systems should change to meet environmental and social concerns.

Traditional power systems implement large power generation plants located geographically and produce most of the power that is then transmitted toward large consumption centres and then distributed between different customers. This construction has started to change towards new scenarios at which distributed generation (DG) units are spread over distribution networks, as shown in Fig. 1.1 for two possible locations. These DGs utilize renewable resources such as wind turbines, photovoltaics, fuel cells, biomass, small hydro-plants, ... etc. Beside their environmental benefits, DGs offer a cheap way into market since they do not suffer huge transmission losses and the surplus heat may be used in useful purposes such as water heating [1]. Moreover they present reliable and uninterruptible source for the customers [2].

The main disadvantage of implementing renewable sources, beside the high capital cost, is the daily and seasonal pattern of the energy. However due to the advances in power electronics, which plays a vital role to match the characteristics of the DG units and the requirements of the grid connection, a large number of DG is being developed in the distribution level [3]. Moreover, a common case where DG is effective and economical occurs when it helps to supply load during contingencies until the utility can build additional delivery capacity [2]. These DGs, besides helping the grid through increasing the feeders' capacity, can enhance the reliability from the consumer point of view (as it will be investigated through the thesis). Reliability here means either the number or duration of service interruptions to consumers.

The massive expansion of DGs is, to a large extent, due to political decisions in many countries. For instance, the Swedish government has introduced new legislation with effect from 1<sup>st</sup> May 2003 (2003:113), which intended to encourage and increase the proportion of electricity produced from renewable resources [4]. This law has confirmed previous guidelines given by the Swedish Parliament in 1991 and 1997, which aims to phase out at a slow rate the nuclear power production so that the need for electrical energy can be met without risking employment and welfare. Accordingly, the first nuclear reactor of Barsebäck was shut down on 30<sup>th</sup> of November 1999 [5].



**Fig. 1.1 Traditional power system (left) and penetration of distributed generator (right). The arrows present the power flow direction.**

Even though large-scale implementation of DG has several driving forces as mentioned above, there are major challenges concerning network interconnection issues that have to be solved [6], [7]. Grid connection of DGs is considered from two main prospective: utility prospective and customer prospective, in addition to commercial power producer prospective that is mainly affected by political laws.

The impact of DGs on power system is studied in a parallel research carried out by a colleague. The main interests may include:

- Voltage profile along feeders due to the penetration of DGs;
- Optimum allocation of DG units, which permits the best location of generators to be found so that the power losses in the distribution network are minimized [8];
- Load forecast, since using DGs masks the true load growth that may eventually lead to problems in case of DGs disconnected for some reasons [2];
- The effect on power quality;
- Fault contribution of DG sources;
- Protection coordination on feeders with DG sources;
- The impact on power system dynamics;
- Impact of increased DGs in weak networks.

The impact of power system on DG and customers is investigated through the thesis from the point of view of power electronics. The main interests may include:

- Improving reliability during power disturbances;
- Voltage and/or frequency regulation in weak networks;
- Efficient use of the energy sources;
- Improving power quality to customers;
- Problems due to the interaction between the power electronics interface of different DGs and the grid (e.g. increased harmonic, network resonance, ... etc.) [9]-[10];
- Proper design of power electronics controllers to minimize system transients and prevent resonance.

## 1.2 Power electronics interface for DGs with wind power source

Since the fastest growing renewable energy source is the wind power [11]-[12], the main focus here will be on DGs utilizing wind energy sources. Basically, the electrical systems of these DGs are divided into three categories [3]:

- Systems without power electronics, at which a fixed speed wind turbines are connected to the grid through induction generators;
- Systems with partially rated power electronics interface;
- Systems with full-scale power electronics interface.

Variable speed wind turbines are utilized in systems with power electronics interface. Normally, these turbines are controlled in such a way to capture the maximum power by varying the rotor speed. They have the advantages of reducing stresses of the mechanical structure and acoustic noise reduction [5].

Wind turbines with partially rated power electronics interface have the advantages of reduced switching losses over full rated ones. However, in full-scale power electronics interface the main advantages are that the generator is decoupled from the grid through the DC-link and the power converter at the grid side enables a fast control over active and reactive powers [3].

A typical variable speed wind turbine system with full-scale power converters is shown in Fig. 1.2, at which the wind turbine is connected through a gear-box to an induction generator (G). The benefit of using the induction generator instead of synchronous generator is to reduce the system size since the latter needs a small power converter for field excitation. The output of the generator is then rectified and the resulting power is transferred through a DC link to a voltage source converter. Voltage source converters (VSCs) implementing isolated gate bipolar transistor (IGBT) switches that are controlled by pulse width modulation (PWM) are used on the grid side for their high controllability and power quality [20]. However, the drawback of using VSCs is their sensitivity to voltage disturbances, e.g. voltage dips [20]. Typically, filter inductors (L-filters) are used to minimize the current harmonics injected into the grid. However the use of inductor-capacitor-inductor filters (LCL-filters) produces almost pure sinusoidal currents at the expense of more complicated control system, as it will be shown through the thesis.

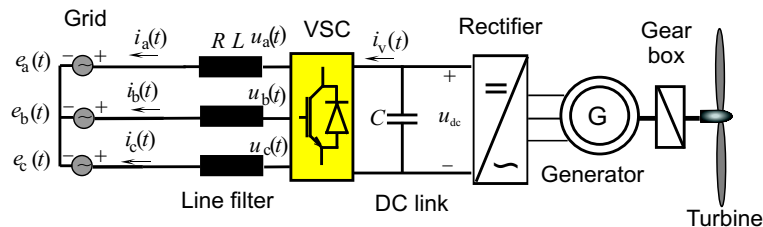


Fig. 1.2 Variable speed wind turbine system with full-scale power converters.

### 1.3 Power quality and system reliability

Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage, since sensitive equipment and non-linear loads are now more common in both the industrial/commercial sectors and domestic environment [15]. Distributed generation can mitigate the majority of these problems by locally providing power to critical loads [7]. Definitions of the most common power quality problems, as given in [15] and [16], are:

- A *voltage dip* is a reduction in the RMS voltage in the range from 0.1 to 0.9 p.u. of the nominal voltage for duration greater than half cycle and less than one minute;
- A *voltage swell* is an increase in the RMS voltage in the range of 1.1 to 1.8 p.u. of the nominal voltage;
- *Harmonics* are periodic sinusoidal distortions of either the supply voltage or load current;
- *Flicker* is a term used to describe the visual effect of small voltage variations on electrical lighting equipment. Note that the maximum human sensibility occurs between 0.5 and 30 Hz;
- *Voltage imbalance* is the deviation in phase and/or magnitude in one or more of the phases of three-phase supply from the ideal waveform;
- A *Transient* is an undesirable momentary deviation of the supply voltage or load current.

For a VSC (the front end of a DG unit), a sudden decrease in the grid voltage normally causes an increase in the grid side current, as the control attempts at maintaining the power to the DC link constant. This can lead to tripping of the converter because of overcurrent, in order to protect the VSC switches. Moreover, most faults are unbalanced and result in unbalanced dips, which produce undesirable power oscillations of low-order frequencies resulting in current harmonics and poor DC-link voltage regulation [20]. Ultimately, this can also lead to tripping of the converter due to DC overvoltage. When a large amount of DGs are installed in the grid, it becomes unacceptable to disconnect generation units every time a disturbance occurs. Moreover, since the main interest, in this thesis, is to enhance the reliability of the electric power system as regarded by customers, the focus here will be on voltage dips and load current harmonics.

### 1.4 Voltage dips

A voltage dip is the voltage experienced at the end user terminals mainly due to a short circuit fault at a certain point in the electrical network. It can also happen due to motor starting or overloads. In spite of short duration, between one cycle and several seconds, voltage dips can have a destructive effect on sensitive equipment, especially electronic devices [2], [14]. The equipment may also fail due to one or more of the following reasons [16]:

- There is not enough voltage on the AC power system to provide the energy that the equipment needs. However this problem is very subtle for very short duration voltage dips;



- Protection tripping (undervoltage, overcurrent or imbalance);
- Quick acting relay typically exists in emergency off (EMO) circuits, which operates very quickly and then it may operate due to a short duration voltage dip and unnecessary shut the whole system;
- Incorrectly trip of a reset circuit at the end of the dip. Reset circuits may exist in some electronic equipment for resetting the output at the start.

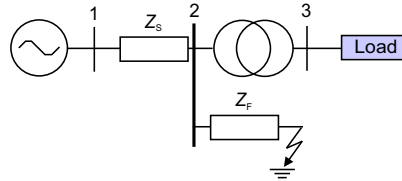
To deeply study the effect of voltage dips on DGs, the dip classification found in [17] has been adopted and used throughout this work.

### 1.4.1 Voltage dips classification

Starting from the different types of faults that can occur in a power system, a classification of voltage dips has been accomplished in [17]. It depends on how the load is connected and how the windings of the supplying transformer are connected. According to this classification, there are seven types of dips designated with the letters “A” to “G”. The system in Fig. 1.3 has been used to quantify the magnitude of a voltage dip in a radial system. In this system, the fault occurs at a remote distance from bus 2 and the load, which could be the DG (as in the thesis), is connected at bus 3. Two impedances are connected to bus 2: the impedance of the system, denoted by  $Z_S$ , which represents Thevinin’s equivalent impedance of the power system, and the fault impedance  $Z_F$ . The load is connected through a transformer to bus 2, at which the voltage, in p.u., is given by:

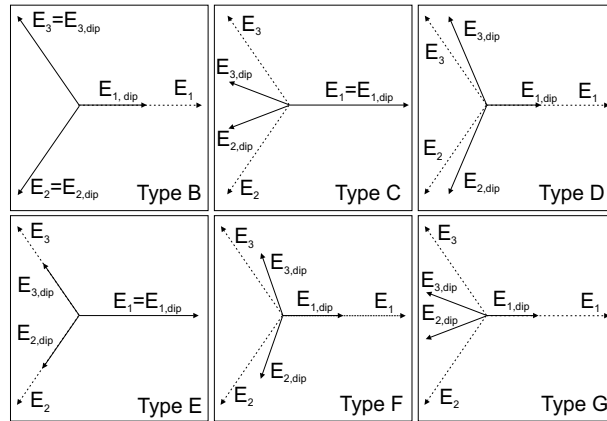
$$V_{\text{dip}} = \frac{Z_F}{Z_F + Z_S} \quad (1-1)$$

assuming that the pre-fault voltage is taken as reference and equal to 1 p.u. This typically means that voltage dips originated in the transmission system are shallow (since  $Z_s$  is small), while voltage dips originated at distribution level can be deep.



**Fig. 1.3 General single-line model for dips classification.**

If first it is assumed that the  $X/R$  ratio of the impedances  $Z_S$  and  $Z_F$  is the same, then  $V_{\text{dip}}$  (or  $E_{\text{dip}}$ ) has zero phase angle. The resulting voltage dip at bus 3 can be of type “A”, which represents a three-phase balanced fault, or any of the six unbalanced types denoted with letters “B” through “G” and reported in Fig. 1.4.



**Fig. 1.4 Voltage dip classification from “B” to “G”. Phasors of three phase voltage before (dotted) and during fault (solid) are displayed.**

The transformer that supplies the load can be one of the following types:

*Type 1:* transformers that do not change anything to voltages (e.g. star grounded/star grounded).

*Type 2:* transformers that blocks the zero-sequence voltage (e.g. Y/Y with at least one not grounded or D/Z).

*Type 3:* transformers that swap line and phase voltages (e.g. D/Y, Y/D, Y/Z).

According to the transformer type, the dip may change from one type to another (seen at bus 3), as listed in Table 1-1. Since the transformer between the load and bus 2 is mainly D/Y (type 3), the following five types at the equipment terminals are normally found:

- Type A, due to three-phase fault;
- Type C and type D, due to single phase and double phase faults;
- Type F and G, due to double phase to ground faults.

Note, however, that the load can in principle be subjected to dips of type “B” and “E” if the fault occurs at the same voltage level as the load or at the transformer bus with transformer *type 1*. Hence, all voltage dip types will be considered in the proceeding chapters.

**Table 1-1 Voltage dips classification as seen at bus 3 in Fig. 1.3.**

|            |  | Dip on the primary side |              |                |                         |                  |                           |   |
|------------|--|-------------------------|--------------|----------------|-------------------------|------------------|---------------------------|---|
| Dip type   |  | A                       | B            | C              | D                       | E                | F                         | G |
| Fault type |  | Three-phase             | Single phase | Phase-to-phase | Phase-to-phase (Δ load) | 2Phase-to-ground | 2Phase-to-ground (Δ load) |   |
| TR type    |  |                         |              |                |                         |                  |                           |   |
| Type 1     |  | A                       | B            | C              | D                       | E                | F                         | G |
| Type 2     |  | A                       | D*           | C              | D                       | G                | F                         | G |
| Type 3     |  | A                       | C*           | D              | C                       | F                | G                         | F |

The superscript \* in Table 1-1 indicates that the dip magnitude is not equal to  $V_{\text{dip}}$  but equal to  $\frac{1}{3} + \frac{2}{3}V_{\text{dip}}$ .

### 1.4.2 Dips associated with phase angle jump

If the X/R ratio for  $Z_S$  and  $Z_F$  is different, the voltage dip seen at the terminals of the load will have a phase angle “ $\psi$ ” called “phase angle jump”. The impedance angle  $\alpha$  is defined as:

$$\alpha = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_S}{R_S}\right) \quad (1-2)$$

where  $Z_S = R_S + jX_S$ ,  $Z_F = R_F + jX_F = zl$ ,  $z$  is the feeder impedance per unit length and  $l$  is the feeder length. The expression of the dip voltage at bus 2 will be:

$$v_{\text{dip}} = \frac{\lambda e^{j\alpha}}{1 + \lambda e^{j\alpha}} = V_{\text{dip}} \angle \psi \quad (1-3)$$

where  $\lambda e^{j\alpha} = zl / Z_S$ .

The four values for the impedance angle  $\alpha$  that are suggested in [17] are considered in the thesis:  $10^\circ$  as the highest expected value for transmission system faults,  $0^\circ$  as the reference value,  $-20^\circ$  for overhead distribution lines, and  $-60^\circ$  for underground distribution cables. In Fig. 1.5, the relation between the phase angle jump and different dip magnitudes at the four impedance angles is shown. The phase angle jump is bigger for smaller dip magnitudes and is more significant when  $\alpha = -60^\circ$ . Note that the dip magnitude refers to the remaining voltage during the dip.

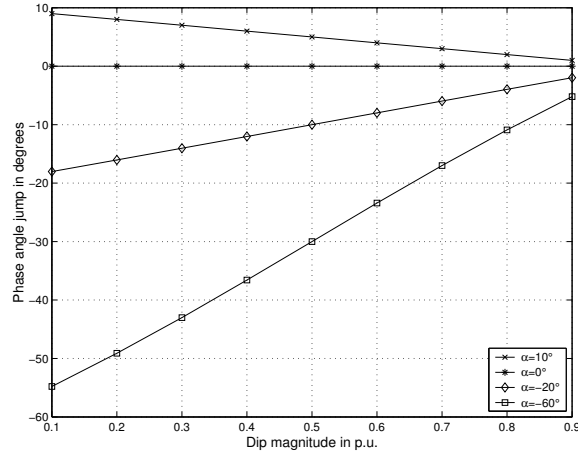


Fig. 1.5 Phase angle jump for different dip magnitudes and impedance angles.

### 1.4.3 Positive/negative sequence sub-classification

The magnitudes of positive sequence ( $E_p$ ) and negative sequence ( $E_n$ ) of the grid voltage for dip types “A” through “G” are calculated using Park transformation and summarized in Table 1-2, where  $E$  is the phase-to-phase RMS grid voltage. It shows that dips “C” and “D” have the same positive and negative sequence magnitudes. The same applies for dips “E”, “F”, and “G”. However they may affect the system in different ways according to Table 1-3, at which the positive and negative sequence components in the  $dq$ -coordinate system (see Appendix A) are calculated. It shows that dips “C” and “D” result in different negative sequence  $dq$ -components. Same goes for dip types “F” and “G”, while dips “E” and “G” are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of different dips on the system.

**Table 1-2 Positive and negative sequence magnitudes of grid voltage for dip type “A” through “G”.**

| Dip type | $E_p$   | $E_n$  |
|----------|---|--|
| A        | $EV_{\text{dip}}$   | 0  |
| B        | $\frac{E}{3}\sqrt{4+4V_{\text{dip}}\cos\psi+V_{\text{dip}}^2}$  | $\frac{E}{3}\sqrt{1-2V_{\text{dip}}\cos\psi+V_{\text{dip}}^2}$ |
| C, D     | $\frac{E}{2}\sqrt{1+2V_{\text{dip}}\cos\psi+V_{\text{dip}}^2}$  | $\frac{E}{2}\sqrt{1-2V_{\text{dip}}\cos\psi+V_{\text{dip}}^2}$ |
| E, F, G  | $\frac{E}{3}\sqrt{1+4V_{\text{dip}}\cos\psi+4V_{\text{dip}}^2}$ | $\frac{E}{3}\sqrt{1-2V_{\text{dip}}\cos\psi+V_{\text{dip}}^2}$ |

**Table 1-3 Positive and negative sequence components of the grid voltage in  $dq$ -coordinates for dip type “A” through “G”.**

| Dip type | $e_{dp}$                                 | $e_{qp}$                             | $e_{dn}$                                 | $e_{qn}$                             |
|----------|--|--------------------------------------|--|--------------------------------------|
| A        | $EV_{\text{dip}}\cos\psi$                | $EV_{\text{dip}}\sin\psi$            | 0  | 0                                    |
| B        | $\frac{E}{3}(2+V_{\text{dip}}\cos\psi)$  | $\frac{E}{3}V_{\text{dip}}\sin\psi$  | $-\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$ | $-\frac{E}{3}V_{\text{dip}}\sin\psi$ |
| C        | $\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$  | $\frac{E}{2}V_{\text{dip}}\sin\psi$  | $\frac{E}{2}(1-V_{\text{dip}}\cos\psi)$  | $\frac{E}{2}V_{\text{dip}}\sin\psi$  |
| D        | $\frac{E}{2}(1+V_{\text{dip}}\cos\psi)$  | $\frac{E}{2}V_{\text{dip}}\sin\psi$  | $-\frac{E}{2}(1-V_{\text{dip}}\cos\psi)$ | $-\frac{E}{2}V_{\text{dip}}\sin\psi$ |
| E        | $\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$ | $\frac{2E}{3}V_{\text{dip}}\sin\psi$ | $\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$  | $\frac{E}{3}V_{\text{dip}}\sin\psi$  |
| F        | $\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$ | $\frac{2E}{3}V_{\text{dip}}\sin\psi$ | $-\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$ | $-\frac{E}{3}V_{\text{dip}}\sin\psi$ |
| G        | $\frac{E}{3}(1+2V_{\text{dip}}\cos\psi)$ | $\frac{2E}{3}V_{\text{dip}}\sin\psi$ | $\frac{E}{3}(1-V_{\text{dip}}\cos\psi)$  | $\frac{E}{3}V_{\text{dip}}\sin\psi$  |

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## 1.5 Thesis Outlines

The thesis is organized as follows:

- The background and motivation of the thesis has been given in *Chapter one*.
- In *Chapter two*, the main system shown in Fig. 1.2 is presented. A simple vector current controller (VCC) for the voltage source converter (VSC) is derived, modelled and tested. Some modifications are suggested to improve the controller. Then the system is examined in case of voltage dips. To give a better performance in case of grid voltage imbalance the dual vector current controller (DVCC) is introduced. Two methods are proposed to calculate the current references used by the controller. At the end of the chapter, design equations for the maximum current that the VSC should hold for different dips are derived. Moreover, a case study has been introduced to show how, with the proper design of the VSC switches and the knowledge of wind statistics, the DG system can ride through voltage dips.
- In *Chapter three*, the focus is mainly on minimization of current harmonics. The LCL-filter is introduced, modelled, and designed for the interface between the VSC and the grid. The controller is modified to meet the new system configuration. The derivation, transient analysis, and performance in case of voltage dips are addressed. The DVCC is implemented to improve the performance in case of grid voltage imbalance. The current references are calculated in such a way to keep the DC-link voltage constant. The DVCC is examined for all voltage dip types and magnitudes. The effect of a change in the LCL-filter parameters is evaluated at the end of the chapter.
- In *Chapter four*, the integration of DG in weak grids is considered. The voltage regulation limit of a DG unit is addressed. Moreover, the performance in case of load disconnection/connection and voltage dips is examined.
- *Chapter five* gives the conclusions of the thesis and suggests possible future work.



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## 2. Grid-Connected Voltage Source Converter with L-filter Interface

### 2.1 Introduction

Voltage source converters (VSCs) are generally preferred over current source converters in grid-connected converter applications. This is mainly justified by the introduction of power-electronics devices (such as IGBTs in distribution level) with self turn-off capabilities, and also the advantages of capacitive DC storage over an inductive one in terms of weight, cost and efficiency [22]. VSC's are, for example, employed in shunt or series compensators. Shunt-connected VSC's are also utilized in the medium voltage (or distribution grid) as interface to distributed generation (DG) or in electric drives applications. In these applications, the DC-link voltage needs to be regulated to the nominal value.

In order to keep the DC-link voltage constant and minimize the grid current amplitude and harmonics during faults, the VSC controller is required to have two main functions: DC-link voltage regulation and current control. Most conventional current controllers have been designed under the assumption of balanced grid voltages. These controllers show undesirable current control characteristics under unbalanced conditions because the current references are distorted by a second-order harmonic due to the negative-sequence voltage [19]. This is due to the negative-sequence voltage in the three-phase domain, which translates into a second-order harmonic in a  $dq$ -frame synchronized with the positive-sequence voltage.

A comparison between different types of current controllers (CCs) for shunt-connected VSC based on their transient operation in case of voltage dips is presented in [20]. It has proved that the dual vector current controller (DVCC) shows the best performance regarding grid current control and DC-link voltage regulation. This controller uses two different vector current controllers for the two sequence components, together with a DC-link voltage controller based on the instantaneous active and reactive power theory.

In this chapter, the variable-speed wind turbine system shown in Fig. 1.2 is considered. A simple vector current controller for the VSC is derived and its transient performance is evaluated. Some modifications are suggested to introduce satisfactory operation of the controller. Then the controller is examined in case of voltage dips. To give a better performance in case of the grid voltage imbalance, the DVCC is implemented. Two methods are proposed and compared in order to calculate the current references used by the controller. The system is examined for all possible voltage dips using dips classification described in *Section 1.4.1*. Design equations are derived to calculate the maximum current that the VSC switches should conduct in case of different dips. At the end of the chapter, a case study is

presented at which a design criterion, based on the knowledge of wind statistics at a specific site, is introduced to give the DG the capability to ride-through faults.

## **2.2 Current-controlled shunt-connected voltage source converter (VSC)**

Current controllers are highly demanded for shunt connected VSCs in order to increase stability of the closed loop controller and to decrease the time response in case of load transients. A number of current control techniques have been developed in literature. As far as the control is concerned, three main categories can be considered: linear controllers, hysteresis controllers and predictive controllers [23]. However, there are some more innovative current controllers that have been adopted, such as neural network controllers and fuzzy logic controllers [24]-[27].

A modification of linear controllers, which applies to all cases where sinusoidal current and voltage are required [23], is the implementation of PI-controllers in the rotating  $dq$ -frame. If the  $dq$ -frame is synchronized with the grid voltage, voltage and current signals become constant vectors or DC-quantities. Hence, a fast response time can be achieved. However, in case of grid voltage transients or harmonics, the response is limited [23]. Moreover, a long transient time may occur in case of simultaneous variations in system parameters, load and grid voltage. Such controllers are also called vector controllers [28].

The vector current controller (VCC) is applied throughout this work, since a strong grid is considered, where the grid voltage is assumed to be pure sinusoidal. In Fig. 2.1, a scheme of the VSC system connected to the grid via a filter inductance (L-filter) along with the VCC is shown. Since the application of distributed generation utilizing renewable sources is considered, the variation of the input DC current  $i_{dc}$  is relatively slow compared to the response time of the controller. Hence,  $i_{dc}$  is modelled as a constant current source. However, the DC-link voltage should be regulated to maintain a constant voltage in case of grid voltage variations (e.g. voltage dips). The three-phase AC currents and voltages are sampled and transformed into their corresponding  $dq$ -components using the transformation angle  $\theta(k)$ . This angle is obtained from the grid voltage using a phase-locked-loop (PLL), which is assumed to be very slow so it does not react during faults or disturbances. The  $dq$ -components of measured currents and voltages are then used along with the reference current signals by the VCC to produce the reference voltage signal. The reference currents are produced in such a way to decrease the DC-link voltage ripple using a “reference currents generation algorithm” that uses the signal coming from the DC-link voltage regulator. The reference voltage vector in the  $dq$ -frame is transformed to three phase quantities using a transformation angle of  $\theta(k)+\Delta\theta(k)$ , where  $\Delta\theta(k)$  compensates for the transformation angle error due to one sample calculation time delay of the controller. The three phase control signals are then used in the PWM modulator to produce the switching pattern for the VSC. The PWM is optimized to increase the maximum output voltage of the converter without



increasing the DC-link voltage [29]. The block “OPT” injects a zero sequence voltage into the control signals. Due to the absence of a neutral wire, the added zero sequence waveforms are cancelled out.

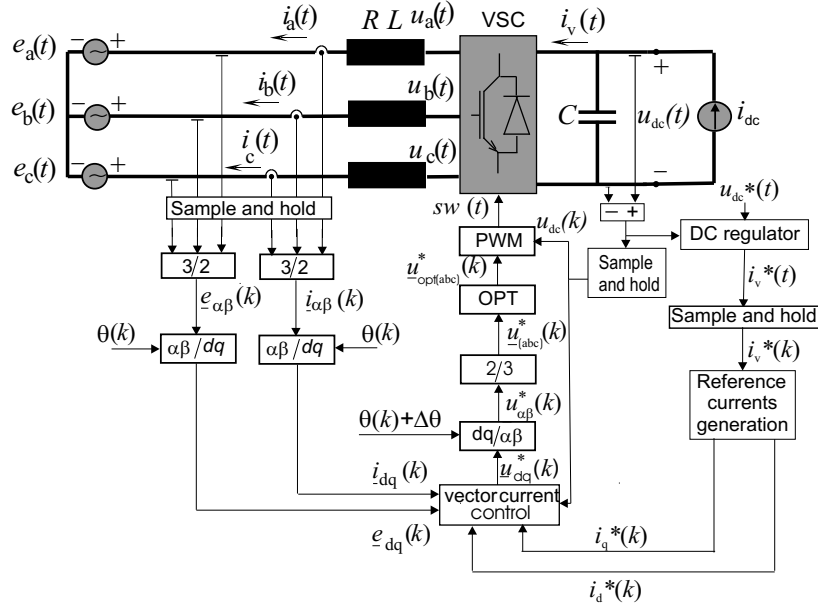


Fig. 2.1 Schematic diagram showing VSC, grid, filter and controller.

### 2.3 Derivation of vector current controller (VCC)

The VCC is derived using a set of balanced grid phase voltages  $e_a(t)$ ,  $e_b(t)$  and  $e_c(t)$ , which is defined by the following equations:

$$e_a(t) = \sqrt{\frac{2}{3}} \cdot E \cdot \cos(\omega t) \quad (2-1)$$

$$e_b(t) = \sqrt{\frac{2}{3}} \cdot E \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) \quad (2-2)$$

$$e_c(t) = \sqrt{\frac{2}{3}} \cdot E \cdot \cos\left(\omega t - \frac{4\pi}{3}\right) \quad (2-3)$$

where  $E$  is the phase-to-phase RMS grid voltage, and  $\omega$  is its angular frequency. Applying the KVL to the VSC circuit shown in Fig. 2.1 gives:

$$u_a(t) - e_a(t) - R \cdot i_a(t) - L \frac{d}{dt} i_a(t) = 0 \quad (2-4)$$

$$u_b(t) - e_b(t) - R \cdot i_b(t) - L \frac{d}{dt} i_b(t) = 0 \quad (2-5)$$

$$u_c(t) - e_c(t) - R \cdot i_c(t) - L \frac{d}{dt} i_c(t) = 0 \quad (2-6)$$

where  $R$  and  $L$  are the filter resistance and inductance respectively,  $u_a(t)$ ,  $u_b(t)$ , and  $u_c(t)$  are the converter terminal phase voltages, and  $i_a(t)$ ,  $i_b(t)$ , and  $i_c(t)$  are the AC phase currents. In the stationary reference frame  $\alpha\beta$ , the equations will become:

$$\underline{u}_{\alpha\beta}(t) - \underline{e}_{\alpha\beta}(t) - R \underline{i}_{\alpha\beta}(t) - L \frac{d}{dt} \underline{i}_{\alpha\beta}(t) = 0 \quad (2-7)$$

The vectors in (2-7) are transformed into the synchronous  $dq$ -frame, which is synchronized with the grid voltage, resulting in:

$$\underline{u}_{dq}(t) - \underline{e}_{dq}(t) - R \underline{i}_{dq}(t) - L \frac{d}{dt} \underline{i}_{dq}(t) - j\omega L \underline{i}_{dq}(t) = 0 \quad (2-8)$$

The term that includes the angular frequency  $\omega$  in (2-8) is referred to as the cross-coupling term, which means a change in the direct current will result in a change in the quadrature current.

The VCC is implemented in discrete time. Thus the currents and voltages are sampled with a sampling time  $T_s$ . The discrete time equations in  $dq$ -coordinates are derived from (2-8) using Forward Euler method, by integrating from  $kT_s$  to  $(k+1)T_s$ , where  $k$  represents a sampling instant and  $(k+1)$  is the next sampling instant, and dividing by  $T_s$ . The resulting equation of the discrete time model, assuming that the average of voltage and current vectors is equal to the corresponding value at the sampling instant  $k$ , will be as follows:

$$\underline{u}_{dq}(k) = \underline{e}_{dq}(k) + R \underline{i}_{dq}(k) + j\omega L \underline{i}_{dq}(k) + \frac{L}{T_s} (\underline{i}_{dq}(k+1) - \underline{i}_{dq}(k)) \quad (2-9)$$

If a proportional (P) controller with dead-beat gain is assumed, the actual current should follow its reference value within one sample as explained by Fig. 2.2.

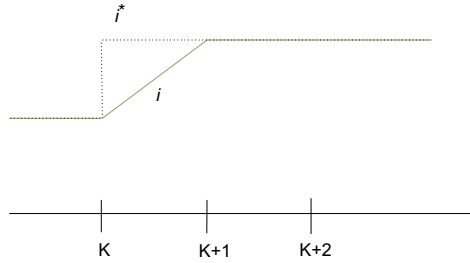


Fig. 2.2 Deadbeat concept.

Thus the  $dq$ -components of the current will be as follows:

$$\underline{i}_{dq}(k+1) = \underline{i}_{dq}^*(k) \quad (2-10)$$

where the asterisk denotes the reference value of the corresponding symbol. Assuming that the VSC voltage vector that is required to give the desired response is equal to the reference vector over one sample, leads to:

$$\underline{u}_{dq}(k) = \underline{u}_{dq}^*(k) \quad (2-11)$$

Substituting (2-10), and (2-11), into (2-9), yields the P-controller equation as follows:

$$\underline{u}_{dq}^*(k) = \underline{e}_{dq}(k) + R\underline{i}_{dq}(k) + j\omega L\underline{i}_{dq}(k) + k_p(\underline{i}_{dq}^*(k) - \underline{i}_{dq}(k)) \quad (2-12)$$

where  $k_p$  is the proportional gain, also called dead-beat gain, and is given in terms of filter parameters as:

$$k_p = \frac{L}{T_s} + \frac{R}{2} \quad (2-13)$$

Also an integral part is needed to remove static errors caused by non-linearities, noisy measurements and non-ideal components. The proportional-integral (PI) controller equations will be:

$$\underline{u}_{dq}^*(k) = \underline{FF}_{dq} + j\omega L\underline{i}_{dq}(k) + k_p(\underline{i}_{dq}^*(k) - \underline{i}_{dq}(k)) + \Delta\underline{u}_{idq}(k) \quad (2-14)$$

where  $\underline{FF}_{dq}$  is the feed-forward term, while  $\Delta\underline{u}_{idq}$  is the integration term of the controller. It is implemented as [44]:

$$\Delta\underline{u}_{idq}(k+1) = \Delta\underline{u}_{idq}(k) + k_i(\underline{i}_{dq}^*(k) - \underline{i}_{dq}(k)) \quad (2-15)$$

where  $k_i$  is the integration constant, which can be written as:

$$k_i = \frac{k_p T_s}{T_i} \quad (2-16)$$

where  $T_i$  is the integral time constant and here it is chosen to be equal to the L-filter time constant  $T_i = \frac{L}{R}$ .

### 2.3.1 Performance of VCC with dead-beat gain

The concept of dead-beat response is unique to discrete time control systems [44]. In dead-beat control, the sampling time  $T_s$  is the only design parameter, since the response settles down in at most one sampling time. Hence, if  $T_s$  is very small the settling time will be also very small which implies a large magnitude of the

control signal  $u_{dq}^*$ . Since it is not possible to increase the control signal without bound because of the saturation phenomena, a trade-off must be made to choose  $T_s$ . However,  $T_s$  is also affected by the type of application. Since the switching frequency of the VSC valves is taken as half the sampling frequency,  $T_s$  should meet the valve specification.

In order to examine the transient performance of the VCC with dead-beat gain, simulations have been carried out using Matlab/Simulink. The system in Fig. 2.1 has been implemented assuming that the DC regulator is fast and ideal so that the DC voltage can be considered constant. Also the reference current generation algorithm is not used, since the transient response is considered performing unit steps in active current reference  $i_d^*$  and reactive current reference  $i_q^*$ . The system data and controller data are presented in Table 2-1 and Table 2-2 respectively.

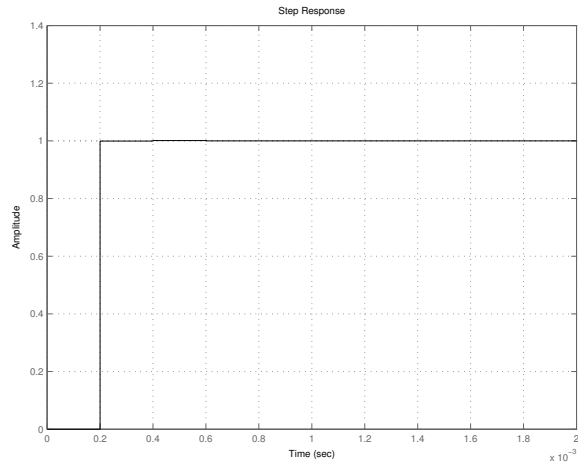
**Table 2-1 System data.**

| Description                                  | Symbol   | Value         |
|--|----------|---------------|
| Nominal (base) rms phase-to-phase AC voltage | $E$      | 400 V         |
| Nominal (base) rms phase current             | $I_n$    | 100 A         |
| Nominal (base) grid frequency                | $f_n$    | 50 Hz         |
| Nominal (base) DC link voltage               | $U_{dc}$ | 650 V         |
| Nominal (base) DC input current              | $I_{dc}$ | 107 A         |
| Filter resistance                            | $R$      | 23 m $\Omega$ |
| Filter inductance                            | $L$      | 0.73 mH       |
| DC link capacitance                          | $C$      | 550 $\mu$ F   |

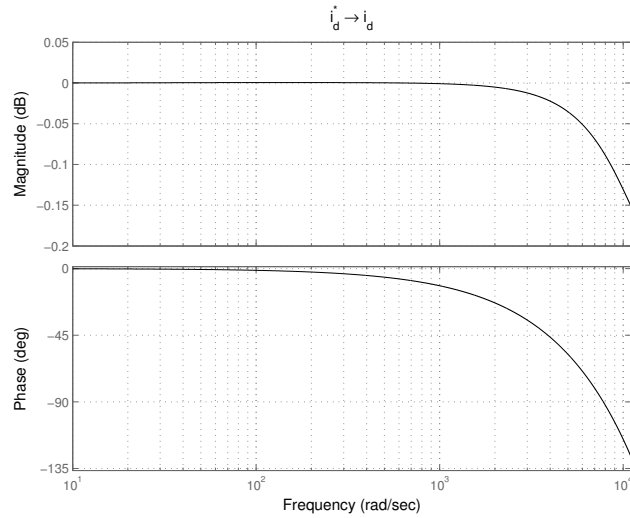
**Table 2-2 Main controller data.**

| Constant                  | Symbol | Value       |
|---------------------------|--------|-------------|
| Sampling frequency        | $f_s$  | 5 kHz       |
| Sampling time             | $T_s$  | 200 $\mu$ s |
| Dead-beat gain            | $k_p$  | 3.7         |
| Integration time constant | $T_i$  | 0.03 s      |

The transient response shown in Fig. 2.3 establishes the dead-beat concept where the  $d$ -component of the actual grid current equals its reference after one sample. The bandwidth, which is the frequency at which the gain drops -3 dB, is high (as shown in Fig. 2.4) implying short settling time.



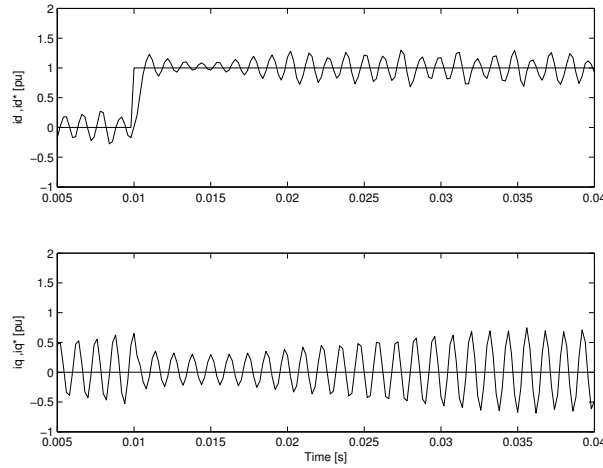
**Fig. 2.3** Transient response for the  $d$ -component of actual grid current due to a unit step in the  $d$ -component of reference grid current.



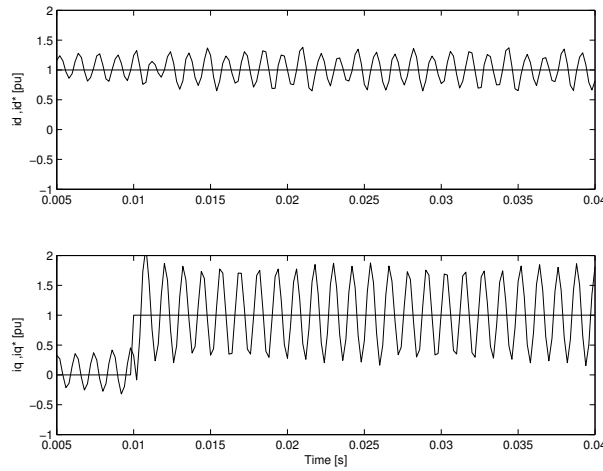
**Fig. 2.4** Bode plot from  $d$ -component of grid current reference to  $d$ -component actual grid current.

However, if the system is implemented practically, one sample time delay will be introduced due to the calculation time of digital controllers [29]. If this time delay is considered, an oscillatory behaviour of the controller will be obtained. This is

shown in Fig. 2.5, for a step in the active component of the reference current  $i_d^*$ , and in Fig. 2.6, for a step in the reactive reference current  $i_q^*$ .



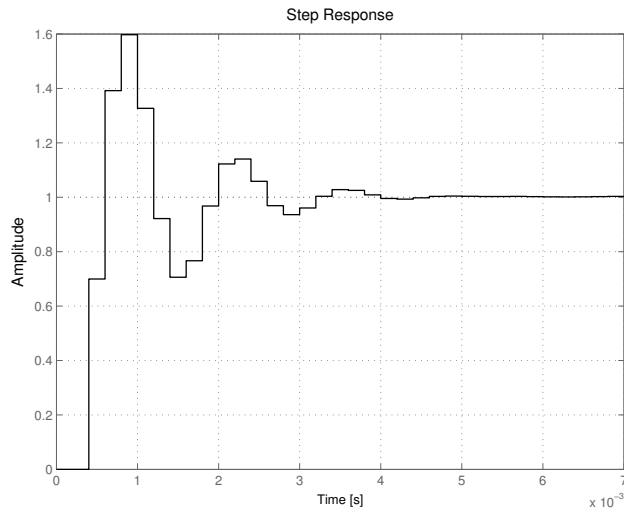
**Fig. 2.5 Time response of VCC due to unit step change in  $i_d^*$  (top) while  $i_q^*$  is kept constant (bottom): system with time delay and dead-beat gain.**



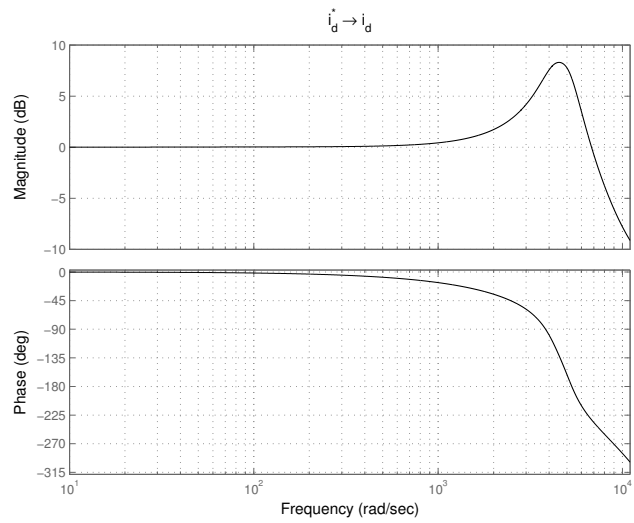
**Fig. 2.6 Time response of VCC due to a unit step change in  $i_q^*$  (bottom) while  $i_d^*$  is kept constant (top): system with time delay and dead-beat gain.**

If the proportional gain of the system is reduced to 70% of dead-beat gain, the oscillations decrease. However, since the gain is reduced, the settling time of the current is longer (about 4 ms) and high overshoot is introduced, as shown in Fig.

2.7. The high gain in the frequency response shown in Fig. 2.8 also implies the high overshoot.

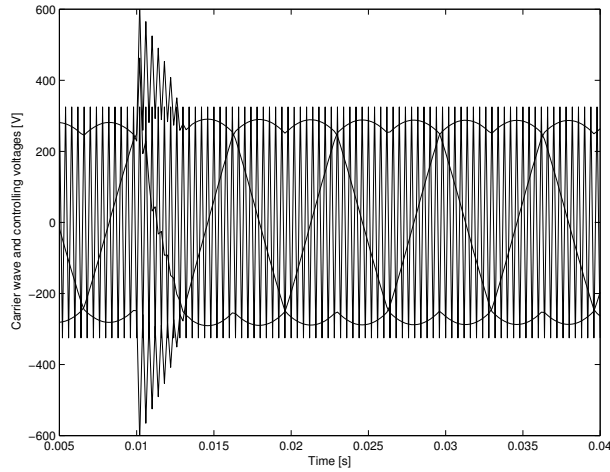


**Fig. 2.7 Step response for the actual grid current due to a unit step in the reference active grid current: time delay and reduced gain.**

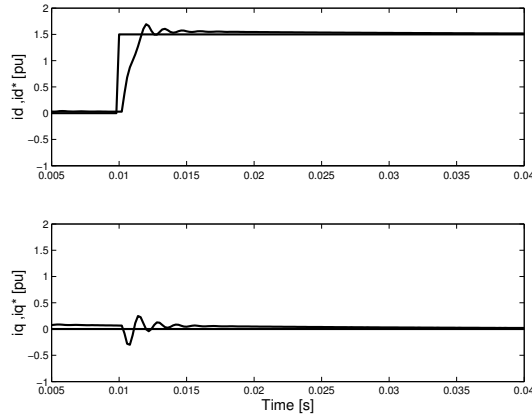


**Fig. 2.8 Bode plot from active grid current reference to actual active grid current: time delay and reduced gain.**

Moreover, when a larger step in  $i_d^*$  is considered, saturation occurs at which the controlling voltage is bigger than the carrier wave amplitude used by the PWM modulator as illustrated in Fig. 2.9. That will result in a slow response and large cross coupling between active and reactive current components as shown in Fig. 2.10.



**Fig. 2.9 Carrier wave and optimized controlling voltages of the PWM modulator with a step in  $i_d^*$  from 0 to 150 A (0.5 p.u.).**



**Fig. 2.10 Response of active current (upper) and reactive current (lower) due to unit step change in  $i_d^*$  while  $i_q^*$  is kept constant: system with 70% of dead-Beat gain.**



### 2.3.2 Modified VCC

In order to improve the transient response of the system and to obtain a high current bandwidth of the VSC, some modifications are implemented in the VCC. These are:

- Smith predictor for delay time compensation;
- Back calculation to deal with integrator windup;
- Limitation of the reference voltage vector.

#### Smith predictor

The time delay in a controlled system would add to the phase lag at a given frequency without altering the magnitude. This increase in the phase lag reduces the system's stability margin and can make the system difficult to control [30]. One solution is to use a Smith predictor, named after O. J. M. Smith who published the method in 1958 [30].

Consider a system (plant) with a delay time  $\tau$ , as depicted in Fig. 2.11, having the following transfer function in the  $s$ -domain:

$$G_p(s) = G(s)e^{-\tau s} \quad (2-17)$$

The Smith predictor attempts to remove the effect of the delay time from the closed-loop control system so that the controller can be designed as if no time delay was present. If the dotted line in Fig. 2.11 is ignored, the delay-free plant will be used to generate the output signal, which would exist if the delay were absent. This delay-free signal is then used in the usual feedback loop instead of the plant output. To help to account for errors in the delay-free model, the delay itself is also modelled and used in order to generate what should be a model of the actual plant output including the delay effect. The dotted line shows how this is then compared with the actual output so that the modelling error is also fed back into the control loop. In this way, the effect of errors in the delay-free model is reduced.

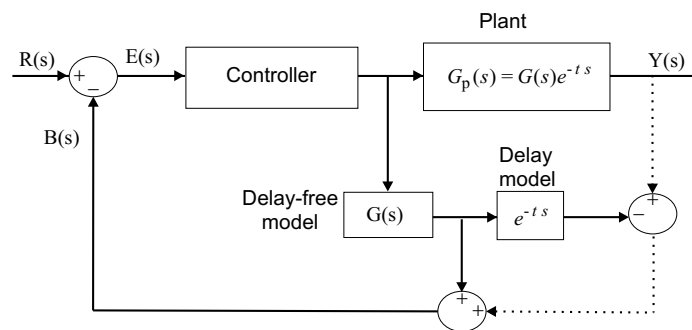


Fig. 2.11 Smith predictor arrangement.

The Smith predictor is implemented in a way analogous to a state observer, which means running a model of the plant in parallel to the plant itself. The estimated or predicted currents are calculated using the plant (model) in (2-9). A compensation term is added to compensate for the error introduced between the model and estimated values. The estimated currents calculated by the Smith predictor are presented in the  $dq$ -frame as:

$$\hat{i}_{dq}(k+1) = \frac{T_s}{L} (u_{dq}^*(k) - e_{dq}(k)) + \left(1 - \frac{RT_s}{L} - j\omega T_s\right) \hat{i}_{dq}(k) + k_{ps}(i_{dq}(k) - \hat{i}_{dq}(k)) \quad (2-18)$$

where  $\hat{i}_{dq}$  represents the estimated currents,  $k_{ps}$  is the Smith gain used for error compensation. By using the Smith predictor, the time delay in the input current of the controller will be cancelled, as illustrated in Fig. 2.12, assuming that  $i_{dq}(k-1) = \hat{i}_{dq}(k-1)$  and  $\hat{i}_{dq}(k) = i_{dq}(k)$ .

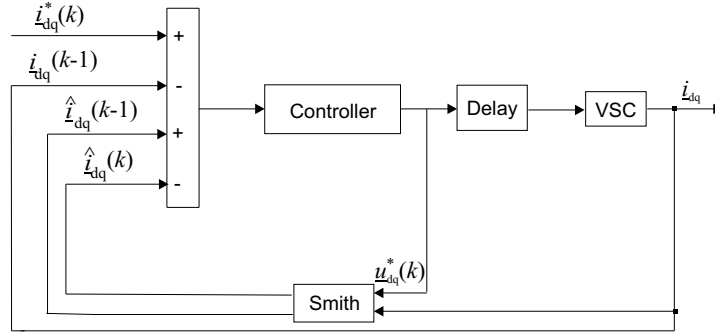
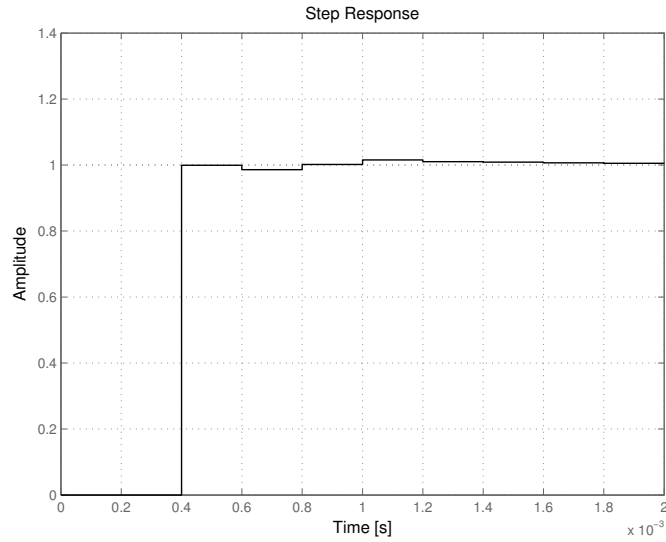


Fig. 2.12 Smith predictor operation.

The transient response is shown in Fig. 2.13 when using dead-beat gain and Smith predictor gain of 0.5. It shows that the actual current is equal to its reference command after two samples, one due to the dead-beat gain and the other is due to the introduced one-sample time delay.



**Fig. 2.13 Transient response in active current due to a unit step in active current reference: system with dead-beat gain and Smith predictor.**

### **Integrator windup**

The output voltages of the VSC,  $u_a(t)$ ,  $u_b(t)$  and  $u_c(t)$ , are controlled by the switching signals,  $sw_a(t)$ ,  $sw_b(t)$  and  $sw_c(t)$ , which are generated by the PWM as depicted in Fig. 2.1 and Fig. 2.14. In the  $\alpha\beta$ -frame this relation is:

$$\underline{u}_{\alpha\beta}(t) = \frac{u_{dc}}{2} \underline{sw}_{\alpha\beta}(t) \quad (2-19)$$

where the switching signal in  $\alpha\beta$ -frame is:

$$\underline{sw}_{\alpha\beta}(t) = \sqrt{\frac{2}{3}} \left( sw_a(t) + e^{j\frac{2\pi}{3}} sw_b(t) + e^{j\frac{4\pi}{3}} sw_c(t) \right) \quad (2-20)$$

Each switching signal may take a value of 1, where the corresponding upper valve is turned on and the lower valve is turned off, or -1, where the corresponding upper valve is turned off and the lower valve is turned on. This results in eight different switching combinations with corresponding eight voltage vectors, as explained in Table 2-3.

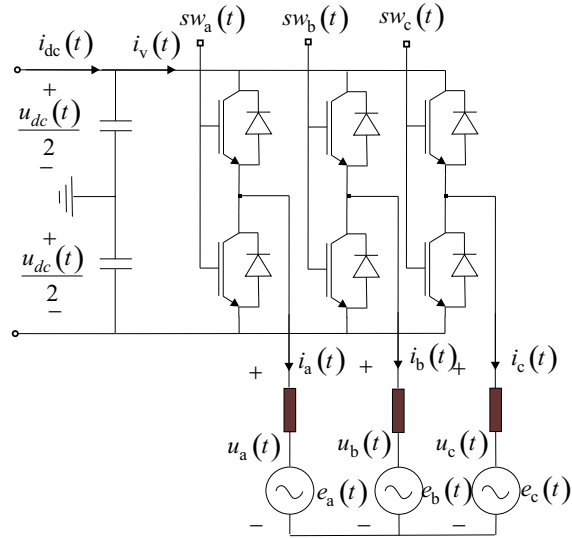


Fig. 2.14 VSC main circuit.

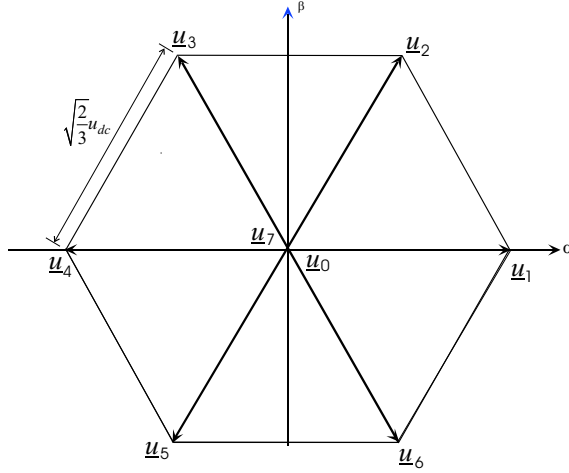
Table 2-3 Switch combinations and resulting voltage vectors.

| $sw_a$ | $sw_b$ | $sw_c$ | $\underline{u}$   | $abs(\underline{u})$ | $arg(\underline{u})$ |
|--------|--------|--------|-------------------|----------------------|----------------------|
| -1     | -1     | -1     | $\underline{u}_0$ | 0                    | $0^\circ$            |
| 1      | -1     | -1     | $\underline{u}_1$ | $\sqrt{2/3}u_{dc}$   | $0^\circ$            |
| -1     | 1      | -1     | $\underline{u}_2$ | $\sqrt{2/3}u_{dc}$   | $60^\circ$           |
| 1      | 1      | -1     | $\underline{u}_3$ | $\sqrt{2/3}u_{dc}$   | $120^\circ$          |
| -1     | -1     | 1      | $\underline{u}_4$ | $\sqrt{2/3}u_{dc}$   | $180^\circ$          |
| 1      | -1     | 1      | $\underline{u}_5$ | $\sqrt{2/3}u_{dc}$   | $240^\circ$          |
| -1     | 1      | 1      | $\underline{u}_6$ | $\sqrt{2/3}u_{dc}$   | $300^\circ$          |
| 1      | 1      | 1      | $\underline{u}_7$ | 0                    | $0^\circ$            |

The six non-zero voltage vectors, denoted by  $\underline{u}_1, \underline{u}_2, \underline{u}_3, \underline{u}_4, \underline{u}_5$  and  $\underline{u}_6$ , form a hexagon as shown in Fig. 2.15. If the reference voltage vector is located in the region within the hexagon but outside the maximum circle that can be inscribed within it, over-modulation occurs, which results in low frequency current harmonics [29]. When the reference voltage vector is outside the hexagon, saturation occurs

which results mainly in integrator windup. In this case the integral of the current control error becomes large resulting in uncontrolled phase currents. One solution to avoid this is to stop the integration, but this would result in a reduced performance of the control system [31]. Instead, back calculation of the current error using a limited reference voltage is used to ride through the saturation period. More details can be found in [31] and [32]. The back calculated current can be found from (2-14), as:

$$\Delta i_{dq}(k) = \frac{1}{k_p} \left( \underline{u}_{dq}(k) - \underline{FF}_{dq}(k) - j\omega L i_{dq}(k) - \Delta \underline{u}_{dq}(k) \right) \quad (2-21)$$



**Fig. 2.15 Hexagon that is spanned by six non-zero voltage vectors in  $\alpha\beta$ -coordinate system.**

### Limitation of reference voltage

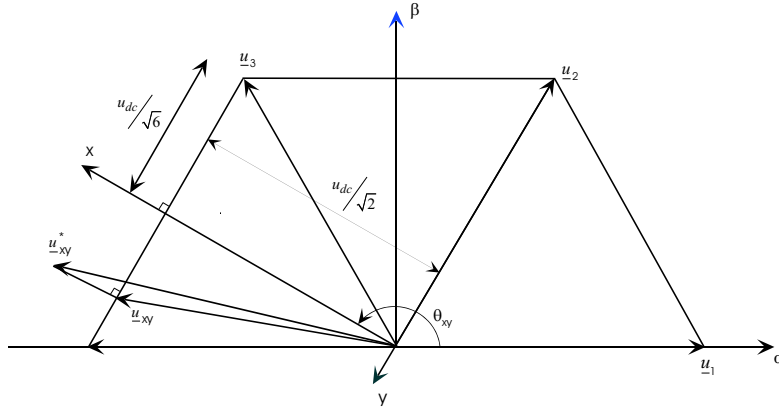
As mentioned above, the reference voltage vector should be limited in case of saturation to avoid integrator windup. There are many methods to do so, some of which are tested and compared in [32]. In this work the “minimum amplitude error limit method” (MAE), found in [31] and [32], is adopted. In this method a new reference voltage vector on the hexagon boundary that is closest to the original reference vector is chosen as shown in Fig. 2.16. This allows minimization of the voltage amplitude error. This is done by mapping the voltage reference into new coordinates  $xy$ . The  $xy$ -coordinate depends on the number of sector in the hexagon that contains the voltage reference. The reference voltage vector in the new coordinates  $\underline{u}_{xy}^*$  is obtained as:

$$\underline{u}_{xy}^* = \underline{u}_{\alpha\beta}^* \cdot e^{-j\theta_{xy}} \quad (2-22)$$

where  $\theta_{xy}$  is the angle between the  $\alpha$ -axis and the  $x$ -axis and is calculated as:

$$\theta_{xy} = (1 + 2(n-1))\pi / 6 \quad (2-23)$$

where  $n$  is the sector number at which the reference vector lies in the hexagon.



**Fig. 2.16 Principle of the minimum amplitude error method.**

The components of the limited reference voltage vector are calculated from Fig. 2.16 as:

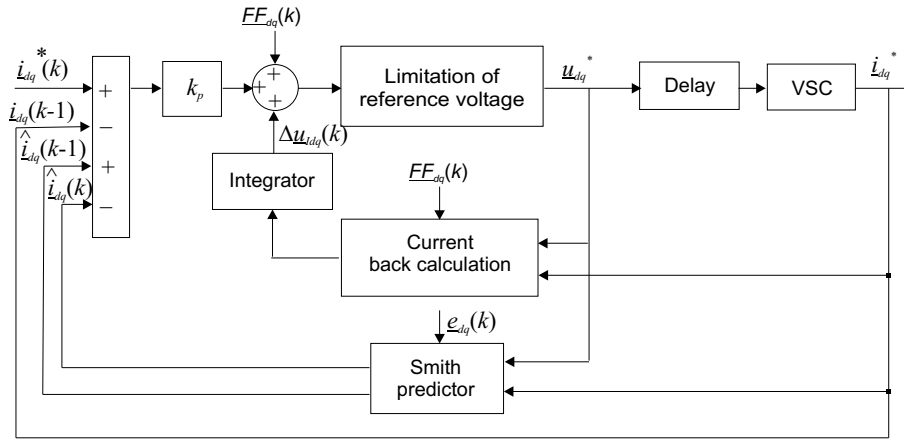
$$u_x = \frac{u_{dc}}{\sqrt{2}} \quad (2-24)$$

$$u_y = \begin{cases} u_y^* & |u_y^*| \leq \frac{u_{dc}}{\sqrt{6}} \\ \text{sign}(u_y^*) \cdot \frac{u_{dc}}{\sqrt{6}} & |u_y^*| > \frac{u_{dc}}{\sqrt{6}} \end{cases} \quad (2-25)$$

### 2.3.3 Performance of modified VCC

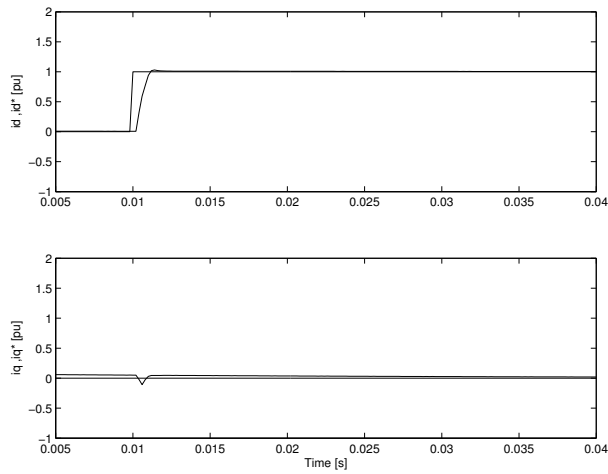
The modifications, presented in *Section 2.3.2*, have been applied to the VCC as suggested by the simplified block diagram shown in Fig. 2.17.

For the sake of comparison, the system utilising modified VCC with 70% dead-beat gain has been simulated for the same current steps used with the simple VCC. A Smith predictor gain of 0.5 was chosen by trial and error to give the best performance.



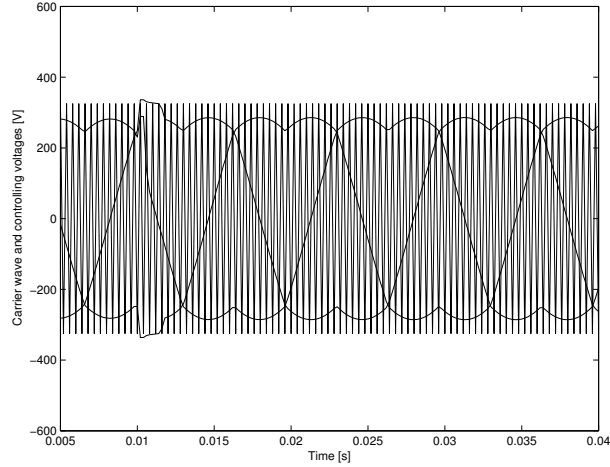
**Fig. 2.17 Block diagram of modified VCC.**

Comparing the response of the modified VCC shown in Fig. 2.18 to the simple VCC response shown in Fig. 2.5, shows that using the modified controller has effectively eliminated the current oscillations.

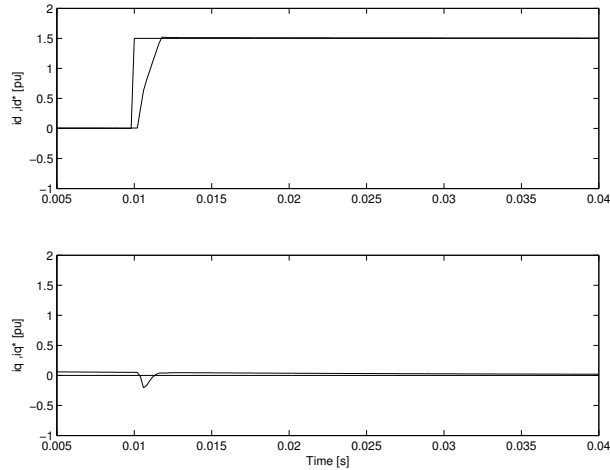


**Fig. 2.18 Time response of VCC due to a unit step change in  $i_d^*$  (upper) while  $i_q^*$  is kept constant (lower).**

Moreover, performing larger steps in the active component of the current reference  $i_d^*$ , the controlling voltage does not exceed the carrier wave, as suggested by Fig. 2.19, which means no saturation occurs. The response of the system is fast and the cross coupling between  $i_d^*$  and  $i_q^*$  is reduced, as shown by Fig. 2.20.



**Fig. 2.19** Carrier wave and optimized controlling voltages of the PWM modulator with a step in  $i_d^*$  from 0 to 150 A (0.5 p.u.).



**Fig. 2.20** Active current (upper) and reactive current (lower) due to a step in  $i_d^*$  from 0 to 1.5 p.u.

### 2.4 Performance in case of voltage dips

Since the main interest in this work is to examine and improve the performance of the VSC in case of voltage dips, the modified VCC has been implemented in the system shown in Fig. 2.1 and tested with different voltage dips using the classification described in Section 1.4.1. Both the DC-link voltage regulator and current reference generator are implemented as explained in the following.



## 2.4.1 DC-link voltage regulator

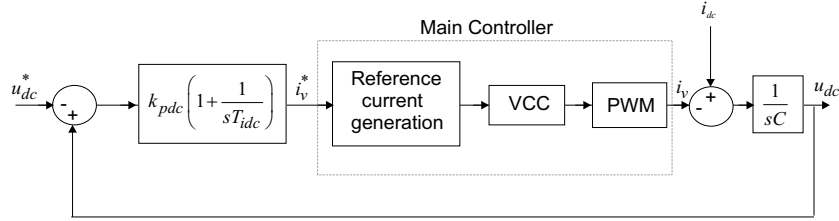
In many grid connected applications, e.g. drive systems or distributed generation utilising renewable sources, the DC-link voltage cannot be considered constant since the change in the grid voltage (e.g. due to voltage dips) will result in a change in the DC-link voltage. Hence, the DC-link voltage should be regulated to insure a correct operation of the VSC and to avoid damage to the power electronic switches and the DC-link capacitor. Also the DC-link current is not constant. However, its variations can be assumed to be much slower than the response time of the control system. Therefore the DC-link is modeled as a capacitor with a constant current source in parallel, which is referred to as weak DC-link model.

A proportional-integral (PI) controller is implemented, where the measured DC capacitor voltage  $u_{dc}$  is compared with its reference value  $u_{dc}^*$  and the error signal is used to produce a reference DC current signal  $i_v^*$  according to:

$$i_v^* = \Delta u_{dc} K_{pdc} \left( 1 + \frac{1}{sT_{idc}} \right) \quad (2-26)$$

Where  $k_{pdc}$ ,  $T_{idc}$  are the proportional gain and integral time constant of the PI-controller respectively,  $s$  is the Laplace operator, and  $\Delta u_{dc} = u_{dc} - u_{dc}^*$ .

The DC current  $i_v^*$  is then used by the reference current generation algorithm to calculate the  $dq$ -components of the reference currents in such a way to decrease the DC-link voltage ripples and grid current harmonics. The DC-link voltage regulator is presented in Fig. 2.21.



**Fig. 2.21** Block diagram of the overall controller.

Assuming that the main controller is fast and ideal and the reference DC voltage as a disturbance, the DC regulator transfer function can be expressed as:

$$\frac{i_v^*}{i_{dc}} = \frac{\frac{K_{pdc}}{C} \cdot \left( s + \frac{1}{T_{idc}} \right)}{s^2 + \frac{K_{pdc}}{C} s + \frac{K_{pdc}}{T_{idc} \cdot C}} \quad (2-27)$$

Comparing with the standard transfer function of a second order system  $TF(s)$ :

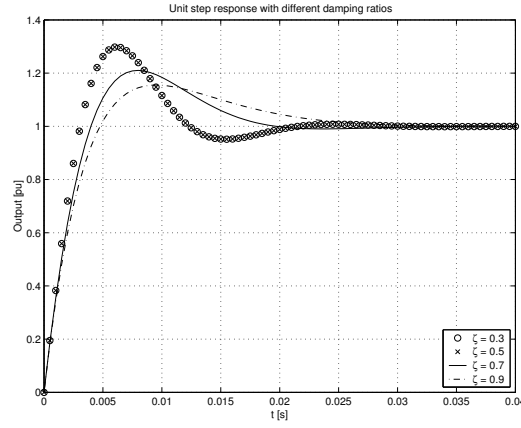
$$TF(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0s + \omega_0^2} \quad (2-28)$$

where  $\zeta$  is the damping factor, and  $\omega_0$  is the natural frequency of the feedback loop, the controller constants will be:

$$T_{\text{idc}} = \frac{K_{\text{pdc}}}{\omega_0^2 \cdot C} \quad (2-29)$$

$$K_{\text{pdc}} = \frac{4\zeta^2}{T_{\text{idc}}} \cdot C \quad (2-30)$$

Selecting  $\zeta = 0.7$  offers a stable response with minimal output overshoot which is free of oscillations [31], as shown in Fig. 2.22. Equation (2-27) has been used to design the PI-controller by varying the value of  $K_{\text{pdc}}$  from 0 to 1 and testing the transient response of the system for a unit step change in the input.



**Fig. 2.22 Unit step response of the DC-link controller for different damping ratios.**

In Fig. 2.23, it is suggested that the DC-link voltage regulator has a faster response as the proportional gain increases. However, a value of 0.2 has been chosen to give the fastest response for the overall control system. Finally, the value of  $T_{\text{idc}}$  is calculated from (2-30). The DC-link voltage regulator constants are reported in Table 2-4.

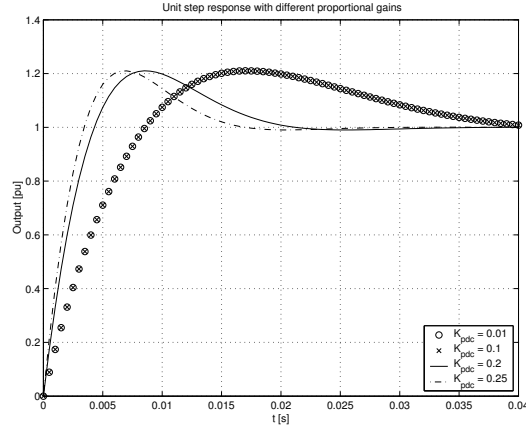


Fig. 2.23 Unit step response of the DC-link controller for different proportional gains.

Table 2-4 DC-link voltage regulator data.

| Constant                  | Symbol    | Value   |
|---------------------------|-----------|---------|
| Proportional gain         | $k_{pdc}$ | 0.2     |
| Integration time constant | $T_{idc}$ | 0.005 s |
| Damping ratio             | $\zeta$   | 0.7     |

## 2.4.2 DC-link capacitor design

The instantaneous active power difference between the AC and DC sides is stored in the capacitor, which causes the DC link voltage to vary. Hence, the size of the capacitor can be determined from the constraint on the maximum allowed DC-link voltage ripple  $\Delta u_{dc}$ . The design expression for the DC-link capacitor size, which has been derived, based on a simplified analysis of the instantaneous active power flow in [31], is:

$$C = \frac{S_n}{u_{dc}^* \Delta u_{dc}} \cdot \frac{1}{2\omega_n} \quad (2-31)$$

where  $S_n$  and  $\omega_n$  are the rated power of the VSC and the fundamental angular frequency of the grid. The allowed  $\Delta u_{dc}$  is considered as 5% of the rated voltage resulting in a DC-capacitance of 5.2  $\mu\text{F}$ . However, due to the high performance of the DC-link voltage controller along with the VCC, the size of the capacitance used is reduced to 550  $\mu\text{F}$ .

### 2.4.3 Current reference generation

In case of weak DC-link systems, proper current references should be generated in order to improve the performance of the VSC in such a way to minimize the DC voltage ripples and at the same time to decrease the AC currents amplitudes and/or harmonics. The generation algorithm depends on the power balance through the system. The active power at the AC side of the converter  $P_1$  is considered equal to the active power at the DC side  $P_{dc}$  assuming zero losses in the converter switches. Different power designations are shown in Fig. 2.24.

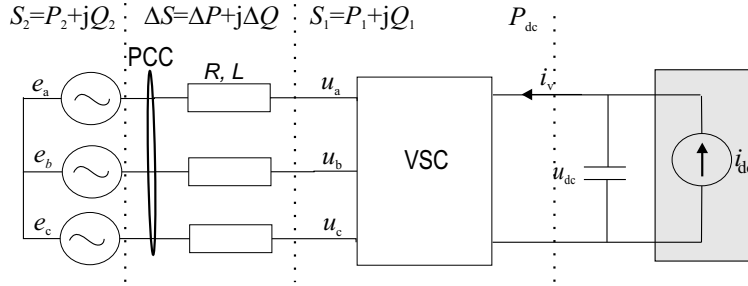


Fig. 2.24 VSC system with various power designations.

The apparent power at the AC-side of the converter  $S_1$  is:

$$S_1 = \underline{u}_{dq} \cdot \underline{i}_{dq}^{\text{conj}} = u_d i_d + u_q i_q + j(u_q i_d - u_d i_q) \quad (2-32)$$

In steady state, the output voltage of the VSC is defined by:

$$\underline{u}_{dq} = \underline{e}_{dq} + R \underline{i}_{dq} + j\omega L \underline{i}_{dq} \quad (2-33)$$

Substituting (2-33) into (2-32) results in:

$$S_1 = e_d i_d + e_q i_q + R(i_d^2 + i_q^2) + j[e_q i_d - e_d i_q + \omega L(i_d^2 + i_q^2)] \quad (2-34)$$

Separating the real and imaginary parts, (2-34) can be expressed in matrix form as:

$$\begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} \quad (2-35)$$

where  $P_1$  and  $Q_1$  are active and reactive power at the AC-side of the converter respectively. The terms  $\Delta P$  and  $\Delta Q$  are active and reactive power dissipated by the filter respectively, which are defined as:

$$\Delta P = R(i_d^2 + i_q^2) \quad (2-36)$$

$$\Delta Q = \omega L (i_d^2 + i_q^2) \quad (2-37)$$

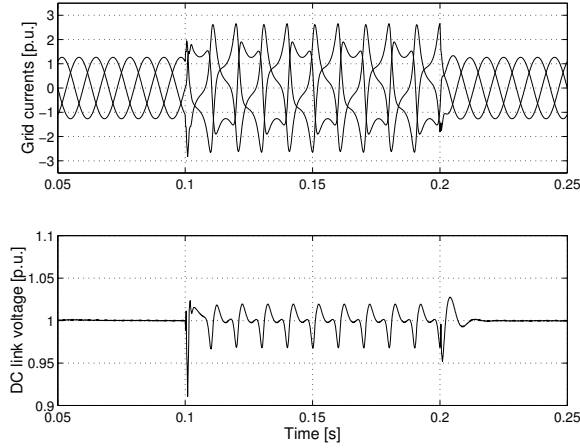
To achieve unity power factor, the reactive power at the grid side  $Q_2 = Q_1 - \Delta Q$  is nullified. The current references are then calculated using (2-35) as follows:

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} P_{ac} - \Delta P \\ 0 \end{bmatrix} \quad (2-38)$$

#### 2.4.4 Performance of modified VCC

The performance of the modified VCC, described in *Section 2.3.2*, has been examined when the grid voltage is subjected to a voltage dip of type “C” with 40% magnitude. The dip is applied at 0.1 s for duration of 0.1 s.

The grid current is shown in Fig. 2.25. Due to the appearance of the negative sequence components caused by the unbalanced grid voltage, second order harmonics are imposed on the current waveform during the dip. The instantaneous maximum value of the current, during the fault, almost reaches 3 p.u. (with the nominal current as base value). Also DC-link voltage peak-to-peak ripples are significant (about 6 % of nominal DC voltage).



**Fig. 2.25** Grid currents (upper) and DC voltage (lower) for 40% magnitude of dip type “C” using modified VCC.

## 2.5 Dual vector current controller (DVCC)

In [20] and [31], different arrangements for the VCC have been examined in case of unbalanced grid voltage. The dual vector current controller (DVCC), which consists of two separate PI controllers, one for controlling the positive-sequence voltage and the other for controlling the negative-sequence voltage, has been proved to give the best performance regarding grid current control and DC-link voltage regulation. A simplified scheme for the DVCC is shown in Fig. 2.26.

The positive sequence PI-controller is described in the positive  $dq$ -frame ( $dqp$ -frame), which rotates in the positive direction, as:

$$\underline{u}_{dqp}^*(k) = \underline{FF}_{dqp} + j\omega L \underline{i}_{dqp}(k) + k_p (\underline{i}_{dqp}^*(k) - \underline{i}_{dqp}(k)) + \Delta \underline{u}_{idqp}(k) \quad (2-39)$$

The negative sequence PI-controller is described in the negative  $dq$ -frame ( $dqn$ -frame), which rotates in the negative direction, as:

$$\underline{u}_{dqn}^*(k) = \underline{FF}_{dqn} - j\omega L \underline{i}_{dqn}(k) + k_p (\underline{i}_{dqn}^*(k) - \underline{i}_{dqn}(k)) + \Delta \underline{u}_{idqn}(k) \quad (2-40)$$

In addition, all the previous controller modifications described in Section 2.3.2 are applied for both positive and negative sequence controllers.

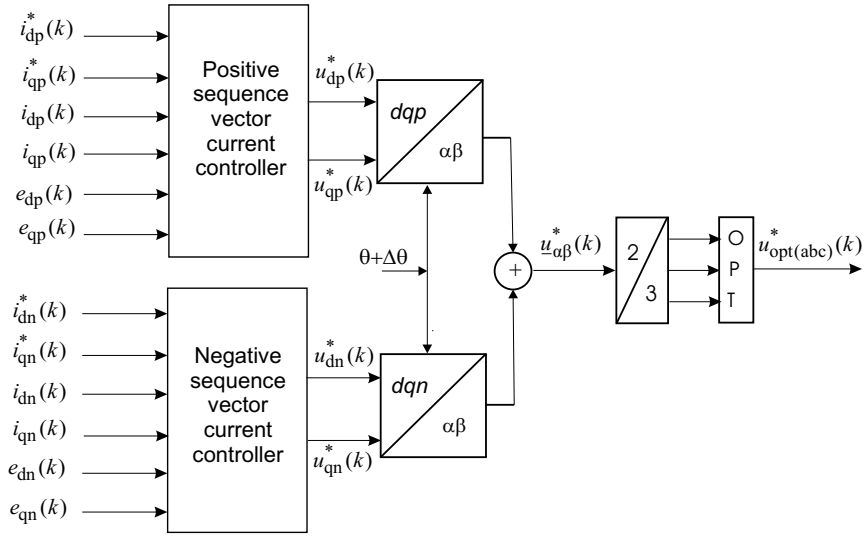


Fig. 2.26 Simplified block diagram of dual vector current controller.

## 2.5.1 Positive and negative sequence extraction

The decomposition of the supply voltage into positive and negative sequence is performed in the  $dq$ -frame, which rotates in the positive direction, in the same way as suggested in [20]. In this frame, the positive sequence is a constant vector (constant amplitude and fixed direction), while the negative sequence is a rotating vector, which rotates with twice the line frequency in the opposite direction, as compared with the positive sequence.

The measured supply voltage, in  $dq$ -frame, and the same signal, delayed by one-fourth of period at the fundamental frequency, are considered. Delaying the signal gives a vector composed by the same positive sequence component and a negative sequence component which has equal amplitude but opposite sign. Therefore, if the signal delayed by one-fourth of period is added to the measured supply voltage, the negative sequence voltage will be removed.

The positive sequence voltage component can thus be extracted from the measured values as:

$$e_{dq,p}(t) = \frac{1}{2} \cdot \left( e_{dq}(t) + e_{dq}\left(t - \frac{T}{4}\right) \right) \quad (2-41)$$

where  $T$  is the period at the fundamental frequency.

The negative sequence can be obtained in the positive rotating plane, as follows:

$$e_{dq,n,p}(t) = \frac{1}{2} \cdot \left( e_{dq}(t) - e_{dq}\left(t - \frac{T}{4}\right) \right) \quad (2-42)$$

which is then transformed into the negative rotating plane by transforming it into  $\alpha\beta$ -frame and back into  $dqn$ -frame using the opposite angle.

The block scheme of the adopted detection technique is shown in Fig. 2.27.

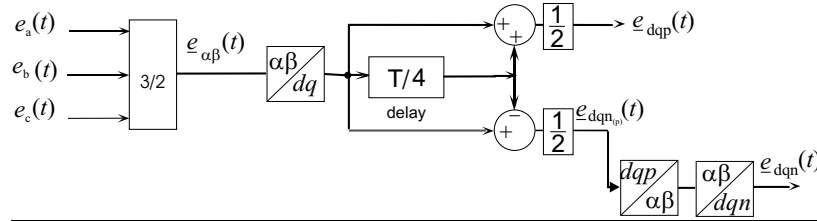


Fig. 2.27 Block scheme of adopted detection technique.

## 2.5.2 Generation of the current references

With the same notation of Fig. 2.24, the power flow equations can be written as follows:

$$P_1 = P_2 + \Delta P \quad (2-43)$$

$$Q_1 = Q_2 + \Delta Q \quad (2-44)$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2} \quad (2-45)$$

$$P_{s2,1} = P_{s2,2} + \Delta P_{s2} \quad (2-46)$$

where  $P$  and  $Q$  are the active and reactive powers, respectively. The subscripts “1” and “2” represent the power at the AC-side of the converter and at the grid side at the point of common coupling (PCC) respectively. The subscripts “c2” and “s2” stand for the second order harmonic cosine component and second order harmonic sine component of the corresponding power, which are called the oscillating powers and are due to the imbalance in the grid voltage. The terms  $\Delta P$ ,  $\Delta Q$ ,  $\Delta P_{c2}$ ,  $\Delta P_{s2}$  are the powers dissipated in the filter.

The apparent power  $S_2$  can be further defined at the PCC, in case of imbalance, in terms of grid voltages and currents in positive sequence and negative sequence  $dq$ -frame as:

$$S_2 = \left( e^{j\omega t} \cdot \underline{e}_{dq} + e^{-j\omega t} \cdot \underline{e}_{dqn} \right) \cdot \left( e^{j\omega t} \cdot \underline{i}_{dq} + e^{-j\omega t} \cdot \underline{i}_{dqn} \right)^{\text{conj}} = p(t) + jq(t) \quad (2-47)$$

from which the instantaneous active power  $p(t)$  and reactive power  $q(t)$  are defined as:

$$p(t) = P_{ac,2} + P_{c2,2} \cos(2\omega t) + P_{s2,2} \sin(2\omega t) \quad (2-48)$$

$$q(t) = Q_{ac,2} + Q_{c2,2} \cos(2\omega t) + Q_{s2,2} \sin(2\omega t) \quad (2-49)$$

where the subscript “ac” stands for the power at the fundamental frequency. Expanding (2-47) and separating different parts as suggested in (2-48) and (2-49), the following matrix is obtained:

$$\begin{bmatrix} P_{ac,2} \\ Q_{ac,2} \\ P_{s2,2} \\ P_{c2,2} \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \cdot \begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} \quad (2-50)$$

The apparent power  $S_1$  at the AC-side of the converter, before the filter, can also be expressed as:



$$S_1 = \left( e^{j\omega t} \cdot \underline{u}_{dqp} + e^{-j\omega t} \cdot \underline{u}_{dqn} \right) \cdot \left( e^{j\omega t} \cdot \underline{i}_{dqp} + e^{-j\omega t} \cdot \underline{i}_{dqn} \right)^{conj} = S_2 + \Delta S \quad (2-51)$$

where  $\Delta S$  is the apparent power consumed by the filter, which can be written as:

$$\Delta S = \Delta P + \Delta P_{c2} \cos(2\omega t) + \Delta P_{s2} \sin(2\omega t) + j\Delta Q \quad (2-52)$$

Expanding (2-51), by expressing the converter output voltage vector in terms of the grid voltage vector by using (2-33) expressed in  $dqp$ - and  $dqn$ -frames, results in the following expressions for the various powers consumed by the filter:

$$\Delta P = R(i_{dp}^2 + i_{qp}^2 + i_{dn}^2 + i_{qn}^2) \quad (2-53)$$

$$\Delta Q = \omega L(i_{dp}^2 + i_{qp}^2 - i_{dn}^2 - i_{qn}^2) \quad (2-54)$$

$$\Delta P_{c2} = 2R(i_{dp} \cdot i_{dn} + i_{qp} \cdot i_{qn}) + 2\omega L(i_{dp} \cdot i_{qn} - i_{qp} \cdot i_{dn}) \quad (2-55)$$

$$\Delta P_{s2} = 2R(i_{dp} \cdot i_{qn} - i_{qp} \cdot i_{dn}) + 2\omega L(-i_{dp} \cdot i_{dn} - i_{qp} \cdot i_{qn}) \quad (2-56)$$

The current references are then calculated, from (2-50) neglecting the VSC switching losses, as follows:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ Q_{ac,2} \\ P_{s2,1} - \Delta P_{s2} \\ P_{c2,1} - \Delta P_{c2} \end{bmatrix} \quad (2-57)$$

To implement this equation, different cases are considered as follows.

### Case 1: Solving nonlinear system of equations

Assuming zero oscillating power at the converter side, the nonlinear system of equations presented in (2-57) can be rewritten as follows:

$$\begin{aligned} e_{dp}i_{dp} + e_{qp}i_{qp} + e_{dn}i_{dn} + e_{qn}i_{qn} - P_{dc} + R(i_{dp}^2 + i_{qp}^2 + i_{dn}^2 + i_{qn}^2) &= 0 \\ e_{qp}i_{dp} - e_{dp}i_{qp} + e_{qn}i_{dn} - e_{dn}i_{qn} - Q_{ac,2} &= 0 \\ e_{qn}i_{dp} - e_{dn}i_{qp} - e_{qp}i_{dn} + e_{dp}i_{qn} + 2R(i_{dp}i_{qn} - i_{qp}i_{dn}) + 2\omega L(-i_{dp}i_{dn} - i_{qp}i_{qn}) &= 0 \\ e_{dn}i_{dp} + e_{qn}i_{qp} + e_{dp}i_{dn} + e_{qp}i_{qn} + 2R(i_{dp}i_{dn} + i_{qp}i_{qn}) + 2\omega L(i_{dp}i_{qn} - i_{qp}i_{dn}) &= 0 \end{aligned} \quad (2-58)$$

or in the general form:

$$Y(x) = 0 \tag{2-59}$$

Where  $Y$  is the function to be solved using numerical methods,  $x$  is the solution set:

$$x = \{i_{dp}, i_{qp}, i_{dn}, i_{qn}\} \tag{2-60}$$

Equation (2-58) can be solved using different numerical methods. Two methods have been tested to find the solution set of reference currents: “Newton-Raphson Method” and “Broyden’s method”. Newton-Raphson method is applied as in the algorithm shown in Fig. 2.28.

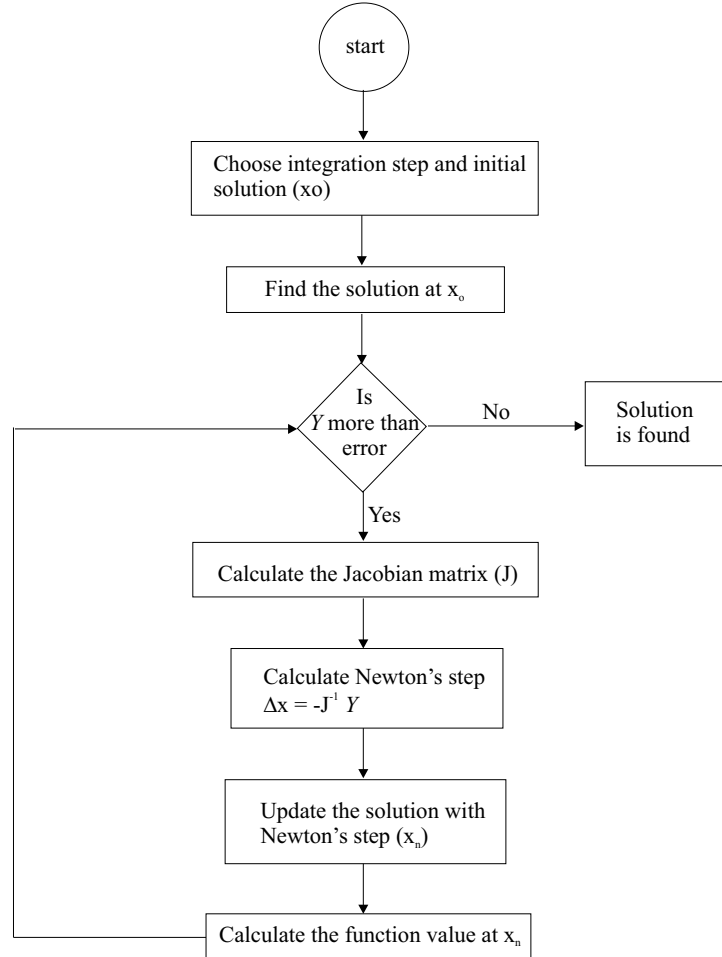


Fig. 2.28 Newton-Raphson method to solve system of non-linear equations.

In some cases, if analytical derivatives are unavailable, other methods (often called Secant methods) are introduced to provide an approximation to the Jacobian matrix. The best of these methods is the first one introduced, which is Broyden's method [54].

Using the algorithm shown in Fig. 2.28, the solution at the normal grid voltage condition is  $x = \{156.5, 0, 0, 0\}$ . For 40% dip type "C", the solution is  $x = \{273.7, 0.2, -117.1, -0.5\}$ . Although this algorithm can be used to obtain current reference values for the analysis purpose, it is not feasible to be implemented in the on-line simulation since fast transient response is needed.

### Case 2: Oscillating power flows from the VSC side to the filter

Assuming that the DC-side of the converter supplies the oscillating power to the filter, and neglecting the converter losses which means  $P_{ac,1}$  is equal to  $P_{dc}$ , the following equations will describe the different powers:

$$P_{ac,2} = P_{dc} - \Delta P, P_{dc} = u_{dc}^* \cdot i_v^* \quad (2-61)$$

$$Q_{ac,1} = \Delta Q, Q_{ac,2} = 0 \quad (2-62)$$

$$P_{c2,1} = \Delta P_{c2}, P_{c2,2} = 0 \quad (2-63)$$

$$P_{s2,1} = \Delta P_{s2}, P_{s2,2} = 0 \quad (2-64)$$

Substituting in (2-57), the reference currents that are calculated as:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (2-65)$$

A dip type "C" with magnitude of 40% has been applied to the VSC system at 0.2 s with duration of 0.1 s. The oscillating powers at the converter side oscillate with double the fundamental frequency during the dip. This means that the DC-link voltage and then the DC-link power both oscillate with double the fundamental frequency, as shown in Fig. 2.29. Then, the current references will also oscillate with double the fundamental frequency during the dip according to (2-65). Consequently  $P_{c2}$  and  $P_{s2}$ , which are the amplitudes of oscillating power components, will also oscillate with double the fundamental frequency as shown by Fig. 2.30 and Fig. 2.31. Since the positive and negative sequence current references oscillate, the actual current will not follow its reference as shown in Fig. 2.32. To smooth out the current references, two ways are proposed. The first way is to transform the current references into the three-phase domain and then transform back into vectors in the  $dqp$ - and  $dqn$ - frames, which are then used by the controller.

In this way the actual current will follow the reference current. However, the transient performance is worse since we are adding a time delay to the system, this is realised in the DC-link voltage shown in Fig. 2.33. Another way is to develop an algorithm that compensates for the oscillations and produces constant current commands during faults, as done in *Case 4*.

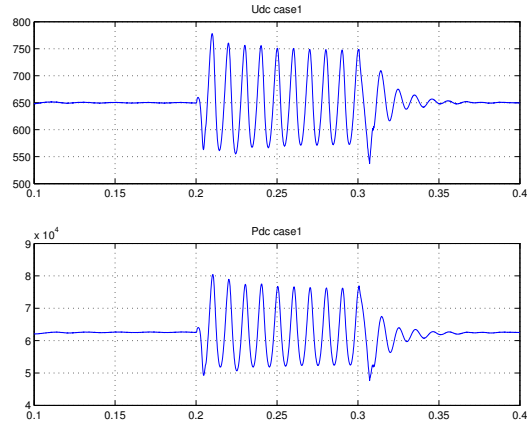


Fig. 2.29 DC voltage (upper), and DC power (lower) for case 2.

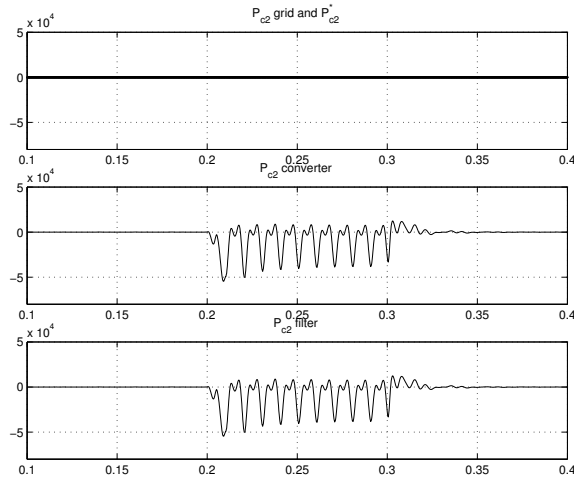


Fig. 2.30  $P_{c2}$  at grid (upper), converter (middle), and filter (lower) for case 2.

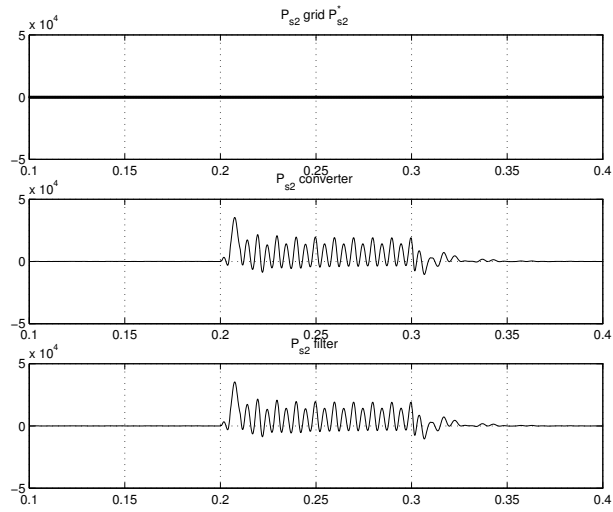


Fig. 2.31  $P_{s2}$  at grid (upper), converter (middle), and filter (lower) for case 2.

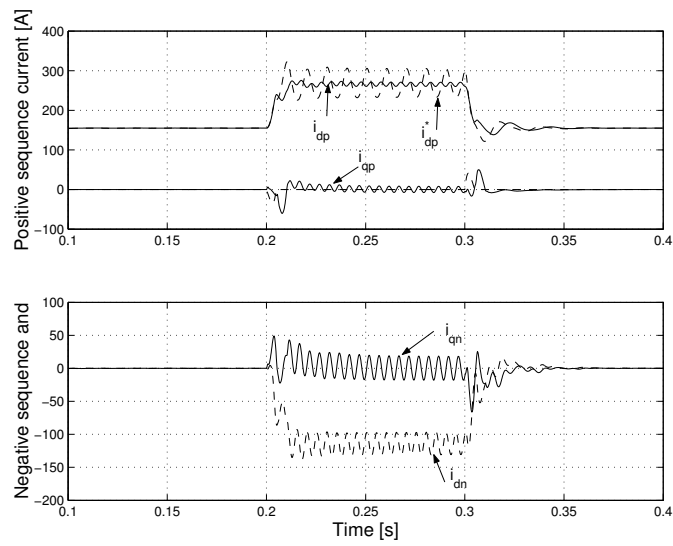
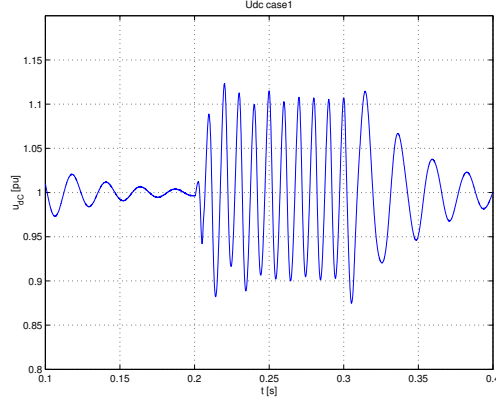


Fig. 2.32 Reference current , and actual current in  $dqp$ -frame (upper) and  $dqn$ -frame (lower).



**Fig. 2.33** DC-link voltage in case of transforming back the current references before using them in the controller.

### Case 3: Reactive power injection

It has been assumed in *case 2* that unity power factor operation is needed ( $Q_{ac,2} = 0$ ). However, if the system is supposed to supply some reactive power to compensate for the lagging power factor loads connected to the same bus, then  $Q_{ac,2}$  must be set to a certain value depending on the required power factor. Then  $Q_{ac,2}$  is calculated as follows:

$$Q_{ac,2} = P_{ac,2} \tan(\phi) \quad (2-66)$$

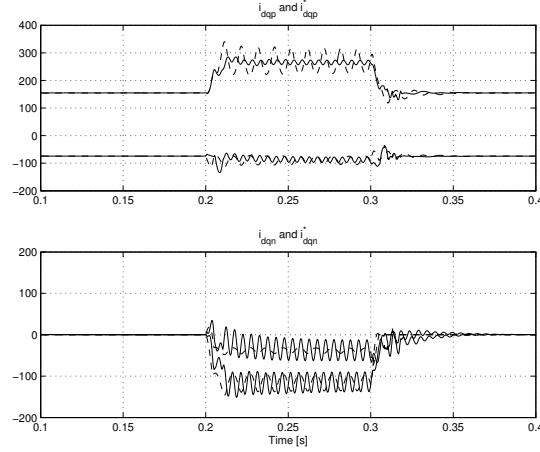
The angle  $\phi$  is positive to give a leading power factor  $pf$ , which is defined as follows:

$$pf = \cos(\phi) \quad (2-67)$$

If  $pf = 0.9$  is required, then  $Q_{ac,2} = 0.48 P_{ac,2}$  should be set in the following equation:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ Q_{ac,2} \\ 0 \\ 0 \end{bmatrix} \quad (2-68)$$

The currents at the grid side is shown in Fig. 2.34.



**Fig. 2.34 Active and reactive grid currents in  $dqp$ -frame (upper) and  $dqn$ -frame (lower): reference (dashed) and actual (solid).**

**Case 4: Oscillating power flows from the grid side to the filter**

In this case the grid supplies the oscillating powers to the filter, as given in the following equation:

$$\begin{bmatrix} i_{dp}^* \\ i_{qp}^* \\ i_{dn}^* \\ i_{qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{dc} - \Delta P \\ 0 \\ -\Delta P_{s2} \\ -\Delta P_{c2} \end{bmatrix} \quad (2-69)$$

The current references are forced to take a constant value as shown in Fig. 2.35 for 40% magnitude of dip type “C”. The oscillating power components are smoothed in the different parts of the system as shown in Fig. 2.36 and Fig. 2.37. The DC voltage and DC-link power are also smoothed during the fault, as depicted in Fig. 2.38.

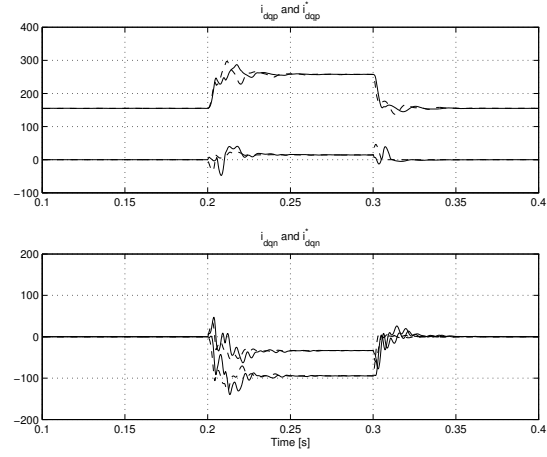


Fig. 2.35 Reference current (dashed) and actual current (solid) for  $dqp$ -components (upper) and  $dqn$ -components (lower) for case 4.

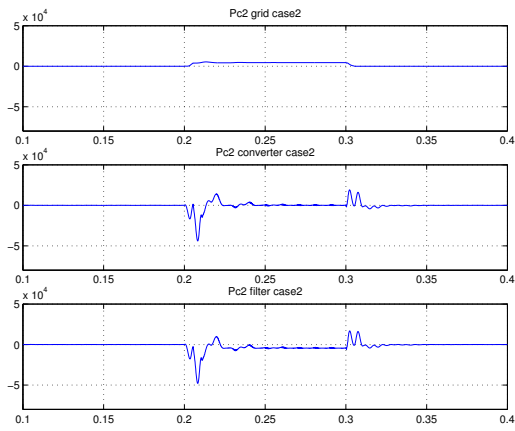
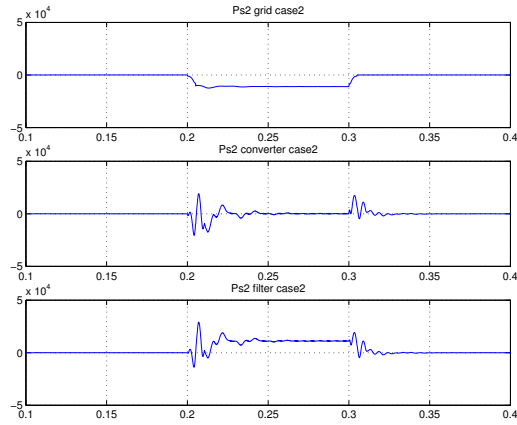
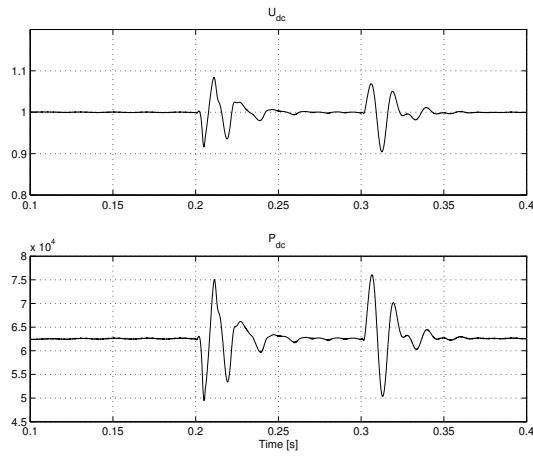


Fig. 2.36  $P_{c2}$  at grid (upper), at converter (middle), and at filter (lower) for case 4.





**Fig. 2.37**  $P_{s2}$  at grid (upper), at converter (middle), and at filter (lower) for case 4.



**Fig. 2.38** DC voltage (upper) and DC power (Lower) for case 4.

## 2.6 Simulation results

In this section the simulation results when implementing the DVCC to the system shown in Fig. 2.1 using Matlab/Simulink are presented. Different simulations have been run for the two algorithms mentioned previously as *case 2* and *case 4*. Dips with phase angle jump are also considered using the four values suggested in [17] and reported in *Section 1.4.2*. Also the effect of changing the input

power  $P_{in}$  is simulated in order to further evaluate the situation when the renewable source does not deliver its nominal active power, which is often the case.

### 2.6.1 Voltage dips without phase angle jump

For the sake of generality, all dip types are examined in case of zero phase angle jump ( $\psi = 0$ ). The results, for the two algorithms mentioned as *case 2* and *case 4*, are shown only for the dip magnitudes presented in Table 2-5. These values are chosen so that the positive-sequence magnitude for all dips is the same and equal to 70% magnitude of dip type “A”.

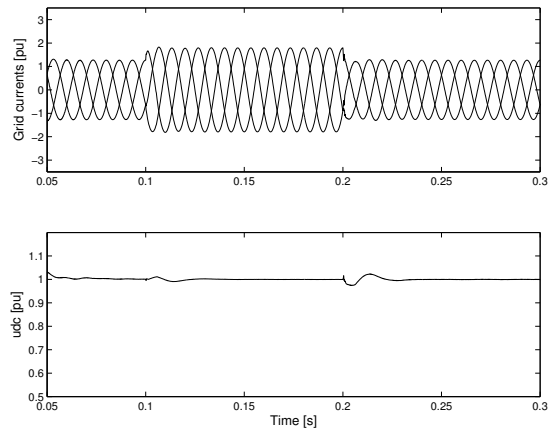
**Table 2-5 Dip magnitudes used in simulations.**

| Dip type | $V_{dip}$ [%] | $e_{dp}$ [V] | $e_{dn}$ [V] | $e_{qp}$ [V] | $e_{qn}$ [V] |
|----------|---------------|--------------|--------------|--------------|--------------|
| A        | 70            | 280          | 0            | 0            | 0            |
| B        | 10            | 280          | -120         | 0            | 0            |
| C        | 40            | 280          | 120          | 0            | 0            |
| D        | 40            | 280          | -120         | 0            | 0            |
| E        | 55            | 280          | 60           | 0            | 0            |
| F        | 55            | 280          | -60          | 0            | 0            |
| G        | 55            | 280          | 60           | 0            | 0            |

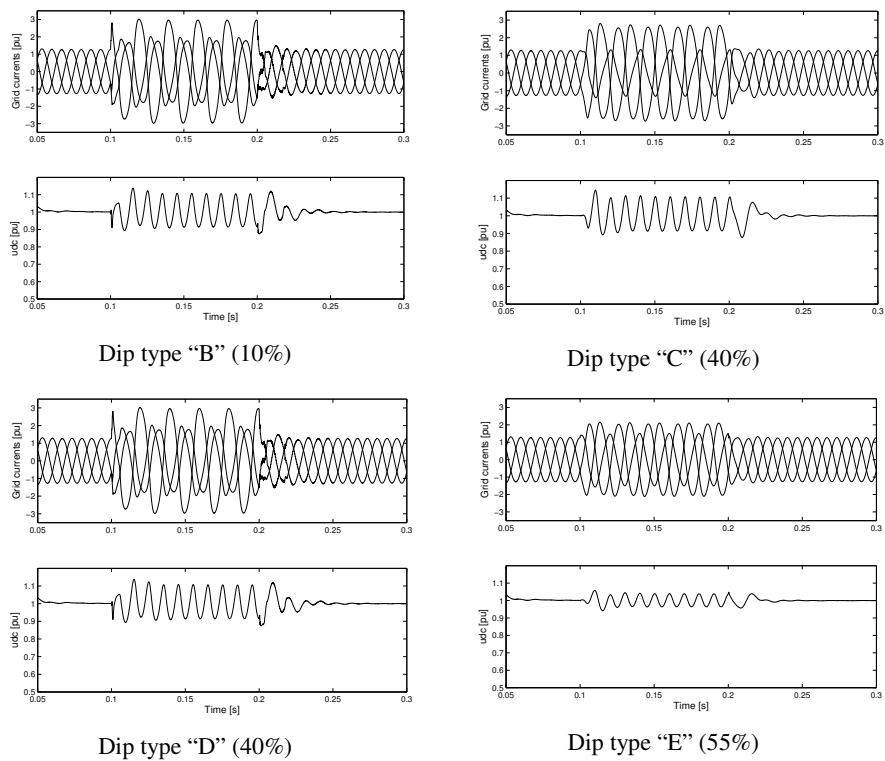
All dip types are applied to the system described in Fig. 2.1. The dip starts at 0.1 s for duration of 0.1 s.

#### Simulation results for case 2

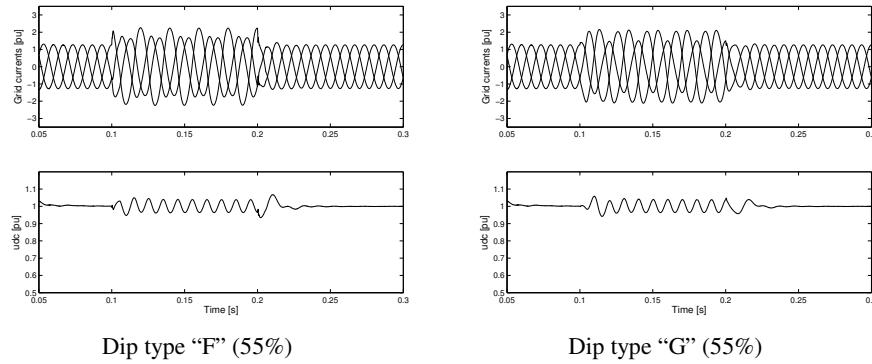
The current reference values are calculated using (2-65), at which the values of the grid currents that are used to calculate  $\Delta P$  are taken from the previous sample. Simulations have been run with all seven dip types described in *Section 1.4.1* and with magnitude varying from 0.1 p.u. to 0.9 p.u. in steps of 0.1. However, only the results corresponding to the magnitudes in Table 2-5 are shown in Fig. 2.39, for the balanced voltage dip, and in Fig. 2.40 and Fig. 2.41, for the unbalanced voltage dips.



**Fig. 2.39** Voltage dip type “A” with 70% magnitude: grid current (top) and DC voltage (bottom).



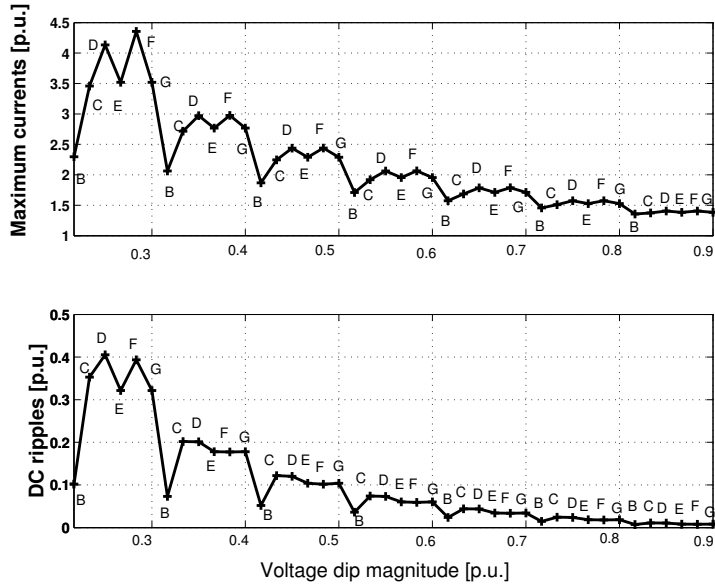
**Fig. 2.40** Grid currents and DC link voltage for dip types “B” through “E”.



**Fig. 2.41** Grid currents and DC link voltage for dip types “F” and “G”.

Since the DC side supplies the oscillating powers in case of unbalanced dips, the DC voltage will contain 100 Hz voltage ripple. However, the grid currents are mainly 50 Hz sinusoidal waves, in spite of the unbalance and increased magnitudes. As calculated from the dip classification given in Table 1-3, dip type “B” of magnitude 10% has exactly the same behavior as dip type “D” of magnitude 40%, since they both have the same positive and negative sequence components. The same applies for dip type “E” of magnitude 55% and dip type “G” of the same magnitude. Dip types “E” and “G” have exactly the same performance regardless of the dip magnitude, since they have same negative and positive sequence components in the  $dq$ -frame.

The effect of all unbalanced types of dips, with various magnitudes, on the maximum grid current and DC voltage ripples, which are both important in designing the converter circuit in order to ride through the voltage dip period, is represented in Fig. 2.42. The dip magnitude starts from 30%, since the controller will not work for all dips with magnitudes under this value due to the increased current, which accumulates in the current references and then gives unstable operation of the controller. However, although the main interest here is to keep the system working in case of voltage dips, it might not be wise to keep it on line for such small magnitudes. This is because it will require much higher specifications for the converter switches, which means more money to ride through an event that might happen once a year. It could be less costly to disconnect the system in case of such small dip magnitudes.



**Fig. 2.42 Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes between 0.3 and 0.9 p.u. (case 2).**

It is worth mentioning here that all simulations have been run for input DC power of 90% of the nominal value, since this power should be supplied from a renewable source, which normally supplies less than its nominal power. So if the converter system is to be designed to ride through all dip types for magnitudes starting from 30% and for 90% input power, the maximum current the switches should be able to hold is 4.35 p.u., which happens in case of dip type “F” of magnitude 30%. Also, the worst expected DC ripple is about 0.4 p.u., which happens in case of 30% magnitude of dip type “D” or “F”.

The same results are plotted separately for the different types of dips, including also the balanced one, in Fig. 2.43. The system in case of dip type “A” has the best performance considering DC voltage ripples because the oscillating powers are nullified for balanced grid voltages, while in case of dip type “B” the system has the best performance considering the maximum grid currents since only one phase is down and the other two phases are healthy. Dips “C” and “D” generate almost the same DC voltage ripples, and that also applies for dips “E”, “F”, and “G”.

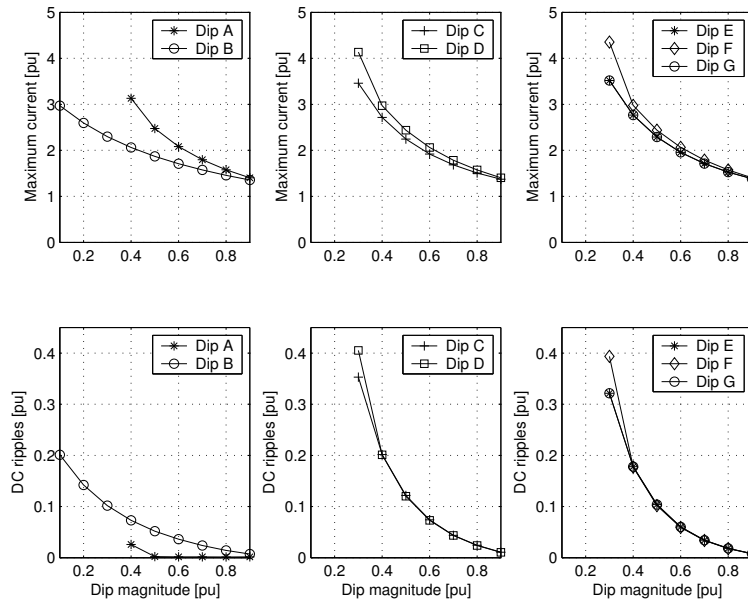
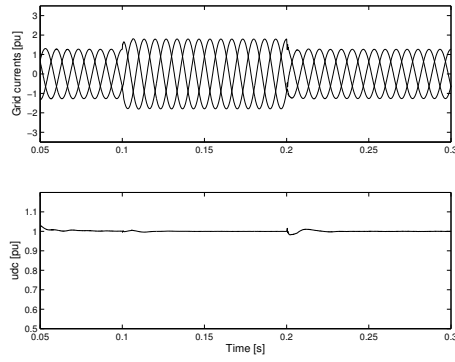


Fig. 2.43 Maximum grid current (upper plots) and DC voltage ripples (lower plots).

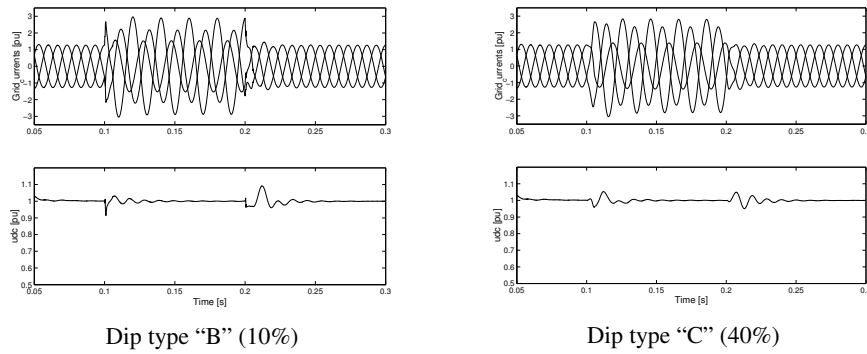
#### Simulation results for case 4

The current reference values are calculated using (2-69), where the values of grid currents that are used to calculate  $\Delta P$ ,  $\Delta P_{s2}$ , and  $\Delta P_{c2}$  are taken one sample back. Simulations have been run with all seven dip types mentioned previously and with magnitude varying from 0.1 p.u. to 0.9 p.u. in steps of 0.1. However, for the sake of comparison between the two cases, only the magnitudes in Table 2-5 are shown in Fig. 2.44 for the balanced voltage dip and Fig. 2.45 to Fig. 2.47 for the unbalanced voltage dips.

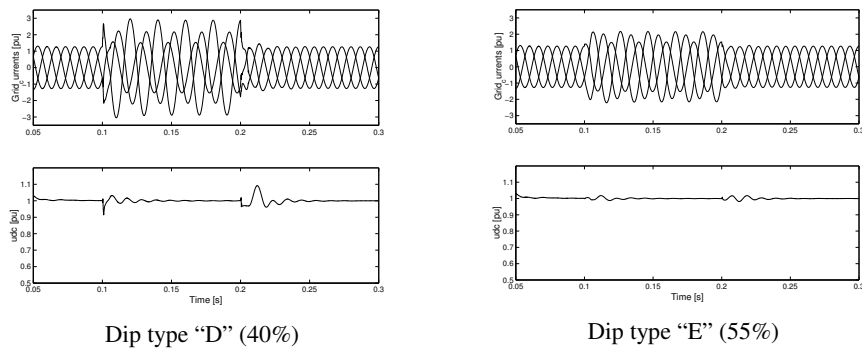
Since the DC side of the converter is not supplying the oscillating powers anymore, the DC voltage is significantly smoothed out, apart from the transients at the beginning and end of the dip, which are mainly due to the inherited delay in the sequence detection technique. The currents are still almost the same as in the previous case. A comparison between the two cases, for the dip magnitudes shown in Table 2-5, considering the maximum grid current and DC voltage ripples is shown in Table 2-6. Note that the DC voltage ripples are considered in the middle of the dip. From the table, it can be noticed that the DC ripples are significantly minimized while the maximum grid currents are slightly changed.



**Fig. 2.44 Voltage dip type “A” with 70% magnitude: grid currents (top) and DC voltage (bottom) for case 4.**



**Fig. 2.45 Grid currents and DC link voltage for dip types “B” and “C” (case 4).**



**Fig. 2.46 Grid currents and DC link voltage for dip types “D” and “E” (case 4).**

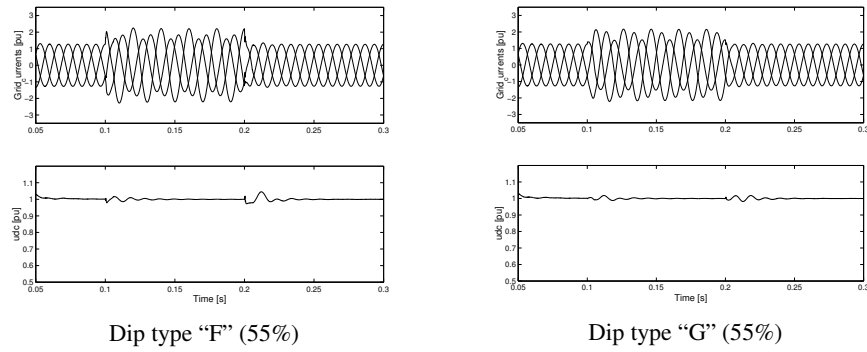


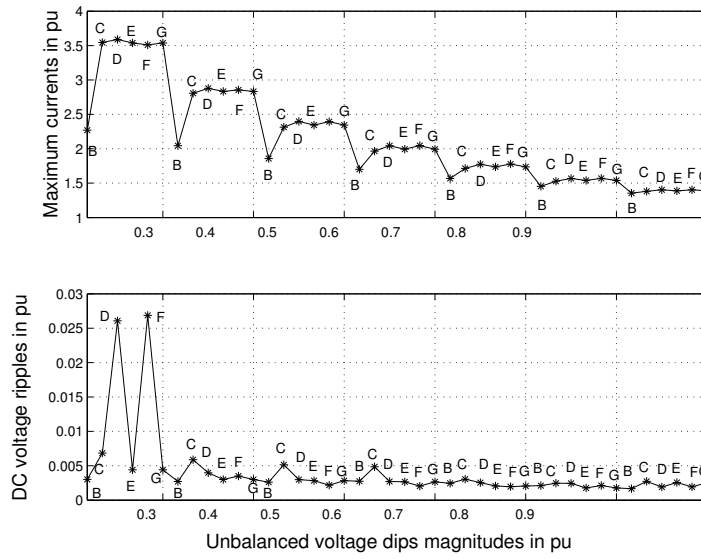
Fig. 2.47 Grid currents and DC link voltage for dip types "F" and "G" (case 4).

Table 2-6 Comparison between case 2 and case 4 considering maximum grid current and DC voltage ripples.

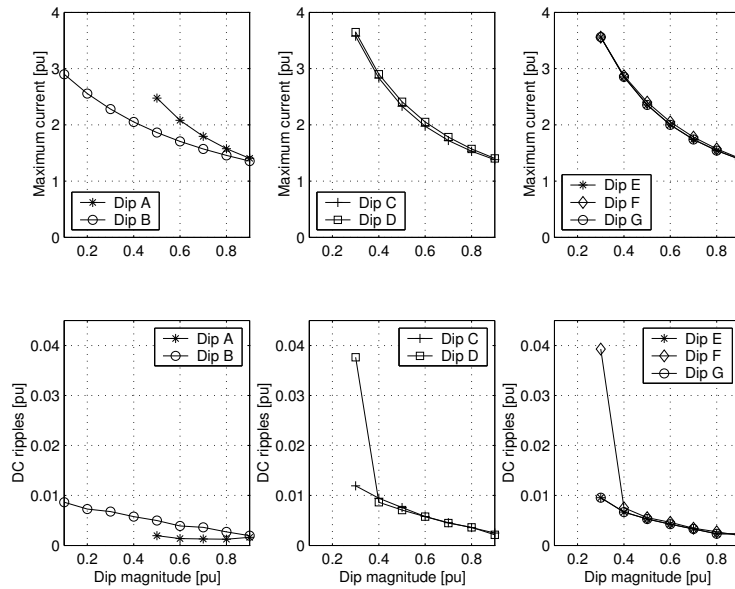
| Dip type | Case 2           |                   |                         | Case 4            |                         |
|----------|------------------|-------------------|-------------------------|-------------------|-------------------------|
|          | $V_{dip}$<br>[%] | $I_{max}$<br>[pu] | $\Delta U_{dc}$<br>[pu] | $I_{max}$<br>[pu] | $\Delta U_{dc}$<br>[pu] |
| A        | 70               | 1.7959            | 0.0016                  | 1.7949            | 0.00128                 |
| B        | 10               | 2.9719            | 0.2011                  | 2.9               | 0.0086                  |
| C        | 40               | 2.7172            | 0.2017                  | 2.832             | 0.0094                  |
| D        | 40               | 2.9719            | 0.2011                  | 2.9               | 0.0086                  |
| E        | 55               | 2.1077            | 0.0794                  | 2.1631            | 0.0047                  |
| F        | 55               | 2.2362            | 0.07788                 | 2.2155            | 0.0049                  |
| G        | 55               | 2.1077            | 0.794                   | 2.1631            | 0.0047                  |

The effect of all types of dips, with various magnitudes, on the maximum grid current and DC voltage ripples is represented in Fig. 2.48 and Fig. 2.49. Figure 2.50 demonstrates more the modification in the maximum current amplitude and DC-link voltage ripples when generating the current references using *case 4* compared to *case 2*. The maximum current the converter switches should be able to hold is reduced to 3.65 p.u., which happens at 30% dip type "D". The maximum DC voltage ripple is just about 2.5% peak-to-peak and it occurs at 30% magnitude of dip type "F". This means that the required rating of the converter system is reduced in *case 4* and also the performance of the system is improved compared to *case 2*.

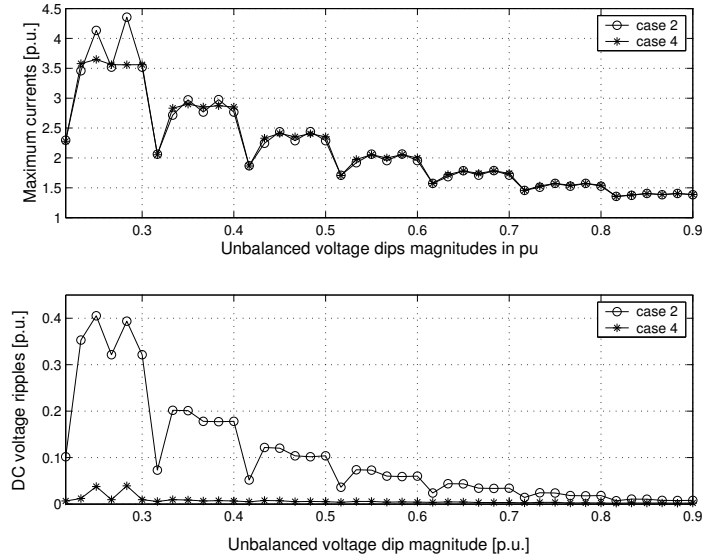




**Fig. 2.48** Maximum grid currents and DC voltage ripples for different unbalanced dip types and magnitudes between 0.3 and 0.9 for case 4.



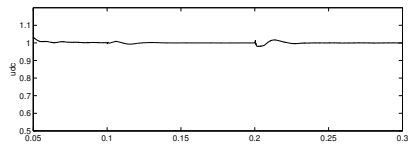
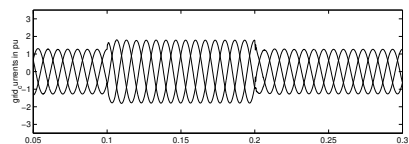
**Fig. 2.49** Maximum grid current (upper plots) and DC voltage ripple (lower plots).



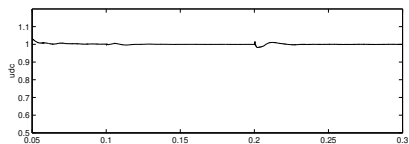
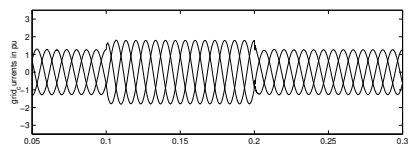
**Fig. 2.50** Maximum grid currents (top) and DC voltage ripples (bottom) for unbalanced dip types and magnitudes from 0.3 to 0.9 for case 2 (circle marked) and case 4 (asterisk marked).

### 2.6.2 Dips with phase angle jump

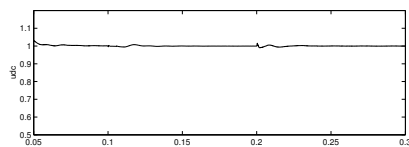
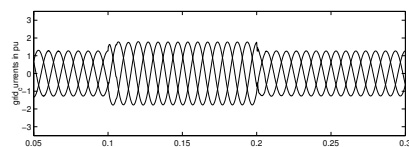
The DVCC has proven to enhance the performance, regarding maximum grid currents and DC voltage ripples, using the current references described in *case 4*. Hence, it is further examined considering dips with phase angle jump. The five dip types obtained due to using a D/Y transformer (Fig. 1.3), which are “A”, “C”, “D”, “F” and “G”, are considered with the same magnitudes reported in Table 2-5. The four values of the impedance angle  $\alpha$  specified in [17], which are  $10^\circ$ ,  $0^\circ$ ,  $-20^\circ$  and  $-60^\circ$ , are applied. Dip type “A” of magnitude 70% is represented in Fig. 2.51, while 40% dip types “C” and “D” and 55% dip types “F” and “G” are presented in Fig. 2.52, Fig. 2.53, Fig. 2.54, and Fig. 2.55 respectively. It seems that for these specific magnitudes the performance of the system, considering maximum grid currents and DC voltage ripples, is not much affected using different impedance angles. Only the transient overshoot and settling time in the DC voltage ripples is bigger in case of  $\alpha = -60^\circ$ .



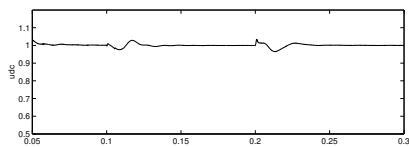
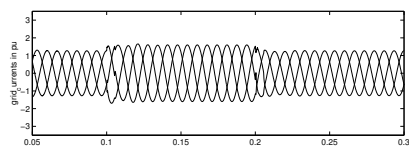
$\alpha = 10^\circ$



$\alpha = 0^\circ$

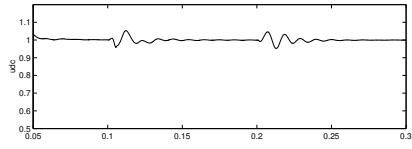
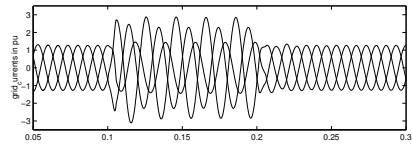


$\alpha = -20^\circ$

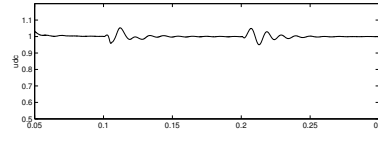
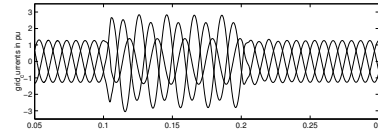


$\alpha = -60^\circ$

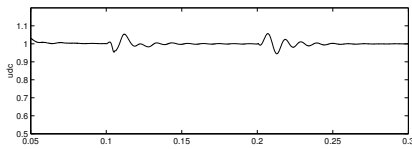
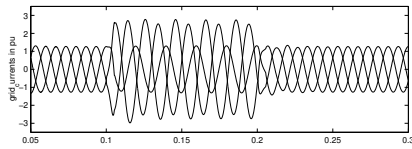
**Fig. 2.51** Grid currents and DC link voltage for 70% dip type “A” with different impedance angles.



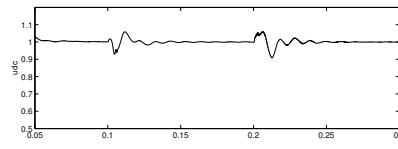
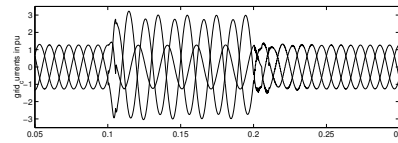
$\alpha = 10^\circ$



$\alpha = 0^\circ$

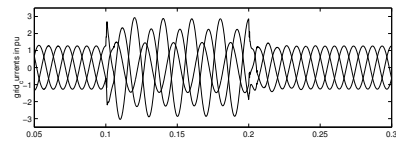


$\alpha = -20^\circ$

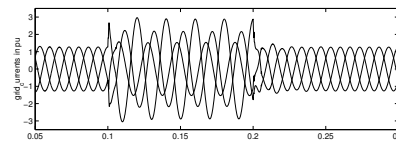


$\alpha = -60^\circ$

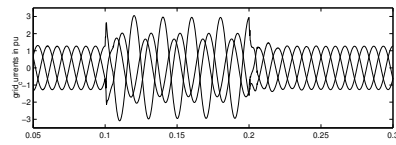
**Fig. 2.52** Grid currents and DC link voltage for 40% dip type “C” with different impedance angles.



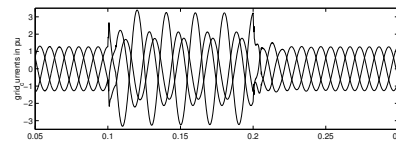
$\alpha = 10^\circ$



$\alpha = 0$

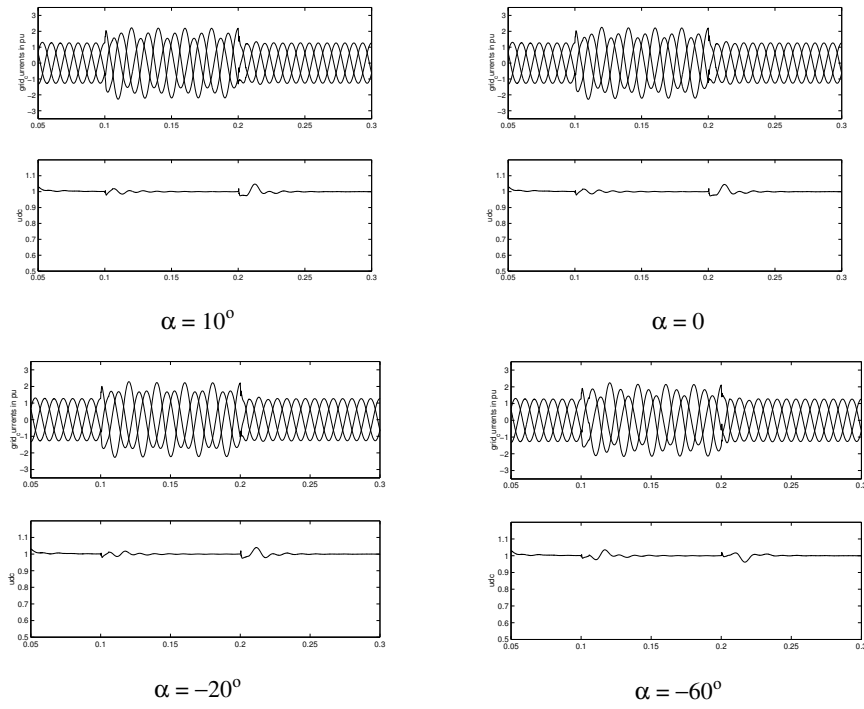


$\alpha = -20^\circ$

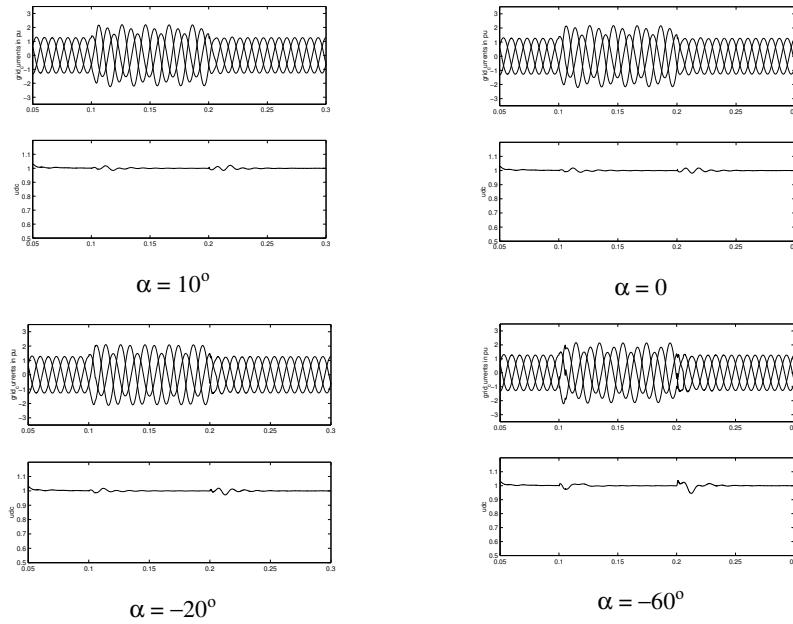


$\alpha = -60^\circ$

**Fig. 2.53** Grid currents and DC link voltage for 40% dip type “D” with different impedance angles.

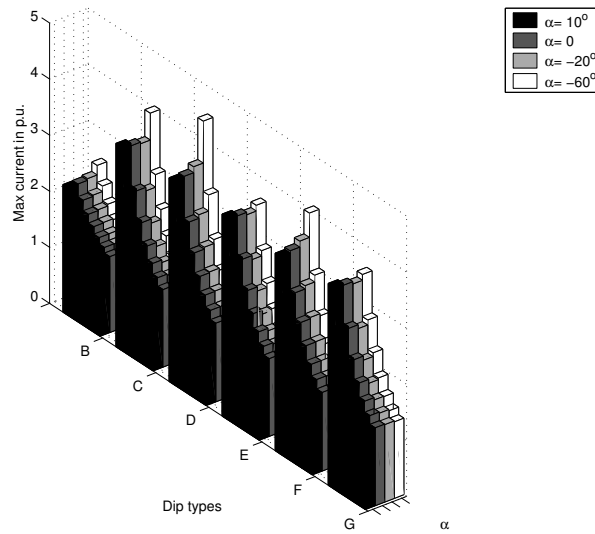


**Fig. 2.54** Grid currents and DC link voltage for 55% dip type “F” with different impedance angles.



**Fig. 2.55** Grid currents and DC link voltage for 55% dip type “G” with different impedance angles.

To have a better overview of the effect of dips with phase angle jump over the maximum currents, the maximum currents for different dip magnitudes and impedance angles are plotted in Fig. 2.56 for the unbalanced dips. The figure shows that the phase angle jump affects the maximum grid currents more in case of smaller dip magnitudes. Differences are very small for  $\alpha = 10^\circ$  and  $\alpha = -20^\circ$  while they seem to be significant when  $\alpha = -60^\circ$ . In that case the maximum current, with 30% magnitude of dip type “D”, is equal to 4.5 p.u. If the converter valves are designed considering the case of zero phase angle jump, they will be able to handle only 3.65 p.u. current as mentioned previously. Hence, in case of a voltage dip with phase angle jump the valves might be destroyed.



**Fig. 2.56 Effect of phase angle jump on the amplitude of phase currents for different unbalanced dips (for each type, dip magnitude varies from 30% to 90% going from left to right).**

## 2.7 Design equations for converter switches

At the distribution level, the VSC mostly utilizes isolated gate bipolar transistors (IGBT's). An IGBT is easy to turn on and off and has low conduction and switching losses. The ratings of a single IGBT can be up to 1.2 kA and 3.3 kV. It has good switching capability (up to 100 kHz), but for very high power devices and applications the frequency is limited to several kHz. On the other hand, the main drawback is poor overcurrent capability, i.e. it cannot withstand more than the peak current it is designed for, even for a short period of time.

In order to calculate the required current rating of the VSC valves to ride through voltage dips at the grid, the maximum current has been calculated for unbalanced faults. Equation (2-65) has been used to calculate the current components in  $dqp$ - and  $dqn$ -frame assuming no losses. Furthermore, the phase angle jump is assumed to be zero for simplicity, which result in zero  $qp$ - and  $qn$ -components of the grid voltage according to Table 1-3. The grid current is then described as:



$$\begin{bmatrix} i_{dp} \\ i_{qp} \\ i_{dn} \\ i_{qn} \end{bmatrix} = \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \begin{bmatrix} e_{dp} \\ 0 \\ -e_{dn} \\ 0 \end{bmatrix} \quad (2-70)$$

where  $P_{dc}$  is the nominal input DC power and  $K$  is the ratio of the input power actually delivered to the DC link. The current components are then transformed back into three phase quantities in positive and negative- sequence frames and then into three-phase current using Park transformation.

In case of single phase faults (dip types “B” and “D”), the maximum phase current (phase  $a$ ) is calculated as follows:

$$I_{\max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp} + e_{dn}} \quad (2-71)$$

while for two phase faults (dip types “C”, “E”, “F”, “G”) , the maximum phase current (phase  $b$ ) is calculated as follows:

$$I_{\max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{e_{dp}^2 - e_{dn}^2} \sqrt{\frac{1}{4} (e_{dp} - e_{dn})^2 + \frac{3}{4} (e_{dp} + e_{dn})^2} \quad (2-72)$$

For three phase faults (dip type “A”), the maximum phase current is:

$$I_{\max} = \sqrt{\frac{2}{3}} \cdot \frac{K P_{dc}}{E \times V_{dip}} \quad (2-73)$$

The values of  $e_{dp}$  and  $e_{dn}$ , which are the positive and negative sequence of the  $d$ -component of the grid voltage, are calculated using Table 1-3 for different voltage dips (with  $E$  is the phase-to-phase RMS grid voltage,  $V_{dip}$  is the dip magnitude, and  $\psi$  is the phase-angle jump). Note that since the dips have zero phase-angle jump, the  $d$ -components correspond to the magnitudes of their sequence voltages. A comparison between the calculated current values and simulated ones has been performed for all dip types, in order to verify the analytical equations, and the results are shown in Fig. 2.57 to Fig. 2.63. It is worth mentioning that the simulated values are obtained using *case 2*, since that case generally induces higher currents.

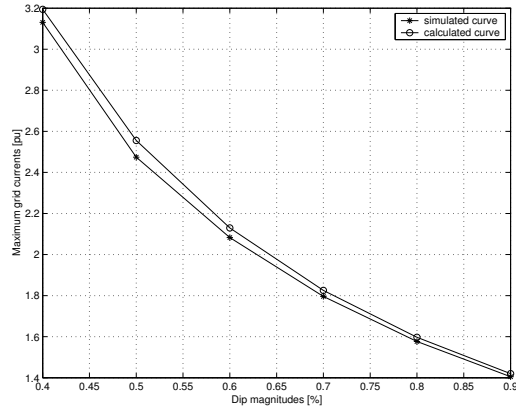


Fig. 2.57 Maximum currents for dip type “A”: simulated (asterisk marked) and calculated (circle marked).

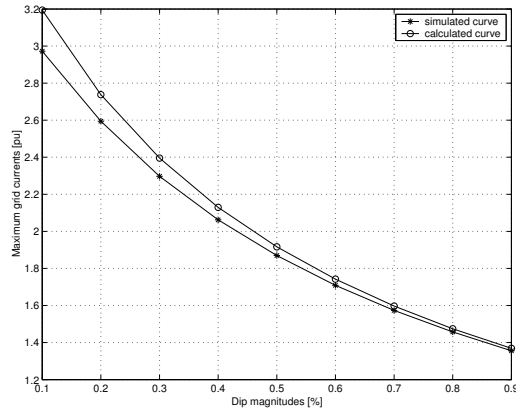
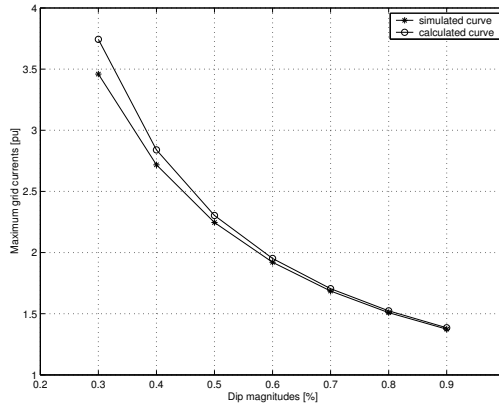
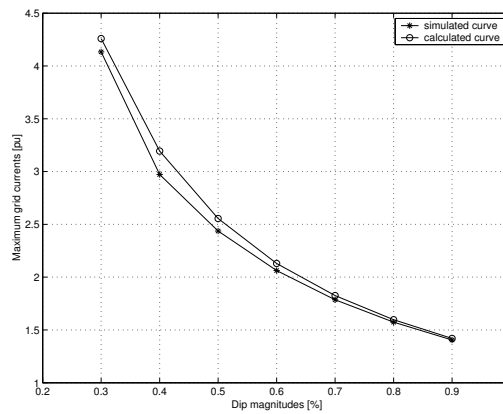


Fig. 2.58 Maximum current for dip type “B”: simulated (asterisk marked) and calculated (circle marked).



**Fig. 2.59** Maximum current for dip type “C”: simulated (asterisk marked) and calculated (circle marked).



**Fig. 2.60** Maximum current for dip type “D”: simulated (asterisk marked) and calculated (circle marked).

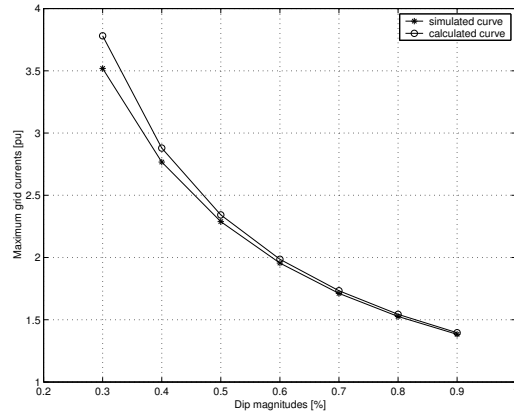


Fig. 2.61 Maximum current for dip type “E”: simulated (asterisk marked) and calculated (circle marked).

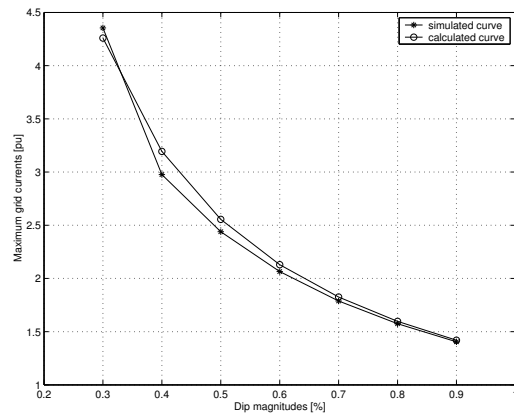
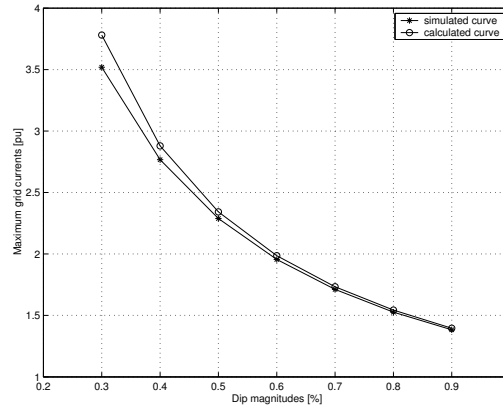


Fig. 2.62 Maximum current for dip type “F”: simulated (asterisk marked) and calculated (circle marked).



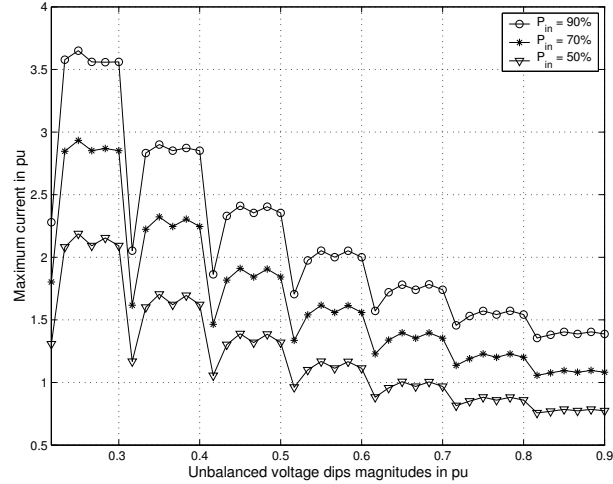
**Fig. 2.63 Maximum current for dip type “G”: simulated (asterisk marked) and calculated (circle marked).**

From the above figures, Fig. 2.57 to Fig. 2.63, it can be concluded that there is an over-estimation at the calculated curves but generally they show the same trend as the simulated ones. The maximum error occurs at 10% dip type “B” and equals 7.48%. This over-estimation is probably due to the accumulated error through the different parts of the simulated system and most likely due to not considering the power dissipated in the filter  $\Delta P$  in the calculated values. However, the over-estimation is preferred in the designing stage because it gives a safety margin to the design values.

The maximum calculated current, which is 4.26 p.u., occurs at 30% magnitude of dip type “D”. Although being over-estimated with respect to the simulated value (Fig. 2.60), it is still less than the simulated case with phase angle jump (at  $\alpha = -60^\circ$  for 30% magnitude of dip type “D”). This means that the case of  $\alpha = -60^\circ$  should be specifically considered if ride through capability for underground cable faults is desired.

## **2.8 Effect of decreasing input power**

From (2-71), (2-72), and (2-73), it is obvious that there is a direct proportionality between the maximum current and the value of the actual input power. In other words, if the input power is lowered by the ratio  $K$ , the maximum value of the current will also be lowered by the same ratio. Simulation results plotted in Fig. 2.64 represent the effect of lowering the input power  $P_{in}$  for different dip types and magnitudes.



**Fig. 2.64 Effect of lowering  $P_{in}$  on maximum grid currents for unbalanced voltage dips with magnitudes from 0.3 p.u. to 0.9 p.u. in steps of 0.1.**

Therefore, if the converter switches have to be rated to ride through all dips with 30% minimum magnitude, the current rating can be decreased from about 3.5 p.u. to 3 p.u., if the input power is decreased from 90% to 70% of nominal value.

One way to optimise the design of the switches is thus to minimize the currents during the fault period, which could be established by temporarily decreasing the input power to the system (decreasing  $K$  in (2-71), (2-72), and (2-73)) during the fault. If this is possible or not depends on the controllability and the response time of the source connected to the DC-link. However, it seems difficult to imagine a realistic case in which the input power could be decreased so quickly. On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Then, to optimize the design it is possible to consider a lower value of the input power, which is delivered by the turbine, for a certain period of time. This means accepting a certain risk that the converter (thus the turbine) might still trip, but can lead to greatly reducing the size of the converter. This is investigated numerically by the following case study.

## 2.9 Case study

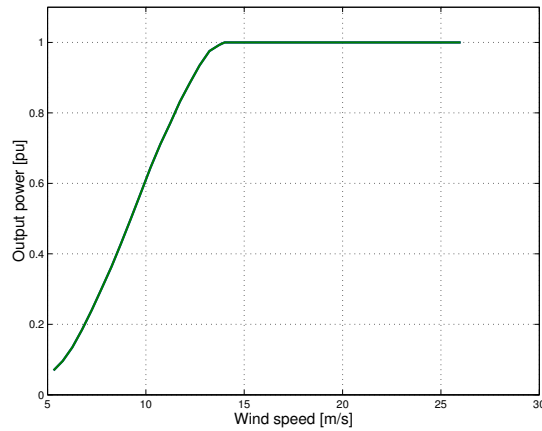
The system in Fig. 1.2 is to be implemented for a wind turbine with rated power 180 kW, speed  $\omega_s = 42$  rpm, gearbox ratio 23.75, and radius of the blades  $R = 11.5$  m. The mechanical efficiency of a turbine  $C_p$ , which measures how efficiently the turbine converts the energy in the wind to electricity, has its largest value of 44% at a wind speed of around 9 m/s [55].

The conversion from wind speed to mechanical power is described by:

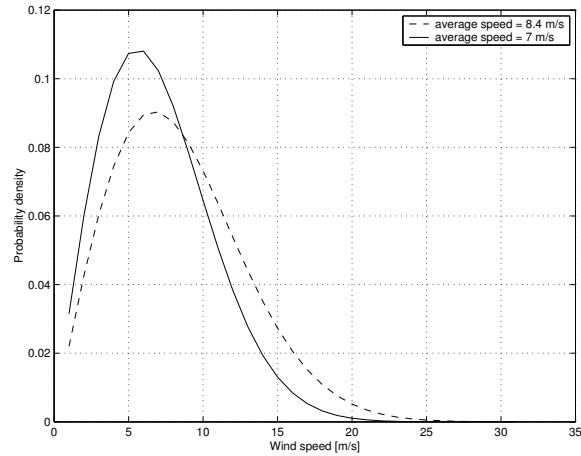
$$P = \frac{\pi \rho \omega_S^3 R^2}{2} C_P(\omega_S) \quad (2-74)$$

where  $\rho$  is the air density, which is set to 1.225 kg/m<sup>3</sup>. Using the given data, the power curve for the turbine is obtained, as in Fig. 2.65. The power is expressed in per unit of the rated power of the turbine. The efficiency of the electrical generator is set to 100%.

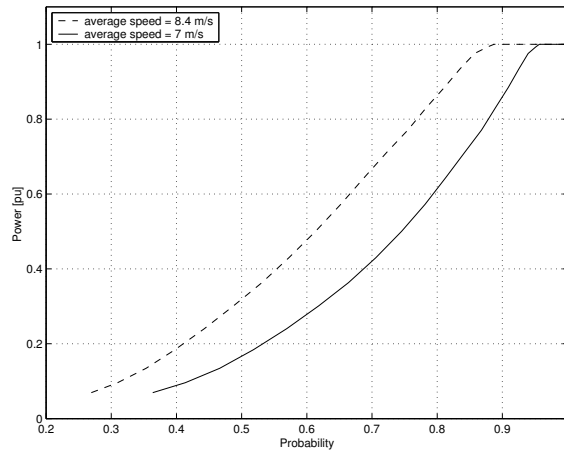
The wind variation of a typical site can be described using the Weibull distribution, as displayed in Fig. 2.66, which shows the probability density for the wind speed at two sites with average speeds of 8.4 m/s and 7 m/s, respectively. The shape parameter for the two curves is set to 2 [56]. By integrating the probability density in Fig. 2.66 and combining it with the power curve in Fig. 2.65, the curve in Fig. 2.67 is obtained. This represents the probability that a given maximum output power is produced.



**Fig. 2.65 Electrical power output of turbine versus wind speed.**



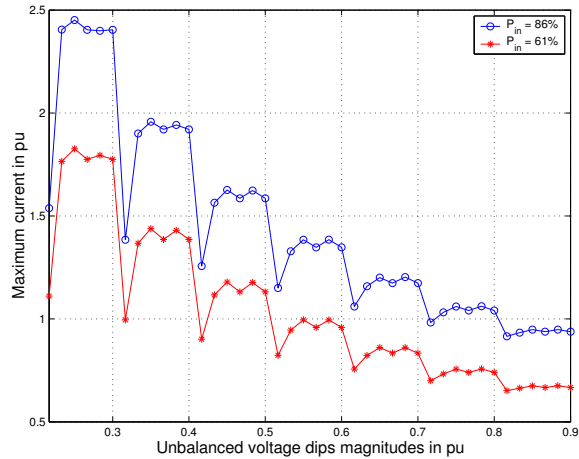
**Fig. 2.66** Weibull distribution for a site with average wind speed 8.4 m/s (dashed) and 7 m/s (solid).



**Fig. 2.67** Probability of output power produced by wind turbine.

It is assumed that it is required to keep the system on line for 80% of the time during a year. This means that the maximum power that can be obtained statistically is about 0.86 p.u. for a site with average wind speed of 8.4 m/s. For a site with average wind speed of 7 m/s, a maximum power of 0.61 p.u. is obtained. The maximum VSC currents for these two power levels for all unbalanced voltage dips are plotted in Fig. 2.68.





**Fig. 2.68 Maximum grid current for unbalanced voltage dips with magnitudes 0.3 to 0.9 p.u. with VSC input power  $P_{in} = 86\%$  (circle marked) and 61% (asterisk marked).**

From Fig. 2.68 it is concluded that the converter will stay in operation in case of dips with magnitude higher than 80% for the first site and 50% for the second site. If the converter must ride through all dips starting with magnitude higher than 30%, it must be rated 2.4 p.u. for the first site and about 1.8 p.u. for the second site. The same figures can be calculated using the design equations derived previously.

By considering the statistic character of the wind output power, it becomes clear that even without oversizing the converter interface, some limited ride-through capability is ensured. However, if a higher ride-through capability is required, some overrating of the VSC will be necessary. This can be limited by accepting a certain risk of tripping (in the given example, the risk would be 20%).

## 2.10 Conclusions

In this chapter, the main system under consideration is presented. A simple PI vector current controller (VCC) is implemented and its transient performance is examined through simulation. Some modifications are suggested and implemented to achieve satisfactory operation of the controller concerning computational time delay, saturation of reference voltage and integrator windup. Then the controller is examined in case of voltage dips, which is the main concern in the thesis. A simple PI-controller for the DC-link voltage regulator has been suggested. The output of this controller is a DC current signal, which is used to modify the current references in such a way as to force the DC voltage to follow its reference. Current harmonics appear during faults due to the appearance of negative sequence components caused by the unbalanced grid voltage. DC-link voltage ripple is also significant.

The dual vector current controller (DVCC) is introduced in order to improve the performance of the VCC in case of grid voltage imbalance. Two methods are demonstrated to calculate the current references used by the controller, referred to as *case 2* and *case 4*. The positive and negative current references, in  $dq$ -coordinates, are derived from the instantaneous power flow between the grid and the VSC. This power flow equation contains second-order harmonic power components, called oscillating powers, due to the imbalance in the grid voltages. In *case 2*, these oscillating powers are forced to flow from the converter side into the filter. In *case 4*, they are forced to flow from the AC grid side into the filter.

Simulation results when implementing the DVCC using Matlab/Simulink are presented. Different simulations have been made for the two reference current generation algorithms. It has been shown that the second case, which is *case 4*, improves the system performance. The DC voltage ripples are considerably smoothed out. They no longer contain 100 Hz oscillations as in *case 2*. The DC voltage is practically constant apart from the transient at the start and end of the voltage dip. The maximum grid current, which the converter switches should carry to ride through the dip, is slightly decreased.

The effect of phase angle jump is also examined considering only *case 4*. It is concluded that the phase angle jump has more effect on voltage dips with smaller magnitudes, and the worst case occurs when the impedance angle  $\alpha = -60^\circ$ . This effect is more significant for “C” and “D” dip types. The maximum current occurs with 30% magnitude of dip type “D” and is equal to 4.5 p.u., i.e. 25% more than its value in case of zero phase angle jump. So the effect of phase angle jump should be considered when designing the converter switches to ride through all dips.

In order to calculate the required current ratings of the converter switches to ride-through different voltage dips in the grid, design equations have been derived in case of zero phase angle jump. These equations give slightly over-estimated values since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power is examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period, which could be a way to decrease the ratings of the converter valves. This, however, would require that the input power to the DC bus be reduced very quickly. However, it seems difficult to imagine a realistic case in which the input power could be decreased so quickly. On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine produces full power might be very low, as the turbine often runs at much lower power. Hence, by considering the statistic character of the wind output power, it is clear that even without oversizing the converter interface, some limited ride-through capability is ensured. However, if a higher ride-through capability is required, some overrating of the VSC will be necessary. This has been investigated through a case study.

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## 3. Grid-Connected Voltage Source Converter with LCL-filter Interface

### 3.1 Introduction

Due to the PWM switching of voltage source converters (VSCs), the grid currents contain high-frequency harmonic components. These components can cause improper operation of other EMI sensitive loads on the grid [35]-[42]. Inserting LCL-filter between the grid and the VSC eliminates high frequency harmonics even with lower switching frequency [33]-[43]. Besides, smaller inductances can be used which improve the transient performance of the VSC [40].

Since the LCL-filter is utilized on the grid side, instability problems could occur at the resonance frequency of the filter. Damping methods are extensively addressed in literature. In [36] a resistance is used in series with the filter capacitor to passively damp the resonance. This resistance increases the system losses and decreases the efficiency of the filter. Instead, methods to actively damp the resonance are adopted as in [34], [37], and [38]. In [34], a converter current controller is designed neglecting the filter capacitance and the active current command is generated from a DC voltage PI controller. A comparison between passive damping and active damping using a lead compensator has been carried out based on  $z$ -plane root locus and Bode plots. The active damping successfully reduces the resonance peak below 0 dB, ensuring the system stability. However it increases the algorithm complexity of the controller. In [38], a lead-lag compensator is applied in the feedback from the capacitor voltage. The converter currents and voltages are sensed and a phase shift is used in the PLL to adjust the angle for the  $dq$ -frame. Moreover, a comparison between none-damped, passively-damped and proposed actively-damped systems is carried out using Bode plots. It has been concluded that the active damping reduces the resonant peak as effective as the passive damping. In [37], three cascaded controllers are used with reference grid current generated from a DC voltage controller. The converter current and capacitor voltage are predicted. Moreover, two active resistances virtually connected in series with the filter inductor resistances are considered in the controller dead-beat gains. However, the use of these resistances is not justified. In [35], and [39] controllers with no damping are proposed. This has been accomplished in [35] by controlling the grid current instead of the converter current and the proper choice of the filter parameters. In [39], two control loops are used: an outer current control loop and an inner capacitor voltage control loop. The latter is used to stabilize the controller and in the same time damp the resonance.

Other problems arising in the grid side are also studied in literature. Changes in different system parameters due to inaccurate measurements or any other variations (such as grid voltage harmonics) are studied in [33], and [37]. The effect of the harmonics in the grid voltage is addressed in [37], and [39]. Grid voltage imbalance is studied in [37]. Moreover, different methods are used for optimal design of LCL-filter parameters as in [34], [41], and [42].

In chapter 2 an extensive study has been carried out in order to investigate the effect of grid voltage imbalance on the VSC system when it is connected to the grid through an L-filter. The dual vector current controller (DVCC) has proved to perform adequately with respect to the grid current and DC voltage. This controller is also presented in case of an LCL-filter interface in [37]. However, the DC voltage is considered constant, hence the reference current commands are given as constant values. Moreover, the controller is tested only in one case of imbalance and no further analysis is presented.

In this chapter, the VSC system connected to the grid through LCL-filter is considered. The LCL-filter is designed and modelled. The effect of adding a resistance to the filter capacitor is discussed. Then, the derivation of the vector current controller (VCC) is presented and its dynamical response is examined. The performance in case of current steps and voltage imbalance is tested for the system with stiff DC link voltage and with regulated DC link voltage. To improve the performance in case of unbalanced voltage dips at the grid, the DVCC is implemented. At the end of the chapter, the robustness of the controller in the sense of filter parameters variation is tested.

### 3.2 LCL-filter design

The schematic diagram of the power circuit of the VSC connected to the grid through LCL-filter is shown in Fig. 3.1.

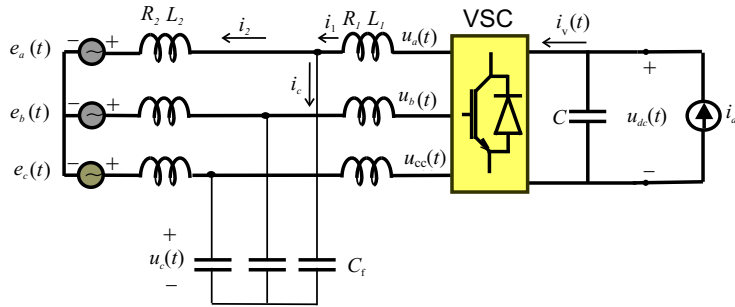


Fig. 3.1 Schematic diagram of the power circuit of VSC connected to the grid through LCL-filter.

Assuming the grid voltage as a disturbance and neglecting  $R_1$  and  $R_2$ . The transfer function of the filter is then  $I_2(s)/U(s)$ , and is calculated as follows:

$$\frac{U(s)}{I_1(s)} = \frac{L_2/C_f}{\left(sL_2 + \frac{1}{sC_f}\right)} + sL_1 = \frac{sL_2 + 1/sC_f}{s^2L_1L_2 + \frac{(L_1 + L_2)}{C_f}} \quad (3-1)$$

Using the current divider rule:

$$I_2(s) = I_1(s) \frac{1/sC_f}{sL_2 + \frac{1}{sC_f}} \quad (3-2)$$

It follows that:

$$I_1(s) = I_2(s) \cdot (s^2 L_2 C_f + 1) \quad (3-3)$$

Then the transfer function becomes:

$$\frac{I_2(s)}{U(s)} = \frac{1/C_f L_1 L_2}{s \left( s^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right)} \quad (3-4)$$

The resonant frequency is then:

$$f_{\text{res}} = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \quad (3-5)$$

The filter parameters are chosen such that the following conditions are satisfied [36], [41]:

- Neglecting the filter resistances, the voltage drop across the inductances should be limited to 10% during nominal operation, which agrees with the previous design criteria for L-filter;
- The grid side inductance is a fraction of the converter side inductance, since the latter is responsible for the attenuation of most of the switching ripple;
- The capacitive value is limited by the decrease of the power factor at rated power in case of idle operation of the VSC (it will be considered as less or equal 10%);
- The resonance frequency is in the range between ten times the fundamental frequency and one half the switching frequency;
- The IEC 1000-3-4 regulation states that current harmonics above 33<sup>rd</sup> should be less than 0.6% of the nominal current;
- The resistances are taken as 10% of the value of the corresponding inductances.

According to these conditions the following equations can be used:

$$L_1 + L_2 = 0.1 \text{ p.u.} \quad (3-6)$$

$$L_2 = r \cdot L_1 \quad (3-7)$$

where  $r$  is the ratio between the inductance on the grid side to the inductance on the converter side, which is less than 1.

$$C_f \leq 0.1 \text{ p.u.} \quad (3-8)$$

$$500 \text{ Hz} < f_{\text{res}} < 1250 \text{ Hz} \quad (\text{for sampling frequency of 5kHz}) \quad (3-9)$$

From (3-4), the gain of the system at the  $h$  harmonic is expressed as:

$$|G(jh\omega)| = \frac{1/C_f L_1 L_2}{\left| jh\omega \left( (jh\omega)^2 + \frac{L_1 + L_2}{L_1 L_2 C_f} \right) \right|} \leq 0.006 \quad (3-10)$$

Equations (3-9) and (3-10) are used as check up conditions. Using a capacitance value of 0.05 p.u., (3-9) is not satisfied for different inductance ratios ( $r$ ), as shown in Fig. 3.2. Increasing the capacitance value to 0.1 p.u., a value of  $r = 0.4$  has been chosen to satisfy all conditions (see Fig. 3.3 and Fig. 3.4). The LCL filter parameters are then calculated as reported in Table 3-1.

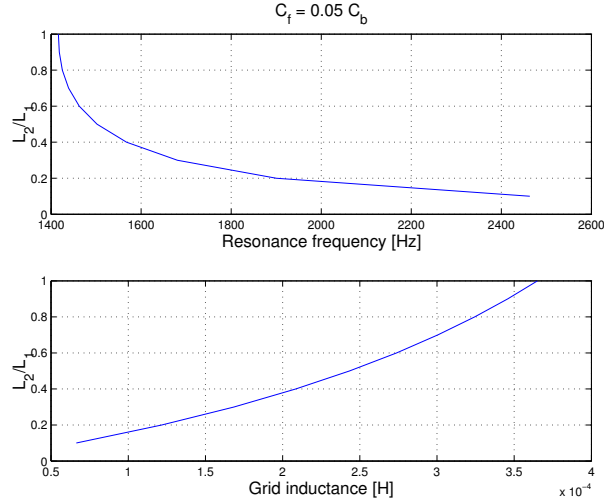


Fig. 3.2 Relation between  $r$  and the resonance frequency (upper), and  $r$  and the grid inductance (lower) for a filter capacitance of 5% of the base value.

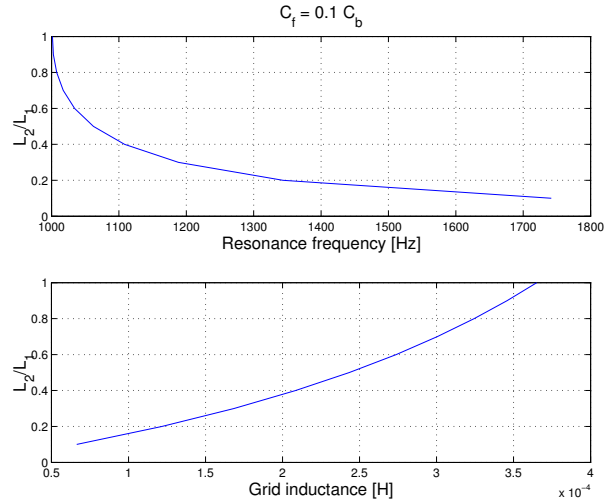
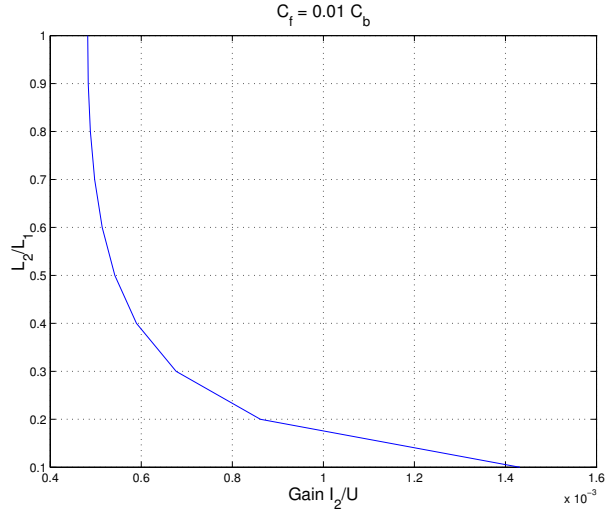


Fig. 3.3 Relation between  $r$  and the resonance frequency (upper), and  $r$  and the grid inductance (lower) for a filter capacitance of 10% of the base value.



**Fig. 3.4** Relation between  $r$  and the gain filter  $I_2/U$ .

**Table 3-1** LCL-Filter parameters.

| Parameter | p.u.      | Actual         |
|-----------|-----------|----------------|
| $L_1$     | 0.071     | 0.52 mH        |
| $R_1$     | $0.1 L_1$ | 1.6 m $\Omega$ |
| $L_2$     | 0.027     | 0.2 mH         |
| $R_2$     | $0.1 L_2$ | 0.6 m $\Omega$ |
| $C_f$     | 0.1       | 137.83 $\mu$ F |

Note that the base impedance is  $Z_{\text{base}}=2.3\Omega$  (as calculated in *Appendix B*).

### 3.3 LCL-filter model

After designing the LCL-filter, a model should be developed in order to analyze the filter performance.

Applying KVL to the LCL-filter circuit (shown in Fig. 3.1), the following equations are obtained (in single phase notation):

$$\frac{di_1}{dt} = \frac{-R_1}{L_1} i_1 - \frac{1}{L_1} u_c + \frac{1}{L_1} u \quad (3-11)$$

$$\frac{di_2}{dt} = \frac{-R_2}{L_2} i_2 + \frac{1}{L_2} u_c - \frac{1}{L_2} e \quad (3-12)$$

Applying KCL at the capacitor connection node, the following equation is obtained (in single phase notation):

$$\frac{du_c}{dt} = \frac{1}{C_f} i_1 - \frac{1}{C_f} i_2 \quad (3-13)$$

Transforming (3-11) through (3-13) into  $dq$ -frame, which is synchronized with the grid voltage as illustrated in Appendix A, and arranging them in the state-space form:

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \quad (3-14)$$

where:

$$x = [i_{1d} \quad i_{1q} \quad i_{2d} \quad i_{2q} \quad u_{cd} \quad u_{cq}]^T \quad (3-15)$$

$$u = [e_d \quad e_q \quad u_d \quad u_q]^T \quad (3-16)$$

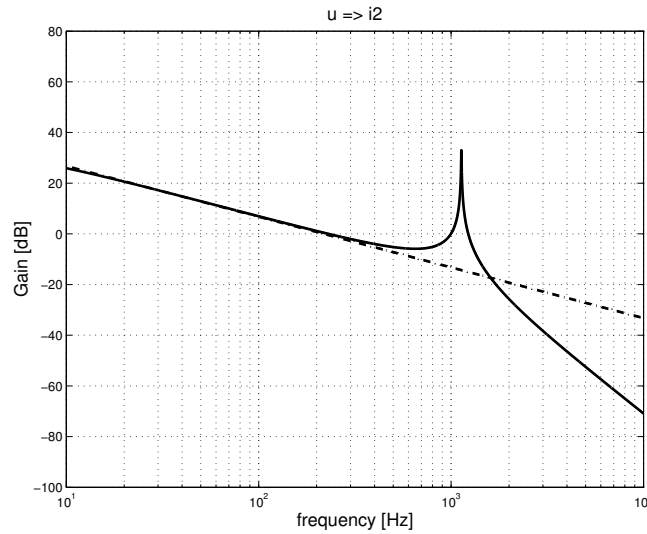
$$A = \begin{bmatrix} \frac{-R_1}{L_1} & \omega & 0 & 0 & \frac{-1}{L_1} & 0 \\ -\omega & \frac{-R_1}{L_1} & 0 & 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-R_2}{L_2} & \omega & \frac{1}{L_2} & 0 \\ 0 & 0 & -\omega & \frac{-R_2}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_f} & 0 & \frac{-1}{C_f} & 0 & 0 & \omega \\ 0 & \frac{1}{C_f} & 0 & \frac{-1}{C_f} & -\omega & 0 \end{bmatrix} \quad (3-17)$$

$$B = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} \\ \frac{-1}{L_2} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (3-18)$$

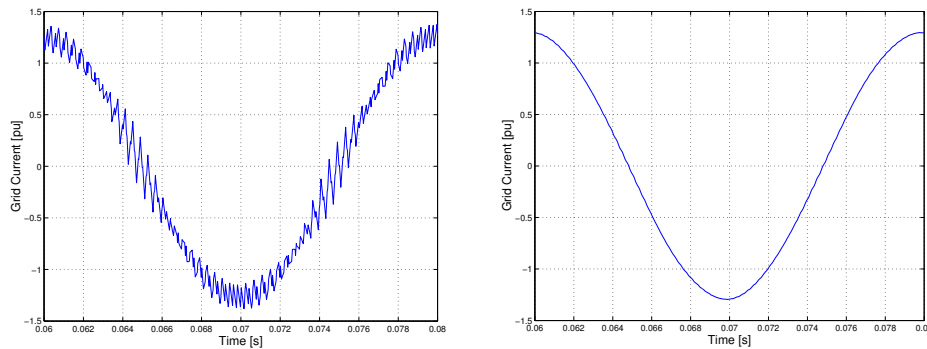
$C$  is the identity matrix of dimension  $6 \times 6$ , and  $y$  is the output vector which in this case is identical to the state vector  $x$ .



The frequency response from the converter voltage  $u$  to the grid current  $i_2$  is shown in Fig. 3.5 for both LCL-filter (parameters are in Table 3-1) and L-filter (with parameters: 0.73 mH and 23 m $\Omega$ ). It is shown that both filters have the same response at low frequencies, while the LCL-filter has better performance at high frequencies since the harmonic attenuation increases to 60 dB/decade for LCL-filter compared to 20 dB/decade for the L-filter. This is more visualised looking into the grid current in case of implementing each filter (see Fig. 3.6).



**Fig. 3.5** Frequency response from converter voltage to grid current for L-filter (dash-dotted) and LCL-filter (solid).



**Fig. 3.6** Phase current on the grid side: L-filter interface (left) and LCL-filter interface (right).

The drawback of the LCL-filter interface is its peak gain at the resonance frequency, which implies an oscillatory behaviour and consequently controller instability. This resonant peak can be damped either passively (using a resistor in series with the filter capacitor), or actively by modifying the controller algorithm.

### 3.4 Passively damped-LCL filter

Adding a damping resistance  $R_d$  in series with the filter capacitor will damp the resonant peak (as shown in Fig. 3.7). However the system losses are increased and high-frequency attenuation efficiency of the filter is decreased, as explained by the decreasing slope of the gain at higher frequencies that approaches the slope in case of L-filter. Alternatively, a method to actively damp the resonance should be developed. This is done here by the proper design of the controller, as explained by the proceeding section.

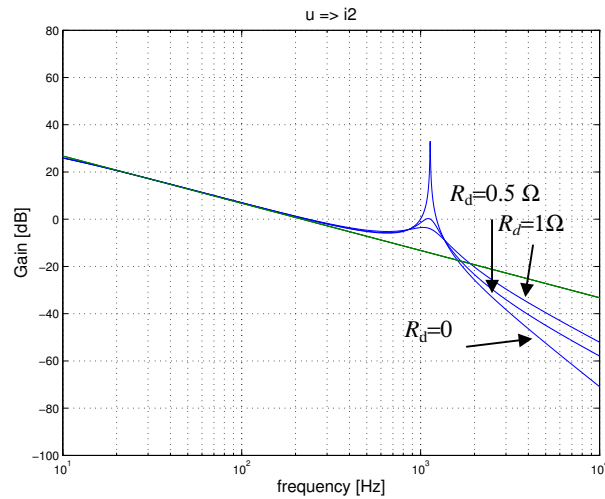


Fig. 3.7 Frequency response of LCL-filter for different values of  $R_d$ .

### 3.5 Derivation of vector current controller (VCC) for LCL-filter system

To increase the stability margin and at the same time to damp oscillations at the resonant frequency of the LCL-filter, three cascaded controllers are applied as shown in Fig. 3.8.

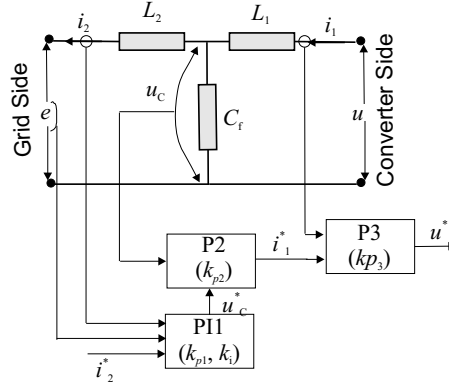


Fig. 3.8 Schematic diagram of the proposed cascaded controller.

The LCL-filter is described in the  $dq$ -frame as follows:

$$\underline{u}_{cdq} = e_{dq} + R_2 i_{2dq} + j\omega L_2 i_{2dq} + L_2 \frac{di_{2dq}}{dt} \quad (3-19)$$

$$\underline{u}_{dq} = \underline{u}_{cdq} + R_1 i_{1dq} + j\omega L_1 i_{1dq} + L_1 \frac{di_{1dq}}{dt} \quad (3-20)$$

$$i_{1dq} = i_{2dq} + j\omega C_f \underline{u}_{cdq} + C_f \frac{d\underline{u}_{cdq}}{dt} \quad (3-21)$$

Integrating over one sampling interval and dividing by  $T_s$  results in the average voltage and current during this interval. The average capacitor voltage over one sampling interval is then:

$$\frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} \underline{u}_{cdq} dt = \frac{1}{T_s} \left( \begin{array}{l} \int_{kT_s}^{(k+1)T_s} e_{dq} dt + R_2 \int_{kT_s}^{(k+1)T_s} i_{2dq} dt + \\ j\omega L_2 \int_{kT_s}^{(k+1)T_s} i_{2dq} dt + L_2 \int_{kT_s}^{(k+1)T_s} \frac{di_{2dq}}{dt} dt \end{array} \right) \quad (3-22)$$

$$\begin{aligned} \underline{u}_{cdq}(k, k+1) = & \underline{e}_{dq}(k, k+1) + R_2 \underline{i}_{2dq}(k, k+1) \\ & + j\omega L_2 \underline{i}_{2dq}(k, k+1) + L_2 \frac{\underline{i}_{2dq}(k+1) - \underline{i}_{2dq}(k)}{T_s} \end{aligned} \quad (3-23)$$

Similarly, the average converter voltage over one sampling interval will be:

$$\begin{aligned} \underline{u}_{cdq}(k, k+1) = & \underline{u}_{cdq}(k, k+1) + R_1 \underline{i}_{1dq}(k, k+1) \\ & + j\omega L_1 \underline{i}_{1dq}(k, k+1) + L_1 \frac{\underline{i}_{1dq}(k+1) - \underline{i}_{1dq}(k)}{T_s} \end{aligned} \quad (3-24)$$

The average converter current is also obtained as:

$$\underline{i}_{1dq}(k, k+1) = \underline{i}_{2dq}(k, k+1) + j\omega C_f \underline{u}_{cdq}(k, k+1) + C_f \frac{\underline{u}_{cdq}(k+1) - \underline{u}_{cdq}(k)}{T_s} \quad (3-25)$$

To obtain the controller equations, the following assumptions are set:

1. Dead-beat operation, where the actual signal equals the reference command after one sample.

$$\underline{i}_{2dq}(k+1) = \underline{i}_{2dq}^*(k) \quad (3-26)$$

$$\underline{i}_{1dq}(k+1) = \underline{i}_{1dq}^*(k) \quad (3-27)$$

$$\underline{u}_{cdq}(k+1) = \underline{u}_{cdq}^*(k) \quad (3-28)$$

2. The quantities that are required to give the desired response are equal to the reference values. This is referring to the quantities on the left-hand side of (3-23) through (3-25), and can be read as follows:

$$\underline{u}_{cdq}(k, k+1) = \underline{u}_{cdq}^*(k) \quad (3-29)$$

$$\underline{i}_{1dq}(k, k+1) = \underline{i}_{1dq}^*(k) \quad (3-30)$$

$$\underline{u}_{dq}(k, k+1) = \underline{u}_{dq}^*(k) \quad (3-31)$$

3. The average grid voltage is constant over one sample, since the sampling frequency is assumed to be several orders in magnitude faster than the grid dynamics.

$$\underline{e}_{dq}(k, k+1) = \underline{e}_{dq}(k) \quad (3-32)$$

4. The average voltage and current values over one sample are constants:

$$\underline{u}_{cdq}(k, k+1) = \underline{u}_{cdq}(k) \quad (3-33)$$

$$\underline{i}_{2dq}(k, k+1) = \underline{i}_{2dq}(k) \quad (3-34)$$

$$\hat{i}_{1dq}(k, k+1) = i_{1dq}(k) \quad (3-35)$$

5. The average current related to the resistive voltage drop is equal to half the sum of reference and actual currents, as follows:

$$\hat{i}_{1dq}(k, k+1) = \frac{i_{1dq}^*(k) + i_{1dq}(k)}{2} \quad (3-36)$$

$$\hat{i}_{2dq}(k, k+1) = \frac{i_{2dq}^*(k) + i_{2dq}(k)}{2} \quad (3-37)$$

Applying the previous assumptions, the controller equations in  $dq$ -frame, considering one sample time delay in the inner controller (P3) and integral part in the outer controller, are:

$$\underline{u}_{cdq}^*(k) = e_{dq}(k) + (R_2 + j\omega L_2) i_{2dq}(k) + kp_1 (i_{2dq}^*(k) - i_{2dq}(k)) + \underline{\Delta u}_{idq}(k) \quad (3-38)$$

$$\hat{i}_{1dq}^*(k) = i_{2dq}(k) + j\omega C_f \underline{u}_{cdq}(k) + kp_2 (\underline{u}_{cdq}^*(k) - \underline{u}_{cdq}(k)) \quad (3-39)$$

$$\underline{u}_{dq}^*(k+1) = \underline{u}_{cdq}(k) + (R_1 + j\omega L_1) \hat{i}_{1dq}(k) + kp_3 (\hat{i}_{1dq}^*(k) - \hat{i}_{1dq}(k)) \quad (3-40)$$

where the gains  $kp_1$ ,  $kp_2$ , and  $kp_3$  are fractions of the corresponding dead-beat gains,  $k_{DB1}$ ,  $k_{DB2}$ , and  $k_{DB3}$ , as explained by the following equations:

$$\begin{aligned} kp_1 &= k_1 k_{DB1} = k_1 \left( \frac{L_2}{T_s} + \frac{R_2}{2} \right) \\ kp_2 &= k_2 k_{DB2} = k_2 \left( \frac{C_f}{T_s} \right) \\ kp_3 &= k_3 k_{DB3} = k_3 \left( \frac{L_1}{T_s} + \frac{R_1}{2} \right) \end{aligned} \quad (3-41)$$

and

$$\underline{\Delta u}_{idq}(k+1) = \underline{\Delta u}_{idq}(k) + k_i (i_{2dq}^*(k) - i_{2dq}(k)) \quad (3-42)$$

where  $k_i = kp_1 \frac{T_s}{T_i}$  and  $T_i$  is the integral time constant.

Predicting the VSC current one sample ahead instead of using the delayed measured current in P3 compensates for the time delay. The estimated converter current is calculated as:

$$\begin{aligned} \hat{i}_{1dq}(k+1) = & \frac{T_s}{L_1} \left( u_{dq}^*(k) - u_{cdq}(k) \right) + \left( 1 - \frac{R_1}{L_1} - j\omega T_s \right) \hat{i}_{1dq}(k) \\ & + kp_s \left( i_{1dq}(k) - \hat{i}_{1dq}(k-1) \right) \end{aligned} \quad (3-43)$$

The integrator windup and the saturation of the reference voltage have been compensated for in the same way as explained in *Chapter 2*.

### 3.6 Controller dynamical analysis

The controller described by (3-38) through (3-43) is now to be examined to investigate its dynamical response.

#### 3.6.1 No-time delay system

Assuming ideal system with no-time delay that is introduced due to calculation time, the overall control system has been modelled and simulated using MatLab. First the controller with dead-beat gains,  $k_1 = k_2 = k_3 = 1$ , has been examined. Although the controller is stable, as seen from Fig. 3.9, the dead-beat operation cannot be established, as can be noticed from the two poles near to the unit disc boundary and the transient response shown in Fig. 3.10. The voltage reference is not modified after one sample and then the actual grid current is not able to follow its reference during one sample. Moreover, the high peak in the frequency response, plotted in Fig. 3.11, implies oscillatory behaviour in spite of the large bandwidth (the frequency when the gain drops to  $-3$  dB), which means decreased rise time. Hence, to decouple the three controllers and acquire better response, the controller gains are lowered as shown in Table 3-2. The controller is stable, as shown in Fig. 3.12, and a step response from grid reference current to actual current shows a fast response with no overshoot, see Fig. 3.13. Moreover, the frequency response, shown in Fig. 3.14, shows a constant gain that equals 0 dB even at higher frequencies and almost the same bandwidth as in the case of dead-beat gains.

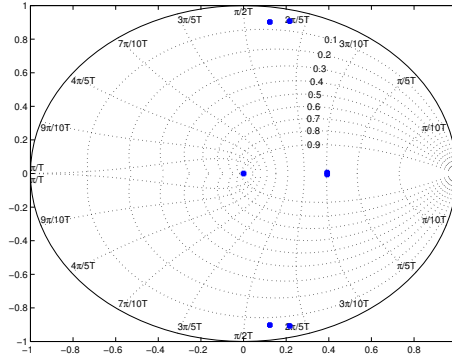
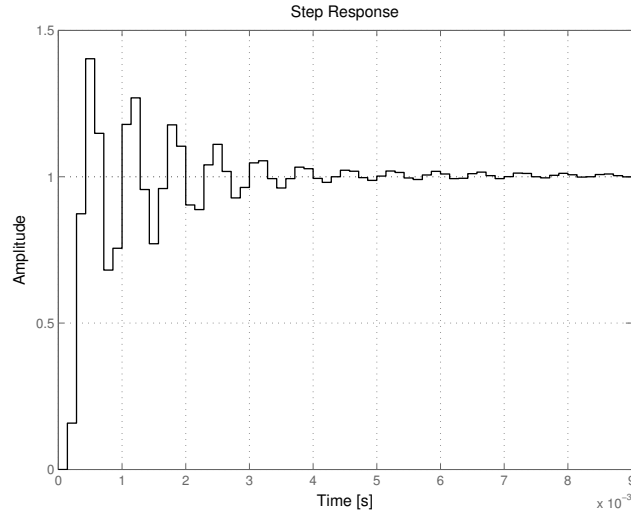
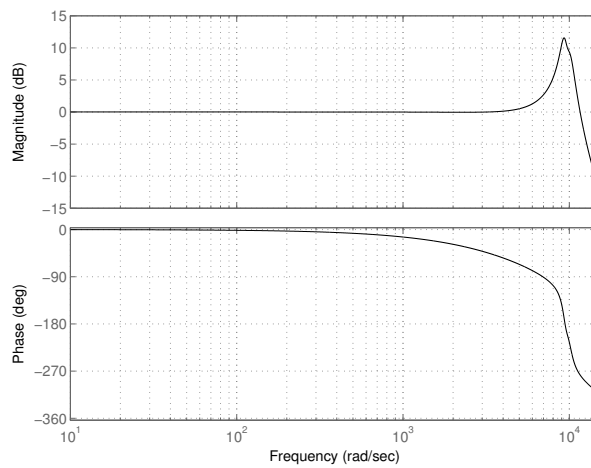


Fig. 3.9 System poles: no-time delay and dead-beat gains.



**Fig. 3.10 Step response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: no-time delay and dead-beat gains.**



**Fig. 3.11 Frequency response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: no-time delay and dead-beat gains.**

**Table 3-2 Controller gain for no-time delay system.**

|       |        |
|-------|--------|
| $k_1$ | 0.7    |
| $k_2$ | 0.8    |
| $k_3$ | 1      |
| $T_i$ | 0.05 s |

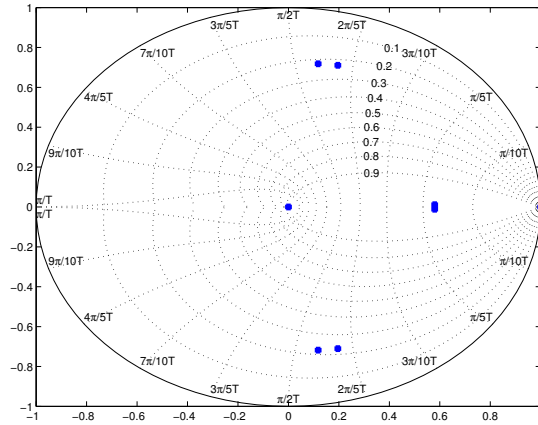


Fig. 3.12 System poles: no-time delay and lower gains.

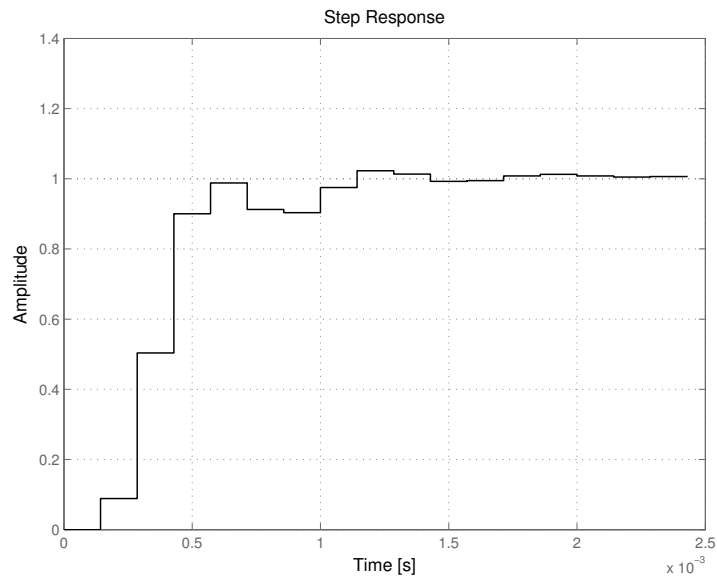
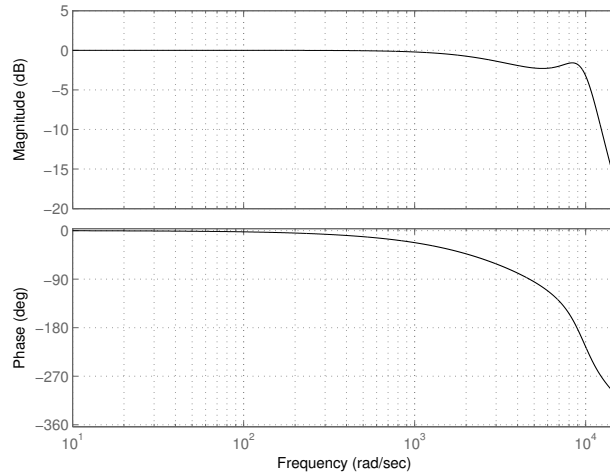


Fig. 3.13 Step response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: no-time delay and reduced gains.





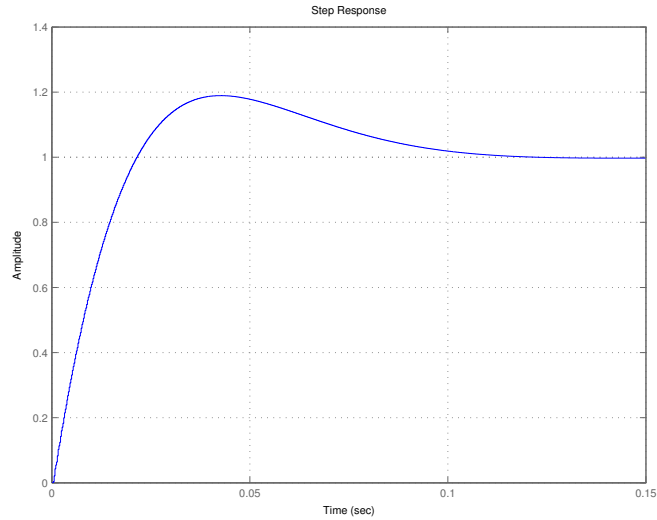
**Fig. 3.14** Frequency response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: no-time delay and reduced gains.

### 3.6.2 One sample time delay with lower gains

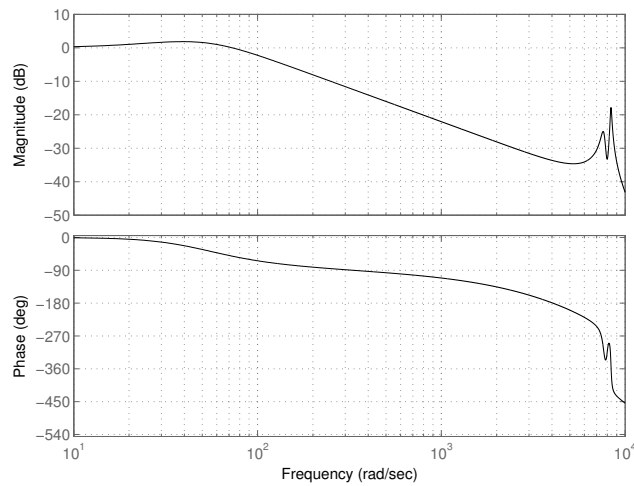
If one sample time delay is considered in order to model the inherent time delay in practical systems, lower gains should be chosen to stabilize the system (as reported in Table 3-3). Although the system is stable, longer transient time and consequently smaller bandwidth are obtained as shown in Fig. 3.15 and Fig. 3.16.

**Table 3-3** Controller gains for one sample time delay system.

|       |        |
|-------|--------|
| $k_1$ | 0.4    |
| $k_2$ | 0.3    |
| $k_3$ | 0.2    |
| $T_i$ | 0.05 s |



**Fig. 3.15** Step response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: one sample time delay with lower gains.



**Fig. 3.16** Frequency response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: one sample time delay with lower gains.

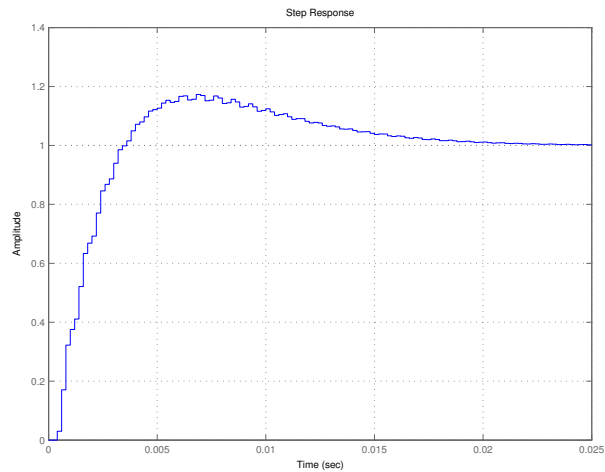
### 3.6.3 One sample time delay with Smith predictor

The Smith predictor is implemented to compensate for the one-sample delay time in order to increase the controller gains as given in Table 3-4. The transient time is reduced, however almost the same overshoot, as in case of the system with lower gains,

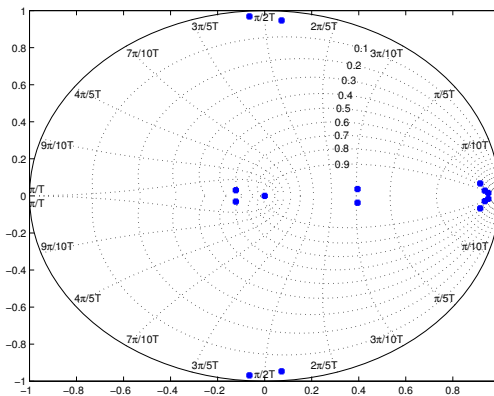
occurs, as shown by Fig. 3.17. This overshoot is mainly due to the two poles near to the upper bound of the unit disc (see Fig. 3.18). These two poles (and their conjugates at the lower bound) are fast moving poles depending on the gain of the inner controller (P3). They move into the unit disc as  $k_{p3}$  takes values less than 30% of the dead-beat gain.

**Table 3-4 Controller gains**

|          |        |
|----------|--------|
| $k_1$    | 1      |
| $k_2$    | 1      |
| $k_3$    | 0.2    |
| $T_i$    | 0.05 s |
| $k_{ps}$ | 0.07   |



**Fig. 3.17 Step response from  $d$ -component of grid current reference to  $d$ -component of actual grid current: one sample time delay with Smith predictor.**



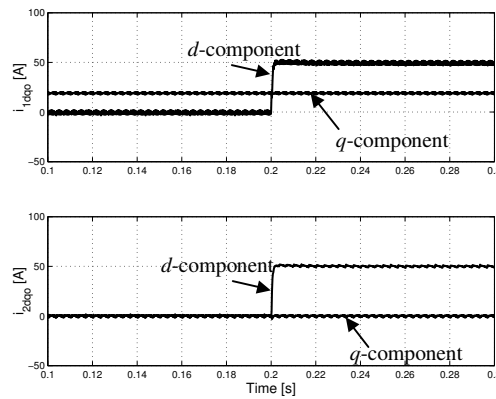
**Fig. 3.18 System poles: one sample time delay with Smith compensator.**

### 3.7 Performance of stiff DC-link system

The complete VSC system that is described in Fig. 3.1, assuming constant DC-voltage input (stiff DC-link), is simulated using MatLab/Simulink to examine its performance due to steps in the reference grid current.

#### 3.7.1 No-time delay system

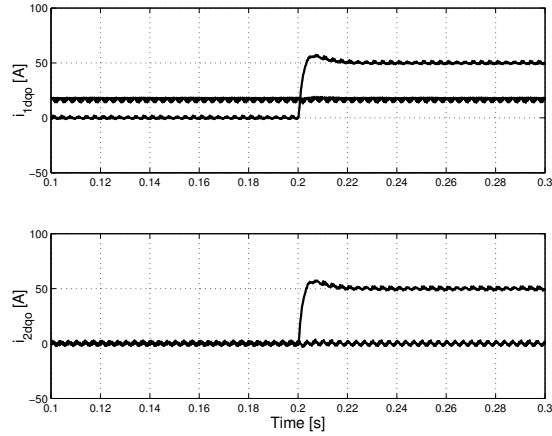
The grid and converter current  $dq$ -components are shown in Fig. 3.19 in case of a step from 0 A to 50 A (0.5 p.u.) in the reference active grid current ( $d$ -component) at 0.2 s. Since the reference reactive grid current ( $q$ -component) is kept constant at 0 A, the VSC will supply the reactive current that is consumed by the LCL-filter. This is a common operation of a DG unit, since usually it is required to keep the power factor at unity at the connection point to decrease the power loss in the feeder (in case of connection to a strong grid).



**Fig. 3.19** Converter-current  $dq$ -components (upper) and grid-current  $dq$ -components (lower).

#### 3.7.2 One sample time delay and Smith predictor

The system implementing Smith predictor to compensate for one sample time delay is simulated for a step from 0 A to 50 A (0.5 p.u.) in the reference active grid current ( $d$ -component) at 0.2 s, while the reference reactive current is constant at 0 A as shown in Fig. 3.20. The performance agrees with the former analysis given in Section 3.6.3, where the settling time is about 0.02 s (one cycle) and almost same overshoot (about 1.2 p.u.).

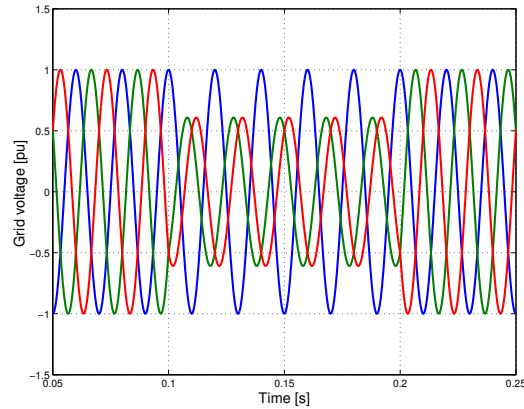


**Fig. 3.20 Converter-current  $dq$ -components (upper) and grid-current  $dq$ -components (lower): system with Smith predictor.**

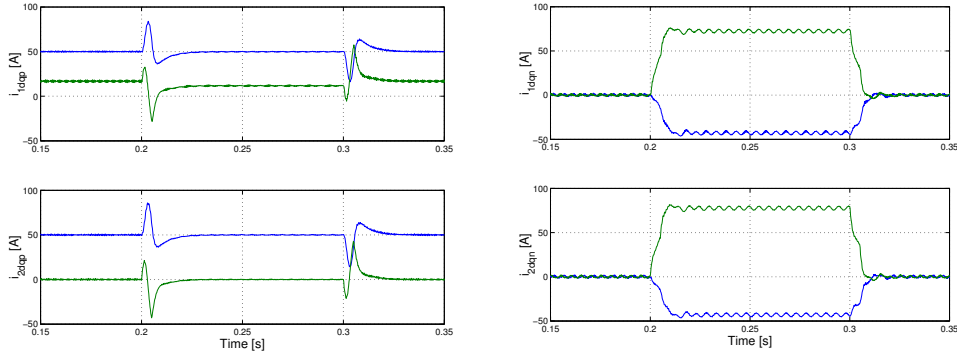
### ***3.8 Performance of stiff DC-link system in case of unbalanced voltage dips***

In this section the performance of the system described in Fig. 3.1, assuming constant DC-voltage input (stiff DC-link), is examined in case of unbalanced grid voltage dips. The sequence separation method explained in *Section 2.5.1* is implemented. Moreover, the voltage dip classification given in [17] and explained in *Section 1.4.1* is applied.

A 40% magnitude of dip type “C” is applied on the grid voltage at 0.1 s for duration of 0.1 s, as shown by Fig. 3.21. The resulting positive and negative sequence current components in  $dq$ -frame are shown in Fig. 3.22.

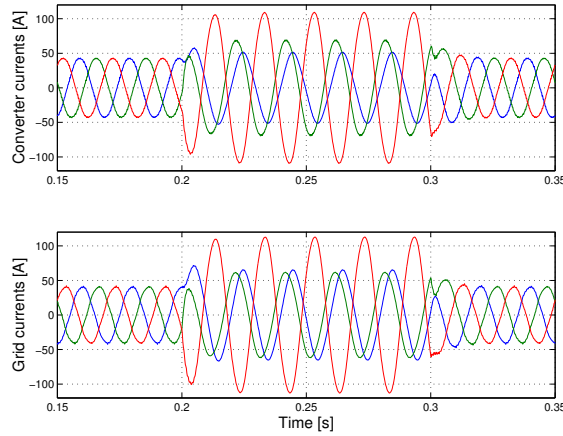


**Fig. 3.21 Grid voltage with 40% dip type “C” applied at 0.1 s for duration of 0.1 s.**



**Fig. 3.22 Positive-sequence (left) and negative-sequence (right) components of converter current (upper) and grid current (lower) in  $dq$ -frame: 40% dip type “C”.**

The resulting three phase currents are unbalanced and increased both in the converter and grid sides as shown in Fig. 3.23.



**Fig. 3.23 Converter current (upper) and grid current (lower): 40% dip type “C”.**

If the stiff DC-link system is to be implemented practically, two criterions might be required, which are symmetrical grid current and/or symmetrical converter current, to meet either the grid regulation or the DG protection regulation. Hence, the controller should be modified in a way to establish these two criterions.

### 3.8.1 Symmetrical grid currents

For the grid currents to be symmetrical, the negative sequence components in  $dq$ -frame should be nullified; i.e.  $i_{2dqn} = 0$ . Hence, in order to compensate for the grid current imbalance, the converter voltage reference should be modified. The negative sequence equations describing the LCL-filter are derived to calculate the appropriate

reference voltage. The equations describing the LCL-filter in steady state and negative sequence frame are:

$$\frac{-R_1}{L_1} i_{1dq} + j\omega i_{1dq} - \frac{1}{L_1} u_{cdqn} + \frac{1}{L_1} u_{dq} = 0 \quad (3-44)$$

$$\frac{-R_2}{L_2} i_{2dq} + j\omega i_{2dq} - \frac{1}{L_2} u_{cdqn} + \frac{1}{L_2} e_{dq} = 0 \quad (3-45)$$

$$\frac{1}{C_f} i_{1dq} - \frac{1}{C_f} i_{2dq} - j\omega u_{cdqn} = 0 \quad (3-46)$$

Then, from (3-45), the following condition should be satisfied:

$$u_{cdqn} = e_{dq} \quad (3-47)$$

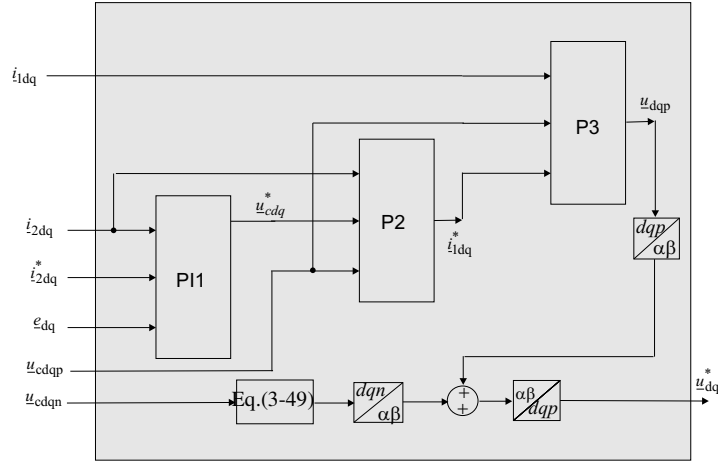
The reference converter current is adjusted (referring to (3-46)) as follows:

$$i_{1dq} = j\omega C_f u_{cdqn} \quad (3-48)$$

Then, the converter voltage reference in  $dqn$ -frame is adjusted (using (3-44)) as follows:

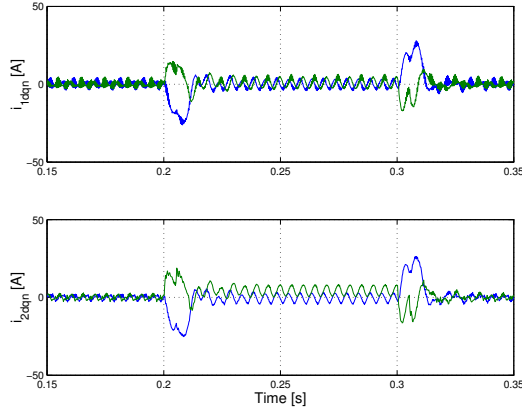
$$u_{dq}^* = u_{cdqn} (1 + \omega^2 C_f L_1) + jR_1 \omega C_f u_{cdqn} \quad (3-49)$$

This is implemented using positive sequence grid voltage and capacitor voltage within the controller equations and the negative sequence capacitor voltage is fed-forward to calculate the negative part of the converter reference voltage, as depicted in Fig. 3.24.

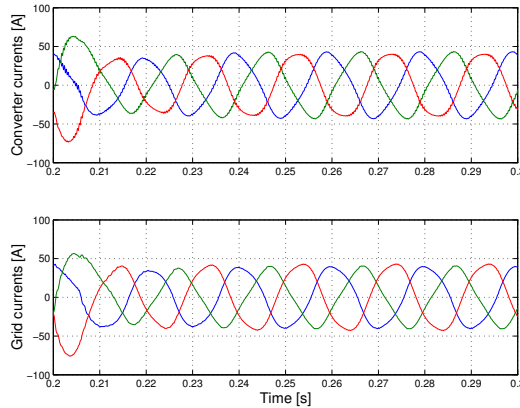


**Fig. 3.24 Simplified block diagram of proposed controller in order to acquire balanced grid currents.**

The controller shown in Fig. 3.24 has been simulated when applying a 40% voltage dip of type “C” at 0.2 s for duration of 0.1 s. The resulting negative sequence converter current and grid current in  $dq$ -frame are shown in Fig. 3.25. Three phase currents are plotted in Fig. 3.26 during the voltage dip period showing decreased and almost symmetrical currents due to decreased negative sequence currents. The transients at the start and end of the dip are mainly due to the inherent settling time of the controller, which has been explained in Section 3.6.3.



**Fig. 3.25** Negative sequence converter current (upper) and grid current (lower) in  $dq$ -frame.

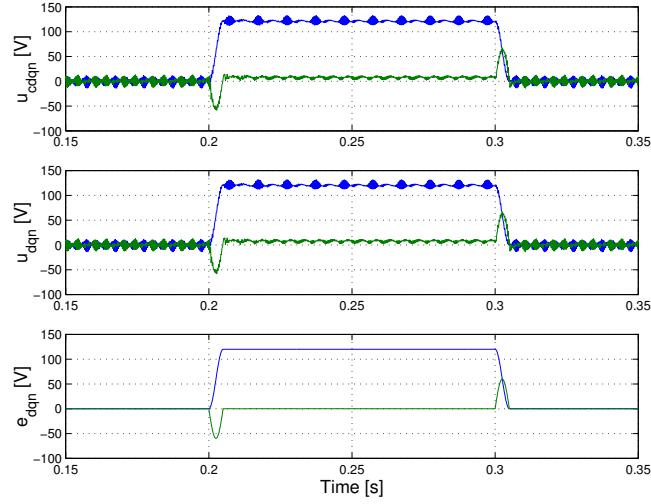


**Fig. 3.26** Converter current (upper) and grid current (lower) during 40% voltage dip of type “C”.

The negative sequence capacitor voltage is equal to the negative sequence converter voltage as shown in Fig. 3.27, since (3-49) is reduced to  $\underline{u}_{dqn} = \underline{u}_{cdqn}$ , which is the condition for balanced converter currents. Hence, the negative sequence converter current is almost nullified preventing the negative sequence grid current from reaching zero since both currents cannot be zero at the same time, as it will be explained in the



next subsection. That explains the remaining negative sequence grid current during the voltage dip shown in Fig. 3.25.



**Fig. 3.27** Negative sequence  $dq$ -components of capacitor voltage (upper), converter voltage (middle) and grid voltage (lower).

### 3.8.2 Symmetrical converter currents

To achieve symmetrical converter currents, the negative sequence of the  $dq$ -components should be nullified, i.e.  $i_{dq} = 0$ . Substituting in (3-44) results in:

$$u_{dq}^* = u_{cdq} \quad (3-50)$$

Hence the controller is implemented in the positive sequence frame and the negative sequence capacitor voltage is fed-forward, as explained in Fig. 3.28. The negative sequence of the converter current is nullified while the negative sequence grid current is significantly reduced, as shown in Fig. 3.29. The ratio of imbalance in the grid current  $r_i$ , which is the ratio of negative sequence current to positive sequence current at fundamental frequency [17], is calculated in  $dq$ -frame as 10% using the equation:

$$r_i = \frac{\sqrt{i_{2dn}^2 + i_{2qn}^2}}{\sqrt{i_{2dp}^2 + i_{2dn}^2}} \times 100 \quad (3-51)$$

The resulting three phase currents are shown in Fig. 3.30. The converter current is symmetrical during the dip period while the grid current is unbalanced with the ratio of 10%.

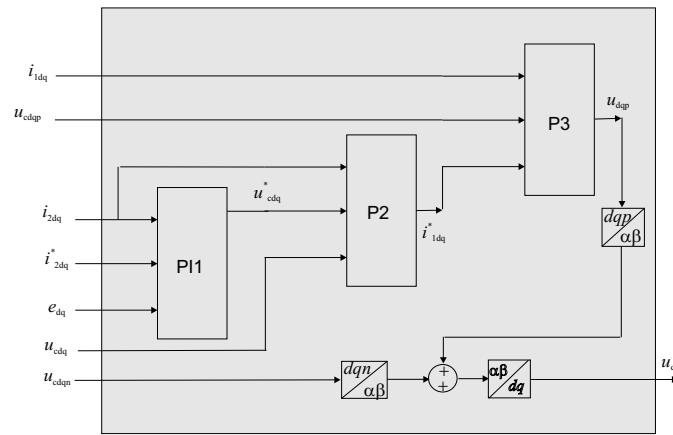


Fig. 3.28 Simplified block diagram of the controller for balanced converter currents.

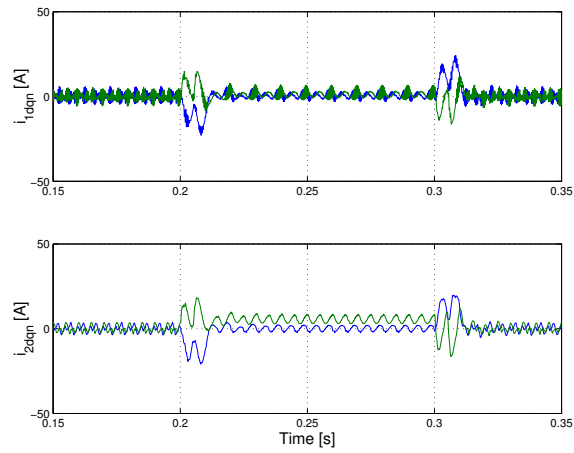


Fig. 3.29 Negative sequence of converter current in  $dq$ -frame.

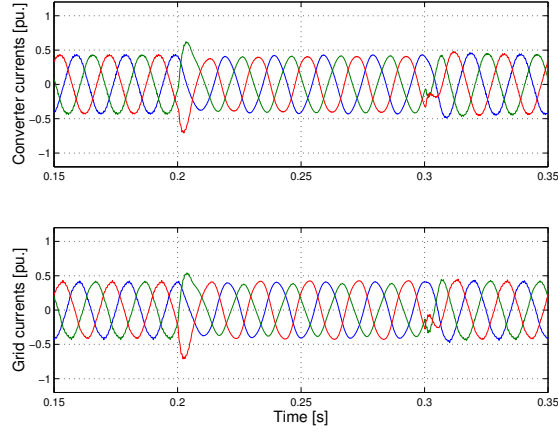


Fig. 3.30 Three-phase converter currents.

### 3.8.3 Symmetrical grid and converter currents

Substituting  $i_{1dq} = 0$  and  $i_{2dq} = 0$  in (3-45) results in  $\underline{u}_{cdqn}^* = \underline{e}_{dq}$ , and in (3-46) results in  $\underline{u}_{cdqn}^* = 0$ . Since both conditions contradict with each other, it is not possible to achieve symmetrical grid and converter currents at the same time.

### 3.9 More Parameters to consider

In the derivation of VCC, as given in *Section 3.5*, it has been assumed that the average voltage and current values over one sample are constants. This assumption is evaluated here by introducing the two parameters  $\xi$  and  $\delta$ , as follows.

$$\underline{u}_{cdq}(k, k+1) = \xi \underline{u}_{cdq}(k) - (\xi - 1) \underline{u}_{cdq}^*(k) \quad (3-52)$$

$$\underline{i}_{2dq}(k, k+1) = \delta \underline{i}_{2dq}(k) - (\delta - 1) \underline{i}_{2dq}^*(k) \quad (3-53)$$

The controller equations are then modified as follows:

$$\underline{u}_{cdq}^*(k) = \underline{e}_{dq}(k) + (R_2 + j\omega L_2) \underline{i}_{2dq}(k) + kp_1 \left( \underline{i}_{2dq}^*(k) - \underline{i}_{2dq}(k) \right) + \underline{\Delta u}_{idq}(k) \quad (3-54)$$

$$\underline{i}_{1dq}^*(k) = \delta \underline{i}_{2dq}(k) - (\delta - 1) \underline{i}_{2dq}^*(k) + j\omega C_f \underline{u}_{cdq}(k) + kp_2 \left( \underline{u}_{cdq}^*(k) - \underline{u}_{cdq}(k) \right) \quad (3-55)$$

$$u_{dq}^*(k+1) = \xi u_{cdq}(k) - (\xi - 1)u_{cdq}^*(k) + (R_1 + j\omega L_1)i_{ldq}(k) + kp_3(i_{ldq}^*(k) - i_{ldq}(k)) \quad (3-56)$$

The effect of changing  $\delta$  and  $\xi$  values from 1 to 0 on the system poles is examined. The system is stable for all  $\xi$  and  $\delta$  values as shown in Fig. 3.31 and Fig. 3.32. The step response is also tested and depicted in Fig. 3.33 and Fig. 3.34. It is concluded that by changing  $\delta$  the poles move slowly into a region with higher damping ratio, however the settling time is increased. Moreover, by changing  $\xi$  the poles move more quickly into a region with higher damping ratio, less settling time, and less overshoot. Hence, the performance of the system has been tested with  $\delta = 1$  and  $\xi = 0.7$  and the same gains as in Table 3-4. An active reference current step is applied at 0.2 s, see Fig. 3.35. Comparing with the ideal case ( $\delta = 1$  and  $\xi = 1$ ), shown in Fig. 3.20, the less overshoot is an obvious difference.

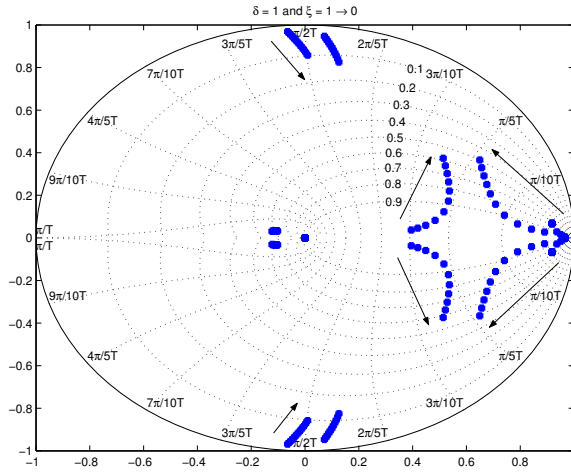


Fig. 3.31 System poles:  $\delta = 1$  and  $\xi$  varies from 1 to 0.

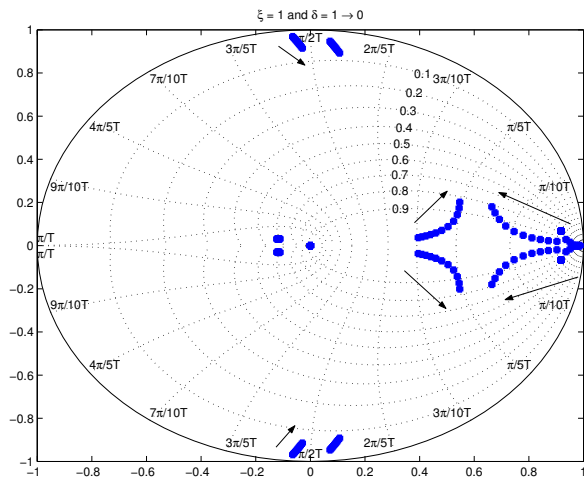


Fig. 3.32 System poles:  $\xi = 1$  and  $\delta$  varies from 1 to 0.

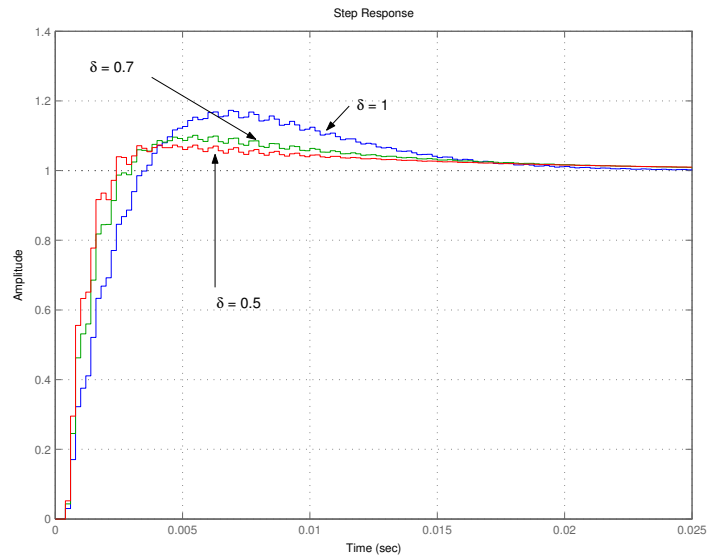
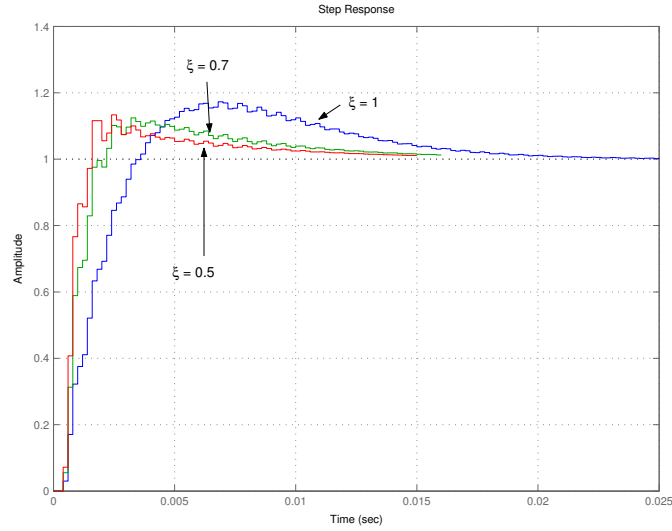
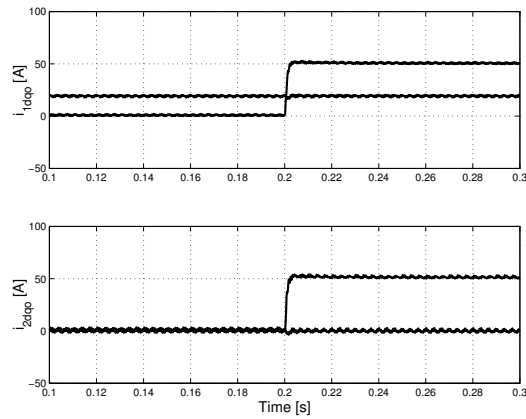


Fig. 3.33 Step response in  $d$ -component of grid current due to a unit step in  $d$ -component of reference grid current:  $\xi = 1$  and  $\delta = 1, 0.7,$  and  $0.5$ .



**Fig. 3.34** Step response in  $d$ -component of grid current due to a unit step in  $d$ -component of reference grid current:  $\delta = 1$  and  $\xi = 1, 0.7,$  and  $0.5$ .



**Fig. 3.35** Converter current (upper) and grid current (lower) in  $dq$ -frame:  $\delta = 1$  and  $\xi = 0.7$ .

### 3.10 Weak DC-link system

The system shown in Fig. 3.1 is considered here. The current references cannot be taken constant, since the DC-link voltage should be regulated to a constant value. Hence the active current reference should be adjusted to keep the DC-voltage close to the nominal value while the reactive current reference can be adjusted to produce specific power factor (reactive power) on the grid side.

### 3.10.1 Current reference generation

The DC-link voltage controller, which is described in *Section 2.4.1*, is used to generate the current commands for the VCC. The current references are then generated to keep the power balance through the system, neglecting the power loss in converter switches. The power at the grid side is:

$$S_2 = e_{dq} i_{2dq}^{conj} \quad (3-57)$$

This is expanded as follows:

$$S_2 = e_d i_{2d} + e_q i_{2q} + j(e_q i_{2d} - e_d i_{2q}) \quad (3-58)$$

The power at the converter side is expressed in the same way as:

$$S_1 = u_d i_{1d} + u_q i_{1q} + j(u_q i_{1d} - u_d i_{1q}) \quad (3-59)$$

Applying KVL at the outer loop of the LCL-filter:

$$\underline{u}_{dq} = e_{dq} + R_1 i_{1dq} + j\omega L_1 i_{1dq} + R_2 i_{2dq} + j\omega L_2 i_{2dq} \quad (3-60)$$

Applying KCL at the capacitor connection node:

$$i_{1dq} = i_{2dq} + j\omega C_f \underline{u}_{cdq} \quad (3-61)$$

Expanding (3-59), results in:

$$P_1 = e_d (i_{2d} - \omega C_f u_{cq}) + i_{1d} (R_1 i_{1d} - \omega L_1 i_{1q} + R_2 i_{2d} - \omega L_2 i_{2q}) \\ + e_q (i_{2q} + \omega C_f u_{cd}) + i_{1q} (R_1 i_{1q} + \omega L_1 i_{1d} + R_2 i_{2q} + \omega L_2 i_{2d}) \quad (3-62)$$

$$Q_1 = e_q (i_{2d} - \omega C_f u_{cq}) + i_{1d} (R_1 i_{1q} + \omega L_1 i_{1d} + R_2 i_{2q} + \omega L_2 i_{2d}) \\ - e_d (i_{2q} + \omega C_f u_{cd}) - i_{1q} (R_1 i_{1d} - \omega L_1 i_{1q} + R_2 i_{2d} - \omega L_2 i_{2q}) \quad (3-63)$$

where  $P_1$  and  $Q_1$  are active and reactive powers at the converter side, respectively. Powers at the converter side and grid side are then related as follows:

$$\begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} = \begin{bmatrix} P_2 \\ Q_2 \end{bmatrix} + \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} \quad (3-64)$$

where  $\Delta P$  and  $\Delta Q$  are the active and reactive powers dissipated in the filter, respectively. These are expressed in two terms: one as a function of the grid-side and converter-side currents;  $\Delta P(i)$  and  $\Delta Q(i)$ , and the second as a function of the grid voltage;  $\Delta P(e)$  and  $\Delta Q(e)$ . Equation (3-64) is expanded as follows, assuming no switching losses:

$$\begin{bmatrix} u_{dc} i_v^* \\ Q_1 \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} + \begin{bmatrix} \Delta P(i) \\ \Delta Q(i) \end{bmatrix} + \begin{bmatrix} \Delta P(e) \\ \Delta Q(e) \end{bmatrix} \quad (3-65)$$

where

$$\Delta P(i) = R_1 (i_{1d}^2 + i_{1q}^2) + R_2 (i_{1d}i_{2d} + i_{1q}i_{2q}) + \omega L_2 (-i_{1d}i_{2q} + i_{1q}i_{2d}) \quad (3-66)$$

$$\Delta Q(i) = R_2 (i_{1d}i_{2q} - i_{1q}i_{2d}) + \omega L_1 (i_{1d}^2 + i_{1q}^2) + \omega L_2 (i_{1d}i_{2d} + i_{1q}i_{2q}) \quad (3-67)$$

$$\begin{bmatrix} \Delta P(e) \\ \Delta Q(e) \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} -\omega C_f u_{cq} \\ \omega C_f u_{cd} \end{bmatrix} \quad (3-68)$$

Rearranging (3-65) results in:

$$\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix}^{-1} \begin{bmatrix} u_{dc}i_v^* - \Delta P_i \\ Q_1 - \Delta Q_i \end{bmatrix} - \begin{bmatrix} -\omega C_f u_{cq} \\ \omega C_f u_{cd} \end{bmatrix} \quad (3-69)$$

To achieve zero reactive power at the grid, the VSC should generate a reactive power  $Q_1$  that is consumed by the filter. Hence:

$$Q_1 = \Delta Q(i) + \Delta Q_c \quad (3-70)$$

where  $\Delta Q_c$  is the power loss in the filter capacitor, it is calculated as:

$$\Delta Q_c = \omega C_f (u_{cd}^2 + u_{cq}^2) \quad (3-71)$$

Then, the reference currents are calculated as:

$$\begin{bmatrix} i_{2d}^* \\ i_{2q}^* \end{bmatrix} = \begin{bmatrix} e_d & e_q \\ e_q & -e_d \end{bmatrix} \begin{bmatrix} u_{dc}i_v^* - \Delta P_i \\ \omega C_f (u_{cd}^2 + u_{cq}^2) \end{bmatrix} - \begin{bmatrix} -\omega C_f u_{cq} \\ \omega C_f u_{cd} \end{bmatrix} \quad (3-72)$$

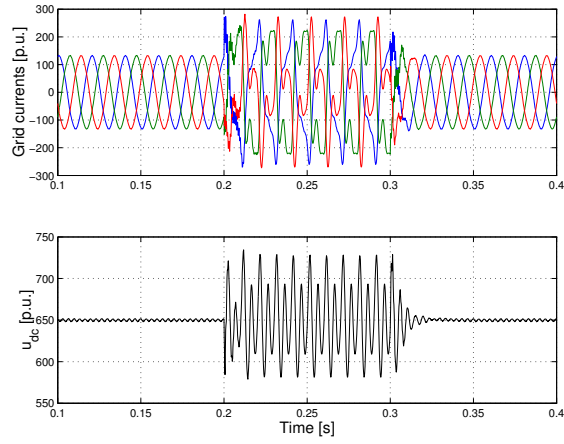
### 3.10.2 Performance in case of unbalanced voltage dips

The controller gains are shown in Table 3-5, when applied to the weak DC-link system. A 40% magnitude of dip type ‘‘C’’ is applied at the grid side at 0.2 s for duration of 0.1 s, as shown in Fig. 3.36. Oscillations of 100 Hz appear during the dip imposed on different currents and voltages, see Fig. 3.37 and Fig. 3.38.

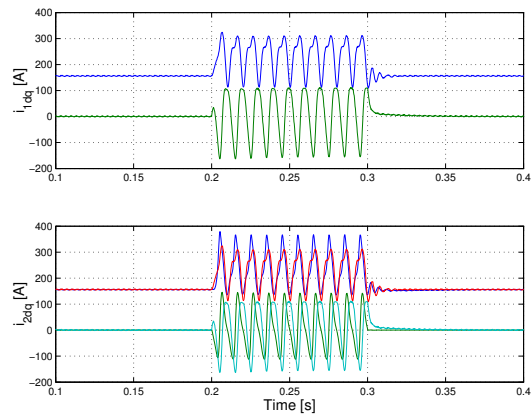
**Table 3-5 Controller gains for weak DC and unbalanced grid voltage.**

|           |         |
|-----------|---------|
| $k_1$     | 1       |
| $k_2$     | 1       |
| $k_3$     | 0.2     |
| $T_i$     | 0.01 s  |
| $k_{ps}$  | 0.5     |
| $k_{pdc}$ | 0.4     |
| $T_{idc}$ | 0.0027s |





**Fig. 3.36** Grid currents (upper) and DC-link voltage (lower).



**Fig. 3.37** Converter current *dq*-components (upper) and grid current *dq*-components (lower).

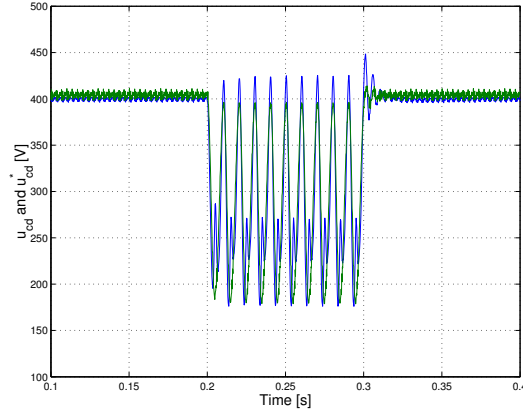


Fig. 3.38 Capacitor voltage  $d$ -component and reference capacitor voltage  $d$ -component.

### 3.11 Dual vector current controller (DVCC) for LCL-filter system

The DVCC presented in Section 2.5, which consists of two separate controllers for controlling positive and negative sequences, has been tested extensively in the previous chapter for the system with L-filter interface. It has proved to give the best performance regarding grid current control and DC-link voltage regulation compared with the VCC, which is implemented in the positive synchronous reference frame. Hence, the DVCC for the system with LCL-filter interface is implemented by transforming the controller, (3-38) to (3-43), into  $dqp$ - and  $dqn$ -frames (as described in Appendix A). The main aim is to acquire sinusoidal grid currents and smooth DC-link voltage in case of unbalanced voltage dips.

#### 3.11.1 Current reference generation for DVCC

The current references are generated in the same manner as in Section 3.10.1. The power at the grid side  $S_2$  is expressed as follows:

$$S_2 = S_{ac,2} + S_{s2,2} + S_{c2,2}$$

where  $S_{ac}$  is the power at the fundamental frequency,  $S_{s2}$  and  $S_{c2}$  are sine and cosine components of the power at double the fundamental frequency, which is called the oscillating power. The power is calculated in  $dqp$ - and  $dqn$ - frames as follows:

$$S_2 = \left( e^{j\omega t} \underline{e}_{dqp} + e^{-j\omega t} \underline{e}_{dqn} \right) \left( e^{j\omega t} i_{2dqp} + e^{-j\omega t} i_{2dqn} \right)^{\text{conj}} \quad (3-73)$$

Expanding this equation leads to:

$$S_{ac,2} = e_{dp}i_{2dp} + e_{qp}i_{2qp} + e_{dn}i_{2dn} + e_{qn}i_{2qn} + j(e_{qp}i_{2dp} - e_{dp}i_{2qp} + e_{qn}i_{2dn} - e_{dn}i_{2qn}) \quad (3-74)$$

$$S_{s2,2} = e_{dp}i_{2qn} - e_{qp}i_{2dn} - e_{dn}i_{2qp} + e_{qn}i_{2dp} + j(e_{qp}i_{2qn} + e_{dp}i_{2dn} - e_{qn}i_{2qp} - e_{dn}i_{2dp}) \quad (3-75)$$

$$S_{c2,2} = e_{dp}i_{2dn} + e_{qp}i_{2qn} + e_{dn}i_{2dp} + e_{qn}i_{2qp} + j(e_{qp}i_{2dn} - e_{dp}i_{2qn} + e_{qn}i_{2dp} - e_{dn}i_{2qp}) \quad (3-76)$$

The power at the converter side  $S_1$  is expressed in the same manner and same designations as:

$$S_1 = S_{ac,1} + S_{s2,1} + S_{c2,1} \quad (3-77)$$

It is calculated in  $dqp$ - and  $dqn$ - frames as follows:

$$S_1 = \left( e^{j\omega t} \underline{u}_{dqp} + e^{-j\omega t} \underline{u}_{dqn} \right) \left( e^{j\omega t} \underline{i}_{1dqp} + e^{-j\omega t} \underline{i}_{1dqn} \right)^{conj} \quad (3-78)$$

Expanding this equation results in the following:

$$S_{ac,1} = u_{dp}i_{1dp} + u_{qp}i_{1qp} + u_{dn}i_{1dn} + u_{qn}i_{1qn} + j(u_{qp}i_{1dp} - u_{dp}i_{1qp} + u_{qn}i_{1dn} - u_{dn}i_{1qn}) \quad (3-79)$$

$$S_{s2,1} = u_{dp}i_{1qn} - u_{qp}i_{1dn} - u_{dn}i_{1qp} + u_{qn}i_{1dp} + j(u_{qp}i_{1qn} + u_{dp}i_{1dn} - u_{qn}i_{1qp} - u_{dn}i_{1dp}) \quad (3-80)$$

$$S_{c2,1} = u_{dp}i_{1dn} + u_{qp}i_{1qn} + u_{dn}i_{1dp} + u_{qn}i_{1qp} + j(u_{qp}i_{1dn} - u_{dp}i_{1qn} + u_{qn}i_{1dp} - u_{dn}i_{1qp}) \quad (3-81)$$

Applying KVL to the outer loop of the LCL-filter:

$$\underline{u}_{dqp} = \underline{e}_{dqp} + R_1 \underline{i}_{1dqp} + j\omega L_1 \underline{i}_{1dqp} + R_2 \underline{i}_{2dqp} + j\omega L_2 \underline{i}_{2dqp} \quad (3-82)$$

$$\underline{u}_{dqn} = \underline{e}_{dqn} + R_1 \underline{i}_{1dqn} - j\omega L_1 \underline{i}_{1dqn} + R_2 \underline{i}_{2dqn} - j\omega L_2 \underline{i}_{2dqn} \quad (3-83)$$

Applying KCL at the filter capacitor connection node:

$$\underline{i}_{1dqp} = \underline{i}_{2dqp} + j\omega C_f \underline{u}_{cdqp} \quad (3-84)$$

$$\underline{i}_{1dqn} = \underline{i}_{2dqn} - j\omega C_f \underline{u}_{cdqn} \quad (3-85)$$

Substituting (3-82) to (3-85) in (3-79), the active power at the converter side will be:

$$\begin{aligned}
 P_{ac,1} = & e_{dp} (i_{2dp} - Y_c u_{cqp}) + i_{1dp} (R_1 i_{1dp} - \omega L_1 i_{1qp} + R_2 i_{2dp} - \omega L_2 i_{2qp}) \\
 & + e_{qp} (i_{2qp} + Y_c u_{cdp}) + i_{1qp} (R_1 i_{1qp} + \omega L_1 i_{1dp} + R_2 i_{2qp} + \omega L_2 i_{2dp}) \\
 & + e_{dn} (i_{2dn} + Y_c u_{cqn}) + i_{1dn} (R_1 i_{1dn} + \omega L_1 i_{1qn} + R_2 i_{2dn} + \omega L_2 i_{2qn}) \\
 & + e_{qn} (i_{2qn} - Y_c u_{cdn}) + i_{1qn} (R_1 i_{1qn} - \omega L_1 i_{1dn} + R_2 i_{2qn} - \omega L_2 i_{2dn})
 \end{aligned} \tag{3-86}$$

where  $Y_c = \omega C_f$ . This reduces to:

$$\begin{aligned}
 P_{ac,1} = & e_{dp} i_{2dp} + e_{qp} i_{2qp} + e_{dn} i_{2dn} + e_{qn} i_{2qn} \\
 & + R_1 (i_{1dp}^2 + i_{1qp}^2 + i_{1dn}^2 + i_{1qn}^2) \\
 & + R_2 (i_{2dp} i_{1dp} + i_{2qp} i_{1qp} + i_{2dn} i_{1dn} + i_{2qn} i_{1qn}) \\
 & + \omega L_2 (-i_{2qp} i_{1dp} + i_{2dp} i_{1qp} + i_{2qn} i_{1dn} - i_{2dn} i_{1qn}) \\
 & + Y_c (-u_{cqp} e_{dp} + u_{cdp} e_{qp} + u_{cqn} e_{dn} - u_{cdn} e_{qn})
 \end{aligned} \tag{3-87}$$

which can be separated into three different parts as follows:

$$P_{ac,1} = P_{ac,2} + \Delta P(i) + \Delta P(e)$$

where  $\Delta P(i)$  is the active power consumed by filter inductors as a function in the grid-side current and the converter-side current, and  $\Delta P(e)$  is the active power consumed by filter inductors as a function in the grid voltage and the capacitor voltage. In the same way, the reactive power at the converter side is calculated as:

$$\begin{aligned}
 Q_{ac,1} = & e_{qp} i_{2dp} - e_{dp} i_{2qp} + e_{qn} i_{2dn} - e_{dn} i_{2qn} \\
 & + \omega L_1 (i_{1dp}^2 + i_{1qp}^2 - i_{1dn}^2 - i_{1qn}^2) \\
 & + R_2 (i_{2qp} i_{1dp} - i_{2dp} i_{1qp} + i_{2qn} i_{1dn} - i_{2dn} i_{1qn}) \\
 & + \omega L_2 (i_{2dp} i_{1dp} + i_{2qp} i_{1qp} - i_{2dn} i_{1dn} - i_{2qn} i_{1qn}) \\
 & + Y_c (-u_{cqp} e_{qp} - u_{cdp} e_{dp} + u_{cqn} e_{qn} + u_{cdn} e_{dn})
 \end{aligned} \tag{3-88}$$

which can be separated into three different parts, as follows:

$$Q_{ac,1} = Q_{ac,2} + \Delta Q(i) + \Delta Q(e)$$

where  $\Delta Q(i)$  is the reactive power consumed by filter inductors as a function in the grid-side current and the converter-side current, and  $\Delta Q(e)$  is the reactive power consumed by filter inductors as a function in the grid voltage and the capacitor voltage. The sine and cosine components of the active oscillating power are derived as:

$$\begin{aligned}
P_{s2,1} &= e_{dp}i_{2qn} - e_{qp}i_{2dn} - e_{dn}i_{2qp} + e_{qn}i_{2dp} \\
&+ 2R_1 (i_{1dp}i_{1qn} - i_{1qp}i_{1dn}) \\
&- 2\omega L_1 (i_{1qp}i_{1qn} + i_{1dp}i_{1dn}) \\
&+ R_2 (i_{2dp}i_{1qn} - i_{2qp}i_{1dn} - i_{2dn}i_{1qp} + i_{2qn}i_{1dp}) \\
&- \omega L_2 (i_{2qp}i_{1qn} + i_{2dp}i_{1dn} + i_{2qn}i_{1qp} + i_{2dn}i_{1dp}) \\
&+ Y_c (-u_{cdn}e_{dp} - u_{cqn}e_{qp} - u_{cdp}e_{dn} - u_{cqp}e_{qn})
\end{aligned} \tag{3-89}$$

$$\begin{aligned}
P_{s2,1} &= P_{s2,2} + \Delta P_{s2}(i) + \Delta P_{s2}(e) \\
P_{c2,1} &= e_{dp}i_{2dn} + e_{qp}i_{2qn} + e_{dn}i_{2dp} + e_{qn}i_{2qp} \\
&+ 2R_1 (i_{1dp}i_{1dn} + i_{1qp}i_{1qn}) \\
&+ 2\omega L_1 (i_{1dp}i_{1qn} - i_{1dn}i_{1qp}) \\
&+ R_2 (i_{2dp}i_{1dn} + i_{2qp}i_{1qn} + i_{2dn}i_{1dp} + i_{2qn}i_{1qp}) \\
&+ \omega L_2 (-i_{2qp}i_{1dn} + i_{2dp}i_{1qn} + i_{2qn}i_{1dp} - i_{2dn}i_{1qp}) \\
&+ Y_c (u_{cqn}e_{dp} - u_{cdn}e_{qp} - u_{cqp}e_{dn} + u_{cdp}e_{qn})
\end{aligned} \tag{3-90}$$

$$P_{c2,1} = P_{c2,2} + \Delta P_{c2}(i) + \Delta P_{c2}(e)$$

Expressing (3-87) to (3-90) in matrix form will result in:

$$\begin{aligned}
\begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} &= \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} \begin{bmatrix} i_{2dp} \\ i_{2qp} \\ i_{2dn} \\ i_{2qn} \end{bmatrix} \\
&+ \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix} Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix}
\end{aligned} \tag{3-91}$$

The current references are then calculated using the following matrix:

$$\begin{bmatrix} i_{2dp}^* \\ i_{2qp}^* \\ i_{2dn}^* \\ i_{2qn}^* \end{bmatrix} = \begin{bmatrix} e_{dp} & e_{qp} & e_{dn} & e_{qn} \\ e_{qp} & -e_{dp} & e_{qn} & -e_{dn} \\ e_{qn} & -e_{dn} & -e_{qp} & e_{dp} \\ e_{dn} & e_{qn} & e_{dp} & e_{qp} \end{bmatrix}^{-1} \begin{bmatrix} P_{ac,1} - \Delta P(i) \\ Q_{ac,1} - \Delta Q(i) \\ P_{s2,1} - \Delta P_{s2}(i) \\ P_{c2,1} - \Delta P_{c2}(i) \end{bmatrix} - Y_c \begin{bmatrix} -u_{cqp} \\ u_{cdp} \\ u_{cqn} \\ -u_{cdn} \end{bmatrix} \quad (3-92)$$

The oscillating power, which is consumed by the filter inductors, is compensated by the power flow from the VSC side. Hence:

$$P_{s2,1} = \Delta P_{s2}(i) \quad (3-93)$$

$$P_{c2,1} = \Delta P_{c2}(i) \quad (3-94)$$

Moreover, the active power at the VSC side is assumed to be equal to the power at the DC side of the converter.

$$P_{ac,1} = u_{dc}^* i_v^* \quad (3-95)$$

To achieve zero reactive power at the grid,  $Q_{ac,1}$  should supply the reactive power consumed by the filter. Hence:

$$Q_{ac,1} = \Delta Q(i) + \Delta Q_c \quad (3-96)$$

where  $\Delta Q_c$  is the power loss in the filter capacitor, which is calculated as:

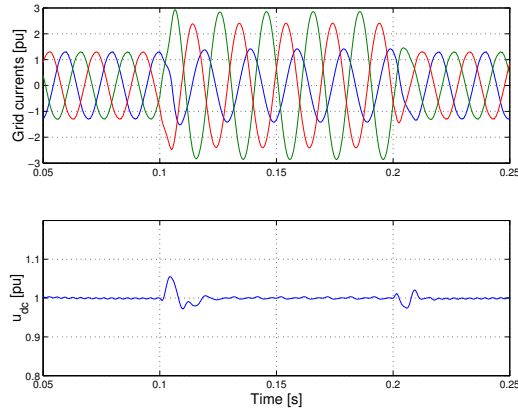
$$\Delta Q_c = \omega C_f \left( u_{cdp}^2 + u_{cqp}^2 + u_{cdn}^2 + u_{cqn}^2 \right)$$

### 3.11.2 Performance in case of unbalanced voltage dips

The DVCC controller gains are reported in Table 3-6. A 40% magnitude of dip type ‘‘C’’ is applied at the grid side. The dip starts at 0.1 s and ends at 0.2 s as shown in Fig. 3.39. The grid current is sinusoidal and the DC-link voltage is almost constant. The transient at the start and end of the dip is due to the inherent settling time (about one cycle) due to the reduced gain in the inner controller as explained before in Section 3.6.3. Compared to the system with L-filter interface (Fig. 2.45), the grid currents are almost the same, however the DC-link voltage transients, at the start and end of the dip, are reduced.

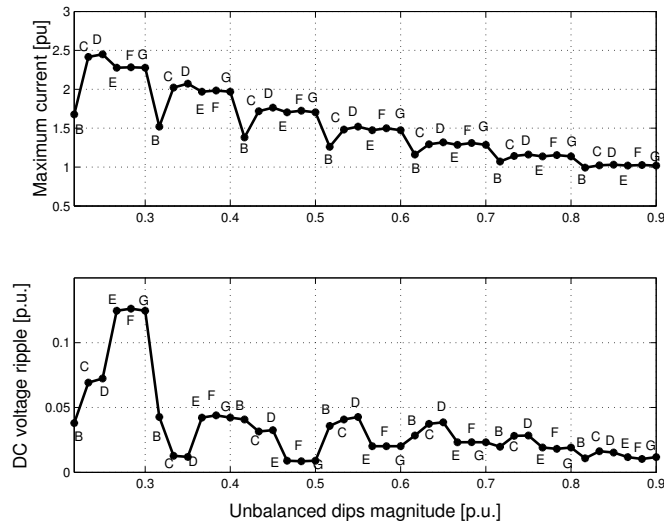
**Table 3-6 DVCC Controller constants.**

|          |     |
|----------|-----|
| $k_1$    | 1   |
| $k_2$    | 0.9 |
| $k_3$    | 0.2 |
| $k_{ps}$ | 0.4 |



**Fig. 3.39** Grid currents (upper) and DC voltage (lower) for 40% magnitude of dip type “C”.

The effect of all unbalanced dips (see the dips classification reported in *Section 1.4.1*), with various magnitudes, on the maximum grid current and DC voltage ripples (in the middle of the dip period) is presented in Fig. 3.40. The base for per unit currents is the maximum of the nominal current of the converter. Compared with the case of L-filter interface system (shown in Fig. 2.48 with a current base value equal to the rms of the nominal current), the currents are almost the same while the DC voltage ripples are slightly increased but still in acceptable range. This is mainly due to the part of the oscillating power consumed by the filter capacitor and not compensated for in the generated reference currents.



**Fig. 3.40** Maximum grid currents (upper) and DC voltage ripples (lower) for different unbalanced dip types and magnitudes from 0.3 to 0.9.

### 3.12 Controller with predicted capacitor voltage

Compared to the system with L-filter interface, the number of sensors (measurements) is increased when implementing LCL-filter interface. Hence in order to reduce the system, the prediction of measured signals is proposed.

Consider a state-space system described as:

$$\begin{aligned} x(k+1) &= Gx(k) + Hu(k) \\ y(k) &= Cx(k) \end{aligned} \tag{3-97}$$

The system is completely observable if the following condition is satisfied [43]:

$$\text{rank} \begin{bmatrix} C \\ CG \\ \vdots \\ CG^{n-1} \end{bmatrix} = n \tag{3-98}$$

where  $n$  is the number of states, and the rank is defined as the number of linearly independent columns or rows of a matrix. This condition is satisfied for the LCL-filter model described in (3-14). Hence, all states can be observed regardless of whether some state variables are available for measurement. This is called full order state observation. Observation of only immeasurable state variables is referred to as minimum order state observation. If it is needed to observe the immeasurable states plus some of the measurable state variables, this is called reduced order state observation [43].

Since the VSC side current is predicted within the controller using Smith predictor and the grid current should be measured to be used in protection equipment, reduced order state observer is implemented to predict the capacitor voltage. The controller is modified as depicted in Fig. 3.41.

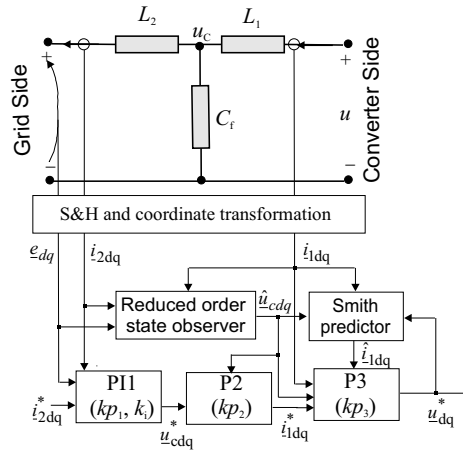


Fig. 3.41 Proposed controller with estimated capacitor voltage.



The controller equations are:

$$\underline{u}_{cdq}^*(k) = \underline{e}_{dq}(k) + (R_2 + j\omega L_2) \underline{i}_{2dq}(k) + kp_1 \left( \underline{i}_{2dq}^*(k) - \underline{i}_{2dq}(k) \right) + \underline{\Delta u}_{dq}(k) \quad (3-99)$$

$$\underline{i}_{1dq}^*(k) = \underline{i}_{2dq}(k) + j\omega C_f \hat{\underline{u}}_{cdq}(k) + kp_2 \left( \underline{u}_{cdq}^*(k) - \hat{\underline{u}}_{cdq}(k) \right) \quad (3-100)$$

$$\underline{u}_{dq}^*(k+1) = \hat{\underline{u}}_{cdq}(k) + (R_1 + j\omega L_1) \underline{i}_{1dq}(k) + kp_3 \left( \underline{i}_{1dq}^*(k) - \hat{\underline{i}}_{1dq}(k-1) \right) \quad (3-101)$$

$$\hat{\underline{i}}_{1dq}(k+1) = \frac{T_s}{L_1} \left( \underline{u}_{dq}^*(k) - \hat{\underline{u}}_{cdq}(k) \right) + \left( 1 - \frac{R_1}{L_1} - j\omega T_s \right) \hat{\underline{i}}_{1dq}(k) + kp_s \left( \underline{i}_{1dq}(k) - \hat{\underline{i}}_{1dq}(k) \right) \quad (3-102)$$

Note that all gains are defined as in Table 3-5.

The observer equations are:

$$\begin{aligned} \hat{\underline{i}}_{2dq}(k+1) = & \frac{T_s}{L_2} \left( \hat{\underline{u}}_{cdq} - \underline{e}_{dq} \right) + \left( 1 - \frac{R_2 T_s}{L_2} \right) \hat{\underline{i}}_{2dq}(k) \\ & - j\omega T_s \hat{\underline{i}}_{2dq}(k) + k_{ec} \left( \underline{i}_{2dq}(k) - \hat{\underline{i}}_{2dq}(k) \right) \end{aligned} \quad (3-103)$$

$$\hat{\underline{u}}_{cdq}(k+1) = \hat{\underline{u}}_{cdq}(k) + \frac{T_s}{C_f} \underline{i}_{1dq}(k) - \frac{T_s}{C_f} \hat{\underline{i}}_{2dq}(k) - j\omega T_s \hat{\underline{u}}_{cdq}(k) \quad (3-104)$$

where  $k_{ec}$  is the observer gain that is introduced to compensate for any differences between the model and the actual system.

### 3.13 Controller robustness

If the LCL-filter parameters are over/under-estimated, their values in the controller will be different from their actual values. In that case, the controller may become instable.

To analyse the effect of variations in the filter parameters, it is assumed that the values in Table 3-1 are the actual values while the estimated parameter values that are used in the controller are:

$$\hat{L}_2 = \Lambda_1 \cdot L_2 \quad (3-105)$$

$$\hat{R}_2 = \Lambda_2 \cdot R_2 \quad (3-106)$$

$$\hat{L}_1 = \Lambda_3 \cdot L_1 \quad (3-107)$$

$$\hat{R}_1 = \Lambda_4 \cdot R_1 \quad (3-108)$$

$$\hat{C}_f = \Lambda_5 \cdot C_f \quad (3-109)$$

where the hat stands for the estimated values of the corresponding parameter and  $\Lambda_1$ ,  $\Lambda_2$ ,  $\Lambda_3$ ,  $\Lambda_4$ , and  $\Lambda_5$  are the ratios of estimated to actual values.

The analysis shows that the system is stable for overestimated grid-side inductor values ( $L_2$ ) as shown in Fig. 3.42, where the arrows show the direction of pole movement. However, the poles slowly move inside the unit circle starting from 50% underestimated values of  $L_2$  as shown in Fig. 3.43.

The system slowly moves into instability starting from 130% of converter-side inductor value ( $L_1$ ) due to the movement of the poles assigned by the arrows in Fig. 3.44, while the poles are moving inside the unit circle for underestimated values (see Fig. 3.45).

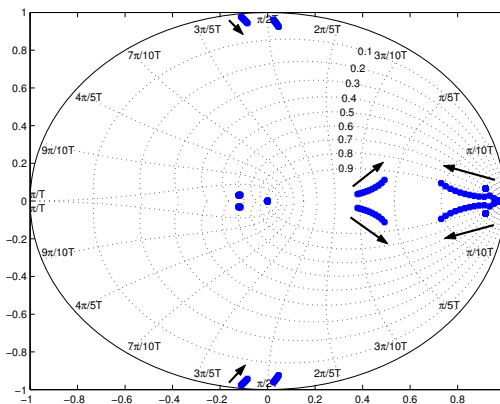
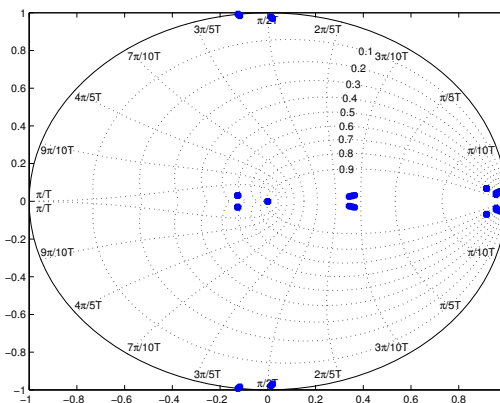
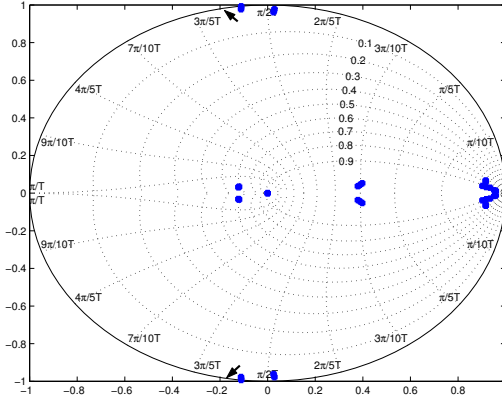


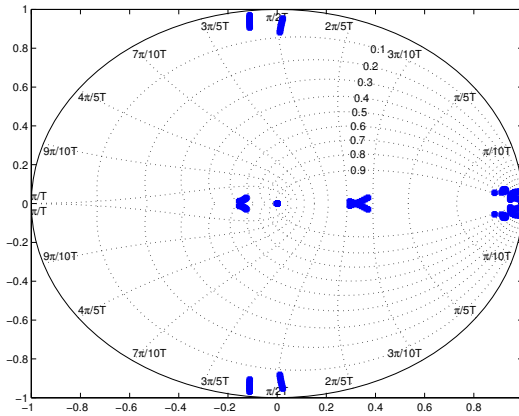
Fig. 3.42 Effect of overestimation in  $L_2$ :  $\Lambda_1$  varies from 100% to 200%.



**Fig. 3.43 Effect of underestimation in  $L_2$ :  $\Lambda_1$  varies from 50% to 90%.**



**Fig. 3.44 Effect of overestimation in  $L_1$ :  $\Lambda_3$  varies from 100% to 120%.**



**Fig. 3.45 Effect of underestimation in  $L_1$ :  $\Lambda_3$  varies from 10% to 90%.**

The resistances  $R_2$  and  $R_1$  have almost no-effect on the pole locations for a wide range of under/over-estimated values. Moreover, the system is stable for overestimated values of filter capacitance ( $C_f$ ) and the poles are moving slowly as shown in Fig. 3.46. Underestimation of  $C_f$  has a negligible effect on the pole locations, as shown in Fig. 3.47. In conclusion, the underestimated  $L_2$  values (less than 50%) and overestimated  $L_1$  values (more than 120%) leads the system to instability, while the change in  $R_1$ ,  $R_2$ , and  $C_f$  does not affect the stability within the tested range (10% - 200%).

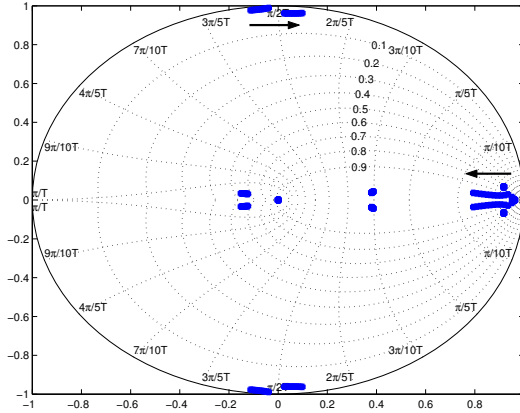


Fig. 3.46 Effect of overestimation in  $C_f$ :  $\Lambda_5$  varies from 100% to 200%.

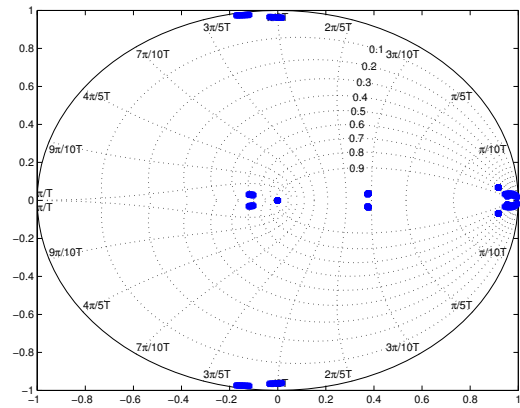


Fig. 3.47 Effect of underestimation in  $C_f$ :  $\Lambda_5$  varies from 10% to 90%.

### 3.14 Conclusions

In this chapter, the voltage source converter (VSC) connected to the grid through LCL-filter is considered. The LCL-filter is designed and modelled. The drawback of using an LCL-filter is the high peak gain realized at the resonance frequency. This gain may be damped passively, by adding a resistance to the filter capacitor, or actively by modifying the controller algorithm. Although, the passive damping is easy to implement, it has been shown that it reduces the filter efficiency at high frequencies.

Then, a cascaded vector current controller (VCC) is derived to increase the stability margin and damp the filter resonance. The performance in case of current steps and voltage imbalance is tested for the system with stiff DC-link voltage and with regulated DC-link voltage. If the system with stiff DC-link voltage is to be implemented

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practically, two criterions have been suggested to modify the VCC depending on either the grid regulation or the distributed generation (DG) protection regulation. Hence, two controllers are proposed: one to produce symmetrical grid currents and the second to produce symmetrical converter currents. It has been shown that it is not possible to control both grid and converter currents to be symmetrical simultaneously. However, controlling the converter current reduces the ratio of imbalance in the grid current.

To improve the performance in case of unbalanced voltage dips at the grid for the system with weak DC-link voltage, the dual vector current controller (DVCC) is implemented. The grid current commands are derived based on the instantaneous power flow through the system. The power loss in the VSC is neglected and the oscillating power, which is the power at double the fundamental frequency produced due to unbalanced faults, is considered to be supplied from the VSC side. The performance of DVCC is evaluated by calculating the maximum current and peak-to-peak DC-link voltage ripples during all types of unbalanced faults.

Compared to the system with L-filter interface, the number of sensors (measurements) is increased implementing LCL-filter interface. Hence in order to reduce the system, the prediction of measured signals is proposed. Since the converter side current is predicted within the controller using Smith predictor and the grid current should be measured to be used in protection equipment, reduced order state observer is implemented to predict the capacitor voltage.

At the end of the chapter, the robustness of the controller in the sense of filter parameters variation is tested. The underestimated values of the grid-side inductance (less than 50%) and overestimated values of the VSC-side inductance (more than 120%) leads the system to instability, while the change in  $R_1$ ,  $R_2$ , and  $C_f$  does not affect the stability within the tested range (10% - 200%).



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## 4. Weak Grid Operation

### 4.1 Introduction

The term weak grid usually refers to systems where the voltage level is not constant as in a stiff (or strong) grid. In other words, the grid impedance is significant and has to be taken into account in the analysis or development tasks. Weak grids are usually found in remote areas where the feeders are long. The grids in these areas are usually designed for small loads [45]. When the design load is exceeded, the voltage level may become below the allowed minimum and/or the thermal capacity of the feeders will be exceeded. Hence, voltage regulation of long weak distribution lines is a challenging problem [45]-[50]. Connection of a DG system could appear as a solution to this problem. However, other problems may appear such as the limitation of the energy transfer from the DG to the grid because of the upper voltage level limit [45], [47]. To the best of the author's knowledge, not much publication has been found on this point.

In [46] a D-STATCOM, which is a voltage source inverter (VSI) based device, is used to regulate and balance the voltage at the distribution bus using reactive power injection. The VSI is connected to the grid through LCL-filter. The grid is modelled as series inductances with five distributed equal loads in between. The total load is 5 KVA and the load at the last section is disconnected to examine a step load change. Two control strategies have been compared. The first control strategy uses two cascaded controllers, inner current controller and an outer voltage controller. The reference active current for the inner controller is generated from a DC-link voltage controller, while the reactive reference current is generated from the outer voltage controller to regulate the bus voltage. This controller shows good transient and steady state performance in case of load changes. However, it is not able to compensate for voltage imbalance. The second control strategy implements the outer controller in both positive and negative sequence frames to be able to compensate for voltage imbalance. However, the voltage regulation limits are not discussed. Moreover, the application of D-STATCOMs is different from the application of DGs in that they do not require active power transfer to/from the grid. In [47] a single phase VSI interface of a photovoltaic DG connected to a weak grid through LCL-filter is considered. The LCL-filter has been chosen to increase the maximum export limit of reactive power from the inverter to the grid, which can be increased also by increasing the DC voltage. The control algorithm measures the phase of the terminal voltage using Fourier extraction and then computes the required inverter voltage for the desired active and reactive power export command. Feedback of filter states is used to provide the stability of the controller at higher frequencies. The control of the real and reactive power flow is done on a cycle-by-cycle basis. Hence, it takes several cycles for the system to settle. In [48], a system of variable speed wind turbine (VSWT), connected to a weak grid through two controllable converters with L-filter interface, is compared with a fixed speed wind turbine. The emphasis has been placed on the control of the converters for VSWT system. The VSWT-side converter applies indirect field-oriented voltage controller, while the grid-side converter applies a current hysteresis controller. The reference values for the latter controller are calculated from the measured phase voltages and the

reference values of the converter active and reactive powers. However, the reactive power reference is not considered, since the voltage compensation is out of interest. Voltage regulation limits are not also considered in [57], since a high DC-link voltage is assumed, which inherently increases these limits.

In this chapter, a three-phase voltage source converter (VSC) is implemented as a front end of a distributed generation (DG) unit. The VSC is connected to a weak grid through an LCL-filter, to smooth out the current on the grid side. The DC-link voltage is considered in two ways: as a constant (or stiff) DC voltage source, and as regulated (or weak) DC voltage with a constant current source. The voltage regulation limits are calculated in both cases. The system is tested in case of a load connection/disconnection and balanced voltage dips.

## 4.2 Weak grid model

A laboratory network model has been used in the simulations to allow future comparison with the experimental work. The model represents a three-phase 400 KV transmission line system. It operates at 400 V with voltage scale of 1:1000 [59]. It consists of six identical  $\pi$  sections of series inductors and shunt capacitors each corresponding to 150 Km. The single line diagram of the simulated scaled distribution network model is shown in Fig. 4.1, where only three sections are considered. The network parameters are given in Table 4-1. The load is chosen to match the VSC rating reported in Table 2-1, as it will be explained later. The system has been simulated in PSCAD/EMTDC.

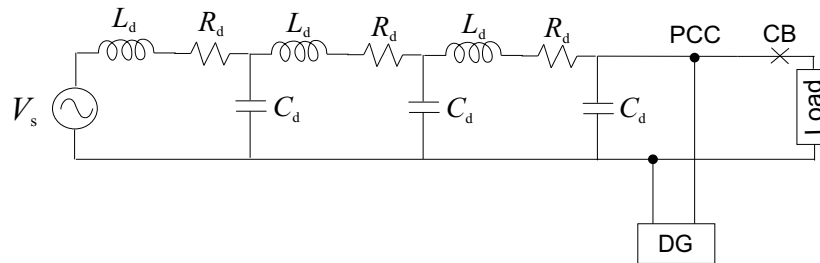


Fig. 4.1 Single line diagram of simulated system.

Table 4-1 Weak network parameters.

| Parameter | Value         |
|-----------|---------------|
| $V_s$     | 400 V         |
| $R_d$     | 0.05 $\Omega$ |
| $L_d$     | 2.05 mH       |
| $C_d$     | 46 $\mu$ F    |



### 4.3 Voltage regulation limit

The energy transfer from a DG unit to the grid is limited in two ways. First, due to the impedance of the grid, the amount of energy that can be absorbed at the point of common coupling (PCC) is limited [45]. This is not considered here, since the control of the DG energy source (e.g. wind energy) is out of interest in this thesis. Second, it is limited by operating limits (or rating) of the VSC system. These limits set the voltage regulation range that the VSC controller can achieve. Hence, they are important to be calculated.

Assuming steady state condition, the LCL-filter capacitance can be neglected. Hence, the equivalent reactance  $X_f$  between the point of common coupling (PCC) and the VSC equals the sum of the series reactances of the LCL-filter, for which values are given in Table 3-1. Assuming zero phase angle of the VSC voltage  $U$ , the angle of the PCC voltage  $E_{(PCC)}$  is  $\delta$ , as depicted in Fig. 4.2. The power flow from the VSC to PCC is derived from the vector diagram shown in Fig. 4.3.

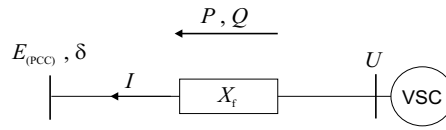


Fig. 4.2 Direction of power flow from VSC to PCC.

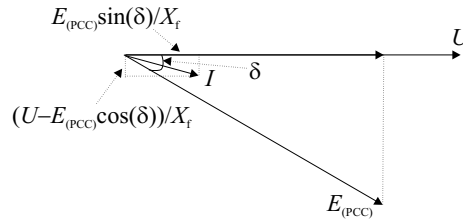


Fig. 4.3 Vector diagram for Fig. 4.2.

The current flowing from the VSC is:

$$I = \frac{E_{(PCC)} \sin \delta}{X_f} - j \frac{U - E_{(PCC)} \cos \delta}{X_f} \quad (4-1)$$

The power transfer to the PCC is then:

$$S = UI^{\text{conj}} = U \left( \frac{E_{(PCC)} \sin \delta}{X_f} + j \frac{U - E_{(PCC)} \cos \delta}{X_f} \right) \quad (4-2)$$

$$P = \frac{UE_{(PCC)} \sin(\delta)}{X_f} \quad (4-3)$$

$$Q = \frac{U}{X_f} (U - E_{(PCC)} \cos \delta) \quad (4-4)$$

The last equation can be read as:

$$Q = \frac{U^2}{X_f} - \sqrt{\left(\frac{UE_{(PCC)}}{X_f}\right)^2 - P^2} \quad (4-5)$$

Since most loads are inductive, the active power  $P$  is considered constant. Hence, the change in the reactive power  $Q$  results in a change in the PCC voltage  $E_{(PCC)}$ . However, the reactive power transfer limit leads to maximum voltage regulation limit. Since the total apparent power of the converter is transferred as active and reactive powers to the PCC, the maximum reactive power flow  $Q_{\max}$  is achieved when the active power is zero. In other words,  $Q_{\max}$  is assumed to be equal to the rated converter power  $S_n$ . Moreover, in most DG systems the DC voltage is either constant or regulated to a certain value, which results in a limited converter voltage. Hence, to calculate the maximum limit for the voltage at PCC, (4-5) is rewritten as follows:

$$E_{(PCC)} = U - \frac{X_f}{U} Q_{\max} \quad (4-6)$$

where  $U$  equals  $\frac{U_{DC}}{2\sqrt{2}}$  for sinusoidal PWM of the VSC. The value of the reactive power limit  $Q_{\max}$  in (4-6) will take a negative sign, which means that it is consumed, since it should compensate for load disconnection. Equation (4-6) is used also to calculate the minimum voltage limit by substituting  $Q_{\max}$  with positive sign. Using the ratings of the VSC, the calculated voltage limit at PCC will be about 30% over/under the nominal value. However, this limit is higher/lower than the actual values since the capacitive and resistive parts of the filter are not considered in the previous analysis. Moreover, the active power loading will also affect this limit since it will decrease the consumed/supplied reactive power resulting in decreasing the voltage limit. Then, the way to get more reactive power or higher voltage regulation limit is to increase the DC-voltage or reduce the impedance of the filter.

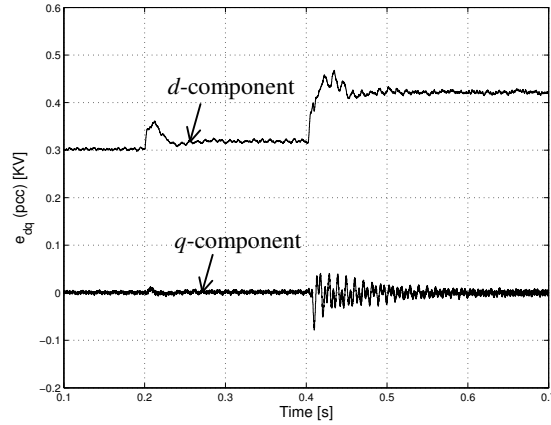
#### 4.4 Voltage regulation for stiff DC-link systems

To prove the regulation limits, the VSC system with stiff DC-link voltage is implemented. The controller, which has been developed in Section 3.5, is tested for the system described in Fig. 4.1.

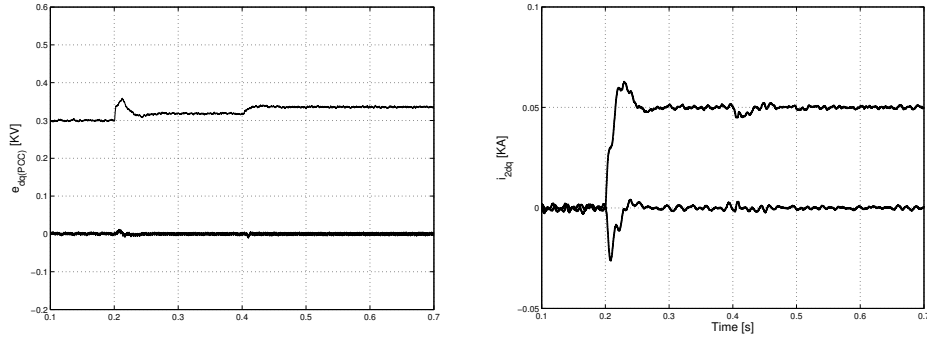
Three pure inductive loads each of 10 KVA are applied at each phase at the PCC. A step in the reference active component of the grid-side current  $i_{2d}^*$  from 0 to 50 A (0.5 p.u.) is applied at 0.2 s, and the load circuit breaker (CB) is disconnected at 0.4 s. The reactive component of the reference grid-side DG current  $i_{2q}^*$  is kept constant at 0 A.

An active current step leads to a step in the active power and then the voltage at the PCC will increase, as shown in Fig. 4.4. The disconnection of the total load will result in raising the PCC voltage above the nominal value. Disconnection of a part of the load

will result in reduced transient oscillations. This is shown in Fig. 4.5, where 2 KVA of the phase load is disconnected at 0.4 s. The system is stabilized within one cycle.



**Fig. 4.4 Voltage  $dq$ -components at PCC: active current step at 0.2 s and total load disconnection at 0.4 s.**



**Fig. 4.5 Voltage  $dq$ -components at PCC (left) and grid-side DG current  $dq$ -components (right): active current reference step at 0.2 s and 2KVA load disconnection at 0.4 s.**

#### 4.4.1 Derivation of the PCC-voltage regulator

As shown in the previous section, if the active power is assumed to be constant, the change in the reactive power leads to a change in the voltage at the PCC. The reactive power generated by the DG at the PCC, which has been derived in *Section 3.10.1*, is:

$$Q_{(PCC)} = e_q(PCC)i_{2d} - e_d(PCC)i_{2q} \quad (4-7)$$

Since the voltage oriented synchronous frame transformation sets the  $q$ -component of the voltage into zero, then  $i_{2q}$  is used to control the reactive power flow. Since

$e_{d(\text{PCC})}$  is regulated, then the reactive current reference is generated to compensate the error in the voltage using a PI-controller, as follows:

$$i_{2q}^*(k) = k_{pv} \left( e_{d(\text{PCC})}(k) - e_{d(\text{PCC})}^*(k) \right) + \Delta i_e(k) \quad (4-8)$$

$$\Delta i_e(k+1) = \Delta i_e(k) + k_{iv} \left( e_{d(\text{PCC})}(k) - e_{d(\text{PCC})}^*(k) \right) \quad (4-9)$$

where  $k_{pv}$ : the proportional gain of the PCC-voltage regulator;  
 $\Delta i_e$ : the integration part;

$k_{iv}$ : the integral constant, which is calculated as  $k_{iv} = \frac{k_{pv}T_s}{T_{iv}}$ ;

$T_{iv}$ : the integration time;

$T_s$ : the sampling time.

The integral time for the PCC-voltage regulator  $T_{iv}$  is chosen to be bigger than the integral time of the main controller, since the voltage regulator should be slow enough to stabilize the system. The voltage regulator constants are calculated by try and error and reported in Table 4-2.

**Table 4-2 Voltage regulator constants.**

|          |             |
|----------|-------------|
| $k_{pv}$ | 0.5         |
| $T_{iv}$ | 0.03 s      |
| $T_s$    | 200 $\mu$ s |

#### 4.4.2 Transient performance of PCC-voltage regulator

The PCC-voltage regulator is implemented as shown in Fig. 4.6. The DC-link voltage regulator and current reference generation blocks are disabled to examine the transient performance in case of reference current steps.

A step in the active current reference  $i_{2d}^*$  from 0 A to 50 A (0.5 p.u.) is applied at 0.2 s, and the total load is disconnected at 0.4 s. The voltage is maintained at the nominal value with long transient time (about 5 cycles) in case of total load disconnection, as shown in Fig. 4.7. However, if only a part of the load is disconnected the voltage is restored in about one cycle, as shown in Fig. 4.8 for disconnection of 2 KVA of the load in each phase.

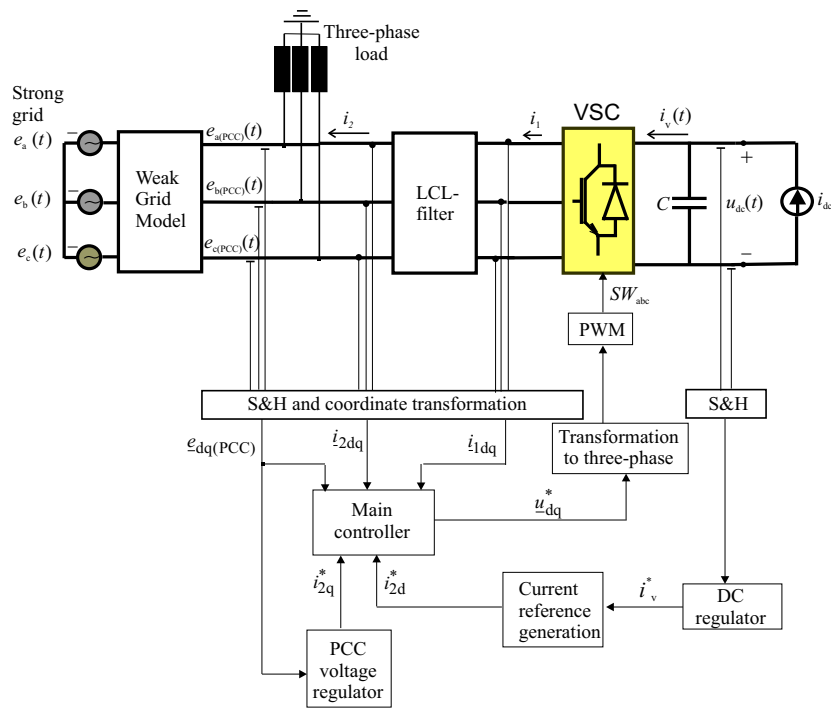


Fig. 4.6 Schematic diagram of controller for weak grid.

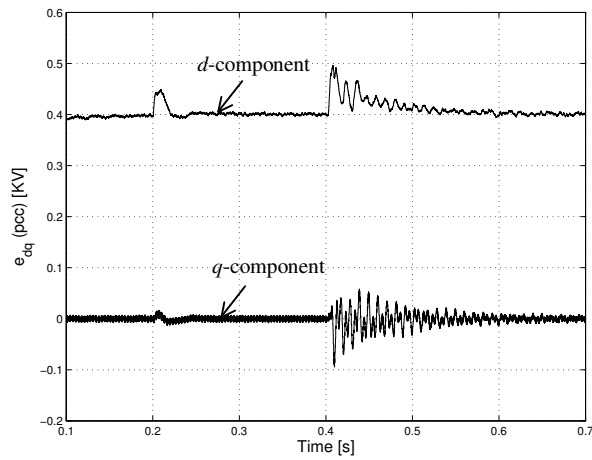
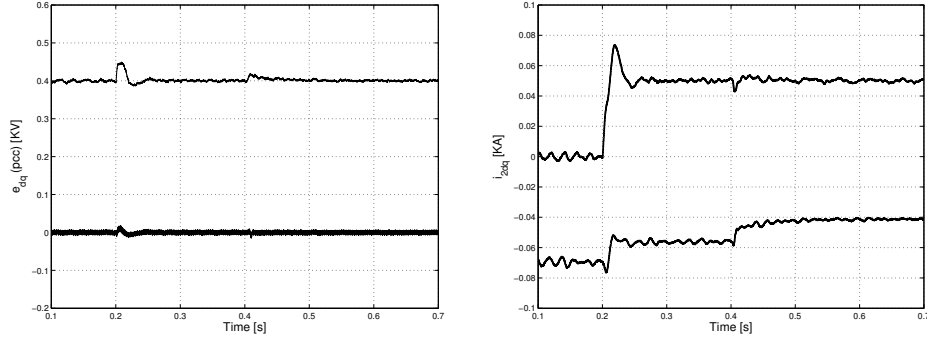


Fig. 4.7 Voltage  $dq$ -components at the PCC: active current step at 0.2 s and total load disconnection at 0.4 s.



**Fig. 4.8 Voltage  $dq$ -components at PCC (left) and grid-side DG current  $dq$ -components (right): active current step at 0.2 s and 2 KVA load disconnection at 0.4 s.**

#### 4.5 Voltage compensation for weak DC-link systems

In weak DC-link systems, the active power flow is controlled to maintain the DC-link voltage constant and equal to the reference value. This is done by generating an active current reference command that adjusts the reference converter voltage in such a way to maintain the required DC-link voltage. In other words, the DC regulator contributes to the PCC voltage compensation by changing the active power. However, the voltage regulation limits are significantly reduced. Equation (4-5) can be rewritten as follows:

$$E_{(PCC)} = \frac{X_f}{U} \sqrt{P^2 + \left( \frac{U^2}{X_f} - Q \right)^2} \quad (4-10)$$

where the reactive power is  $Q = \sqrt{S_n^2 - P^2}$ , assuming no harmonics.

The maximum limit for the voltage at the PCC will occur in case of load disconnection where the reactive power  $Q$  must be consumed by the DG and then it will take a negative sign. On the other hand, the minimum limit for the voltage at the PCC will occur in case of load connection where the reactive power  $Q$  must be supplied to the PCC and then it will take a positive sign. The voltage limits are then calculated for  $P = P_{dc}$ , where  $P_{dc}$  is the active power required to keep the DC-link voltage equal to the reference command. These limits are calculated as about 4% above/under the nominal value. Hence, the disconnected/connected load that the VSC controller can compensate for, in case of VSC with weak DC-link, is much less than the case of VSC with stiff DC-link.

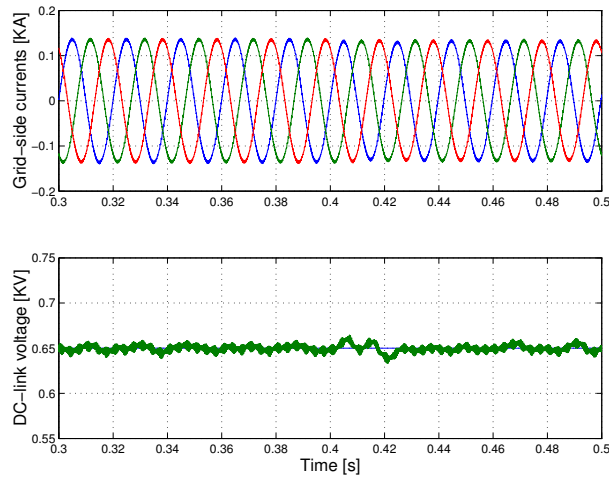
The voltage regulator then calculates the required reactive power. The time constant of the voltage regulator is chosen to be longer than the time constant of the DC regulator to decouple their operation. Gains for both regulators are reported in Table 4-3.

**Table 4-3 DC regulator and voltage regulator constants.**

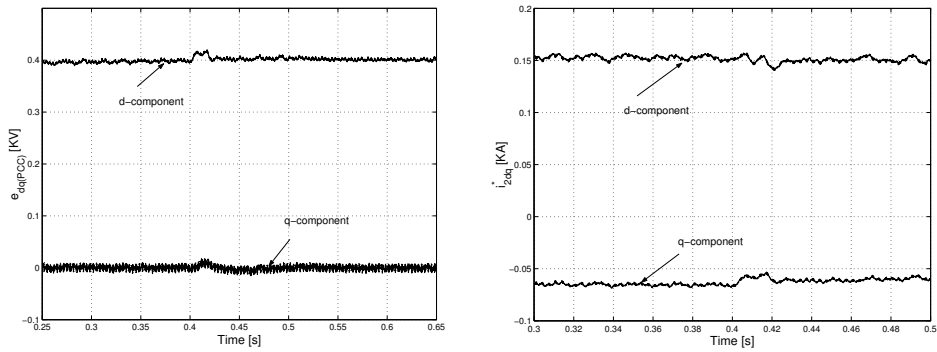
|           |                                     |        |
|-----------|-------------------------------------|--------|
| $k_{pdc}$ | DC regulator proportional gain      | 0.6    |
| $T_{idc}$ | DC regulator integration time       | 0.04 s |
| $k_{pv}$  | Voltage regulator proportional gain | 0.5    |
| $T_{iv}$  | Voltage regulator integration time  | 0.05 s |

### 4.5.1 Load disconnection

The VSC with weak DC-link is examined in case of 2 KVA load disconnection in each phase at 0.4 s. The DC-link voltage, shown in Fig. 4.9, is maintained at its reference value and the PCC voltage is regulated to the nominal value, as shown in Fig. 4.10. The transient time, which is about one cycle, is mainly due to the inherent transient time of the main controller, as explained in *Section 3.6.3*.



**Fig. 4.9** Grid-side current of the VSC (upper) and DC-link voltage (lower): load is disconnected at 0.4 s.

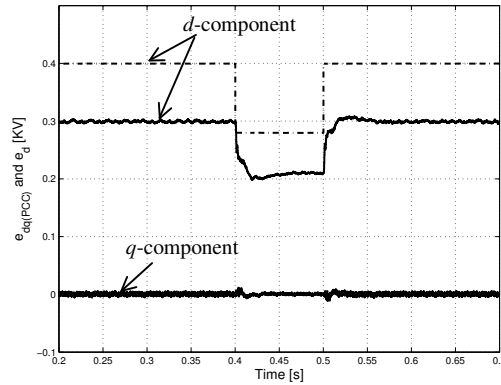


**Fig. 4.10** PCC voltage  $dq$ -components (left) and reference grid-side current (right).

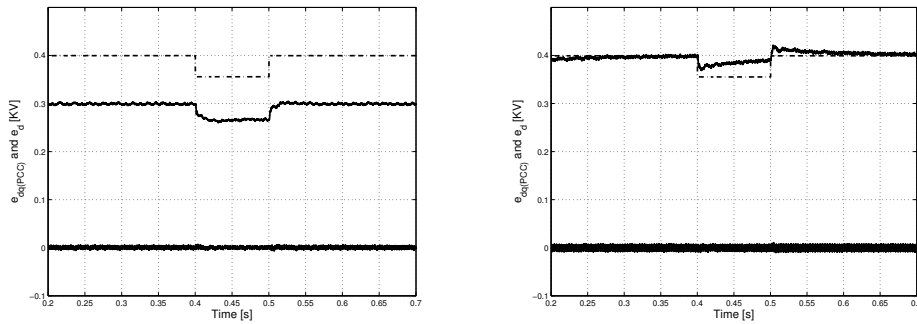
## 4.5.2 Balanced voltage dips

The application of balanced voltage dips at the point of common coupling (PCC) has the same effect on the PCC voltage as the case of connection and then disconnection of three phase balanced loads.

Since the lower voltage limit for systems with stiff DC-link is 30% as mentioned before, the system should be able to mitigate dips starting from 70% and higher at the PCC. Applying a 70% magnitude of dip type “A” at 0.4 s for duration of 0.1 s at the strong grid source results in about 50% dip at the PCC, as shown in Fig. 4.11, in case of deactivated PCC voltage regulator. Then, 89% magnitude of dip type “A” is applied at the strong grid, which results in about 70% remaining voltage at the PCC during the dip as shown in Fig. 4.12. As shown in the same figure, the voltage is successfully regulated, however a long rise time inherently exists due to the choice of large compensator time constant to decouple the operation of different controllers.



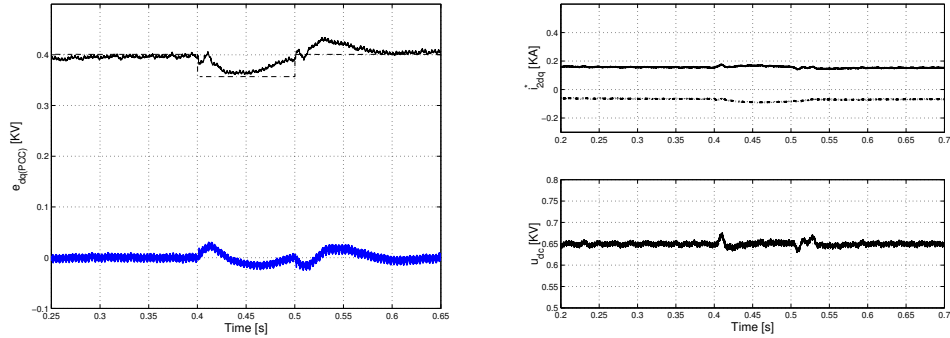
**Fig. 4.11** Voltage at PCC (solid) and voltage at the strong grid (dash-dotted)  $d$ -component for 70% balanced dip at the strong grid (stiff DC-link) with no-Compensation.



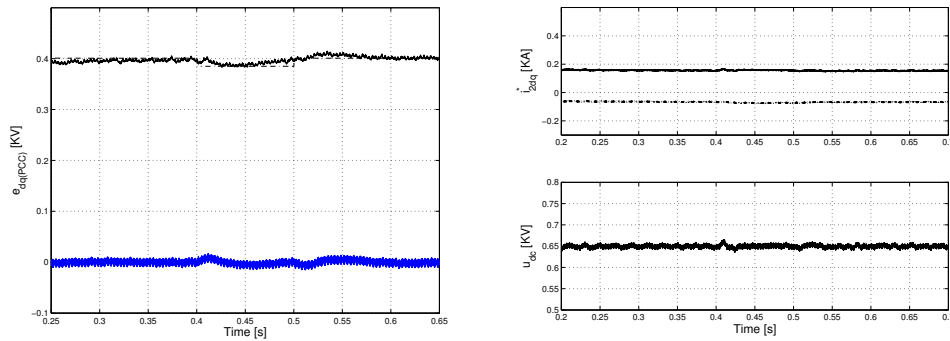
**Fig. 4.12** Voltage at PCC (solid) and voltage at the strong grid (dash-dotted)  $d$ -component for 89% balanced dip at the strong grid (stiff DC-link) with: no-Compensation (left) and voltage compensation (right).



For weak DC-link systems, the lower voltage limit is 4% as explained before. The system is tested with 89% magnitude of dip type “A”, as shown in Fig. 4.13, and 96% magnitude of dip type “A”, as shown in Fig. 4.14, at the strong grid. The controller is capable of maintaining the voltage for both cases, however the same long transient time holds.



**Fig. 4.13** Balanced dip of magnitude 89% at the strong grid (weak DC-link system): voltage  $dq$ -component at PCC (left), reference currents  $dq$ -component and DC-link voltage (right).



**Fig. 4.14** Balanced dip of magnitude 96% at the strong grid (weak DC-link system): voltage  $dq$ -component at PCC (left), reference currents  $dq$ -component and DC-link voltage (right).

## 4.6 Conclusions

In this chapter, a three-phase voltage source converter (VSC) is implemented as a front end of a distributed generation (DG) unit. The VSC is connected to a weak grid through an LCL-filter, to smooth out the current on the grid side. A laboratory network model has been used in the simulation to allow future comparison with the experimental work.

The DC-link voltage input of the VSC is considered in two ways: as a constant (or stiff) DC voltage source, and as regulated (or weak) DC voltage with constant DC

current source. Voltage regulation limits are calculated for both cases to be: 30% of nominal value for the VSC with stiff DC-link voltage, and 4% for the VSC with weak DC-link voltage.

A PI-controller is described for the regulation of the voltage at the point of common coupling (PCC). It is implemented as an outer loop for the main vector current controller (VCC), which has been derived in the previous chapter. The controller is tested in case of a load connection/disconnection and balanced voltage dips. It has been shown that it is capable of regulating the PCC voltage within the calculated regulation limits.

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## 5. Conclusions and Future Work

### 5.1 Introduction

The aim of the thesis has been to investigate how the power electronics interface for a distributed generation (DG) unit can enhance the reliability of the electric power system as experienced by customers. This reliability is considered from two points of view: voltage dips and current harmonics. In order to realize that, a DG unit implementing a variable-speed wind turbine with full-scale converter interface is considered. Throughout the work, a voltage source converter (VSC) is implemented as the front end of the DG unit due to its high controllability and output power quality. This chapter presents the conclusions of the work and introduces some possible future work.

### 5.2 Conclusions

The performance of the voltage source converter (VSC) connected to the grid through a filter inductor (L-filter) and subject to unbalanced voltage dips has been treated. The dual vector current controller (DVCC) has been implemented and tested extensively through the simulation of all possible voltage dips that may occur at the converter terminals. Two methods for generation of current references for the controller have been implemented and compared. These methods depend on how the oscillating power, which is the power at double the fundamental frequency produced due to unbalanced faults, is compensated. In the first case, the oscillating powers are supplied from the DC side into the filter, while in the second case the oscillating powers are supplied from the grid side and dissipated in the filter. The second case has shown better performance (compared to the first case) regarding the grid current harmonics and DC-link voltage regulation. The grid currents are slightly decreased and the DC voltage ripple is significantly smoothed out during the transient at the beginning and end of the dip, and reduced practically to zero during the dip.

The effect of dips with phase angle jump has been also examined with different dip types and magnitudes. For the impedance angles considered here, it can be concluded that there is no noticeable difference in maximum current amplitude and DC voltage ripple during the dip for impedance angles of  $\alpha = 10^\circ$  and  $\alpha = -20^\circ$  (representing dips generated at transmission level or distribution level with overhead lines). On the other hand, for  $\alpha = -60^\circ$ , which represents dips originated by faults in underground cables, the effect of the phase angle jump is noticeable and more significant for lower dip magnitudes. So this effect should be taken into account when designing the converter circuit to ride through the smaller-magnitude voltage dips.

Design equations have been derived to calculate the required current rating of the converter switches to be able to ride through a specific dip magnitude. The designed current ratings are slightly over-estimated since they are derived without considering the power dissipated in the filter. However, this over-estimation is preferred in the design stage because it gives a safety margin to the design values.

The effect of decreasing the input power is also examined. Temporarily decreasing the input power to the system during fault reduces the currents during that period,

which could be a way to decrease the ratings of the converter valves. This, however, would require that the input power to the DC bus be reduced quickly. However, it seems difficult to realize a voltage source at which the input power can be decreased so quickly. On the other hand, if the DC bus is powered by a source that is stochastic in nature, e.g. wind, one could argue that the probability that a dip occurs when the wind turbine is producing full power might be very low, as the turbine often runs at much lower power. Hence, by considering the statistic character of the wind output power, it is clear that even without oversizing the converter interface, some limited ride-through capability is ensured. However, if a higher ride-through capability is required, some overrating of the VSC will be necessary. This has been investigated through a case study.

An inductor-capacitor-inductor filter (LCL-filter) is then implemented, instead of the L-filter, to eliminate high frequency harmonics imposed on the grid side current due to PWM switching of the VSC. A cascaded vector current controller (VCC) is derived to increase the stability margin and damp the filter resonance. The performance in case of current steps and voltage imbalance is tested for the system with stiff DC-link voltage and with regulated DC-link voltage. If the system with stiff DC-link voltage is to be implemented practically, two criterions have been proposed to modify the VCC depending on either the grid regulation or the DG protection regulation. Hence, two controllers are proposed: one to produce symmetrical grid currents and the second to produce symmetrical converter currents. It has been shown that it is not possible to control both grid and converter currents to be symmetrical simultaneously. However, controlling the converter current reduces the ratio of imbalance in the grid current.

To improve the performance in case of unbalanced voltage dips at the grid for the system with weak DC-link voltage, the DVCC is implemented. The grid current commands are derived based on the instantaneous power flow through the system. The power loss in the VSC is neglected and the oscillating power, which is the power at double the fundamental frequency produced due to unbalanced faults, is considered to be supplied from the VSC side. The performance of DVCC is evaluated by calculating the maximum current and peak-to-peak DC-link voltage ripples during all types of unbalanced dips. Compared to the case of L-filter interface system, the currents are almost the same while the DC voltage ripples are slightly increased but still in acceptable range.

The robustness of the controller in the sense of filter parameters variation is tested. The underestimated values of the grid-side inductance (less than 50%) and overestimated values of the VSC-side inductance (more than 120%) leads the system to instability, while the change in inductors' resistances and filter capacitance does not affect the stability within the tested range (10% - 200%).

The VSC connected to a weak grid through an LCL-filter is then considered. A laboratory network model has been used in the analysis to allow future comparison with the experimental work. The voltage regulation limits are calculated to be: 30% of nominal value for the VSC with stiff DC-link voltage, and 4% for the VSC with weak DC-link voltage, for the specified system ratings. A PI-controller is proposed for the regulation of the voltage at the point of common coupling (PCC). It is implemented as an outer control loop, while the main vector current controller (VCC) represents an inner control loop. The controller is tested in case of a load connection/disconnection and balanced voltage dips. It has been shown that it is capable of regulating the PCC voltage within the calculated regulation limits.

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### **5.3 Future work**

The operation of a grid connected voltage source converter (VSC) through LCL-filter in case of weak grid has been examined in case of load connection/disconnection and balanced voltage dips on the grid. The controller has been modified to regulate the voltage at the point of common coupling (PCC) in these cases. However, most dips are unbalanced, resulting in oscillations of double the fundamental frequency in the grid side current, the voltage at the PCC, and the DC-link voltage. Hence, the controller should be modified to eliminate these oscillations and maintain the voltage at the PCC equal to the nominal value. Moreover, the energy transfer from a DG unit to the grid is limited by the operating limits (or ratings) of the VSC system. These limits set the voltage regulation range that the PCC-voltage regulator can achieve, and consequently limit the reliability of the power system experienced by customers. Hence, it is important to investigate how to increase these limits without a significant increase in the total cost. In addition, in linear controllers, such as the controller implemented throughout the thesis, parameter variations, load variations, and input voltage variations are not considered simultaneously. This results in comparatively long transient time. Hence, it is important to investigate if the transient performance of the system will be improved by designing a non-linear controller.

The VSC controller has been designed and verified by using simulation in Matlab/Simulink, for the system connected to a strong grid, and in PSCAD/EMTDC, for the system connected to a strong grid and a weak grid. Comparing equivalent simulation in both programs has been carried out showing a good agreement in the results. However, the simulation should be verified through experimental work to give more practical insight over different conclusions and validate the efficiency of the proposed controller.

Moreover, a variable-speed wind turbine system with full-scale converter interface is considered along the thesis, where the grid-connected converter is supplied by the wind turbine through a diode rectifier with a capacitive DC-link. This scheme is not common to all energy sources used for DGs. An issue to address is if and how the same control techniques can be applied to the grid interface in other DG topologies. This requires more insight into several existing DG sources and how they are interfaced with the power system. Also, the response time of the DG source is of importance because it can limit the transient performance of the system.



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## References

- [1] G. Joos, B.T Ooi, D. McGillis, F.D. Galiana, and R. Marceau, "The potential of distributed generation to provide ancillary services," *IEEE Power Engineering Society Summer Meeting*, 16-20 July 2000, vol. 3, pp. 1762 – 1767.
- [2] T. E. Mcdermott, and R. C. Dugan, "PQ, Reliability and DG," *IEEE Industry Applications Magazine*, vol. 9, no. 5, pp. 17-23, September/October 2003.
- [3] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Systems," *IEEE Trans. on Power Electronics*, vol. 19, no. 5, pp. 1184-1194, September 2004.
- [4] Swedish Energy Agency, Tech. Rep. ET 26:2004, available on line at: [www.stem.se](http://www.stem.se).
- [5] A. Petersson, "Analysis, Modeling and Control of Doubly-Fed Induction Generators for Wind Turbines," Licentiate thesis, Tech. Rep. ISSN 1651-4998, Chalmers University of Technology, Sweden, 2003.
- [6] J. H. R. Enslin, "Interconnection of Distributed Power Inverters with the Distribution Network," *IEEE Power Electronics Society Newsletter*, vol. 15, no. 4, pp. 7-8, Fourth Quarter 2003.
- [7] R. Lawrence and S. Middlekauff, "The New Guy on the Block: Applying distributed generation tools in power design systems," *IEEE Industry Applications Magazine*, vol. 11, no. 1, pp. 54-59, January/February 2005.
- [8] N. Canard, J. F. Dumas and F. Hadjsaid, "Dispersed generation impact on distribution networks," *IEEE Computer Application on Power*, pp. 22-28, April 1999.
- [9] J.H.R. Enslin, and P. J. M. Heskes, "Harmonic Interaction Between a Large Number of Distributed Power Inverters and the Distribution Network," *IEEE Trans. on Power Electronics*, vol. 19, no. 6, pp. 1586-1593, November 2004.
- [10] E. Twining, and D. G. Holmes, "Voltage Compensation in Weak Distribution Networkd using Multiple Shunt Connected Voltage Source Inverters," *IEEE Power Tech Conference*, June 23<sup>rd</sup> – 26<sup>th</sup> 2003, vol. 4.
- [11] M. Bayegan, "A Vision of the Future Grid," *IEEE Power Engineering Review*, December 2001, pp. 10-12.
- [12] CIGRE TF 38.01.10, "Modeling New Forms of Generation and Storage" November 2000.
- [13] M.F. McGranaghan, D.R. Mueller, and M.J Samotyj, "Voltage sags in industrial power systems," *IEEE Transactions on Industry Applications*, vol. 29, no. 2, March-April 1993, pp. 397 –403.
- [14] H.G. Sarmiento, and E. Estrada, "A voltage sag study in an industry with adjustable speed drives," *IEEE Industry Applications Magazine*, vol. 2, no.1, Jan.-Feb. 1996, pp. 16 –19.
- [15] J. Stones, and A. Collinson, "Power Quality," *Power Engineering Journal*, vol. 15, issue 2, April 2001, pp. 58-64.
- [16] Power Standards Lab (PSL), on line: [www.powerstandards.com](http://www.powerstandards.com).
- [17] M.H.J. Bollen, *Understanding power quality problems: voltage sags and interruptions*, New York, IEEE Press, 1999.

- [18] J. Kang, and S. Sul, "Control of Unbalanced Voltage PWM Converter Using Instantaneous Ripple Power Feedback," in *Proc. of 28<sup>th</sup> IEEE Power Electronics Specialists Conference (PESC'97)*, vol. 1, pp. 503-508.
- [19] H.S. Kim, H.S. Mok, G.H. Choe, D.S. Hyun, and S.Y. Choe, "Design of Current Controller for Three-Phase PWM Converter with Unbalanced Input Voltage," *IEEE 29<sup>th</sup> Annual Power Electronics Specialists Conference (PESC'98)*, pp. 503-509.
- [20] G. Saccomando, and J. Svensson, "Transient Operation of Grid Connected Voltage Source Converter Under Unbalanced Voltage Conditions," *IEEE Industry Applications Society Annual Meeting (IAS'01)*, 30 Sept.-4 Oct. 2001, vol. 4, pp. 2419-2424.
- [21] H. Song, and K. Nam, "Dual Current Control Scheme for PWM Converter Under Unbalanced Input Voltage Conditions," *IEEE Trans. on Industrial Electronics*, vol. 46, pp. 953-959, October 1999.
- [22] Y. Suh, V. Tijeras, and T. A. Lipo, "A Nonlinear Control of the Instantaneous Power in dq Synchronous Frame for PWM AC/DC Converter Under Generalized Unbalanced Operating Conditions," *IEEE Industry Applications Society Annual Meeting (IAS'02)*, 13-18 Oct. 2002, vol. 2, pp. 1189-1196.
- [23] L. Malesani, and P. Tomasin, "PWM Current Control Techniques of Voltage Source Converters – A survey," *IEEE Industrial Electronics Conference (IECON'93)*, 15-19 Nov. 1993, vol.2, pp. 670-675.
- [24] M. Jasinski, M. Liserre, F. Blaabjerg, and M. Cichowlas "Fuzzy logic current controller for PWM rectifiers," *IEEE 28th Annual Conference of the Industrial Electronics Society (IECON'02)*, vol.2, 5-8 Nov. 2002, pp.1300 – 1305.
- [25] M. Rukonuzzaman, and M. Nakaoka, "Space voltage vector modulation based voltage source inverter with fuzzy logic current controller," *IEEE International Conference on Industrial Technology*, 19-22 Jan. 2000, vol.1, pp.272 – 277.
- [26] M. Rukonuzzaman, and M. Nakaoka, "Fuzzy logic current controller for three-phase voltage source PWM-inverters," *IEEE Industry Applications Society Annual Meeting (IAS'00)*, 8-12 Oct. 2000, vol.2, pp.1163 – 1169.
- [27] F.D. Kanellos, and N.D. Hatzargyriou, "A new control scheme for variable speed wind turbines using neural networks," *IEEE Power Engineering Society Winter Meeting*, 27-31 Jan. 2002, vol.1, pp.360 – 365.
- [28] H. Bevrani, M. Abrishamchian, and N. Safari-Shad "Nonlinear and linear robust control of switching power converters," *IEEE International Conference on Control Applications*, 22-27 Aug. 1999, vol. 1, pp.808 – 813.
- [29] J. Svensson, "Grid-Connected Voltage Source Converter- Control Principles and Wind Energy Applications," PhD thesis, ISBN: 91-7197-610-8, Chalmers University of Technology, Gothenburg, Sweden, 1998.
- [30] K. Dutton, S. Thompson, B. Barraclough, *The Art of Control Engineering*, Addison-Wesley Longman, 1997.
- [31] G. Saccomando, "Grid-connected VSC operating under voltage disturbance conditions," Chalmers University of Technology, Tech. Rep. ISSN 1401-6176, 2001.
- [32] R. Ottersten, and J. Svensson, "Vector Current Controlled Voltage Source Converter- Deadbeat Control and Saturation Strategies," *IEEE Trans. on Power Electronics*, vol. 17, no. 2, pp. 279- 285, March 2002.
- [33] F. Blaabjerg, E. Chiarantoni, A. Dell'Aquila, M. Liserre, and S. Vergura, "Analysis of the Grid Side Behavior of a LCL-Filter Based Three-Phase Active



- 
- Rectifier,” *IEEE International Symposium on Industrial Electronics (ISIE '03)*, 9-11 June 2003, vol. 2, pp. 775 – 780.
- [34] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, “Stability Improvements of an LCL-filter based Three-phase Active Rectifier,” *Power Electronics Specialists Conference (PESC'02)*, 23-27 June 2002, vol. 3, pp. 1195 - 1201.
- [35] R. Teodorescu, F. Blaabjerg, M. Liserre, and A. Dell'Aquila, “A stable three-phase LCL-filter based active rectifier without damping,” *Industry Applications Conference (IAS'03)*, 12-16 Oct., vol. 3, pp.1552 - 1557.
- [36] M. Liserre, F. Blaabjerg, and S. Hansen, “Design and Control of an LCL-filter Based Three-phase Active Rectifier,” *36<sup>th</sup> Industry Applications Conference (IAS'01)*, 30<sup>th</sup> Sept.-4<sup>th</sup> Oct 2001, vol.1, pp.299 – 307.
- [37] E. J. Bueno, F. Espinosa, F. J. Rodriguez, J. Urena, and S. Cobrecas, “Current Control of Voltage Source Converters Connected to the Grid Through an LCL-filter,” *35<sup>th</sup> IEEE Power Electronics Specialists Conference (PESC'04)*, 20-25 June 2004, vol. 1, pp 68-73.
- [38] V. Blasko, and V. Kaura, “A Novel Control to Actively Damp Resonance in Input LC filter of a Three-phase Voltage Source Converter,” *IEEE Trans. on Industry Applications*, vol. 33, issue 2, pp. 542 – 550, March-April 1997.
- [39] E. Twining, D.G. Holmes, “Grid current regulation of a three-phase voltage source inverter with an LCL input filter,” *Power Electronics Specialists Conference (PESC 02)*, 23-27 June 2002, vol. 3, pp.1189 – 1194.
- [40] M. Lindgren, “Modeling and Control of Voltage Source Converters Connected to the Grid,” PhD Thesis, Chalmers University of Technology, Gothenburg, Sweden, November 1998.
- [41] M. Bojrup, “Advanced Control of Active Filters in a Battery Charger Application, PhD thesis,” Lund University, Sweden 1999.
- [42] M. Malinowski, and S. Bernet, “Simple Control Scheme of PWM Converter Connecting wind Turbine with Grid- Simulation Study,” *Nordic Wind Power Conference*, 1-2 March 2004, Chalmers University of Technology, Sweden.
- [43] C. L. Phillips and H. T. Nagle, *Digital Control Systems Analysis and Design*, Prentice-Hall, 1995.
- [44] K. Ogata, *Discrete-Time Control Systems*, Prentice-Hall, 1995.
- [45] H. Bindner, “Power Control for Wind Turbines in Weak Grids: Concepts Development,” Tech. Rep., ISBN 87-550-2550-1, Riso National Laboratory, Roskilde, March 1999.
- [46] E. Twining, M.J. Newman, P.C. Loh, and D.G. Holmes, “Voltage Compensation in Weak Distribution Networks Using a D-STATCOM,” *Power Electronics and Drive Systems Conference (PEDS'03)*, 17-20 Nov. 2003, vol. 1, pp. 178 – 183.
- [47] G. Ledwich and H. Sharma, “Connection of Inverters to a Weak Grid,” *Power Electronics Specialists Conference (PESC'00)*, 18-23 June 2000, vol. 2, pp. 1018 – 1022.
- [48] F. D. Kanellos and N.D. Hatziagyriou, “The Effect of Variable-Speed Wind Turbines on the Operation of Weak Distribution Networks,” *IEEE Trans. on Energy Conversion*, vol. 17, issue 4, pp. 543 – 548, Dec. 2002.
- [49] C.V. Nayar, “Control and Interfacing of Bi-directional Inverters for Off-Grid and weak Grid Photovoltaic Systems,” *IEEE Power Engineering Society Summer Meeting*, 16-20 July 2000, vol. 2, pp. 1280 – 1282.
- [50] H. Dehbonei, C. Nayar, L. Borl, “A combined Voltage Controlled and Current Controller “Dual Converter” for a Weak Grid Connected Photovoltaic System with

- Battery Energy Storage,” *Power Electronics Specialists Conference (PESC’02)*, 23-27 June 2002, vol. 3, pp. 1495 – 1500.
- [51] R. Teodorescu, F. Blaabjerg, “Flexible Control of Small Wind Turbines With Grid Failure Detection Operating in Stand-Alone and Grid-Connected Mode,” *IEEE transactions on Power Electronics*, vol. 19, no. 5, September 2004.
- [52] K. Macken, and M. H. J. Bollen, ”Mitigation of Voltage Dips Through Distributed Generation Systems,” *IEEE trans. on Industry Applications*, vol. 40, no. 6, pp. 1686-1693, November/December 2004.
- [53] T. M. L. de Assis, E. H. Watanabe, L. A. S. Pilpito, and R. B. Sollero, “A New Technique to Control Reactive Power Oscillations Using STATCOM,” *10th International Conference on Harmonics and Quality of Power*, 6-9 Oct. 2002, vol. 2, pp. 607 – 613.
- [54] W.H. Press, S.A. Teukolsky, W.T. Vetterling, B.P. Flannery, *Numerical Recipes in C: The Art of Scientific Computing*, 2<sup>nd</sup> edition, Cambridge University Press, 1992. Available on-line at [www.nr.com](http://www.nr.com).
- [55] Danish Wind Industry Association, available on line at [www.windpower.org](http://www.windpower.org).
- [56] S. Lundgren, “Configuration Study of Large Wind Parks,” Tech. Rep., ISSN 1651-4998, Licentiate Thesis, Chalmers University of Technology, Sweden 2003.
- [57] M. I. Marei, E. F. El-Saadany and M. M. A. Salama, “Flexible Distributed Generation,” *IEEE Power Engineering Society Summer Meeting*, vol. 1, 21-25 July 2002, pp. 49 – 53.
- [58] D.R. Criswell, and R.D. Waldron, “Lunar System to Supply Solar Electric Power to Earth,” *Energy Conversion Engineering Conference (IECEC’90)*, 12-17 August 1990, vol. 1, pp. 61-71.
- [59] M. Bongiorno, Control of Voltage Source Converter for Voltage Dip Mitigation in Shunt and Series Configuration, Licentiate thesis, ISSN 1651-4998, Chalmers University of Technology, Gothenburg, Sweden 2004.

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## Appendix A: Transformations for Three-phase

### Systems

This appendix reports necessary transformations to calculate voltage vectors from three-phase quantities and vice versa. Expressions of voltage and current vectors both in the fixed and rotating reference frames are given in the general case of unsymmetrical three-phase quantities.

#### A.1 Transformation of three-phase quantities into vectors

A three-phase positive system constituted by the three quantities  $x_1(t)$ ,  $x_2(t)$  and  $x_3(t)$  can be transformed into a vector in a complex reference frame, usually called  $\alpha\beta$ -frame, by applying the transformation defined by:

$$\underline{x} = x_\alpha(t) + jx_\beta(t) = \frac{2}{3}K \left[ x_1(t) + x_2(t) \cdot e^{j\frac{2}{3}\pi} + x_3(t) \cdot e^{j\frac{4}{3}\pi} \right] \quad (\text{A.1})$$

where the factor  $K$  is usually taken equal to  $\sqrt{\frac{3}{2}}$  for ensuring power invariance between the two systems. Equation (A.1) can be expressed as a matrix equation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \mathbf{C}_{23} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \quad (\text{A.2})$$

where:

$$\mathbf{C}_{23} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \quad (\text{A.3})$$

The inverse transformation is given by:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C}_{32} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \quad (\text{A.4})$$

where:

$$\mathbf{C}_{32} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \quad (\text{A.5})$$

This holds under the assumption that the sum of the three quantities is zero. Otherwise, there will also be a constant (zero-sequence) component. In the latter case, (A.2) and (A.4) become:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} = \mathbf{C}_{230} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} \quad (\text{A.6})$$

and for the inverse transformation:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} = \mathbf{C}_{320} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0(t) \end{bmatrix} \quad (\text{A.7})$$

with the two matrixes given by:

$$\mathbf{C}_{230} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \end{bmatrix} \quad (\text{A.8})$$

and

$$\mathbf{C}_{320} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{6}} \end{bmatrix} \quad (\text{A.9})$$

## A.2 Transformation from fixed to rotating coordinate system

Let the vectors  $\underline{v}(t)$  and  $\underline{w}(t)$  rotate in the  $\alpha\beta$ -frame with the angular frequency  $\omega(t)$  in the positive (counter-clockwise) direction. If the vector  $\underline{w}(t)$  is taken as the  $d$ -axis of a  $dq$ -frame that rotates in the same direction with the same angular frequency  $\omega(t)$ , both vectors  $\underline{v}(t)$  and  $\underline{w}(t)$  will appear as fixed vectors in that frame. The

components of  $\underline{v}(t)$  in the  $dq$ -frame are thus given by the projections of the vector on the direction of  $\underline{w}(t)$  and on the orthogonal direction, as illustrated in Fig.A.1.

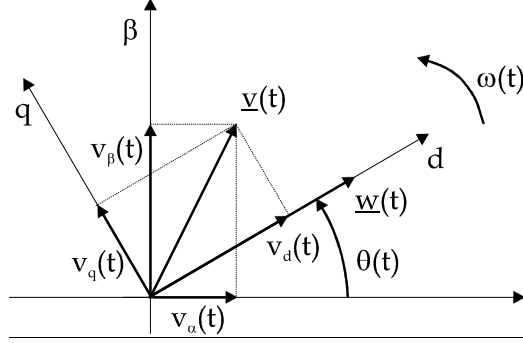


Fig.A.1. Relation between the  $\alpha\beta$ -frame and the  $dq$ -frame.

The transformation can be written in vector form as:

$$\underline{v}_{dq}(t) = e^{-j\theta(t)} \cdot \underline{v}_{\alpha\beta}(t) \quad (\text{A.10})$$

with the angle  $\theta(t)$  in Fig.A.1 given by

$$\theta(t) = \theta_0(t) + \int_0^t \omega(\tau) d\tau \quad (\text{A.11})$$

and the inverse transformation is defined by the expression

$$\underline{v}_{\alpha\beta}(t) = e^{j\theta(t)} \cdot \underline{v}_{dq}(t) \quad (\text{A.12})$$

The components in the  $dq$ -frame can be determined from Fig.A.1. In matrix form, the transformation from the  $\alpha\beta$ -frame to the  $dq$ -frame can be written as:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \mathbf{R}(-\theta(t)) \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \quad (\text{A.13})$$

and the inverse is given by

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \mathbf{R}(\theta(t)) \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \quad (\text{A.14})$$

where the projection matrix is

$$\mathbf{R}(\theta(t)) = \begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) \\ \sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \quad (\text{A.15})$$

## A.2.1 Transformations for voltage and current vectors in the $dq$ -system

Suppose a symmetrical sinusoidal three-phase voltage with angular frequency  $\omega(t)$  is transformed into a vector  $\underline{u}(t) = u_\alpha(t) + ju_\beta(t)$  in the  $\alpha\beta$ -frame. When transforming it further to the  $dq$ -frame, the  $q$ -axis in the  $dq$ -frame is normally defined as parallel to

the voltage vector  $\underline{u}(t)$ . This definition originates from a flux vector parallel to the  $d$ -axis in the  $dq$ -frame. The voltage vector is proportional to the time derivative of the flux vector. As a consequence of the chosen reference vector, the voltage vector  $\underline{u}(t)$  will only contain a  $q$ -component in the  $dq$ -frame. The transformation equation for a current vector from the  $\alpha\beta$ -frame to the  $dq$ -frame becomes, in matrix form:

$$\begin{bmatrix} u_d(t) \\ u_q(t) \end{bmatrix} = \mathbf{R} \left( - \left( \omega t - \frac{\pi}{2} \right) \right) \cdot \begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} \quad (\text{A.16})$$

and the inverse

$$\begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} = \mathbf{R} \left( \omega t - \frac{\pi}{2} \right) \cdot \begin{bmatrix} u_d(t) \\ u_q(t) \end{bmatrix} \quad (\text{A.17})$$

The transformation from the  $\alpha\beta$ -frame into the  $dq$ -frame for current vectors is the same as for voltage vectors.

### A.3 Voltage vectors for unsymmetrical three-phase systems

#### A.3.1 Expressions in the $\alpha\beta$ -coordinate system

The phase voltages for a three-phase system can be written as:

$$\begin{aligned} e_a(t) &= E_a(t) \cdot \cos(\omega t - \varphi_a) \\ e_b(t) &= E_b(t) \cdot \cos\left(\omega t - \frac{2}{3}\pi - \varphi_b\right) \\ e_c(t) &= E_c(t) \cdot \cos\left(\omega t - \frac{4}{3}\pi - \varphi_c\right) \end{aligned} \quad (\text{A.18})$$

where  $E_a(t)$ ,  $E_b(t)$  and  $E_c(t)$  are the amplitudes of the three-phase voltages,  $\varphi_a$ ,  $\varphi_b$  and  $\varphi_c$  are the phase angles of the three-phase voltages, and  $\omega$  is the angular frequency of the system.

If the amplitudes  $\hat{e}_a(t)$ ,  $\hat{e}_b(t)$  and  $\hat{e}_c(t)$  are unequal, the voltage vector can be written as the sum of two vectors rotating in opposite directions and interpreted as positive- and negative-sequence vectors:

$$\underline{e}_{\alpha\beta}(t) = E_p e^{j(\omega t + \varphi_p)} + E_n e^{-j(\omega t + \varphi_n)} \quad (\text{A.19})$$

where  $E_p$  and  $E_n$  are the amplitudes of positive- and negative-sequence vectors, respectively, and the corresponding phase angles are denoted by  $\varphi_p$  and  $\varphi_n$ . To determine amplitudes and phase angles of positive- and negative-sequence vectors in (A.19), a two-step solving technique can be used. First, the phase shifts are set to zero, so that the amplitudes  $E_p$  and  $E_n$  can easily be detected. In the next step, the phase shifts  $\varphi_p$  and  $\varphi_n$  are determined.

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### A.3.2 Expressions in the $dq$ -coordinate system

When transforming an unsymmetrical three-phase voltage into the  $dq$ -coordinate system, two rotating frames are used, accordingly. They are called positive and negative synchronous reference frames and denoted by  $dqp$ - and  $dqn$ -, respectively. They can be defined by the transformations:

$$\underline{e}_{dqp}(t) = e^{-j\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \quad (\text{A.20})$$

$$\underline{e}_{dqn}(t) = e^{+j\theta(t)} \cdot \underline{e}_{\alpha\beta}(t) \quad (\text{A.21})$$

where the transformation angle  $\theta(t)$  is locked to the positive phase sequence flux vector. The positive phase sequence vector in the  $dqp$ -coordinate system is expressed as:

$$e_{dp} + je_{qp} = -E_p \sin(\varphi_p) + jE_p \cos(\varphi_p) \quad (\text{A.22})$$

and the negative phase sequence vector in the  $dqn$ -coordinate system is given by

$$e_{dn} + je_{qn} = -E_n \sin(\varphi_n) + jE_n \cos(\varphi_n) \quad (\text{A.23})$$

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## Appendix B: Per Unit Base Values

The base values for voltage and current are equal to:

$$E_{\text{base}} = 400 \text{ V}$$

$$I_{\text{base}} = 100 \text{ A}$$

The base value of the impedance is then obtained according to:

$$Z_{\text{base}} = \frac{E_{\text{base}}}{\sqrt{3}I_{\text{base}}} = 2.3\Omega$$

The base values for the DC-link voltage and current are equal to:

$$U_{\text{DC,base}} = 650 \text{ V}$$

$$I_{\text{DC,base}} = \frac{\sqrt{3}E_{\text{base}}I_{\text{base}}}{U_{\text{DC,base}}} = 107 \text{ A}$$