CHALMERS

Control of Switch-mode Power Supplies

A digital approach for half-bridge converters

Master of Science Thesis

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Abstract

In this master thesis a digital controller for a switch-mode power supply (SMPS) based on a half-bridge topology has been implemented. The SMPS originally has an analog control board. This original control board has been removed and replaced by a digital controller. Hardware for output voltage and current measurement was constructed as well as gate driving circuitry.

Control design was performed based on an average model for the half-bridge. Two different controllers were designed where one regulates the output voltage and the other regulates the output current. The controllers have been implemented digitally using a STM32 microcontroller from STMicroelectronics. The developed digital controllers has been tested to investigate the performance of the system. The thesis work also contains theoretical studies on paralleled SMPS in system.

Test results show that the SMPS, controlled by the digital controller, can deliver constant voltage and constant current. When combining the two modes, a voltage source with current limiting or a current source with voltage limiting is obtained. However, the noisy environment due to the switching signals makes measurements questionable and further investigations of the performance of the controllers should be done.

Sammanfattning

En digital regulator för ett switchat spänningsaggregat baserat på en halvbrygga har konstruerats i detta examensarbete. Det ordinarie styrkortet på spänningsaggregatet är analogt. Detta styrkort har bytts ut mot en digital lösning. Hårdvara för mätning av spänning och ström samt gate-drivning har konstruerats.

Regulatordesign har gjorts baserat på en tillståndsmodell över halvbryggan. Två regulatorer designades för spänning- respektive strömreglering. Regulatorerna har implementerats digitalt med hjälp av en STM32 microprocessor från STMicroelectronics. De utvecklade regulatorerna testades för att undersöka egenskaperna hos systemet. Examensarbete innehåller även teoretiska studier om parallellkopplade spänningsaggregat.

Resultat från tester visar att spänningsaggregatet reglerat av de digitala regulatorerna kan leverera konstant spänning och ström. Genom att kombinera de två regulatorerna erhålls en spänningskälla med strömbegränsning alternativt en strömkälla med spänningsbegränsning. På grund av den brusiga miljön till följd av snabba switch-omslag kan mätresultaten ifrågasättas. Vidare utvärdering av de digitala regulatorerna bör därför göras.

Preface

This master thesis was performed at the department of Signals and System and the department of Energy and Environment during the winter of 2008/2009. The practical work was performed at the company Alelion Batteries AB.

Alelion Batteries AB was formed in 2006 and is a spinoff from ETC (EnergiTekniskt Centrum) which is an R & D company in advanced energy technology. Alelion Batteries AB is based in Nödinge just north of Gothenburg. The company is specialized in products and services using modern energy and electronics technology where mobility and "green" solutions are key words. They have the entire chain from definition to delivery via development as their area of operation. The Li-ion battery is a fundamental part of their products.

The writers would like to thank their supervisors Jonas Sjöberg and Torbjörn Thiringer at Chalmers University of Technology and Dag Lundström at Alelion Batteries AB. The writers would also like to thank the personell at Alelion Batteries AB for providing their knowledge during this thesis work.

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Contents

1 Introduction

Alelions Batteries AB are interested in developing a module system of switch-mode power supplies (SMPS). The primary purpose will be charging of their own Li-Ion batteries. A module system is a cost efficient way to build power supplies with different power ratings since only one standard converter needs to be produced. A number of these standard converters can then be connected to achieve desired power rating. The system approch also gives the possibility for a redundant system.

The purpose of this master thesis is to construct an embedded platform and control algorithms for a SMPS. The algorithms should be designed for both constant voltage and constant current control. A combination of these two modes can then be used for Li-Ion battery charging. Possible solutions for connecting multiple power supplies in a system will be investigated.

The embedded platform shall be based around a STM32 32-bit microcontroller which is one of the standard microcontrollers used at the company. The algorithms will be evaluated using a 400 W SMPS available from the electronics magazine Elektor. This power supply, called SAPS-400, is based on a half-bridge topology.

The master thesis will present the theory behind the SMPS and especially the half-bridge topology in Chapter 2. This chapter will also present the theory of current sharing for a system of paralleled SMPS. Finally, the chapter will present the control theory used in the controller design and some features of microcontrollers. Chapter 3 describes the experimental setup and the hardware for the SAPS-400 module, the STM32 development board and the developed interface circuit between them. In Chapter 4, the design and implementation of the control algorithms is presented. The test results are presented in Chapter 5. Finally, Chapter 6 presents conclusions and suggestions for future work.

2 Theory

In this chapter the theory behind the switch-mode power supplies and especially the half-bridge converter is presented. The theory used when designing controllers for a half-bridge converter along with some important microcontroller features is also presented.

2.1 Switch-mode power supplies

Switch-mode power supplies (SMPS) are very common today due to their advantages compared to linear supplies. The main advantages are high efficiency, low cost, low weight and size. However, one drawback is that they require a more complex design.
There are several topologies used in SMPS. Different topologies are suitable for different power ratings. The most common topology is the flyback converter. The flyback converter has the advantages of low component cost and is used for small power ratings, usually less than 150W. The half- and full-bridge converters are more expensive topologies but provide a higher power rating. The half-bridge is suitable in the power range of 250-1000W. The more expensive full-bridge is suitable when the power rating is greater than 1000W [1]. Details about the half-bridge converter are described in the following sections.

2.1.1 Basic structure of a half-bridge converter

Figure 2.1 shows the basic circuit of a half-bridge converter. The two capacitors C_1 and C_2 are used as a voltage divider, to keep the voltage across the primary windings of the transformer at half the input voltage V_i. The switches can be e.g. MOSFETs or Bipolar transistors. The switches, $Q_1$and Q_2, alternately apply positive or negative voltage V_p to the primary side of the transformer creating a square-wave AC. This square-wave is then stepped either up or down by the high frequency transformer. During the on-time of the switches energy is transferred from the primary side to the secondary side. The square-wave is then rectified by the diodes, D_1 and D_2, and filtered through an LC-filter to create the output DC voltage V_o .

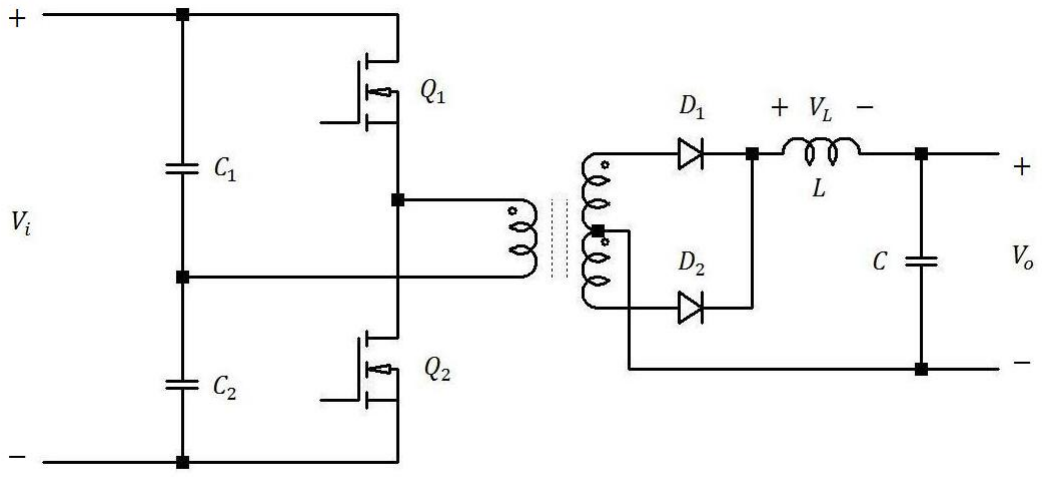

Figure 2.1: *Basic half-bridge converter topology.*

The half-bridge converter operates in four modes. In mode 1, Q_1 is on and Q_2 is off. During this mode the voltage across the primary winding is V_p. This voltage causes the current i_p in the primary winding to build up and energy is transferred to the secondary winding and onto the LC-filter and the output load. The rectifying diode D_1 is conducting while D_2 is reversed biased causing the polarity of the output voltage to be positive. The voltage across the secondary winding is calculated as

$$V_s = N\frac{V_i}{2} \tag{2.1}$$

where N is the ratio between the number of turns in the secondary and the primary side of the transformer. Hence,

$$N = \frac{N_s}{N_p}. \tag{2.2}$$

Using Kirchhoff's second law on the secondary gives,

$$V_s = V_L + V_o \tag{2.3}$$

where V_L is the voltage across the output inductor and V_o is the output voltage. This is under the assumption that the diodes are ideal.

The current in the output inductor L increases during mode 1 given by

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{1}{L}\left[N\frac{V_i}{2} - V_o\right] \tag{2.4}$$

where (2.2) and (2.3) have been used.

At the end of mode 1, at $t = dT_s$ where d is the duty cycle and T_s is the switching period, the peak inductor current is given by

$$I_{L(peak)} = I_L(t = 0) + \frac{1}{L}\left[N\frac{V_i}{2} - V_o\right]dT_s\ . \tag{2.5}$$

In mode 2, both of the switches Q_1 and Q_2 are off and the rectifying diodes are conducting the magnetizing inductor current that was stored during the previous mode. The voltage V_s on the secondary winding is now zero. Using Kirchhoff's second law gives,

$$0 = V_L + V_o. \tag{2.6}$$

During mode 2, which is during $dT_s < t \leq T_s/2$, the inductor current will fall with the slope given by

$$\frac{di_L}{dt} = -\frac{V_o}{L}. \tag{2.7}$$

This gives

$$I_L(T_s/2) = I_{L(peak)} - \frac{V_o}{L}\left(\frac{T_s}{2} - dT_s\right). \tag{2.8}$$

In mode 3, Q_1 is off and Q_2 is on. The voltage across the primary winding is now $-V_p$. This leads to that D_2 will conduct and D_1 will be forward biased. Thus, the inductor current and the output voltage will be the same as in mode 1. In the same way mode 4, where Q_1 and Q_2 are both off, will be similar to mode 2. Figure 2.2 shows the associated waveforms in steady-state.

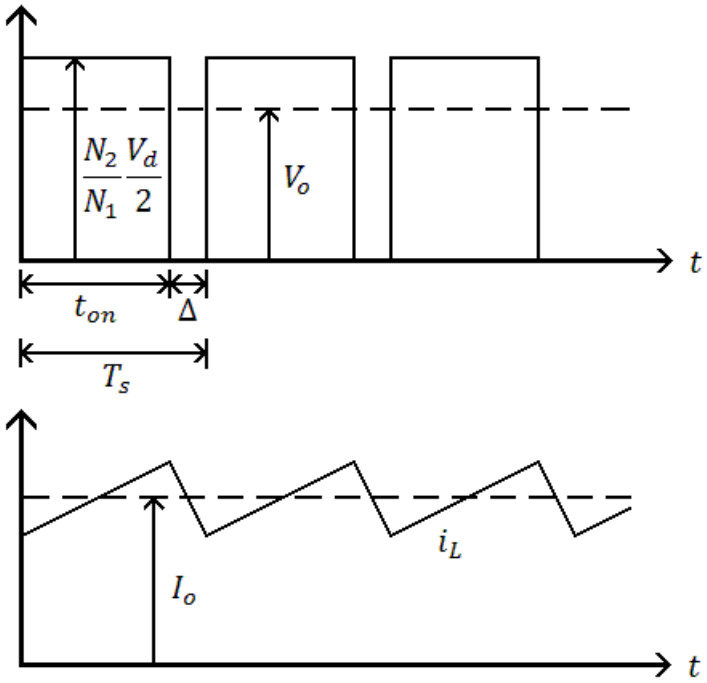

Figure 2.2: *Steady-state waveforms for Half-Bridge topology.*

By using (2.5) and (2.7) and integrating the voltage across the inductor over one switching period the output voltage is obtained as

$$V_o = NV_i d. \tag{2.9}$$

It is seen from (2.9) that the output voltage in steady state can be controlled by changing the duty-cycle assuming that the input voltage is constant [2].

2.1.2 Small-signal average model

Assuming the state variables to be the current, i_L, through the output inductor and the voltage, u_C, across the output capacitor, the state equations for the half-bridge converter can be written as

$$\dot{\boldsymbol{x}} = A_1\boldsymbol{x} + B_1V_s, \qquad \text{during } dT_s \tag{2.10}$$

and

$$\dot{\boldsymbol{x}} = A_2\boldsymbol{x} + B_2V_s, \qquad \text{during } (1-d)T_s. \tag{2.11}$$

Here, $A_1$and A_2 are state matrices and B_1 and B_2 are vectors. V_s is voltage across the secondary winding of the high-frequency transformer. Using the state variables, the output signal, y, can be written as

$$y = C_1\boldsymbol{x}, \qquad \text{during } dT_s \tag{2.12}$$

and

$$y = C_2\boldsymbol{x}, \qquad \text{during } (1-d)T_s. \tag{2.13}$$

Depending on the value of the C_1 and C_2 matrices, the output can be either the voltage, current or a linear combination of the voltage and current.

Time weighting and averaging (2.10)-(2.13) gives

$$\dot{\boldsymbol{x}} = [A_1 d + A_2(1-d)]V_d + [B_1 d + B_2(1-d)]V_s, \tag{2.14}$$

and

$$y = [C_1 d + C_2(1-d)]\boldsymbol{x}. \tag{2.15}$$

Equations (2.14) and (2.15) are the average circuit description during a switching period. Equation (2.14) and (2.15) are then used to determine the transfer function of the power stages. Details can be found in [3]. The transfer function of the power stages can be written as

$$T_p(s) = \frac{\tilde{y}(s)}{\tilde{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)\boldsymbol{X} + (B_1 - B_2)V_s] + (C_1 - C_2)\boldsymbol{X}. \tag{2.16}$$

Here,

$$A = A_1 d + A_2(1-d) \tag{2.17}$$

and

$$C = C_1 d + C_2(1-d). \tag{2.18}$$

During the on-time of the switch, that is, $0 < t \leq dT_s$, the half-bridge converter can be represented by the circuit in Figure 2.3.

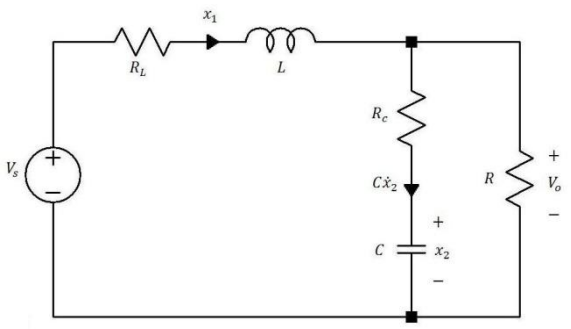

Figure 2.3: *Half-bridge converter during on-time of the switch.*

Using the state vector $\boldsymbol{x} = [x_1 \ x_2]^T = [i_L \ u_C]^T$ and applying Kirchhoff's laws on the circuit in Figure 2.3 gives

$$-V_s + L\dot{x}_1 + R_L x_1 + R(x_1 - C\dot{x}_2) = 0 \tag{2.19}$$

and

$$-x_2 - CR_c\dot{x}_2 + R(x_1 - C\dot{x}_2) = 0 \tag{2.20}$$

Using (2.19) and (2.20) and solving for $\dot{x}_1$ and $\dot{x}_2$ gives the state space equation

$$\dot{\boldsymbol{x}} = \underbrace{\begin{bmatrix} \frac{-R_c \cdot R - R_L \cdot R - R_c \cdot R_L}{L \cdot (R_c + R)} & \frac{-R}{L \cdot (R_c + R)} \\ \frac{R}{C \cdot (R_c + R)} & \frac{-1}{C \cdot (R_c + R)} \end{bmatrix}}_{A_1} \boldsymbol{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B_1} V_s \tag{2.21}$$

which is valid during the on-time of the switch. During $d \cdot T_s < t \leq T_s$, when the switch is off, the power stage of the half-bridge converter can be represented by the circuit in Figure 2.4.

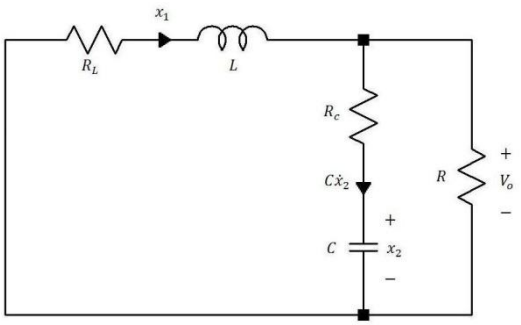

Figure 2.4: *Half-bridge converter during off-time of the switch.*

Again, using the same state vector as earlier, applying Kirchhoff's laws on the circuit gives

$$L\dot{x}_1 + R_L x_1 + R(x_1 - C\dot{x}_2) = 0 \tag{2.22}$$

and

$$-x_2 - CR_c\dot{x}_2 + R(x_1 - C\dot{x}_2) = 0. \tag{2.23}$$

Using (2.22) and (2.23) and solving for $\dot{x}_1$ and $\dot{x}_2$ gives the state space equation

$$\dot{\boldsymbol{x}} = \underbrace{\begin{bmatrix} \frac{-R_c \cdot R - R_L \cdot R - R_c \cdot R_L}{L \cdot (R_c + R)} & \frac{-R}{L \cdot (R_c + R)} \\ \frac{R}{C \cdot (R_c + R)} & \frac{-1}{C \cdot (R_c + R)} \end{bmatrix}}_{A_2} \boldsymbol{x} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{B_2} V_s. \tag{2.24}$$

This equation is valid during the off-time of the switch.

By comparing (2.21) and (2.24) it is seen that $A_1 = A_2$ and that $B_2 = 0$. Using $A_1 = A_2$ in (2.17) gives

$$A = A_1. \tag{2.25}$$

Since the output signal is the same in both the on- and off-time of the switch, (2.18) gives

$$C = C_1 = C_2. \tag{2.26}$$

If the output voltage V_o is the output signal, Kirchhoff's law applied on the circuit in Figure 2.4 and using (2.21) gives

$$\begin{aligned} y = V_o &= u_{R_C} + u_C = R_C C \frac{du_C}{dt} + u_C \\ &= R_C C \dot{x}_2 + x_2 = \frac{R_C \cdot R}{R_C + R} x_1 + \frac{R}{R_C + R} x_2. \end{aligned} \tag{2.27}$$

Finally using (2.27) in (2.12) the output vector is given as

$$y = \underbrace{\begin{bmatrix} \frac{R_C \cdot R}{R_C + R} & \frac{R}{R_C + R} \end{bmatrix}}_{C_v} \boldsymbol{x}. \tag{2.28}$$

If instead the output current is the output signal, Kirchhoff's laws and (2.21) give

$$\begin{aligned} y = i_o &= i_L - i_C = i_L - C \frac{du_C}{dt} \\ &= x_1 - C \dot{x}_2 = \frac{R_C}{R_C + R} x_1 + \frac{1}{R_C + R} x_2. \end{aligned} \tag{2.29}$$

The output vector can in this case be identified as

$$y = \underbrace{\begin{bmatrix} \frac{R_C}{R_C + R} & \frac{1}{R_C + R} \end{bmatrix}}_{C_c} \boldsymbol{x}. \tag{2.30}$$

A reasonable assumption is that $R_C \ll R$. Using this assumption the simplified state matrix becomes

$$A \approx \begin{bmatrix} \frac{-R_C - R_L}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{C \cdot R} \end{bmatrix}. \tag{2.31}$$

Using the same assumption, the simplified output vectors becomes

$$C_v \approx [R_C \quad 1] \tag{2.32}$$

and

$$C_c \approx \begin{bmatrix} \frac{R_C}{R} & \frac{1}{R} \end{bmatrix}. \tag{2.33}$$

Now using (2.21), (2.31) and (2.32) in (2.16) yield the transfer function from duty-cycle to output voltage as

$$T_{P_V}(s) = \frac{1+sR_cC}{LC\left(s^2+\left(\frac{1}{CR}+\frac{R_C+R_L}{L}\right)s+\frac{1}{LC}\right.}V_s. \quad (2.34)$$

The transfer function $T_{P_C}(s)$ from duty-cycle to output current is obtained by using (2.21), (2.31) and (2.33) in (2.16)

$$T_{P_C}(s) = \frac{1+sR_cC}{RLC\left(s^2+\left(\frac{1}{CR}+\frac{R_C+R_L}{L}\right)s+\frac{1}{LC}\right.}V_s. \quad (2.35)$$

2.2 SMPS in paralleled system

The main objective when connecting multiple SMPS in parallel is to increase the output power and to achieve redundancy for the system. The system should be able to retain functionality in case of failure in one or more individual converters as long as the remaining converters can deliver sufficient output power. A paralleled system of converters has a number of advantages compared to a single high power converter. The most important advantages are higher efficiency, better dynamic response and better load regulation [4].

A desirable characteristic of a paralleled system is that all converters share the load current equally. Due to tolerances in the converters they are usually not identical. If no special provisions are made it is possible that one or more converters have an excessive load current. This will cause higher thermal stress and therefore reduce the redundancy for the system. The redundancy can be defined as the ability of a system to function even if some part of it failures. Hence, an important challenge is to achieve good current sharing between the converters. There are a number of methods for achieving current sharing when connecting SMPS in system and some of these methods are described in the following sections.

2.2.1 Droop methods

A droop method is a simple way to achieve current sharing when paralleling converters. It is an open loop method which is used to set the impedance of the output. Due to the impedance, the voltage will drop at higher currents. The current sharing is poor at low current levels, but performs better at higher levels. Higher impedance gives better current sharing but the load regulation performance will be decreased. The advantages are simple implementation and no requirements for connections between the converters.

2.2.2 Active current sharing

To achieve better current sharing compared to droop methods, active current sharing can be used. There are several methods when considering active current sharing. Control structures are different ways to implement the controller hardware and are described in section 2.2.2.1. Different current programming methods are then used to determine how the current sharing should be performed and are described in section 2.2.2.2.

2.2.2.1 Control structures

Three common control structures used for current sharing are inner loop, outer loop and external controller.

2.2.2.1.1 Inner loop

This control structure uses only one voltage controller for all converters. A block diagram over the structure can be seen in Figure 2.5. The output current for each converter is measured and fed to the current programming block. This block calculates how the output current should be distributed for each converter. The output voltage is measured at one point where all converters are merged. The output error, which is defined as the difference between the reference voltage and the output voltage, is then used by the voltage controller, $G(s)$, to calculate a common control signal. The output from the current programming block is then added to the common control signal to obtain an individual control signal for each converter.

The advantages with the method are stable current sharing and good output voltage regulation. This is due to that, the inner loop regulates the current without affecting the outer voltage loop. The drawbacks are poor redundancy and less modularity of the system. If the common voltage loop fails there is no voltage control for the converters.

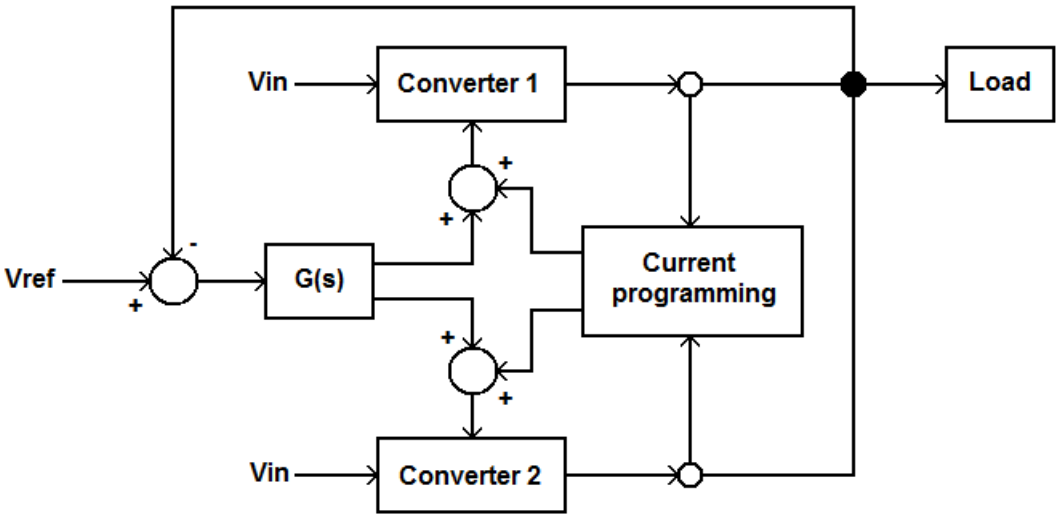

Figure 2.5: *Basic structure of inner loop current sharing.*

2.2.2.1.2 Outer loop

This control structure has an individual feedback and reference voltage for every converter in the system. A block diagram of the structure can be seen in Figure 2.6. Each converter is controlled by an own voltage controller $G(s)$. The output current for each converter is measured and fed to the current programming block. This block calculates how the output current should be distributed for each converter. The output from the current programming block is then added to the individual voltage references to produce a new reference signal.

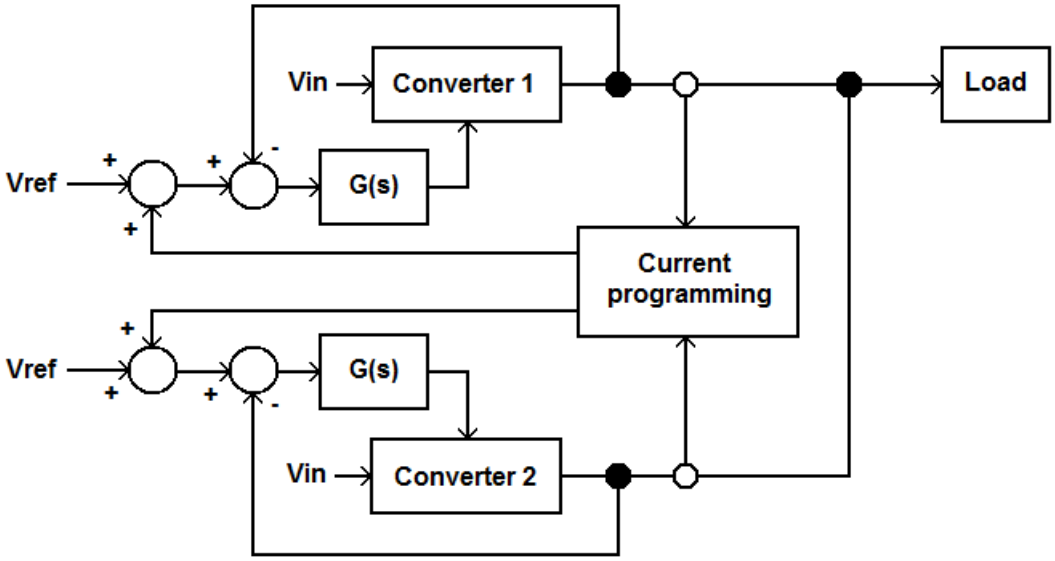

Figure 2.6: *Basic structure of outer loop current sharing.*

The advantages with this method are good modularity, flexibility to expand the system, and good redundancy due to the individual feedbacks. The drawbacks are risk for instability at transients and limited gain for the voltage feedback. The instability is caused by the introduction of the current sharing error into the voltage control loop.

2.2.2.1.3 External controller

This control structure uses an external controller. A block diagram of the structure can be seen in Figure 2.7. The output current and voltage signal for all individual converters are measured and fed to the external controller. This information is then used to determine individual control signals for each converter. The external controller can also provide clock signals for the converters. If the clocks then are phased, the ripple in the output voltage can be dramatically reduced.

The advantages for this method are easy implementation of active current sharing, good current and voltage regulation and ripple reduction by phased clocks. The drawbacks are more interconnections and less modularity. The redundancy is also reduced due to the many interconnections and the fact that only one controller is used.

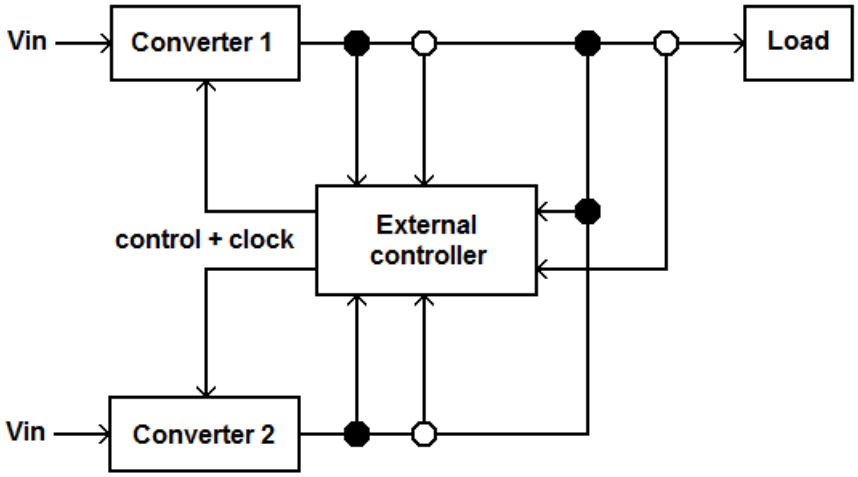

Figure 2.7: *Basic structure of external controller current sharing.*

2.2.2.2 Current programming

The current programming methods determine how the current sharing should be performed. Average current uses the average current for all converters and master slave programming uses the current from only one converter.

2.2.2.2.1 Average current programming

In average current programming, the output current from all converters are used to determine the average current for the system. The current from each converter is weighted differently depending on the power rating of the converter. The weighted current is then compensated by the output current for the converter to obtain the current sharing signal.

2.2.2.2.2 Master-slave programming

In master-slave current programming only one converter determines the current reference. There are different methods to determine the master converter. One method is a dedicated master where only one converter is assigned to be master. The drawback is the redundancy. If the master fails, the system will also fail. Another method is to use a rotating master where the master jumps between the converters controlled by specific control logic. One advantage compared with the dedicated master is better redundancy. The drawbacks are risk for voltage disturbances when the master changes and complicated implementation. A third method is to use an automatic master, where the converter that supplies the highest current becomes the master. The automatic master solution has advantages over both the average current and the other master-slave methods. The method has high redundancy and it is easy to expand or modify the system.

2.3 Control theory

The method used when designing a controller for a half-bridge converter is described in this section. The discretization method used together with an integrator windup solution are also presented.

2.3.1 The K-factor approach

When designing controllers for half-bridge converters the K-factor approach can be used [5]. This method gives the system with a determined crossover frequency and phase margin and results in a controller on the form

$$G_C(s) = \frac{k_c}{s}\frac{\left(1+\frac{s}{\omega_z}\right)^2}{\left(1+\frac{s}{\omega_p}\right)^2}. \tag{2.32}$$

When designing a controller, important characteristics such as good stability, good reference following, and compensation for disturbances are desired. Good reference following need a controller with high gain at low frequencies. This is achieved by placing one pole at zero in the controller transfer function, as can be seen in (2.32). The design of a controller using the K-factor approach is based on the desired cross-over frequency and phase margin of the closed loop system. A high cross-over frequency gives high gain which implies fast system response to disturbances. If a high cross-over frequency is used, the phase needs to be compensated to maintain system stability. This is achieved by adding two zeros at ω_z in the controller transfer function, which give positive phase shift. To prevent noise from being amplified through the controller, two poles at ω_p are added to decrease the gain at higher frequencies. These two poles give negative phase shift.

The first step when designing a controller using the K-factor approach is to choose the cross-over frequency. Using the cross-over frequency and by choosing the desired phase margin, the required phase boost of the controller at the cross-over frequency can be calculated. The phase margin of the closed loop system is defined as

$$\emptyset_{PM} = 180^\circ + \angle G_P(s)|_{f_c} + \angle G_C(s)|_{f_c}. \tag{2.33}$$

Here, $\angle G_P(s)|_{f_c}$ is the phase of the process at the cross-over frequency and $\angle G_C(s)|_{f_c}$ is the phase of the controller at the cross-over frequency. $\angle G_C(s)|_{f_c}$ can be calculated as

$$\angle G_C(s)|_{f_c} = -90^\circ + \emptyset_{boost} \tag{2.34}$$

where the -90 degrees phase lag is the result from the controller pole at zero. Inserting (2.33) into (2.34) and rearranging the terms gives the required phase boost at the cross-over frequency as

$$\emptyset_{boost} = -90^\circ + \emptyset_{PM} - \angle G_P(s)|_{f_c}. \tag{2.35}$$

The next step is to calculate the controller gain which gives the loop transfer gain at the crossover frequency equal to one. The loop gain is defined as

$$|G_L(s)|_{f_c} = |G_c(s)|_{f_c}\left|G_p(s)\right|_{f_c} = 1\ . \tag{2.36}$$

Rearranging the terms in (2.36) gives the controller gain at the crossover frequency as

$$|G_c(s)|_{f_c} = \frac{1}{|G_p(s)|_{f_c}}. \tag{2.37}$$

The K factor can now be determined as

$$K = \tan\left(45^\circ + \frac{\emptyset_{boost}}{4}\right). \tag{2.38}$$

The K factor determines the ratio between the placement of the poles at ω_p and zeros at ω_z in the controller. From the K factor, ω_p is determined as

$$\omega_p = K \cdot \omega_c \tag{2.39}$$

and ω_z as

$$\omega_z = \frac{\omega_c}{\mathrm{K}}\ . \tag{2.40}$$

Finally the static gain k_c of the controller is calculated as

$$k_c = |G_c(s)|_{f_c}\frac{\omega_c}{K}. \tag{2.41}$$

2.3.2 Discretization

When implementing a continuous controller in microcontroller, discretization must be performed. There are a number of methods for descretization such as first-order hold, the Tustin approximation etc [6]. Discretization of a continuous controller is easily done using mathematical software such as Matlab. When performing discretization of the differential equation obtained during control design in continuous time, a difference equation is obtained. The difference equation is an approximation of the differential equation. E.g. using first-order hold the continuous transfer function $G(s)$ is approximated as

$$H_{foh}(z) = \frac{(z-1)^2}{zh}\mathcal{Z}\left[\mathcal{L}^{-1}\left(\frac{G(s)}{s^2}\right)_{t=kh}\right]. \tag{2.42}$$

Here, h is the sample interval.

The sampling period need to be determined in relation to the bandwidth of the system. A rule of thumb for choosing the sample interval h is

$$\frac{2\pi}{\omega_b h} = N. \tag{2.43}$$

Here, ω_b is the bandwidth of the closed loop system. N should be in the interval 10-20 [7]. If the sample period is too short numerical problems can occur due to arithmetic resolution limits. A too large sampling period can result in an insufficient approximation of the continuous controller.

2.3.3 Integrator windup

If the regulated system contains an actuator which can become saturated, this may lead to undesirable effects if the controller contains an integrator. If the actuator becomes saturated due to a large control error, the integrator in the controller may integrate up to a large value. The integral may be so large that even if the control error decreases, the integrator will still saturate the actuator. The time before the integral resumes a normal value may be considerable. This phenomenon is known as integrator windup and can be avoided in several ways.

In a digital controller, integrator windup can be avoided by limiting all the control signals in the difference equation. The limit is usually set to the maximum real control signal value. This way the controller always uses the actual actuator output in calculations resulting in that the size of the integral is limited. Limiting integral action is known as Anti-windup [7].

2.4 Microcontrollers

Microcontrollers have many different features such as analog to digital conversion, Pulse Width Modulation etc. These features are very useful when implementing digital controllers and are described in more detail in this section.

2.4.1 Analog to digital conversion

To convert analog signals to a digital value an Analog Digital Converter (ADC) is used [8]. The analog signal is compared to a constant analog reference and then discretized by the ADC to a numerical value. The number of bits the ADC converter uses determines the number of digital levels and hence the resolution of the converted signal. The converted value, n_{value} , can be determined as

$$n_{value} = \frac{V_{signal}}{V_{ref}} N_{levels} . \tag{2.44}$$

Here, V_{signal} is the analog signal to be converted and V_{ref} is the analog reference signal used for the conversion.

2.4.2 Pulse Width Modulation

In Pulse Width Modulation (PWM) a constant period with a variable duty-cycle is used to generate signals where the duty-cycle can vary between 0-100% [8]. The duty-cycle, d ,which controls the output, is defined as the ratio between the on time, τ_{on}, and the period time, τ_{period} .

$$d = \frac{\tau_{on}}{\tau_{period}} \tag{2.45}$$

In analog circuits PWM signals are generated by an analog comparator and a saw-tooth wave generator. The analog signal which is used to control the duty-cycle is compared with the saw-tooth wave by the comparator. The output from the comparator is high when the analog signal is greater than the saw-tooth wave and switch to zero when the

saw-wave is greater. The period time for the PWM is determined by the period time of the saw-tooth wave.

In digital circuits PWM signals are generated by a digital comparator and a counter. The counter replaces the saw-tooth wave generator and counts from zero to a specific value. The value that is used to control the duty-cycle is compared by the comparator with the value from the counter. The resolution of the PWM signal is determined by the counters maximal value. The period of the PWM cycle is then determined by the counter maximal value and the clock speed of the counters.

2.4.3 Fixed point arithmetic

Calculations in microcontrollers can be implemented with fixed point or floating point arithmetic [9]. Floating point uses a binary point that can vary depending on the size of the value. This results in a high dynamic range which is useful when working with both large and small values at the same time. One drawback with floating point is the high processing power that is needed. Usually when floating point is needed a processor with special hardware for floating point arithmetic is used.

Fixed point uses a fixed decimal point instead. This results in more simple arithmetic that can be handled by ordinary microprocessor instructions. The drawback is that the dynamic range is limited. But with proper scaling of values the fixed point can be used in most cases.

Fixed point can in reality only store integers. The fixed decimal point is virtual and implemented by scaling the real value with a weight. With proper scaling, the necessary amount of resolution and dynamic range can be achieved.

A very common way to scale a value is to shift the bits to the left or right. This corresponds to multiply or divide the value with a factor of 2.

The scaling leads to some errors and limitations. There are some important notations that can be used to describe these factors.

- Precision is the maximum number of non-zero bits that can be represented. In fixed point this is the same as the word length.
- Resolution is the minimum none zero value that can be represented. This is one important factor when scaling the real values.
- Range is the difference between the maximum and the minimum value that can be represented.
- Accuracy is the maximum difference between the real value and the represented value.
- Dynamic range is the ratio of the maximum and the minimum absolute value that can be represented. This is important to consider when working with both large and small values at the same time.

3 Experimental setup

The hardware used consists of a SAPS-400 SMPS and a STM32 microcontroller development board which are described in this chapter, together with the additional hardware needed.

3.1 SAPS-400 Switch-mode Power Supply

SAPS-400 is a SMPS module designed by the electronics magazine Elektor [10]. It is based on a half-bridge topology and can deliver up to 400W of power. Since the module is intended for audio applications there are dual outputs rails that can supply a symmetric voltage. Output voltage for each rail can be set from 35V up to 60V with a potentiometer and is controlled by an analog control circuit. Switching frequency is 85 kHz and the efficiency is specified to 92% at 100 to 120 or 200 to 240 VAC input voltage. A more detailed description of the SAPS-400 is presented in the following sections.

3.1.1 Power board

The SAPS-400 can be seen in Figure 3.1. The schematic diagram for the SAPS-400 power board can be found in [10]. On the input side a rectifier bridge is used to rectify the AC voltage from the main voltage to a DC voltage. The DC voltage is charged in two primary capacitors which form a voltage divider with help of two resistors. There are filters for EMI suppressions implemented by capacitors and an inductor. Protection for the converter is implemented by a fuse and a TVS (Transient Voltage Suppression) diode. Soft start is implemented using a PTC (Positive Temperature Coefficient) resistor to avoid large current when the primary capacitors are charged at startup.

The voltage divided by the capacitors is then switched through a high-frequency transformer, using two MOSFETs connected in a half-bridge, to either ground or the full DC voltage. The MOSFET gates are driven by a pulse transformer and a high current driver. The high frequency transformer has 26 turns in the primary winding and is designed for a switching frequency of 85 kHz. At this frequency the flux density of the transformer core is optimally used. There are two main secondary windings at 13 turns each. A full wave rectifier is used to achieve two output rails with ground between the two windings. An LC filter is used to reduce the ripple in the output voltage. The two windings in the inductor are winded on the same core. This give better cross regulation between the two output rails.

The error signal for the controller is fed back using voltage divider and a zener diode chain. By a variable zener diode the reference point for the output voltage can be adjusted. To isolate the secondary side an opto coupler is used to forward the error signal to the control board. There are also two secondary outputs which deliver a constant symmetric voltage at 15V. These outputs are regulated with linear voltage regulators and have an own winding with 4 turns in the transformer. The control board is supplied by an own winding with 4 turns in the transformer and a linear voltage regulator. A drawback of this is that a minimum load is needed to keep the converter running. To initially startup the circuit an emitter follower is used to supply the control board. A thermostat is used to shut down the startup circuit in case of failure or short circuit. If the module fails to start the collector resistor in the emitter follower will heat

up and affect the thermostat. A current transformer is used to measure the current into the high frequency transformer to implement a short circuit protection. At high current, the control board will turn off the switching transistors to protect the converter.

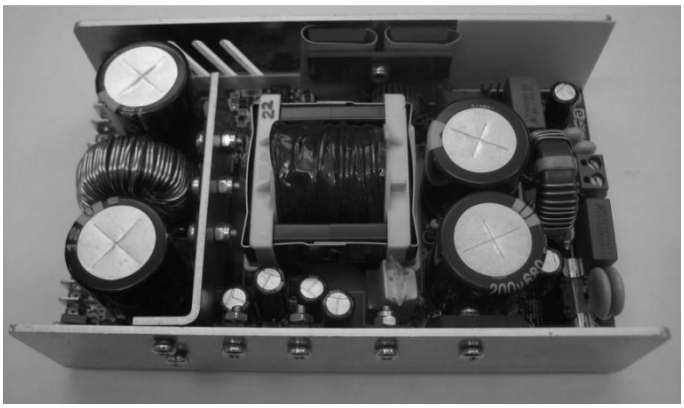

Figure 3.1: *SAPS-400.*

3.1.2 Original analog control board

All the original control functions for the SAPS-400 can be found on a separate control board. The board is designed around an analog PWM controller which generates the PWM signal to drive the transistors. The input is the error signal from the output voltage. The signal is filtered before it is forwarded to a comparator in the PWM controller chip. The switching frequency is set by a resistor network to 85 kHz. The controller chip also handles dead time generation between PWM cycles and soft start. When the signal from the current transformer is above the limit, a pulse is generated by a timer circuit to shutdown the controller chip. There is also an input for synchronization of the PWM controller with other modules. The output to the transistors gate is buffered by a high current driver.

3.1.3 Component values

The small signal model for a half-bridge converter, such as the SAPS-400, contains some component value which has to be determined. All the values that are used in the model can be seen below. The capacitors capacitance, C, and ESR, R_c, is determined from the capacitors datasheet. Since the inductor was winded by hand and the material for the core was unknown, it is hard to find the component values theoretically. An experimental method was therefore chosen to determine the inductance, L, and ESR, R_L. The numerical values used were:

- $R_c = 40m\Omega$
- $R_L = 20m\Omega$
- $L = 20\mu H$
- $C = 1650\mu F$

The circuit in Figure 3.2 can be used to determine the inductance by finding the resonance frequency of the filter. In the circuit the inductor was paralleled with a capacitor with a known value. This filter was then driven by a signal generator. A

resistor was added to protect the generator from short circuit. The output signal from the filter was then observed using an oscilloscope. By sweeping the frequency slowly and observing the amplitude of the output, the resonance frequency can be found. At this frequency, the amplitude of the output will have its maximum value. The resonance frequency f_0 and the known value of the capacitors C can then be used to determine the value of the inductor L by using (3.1). The ESR for the inductor was estimated by counting the number of turns and the diameter of the wire.

$$L = \frac{1}{C(2\pi f_0)^2} \tag{3.1}$$

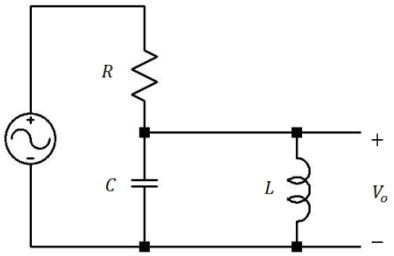

Figure 3.2: *Resonance circuit*

3.2 Keil STM32 development board

A development board from Keil with a STM32 processor is used as the new control board for the SAPS-400. The STM32 processor is a 32 bits processor with a Cortex ARM core. The development board has some hardware attached to the processor to simplify the development of different applications. E.g. there is a 2x16 characters LCD display, 8 LEDs, 3 buttons and 1 potentiometer. There are also many interfaces to communicate with the board E.g. USB, CAN and RS232 ports. All pins on the processor can also be accessed through headers on the board. The development board can be seen in Figure 3.3. In this application, two inputs to the ADC converter and two outputs for PWM signals are used to control the SAPS-400 board. The RS232 port is used to set the reference values for the controllers. In the following sections the features of the microcontroller and the development tools are described.

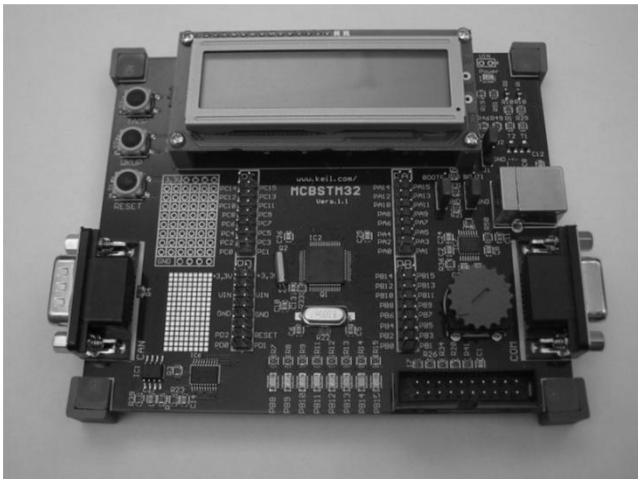

Figure 3.3: *KEIL MCBSTM32 development board.*

3.2.1 STM32 microcontroller

The STM32 microcontroller family from STMIcroelectronics is 32-bit flash microcontrollers based on the ARM Cortex-M3 core. This core is specially developed for embedded applications such as microcontrollers, automotive body systems industrial control systems and wireless networking [11]. The STM32 microcontroller is available in various pin- and memory-sizes. The specific microcontroller used was STM32F103RBT6 and some of its features are:

- Up to 72 MHz clock frequency
- 12-bit analog to digital converter, 16 channels
- 8 Timers
- USART
- CAN
- 128 kB flash memory

3.2.2 Development tools

For C-code development the Eclipse platform was used. This platform is freeware and available for download online. This platform is used combined with the GCC C-compiler. This compiler is also freeware and available for download online. For debugging and flash programming of the microcontroller the software µVision3 from Keil Software inc. was used. This software is included when purchasing the Keil STM32 development board.

3.3 Interface

The output voltage and current from SAPS-400 needs to be measured and fed back to the STM32 board. For this purpose a simple interface board was developed. It was built on a special prototype board with a hatched ground plane to provide a good electrical environment. Passive components were of SMD type and soldered on the solder side of the board. The interface board can be seen in Figure 3.4 and the schematic diagram is found in Appendix. In the following sections more details about the different parts of the interface circuits are described.

3.3.1 Voltage measurement

The output voltage from the SAPS-400 is measured with a simple voltage divider. Two resistors with tolerance 1% were used to divide the voltage. The values of the resistors were set to achieve 3.3V to the ADC converter when the input voltage is 103.3 V. The divided voltage is buffered with an OP amplifier configured as a voltage follower. To avoid aliasing the output from the amplifier is filtered with a simple RC filter before the ADC converter. The cutoff frequency for the RC filter was set to 1600 Hz.

3.3.2 Current measurement

The output current from the SAPS-400 is measured with a shunt resistor. A thick film resistor at 10 mΩ and 1% tolerance resistance was used. The resistor has four

connections to avoid errors in the small induced voltage. Two connections are used for the current and two for the measurement. The instrument amplifier MAX4080 from Maxim is used to gain the small differential voltage over the resistor. This version of the amplifier has a constant gain of 20. This gives 3.3 V to the ADC converter when the current through the shunt resistor is 16.5A. To avoid aliasing the voltage from the amplifier is filtered with a simple RC filter before the ADC converter. The cutoff frequency for the RC filter was set to 1600 Hz which is the same as the filter for the voltage sensing.

3.3.3 Gate driver

The MOSFETs in the SAPS-400 needs to be driven by a driver to ensure fast rise and fall times. The push-pull driver chip MAX627 from Maxim is used to drive the MOSFETs gates through the pulse transformer on the power board of the SAPS-400. The pulse transformer isolates the control and interface board from the main voltage at the SAPS-400.

3.3.4 Communication

The communication with the system is done with a PC through RS232. This interface is already implemented at the STM32 board. A CAN port which is available on the development board can be used to interconnect a system of converters.

3.3.5 Power Supply

A laboratory power supply is used to supply the interface board at 12 V. This voltage is used to drive the MOSFET driver. A 5 V linear voltage regulator is used to drive the voltage and current measuring circuits. The STM32 board is also supplied with 5 V by the voltage regulator.

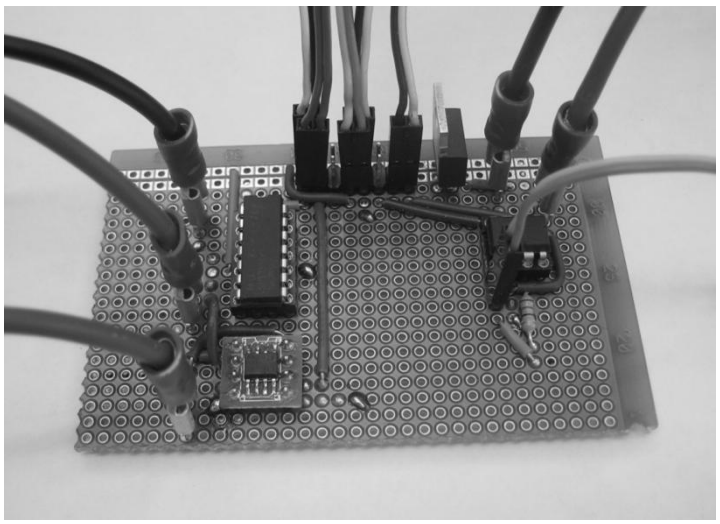

Figure 3.4: *Interface board.*

3.4 Experiment strategy

During implementation of control algorithms the performance of the feedback system is tested. This is done by measuring and investigating the output voltage and current in some different test cases. The test setup is described in the following sections.

3.4.1 Load

A resistive load will be used during performance testing consisting of two effect resistors. The resistors have resistance 22 Ω and rated to 200 watts each. One single resistor or two parallelled resistors will be used during experiments giving load resistances of 11 and 22 Ω.

3.4.2 Measurements

The output voltage and current from the SAPS-400 SMPS are measured at the analog inputs of the STM32 microcontroller. All signals are measured using a four channel MSO 2024 digital oscillioscope from Tektronix. Numerical data and images from the tests are saved and exported to a PC. The numerical data is imported in Matlab and post-processed to correct units. This processed data is then used for plotting the results.

3.4.3 Test cases

During experiments the system will be exposed to different reference changes for the voltage and current at different loads. Also, load changes will be applied to investigate the system ability to compensate for disturbances. Reference changes was done by sending reference values via a serial port using a simple Matlab script.

To verify correct PWM signal generation a low input voltage was used for the SMPS during the first tests. The final tests were then performed using 110 VAC input voltage.

4 Control of the half-bridge converter

In this chapter the controller design and implementations are presented.

4.1 Controller design

The model used when designing the voltage and current regulators was the transfer function from duty cycle to output voltage and current derived in Chapter 2.1.2. Bode plots for the two models are shown in Figure 4.1. The numerical component values are found in Chapter 3.1.3. The resistance value for the load was set to 11 Ω since this is the minimum resistive load which will be used during tests. The voltage was set to 156 V which is the DC voltage across the primary capacitors at 110 VAC input.

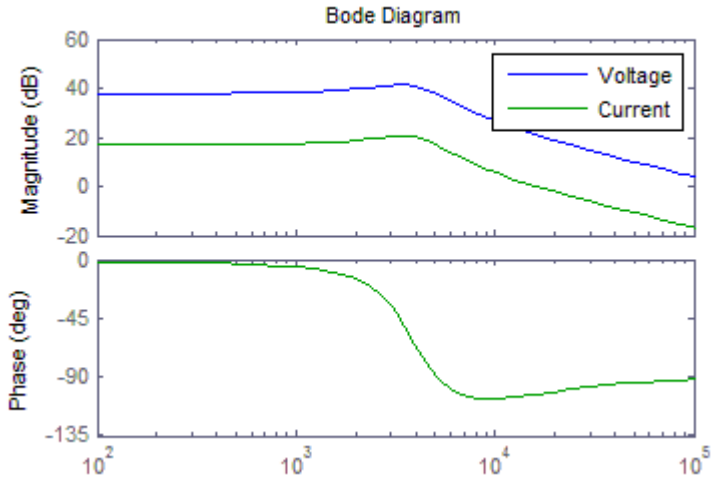

Figure 4.1: *Bode plots for voltage and current processes.*

Figure 4.1 shows that the processes have constant gain and low phase shift at low frequencies. Beyond the resonance frequency of the LC filter the gain start to decrease with 40 dB per decade and the phase tends to -180 degrees. The ESR in the capacitors introduces a zero in the transfer function. Beyond this zero the gain decrease with 20 dB per decade and the phase tends to -90 degrees.

The derived models for the converter are used in the design of the voltage and current controllers. The resonance frequency for the LC filter is calculated to approximately 620 Hz. Based on this frequency the crossover frequency was chosen to 1200 Hz. The phase margin was chosen to 60 degrees to give the system adequate stability. The parameters in the voltage and current controllers are then calculated according to the K-factor method described in Chapter 2.3.1. Figure 4.2 shows the Bode plots for the voltage and current controllers.

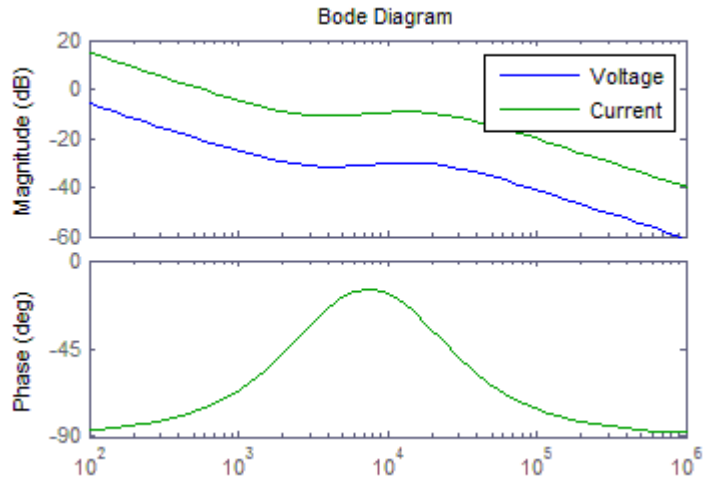

Figure 4.2: *Bode plots for the designed controllers.*

The Bode plot shows a higher gain at low frequencies and a positive phase boost at the crossover frequency. At higher frequencies the gain decreases implying that high frequency disturbances are damped. Figure 4.3 shows the Bode plots for the closed loop systems for both controllers.

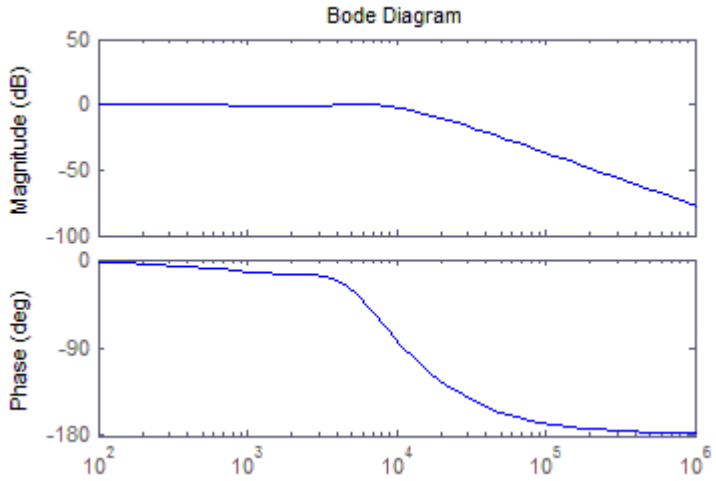

Figure 4.3: *Bode plots for the closed loop systems.*

The closed loop system describes the gain and phase characteristics of the system. The bandwidth for the system can be seen at the point where the closed loop gain has decreased 3 dB. This can be estimated to $10.9 \cdot 10^3$ Rad/s. Figure 4.4 shows step responses for both controllers for a step of one unit.

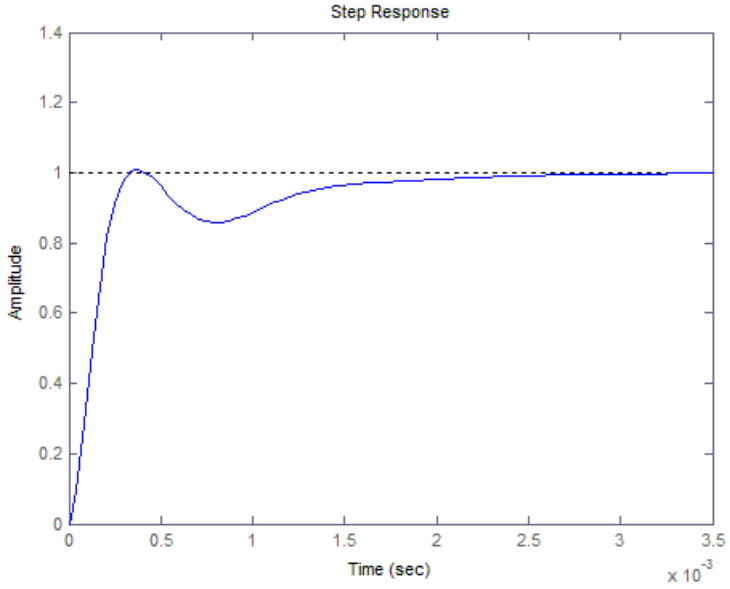

Figure 4.4: *Step response for the designed controllers.*

Designing for cross-over frequency $f_c = 1200\ Hz$ and phase margin $\varphi_m = 60°$, results in the voltage and current controller transfer functions

$$G_v(s) = \frac{3.789 \cdot 10^{-6} s^2 + 0.0278 s + 51}{4.164 \cdot 10^{-9} s^3 + 1.291 \cdot 10^{-4} s^2 + s} \tag{4.1}$$

and

$$G_c(s) = \frac{4.168 \cdot 10^{-5} s^2 + 0.3058 s + 560.9}{4.164 \cdot 10^{-9} s^3 + 1.291 \cdot 10^{-4} s^2 + s}. \tag{4.2}$$

Discretizing the transfer functions (4.1) and (4.2) using the First Order Hold method with sample period of $h = \frac{1}{f_s} = \frac{1}{17578\ Hz}$, where f_s is the sample frequency, gives the discrete controllers

$$G_v(Z) = \frac{0.01714 - 0.01688 Z^{-1} - 0.006457 Z^{-2} + 0.007202 Z^{-3}}{1 - 1.828 Z^{-1} + 0.99976 Z^{-2} - 0.1715 Z^{-3}} \tag{4.3}$$

and

$$G_c(Z) = \frac{0.1885 - 0.1857 Z^{-1} - 0.07102 Z^{-2} + 0.007922 Z^{-3}}{1 - 1.828 Z^{-1} + 0.99976 Z^{-2} - 0.1715 Z^{-3}}. \tag{4.4}$$

The sample period used gives a ratio according to (2.43) as

$$N = \frac{2\pi}{\omega_b h} = \frac{2\pi f_s}{\omega_b} \approx 10.13. \tag{4.5}$$

Equation (4.5) shows that N is within the recommended interval described in Chapter 2.3.2.

4.2 Implementation of digital controllers

The digital controller implementations use some of the peripheral modules in the microcontroller. In the following sections these modules are presented in more detail.

4.2.1 PWM outputs

Two PWM signals are implemented by use of two timers and two comparators. These PWM signals are used to control the power switches in the converter and they are not allowed to be high at the same time to avoid short circuit in the half bridge.

The two timers run on a peripheral clock at 72 MHz, which is the highest frequency possible. The components of the SAPS-400 SMPSU are optimized for a switching frequency of 85 kHz. Though, this switching frequency was slightly decreased to increase the resolution in the PWM-signal. Using a switching frequency of 70.38 kHz gives a PWM resolution of 512 levels. Both timers count from 0 to 1023 and are synchronized. One of the timers starts with an offset at 512 which results in a phase shift of 180 degrees. The duty cycles are not allowed to be higher than 50% to avoid to high outputs at the same time. The two toggling PWM outputs and the synchronized AD conversions can be seen in Figure 4.5.

4.2.2 AD-conversion

When measuring the output current and voltage from the SAPS-400 two Analog to Digital Converter (ADC) channels are used. The STM32 microcontroller used only has one ADC module and can therefore not do multiple conversions simultaneously. However the ADC can be configured in scan mode which performs a sequence of AD-conversions. Using this mode the conversion only needs to start once and the ADC will automatically perform a sequence of conversions. Configuring the ADC in Direct Memory Access (DMA) mode implies that once a conversion is completed, the converted value is transferred to a global vector in the memory. An interrupt by the DMA is generated when the data transfer is completed and notifies that new ADC values are available.

The ADC module clock is divided from the system clock by a pre-scaler. At the highest frequency of 36 MHz an analog to digital conversion is completed in 1.17 µs. Conversion is performed in 12 bits. During the analog to digital conversion the ADC samples the input under some time to create a mean value. This sample time can be set in software.

To control the sampling instant and sampling frequency, a timer is used to trigger the AD conversions. The timer is synchronized with the PWM timers by setting the period time to a multiple of the period of the PWM timers. This multiple factor and the frequency of the PWM then determine the sampling frequency of the controller. This timer can be seen as a timeline for the controller. A diagram of the timing can be seen in Figure 4.5. A comparator is used to trigger the AD conversion through an event generated on comparator match. Sampling instants can be added and placed freely in the timeline by setting the comparator register. When the AD conversion is completed an interrupt is generated which set the next sampling point. To avoid noise in the conversions due to the switching the sampling instant is chosen to be at the 25 % or

75% of the PWM cycle depending on the duty cycle. Depending on the multiple factor used, more conversions can be used to calculate a mean value. In the interrupt, the AD values are added to the mean value. After the last conversion, the calculation of the control signal is done. Then, the next sampling instant is set to a fixed point near the end of the timeline. When this dummy conversion is completed the interrupt updates the PWM comparators with the new control signal. The sampling instant for the next control period is also set depending on the duty cycle. In the implementation the multiple factor was set to 8 which give a sampling frequency of 17578 Hz and 4 conversions is performed during a control period.

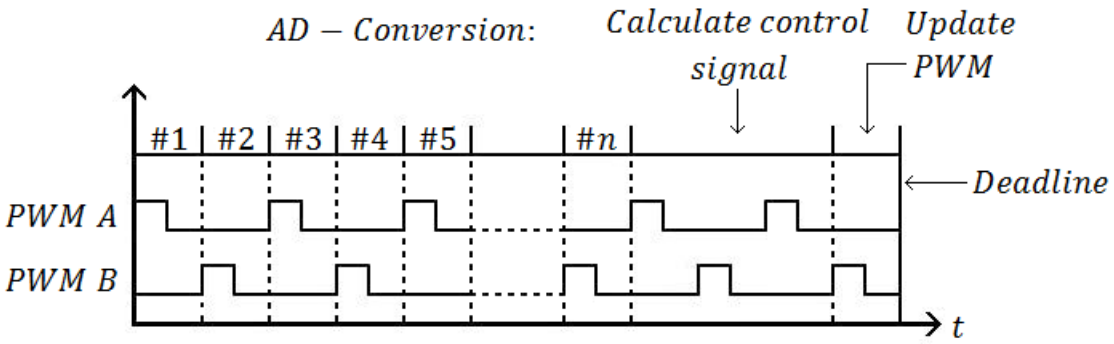

Figure 4.5: *Overview of the software timing.*

4.2.3 Control signal calculations

The first step when calculating the control signal was to generate the control error by calculating the difference between the reference value, converted to a corresponding AD-value, and the measured output AD-value. To simplify the interpretation of the result during calculations, this error was then scaled to a value corresponding to the SI-unit multiplied by factors of 10. This gives better resolution in the result since fixed point numbers are used. The new control signal is calculated using the difference equation designed in previous chapter. The coefficients in the equation are scaled with a factor of 10000 before being implemented in software to provide good resolution. This new control signal is then converted to a corresponding PWM duty-cycle. If the calculations results in a PWM-output larger than 45%, this result is ignored and the PWM-output is set to 45%. This will also be the value used for future control signal calculations. The controller will therefore never use control signal larger than 45%. This method for limiting control signals is a simple form of anti-windup [7]. Past error and control signal values are then scaled to remove the scale factor of the controller coefficients before being saved for future calculations.

Both the voltage and the current controller are implemented in the software. Both controllers calculate their own control signals and the lowest control signal is then used to drive the converter. This gives the possibility to use the converter as both constant voltage and constant current sources. By setting the voltage reference to a desired value and the current reference to its maximum value the converter works as a constant voltage source. If the current reference is set to some lower value, the converter will also have a current limitation. If the current reach the limit value the converter will start

to work in current mode instead. This can be used in a reverse manner to use the converter as a constant current source with or without voltage limitation.

4.2.4 Communication

Serial communication is used to receive new reference values and to send measured output voltage and current values. A USART module is used to handle the communication. When data is received, an interrupt is generated to handle the incoming data. The first byte is a command byte which tells the microcontroller what type of data that are following. Then data is received as two bytes with the Most Significant Byte (MSB) first. The output data stream consists of five bytes. The first byte is a synchronizing byte. Then the measured voltage and current are sent as two bytes each with the MSB first.

5 Experimental results

5.1 Voltage controller

Figure 5.1-5.5 shows the output voltage and current during voltage reference changes. In these cases the voltage controller is used to control the output of the half-bridge and the current controller is shut off.

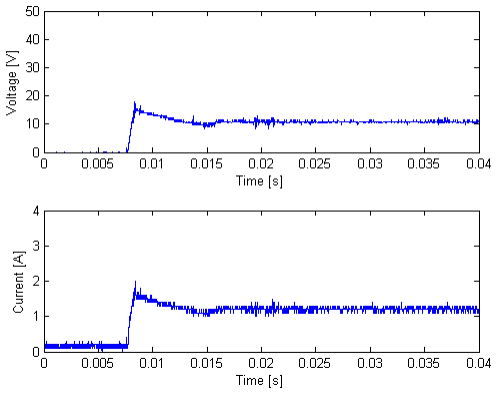

Figure 5.1: *Step response 0-12 V, 11 Ω load.*

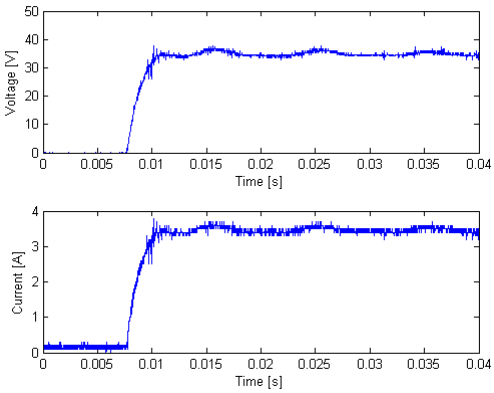

Figure 5.2: *Step response 0-36 V, 11 Ω load.*

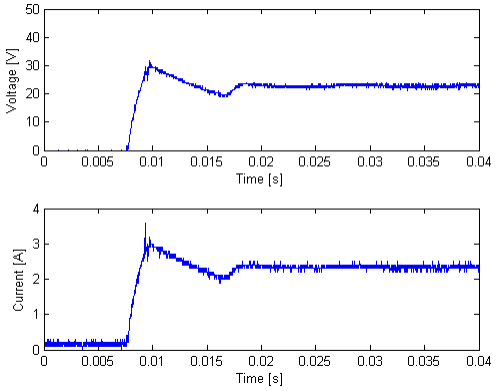

Figure 5.3: *Step response 0-24 V, 11 Ω load.*

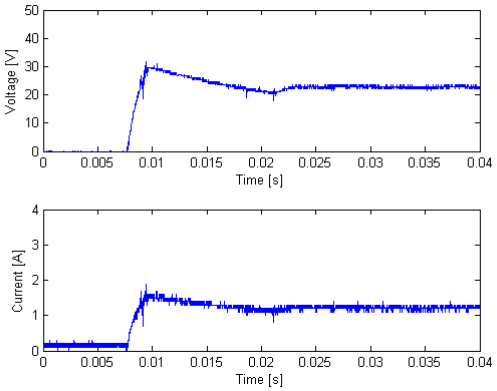

Figure 5.4: *Step response 0-24 V, 22 Ω load.*

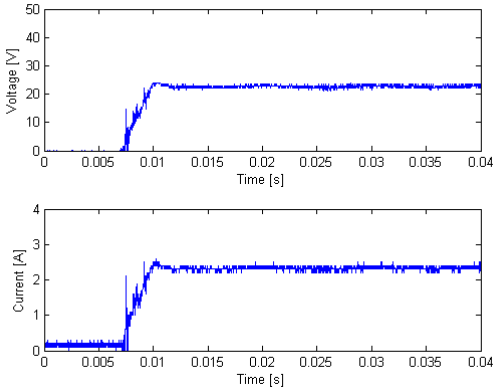

Figure 5.5: *Step response 0-24 V with ramp activated, 11 Ω load.*

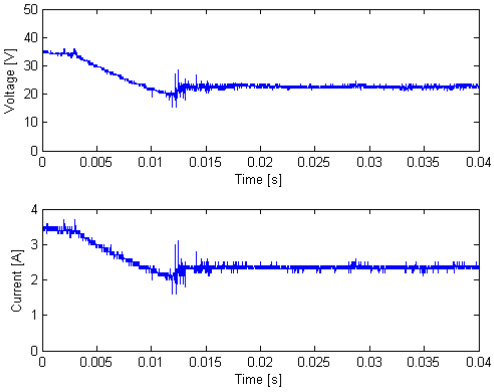

Figure 5.6: *Step response 36-24V, 11 Ω load.*

It can be seen that the reference is reached in all cases but the shape of the response varies with the load used. The controller has a fast response which overcharges the output capacitors at low reference levels. This produces an over-shoot at the output which can be seen from Figure 5.1 and 5.3. The over-shoot attenuates then when the capacitors are discharged through the load. When the overshoot has attenuated the output is held at the reference level. A high load decreases the time to reach the reference. This can be seen by comparing Figure 5.3 with Figure 5.4.

At higher levels, as in Figure 5.2, no over-shoot is produced. This is because the controller has a saturated control signal and at higher levels the maximum control signal is not enough to produce an over-shoot. Though, in this case the output appears to be less stable and Figure 5.2 shows that a low-frequency component is present in the output.

One way to decrease the over-shoot at low reference levels is to implement a ramp function where the reference is ramped up internally in the control algorithm. Figure 5.5 shows the step response when a ramp function is implemented. Here, very low over-shoot is produced and the reference is reached in less time compared to the case were no ramp function was implemented.

Figure 5.6 shows the system response when the reference is decreased. The output voltage slowly decreases to the reference value with the same slope as in Figure 5.4.

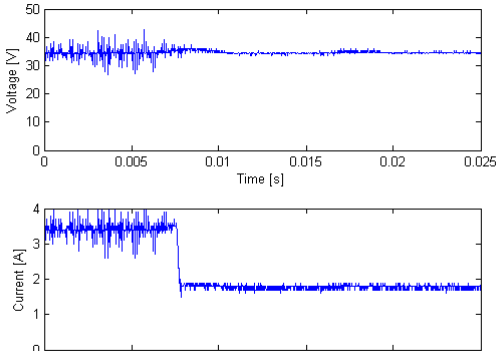

Figure 5.7: *Response at 36 V, 11-22 Ω load change.*

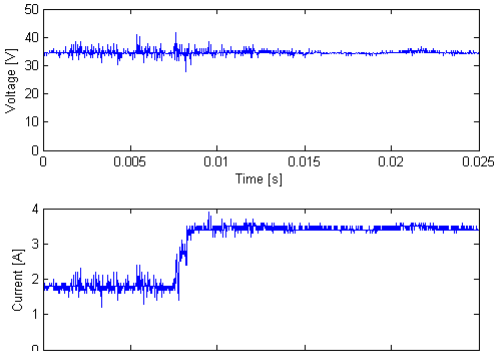

Figure 5.8: *Response at 36 V, 22-11 Ω load change.*

The response when the load is changed while the reference is held constant can be seen in Figure 5.7 and Figure 5.8. In both cases it can be seen that the output voltage is stable at the reference during a load change.

5.2 Current controller

Figure 5.9-5.14 shows the output current and voltage during current reference changes. In these cases the current controller is used to control the output of the half-bridge and the voltage controller is shut off.

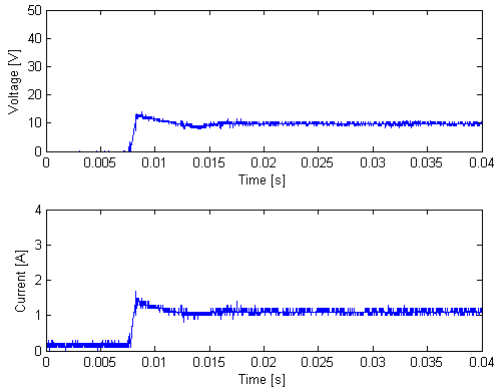

Figure 5.9: *Step response 0-1 A, 11 Ω load.*

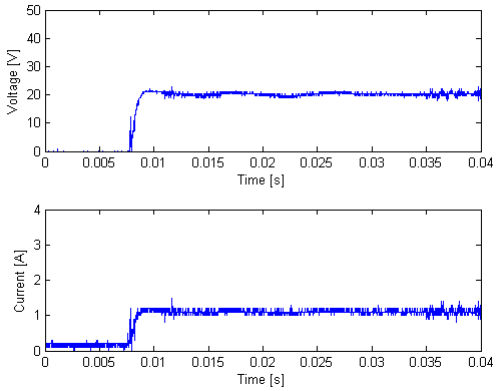

Figure 5.10: *Step response 0-1 A, 22 Ω load.*

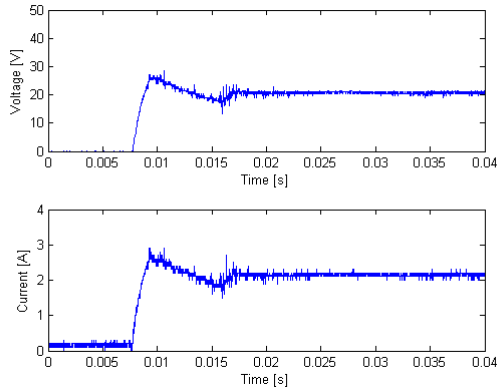

Figure 5.11: *Step response 0-2 A, 11 Ω load.*

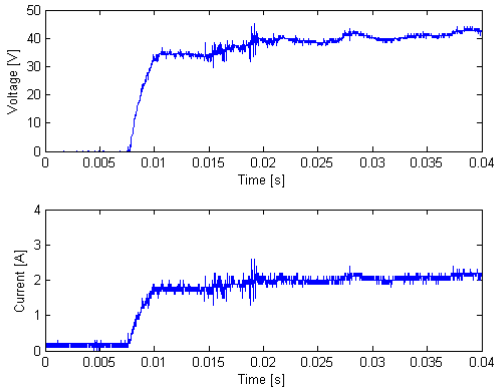

Figure 5.12: *Step response 0-2 A, 22 Ω load.*

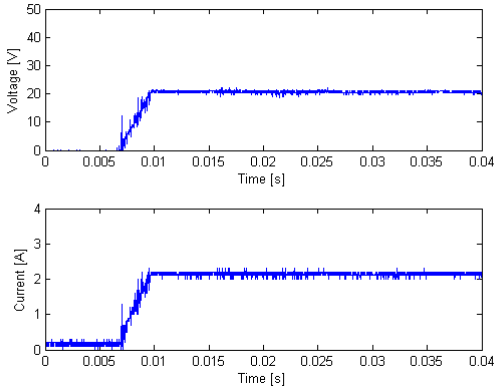

Figure 5.13: *Step response 0-2 A with ramp activated, 11 Ω load.*

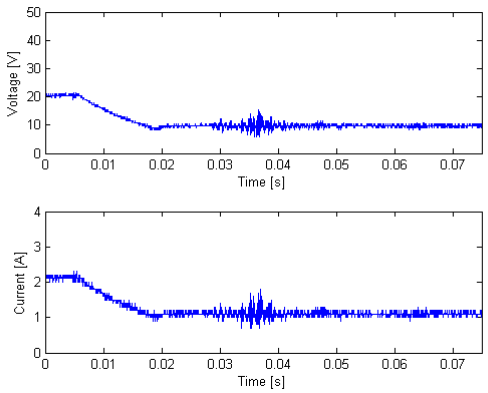

Figure 5.14: *Step response 2-1 A, 11 Ω load.*

It can be seen that the shape of the output current varies with the load used. With a load at 11 Ω the output current have an over-shoot similar to Figure 5.9 and 5.11. The over-shoot is produced due to the fast response of the current controller. This gives a large control signal which gives an over-shoot in the cases when the output power is low as in Figure 5.9 and Figure 5.11. After the peak of the over-shoot the current decreases towards the reference when the output capacitors discharge through the load.

A resistive load of 22 Ω results in output currents without over-shoot similar to Figure 5.10 and Figure 5.12. The explanation for this is that the controller is designed for a load at 11 Ω. Because of the higher load the controller behaves more softly at the reference change. The controller simply calculates a control signal which is lower than a controller designed for 22 Ω load would have.

In the same way as in voltage control the over-shoot produced can be removed by implementing a ramp function for the current reference. Figure 5.13 shows the step response for the current controller with this ramp function activated. Here, no over-shoot is produced and the output current is stable in shorter time compared to the case without ramp function.

The response for the output current when the reference is decreased can be seen in Figure 5.14. The time to reach the new value depends on the discharging of the output capacitors in the same way as for the voltage controller.

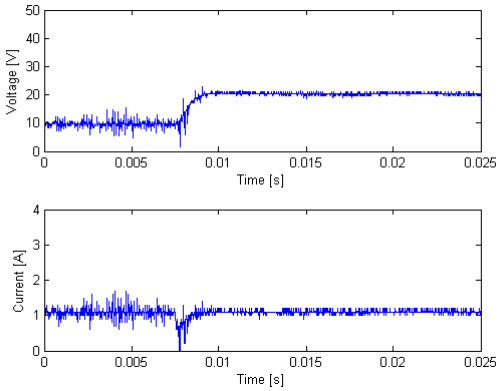

Figure 5.15: *Response at 1A, 11-22 Ω load change.*

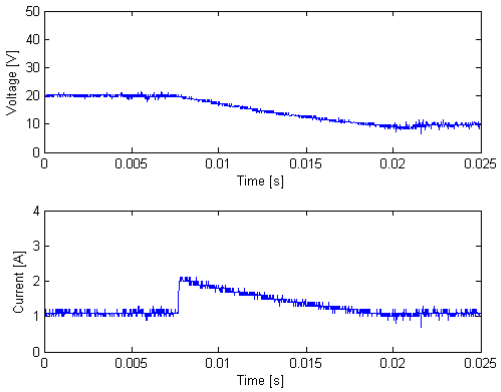

Figure 5.16: *Response at 1A, 22-11 Ω load change.*

In Figure 5.15 and Figure 5.16 the response for load changes are shown. In both cases the response is slower than for the voltage controller. This is due to that the voltage across the output capacitors needs to be changed. In the first case the output power is increased by increasing the load resistance, resulting in that the voltage needs to increase. The current shows a small drop at the time of the load change. In the next case the output power is decreased by decreasing the load resistance. In this case the voltage across the capacitors needs to decrease before the current returns to the reference.

6 Conclusions

6.1 Comments to experimental results

The experiements from Chapter 5 shows good results for the designed controllers. The controlled system follows the voltage and current references and compensate for load changes.

The practical experiments show a larger overshoot and a slower response to reference changes compared to the Matlab simulation in Figure 4.4. One possible explanation to this is that the model used may be inaccurate. Since some important component values are determinded experimentally this may be a possible source of errors. The reason for the slower response time compared to simulations can be that a simple form of anti-windup is implemented. In simulations the controller is allowed to use unlimited control signals. This is however not possible in reality where the control signal is limited.

The overshoot which is present can be removed by implementing a reference ramp function. This function changes the reference value with a fixed slope and the results are reduced overshoot and faster response time.

When applying load changes to the system the results are good for the voltage controller where the load change is practically invisable in the output voltage. When applying a load change to the current controller there are some disturbances. This is a result from the need of charging and discharging of the output capacitors to the reference voltage.

There are some devation between the real voltage and current and the reference values. This can be explained by how the sampling point is determined. The controller needs the mean value of the output to work correctly and the method used can lead to some devation from this value due to the ramp shape of the output signals. The noisy environment can also effect the measured values.

6.2 Suggestions on future work

Due to the noisy enviroment, one important improvement would be to construct a well designed PCB for the controller. A solid ground and supply plane and especially an dedicated part for the analog circuitry should be needed for more accurate measurments. If the controller board are designed on the same board as the half-bridge, the cables can also be removed.

For a more stand alone solution, an on-board power supply for the control logic should be implemented to remove the use of an external power source. A CAN or RS485 bus should be implented to prepare the design of system of SMPS. These communcation media are sutaible when several units should communicate together in a system.

Fine tuning of the controllers can be performed in order to improve the performance of the system. Some other more advanced control method may be used to se if this can improve the performance of the feedback system.

An over-current protection should be implemented to avoid saturation of the transformer and protection against overload.

6.3 SMPS in paralleled system

To construct a modular system of SMPS with current sharing, a method for implementing this should be chosen. Droop methods results in a simple solution but has low efficiency. There will also be difficulties designing a system of converters with different power ratings. This can affect the flexibility of the system. To achieve high efficiency and good flexibility an active current method would be preferable.

One common and simple method used today for analog controllers are implemented by an inner loop structure and a dedicated master. One converter controls the voltage for the system and the error signal from the voltage control loop is used to control the rest of the converters. This method gives good voltage regulation and fast current sharing but has low redundancy. If the master converter fails the system will also fail. Therefore is the inner loop less preferable if high redundancy is desired.

To achieve high redundancy, an outer loop structure should be used. The most common method for outer loop structures is average current programming. In the analog case it is implemented by connecting all converters to a current sharing bus. The bus is driven by the converter current monitor through a resistor. The voltage at the bus then represents the average current supplied by the system. If the current for an individual converter differs from the average current on the bus there will be a voltage drop across the resistor. This voltage is then used to compensate the reference value in the control loop for that converter. Another common method in the analog case for outer loop structures can be implemented by replacing the resistor with a diode. This replaces the average current programming to an automatic master current programming. The converter that supplies the highest current then drives the bus. The outer loop structure has the advantages of high flexibility and reliability. The disadvantage is that the voltage regulation can be disturbed by the current sharing compensation.

For a digital controller implementation with high flexibility and redundancy an active current sharing with an outer loop structure should be used. The current programming can be average current or automatic master.

If the average current programming is used, one converter has to calculate the average current for the system. This can be done by assigning a master converter that requests the output current from all slave converters and then broadcast the average current back. One way to implement the communication is by using a CAN or RS485 bus. To achieve high redundancy it is important that all converters can be assigned to masters if the current master fails. The master slave current programming can be done if all converters broadcast theirs output current and the highest received value are then used for current sharing.

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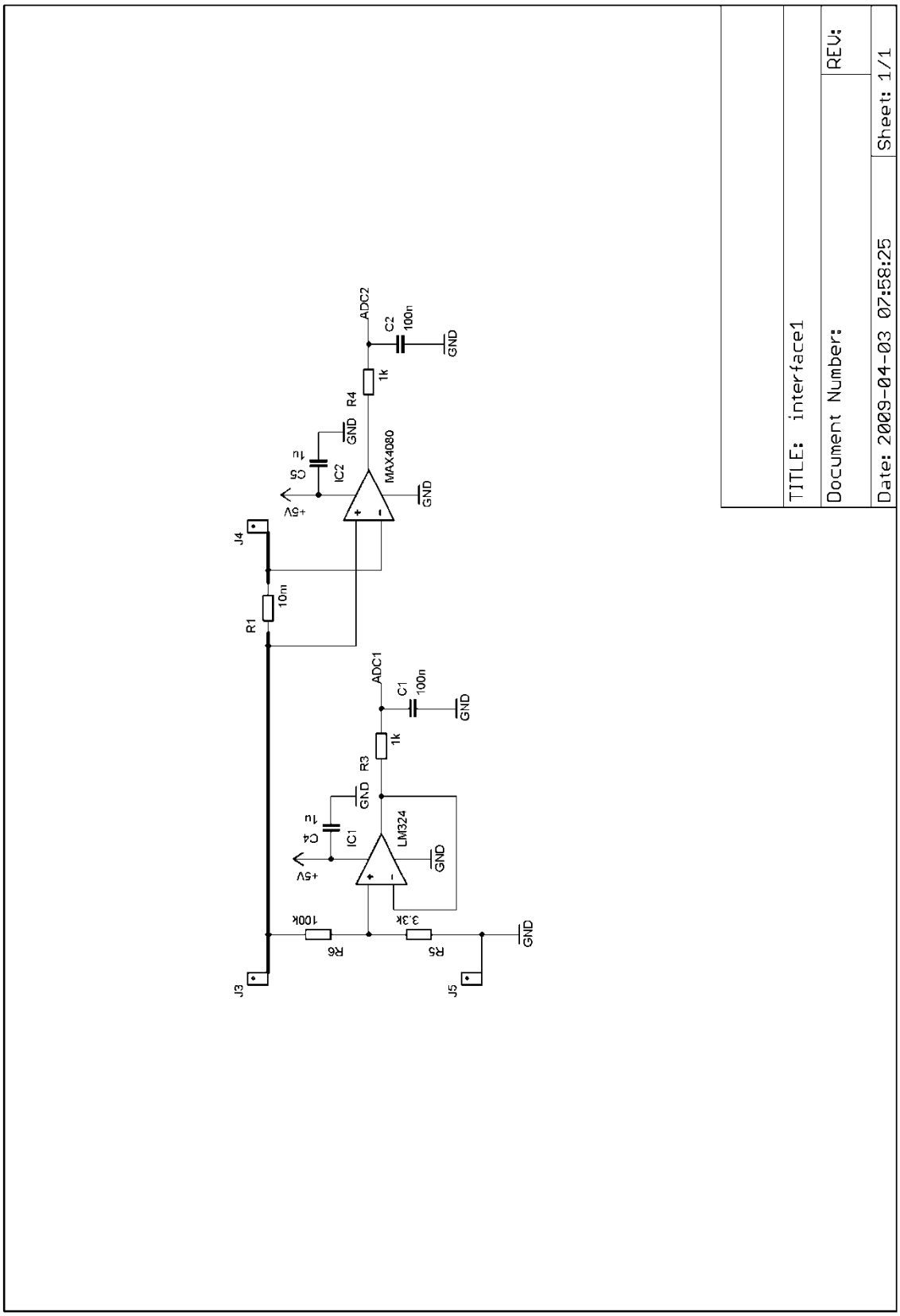
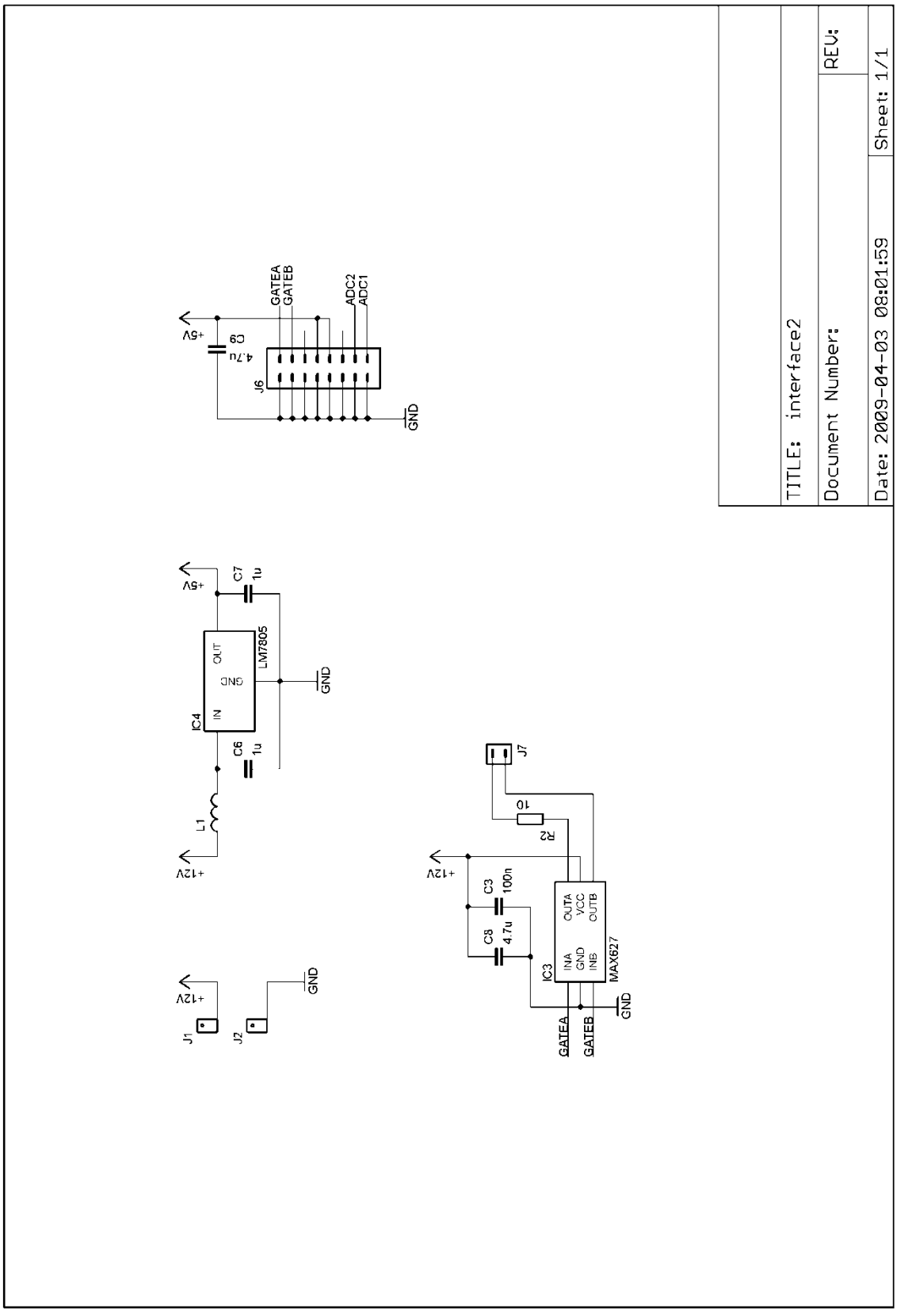
Appendix

Interface circuit diagram

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ADC1
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+5V
C7
1u
IC4
IN
GND
OUT
LM7805
GND
C6
1u
L1
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R2
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C3
100n
C8
4.7u
IC3
INA
GND
INB
OUTA
VCC
OUTB
MAX627
GATEA
GATEB
GND
+12V
J1
J2
GND

Matlab code for controller design

```
clc
format long

Vd=156;          %Voltage input
R=11;            %Load resistance
C=3300e-6/2;     %Capacitance in LC filter
L=40e-6;         %Inductance in LC filter
Rc=80e-3;        %Capacitor ERS
Rl=40e-3;        %Inductors ERS
N1=26;           %Number of windings in transformer at primary side
N2=26;           %Number of windings in transformer at secondary side

fs=17.578e3;     %Sampling frequency
fc=1200;         %Crossover frequency
pm=60;           %Phase margin

s=tf('s');

w0=1/sqrt(L*C);
exi=(1/(C*R)+(Rc+Rl)/L)/(2*w0);
wz=1/(Rc*C);

%Process for voltage
Tpv=((Vd/2)*(N2/N1))*(w0^2/wz)*((s+wz)/(s^2+2*exi*w0*s+w0^2));

%Process for current
Tpc=((Vd/2)*(N2/N1))*(w0^2/wz)*((s+wz)/(R*(s^2+2*exi*w0*s+w0^2)));

wc=2*pi()*fc;
boost=-pi()/2+pm*(pi()/180)-angle(freqresp(Tpv,wc));
K=tan(pi()/4+boost/4);
wz=wc/K;
wp=wc*K;
kc=(1/abs(freqresp(Tpv,wc))*(wz/K));

%Controller for voltage
Tcv=(kc/s)*(((1+s/wz)^2)/((1+s/wp)^2));

%Discrete controller for voltage
Tcvd=c2d(Tcv,1/fs,'foh');
[TcvdNum,TcvdDen]=tfdata(Tcvd,'v')

wc=2*pi()*fc;
boost=-pi()/2+pm*(pi()/180)-angle(freqresp(Tpc,wc));
K=tan(pi()/4+boost/4);
wz=wc/K;
wp=wc*K;
kc=(1/abs(freqresp(Tpc,wc))*(wz/K));

%Controller for current
Tcc=(kc/s)*(((1+s/wz)^2)/((1+s/wp)^2));

%Discrete controller for current
Tccd=c2d(Tcc,1/fs,'foh');
[TccdNum,TccdDen]=tfdata(Tccd,'v');
```

```
%Loop transfer for voltage
vlt=Tpv*Tcv;

%Loop transfer for current
clt=Tpc*Tcc;

%Closed loop for voltage
ccl=feedback(vlt,1);

%Closed loop for current
vcl=feedback(clt,1);
```