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# Mixed-mode Circuit and Device Simulations of IGBT with Gate Unit Using Synopsys Sentaurus Device

*Master of Science Thesis*


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# Abstract

The use of simulation tools is of great value in the process of developing new power electronics devices and new converter topologies. The development time of power electronics and converter topologies can be shortened by the use of simulation tools.

Sentaurus Device combines a good numerical model of power electronics devices and complex external circuits. It's capable to simulate the IGBT switching behaviours applying different gate unit settings in HVDC Light™.

The numerical model of the IGBT is studied in the thesis. The results of the IGBT fine-tuning are carried out. Implementing the IGBT model with its gate unit circuit using Sentaurus Device, the impact of various gate drive settings on the IGBT switching losses is demonstrated.

***Key words: Sentaurus Device, IGBT, numerical model, HVDC Light*™ *gate unit, switching losses***

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Last but certainly not least, I will give my gratitude to my friends in Västerås and Göteborg. Thanks for your company and help during my master study in Sweden.

I dedicate this thesis to my mother and father.

Västerås, June 2009

Lei Zhou

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# Chapter 1
# Introduction

This chapter gives a brief introduction of the background concerning the field of the thesis. After that, the objectives and the outline of the whole work are also included in the end.

## 1.1 Background

The use of simulation tools is of great value in the process of developing new power devices (diode, thyristor, IGBT, MOSFET etc.), new converter topologies (e.g. for motor drives, power distribution and transmission etc.). Device and circuit designs can be tested under various operating conditions by using simulation tools before the devices and circuits are actually built. Thus, the development time can be shortened.

For power devices and converter circuits, there are a number of commercially available simulation tools, e.g. SPICE, SABER for circuit simulations, MINIMOS, ATLAS, MEDICI, DAVINCI for device simulation etc. The circuit simulation tools are good at simulation of the converter circuits but have rather simple models for the devices, especially power devices. But device simulation tools can simulate the electrical characteristics of semiconductor devices, as a response to external electrical, thermal or optical boundary conditions imposed on the structure.

Sentaurus Device offered by Synopsys has been used by ABB Semiconductors AG, Lenzburg and ABB Corporate Research, Switzerland (CHCRC) and has been proved that it can combine the numerical device model with a fairly good external circuit representation. It would be of great value to establish the simulation environment (Sentaurus Device) in ABB Corporate Research in Sweden for the future projects, mainly for Power Systems applications (HVDC and FACTS).

## 1.2 Objectives

The goal for this Diploma work is to test and evaluate the simulation tool Sentaurus Device at ABB Corporate Research, Sweden (SECRC). The outcome of this study will be a basis for a possible future establishment of this simulation tool at SECRC. The result of the work is that there may be a simulation tool (combining numerical device simulation with fairly good circuit representation) that can be used in the Power Systems applications projects in SECRC.

For testing the simulation tool the new 4.5kV STP+ StakPak IGBT from ABB Semiconductors was used together with an implementation of the HVDC Light™ gate uni. The numerical models of the IGBT were supplied by the manufacturer (ABB Semiconductor AG, Lenzburg) and the HVDC Light™ gate unit to be investigated was given from ABB [1]. The IGBT steady-state characteristics and dynamic properties should be simulated to examine the fitness between numerical model and real device.
The simulation implementing the gate unit with the numerical model of the IGBT should be compared with the experimental data. Several sets of simulations should be

run to study the impact of different gate unit parameters on the IGBT switching behaviors.

## 1.3 Outline of the thesis

### Chapter 2

Sentaurus Device and TCAD software package are described in this chapter. It gives the basic structure of Senataurus Device and the difference between the mixed-mode device simulation and single device simulation.

### Chapter 3

The IGBT numerical model is studied in this chapter. And the fine-tuning of steady-state characteristics and dynamic properties is carried out.

### Chapter 4

In this chapter, the gate unit for HVDC Light™ is described. The single-pulse test is explained to use for the switching transient behavior simulation of IGBT. The command file for Sentaurus Device is carried out.

### Chapter 5

Various gate unit settings are simulated in this chapter. The impact of different settings of gate unit is demonstrated.

### Chapter 6

This chapter summarizes the work in this thesis and brings forward future aims in this field.

# Chapter 2
# Description of Sentaurus Device

## 2.1 Overview

Sentaurus Device is one of the device simulation tools in TCAD (Technology Computer-Aided Design) which is the simulation package offered by Synopsys to develop and optimize semiconductor processing technologies and devices. It was referred to 'DESSIS' before ISE AG sold out the program to Synopsys.

Sentaurus Device is capable of simulating electrical, thermal and optical characteristics of silicon-based and compound semiconductor devices. It simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. [2]

## 2.2 Simulation Flow in TCAD

Synopsys TCAD offers a comprehensive suite of products that includes processing and device simulation tools, as well as a GUI-driven simulation environment for managing simulation tasks and analyzing simulation results.

Figure 2.1 gives the basic structure of the TCAD simulation package.

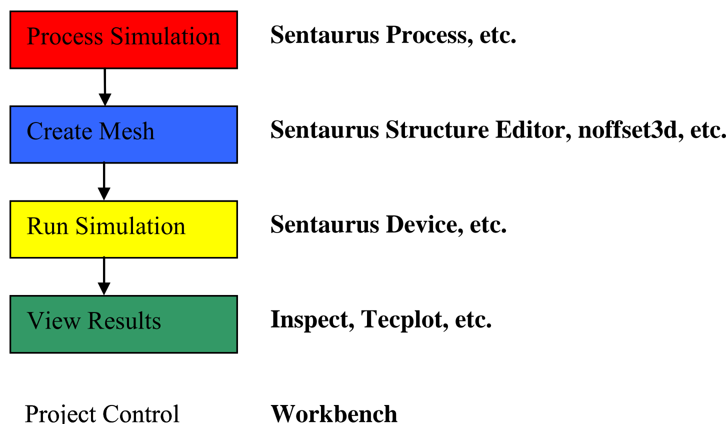


*Figure 2.1: Simulation Packages*

In order to understand how Sentaurus Device works, the structure of the simulation flow is given in Figure 2.2.

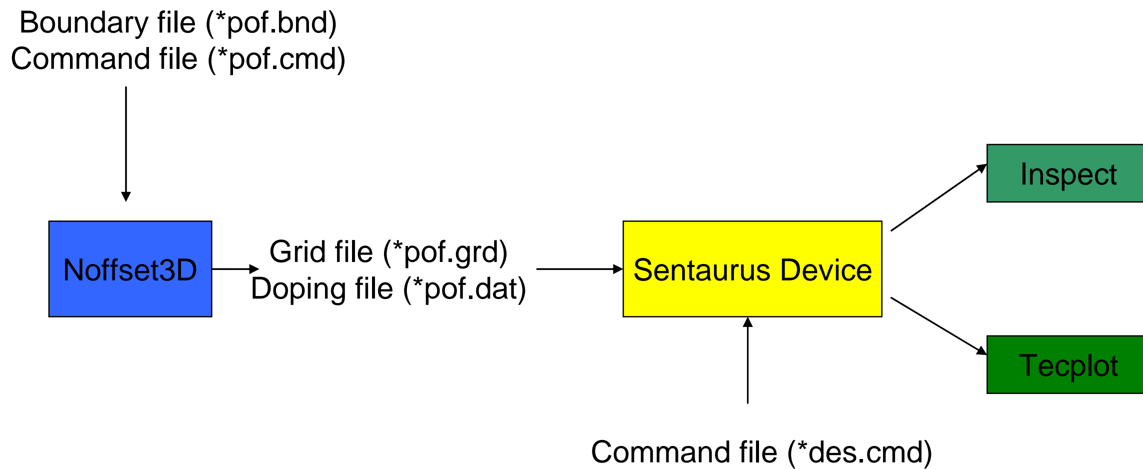


*Figure 2.2: Simulation Flow*

In Figure 2.2, it is explained that the mesh generator Noffset3D takes the boundary and command files to make the grid and doping files for Sentaurus Device. After running the command file for Sentaurus Device, the results can be viewed by Inspect or Tecplot in the form of images or exported data.

## 2.3 Basic Sentaurus Device

In this section, the single device simulation (without external circuits) will be represented.

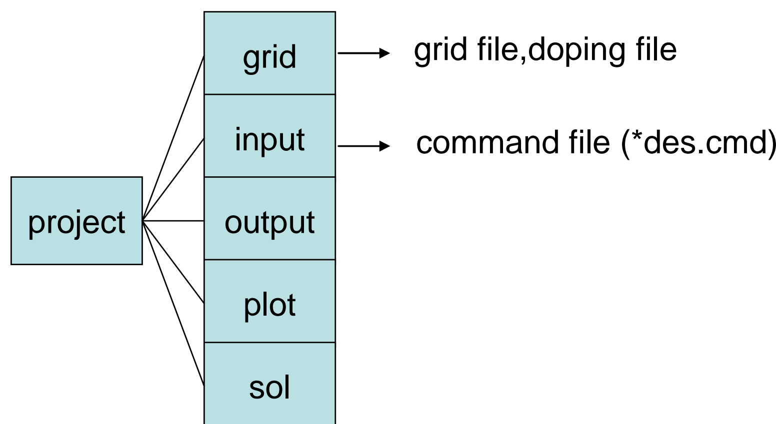


*Figure 2.3: Project Folder Structure*

The mesh generator (e.g. Mesh, Noffset3D, Sentaurus Mesh etc.) takes the grid command file (e.g. *msh.cmd, *pof.cmd, *mdr.cmd, etc.), boundary files to create the grid files for the device simulation. Those files should be created and saved in the folder 'grid' under a project folder, as Figure 2.3 displayed. Since the thesis work is not focusing on the processing simulation parts, the grid command file and how to generate the mesh are not studied in detail here.

In order to run the simulation, it's important to understand the command file for Sentaurus Device (*des.cmd) which should be saved in the folder 'Input'. To start the

simulation, we should go to the project folder and type the command 'sdevice input/*des.cmd' under Linux terminal.

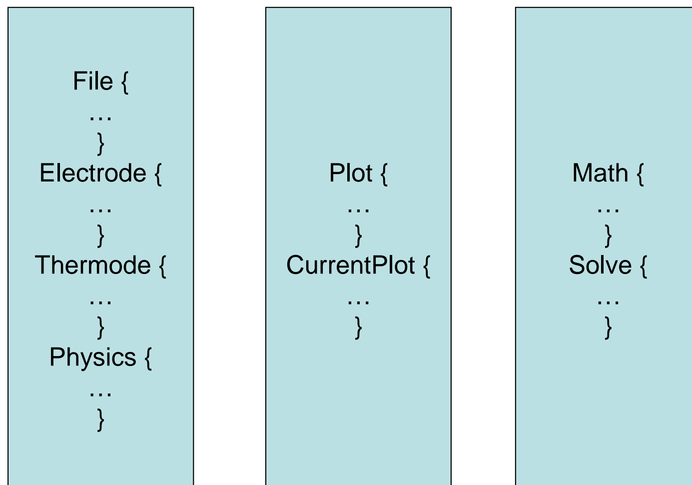


*Figure 2.4: Different Sections for a Sentaurus Device Command File*

Figure 2.4 gives the basic structure of a Sentaurus Device command file. The left block in Figure 2.4 specifies the device. A device is defined by its mesh and doping (File section), contacts and thermodes (Electrode and Thermode sections), and the physical modes which can be selected globally or for specific materials, regions, interfaces (Physics section). The middle block in Figure 2.4 defines the output of the simulation. Plot and CurrentPlot sections specify the results to be saved for a given simulation. The right block in Figure 2.4 specifies the simulation. Different simulations are defined in the Solve section. The parameters for the methods used are defined in the Math section. More examples and explanations about the command file for Sentaurus Device will be given in a later chapter.

## 2.4 Mixed-mode Sentaurus Device

In the previous section, the single device simulation command file is explained. But Sentaurus Device is also a mixed-mode device and circuit simulator. In this section, the command file for the mixed-mode device simulation will be explained.

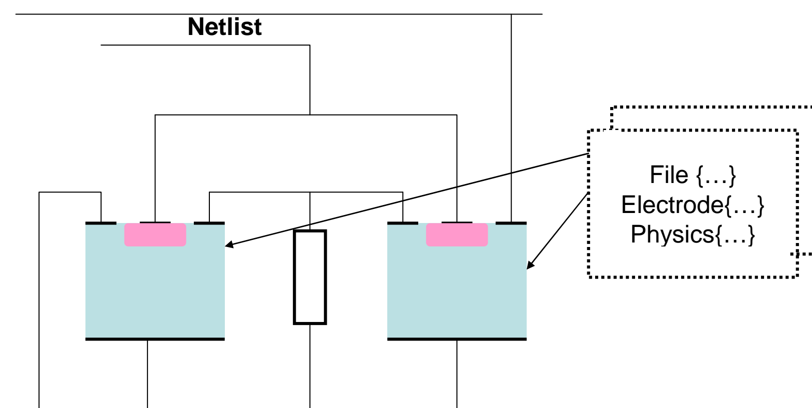


*Figure 2.5: Multiple Devices*

The command file for a multi-device simulation includes the mesh (File section), contacts (Electrode and Thermode Sections), and physical models (Physics Section) for each device. All the devices are defined under the Device sections. Furthermore, a circuit netlist must be defined in the command file to connect each device as showed in Figure 2.5. The System section is required to create and connect devices. Another difference from a single device simulation is that the Solve commands must be specified to solve the whole system of devices.

Sentaurus Device provides four different types of compact models in mix-mode simulations: SPICE, HSPICE, Built-in, User-defined. In this thesis work, SPICE compact models are mainly used. More details will be explained in a later chapter.

# Chapter 3
# Numerical Model of IGBT and Its Fine-tuning

The IGBT (Insulated Gate Bipolar Transistor) is led to an increasing interest in industrial applications, e.g. HVDC light, SVC light, wind power generators, etc.
To understand Sentaurus Device and evaluate its value on future projects for Power System applications, a study on IGBT (Insulated Gate Bipolar Transistor) under Sentaurus Device is necessary and with great value.

## 3.1 Basic Structure of IGBT

An IGBT is the combination of a BJT (Bipolar Junction Transistor) which has lower conduction losses in the on state, but has longer switching times and a MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) which can be turned on and off much faster, but has lager on-state conduction losses. IGBT combines the best qualities of both types of devices.

*Figure 3.1* gives the basic structure of an IGBT. As we can see from the figure, the n+pn-n+ structure forms the n-channel MOSFET. The presence of p+ layer forms the drain (collector) of the IGBT.

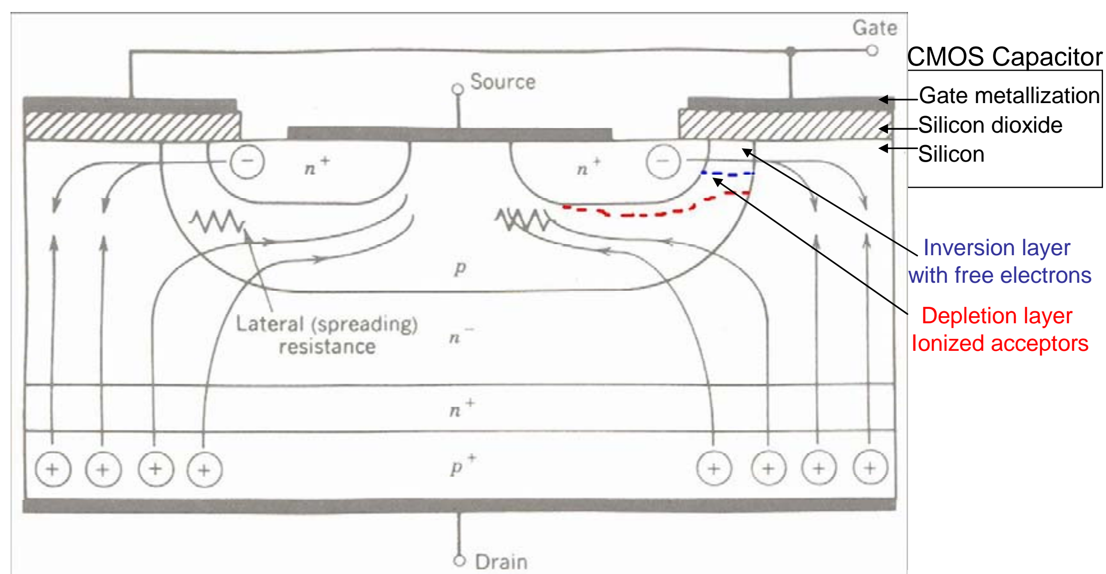


*Figure 3.1: On-state Current Flow paths of an IGBT*

The gate-source (gate-emitter) voltage controls the state of an IGBT. When Vgs (gate-source voltage) is less than the threshold voltage, there's no inversion layer created to connect the drain (collector) to the source (emitter). Hence, the device is in the off state.

The on-state operation of an IGBT is showed in Figure 3.1. The gate metallization, the silicon dioxide underneath the gate conductor and the silicon under beneath the silicon dioxide form a MOS capacitor. When a small positive gate-source voltage is applied to the MOS capacitor, a depletion region is formed at the interface between the SiO2 and the silicon by forcing the positively charged holes away from the

interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If the gate-source voltage is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface. The inversion layer shorts the n- drift region to the n+ source region. An electron current which flows through this inversion layer causes a substantial hole injection from the p+ drain contact layer into the n- drift region. The injected holes move across the drift region by both drift and diffusion with a variety of paths and reach the p-type body region. When the holes are reaching the p-type body region, their space charge attracts electrons from the source metallization that contacts the body region, and the excess holes are quickly recombined

# 3.2 Numerical Model of IGBT and Diode

The numerical simulation of the IGBT and the diode is based on FEM (Finite Element Method). The exact knowledge of various device parameters like layer thickness, carrier lifetime, doping concentration is required. In this thesis, the models as showed in Figure 3.2 and Figure 3.3 are taken from ABB Corporate Research, Switzerland and ABB Semiconductor AG, Lenzburg.

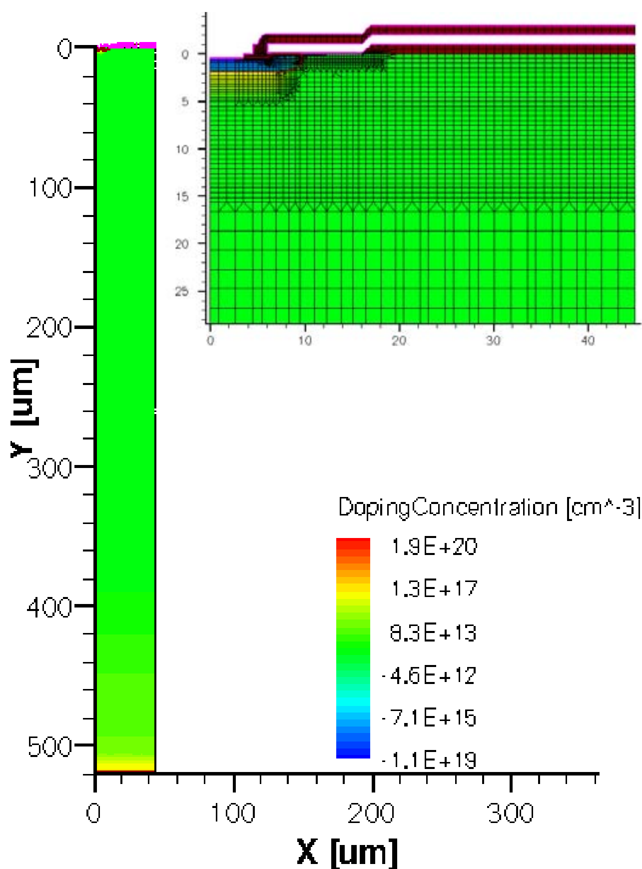


*Figure 3.2: Mesh and Grid of IGBT Model in Sentaurus Device*

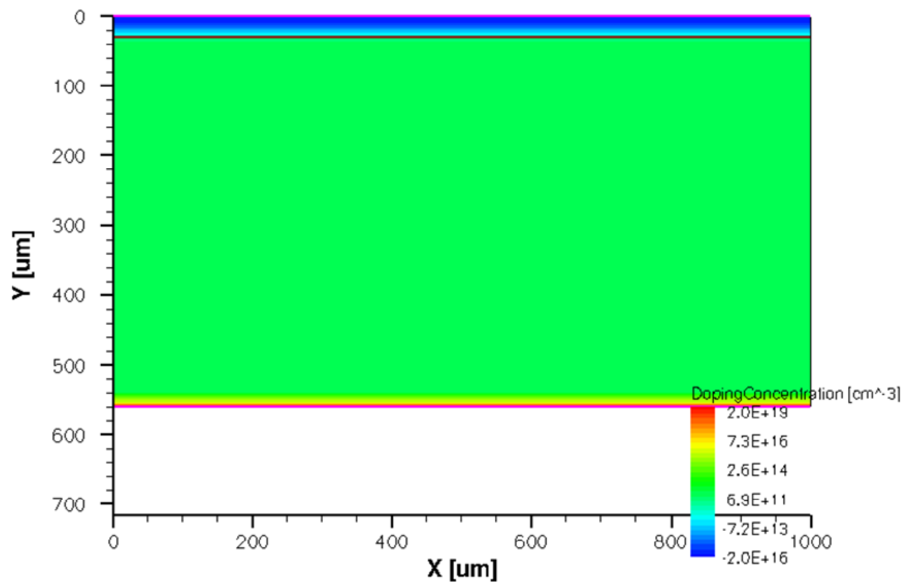


*Figure 3.3: Grid of Diode Model in Sentaurus Device*

As we can see from Figure 3.2, the IGBT is represented using a half of its elementary cell (symmetry). The left part in Figure 3.2 shows the whole half of the elementary cell and the right part shows a zoom in around the MOSFET region. In order to minimize the size of the grid, all other cells and the junction termination periphery are neglected. But we should keep in mind that the real power semiconductor device consists of a large number of such elementary cells in parallel. In order to represent the whole semiconductor device, the so called 'areafactor' is defined in the simulation.

.

*Figure 3.4: ABB StakPak™ K Series Press-pack IGBT 5SNA 200045K0301*

The models showed in Figure 3.2 and Figure 3.3 represents the real IGBT as displayed in Figure 3.4. The IGBT in Figure 3.4 is an ABB StakPak™ K Series Press-pack IGBT 5SNA 200045K0301 which is a 4.5kV 2000A device [3]. It consists of 6 modules (so called sub-modules) on the device as we can see from Figure 3.4. There are 6 IGBT chips (dies) and diode chips (dies) in each sub-module. So the total number of the IGBT dies is 36, which is the same for the diode dies, on the IGBT showed in Figure 3.4.

In order to build the same model as the device showed in Figure 3.4, the areafactor should be defined. It can be defined in the electrode section. In Sentaurus Device, the simulated cell area is the width of the IGBT grid (45e-4cm), as showed in Figure 3.2 above, multiplied by 1e-4cm (=the default extension along the z-coordinate). It results in a cell area of 4.5e-7cm2 if the area factor is set to 1. The active area of the IGBT die in the 4.5kV StakPak device in Figure 3.4 is 1.1cm2 which corresponds to an area factor=2.444e6 (2.444e6 × 4.5e-7 = 1.1 cm2). Because there are 36 dies in the complete module, we here use the area factor=8.8e7 (36 × 2.444e6) if we want to simulate the complete device (total active IGBT area 39.6 cm2).

From Figure 3.3 , the width of the diode cell grid is 1000e-4cm. The simulated cell area then equals 100e-7cm2. The active area of the diode dies in the real device showed in Figure 3.4 is 1.06cm2. The total diode area in the module is then 36 × 1.06 = 38.16 cm2 corresponding to an area factor for the diode of 3.816e6 (100e-7 × 3.816e6 = 38.16 cm2).

Similar to the theoretic structure of the IGBT, the contact, oxide and silicon are defined in Figure 3.2. Applying the different doping concentration and materials forms the n+pn-n+p+ structure as displayed in Figure 3.2.

## 3.3 Device Definition for IGBT in Sentaurus Device

```
Device igbt {
     file {
          grid   = "grid/HThp47igbt_tau_mdr"
          doping = "grid/HThp47igbt_tau_mdr"
          lifetime="grid/HThp47igbt_tau_mdr"
          param  = "input/par10q.par"
     }
     electrode {
          #collector
          { name="cathode" voltage=0 areafactor=8.8e7 }
          #emitter
          { name="anode" voltage=0 areafactor=8.8e7 }
          #gate
          { name="gate" barrier=-0.55 voltage=0
areafactor=8.8e7 }
     }
        physics {
          temperature=400
          thermodynamic
      EffectiveIntrinsicDensity(BennettWilson)
      OxideCharge = 0
      Recombination ( SRH(DopingDependence
ExpTemperatureDependence)
          Auger Avalanche(Eparallel) )
                Mobility ( DopingDependence
                HighFieldSaturation
                NormalElectricField
```

```
                    CarrierCarrierScattering )
            }
        math {
        }
}
```

The routines above define the IGBT device in Sentaurus Device.

The mesh, doping files and carrier lifetime profiles are defined under the File section (inside the Device section).

Collector, Emitter, Gate (Drain, Source, Gate) are defined under the Electrode section. The voltage applied on collector and emitter is 0. The voltage applied on the gate depends on different types of simulation. For the devices like IGBT, MOSFET with the MOS capacitor, the metal-semiconductor work function difference should be defined. This is defined in the Barrier value. It's the difference between the metal Fermi level in the electrode and the intrinsic Fermi level in the semiconductor. The value is consistent with the n+ polysilicon doping.

In the physics section, the physics of the numerical model of IGBT in Sentaurus Device is defined.

The temperature value is set in the physics section. Different temperature affects the thermal equilibrium of semiconductor.

The simulation mode is also defined in this section. The drift-diffusion, thermodynamic, hydrodynamic and Monte Carlo simulation modes are available in Sentaurus Device. The drift-diffusion mode is the isothermal simulation. It is described by the basic semiconductor equations which are the Poisson equation and the electron and hole continuity equations.

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap} \qquad 3.1$$

$$-\nabla \vec{J}n = qRnet + q\frac{\partial n}{\partial t} \quad ; \; -\nabla \vec{J}p = qRnet + q\frac{\partial p}{\partial t} \qquad 3.2$$

For the drift-diffusion model, the current densities for electrons and holes are given by:

$$\vec{J}_n = -nq\mu_n \nabla \phi_n ; \vec{J}_p = -pq\mu_p \nabla \phi_p \qquad 3.3$$

In our simulation, we use the thermodynamic simulation mode. It extends the drift-diffusion approach to account for electrothermal effects, under the assumption that the charge carries are in the thermal equilibrium with the lattice. The carrier temperature and the lattice temperature are defined by a single temperature T.

The silicon bandgap narrowing model is defined in the physics section as well. It determines the intrinsic carrier concentration. In our simulation, for the IGBT, the BennettWilson is used.

The initial gate oxide charge is defined also. Since it affects the MOS capacitor, it's important to set it to 0.

Another important factor in the physics section is the definition for recombination. Any electron which exists in the conduction band is in a meta-stable state and will eventually fall back to a lower energy position in the valance band. When the electron falls back down into the valence band, it also effectively removes a hole because it should be kept as an empty valence band state. There are three types of recombination: Radiative recombination, Shockley-Read-Hall (SRH) recombination and Auger recombination. In our simulation, SRH and Auger recombination are used. SRH recombination is the recombination through the defects. It doesn't occur in perfectly pure, undefected materials. Auger recombination is most important in heavily doped or heavily excited material.

The carrier mobility is also described in the physics section. The constant mobility model is only used for the undoped materials. For the doped materials, the carriers scatter with the impurities. This leads to a degradation of the mobility. In our simulation, the mobility is the doping-dependent mobility.

## 3.4 Fine Tuning of IGBT

Some simple simulations will be presented in this section to examine the match between the numerical models with the real experimental IGBT. These simulations include the blocking capability, on-state characteristics, gate threshold voltage, turn-on and turn-off of IGBT.

Though the exact mapping of the IGBT geometry and structure was taken from the manufacturer, the first simulation result is far off from the experimentally measured data. The explanation could be that any power semiconductor device is a three-dimensional object with a significant number of different regions with specific functions, for example the large areal fraction of the junction termination regions, regions for the metallization of the gate bonding pad and structural variations along a cathode stripe.

Therefore, the fine tuning of the device is necessary. But those tasks were done by ABB Corporate Research, Switzerland [7]. In order to understand the numerical model and software package better, the basic study on the grid optimization part is required. All the simulation results presented in this thesis report are from the final grids from ABB Corporate Research, Switzerland. However, we also made these simulations in this study.

The optimization process basically is divided to two parts: steady-state characteristics and dynamic properties.

### 3.4.1 Steady-state Characteristics

The fine tuning starts from the steady-state characteristics such as device blocking capability, on-state characteristics, gate threshold voltage. At this stage, appreciate doping files are applied in the internal IGBT structure to match the simulation results with the experimental data.

For example, changing the anode-emitter peak doping concentration could reduce the IGBT on-state voltage drop; the threshold voltage is affected by the doping density in the p-doped p-base region representing the channel; the width of this p-base region affects the saturation current density.

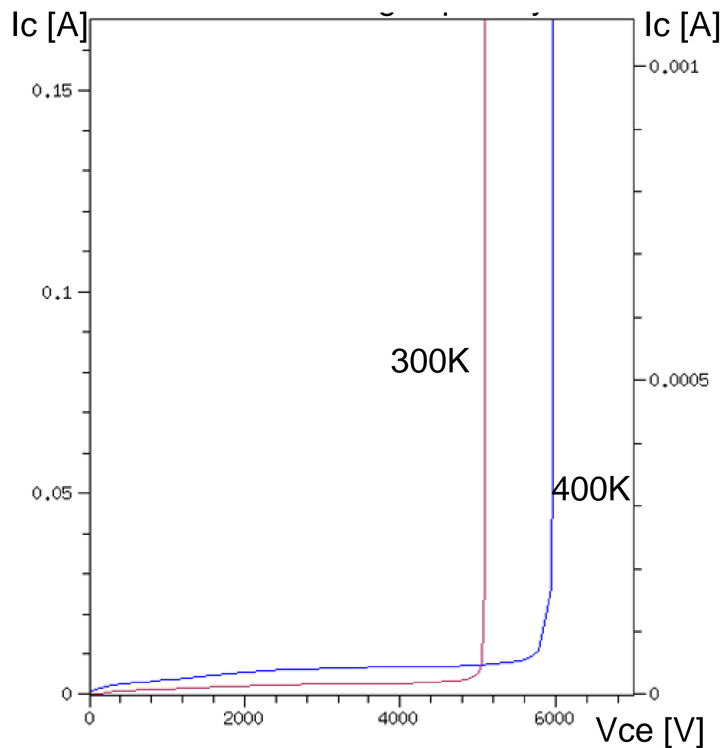


*Figure 3.5: IGBT Blocking Capability*

Figure 3.5 gives the blocking capability both at room temperature 25°C and 125°C. From the datasheet of 5SNA 200045K0301, the IGBT blocking voltage capability is 4.5kV. At room temperature, the simulation result is around 4.7kV. It matches the experimental data in the acceptable range.

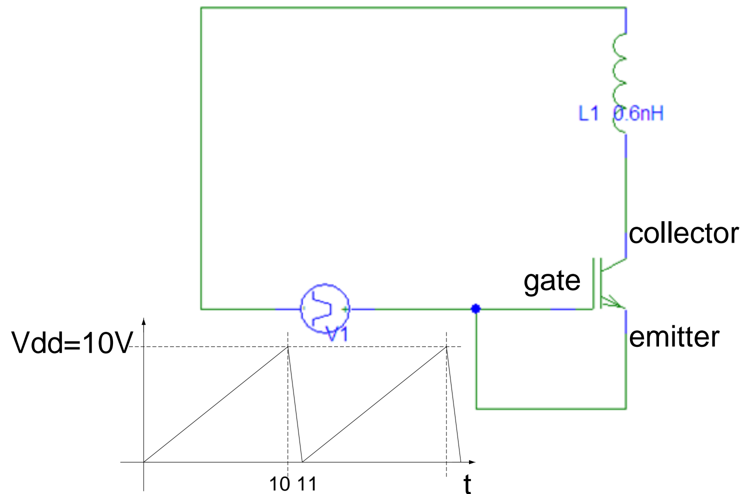

*Figure 3.6: Setup of Gate Threshold Voltage Simulation*

Figure 3.6 is the simulation setup for determining the gate threshold voltage. The voltage source Vdd as showed in Figure 3.6 increases by the time. The 'transient' simulation starts at t=0, and ends at t=10s. That means the voltage applied on the gate varies from 0V to 10V. When IGBT is conducting, Ic increases distinctly at one point which is the gate threshold voltage.

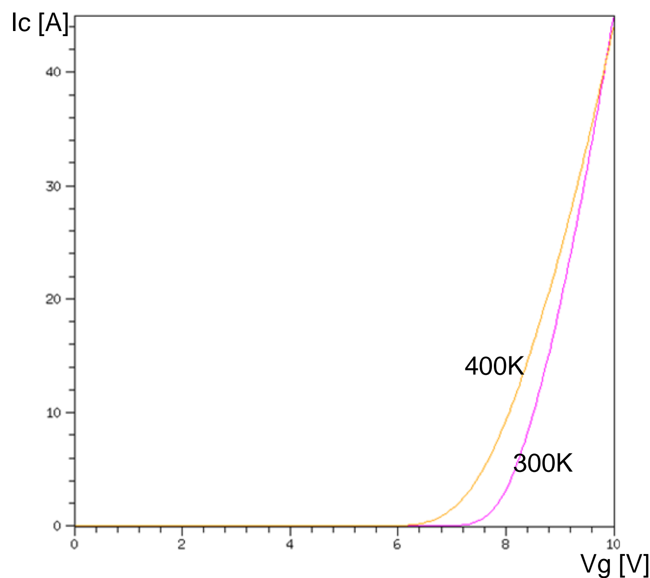

*Figure 3.7: Gate Threshold Voltage*

The simulation result is displayed in Figure 3.7. At room temperature 25°C, the threshold voltage is around 7V which matches well with the datasheet [3]. The datasheet shows that the gate-emitter threshold voltage is in the range between 5.5 and 7V.

The on-state characteristics at 125°C from simulations and datasheet are displayed in Figure 3.8. The different gate voltages applied at the gate give a series of U-I characteristics.

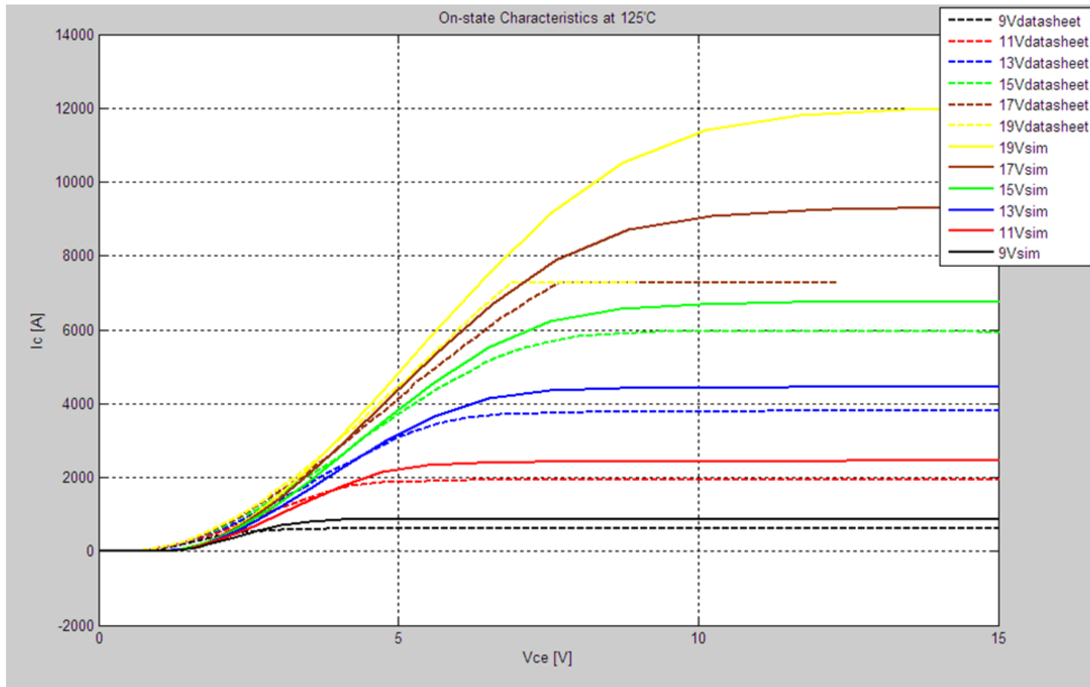


*Figure 3.8: On-state Characteristics at 125°C from Simulation and Datasheet*

From Figure 3.8, it's obvious that the saturation current doesn't agree well. Because during the fine-tuning, the common contradiction arises when a good fit of the saturation current density and the device on-state voltage is needed at the same time. The fine-tuning has been done in ABB Corporate Research, Switzerland mainly focuses on the good agreement in current levels up to 4000A for around 15V on the gate, which can be observed in Figure 3.8 (the green curves).

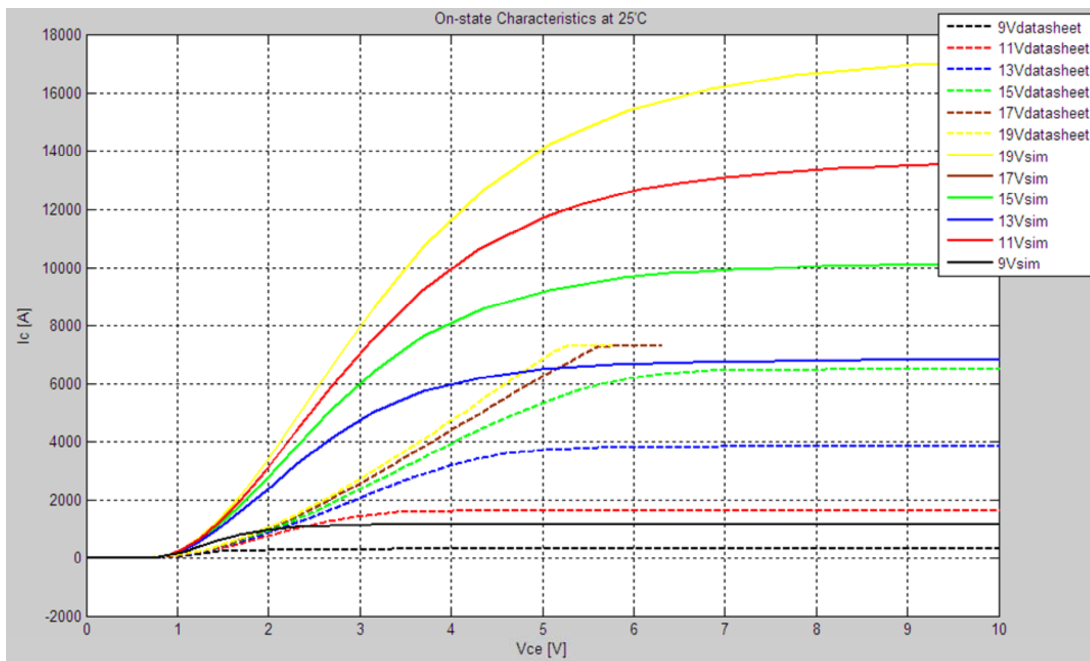


*Figure 3.9: On-state Characteristics at 25°C from Simulation and Datasheet*

The on-state characteristics at 25°C from simulations and the datasheet are showed in Figure 3.9. The simulation results don't agree with the data from the datasheet.

Because the fine-tuning done by ABB Corporate Research, Switzerland is aiming for 125°C which is the operating temperature will be used in the later simulations.

## 3.4.2 Dynamic Properties

The second optimization loop which focuses on turn-off and turn-on switching losses should be followed after the first fit to steady-state data. The shape of the IGBT collector tail current which affects the turn-off behavior depends on the initial steady-state distribution of the modulated charge in the n-base. It means that improving the tail current behavior may cause adverse results to the just optimized steady-state characteristics. This could explain why it may seem there's not a particularly good fit to the experimental steady-state characteristics. The fit quality for the transient simulations is with higher priority.

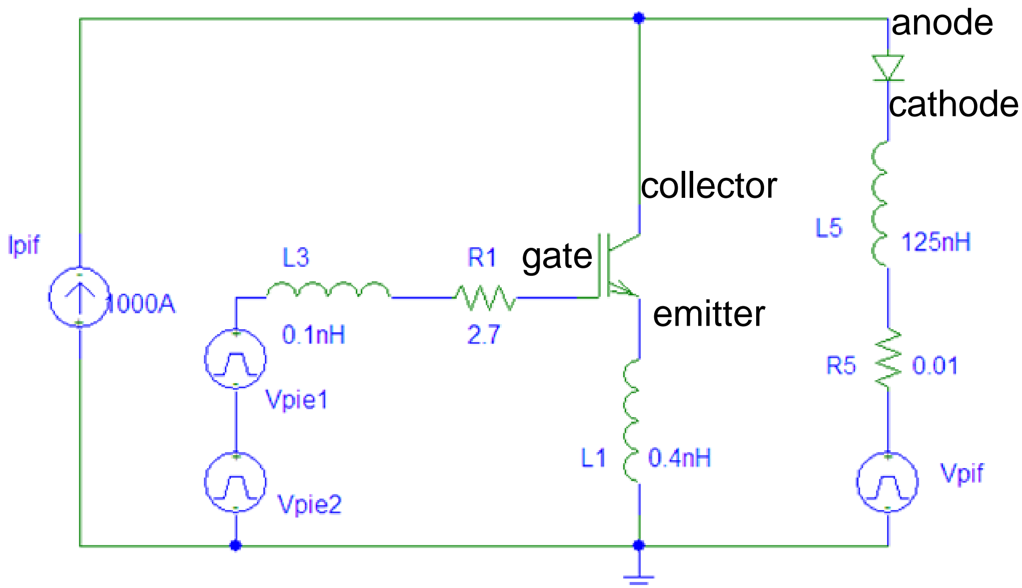


*Figure 3.10: Simulation Setup for Turn-off and Turn-on Switching Behaviors*

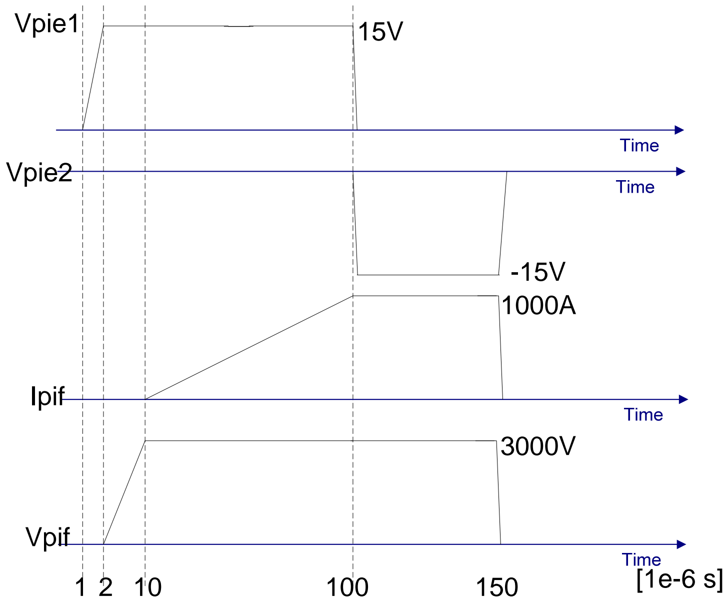


*Figure 3.11: Current and Voltage Sources for Turn-off*

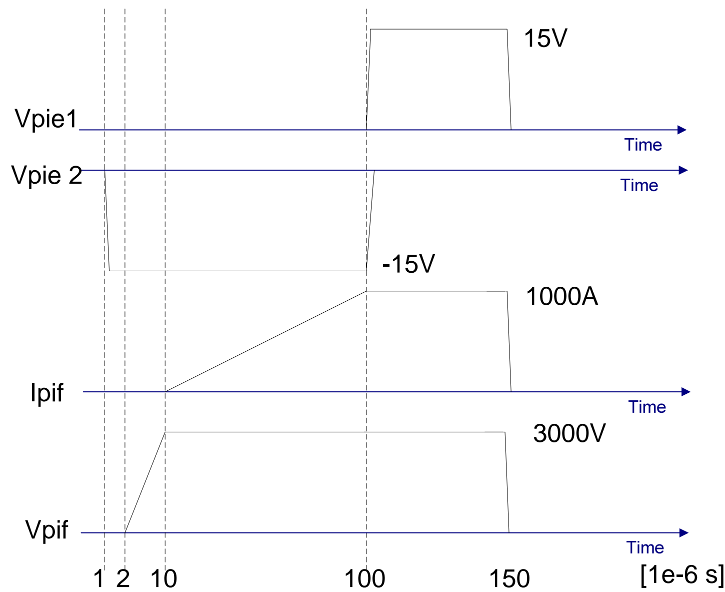


*Figure 3.12: Current and Voltage Sources for Turn-on*

Figure 3.10 shows the circuit for a turn-off and turn-on switching simulation in Sentaurus Device. Vpie1 and Vpie2 are the voltage sources feeding to the gate. By changing their sequence, it controls turn-on and turn-off of the device as displayed in Figure 3.11 and Figure 3.12. Ipif is the current source with an amplitude of 1000A, when Vpif is the voltage source with amplitude of 3000V. They represent the operating condition in the simulation. Both the device turn-off and turn-on is made at time position 100e-6 s.

The area factor in these simulations is 3.473e7 which is half of the ABB StakPak IGBT model. It represents the previous ABB IGBT product ( HiPak device). The datasheet [4] of HiPak IGBT shows Eon=3.0J, Eoff=4.3J at 125°C. Figure 3.13 and Figure 3.14 give the turn-on and turn-off behavior at 125°C of the IGBT.

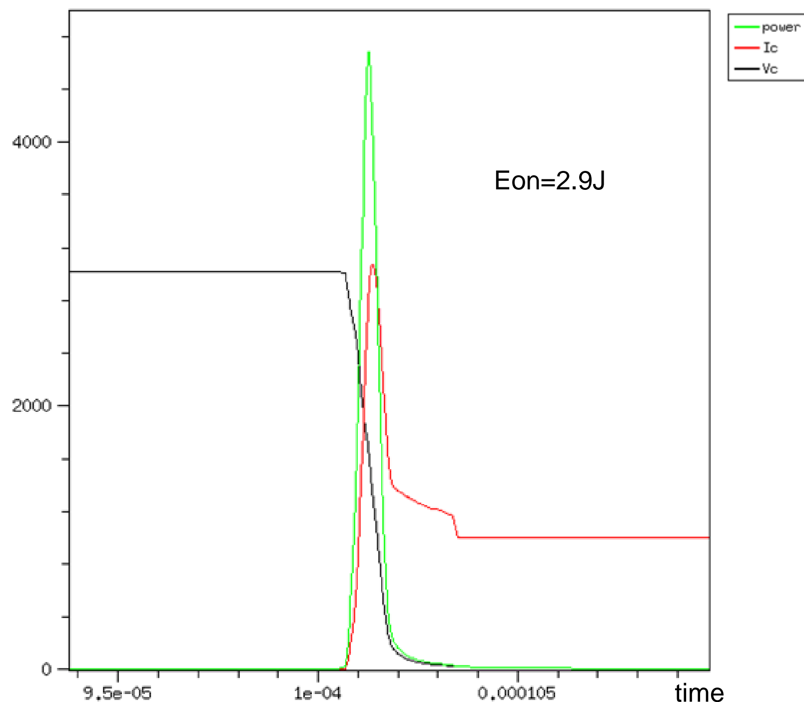

*Figure 3.13: Turn-on Simulation at 125°C*

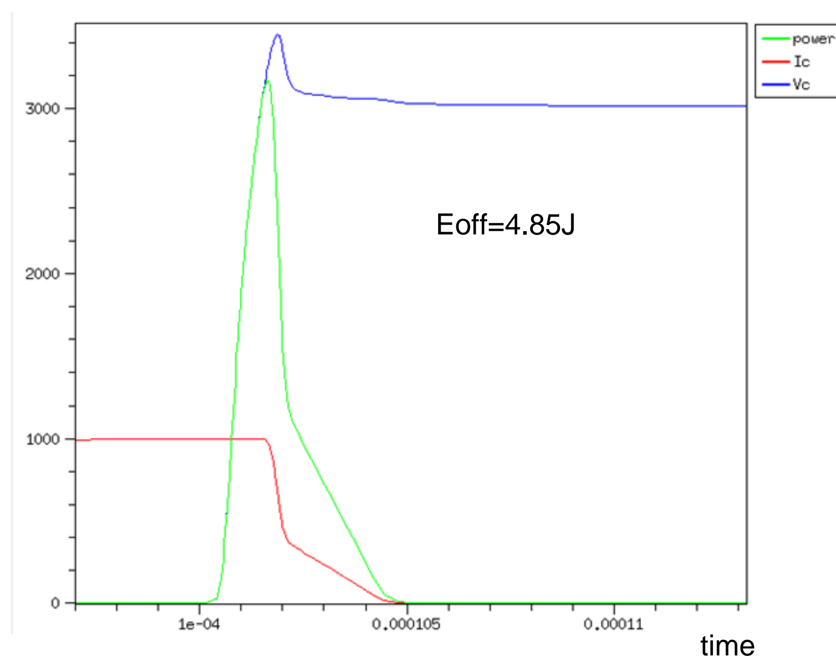


*Figure 3.14: Turn-off Simulation at 125°C*

The simulation results are in a good fit with the datasheet. Though the simulation results represent another IGBT device (HiPak), we conclude the fine-tuning of dynamic process also is sufficient for the StakPak device.

## 3.4.3 Conclusion

Through the fine-tuning of IGBT, the steady-state characteristics and dynamic properties of the numerical model fit better with the datasheet of the real device. The process is necessary in order to represent the good simulation model of IGBT.

However, the agreement between the simulations and datasheet is not perfect. In the first loop of optimization, the steady-state characteristics are considered. But due to the contradiction between the saturation current density and device on-state voltage, there are some mismatches between the simulations and datasheet. The second optimization loop which focuses on the dynamic properties also affects the just optimized steady-state characteristics. But we give the priority to the dynamic properties.

We conclude that both the steady-state characteristics and dynamic properties of the IGBT numerical model are sufficient for the simulations which combine with its gate unit.

# Chapter 4
# IGBT Switching Transient Simulation under Sentaurus Device

The semiconductor losses are the main part of the total losses of the whole HVDC Light™ system. The turn-on and turn-off switching events generate the large part of the semiconductor losses. Except the impact of the IGBT and diode combination used, the gate control pattern generated in the gate unit also has a strong effect on the switching losses.

The simulation of IGBT switching transient behaviors is used to find the gate control pattern which minimizes the switching losses. Sentaurus Device can perform the mixed-mode simulations which combine the numerical device and a complex spice based circuit. Sentarus Device is able to perform those simulations. But the complexity of the spice part is limited because it may lead to the numerical convergence problems. So the simplified circuit and gate unit model are required.

## 4.1 Description of Single-pulse Test Circuit

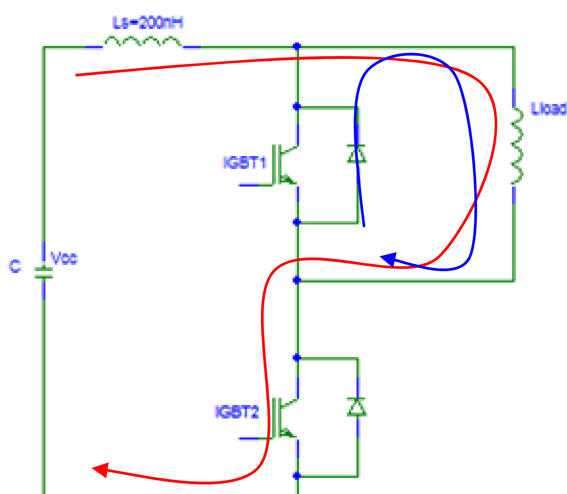


*Figure 4.1: Schematic of Single-pulse Test Circuit*

Figure 4.1 is the single-pulse test circuit used in the measurements of the devices. The upper IGBT1 is always off. When the lower IGBT2 is turned on, the current goes through it, as the red line in Figure 4.1 and the current increase rate is controlled by the capacitor voltage Vcc and the inductance Lload. When IGBT2 is turned off, the upper diode provides the free wheeling path, as the blue line in Figure 4.1. A schematic of the switch sequence pattern and the resulting currents in the two devices in the single pulse circuit is shown in Figure 4.2. Ls represents the loop stray inductance in the HVDC Light™ converters.

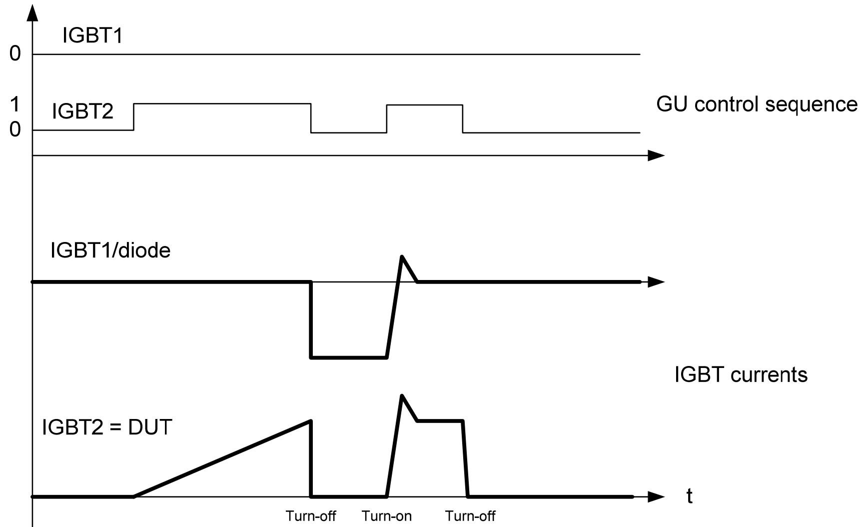


*Figure 4.2: Single-pulse Test Switching Sequence*

By measuring the current and voltage across the lower IGBT2, the switching transient behaviors in turn-on and turn-off of IGBT2 are tested.

Because IGBT1 doesn't operate during the test, it would be easier to delete it in the simulation setup. When the capacitor is charged up, it's treated as a constant voltage source which is used in the simulation setup. The inductance load due to its large value is substituted by a constant current source in the simulation setup (this is because during the short times involved in the switching sequences the current through the inductor will be almost constant).

Figure 4.3 shows the simplified circuit setup in simulations. Considering the complicated numerical model of IGBT, this setup will reduce the simulation work in Sentaurus Device.

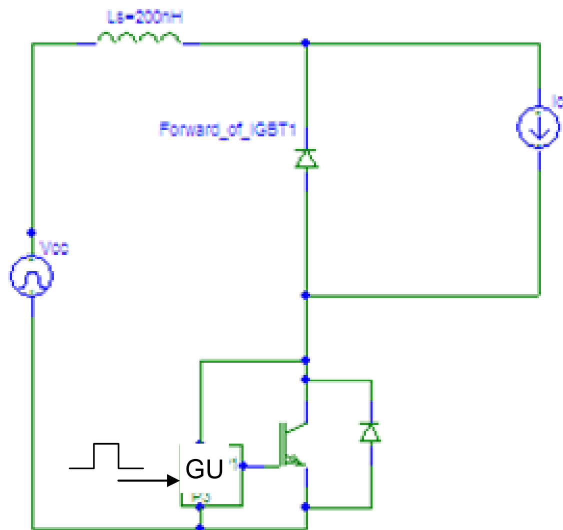


*Figure 4.3: Simplified Circuit in Simulations*

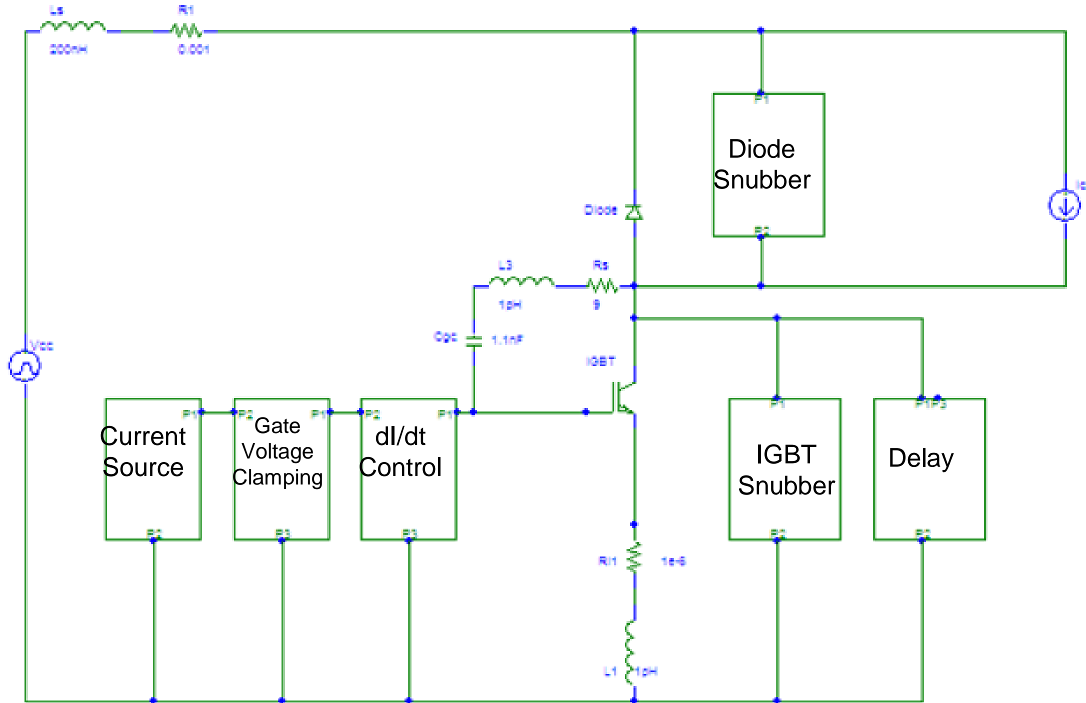


*Figure 4.4: Simulation Circuit in Sentarus Device*

Figure 4.4 gives the basic structure of the simulation circuit. For the diode and IGBT, the snubber circuits are applied. The function of the snubber circuit is to reduce the electrical stresses applied on the device. The delay block in Figure 4.4 is used to represent the delays generated from the electronics in the real gate unit as well as the measurement probes. The capacitor Cgc is a feedback from collector to gate. The main purpose of the Cgc is to give a feedback at turn-off to have an active control of the dV/dt at turn-off.

The gate unit is divided into three parts: current source, gate voltage clamping, dI/dt control. More detail about the gate unit will be discussed in the next section.

## 4.2 Gate Unit Implementation in Sentaurus Device

The function of the gate unit is to switch the IGBT from the off state to the on state and vice versa. The different gate voltage patterns generated from the gate unit will give the different shapes of the voltage and current curves across the IGBT. So changing some parameters in the gate unit may affect the switching losses.
As showed in Figure 4.4, the gate unit mainly consists of the current source, gate voltage clamping, dI/dt control.

### 4.2.1 Current Sources

The gate current sources consist of two parts. One part is the turn-on current sources. They are controlled by the voltage-controlled switches. One group of switches is controlled by Vce. Another group of switches is controlled by gate threshold voltage. The second part is the turn-off current sources which are controlled by Vce.

The current source Ig actually consists of several different current sources. The operation of the current sources depends on the collector and emitter voltage Vce. The different gate currents feeding the gate capacitance gives a good operation and takes care of the device spread when connecting many IGBTs in series. Different current sources combinations give different turn-on losses.

## 4.2.2 dI/dt Control at Turn-on

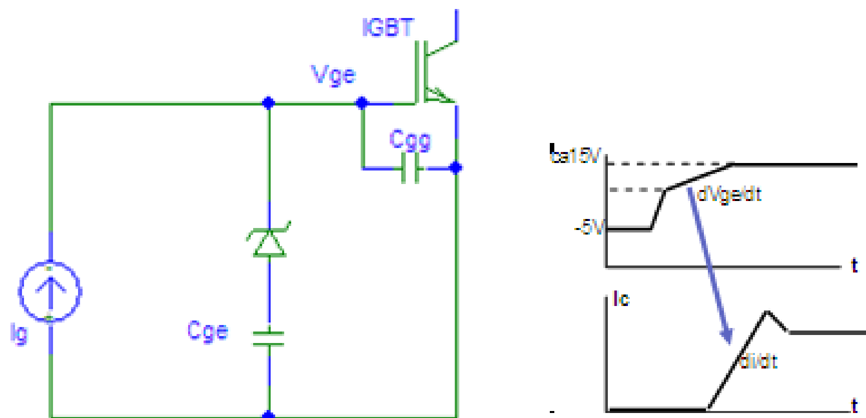


*Figure 4.5: Principle of dI/dt Control of IGBT Turn-on*

The turn-on dI/dt of IGBT is a function between the gate voltage and the output of the device, as showed in Figure 4.5. The dI/dt control is the correlation with the dVge/dt of the gate voltage. The dVge/dt is controlled by constant current sources providing Ig to charge the gate capacitance Cge. The switching speed at turn-on is thereby controlled by Cge and Ig.

An external Cge is used to give a better controlled dVge/dt (and dIc/dt) and minimize the device variations of the internal gate capacitance, Cgg, of the IGBT to have a more stable performance. The zener diode indicates that the capacitor Cge is charged by the current source Ig only for a gate voltage level above the zener voltage.

In the Sentarus Device simulation circuit, the zener diode is represented by a voltage source and a normal diode. Vdis and the switch (Swdis) discharges Cge before the IGBT turn-on.

## 4.2.3 Gate Voltage Clamping

When the gate voltage Vge has reached a certain level Vge(th), the current sources should be switched off and a clamping circuit should be switched in to keep the gate voltage constant during the on-state of the IGBT. It keeps the gate voltage stable at a high level which ensures a low on-state voltage of the IGBT.

The clamping circuit consists of the positive gate clamping section (the left part with voltage source Vclp) and the negative clamping section (the right part with voltage

source Vcln) which give the stable voltage when the IGBT is at on and off state, respectively. The positive clamping consists of a 'passive part' (Diclp, Rclp, Cclp1 and Cclp2) and the 'active' clamping through the switches Swclp1 and Swclp2 that actively goes in at Vge>Vge(th). This is mainly done to be able to more strongly clamp the gate voltage so it does not raise too high in short circuit.

The Vge(th) level also influences the turn-on switching behavior. If the level is too low, the tail of Vce will be high which gives higher turn-on losses. But too high Vge(th) may cause a device failure during the short-circuit testing because it influences the peak current value.

## 4.3 Command File in Sentaurus Device

The command file is referred to Appendix.

The device section to define the IGBT and diode in Sentaurus Device is similar as the case explained in Section 3.3.

All the components except the IGBT and diode used in the circuits discussed in the previous sections are the spice models. In the file section, it defines the spice path which gives Sentaurus Device the access to the spice components. Meanwhile, the output and plot files are also defined in the file section.

The simulation circuit, which is following the explanation in the previous parts in this chapter, is built in the system section.

The voltage-controlled switches are used in the gate current source unit. They control the different levels of currents feeding into the gate which during turn-on depend on the IGBT gate-emitter voltage and collector-emitter voltage, and in turn-off they depend on the collector-emitter voltage. Due to the complexity of the IGBT model and the spice external circuits, there's a substantial convergence problem in the simulation. And all these convergence problems occur on the voltage-controlled switches because the IGBT gate-emitter voltage and collector-emitter voltage are not stable at one value during the simulation. There are some possible ways to overcome the convergence problems on the switches. For example, it could be achieved by changing the math section settings and solve section settings.

The math section specifies the defaults for the different solve commands. The transient simulation is controlled by the different keywords in the math section. In our simulation, the simpler backward Euler (BE) transient mode is used. The error control of the nonlinear equations convergence is also needed during a transient simulation.

In the solve section, the coupled command activates a Newton solver over a set of equation-variable pairs which are the Poisson equation, electron and hole continuity equations. The transient command is used to perform a transient time simulation. It must start with a device that has already been solved. The simulation continues by iterating between incrementing time and re-solving the device.

The convergence problem can be overcome by changing the settings in the math and solve sections. For most problems, Newton iterations converge best with full derivatives. But in some cases by switching off mobility and avalanche derivatives (AvalDerivatives, Derivatives), it improves the convergence performance. Under the transient command, the convergence performance could be changed by changing the increment and decrement level or by applying the plot command (e.g, plot{Range=(500,505) Intervals=500} to force the transient simulation to compute solutions for the specified time point.

It's possible to overcome the convergence problems by the ways mentioned above. We did apply these methods and some switches perform well without any convergence problem, but not for all. So another strategy is applied in the simulation to overcome the convergence problems.

Because these switches are used to control the current source, we can change the current source time sequence instead of using the switches if we can know the exact time when the IGBT gate-emitter voltage and collector-emitter voltage reach the specified level. This is done by tracking down the time when the convergence problem occurs (the same time when the gate-emitter voltage and collector-emitter voltage reach the specified level where the switch should act). Though it's a bit time-consuming, it makes the simulation run without any convergence problem.

# Chapter 5
# Sentaurus Device Simulation Results

In this chapter, the simulation results based on different gate unit settings will be presented. The simulation data will be compared and analyzed with the experimental data

## 5.1 Pre-charging of Snubber Capacitors

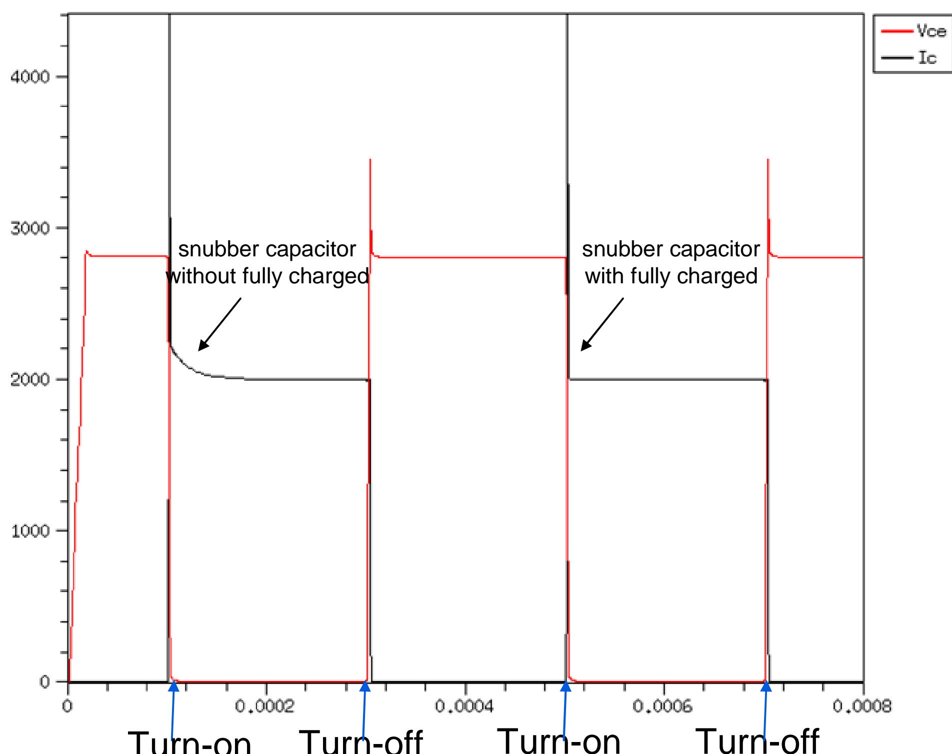


*Figure 5.1: Double Pulse Sequence Simulation*

In our simulation, there are two turn-on switching events and two turn-off switching events as displayed in Figure 5.1. But the turn-on curve at 100µs is different from the turn-on curve at 500µs. At 100µs, a slower decay of the current takes place, as showed in Figure 5.1. The reason is that the snubber capacitors are not fully charged to the snubber voltage source 3000V at the turn-on at 100µs.

The double pulse sequence simulation is the solution to this problem. And the second pulse should be used for analysis.

## 5.2 Comparison with Measurement Data

It's always important to examine the simulation data with the measurement data. The available measurement data used the following circuit and gate unit settings: Ls=200nH, Cgc=1.1nF, Cge=1000nF, Vcc=2700V, Ia=2000A, T=400K,

Vge_clamping=13.7V, Lge=600pH, constant current source Ig=5.18A (turn-on), the current sources for turn-off are with several levels which are controlled by Vce.

## 5.2.1 IGBT Turn-on

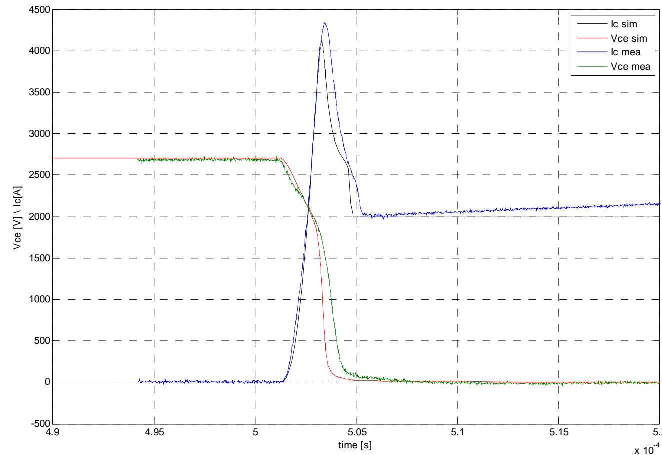


*Figure 5.2: IGBT Turn-on Comparison between Simulation and Measurements*

Figure 5.2 displays the IGBT turn-on Vce and Ic curves for both simulation and measurements. From the figure, the peak value of Ic in simulation is smaller than in the measurement. dIc/dt is almost the same for both cases. From calculation, we get that dIc/dt from simulation is 1867 A/µS. From measurements, it's 1905 A/µS.

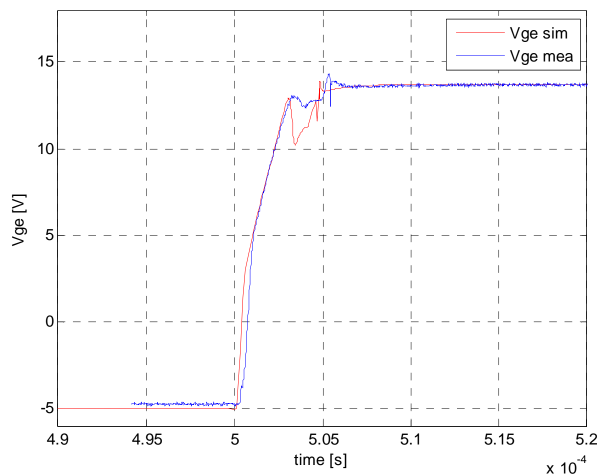


*Figure 5.3: Turn-on Gate Voltage Comparison between Simulation and Measurements*

Figure 5.3 shows the gate voltage during the IGBT turn-on. The simulation results agree with the measurement results quite well. The first voltage drop on Vge curves shows the difference between the simulation and measurements. It could be resulted by the gate-emitter inductance. In the real experiments, the thickness of the device will result the inductance which affects the measurements for the gate emitter voltage. The inductance is between the IGBT emitter of the chip inside the module and the external emitter contact on the outside of the module. So 600pH is used for that inductance during the simulations. But this value is not an accurate value.

From Figure 5.2 and Figure 5.3, we can conclude that the agreement between simulation and measurements should be quite sufficient for using the simulations for testing trends in behaviors when changing operation and gate driving parameters. But the exact absolute value of the turn-on losses Eon will not be completely correct.

As showed in Figure 5.4, it's different for the turn-on peak power between the measurement and simulation.

By integrating the power curves, we get the turn-on losses for both cases. The simulation turn-on loss is 7.05J. But the turn-on loss is 10.49J in the measurements. Though the agreement for the turn-on loss between simulation and measurements is not so sufficient, the simulation agrees with the measurements quite sufficiently for studying the relative impact of various operation conditions and gate driving parameters on the switching transient behaviors.

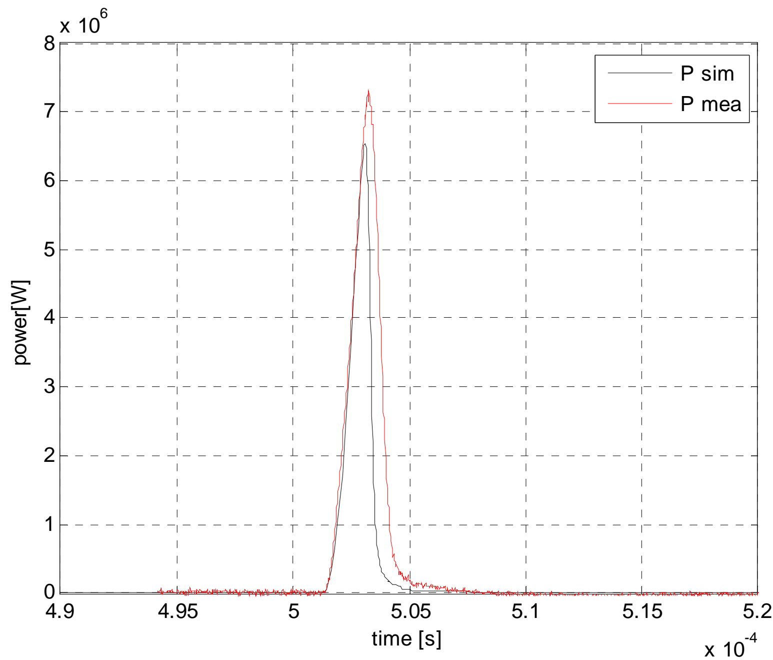


*Figure 5.4: Turn-on Power Comparison between Simulation and Measurements*

## 5.2.2 IGBT Turn-off

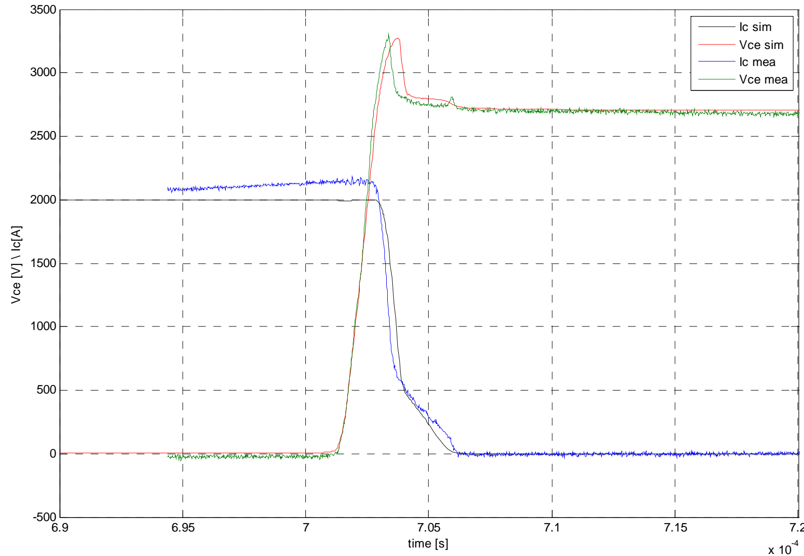


*Figure 5.5: IGBT Turn-off Comparison between Simulation and Measurements*

Figure 5.5 displays the IGBT turn-off Vce and Ic curves for simulation and measurements. Comparing those curves, we can see that the agreement between the simulation and measurements are quite good.

Figure 5.6 shows the gate voltage during IGBT turn-off. There's a large difference between the simulation and measurements. But the Vce, Ic curves agree quite well.

The reason could be due to a disturbance in the measurement of the gate voltage and also because of the approximations made in the numerical model when transforming the real 3D MOSFET of the IGBT structure to a 2D structure for the simulations, since this will affect the gate voltage behavior.

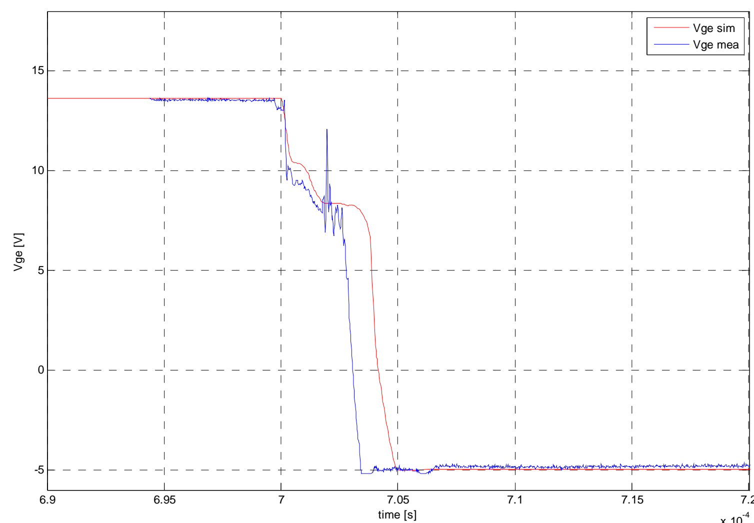


*Figure 5.6: Turn-off Gate Voltage Comparison between Simulation and Measurements*

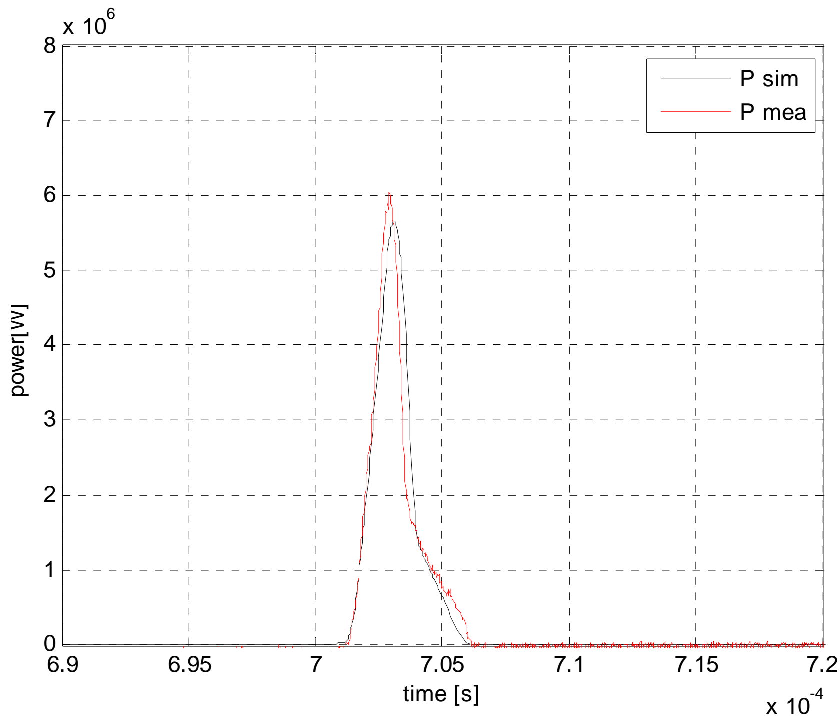


*Figure 5.7: Turn-off Power Comparison between Simulation and Measurements*

Looking at the power curves as displayed in Figure 5.7, we can see that the simulation results agree well with the measurement results. The turn-off loss in the simulation is 9.93J. And it is 9.25J in the measurements.

## 5.2.3 Diode Recovery

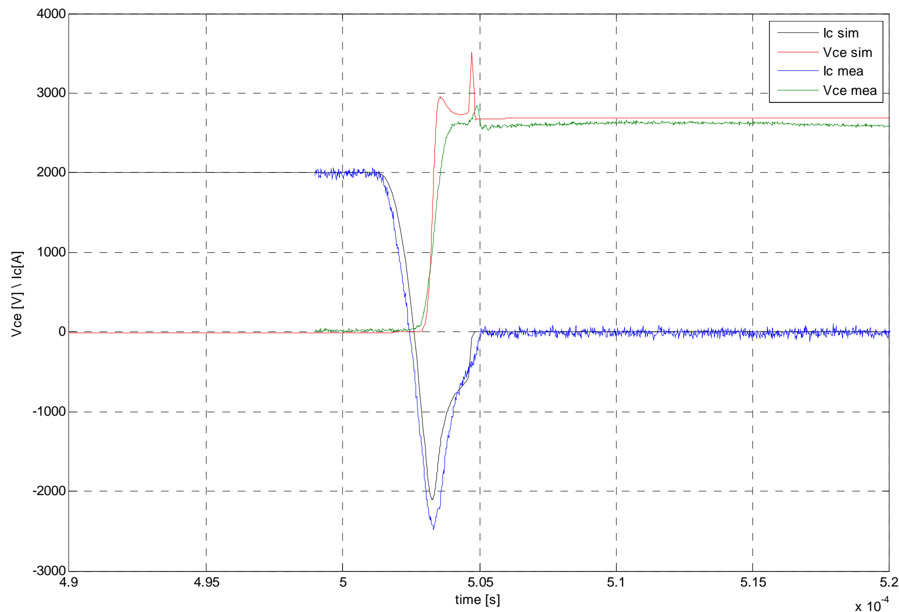


*Figure 5.8: Diode Recovery Comparison between Simulation and Measurements*

From Figure 5.8, it shows the diode recovery current and voltage curves. Similar to IGBT turn-on, the agreement between the diode current is good. But the voltage doesn't agree so well.

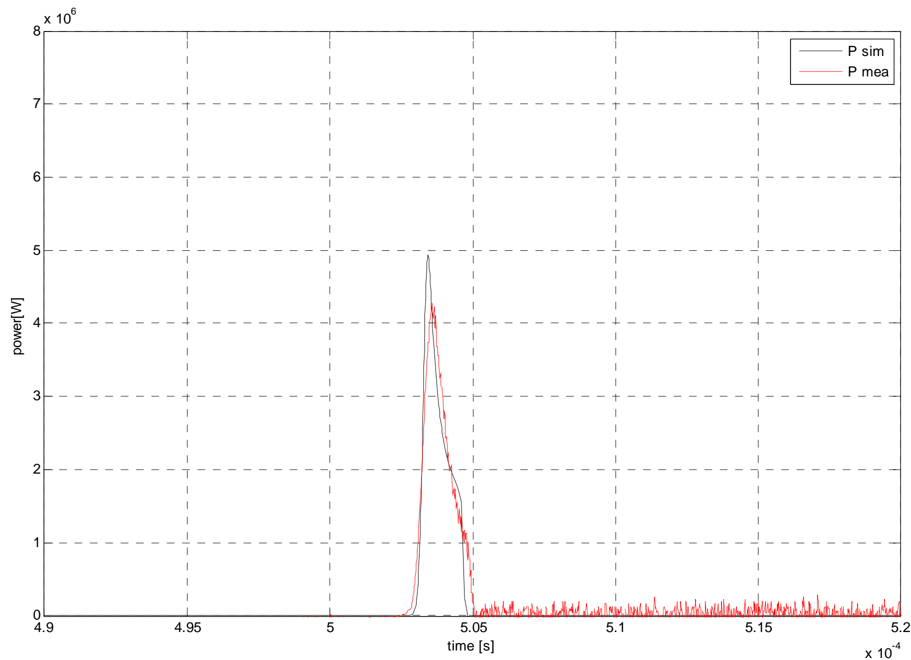


*Figure 5.9: Diode Recovery Power Comparison between Simulation and Measurements*

The power curves are as displayed in Figure 5.9. The simulation results do not match the measurements so well.

For the diode recovery losses, the simulation result is 4.32J. And it's 5.07J in the measurement.

## 5.3 Impact of Gate-emitter Inductance

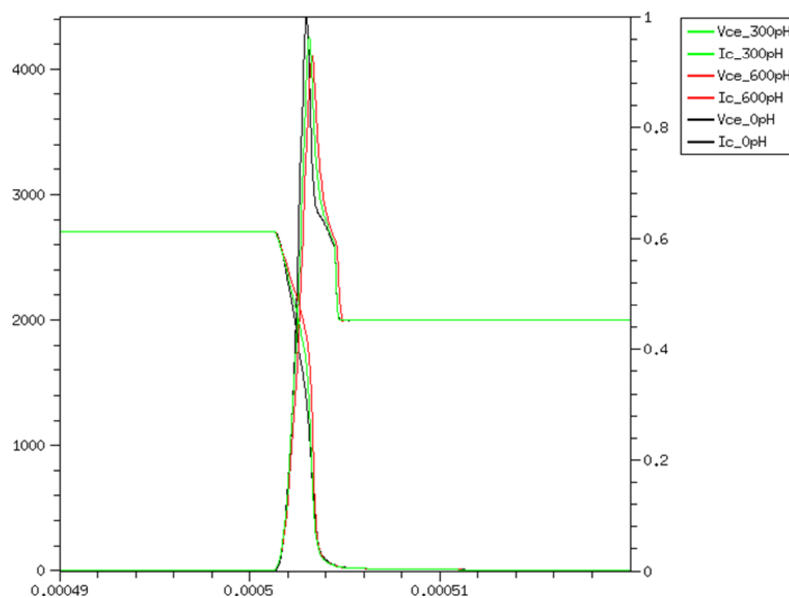


*Figure 5.10: IGBT Turn-on Behaviors with Different Gate-emitter Inductance*

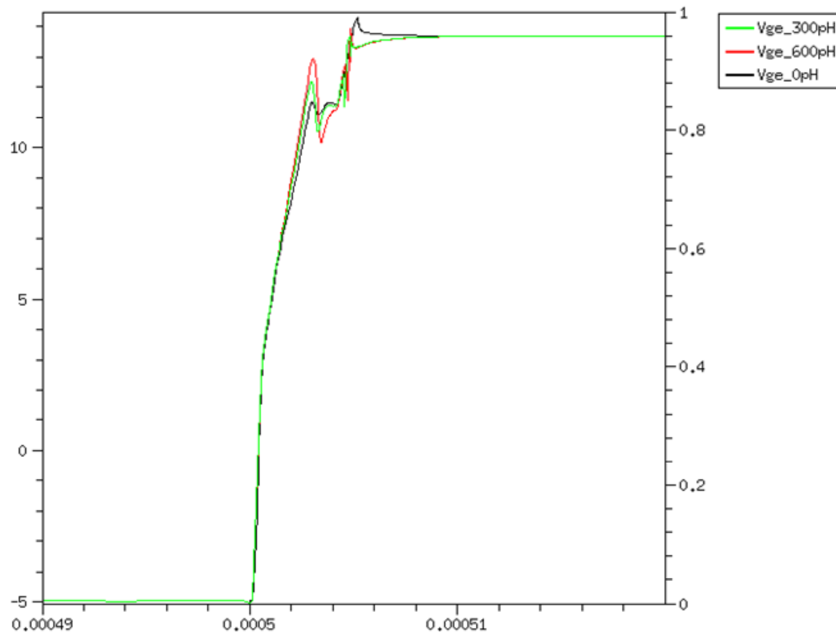


*Figure 5.11: Gate Voltage with Different Gate-emitter Inductance*

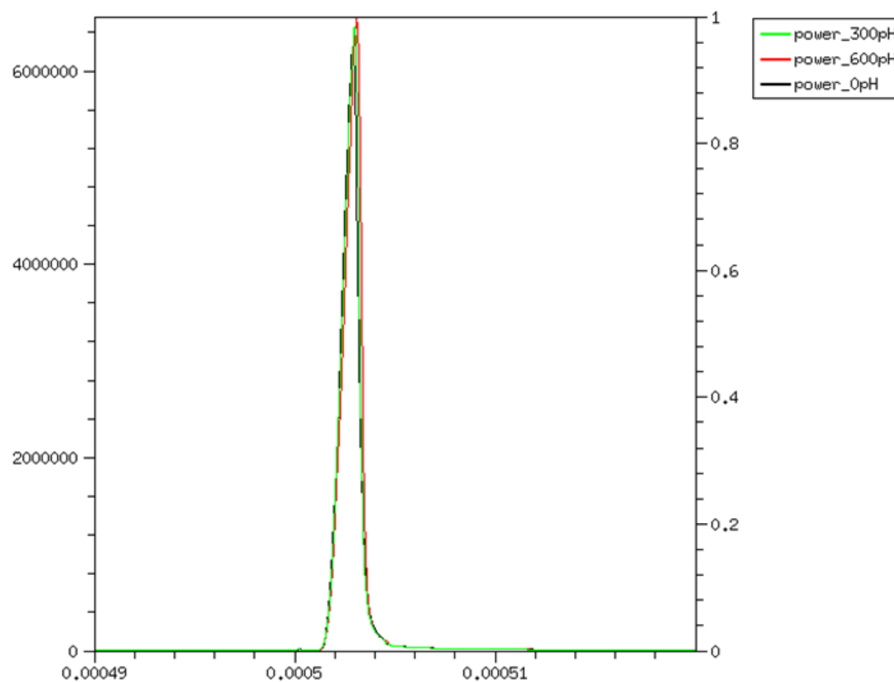


*Figure 5.12: IGBT Turn-on Power Curves with Different Gate-emitter Inductance*

In the previous section, it's mentioned that we estimate the gate-emitter inductance as 600pH in the simulation. But it's a rough estimation and it would be interesting to compare with different gate-emitter inductance estimations. The 0pH, 300pH and 600pH cases are compared in the simulation.

From Figure 5.10, we can see that the higher gate-emitter inductance reduces the peak value of Ic more and decreases the dIc/dt. Figure 5.11 reflects the gate-emitter inductance impact on the gate voltage curves. The first voltage drop on the gate voltage curves shows the impact of the gate-emitter inductance. The higher inductance results the bigger voltage drop. That is because the voltage drop is caused

by $L\frac{dIc}{dt}$. When Ic reaches the peak value, there's a big negative change on Ic. That causes $L\frac{dIc}{dt}$ is negative which represents the voltage drop on the gate voltage curves.

Figure 5.12 gives the power curves for all the cases. The peak power also increases with the increased gate-emitter inductance. By calculating the turn-on losses, we can see that the turn-on losses increase with the increased gate-emitter inductance. The turn-on losses are 6.7J, 6.84J, and 7.05J for 0pH, 300pH and 600pH, respectively.

# 5.4 Impact of Cge

To look at the impact of different Cge, see Figure 4.5, values on the switching transient behaviors, we set the simulation environment like this, Ls=200nH, Cgc=1.1nF, Vcc=2800V, Ia=2000A, T=400K, constant current source Ig=5.18A (turn-on). Then we vary the Cge value with 660nF and 990nF. The different simulation results will be presented. The impact on turn-on, turn-off and diode recovery behaviors will be analyzed in this section.

## 5.4.1 IGBT Turn-on

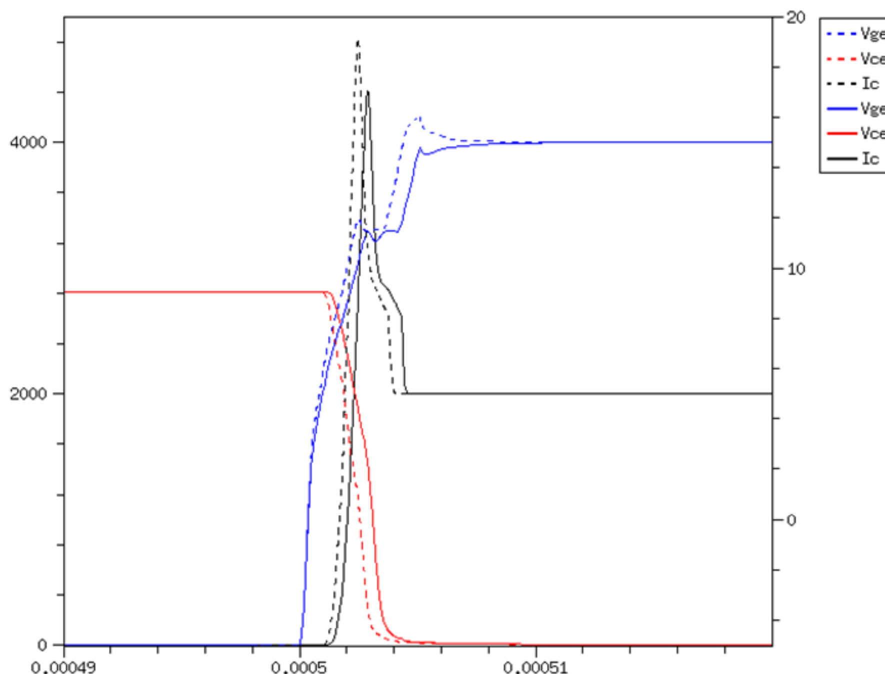


*Figure 5.13: IGBT Turn-on Curves with Different Cge*

Figure 5.13 shows the IGBT turn-on curves with different Cge values. The solid curves are the collector current Ic, collector emitter voltage Vce and gate voltage Vge under the simulation with Cge=990nF. The dashed curves are under the simulation with Cge=660nF. Both cases are with the same turn-on current source which is the constant current source 5.18A.

From Figure 5.13, it's obvious that with the lower value of Cge, the speed of turn-on is faster. The reason is because the current source charges slower to the higher Cge. That results a slower dVge/dt. As mentioned in Chapter 4, dVge/dt controls the turn-on dIc/dt.

The different values of Cge affect the speed of turn-on. That means Cge also will impact the turn-on losses. Figure 5.14 and Figure 5.15 display the power curve at turn-on (at the time position 500µS in Figure 5.1) and the energy curve. We can conclude that the turn-on loss will decrease with decreased Cge because of the increased turn-on speed dIc/dt.

In our simulation, the turn-on losses with Cge=990nF is 7.08J. And it will be reduced to 5.84J with Cge=660nF. Though the turn-on losses reduced with a considerable value, the maximum dIc/dt also increases with the decreased Cge. And that may give problems in series connection and also this turn-on dIc/dt results in the same turn-off dIc/dt for the diode turn-off in the phase leg that may also create problems for the diode.

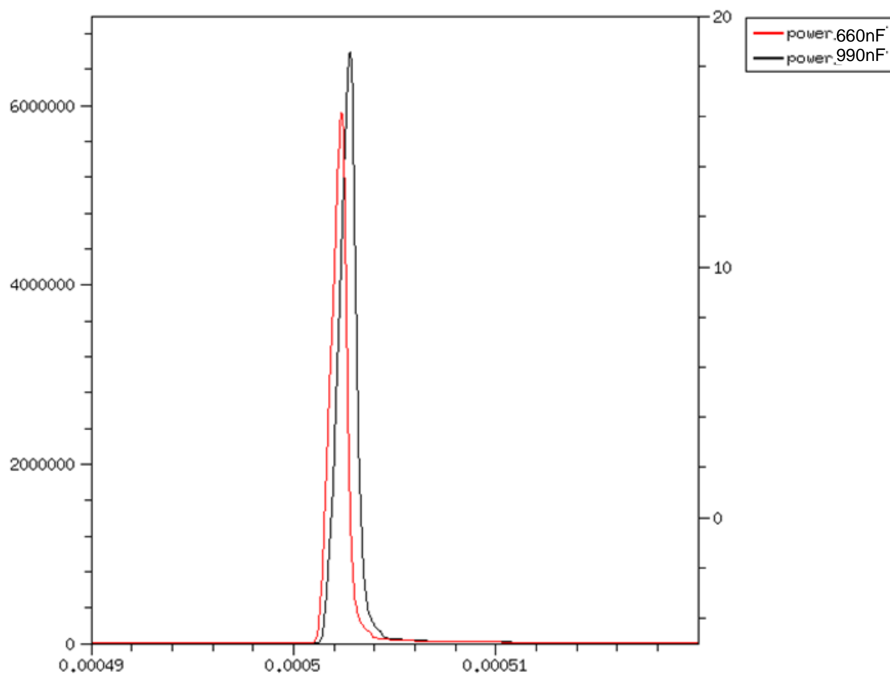


*Figure 5.14: IGBT Turn-on Power Curves with Different Cge*

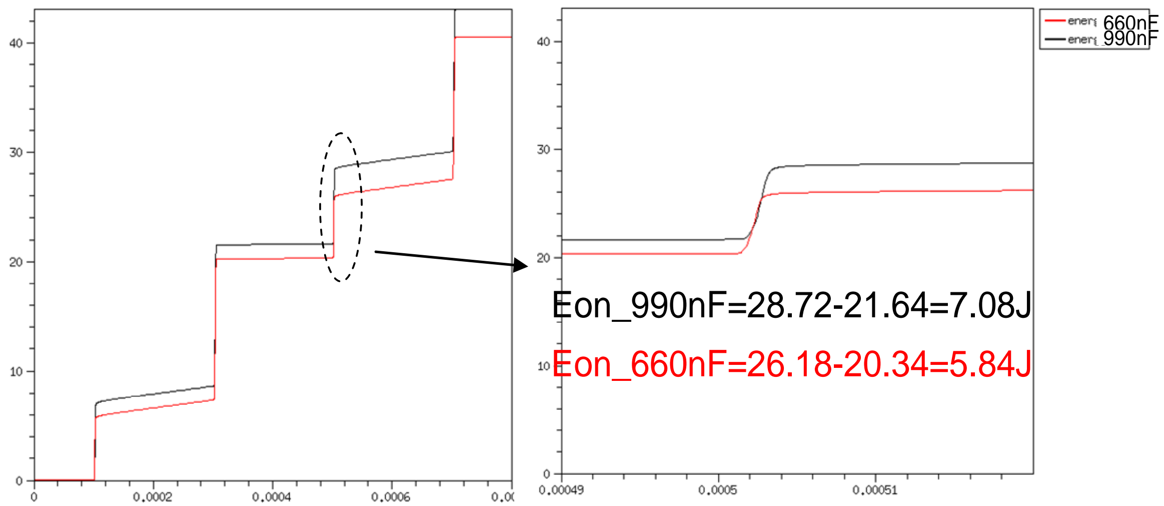

*Figure 5.15: IGBT Turn-on Energy Curves with Different Cge*

## 5.4.2 IGBT Turn-off

Cge controls only the turn-on switching speed on. But it has no impact at turn-off. From Figure 5.16, it proves that Cge has no impact at turn-off curves.

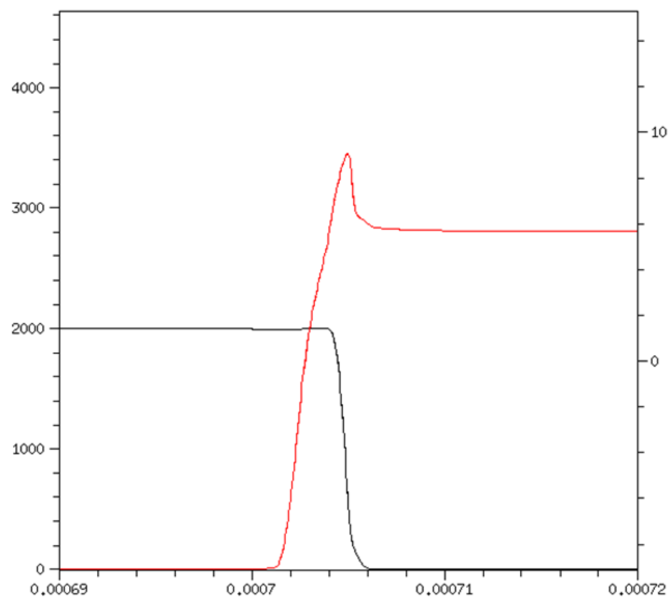

*Figure 5.16: Turn-off Curves with Different Cge*

## 5.4.3 Diode Recovery

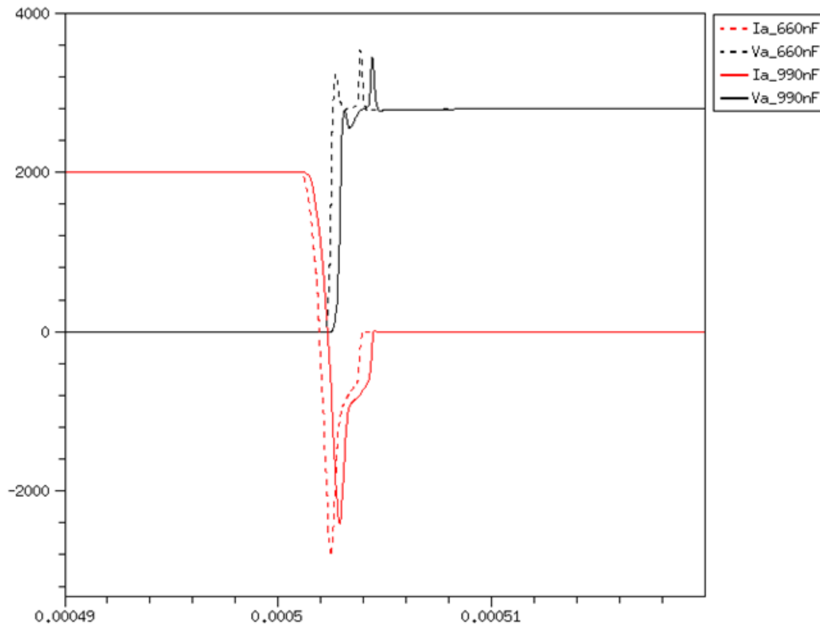


*Figure 5.17: Diode Recovery with Different Cge*

The diode recovery curves are displayed in Figure 5.17. Ia is the diode current. Va is the voltage over the diode. The turn-on of IGBT2 in Figure 4.1 gives a turn-off of the diode in the IGBT1 module (which is only represented by a diode in the simulation).

Though the decreased value of Cge gives a faster IGBT turn-on speed and lower IGBT turn-on losses, it also impacts the diode recovery power and losses. Figure 5.18and Figure 5.19 demonstrates the diode recovery power and energy curves with different Cge values.

From those figures, the decreased Cge value gives higher peak power in the diode, as well as the higher diode recovery losses.

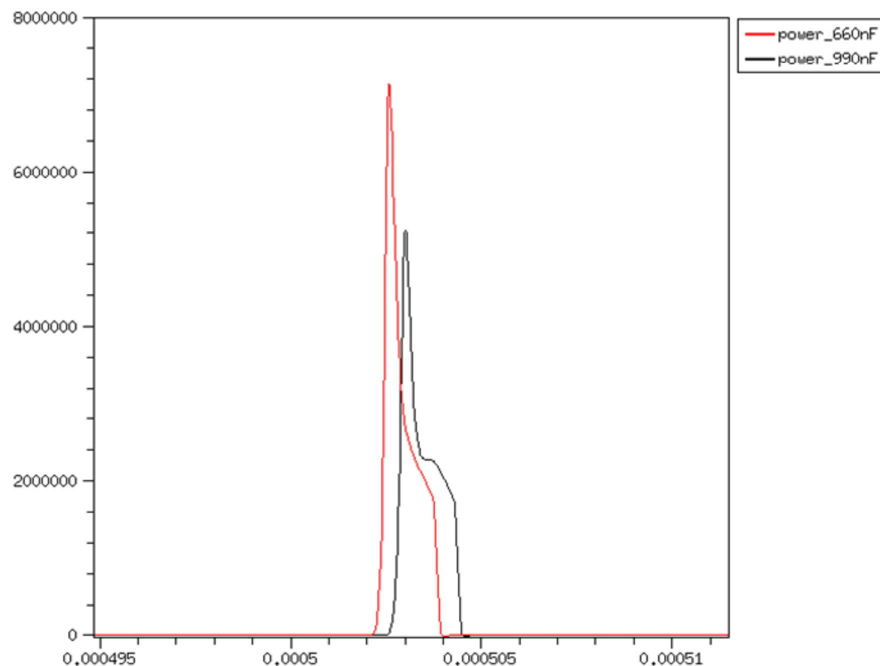


*Figure 5.18: Diode Recovery Power Curves with Different Cge*

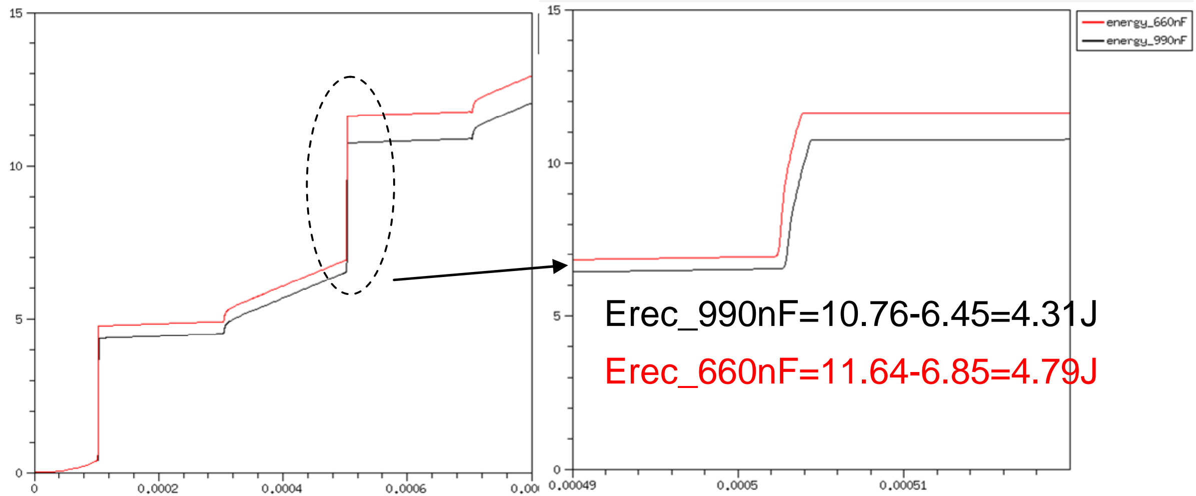


*Figure 5.19: Diode Recovery Energy Curves with Different Cge*

## 5.5 Impact of Cgc

Cgc is a feedback from collector to gate, as showed in Figure 4.4. It controls the dVce/dt during switching. So theoretically, the value Cgc affects both the turn-off and turn-on switching.

In order to analyze the impact of Cgc on the turn-off and turn-on curves, the simulation settings are set as: Ls=200nH, Cge=990nF, Vcc=2800V, Ia=2000A, T=400K, constant current source Ig=5.18A (turn-on). Two cases are simulated which are Cgc=1.1nF, Cgc=3.3nF.

### 5.5.1 IGBT Turn-on

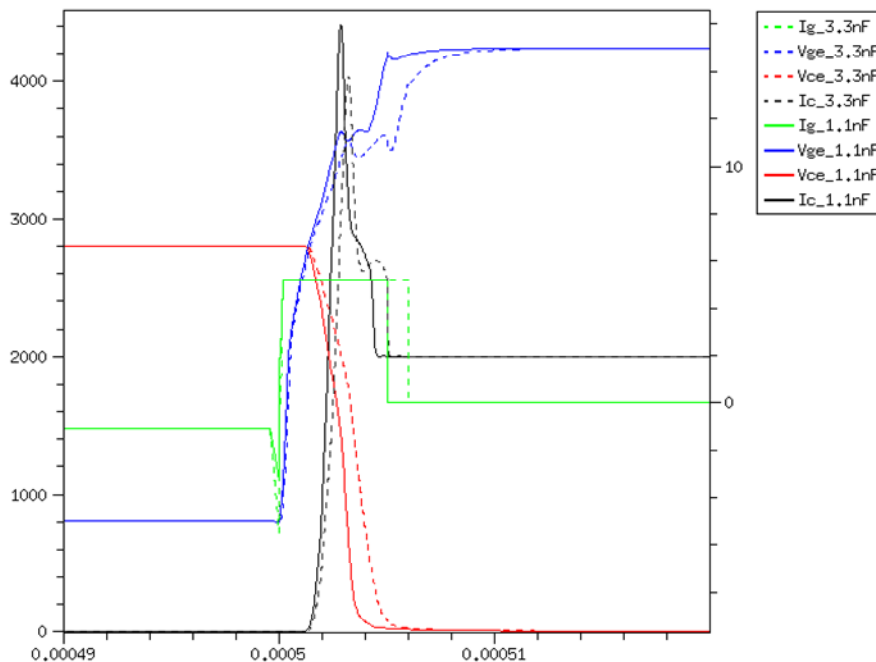


*Figure 5.20: IGBT Turn-on Behaviors with Different Cgc Values*

Figure 5.20 shows the IGBT turn-on Vce and Ic curves with the Vge curve. From the Vge curve (blue curves), we can see the impact of Cgc on dVge/dt. dVge/dt affects dIc/dt. Thus, Cgc affects the IGBT turn-on switching speed and losses.

Figure 5.21 and Figure 5.22 give the power and energy curve with different Cgc values.

We can see that the higher value of Cgc increases the IGBT turn-on peak power and losses. That is because it takes longer time to charge the higher Cgc which results the lower dVge/dt and dIc/dt.

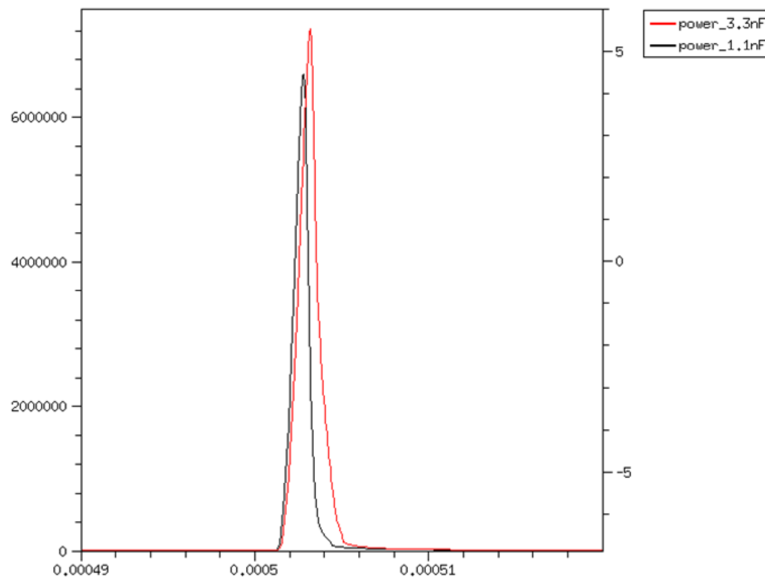


*Figure 5.21: IGBT Turn-on Power Curves with Different Cgc Values*

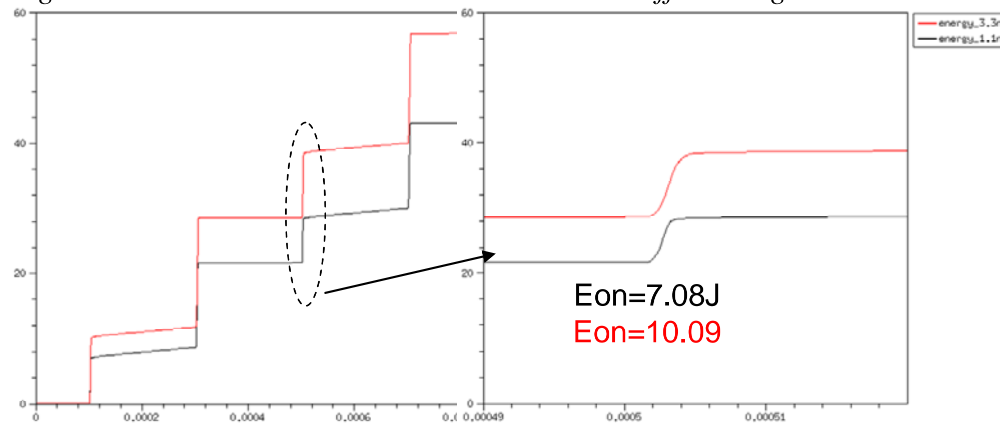


*Figure 5.22: IGBT Turn-on Energy Curves with Different Cgc Values*

## 5.5.2 IGBT Turn-off

Because Cgc affects dVge/dt, Cgc also has impact on the turn-off behaviors which is its main purpose. Figure 5.23 display the IGBT turn-off curves. Similar to the turn-on curves, the turn-off switching time is longer with the higher Cgc due to the lower dVge/dt.

The power and energy curves are displayed in Figure 5.24 and Figure 5.25. The peak power in these two cases is almost the same. But the turn-off losses is higher with the higher Cgc. The reason is the same for the turn-on. Because higher Cgc slows down dVge/dt, it increases the switching time and losses.

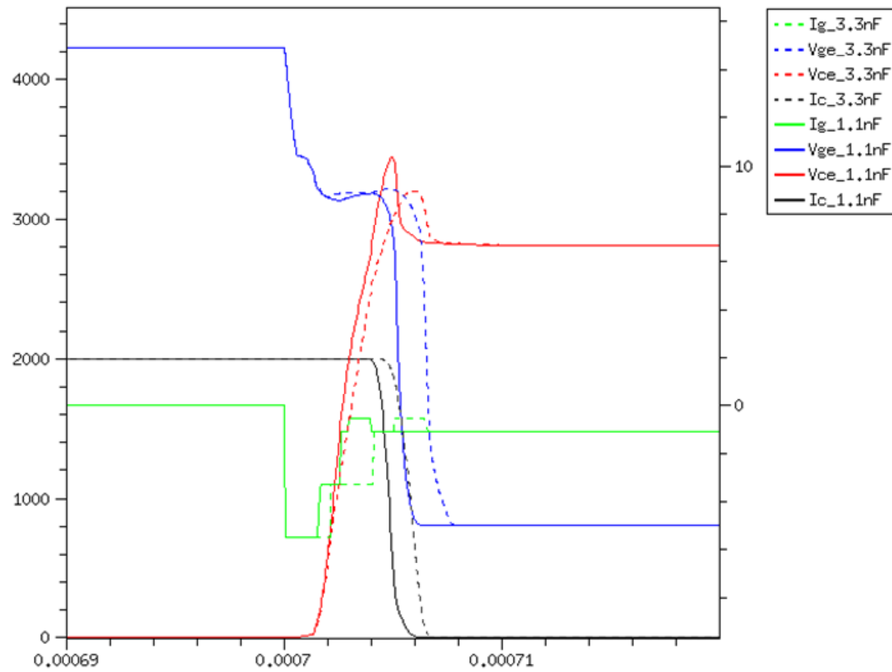

*Figure 5.23: IGBT Turn-off Curves with Different Cgc Values*

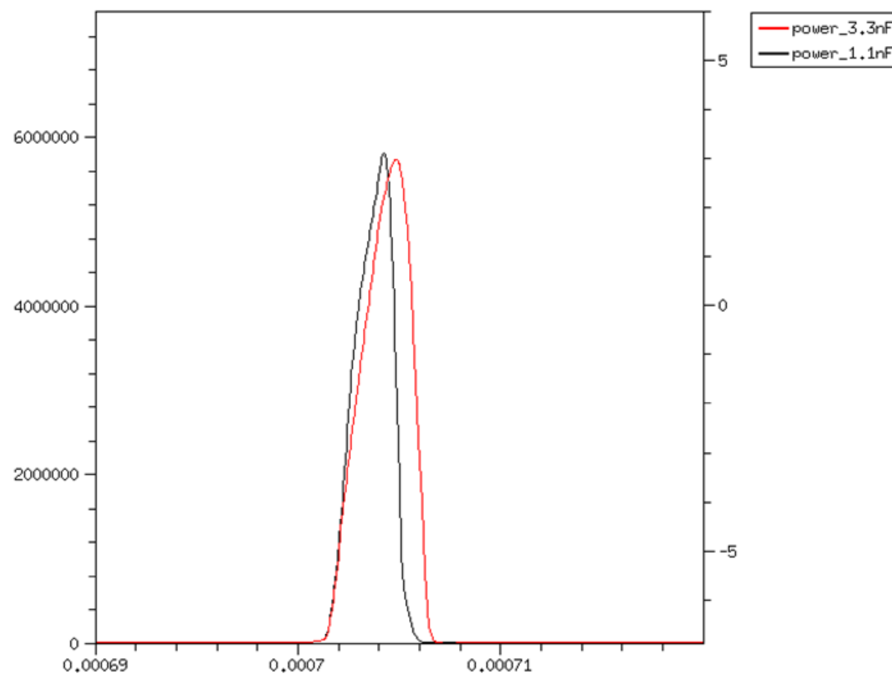

*Figure 5.24: IGBT Turn-off Power Curves with Different Cgc Values*

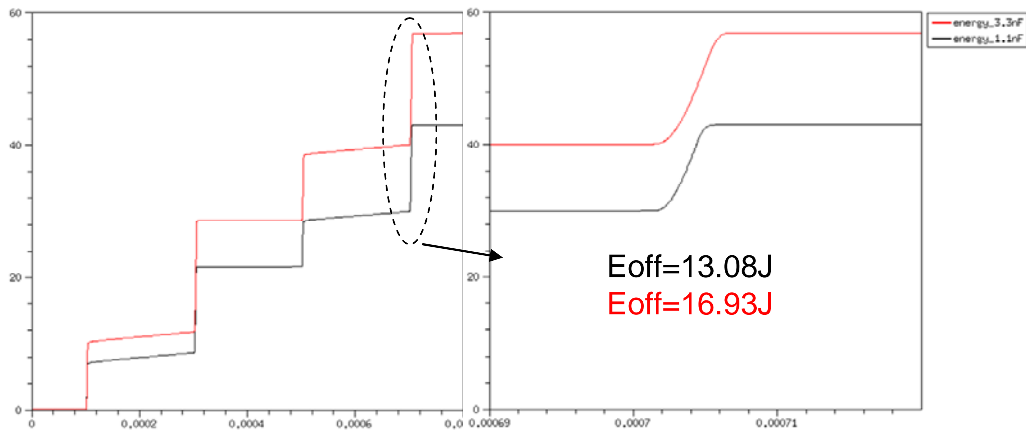


*Figure 5.25: IGBT Turn-off Energy Curves with Different Cgc Values*

### 5.5.3 Diode Recovery

Figure 5.26 shows the diode recovery behaviors with Cgc=1.1nF and 3.3nF. The deviation of diode recovery current dIa/dt also is affected by the value of Cgc. Thus, the power and losses also are affected.

Figure 5.27 and Figure 5.28 display the power and energy curves. The higher Cgc which increases the IGBT turn-on losses decreases the peak power of diode recovery. The diode recovery losses also decrease with the increased Cgc value.

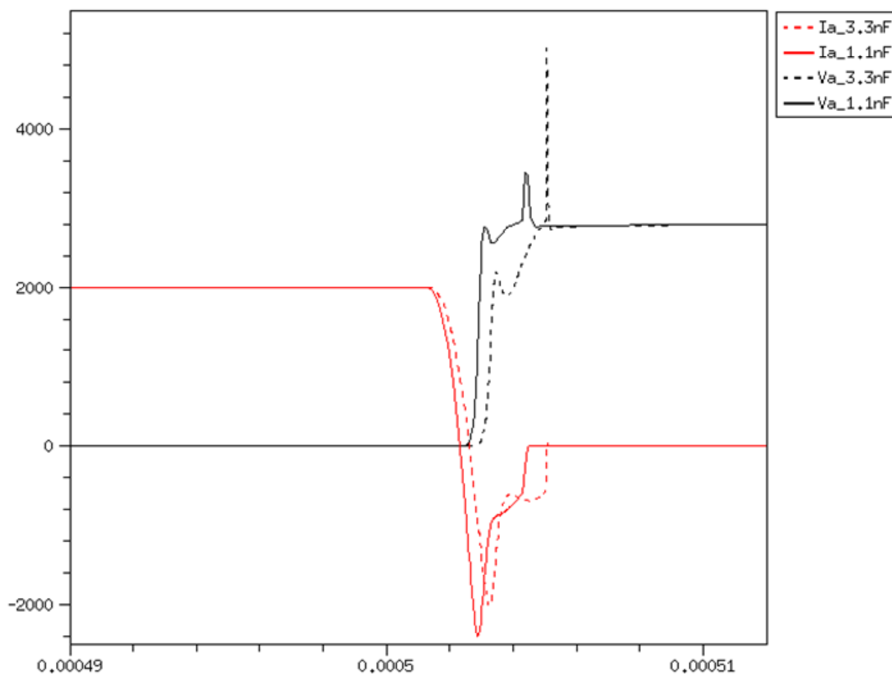


*Figure 5.26: Diode Recovery Curves with Different Cgc Values*

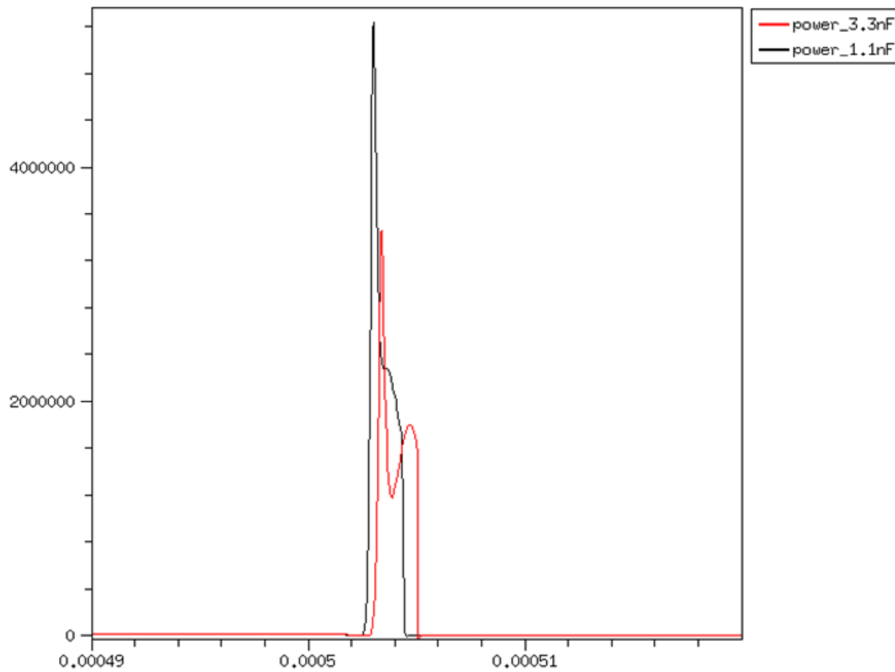


*Figure 5.27: Diode Recovery Power Curves with Different Cgc Values*

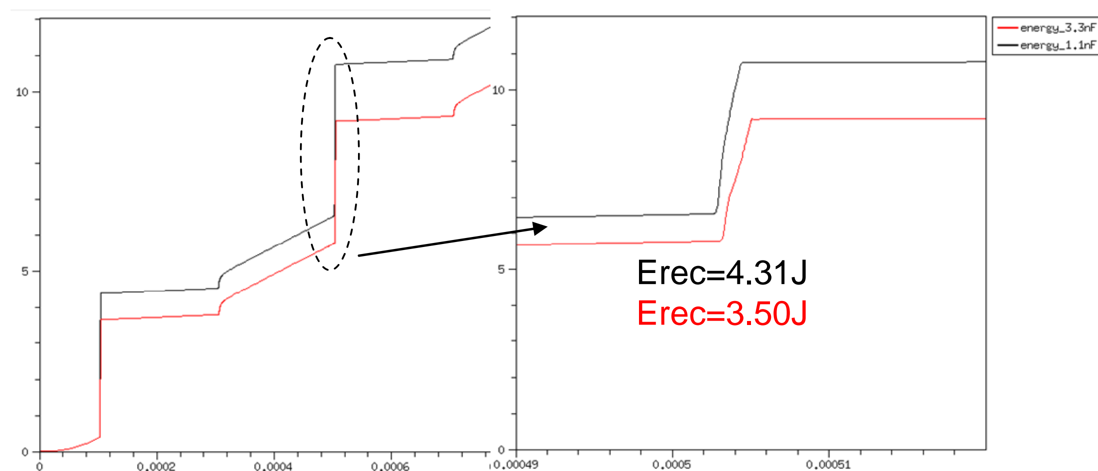


*Figure 5.28: Diode Recovery Energy Curves with Different Cgc Values*

# 5.6 Impact of Gate Threshold Voltage Vge(th)

As mentioned before, Vge(th) has the impact on the IGBT turn-on behaviors. If the Vge(th) is set too low, it may increase the turn-on losses. But if it's too high, it could cause the device failure during the short-circuit testing. It's a trade-off to find out the optimum value of Vge(th).

The simulation environment to examine the impact of Vge(th) is set as below: Ls=200nH, Cgc=1.1nF, Cge=990nF, Vcc=2800V, Ia=2000A, T=400K, the turn-on current sources settings are with several levels which are controlled by Vce.

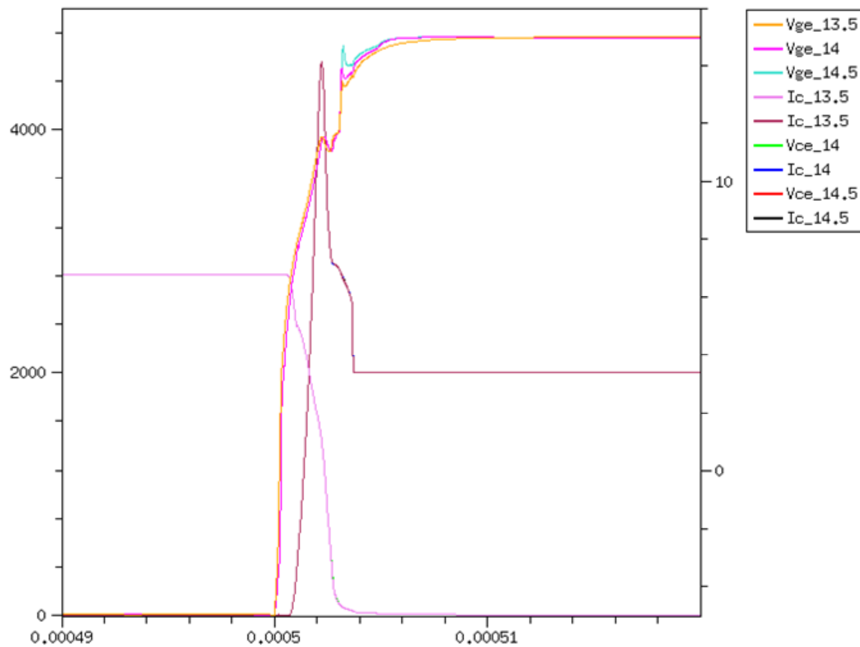


*Figure 5.29: Impact of Vge(th) on IGBT Turn-on*

Figure 5.29 displays the IGBT turn-on behaviors with various Vge(th) settings. From the figure, it's hard to see the difference among the Vce and Ic curves with different Vge(th) values. But for the gate voltage curves, it's obvious that they are different for each value. It could be that the simulation setting for Ic=2000A is too low.

# 5. 7 Different Current Source Settings for IGBT turn-on and Diode Recovery

As we've known already, Cge and the current source feeding to the IGBT gate can control the speed of IGBT turn-on switching. The impact of Cge has been discussed in the previous section.

In this section, we set the simulation conditions as this: Ls=200nH, Cgc=1.1nF, Cge=990nF, Vcc=2800V, Ia=2000A, T=400K. Then we apply different combinations of the current sources to analyze the impact of the current sources on the switching behaviors.

## 5.7.1 Constant and Standard Current Sources Settings

First of all, the standard settings for the current sources are with several levels which are controlled by Vce.

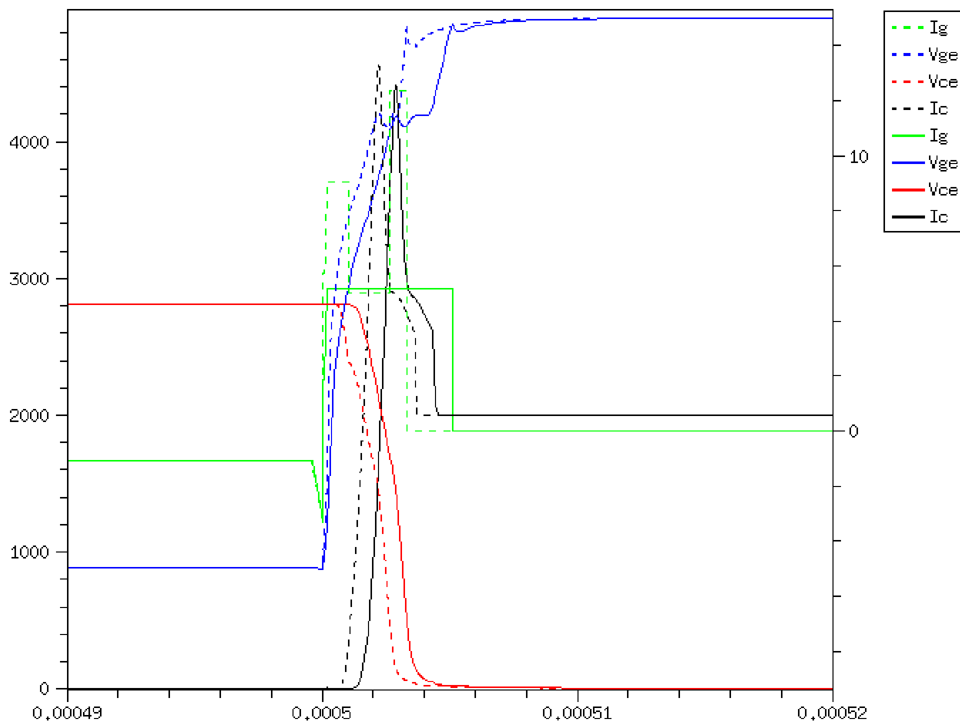


*Figure 5.30: Comparison with Constant and Standard Current Sources Settings*

Figure 5.30 give the Ic, Vce and Ig, Vge curves with different current sources settings. The solid curves are with the constant current source 5.18A. The dashed curves are with the standard settings for the current sources.

Figure 5.31 and Figure 5.32 give the power and energy curves of IGBT turn-on. From the figures, we can see that the turn-on losses are almost the same with these two different settings.

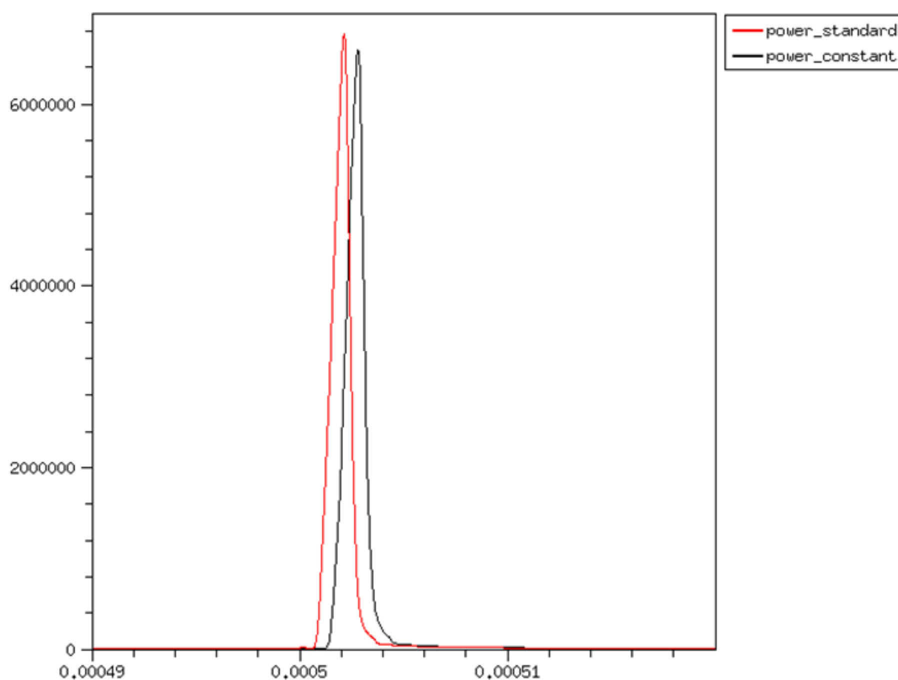


*Figure 5.31: IGBT Turn-on Power Curves with Constant and Standard Current Sources Settings*

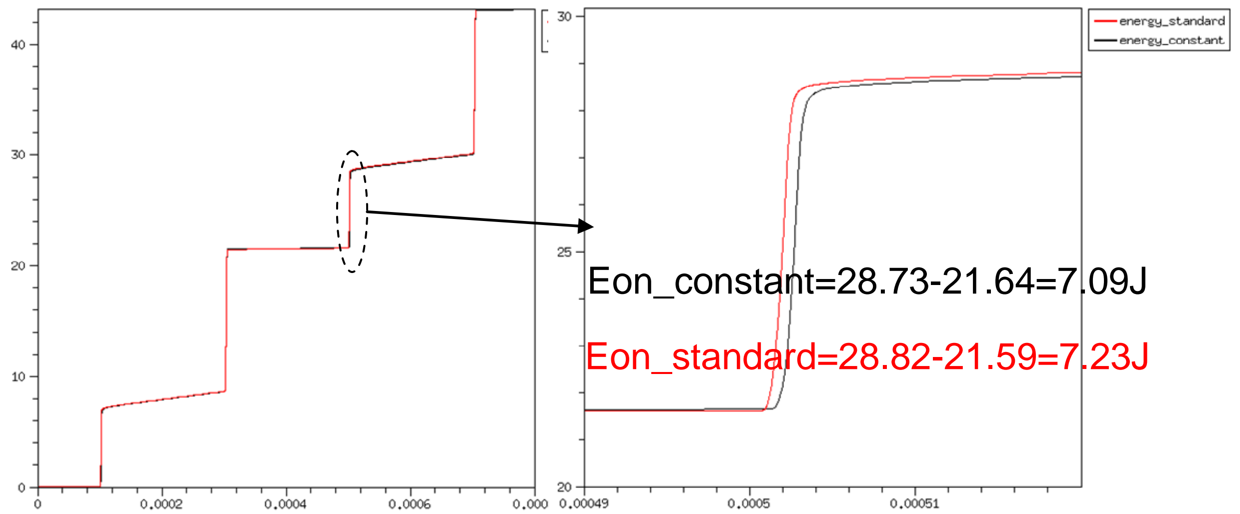


*Figure 5.32: IGBT Turn-on Energy Curves with Constant and Standard Current Sources Settings*

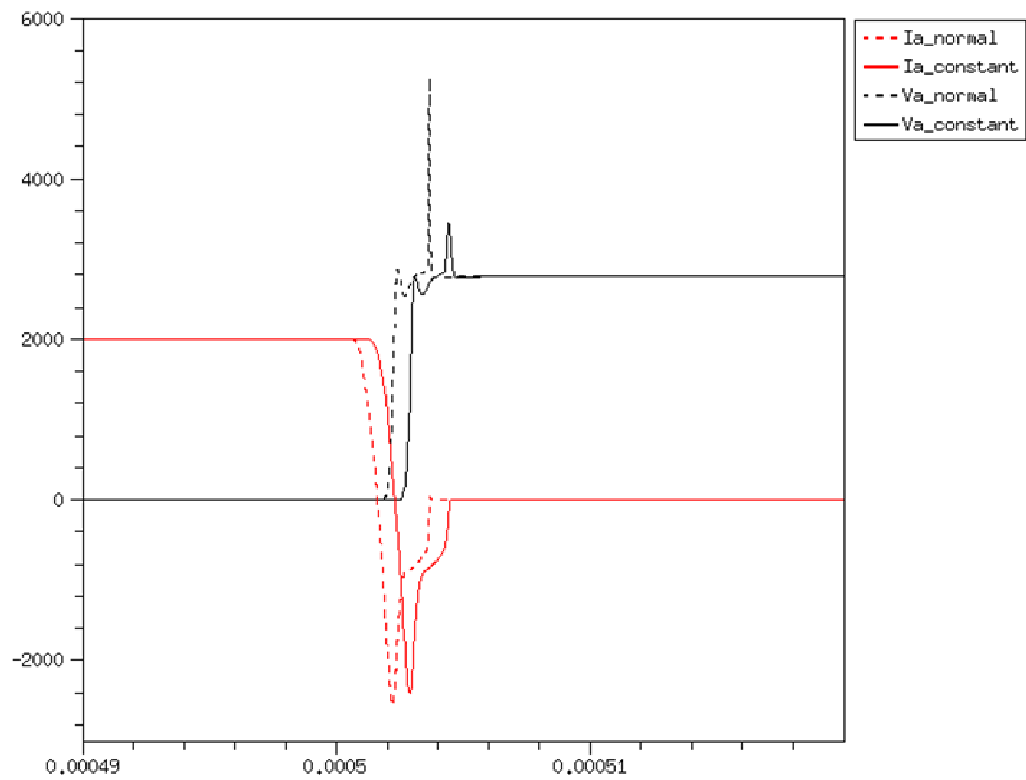


*Figure 5.33: Diode Recovery with Constant and Standard Current Sources Settings*

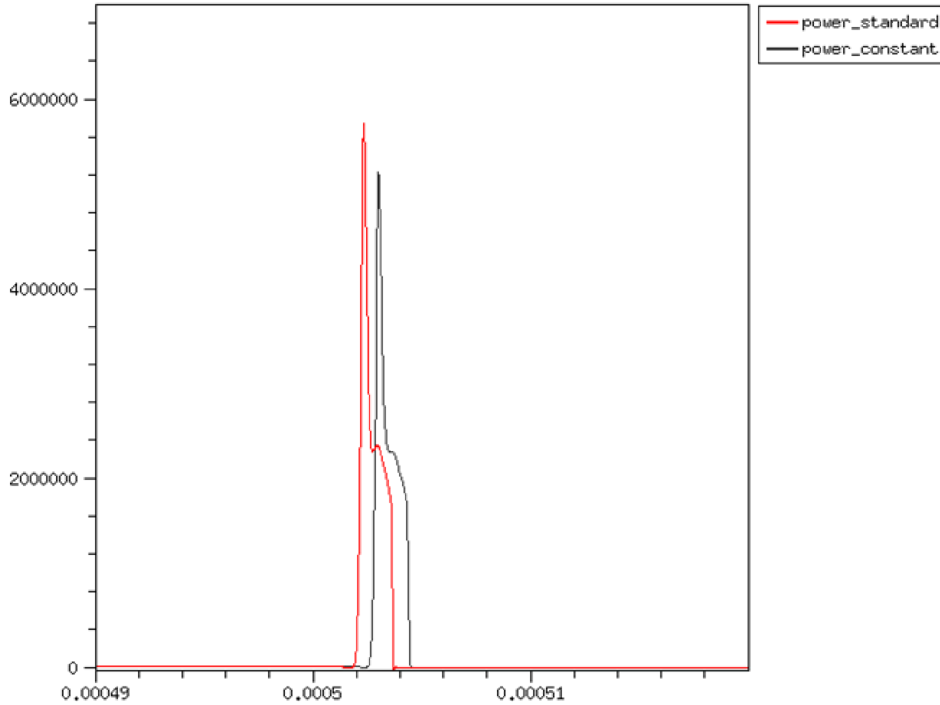


*Figure 5.34: Diode Recovery Power Curves with Constant and Standard Current Sources Settings*

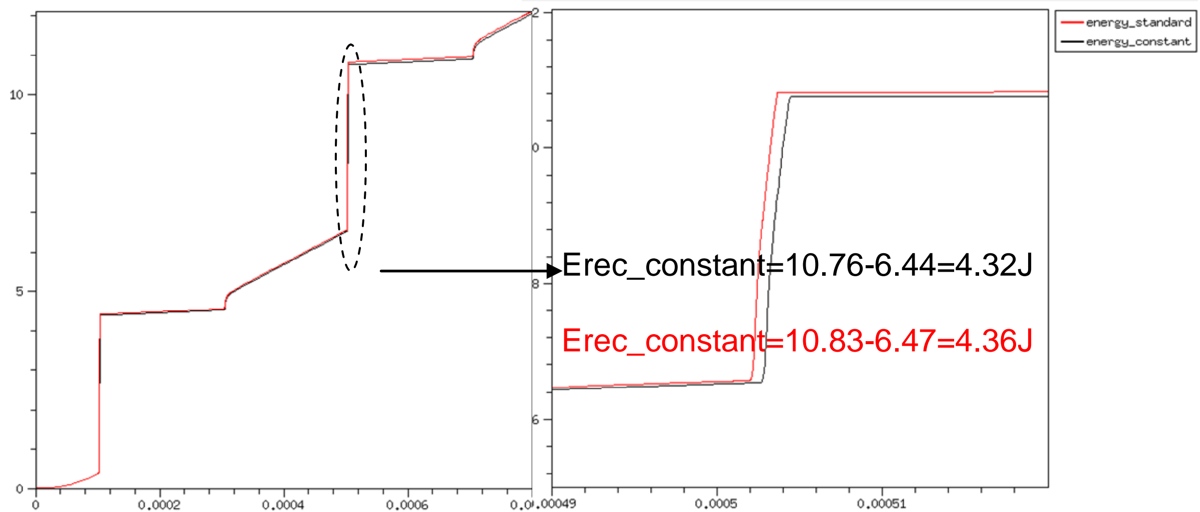


*Figure 5.35: Diode Recovery Energy Curves with Constant and Standard Current Sources Settings*

Figure 5.33 display the diode recovery curves Ia, Va. From the figure, we can see that the spike on the voltage curve Va in the standard settings is much higher than the one with the constant current source. But for the power and energy curves which are displayed in Figure 5.34 and Figure 5.35, they are almost the same with these two different settings.

## 5.7.2 Different Scales of Standard Current Sources Settings

In the previous section, the constant and standard current sources settings are compared. Here we will examine the effect of various scaling of the gate current

sources relative the standard values mentioned above. Simulations were done by scaling the amplitude of the current sources by the factor 0.5, 1, 1.5 and 2 times the standard setting respectively. Thus, the impact on different amplitudes of the current sources will be analyzed.

Ic and Vce across the IGBT are displayed in Figure 5.36. We can see that the peak value of Ic increases with the increased amplitude of current sources. The IGBT turn-on speed also increases with the increased amplitude of current sources.

From Figure 5.37, it shows the impact of the current sources on the gate voltage. The higher value of current feeding to the gate results the higher dVce/dt. By controlling the dVce/dt, it controls the turn-on speed of the device.

The power and energy curves for IGBT turn-on are given in Figure 5.38 and Figure 5.39. Lower amplitude of current sources gives higher IGBT turn-on peak power and losses.

We can conclude that the more current feeding into the gate will give the less IGBT turn-on losses. But the gate current also impacts on the diode recovery behaviors.
Figure 5.40 displays the diode recovery current and voltage. It gives the information that the peak diode recovery current increases with the increased amplitude of the current sources.

Figure 5.41 and Figure 5.42 show the power and energy curves for the diode recovery. The peak power is much higher for the higher amplitude of current sources than it with the lower amplitude of current sources. The diode recovery losses increased with the increased current sources.

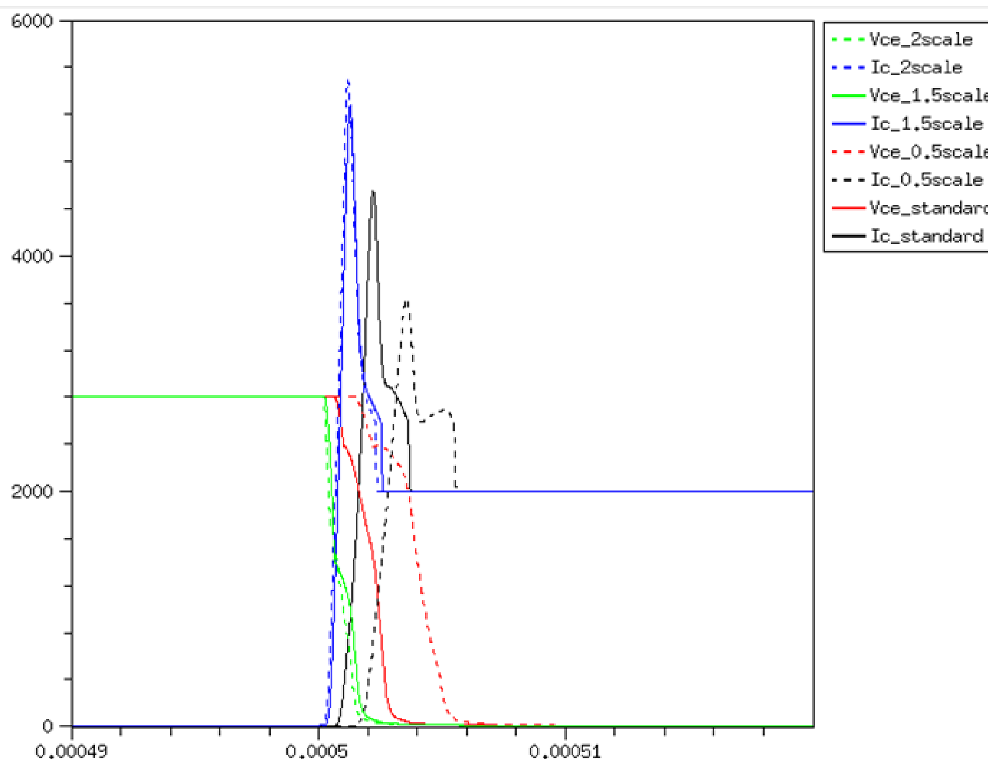


*Figure 5.36: Vce and Ic Profiles with Different Scaled Current Sources Settings*

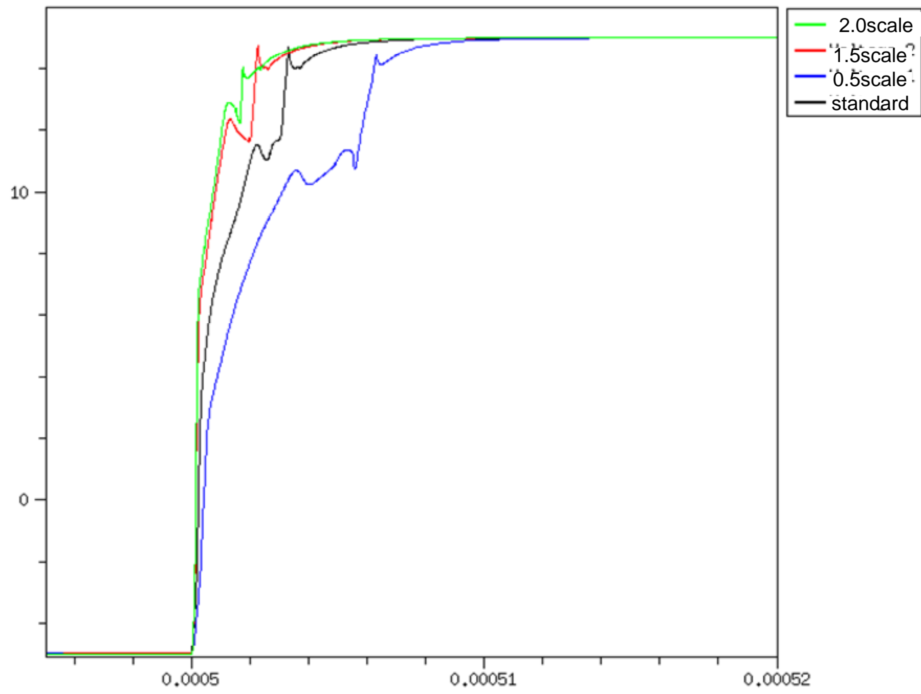

*Figure 5.37: Vge with Different Scaled Current Sources Settings*

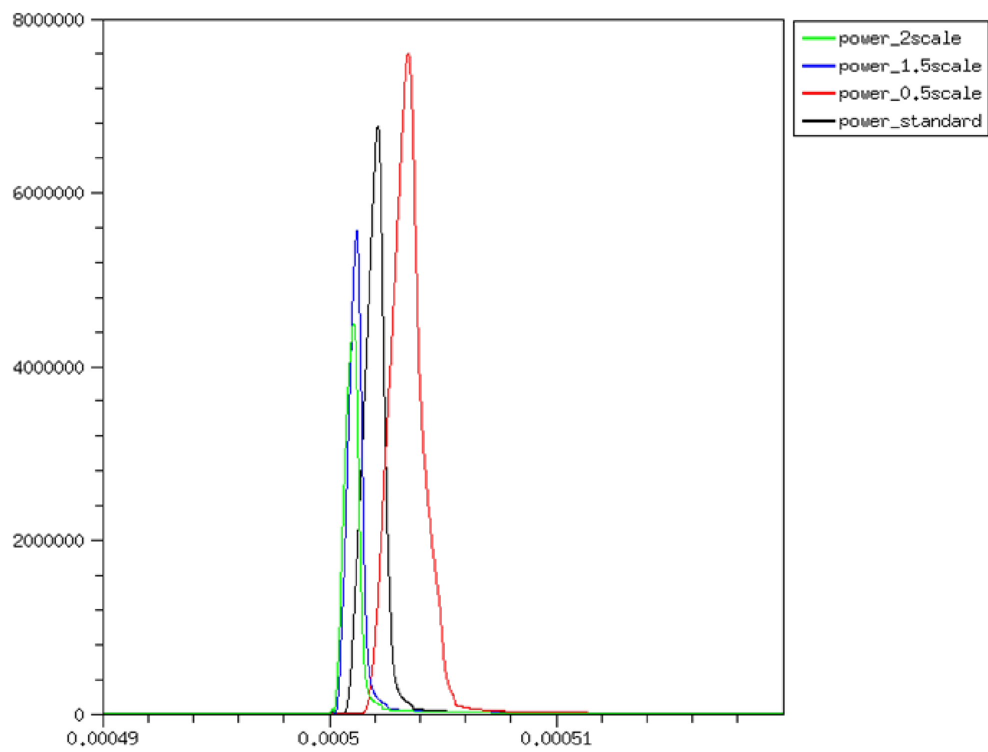

*Figure 5.38: Turn-on Power Curves for Different Scaled Current Sources*

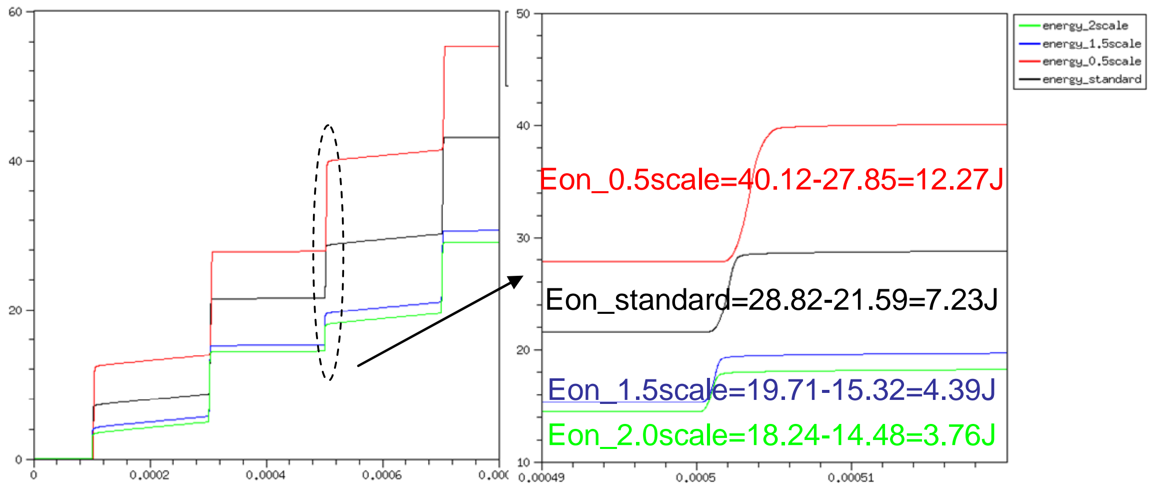


*Figure 5.39: Energy Curves for Different Scaled Current Sources*

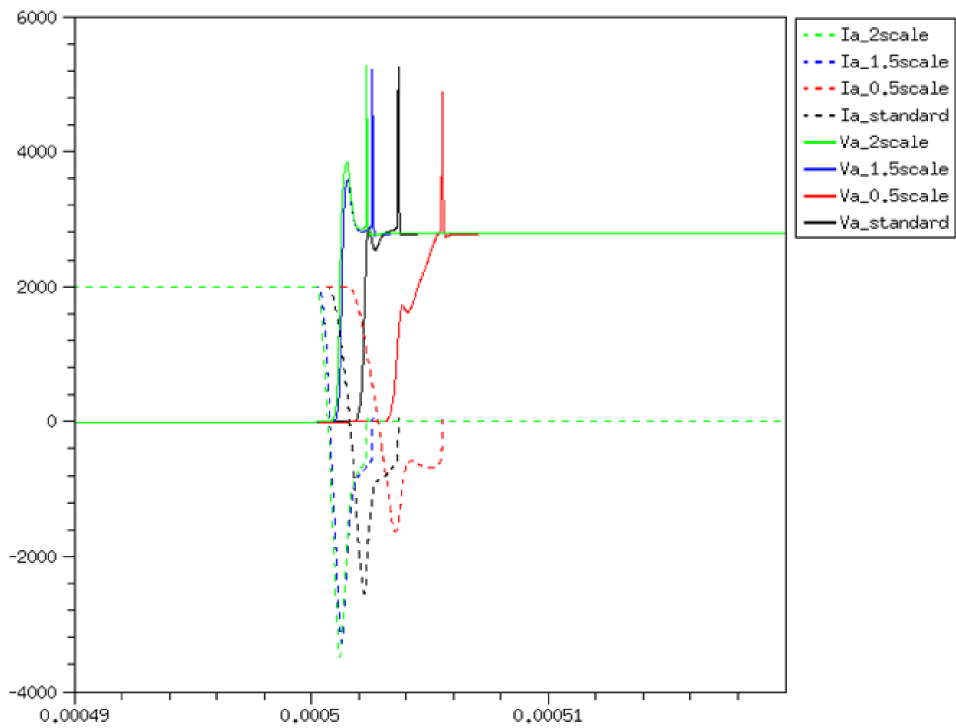


*Figure 5.40: Diode Recovery Behaviors with Different Scaled Current Sources*

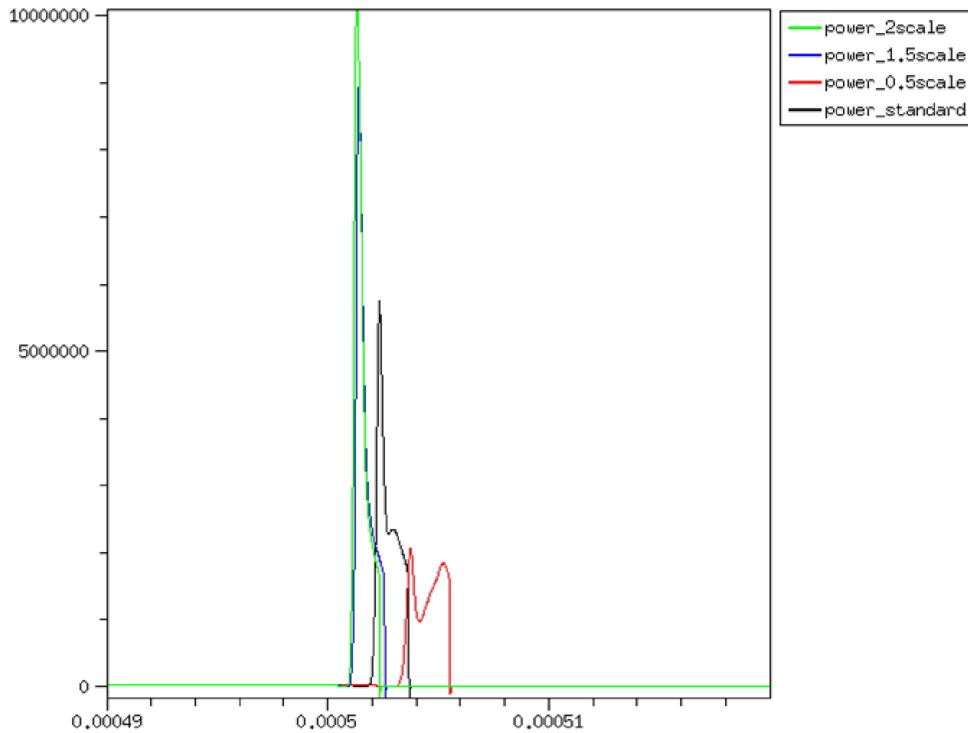


*Figure 5.41: Diode Recovery Power Curves with Different Scaled Current Sources*

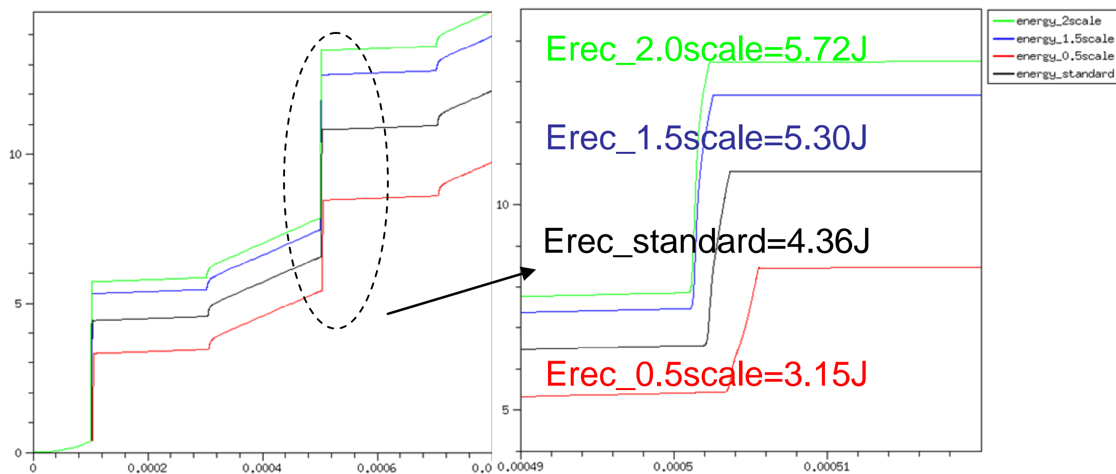


*Figure 5.42: Diode Recovery Energy Curves with Different Scaled Current Sources*

## 5.8 Different Current Source Settings for IGBT turn-off

The simulation conditions are set as: Ls=200nH, Cgc=1.1nF, Cge=990nF, Vcc=2800V, Ia=2000A, T=400K.

The standard turn-off current source is with several levels which are controlled by Vce. The current sources scaled with 0.5, 1.5, 2.0 are applied in the simulation in order to study the current sources settings' impact on IGBT turn-off.

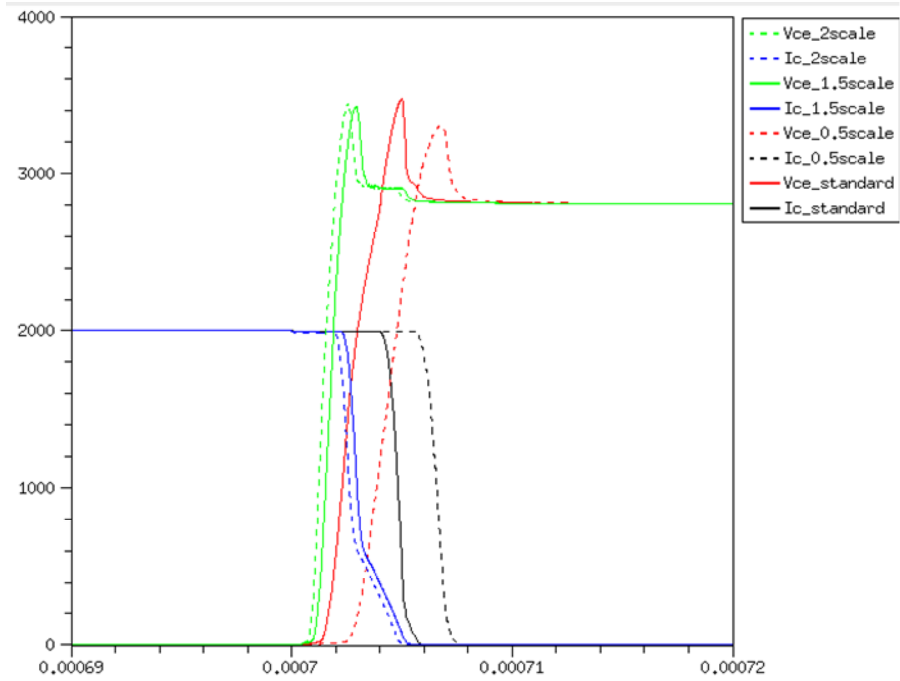


*Figure 5.43: IGBT Turn-off with Different Scaled Current Sources*

Figure 5.43 shows the IGBT turn-off curves with different scaled current sources. From the figure, the higher amplitude the current sources increased the turn-off speed.

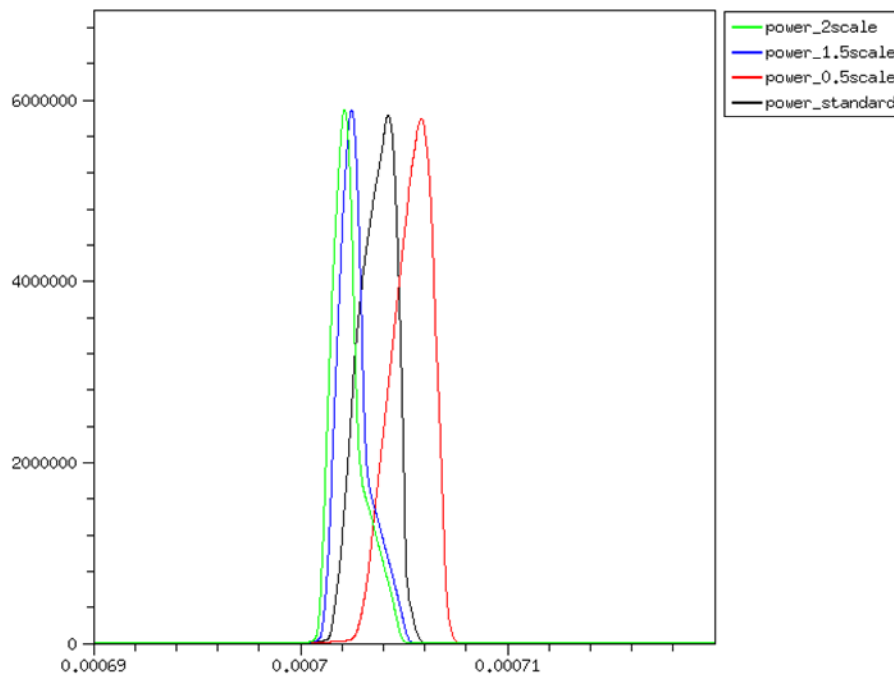


*Figure 5.44: IGBT Turn-off Power Curves with Different Scaled Current Sources*

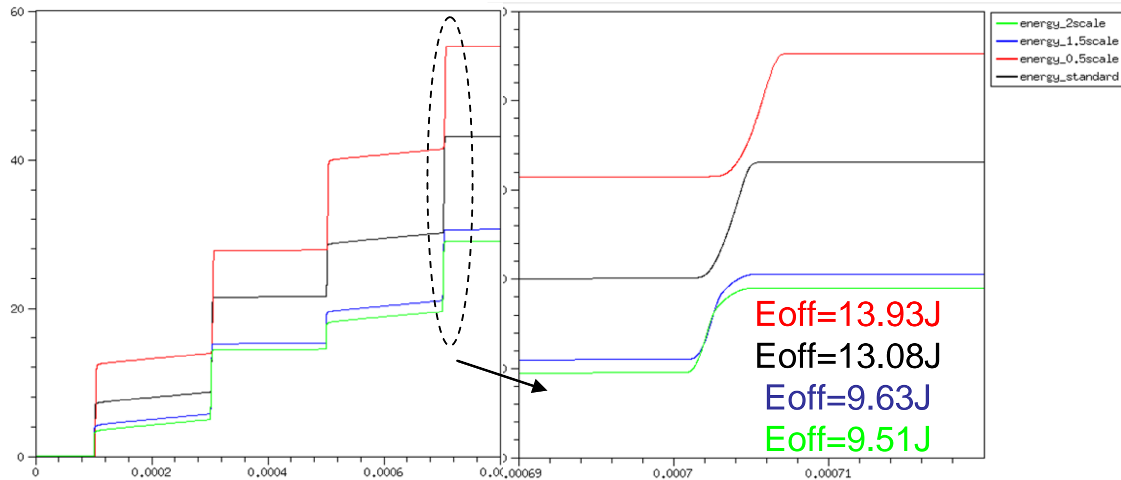

*Figure 5.45: IGBT Turn-off Energy Curves with Different Scaled Current Sources*

Figure 5.44 and Figure 5.45 show the IGBT turn-off power and energy curves with different current settings. The IGBT turn-off peak power is almost the same for different cases. But the energy has a distinct increase from scale 0.5 and 1 (which are almost the same between scale 0.5 and 1) to scale 1.5 to 2 (which are almost the same between scale 1.5 and 2).

# 5.9 Conclusion

In this chapter, the simulation results are presented. First of all, the simulation results are compared with the experimental results with the same settings. From the comparison, we conclude that the IGBT turn-off switching behaviors and losses between the simulation and measurement match fairly well. For the IGBT turn-on losses, the simulation results differ more as compared with the measurement results. But the agreement between the simulation and measurement is sufficient for the studying on the relative impact of various operating conditions on the transient switching behaviors.

After agreeing with the measurement results, we apply different groups of simulations. First, the impact of Cge is studied for the case where the higher Cge gives higher IGBT turn-on losses, while it doesn't affect the turn-off behaviors. Second, the impact of Cgc is also simulated. Cgc controls the dVge/dt. Thus, it affects both the IGBT turn-on and turn-off losses. The higher Cgc results the higher turn-on and turn-off losses. Then, we've done the simulations with different Vge(th) values. The last group of simulations compares the impact of different scaled turn-on and turn-off current sources. The conclusion is displayed in Figure 5.48 and Figure 5.49.

By analyzing the figures, we can get that the IGBT turn-on and diode recovery losses are reduced by 4% by changing Cge from 1000nF to 800nF, 16% by changing Cgc from 3.3nF to 1.1nF, 18% by changing the current sources from scale 1 to scale 2. The IGBT turn-off losses are reduced by 22% by changing Cgc from 3.3nF to 1.1nF, 27% by changing the current sources from scale 1 to scale 2.

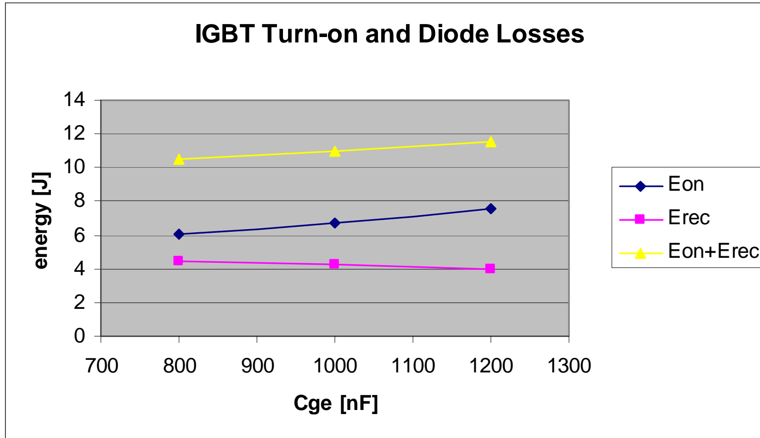


*Figure 5.46: Cge Impact on IGBT Turn-on and Diode Recovery Losses*

The simulation conditions in Figure 5.46 are set as: Ls=200nH, Cgc=1.1nF, Cge=800nF, 1000nF, 1200nF, Vcc=2700V, Ia(on)=2000A, Ig=5.18A (constant), T=400K.

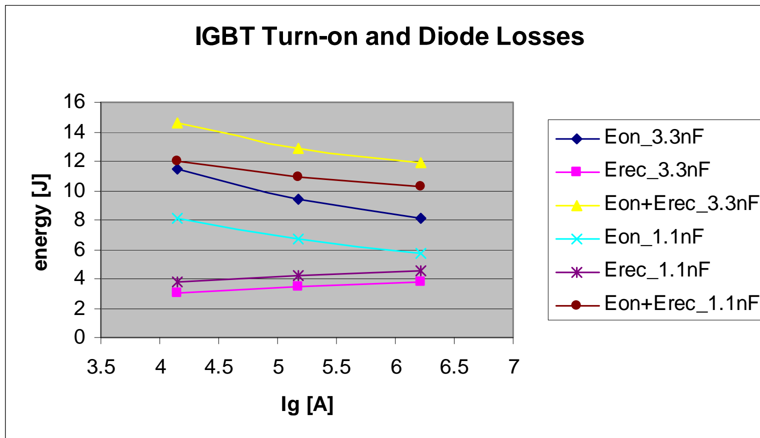


*Figure 5.47: Cgc Impact on IGBT Turn-on and Diode Recovery Losses*

The simulation conditions in Figure 5.46 are set as: Ls=200nH, Cgc=1.1nF, 3.3nF, Cge=1000nF, Vcc=2700V, Ia=2000A, Ig(on)=4.14A, 5.18A, 6.22A, T=400K.

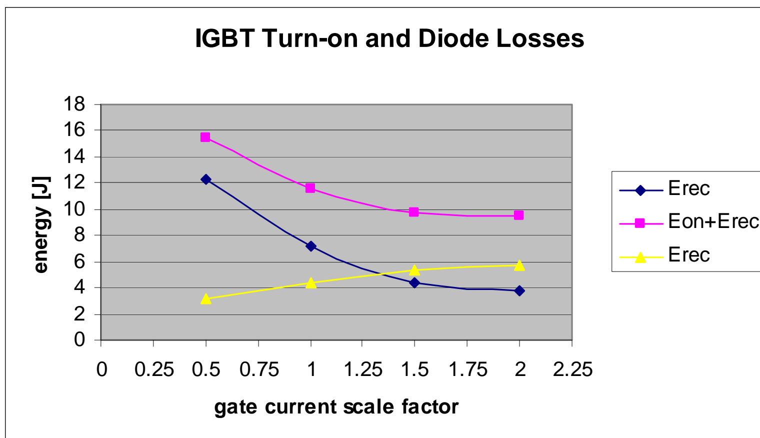


*Figure 5.48: IGBT Turn-on and Diode Recovery Losses with Different Scaled Turn-on Current Sources*

The simulation conditions in Figure 5.48 are set as: Ls=200nH, Cgc=1.1nF, Cge=990nF, Vcc=2800V, Ia(on)=2000A, Ig=0.5, 1, 1.5, 2 scale of standard settings, T=400K.

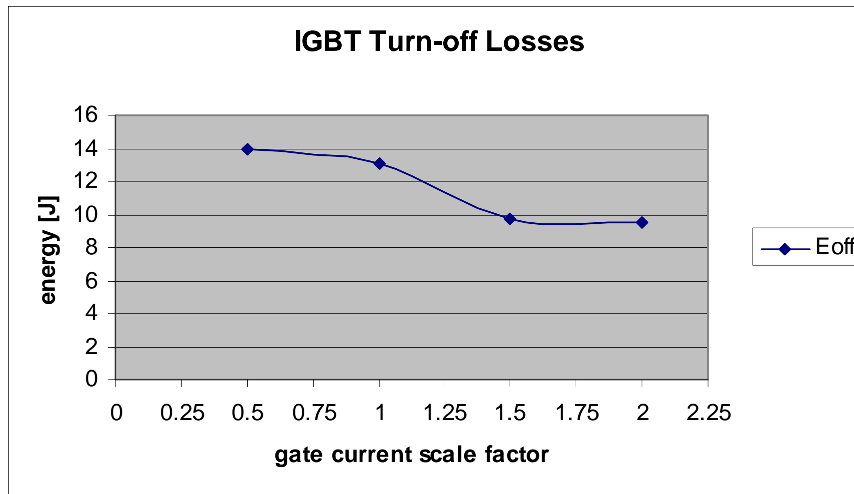


*Figure 5.49: IGBT Turn-off Losses with Different Scaled Turn-off Current Sources*

The simulation conditions in Figure 5.49 are set as: Ls=200nH, Cgc=1.1nF, Cge=990nF, Vcc=2800V, Ia=2000A, Ig(off)=0.5, 1, 1.5, 2 scale of standard settings, T=400K.

# Chapter 6
# Conclusion and Future Work

This chapter summarizes the work in this thesis and puts forward future aims in this field.

## 6.1 Conclusions

Sentaurus Device has been installed at ABB Corporate Research, Sweden. The HVDC Light™ gate unit has been implemented in Sentaurus Device. Through the simulation of HVDC Light™ gate unit, the software Sentaurus Device has been evaluated.

Sentaurus Device combines a good numerical model of IGBT and a complex external circuit. The steady-state characteristics of IGBT don't agree with the data sheet very well because the fine-tuning of the IGBT numerical model mainly focuses on the dynamic properties. The simulation results of IGBT switching match with the experimental measurements fairly well. It's capable to simulate the IGBT switching behaviors to optimize the HVDC Light™ gate unit to reduce the IGBT switching losses.

Several different groups of simulations were carried out to show the impact of different parameters in the gate unit on the IGBT switching losses. The gate-emitter capacitance Cge affects the IGBT turn-on behavior. The increased Cge increases the IGBT turn-on losses. The gate-collector capacitance Cgc affects both the IGBT turn-on and turn-off behaviors. The higher value of Cgc gives higher losses. The higher amplitude of gate current sources gives the lower IGBT turn-on and turn-off losses. But it results the steeper dIc/dt.

## 6.2 Future Work

Though Sentaurus Device is capable to simulate the IGBT switching behaviors with a rather complex external gate unit circuit, the simulation is time consuming. The Workbench in TCAD software package can be applied for a group of simulations. In the thesis due to the time limitation, it doesn't carry out the project control solution by Workbench.

The convergence of the voltage controlled switches in the gate unit circuit is a big problem. In the thesis, the solution is done by changing the current source time sequence and omitting the switches. The convergence problem can also be solved by changing the settings of solve and math sections in the command file or replacing the voltage controlled switches with MOSFET, which are not carried out in the thesis.

The same numerical model of IGBT with different external circuit (not only the HVDC Light™) can also be simulated and evaluated. It could be used for the other projects in ABB Corporate Research, Sweden, e.g. the DC breaker.

ABB Corporate Research, Sweden will decide if the Sentaurus Device simulation environment will be installed, considering the cost of the software package and the competence using the software build-up.

# Appendix

This is the command file for Sentaurus Device which combines the IGBT model and HVDC Light™ gate unit. It represents the single-pulse test to simulate the IGBT switching transient behaviours.

```
#  Sdevice input: turn-on / turn-off simulation
#
HVDC_GU_SPT_400K2800V2000A_HThp47igbt_HT45B20b_diode_200n
H_660nF_delay14_2V"
#  emitter ind = 0.0 nH
#  stray inductance = 200 nH
Device igbt {
     file {
          grid   = "grid/HThp47igbt_tau_mdr"
          doping = "grid/HThp47igbt_tau_mdr"
          lifetime="grid/HThp47igbt_tau_mdr"
#         load   = "sol/XXXX_des"
          param  = "input/par10q.par"
     }
     electrode {
          #collector
          { name="cathode" voltage=0 areafactor=8.8e7 }

          #emitter
          { name="anode" voltage=0 areafactor=8.8e7 }

          #gate
          { name="gate" barrier=-0.55 voltage=0
areafactor=8.8e7 }
     }
        physics {
#               In = 2000 A
          temperature=400
          thermodynamic
                EffectiveIntrinsicDensity(BennettWilson)
                OxideCharge = 0
                Recombination ( SRH(DopingDependence
ExpTemperatureDependence)
          Auger Avalanche(Eparallel) )
                Mobility ( DopingDependence
                HighFieldSaturation
                NormalElectricField
                CarrierCarrierScattering )
        }
     math {
#          Cylindrical
     }
}
```

```
Device diode {
file {
     grid      ="grid/HT45B20b_diode_mdr.grd"
     doping    ="grid/HT45B20b_diode_mdr.dat"
#    output    = "360R_560B_RT_HeHe_7e_des.log"
#    plot      = "360R_560B_RT_HeHe_7e_des.dat"
#    save      = "360R_560B_RT_HeHe_7e_des.sav"
#    current   = "360R_560B_RT_HeHe_7e_des.plt"
        parameters = "input/pard14.par"
        PMIUserFields="grid/HT45B20b_diode_mdr.dat"
}

     electrode {
          #cathode n+
          { name="cathode" voltage=0 areafactor=3.816e6 }

          #anode p+
          { name="anode" voltage=0 areafactor=3.816e6 }
     }
physics {
        temperature=400
#        AreaFactor = 1.06e5
     EffectiveIntrinsicDensity(slotboom)
          Recombination (
          SRH (
               DopingDependence
               TemperatureDependence
              )
          Auger
                Avalanche (VanOverstraeten
GradQuasiFermi)
                     )

         Traps(
               (
                 * VO
                 Acceptor Level
                 EnergyMid=0.16 fromCondBand
                 Conc=4.06e15
                 eXsection=8e-15 hXsection=3e-14
eGfactor=1 hGfactor=1
                 Sfactor="DeepLevels"
                 Add2TotalDoping
               )

               (
                 * O-O
                 Donor Level
                 EnergyMid=0.356 fromValBand
                 Conc=4.06e15
```

```
                  eXsection=4e-16 hXsection=2e-16
eGfactor=1 hGfactor=1
                  Sfactor="PMIUserField0"
                  Add2TotalDoping
                )
              )

        Mobility ( phumob(phosphorus)
                   HighFieldSaturation
     )
}

     math {
          #Cylindrical
     }
}

File {
        SPICEPath = "input"
     output=
"output/HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B2
0b_diode_200nH_660nF_14_2V"
     current =
"output/HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B2
0b_diode_200nH_660nF_14_2V"
     plot =
"output/HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B2
0b_diode_200nH_660nF_14_2V"
}
System {
        igbt igbt ("cathode"=node4 "anode"=node5
"gate"=node3)                  #IGBT
     diode diode ("cathode"=node6 "anode"=node5)
               #DIODE
     Inductor_pset  l5    (node6 node7) {inductance=200e-
9}   # uHcm2        #stray ind
        Initialize ( l5.branch = 0 )
     Inductor_pset  l1    (node4a node4b)
     {inductance=1e-12}       #emitter ind
        Initialize ( l1.branch = 0 )
     Inductor_pset  l2    (node4b 0)
     {inductance=1e-12}       #emitter ind
        Initialize ( l2.branch = 0 )
     Inductor_pset  lg1   (node3b node3a)
     {inductance=1e-12}       #gate ind
        Initialize ( lg1.branch = 0 )
     Inductor_pset  lg2   (node3c node3b)
     {inductance=1e-12}       #gate ind
        Initialize ( lg2.branch = 0 )
     Inductor_pset  lgc   (node2 node2a)
     {inductance=1e-12}       #gate coll ind
```

```
        Initialize ( lgc.branch = 0 )
     Resistor_pset  rl1  (node4 node4a) {resistance=1e-6}
               #stray ind res
     Resistor_pset  rl   (node7 node8)
     {resistance=0.001}            #stray ind res
        Resistor_pset    rg   (node9 node333)
{resistance=0.001}            #gate test res
        Resistor_pset    rgg  (node3a node3)
{resistance=0.001}            #gate test res
        Resistor_pset    rg3  (node3c node33)
{resistance=0.001}            #gate test res
        Resistor_pset    rg4  (node33 node333)
{resistance=0.001}            #gate test res
        Resistor_pset    ra1  (nodes1 0)
{resistance=0.001}                 #gate test res
        Resistor_pset    ra2  (nodes2 0)
{resistance=0.001}                 #gate test res
        Resistor_pset    ra3  (nodes3 0)
{resistance=0.001}                 #gate test res
        Capacitor_pset  cgc     (node3a node2)
{capacitance=1.1e-9}               #CE feedback
        Capacitor_pset  cgg     (node3 node4)
{capacitance=1e-12}           #CG feedback
        Resistor_pset    rs   (node2a node5)
     {resistance=9}                #CE feedback

        Resistor_pset    rg1  (node3a 0)
     {resistance=100e3}            #gate res
#       Resistor_pset    rg11 (node3a nodeg1)
     {resistance=1.0e6}            #gate delay
#        Resistor_pset   rge1 (nodeg1 nodeg2)
     {resistance=1.1e3}            #gate delay
#        Capacitor_pset  cge1    (nodeg2 0)
{capacitance=1.0e-11}              #gate delay
#        Resistor_pset   rge2 (nodeg2 nodeg3)
     {resistance=1.1e3}            #gate delay
#        Capacitor_pset  cge2    (nodeg3 0)
{capacitance=1.0e-11}              #gate delay
#        Resistor_pset   rge3 (nodeg3 nodeg4)
     {resistance=1.1e3}            #gate delay
#        Capacitor_pset  cge3    (nodeg4 0)
{capacitance=1.0e-11}              #gate delay
#        Resistor_pset   rge4 (nodeg4 nodeg5)
     {resistance=1.1e3}            #gate delay
#        Capacitor_pset  cge4    (nodeg5 0)
{capacitance=1.0e-11}              #gate delay
#        Resistor_pset   rge5 (nodeg5 nodeg6)
     {resistance=1.1e3}            #gate delay
#        Capacitor_pset  cge5    (nodeg6 0)
{capacitance=1.0e-11}              #gate delay
```

```
        Resistor_pset    rbr1 (node5 node51)
     {resistance=7920}             #switch delay
        Resistor_pset    rbr2 (node51 node4b)
     {resistance=80}                    #switch delay
        Resistor_pset    rde1 (node51 node52)
     {resistance=80}                    #switch delay
        Capacitor_pset  cde1    (node52 node4b)
{capacitance=1.0e-10}              #switch delay
        Resistor_pset    rde2 (node52 node53)
     {resistance=80}                    #switch delay
        Capacitor_pset  cde2    (node53 node4b)
{capacitance=1.0e-10}              #switch delay
        Resistor_pset    rde3 (node53 node54)
     {resistance=80}                    #switch delay
        Capacitor_pset  cde3    (node54 node4b)
{capacitance=1.0e-10}              #switch delay
        Resistor_pset    rde4 (node54 node55)
     {resistance=80}                    #switch delay
        Capacitor_pset  cde4    (node55 node4b)
{capacitance=1.0e-10}              #switch delay
        Resistor_pset    rde5 (node55 node56)
     {resistance=80}                    #switch delay
        Capacitor_pset  cde5    (node56 node4b)
{capacitance=1.0e-10}              #switch delay

        Vsource_pset    vdd     (node8  node4b) {pulse=(0
2800 2e-6 8e-6 2e-6 790e-6 800e-6)}     #DClink volt

        Vsource_pset    vclp    (node26  0)     {pulse=(0
15.0 1e-7 9e-7 1e-7 799e-6 800e-6)}     #pos gate clp
        DIO_pset        diclp   (node333 node12)
{area=0.5 }         #schottky #pos gate clp
        Resistor_pset   rclp3   (node25 node26)
{resistance=0.1}              #pos gate clp
     Inductor_pset  lclp (node13 node25)
     {inductance=1e-8}             #pos gate clp
        Capacitor_pset  cclp2   (node25 0)
{capacitance=6.6e-6}               #pos gate clp
        Capacitor_pset  cclp1   (node13 0)
{capacitance=8.0e-6}               #pos gate clp
        Resistor_pset   rclp1   (node12 node13)
{resistance=0.25}             #pos gate clp
        Resistor_pset   rclp2   (node25 node27)
{resistance=0.5}              #pos gate clp
#    Capacitor_pset  crclp2  (node25 node27)
{capacitance=2e-7}            #pos gate clp
        swclDe_pset     swclp1  (node333 node27a node3a
0) { }                   #pos gate clp
     Capacitor_pset  cswclp1 (node333 node27a)
{capacitance=1e-13}           #pos gate clp
```

```
        swclBa_pset     swclp2  (node27 node27a node200
0) { }                  #pos gate clp
     Capacitor_pset  cswclp2 (node27 node27a)
{capacitance=1e-13}          #pos gate clp
        Vsource_pset    v333    (node200  0)
{pulse=(0 300 1e-7 299.9e-6 99.9e-6 1e-7 400e-6)}
     #pos gate clp

        Vsource_pset    vcln    (0  node11)     {pulse=(0
4.1 1e-7 9e-7 1e-7 799e-6 800e-6)} #neg gate clp
        Diode_pset      dicln   (node10 node33) {area=0.5
}                        #neg gate clp
        Resistor_pset   rcln    (node10 node11)
{resistance=0.01}                 #neg gate clp

        Vsource_pset    vcon    (node15 node16) {pulse=(0
6.2 1e-7 9e-7 1e-7 799e-6 800e-6)} #dIdt control
        dioD4_pset      dicon   (node14 node15)
{area=0.01 }                      #dIdt control
        Resistor_pset   rdicon  (node14
node15a){resistance=3.3}               #dIdt control
        Capacitor_pset  cdicon  (node15a
node15){capacitance=33e-9}                  #dIdt
control

        Resistor_pset   rcon    (node33 node14)
{resistance=0.25}                 #dIdt control
        Capacitor_pset  cge     (node16 0)
{capacitance=660e-9}                   #dIdt control
        Resistor_pset   rdis    (node16 node23)
{resistance=0.5}                    #changed     #dIdt
control
        Vsource_pset    vdis    (0 node24)      {pulse=(0
5 1e-7 9e-7 1e-7 799e-6 800e-6)}   #dIdt control
        swdM_pset       swdis   (node24 node23 node100 0)
{ }                        #roff=5000   #dIdt control
        Vsource_pset    vccc    (node100 0)     {pulse=(0
100 92e-6 1e-6 0.1e-6 7e-6 400e-6)}     #dIdt control

        Resistor_pset   rsnb1   (node17 node18)
{resistance=10}                        #IGBT snb
        Diode_pset      disnb1  (node5 node17)  {area=5 }
                         #IGBT snb
        Resistor_pset   rsnb2   (node18 node4b)
{resistance=1.8e4}                #IGBT snb
        Capacitor_pset  csnb1   (node18 node4b)
{capacitance=1760e-9}                  #IGBT snb
#    Initialize     ( node18 = 2000 )
        Isource_pset    isnb1   (node18 node19) {
dc=0.025}                    #IGBT snb
```

```
        Vsource_pset    vsnb1   (node19 node4b) { dc=300}
                         #IGBT snb
        Resistor_pset   rsnb3   (node18 node19)
{resistance=8.1e4}                #IGBT snb

        Resistor_pset   rsnb4   (node20 node21)
{resistance=10}                        #diode snb
        Diode_pset      disnb2  (node6 node20)  {area=5 }
                         #diode snb
        Resistor_pset   rsnb5   (node21 node5)
{resistance=1.8e4}                #diode snb
        Capacitor_pset  csnb2   (node21 node5)
{capacitance=1760e-9}                  #diode snb
#    Initialize     ( node21 = 2000 )
        Isource_pset    isnb2   (node21 node22) {
dc=0.025}                    #diode snb
        Vsource_pset    vsnb2   (node22 node5)  { dc=300}
                         #diode snb
        Resistor_pset   rsnb6   (node21 node22)
{resistance=8.1e4}                #diode snb

        Isource_pset    ic      (node4b node5) {pulse=(0
2000  10e-6 88e-6 2e-6 702e-6  800e-6)}#coll current
     Isource_pset    igon0   (0 nodesw0)    {pulse=(0
0.00  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
     Isource_pset    igon1   (0 nodesw1)    {pulse=(0
18.34  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
        Isource_pset    igon2   (0 nodesw2)    {pulse=(0
4.06  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
        Isource_pset    igon3   (0 nodesw3)    {pulse=(0
0  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
        Isource_pset    igon4   (0 nodesw4)    {pulse=(0
7.35  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
        Isource_pset    igon5   (0 nodesw5)    {pulse=(0
0.00  100e-6 1e-7 1e-7 199.8e-6 400e-6)}#turn-on source
        Isource_pset    igaux   (node9 nodes1) {pulse=(0
2.00  1e-7   9e-7 1e-6 20e-6 800e-6)}   #aux gate source
        Isource_pset    igoff0  (node9 nodes2) {pulse=(0
5.5  300e-6 1e-7 1e-7 200e-6 800e-6)}   #toff source
        Isource_pset    igoff0a (node9 nodes3) {pulse=(0
5.5  700e-6 1e-7 1e-7 100e-6 800e-6)}   #toff source
        Isource_pset    igoff1  (0 nodesw6)    {pulse=(0
2.4  300e-6 1e-7 1e-7 200e-6 800e-6)}   #toff source
        Isource_pset    igoff1a (0 nodesw6)    {pulse=(0
2.4  700e-6 1e-7 1e-7 100e-6 800e-6)}   #toff source
        Isource_pset    igoff2  (0 nodesw7)    {pulse=(0
2.0  300e-6 1e-7 1e-7 200e-6 800e-6)}   #toff source
        Isource_pset    igoff2a (0 nodesw7)    {pulse=(0
2.0  700e-6 1e-7 1e-7 100e-6 800e-6)}   #toff source
        Isource_pset    igoff3  (0 nodesw8)    {pulse=(0
0.55  300e-6 1e-7 1e-7 200e-6 800e-6)}#toff source
```

```
        Isource_pset    igoff3a (0 nodesw8)    {pulse=(0
0.55  700e-6 1e-7 1e-7 100e-6 800e-6)}#toff source
        Isource_pset    igoff4  (0 nodesw9)    {pulse=(0
0.35  300e-6 1e-7 1e-7 200e-6 800e-6)}#toff source
        Isource_pset    igoff4a (0 nodesw9)    {pulse=(0
0.35  700e-6 1e-7 1e-7 100e-6 800e-6)}#toff source
        Isource_pset    igoff5  (0 nodesw10)   {pulse=(0
0.1  300e-6 1e-7 1e-7 200e-6 800e-6)}   #toff source
        Isource_pset    igoff5a (0 nodesw10)   {pulse=(0
0.1  700e-6 1e-7 1e-7 100e-6 800e-6)}   #toff source

        sw0s_pset       sw0s    (nodesw0 nodesw01 node53
0) { }                        #switch0
        sw01mod9g_pset   sw01    (nodesw01 node9 node3a
0) { }                        #switch01
        Diode_pset      disw0   (nodesw0 nodedw0)
{area=0.5 }                        #sw0 commute
        Vsource_pset    vsw0    (nodedw0 0) { dc=100 }
                         #sw0 commute
        Capacitor_pset  csw0    (nodesw0 nodesw01)
{capacitance=1e-13}                #sw0 commute
        Capacitor_pset  csw01   (nodesw01 node9)
{capacitance=1e-13}                #sw0 commute
        Capacitor_pset  cdw0    (nodedw0 0)
{capacitance=1e-13}                #sw0 commute

        sw1s_pset       sw1s    (nodesw1 nodesw11 node53
0) { }                        #switch1
        sw01mod9g_pset   sw11    (nodesw11 node9 node3a
0) { }                        #switch11
        Diode_pset      disw1   (nodesw1 nodedw1)
{area=0.5 }                        #sw1 commute
        Vsource_pset    vsw1    (nodedw1 0) { dc=100 }
                         #sw1 commute
        Capacitor_pset  csw1    (nodesw1 nodesw11)
{capacitance=1e-13}                #sw1 commute
        Capacitor_pset  csw11   (nodesw11 node9)
{capacitance=1e-13}                #sw1 commute
        Capacitor_pset  cdw1    (nodedw1 0)
{capacitance=1e-13}                #sw1 commute

        sw2s_pset       sw2s    (nodesw2 nodesw21 node53
0) { }                        #switch2
        sw01mod9g_pset   sw21    (nodesw21 node9 node3a
0) { }                        #switch21
        Diode_pset      disw2   (nodesw2 nodedw2)
{area=0.5 }                        #sw2 commute
        Vsource_pset    vsw2    (nodedw2 0) { dc=100 }
                         #sw2 commute
        Capacitor_pset  csw2    (nodesw2 nodesw21)
{capacitance=1e-13}                #sw2 commute
```

```
        Capacitor_pset  csw21   (nodesw21 node9)
{capacitance=1e-13}               #sw2 commute
        Capacitor_pset  cdw2    (nodedw2 0)
{capacitance=1e-13}               #sw2 commute

        sw3s_pset       sw3s    (nodesw3 nodesw31 node53
0) { }                          #switch3
        sw01mod9g_pset   sw31    (nodesw31 node9 node3a
0) { }                          #switch31
        Diode_pset      disw3   (nodesw3 nodedw3)
{area=0.5 }                       #sw3 commute
        Vsource_pset    vsw3    (nodedw3 0) { dc=100 }
                         #sw3 commute
        Capacitor_pset  csw3    (nodesw3 nodesw31)
{capacitance=1e-13}               #sw3 commute
        Capacitor_pset  csw31   (nodesw31 node9)
{capacitance=1e-13}               #sw3 commute
        Capacitor_pset  cdw3    (nodedw3 0)
{capacitance=1e-13}               #sw3 commute

        sw4s_pset       sw4s    (nodesw4 nodesw41 node53
0) { }                          #switch4
        sw01mod9g_pset   sw41    (nodesw41 node9 node3a
0) { }                          #switch41
        Diode_pset      disw4   (nodesw4 nodedw4)
{area=0.5 }                       #sw4 commute
        Vsource_pset    vsw4    (nodedw4 0) { dc=100 }
                         #sw4 commute
        Capacitor_pset  csw4    (nodesw4 nodesw41)
{capacitance=1e-13}               #sw4 commute
        Capacitor_pset  csw41   (nodesw41 node9)
{capacitance=1e-13}               #sw4 commute
        Capacitor_pset  cdw4    (nodedw4 0)
{capacitance=1e-13}               #sw4 commute

        sw5s_pset       sw5s    (nodesw5 nodesw51 node53
0) { }                          #switch5
        sw01mod9g_pset  sw51    (nodesw51 node9 node3a 0)
{ }                      #switch51
        Diode_pset      disw5   (nodesw5 nodedw5)
{area=0.5 }                       #sw5 commute
        Vsource_pset    vsw5    (nodedw5 0) { dc=100 }
                         #sw5 commute
        Capacitor_pset  csw5    (nodesw5 nodesw51)
{capacitance=1e-13}               #sw5 commute
        Capacitor_pset  csw51   (nodesw51 node9)
{capacitance=1e-13}               #sw5 commute
        Capacitor_pset  cdw5    (nodedw5 0)
{capacitance=1e-13}               #sw5 commute
```

```
        sw6s_pset       sw6s    (nodesw6 node9 node53 0)
{ }                      #switch6
        Diode_pset      disw6   (nodesw6 nodedw6)
{area=0.5 }                         #sw6 commute
        Vsource_pset    vsw6    (nodedw6 0) { dc=100 }
                         #sw6 commute
        Capacitor_pset  csw6    (nodsw6 node9)
{capacitance=1e-13}                 #sw6 commute

        sw7s_pset       sw7s    (nodesw7 node9 node53 0)
{ }                      #switch7
        Diode_pset      disw7   (nodesw7 nodedw7)
{area=0.5 }                         #sw7 commute
        Vsource_pset    vsw7    (nodedw7 0) { dc=100 }
                         #sw7 commute
        Capacitor_pset  csw7    (nodesw7 node9)
{capacitance=1e-13}                 #sw7 commute

        sw8s_pset       sw8s    (nodesw8 node9 node53 0)
{ }                      #switch8
        Diode_pset      disw8   (nodesw8 nodedw8)
{area=0.5 }                         #sw8 commute
        Vsource_pset    vsw8    (nodedw8 0) { dc=100 }
                         #sw8 commute
        Capacitor_pset  csw8    (nodesw8 node9)
{capacitance=1e-13}                 #sw8 commute

        sw9s1_pset      sw9s1   (nodesw9 node9 node53 0)
{ }                      #switch9
        Diode_pset      disw9   (nodesw9 nodedw9)
{area=0.5 }                         #sw9 commute
        Vsource_pset    vsw9    (nodedw9 0) { dc=100 }
                         #sw9 commute
        Capacitor_pset  csw9    (nodesw9 node9)
{capacitance=1e-13}                 #sw9 commute

        sw10s_pset      sw10s   (nodesw10 node9 node53 0)
{ }                      #switch10
        Diode_pset      disw10  (nodesw10 nodedw10)
{area=0.5 }                         #sw10 commute
        Vsource_pset    vsw10   (nodedw10 0) { dc=100 }
                              #sw10 commute
        Capacitor_pset  csw10   (nodesw10 node9)
{capacitance=1e-13}                 #sw10 commute

        Initialize ( node3=0 node4=0 node5=0 node6=0
node9=0 )
        Plot
"HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B20b_diod
e_200nH_660nF_14_2V"
                                        ( time()
```

```
                           i(sw0s nodesw01)
#current switch0
                        v(nodesw0 nodesw01)
     #voltage switch0
                        i(sw01 node9)        #current
switch01
                        v(nodesw01 node9)
     #voltage switch01
                        i(csw0 nodesw01)
     #current cap csw0
                        i(csw01 node9)       #current cap
csw01
                        i(disw0 nodedw0)
     #current diode switch0
                        v(nodesw0 nodedw0)
     #voltage diode switch0
                        i(cdw0 0)            #current cap
cdw0

                                    i(sw1s nodesw11)
     #current switch1
                                    v(nodesw1 nodesw11)
     #voltage switch1
                        i(sw11 node9)        #current
switch11
                        v(nodesw11 node9)
     #voltage switch11
                        i(csw1 nodesw11)
     #current cap csw1
                        i(csw11 node9)       #current cap
csw11
                        i(disw1 nodedw1)
     #current diode switch1
                        v(nodesw1 nodedw1)
     #voltage diode switch1
                        i(cdw1 0)            #current cap
cdw1

                              i(sw2s nodesw21)
     #current switch2
                                    v(nodesw2 nodesw21)
          #voltage switch2
                        i(sw21 node9)        #current
switch21
                        v(nodesw21 node9)
     #voltage switch21
                        i(csw2 nodesw21)
     #current cap csw2
                        i(csw21 node9)       #current cap
csw21
```

```
                        i(disw2 nodedw2)
     #current diode switch2
                        v(nodesw2 nodedw2)
     #voltage diode switch2
                        i(cdw2 0)           #current cap
cdw2

                                    i(sw3s nodesw31)
     #current switch3
                                    v(nodesw3 nodesw31)
          #voltage switch3
                        i(sw31 node9)       #current
switch31
                        v(nodesw31 node9)
     #voltage switch31
                        i(csw3 nodesw31)
     #current cap csw3
                        i(csw31 node9)      #current cap
csw31
                        i(disw3 nodedw3)
     #current diode switch3
                        v(nodesw3 nodedw3)
     #voltage diode switch3
                        i(cdw3 0)           #current cap
cdw3

                                    i(sw4s nodesw41)
     #current switch4
                                    v(nodesw4 nodesw41)
          #voltage switch4
                        i(sw41 node9)       #current
switch41
                        v(nodesw41 node9)
     #voltage switch41
                        i(csw4 nodesw41)
     #current cap csw4
                        i(csw41 node9)      #current cap
csw41
                        i(disw4 nodedw4)
     #current diode switch4
                        v(nodesw4 nodedw4)
     #voltage diode switch4
                        i(cdw4 0)           #current cap
cdw4

                                    i(sw5s nodesw51)
     #current switch5
                                    v(nodesw5 nodesw51)
          #voltage switch5
                        i(sw51 node9)       #current
switch51
```

```
                   v(nodesw51 node9)
     #voltage switch51
                   i(csw5 nodesw51)
     #current cap csw5
                   i(csw51 node9)      #current cap
csw51
                   i(disw5 nodedw5)
     #current diode switch5
                   v(nodesw5 nodedw5)
     #voltage diode switch5
                   i(cdw5 0)           #current cap
cdw5

                               i(sw6s node9)
     #current switch6
                               v(nodesw6 node9)
     #voltage switch6
                   i(csw6 node9)       #current cap
csw6
                   i(disw6 nodedw6)
     #current diode switch6
                   v(nodesw6 nodedw6)
     #voltage diode switch6

                               i(sw7s node9)
     #current switch7
                               v(nodesw7 node9)
     #voltage switch7
                   i(csw7 node9)       #current cap
csw7
                   i(disw7 nodedw7)
     #current diode switch7
                   v(nodesw7 nodedw7)
     #voltage diode switch7

                               i(sw8s node9)
     #current switch8
                               v(nodesw8 node9)
     #voltage switch8
                   i(csw8 node9)       #current cap
csw8
                   i(disw8 nodedw8)
     #current diode switch8
                   v(nodesw8 nodedw8)
     #voltage diode switch8

                               i(sw9s node9)
     #current switch9
                               v(nodesw9 node9)
     #voltage switch9
```

```
                        i(csw9 node9)        #current cap
csw9
                        i(disw9 nodedw9)
     #current diode switch9
                        v(nodesw9 nodedw9)
     #voltage diode switch9

                                    i(sw10s node9)
     #current switch10
                                    v(nodesw10 node9)
     #voltage switch10
                        i(csw10 node9)       #current cap
csw10
                        i(disw10 nodedw10)
     #current diode switch10
                        v(nodesw10 nodedw10) #voltage
diode switch10

                        v(node100 0)         #auxillary
voltage vccc
                        v(node200 0)         #auxillary
voltage v333

                                    i(ra1 nodes1)
     #auxillary gate current source - ramp up
                                    i(ra2 nodes2)
     #gate current source - igoff0
                                    i(ra3 nodes3)
     #gate current source - igoff0a

                                    i(rg node333)
     #gate current test ( Rg )
                        i(rg4 node33)        #gate
current test ( Rg4 )
                                    i(rg3 node3c)
     #gate current test ( Rg3 )
                        i(rgg node3)         #IGBT gate
current ( Rgg )
                        i(rg1 node3a)        #current
through gate resistor Rg1
                                    i(rs node2a)
     #collector feedback to gate current
                        v(node2 node3a)      #voltage
across Cgc

                                    i(rcln node10)
     #neg gate clamp current through Rcln
                                    v(node10 node33)
     #neg gate clamp diode voltage
```

```
                        v(node13 0)               #pos
gate clamp voltage across Cclp1
                        i(cclp1 0)           #pos gate
clamp current through Cclp1
                                    i(rclp1 node13)
     #pos gate clamp current in Rclp1
                        i(diclp node12)      #pos gate
clamp current through diclp
                        v(node333 node12)         #pos
gate clamp voltage across diclp
                                    i(rclp2 node27)
     #pos gate clamp current through Rclp2
                        i(rclp3 node25)      #pos gate
clamp current through Rclp3
                                    v(node333 node27a)
     #pos gate clamp voltage across swclp1
                        v(node27a node27)         #pos
gate clamp voltage across swclp2
                        v(node25 0)               #pos
gate clamp voltage across Cclp2
                        i(cclp2 0)           #pos gate
clamp current through Cclp2
                        i(lclp node25)       #pos gate
clamp current through Lclp
                        v(node13 node25)          #pos
gate clamp voltage across Lclp

                                    i(dicon node15)
     #dIdt control current throught diode
                                    v(node14 node15)
     #dIdt control voltage across diode
                                    i(cge 0)
     #dIdt control current through capacitor Cge
                                    v(node16 0)
     #dIdt control voltage across capacitor Cge
                                    i(rdis
HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B20b_diode
_200nH_660nF_14_2V.innode23)       #dIdt control current
through resistor Rdis
                                    v(node16 node23)
     #dIdt control voltage across resistor Rdis
                                    i(swdis node24)
     #dIdt control current through switch swdis
                                    v(node24 node23)
     #dIdt control voltage across switch swdis

                                    v(node5 node4b)
     #IGBT collector emitter voltage
                                    i(rl1 node4a)
     #IGBT collector current
```

```
                                        v(node3a 0)
     #IGBT gate voltageA
                        v(node3 0)          #IGBT gate
voltage
                        v(node3 node4)      #effective
IGBT gate voltage
                        v(node4 node4a)     #voltage
across rl1
                        v(node4a node4b)
     #voltage across l1
                        v(node4b 0)
     #voltage across l2
                        v(node3c node3b)
     #voltage across lg2
                        v(node3b node3a)
     #voltage across lg2
                        v(node2 node2a)     #voltage
across lgc
                        v(node333 0)        #IGBT test
gate voltage
                        v(node9 0)             #turn-on
source clamp voltage across swcs

                        i(disnb1 node17)         #diode
current IGBT snubber
                        i(disnb2 node20)         #diode
current diode snubber
                        i(csnb1 node4b)     #cap current
IGBT snubber
                        i(csnb2 node5)      #cap current
diode snubber
                        v(node18 0)              #cap
voltage IGBT snubber
                        v(node21 node5)     #cap voltage
diode snubber
                        i(diode node6)      #diode
current
                        v(node6 node5)      #diode
voltage
)
     Plot
"IV_HVDC_GU_SPT_ExpA_400K2800V2000A_HThp47igbt_HT45B20b_d
iode_200nH_660nF_14_2V"
                                        ( time()
                                        i(rl1 node4a)
     #IGBT collector current
                                        v(node3a 0)
     #IGBT gate voltage
                        v(node5 node4b)     #IGBT
collector emitter voltage
```

```
                        i(l5 node7)               #diode
forward current
                                    i(rg node333)
     #gate current test ( Rg )
                        v(node5 node6)       #diode
forward voltage
                        i(diode node5)       #diode
reverse current
                        v(node6 node5)       #diode
reverse voltage
#                       v(node52 node4b)
#                       v(node53 node4b)
#                       v(node54 node4b)
#                       v(node55 node4b)
#                       v(node56 node4b)
     #delayed IGBT collector emitter voltage
#                       v(nodeg1 0)
#                       v(nodeg2 0)
#                       v(nodeg3 0)
#                       v(nodeg4 0)
#                                   v(nodeg5 0)
#                       v(nodeg6 0)
     #delayed IGBT gate emitter voltage
#                       i(rg4 node33)        #gate
current test ( Rg4 )
)
}
math {
     NewDiscretization
        Derivatives
        AvalDerivatives
     Digits=5
     AutomaticCircuitContact
     method=blocked
     Notdamped=1
     Iterations=15
     Extrapolate
     transient=BE
     error(poisson)=1
     error(electron)=1
     error(hole)=1
     error(contact)=1
     error(circuit)=1
#    NoCheckTransientError
     }

plot {
     Potential Edensity Hdensity
        ElectricField/Vector
     eCurrent/Vector hCurrent/Vector TotalCurrent
     eLifetime hLifetime
```

```
     Avalanche
     SRHRecombination AugerRecombination
}

solve {
# Make igbt acceptable
     coupled (digits=6 NotDamped=1){ "igbt".poisson
"igbt".electron "igbt".hole }

# Make the load diode acceptable
        coupled (digits=6 Notdamped=1){ "diode".poisson
"diode".electron "diode".hole }


     Transient ( InitialStep=1e-11 MaxStep=5e-6
MinStep=1e-16
              InitialTime=0 FinalTime=8.0e-4
              Increment=1.1 Decrement=2.5
              Plot{Range=(502.5e-6, 503.5e-6)
Intervals=50}
               )
              { coupled (digits=3 iterations=10
NotDamped=5)
              { poisson electron hole circuit contact} }
}
```

## Reference

[1] Jon Rasmussen, “PSpcie Models for IGBT Position and H-bridge Test Circuit”, ABB Internal, June 2003

[2] Sentaurus Device User Guide, Version A-2008-09, Synopsys, September 2009

[3] ‘’ABB StakPak™ K Series Press-pack IGBT 5SNA 200045K0301 Draft’’, ABB Internal, June 2008

[4] ‘’ABB HiPak™ IGBT Module 5SNA 1000G450300 Preliminary’’, ABB Internal, October 2007

[5] Friedhelm Bauer, “HVDC Light™ Gate Unit Implementation in DESSIS: part 1.”, ABB Internal, July 2006

[6] Friedhelm Bauer, “HVDC Light™ Gate Unit Implementation in DESSIS: part 2.”, ABB Internal, November 2006

[7] Friedhelm Bauer, “HVDC Light™ Gate Unit Implementation in DESSIS: part 3-4.5kV SPT+ grids.”, ABB Internal, May 2008

[8] Willy Hermansson, “DESSIS Simulations of IGBT Switching. Study of Various Gate Drive Settings and Effect on Losses on C-technology IGBTs.”, ABB Internal, November 2007

[9] A-C Lerström, Ingvar Hagman, “IGBT Position Model”, ABB Internal, August 2001

[10] L. Benbahouche, S. Latrech, “New Numerical Power IGBT Model and Simulation of its Electrical Characteristics”, Smolenice Castle, Slovakia, 14-16 October 2002

[11] N. Mohan, T. Undeland, W. Robbins, ‘’Power Electronics Converters, Applications, and Design’’, 3rd Edition, Wiley