THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

CONTROL OF STATIC SERIES COMPENSATOR FOR MITIGATION OF POWER QUALITY PROBLEMS

by

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ABSTRACT

Power Electronics and Advanced Control technologies have made it possible to mitigate power quality problems and maintain the operation of sensitive loads. Among power system disturbances, voltage dips, swells, and harmonics are some of the severe problems to the critical industrial loads. The static series compensator (SSC) is best suited to protect such loads against those disturbances. This thesis focuses on the control of the SSC in order to improve the transient and the steady-state responses and increase its injection capability.

To mitigate voltage dips, the thesis proposes a vector-controlled based algorithm to improve the transient and the steady-state responses of the SSC. The developed algorithm incorporates both current and voltage controllers with an inner current loop and outer voltage loop. Thus, it is referred to as the Double Vector Control (DVC) algorithm. To cope with unbalanced dips, a fast technique to detect the positive and the negative sequences is employed. Then the two sequences are controlled separately. Also the influence of the switching frequency on the controller performance is studied.

A Software Phase Locked Loop with a PI controller is proposed in order to obtain the phase and the frequency information of the grid voltage. The tuning of the PI controller is made according to a developed criterion based on the frequency requirements of the loads.

A number of power system events are studied and the behavior of the SSC is tested against each event. These events include short-circuit faults, capacitor-bank energizing, transformer energizing and load switching (linear and non-linear loads). Recommendations regarding the SSC operation for each event are given.

The possibility of employing the SSC to mitigate voltage swells and overvoltages is investigated. An overvoltage protection scheme is proposed, based on a combination of a dc resistor with a chopper and the SSC. The design equations of the dc resistor together with the chopper are provided.

In order to mitigate voltage harmonics, a new controller is developed and implemented. In the proposed controller, a moving average filter is implemented in the synchronous reference frame to extract the fundamental component of the measured voltages and currents. Also, an active filtering capability is added by using the resonant filters for the 5^{th} and the 7^{th} harmonics. After the extraction of the fundamental component, it is controlled by the DVC. The operation of the SSC under distorted utility conditions and voltage dips is discussed.

The thesis also proposes two control techniques to charge the energy storage capacitor of the SSC. One of the techniques is based on a shunt diode rectifier, which is placed either on the load side or the grid side (both configurations are studied). The other technique exploits the voltage source converter of the SSC in combination with a proper control algorithm to charge the capacitor. A design guide for the energy storage capacitor is given.

To minimize the required active power, this thesis discusses and compares four different compensation strategies: 1) Voltage Difference Compensation; 2) In-Phase Compensation; 3) Phase Advance Compensation; 4) Progressive Phase Advance Compensation. The effect of the load power factor on the different strategies is investigated. A control algorithm based on a combination of the four strategies is proposed taking into account the minimization of the active power and keeping the injected voltage within the ratings of the SSC.

The validity of the developed controllers is verified by simulations and experiments. The simulation models are developed and implemented in the PSCAD/EMTDC package. A 10 kV SCC prototype is exploited to carry out the experiments with various load types.

KEYWORDS:

Custom Power, Dynamic Voltage Restorer, Energy Storage, Power Electronics, Power Quality, Static Series Compensator, Vector Control, Voltage Dips, Voltage Swells, Voltage Harmonics.

PREFACE

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LIST OF PUBLICATIONS

PUBLISHED PAPERS

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[2] H. Awad, J. Svensson, M.H.J. Bollen, "Phase-locked loop for static series compensator," *in Proc. of European Power Electronics Conference, EPE* 2003, Toulouse, France, Sep. 2003.

[3] H. Awad, J. Svensson, M.H.J. Bollen, " Static series compensator for voltage dips mitigation," *in Proc. of the IEEE PowerTech Conference,* 2003*,* Bologna, Italy.

[4] H. Awad, J. Svensson, M.H.J. Bollen, " Testing static series compensator against capacitor bank energizing," *in Proc. of the IEEE PowerTech Conference*, 2003*,* Bologna, Italy.

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[13] H. Awad, M.H.J. Bollen, "Energy optimization control techniques by static series compensator for constant power factor loads," *in Proc. of the IEEE Power Engineering Society General Meeting,* PES GM 2004, accepted.

[14] H. Awad, F. Blaabjerg, "Mitigation of voltage swells by static series compensator," *in Proc. of the IEEE Power Electronics Specialist Conference*, PESC 2004, accepted.

[15] H. Awad, F. Blaaberg, "Operation of static series compensator under distorted utility conditions," *IEEE Trans. on Power Systems*, accepted.

CONTENTS

CHAPTER

1. INTRODUCTION

1.1. BACKGROUND AND MOTIVATION

Modern industrial processes are based on a large amount of electronic devices such as programmable logic controllers and adjustable speed drives. Unfortunately, electronic devices are sensitive to disturbances, and thus, industrial loads become less tolerant to power quality problems such as voltage dips, voltage swells, and harmonics.

Voltage dips are considered the most severe disturbances to the industrial equipment [1,2]. A paper machine can be affected by disturbances of only 10 % voltage drop lasting for 100 ms [3]. A voltage dip of 75 % (of the nominal voltage) with duration shorter than 100 ms can result in material loss in the range of thousands of US dollars for the semiconductors industry [4].

Swells and overvoltages can cause overheating, tripping or even destruction of industrial equipment such as motor drives, surge arrestors and control relays. From the reference [5], the following statement is quoted: " *There are about 100 million US Dollars direct losses of damaged electronic devices caused by lightning overvoltage in Shanghai, China, 1999. So, adopting effective measurements and devices to protect these electronic systems from being damaged by electromagnetic impulse and overvoltage is very urgent*."

Harmonic contamination has become a problem to sensitive loads. The effect of harmonic distortion on equipment and power system operation is documented in many textbooks such as [6] and [7], and in research publications, for instance [8] and [9]. The electronic equipment is a very sensitive load against harmonics because their control depends on either the peak value, or the zero crossing of the supplied voltage, which are all influenced by the harmonic distortion.

To overcome the mentioned problems, the concept of custom power has been introduced recently [2,10]. Custom power is a strategy, which is designed primarily to meet the requirements of industrial and commercial customers. The concept of custom power is to use power electronics or static controllers in the medium voltage distribution system aiming to supply reliable and high-quality power to sensitive users.

Power electronic valves are the basis of those custom power devices such as the static transfer switch, active filters and converter-based devices. Converter-based power electronics devices can be divided into two main groups: shunt-connected and series-connected devices. Both shunt- and series-connected devices have been proposed in literature for the medium-voltage applications. The shunt-connected device is known as the Distribution Static Compensator (DSTATCOM) [11,12] and the series device is known as the Static Series Compensator (SSC), commercially known as the dynamic voltage restorer [3, 13, 14, 15]. It has also been reported in literature that both the SSC and DSTATCOM have been used to mitigate the majority of the power system disturbances such as voltage dips, swells, flicker, unbalance and harmonics [11-15]. The SSC is best suited to mitigate voltage dips and unbalanced grid voltages, where it can inject a voltage in series with the supply voltage to keep the voltage constant at the load. The dynamic performance of the SSC is important since the load should not be exposed to voltage dips at all in order to maintain a reliable operation.

The thesis focuses on the control of the SSC in order to improve the transient and the steady-state responses and the injection capability. The injecting capability of the SSC is not only influenced by the control algorithm but also limited by the size of the energy storage device employed. Thus, a study of the energy storage is carried out when using a capacitor bank as the energy storage device. Three power quality issues are mainly investigated in the thesis: 1) voltage dips; 2) voltage swells; 3) voltage harmonics. For each problem, a control algorithm is developed and implemented in order to ensure the successful operation of the SSC.

1.2. CONTRIBUTIONS

1.2.1. Modeling and Simulation of SSC

A simulation model incorporating the SSC, the grid and different load types is developed and implemented in PSCAD/EMTDC. The model combines both the existed component models and the user-defined models. User-defined models are designed using the FORTRAN language and they are mainly built in the controller of the SSC.

1.2.2. Double Vector Controller for Balanced Dips

A control algorithm is developed and implemented in order to mitigate the balanced voltage dips. It is based on the vector control approach and consists of two control loops. Thus, the developed control algorithm is referred to as the Double Vector Control (DVC) algorithm.

The DVC incorporates both voltage and current controllers and it has improved the transient performance of the SSC. The response time of the DVC is considerably fast. Thus, the load voltage is restored within this response time (less than 4 ms) in case of balanced voltage dips.

1.2.3. Mitigation of Unbalanced Dips

Two control strategies have been proposed and implemented in order to mitigate unbalanced voltage dips by the SSC. The first strategy uses a fast technique for separating positive and negative sequence components of the supply voltage, which are then controlled separately. Thus, two controllers are implemented for the two sequences, each based on the vector control. The second strategy is based on using only a positive sequence controller and increasing the switching frequency.

1.2.4. Software Phase Locked Loop

A software phase-locked loop (SPLL) with a PI controller has been proposed for the SSC applications. A criterion to tune the SPLL is developed and the gains of the PI controller are determined to obtain the desired transient performance and moreover filter out the harmonics of the grid voltage. The proposed SPLL plays an important role to control the flow of the electrical energy between the SSC and the grid. The proper gains of the PI controller are selected in order to obtain the correct phase information of the grid voltage for the different compensation strategies.

1.2.5. Control and Optimization of Energy Flow

Startup of SSC

During startup of the SSC, the voltage source converter (VSC) of the SSC is used to charge its energy-storage capacitor. Thus, the proposed charging procedure is called the self-charging technique. Two options have been proposed: 1) the phase angle of the load voltage is constant; 2) the magnitude of the load voltage is constant. A charging control algorithm has been proposed and implemented in each case. The factors affecting the design of the energy storage-capacitor have been investigated and a design guide for the energy-storage capacitor is given.

Minimization of Active Power Requirements

Minimization of the injected active power is realized by injecting a voltage with the proper phase shift with respect to the load current. This idea has been proposed in literature and referred to as the Phase Advance Compensation (PAC). However, in some cases, the PAC may fail to minimize the active power because of the power factor of the load. Thus, four different compensation strategies have been studied in order to ensure the minimization of the active power: 1) Voltage Difference Compensation; 2) In-Phase Compensation; 3) Phase Advance Compensation; 4) Progressive Phase Advance Compensation. The effect of the load power factor on the compensation techniques has been investigated. A control algorithm based on a combination of the four strategies is proposed taking into account the

issues: 1) minimization of the active power; 2) keeping the injected voltage within the ratings of the SSC; 3) smoothing the load voltage waveform.

1.2.6. Controller for Mitigation of Voltage Dips and Harmonics

A control algorithm to mitigate the voltage dips and harmonics has been developed and implemented experimentally. A moving average filter is employed to extract the fundamental components of the measured voltages and currents. Those are needed to control the performance of the SSC. Also, an active filtering capability is added by using the resonant filters for the 5^{th} and the 7^{th} harmonics. With this algorithm both the fundamental component and harmonics are accurately detected and controlled.

1.2.7. Mitigation of Voltage Swells and Overvoltage Protection

The possibility of employing the SSC to mitigate voltage swells/overvoltages has been investigated theoretically and experimentally. An overvoltage protection scheme has been proposed to protect the SSC online and offline. The online overvoltage protection is based on using a dc chopper with a resistor. The design of the dc resistor has been discussed.

1.2.8. Influence of Power System Events on SSC Performance

A number of power system events have been described and simulated. The simulated events are: short-circuit faults; capacitor-bank energizing; transformer energizing; load switching (induction motor start, diode rectifier start). The performance of the SSC with the DVC algorithm has been examined for each event. Moreover, the case of capacitor bank energizing was studied in more details because the capacitor bank switching results in a sustained overvoltage and a voltage transient.

1.3. THESIS OUTLINE

The thesis is composed of this introductory chapter, three chapters, and ten papers (publications) arranged as follows:

Chapter 2 presents the system description and the developments of the research work. General description of the SSC is given and different converter topologies are explored. All the developed controllers are explained and the investigated topics are discussed.

The results of the simulations and experiments are analyzed in Chapter 3.

Chapter 4 introduces the conclusions of the research work and proposes further research topics based on the achievements of this work.

Paper A presents an overview of the power electronics controllers used for power quality improvements. The definitions and examples of the power quality problems are given. The focus was given on the voltage dips, as they are the most severe problem to industrial loads.

Some solutions to mitigate the power quality problems by using the power electronics apparatus are explored.

The operational principle, configuration, design criteria, and rated power estimation of the SSC are explained in Paper B. The used control techniques are discussed aiming to compromise among them based on their suitability with the SSC requirements.

In Paper C, the principle and verification of the DVC algorithm are presented. The loop gains are determined according to the system stability analysis, carried out on the closed loop system. Experiential results on a 10 kV SSC setup are shown with different load types: static linear; dynamic linear and nonlinear loads.

Mitigation of unbalanced voltage dips is investigated in Paper D. Two control strategies to improve the dynamic performance of the SSC are presented. The first strategy uses a fast technique for separating positive and negative sequence components of the supply voltage, which are then controlled separately. The second strategy is based on using only a positive sequence controller and increasing the switching frequency.

Paper E proposes a software phase-locked loop (SPLL) with a PI controller for the SSC applications. A tuning criterion for the SPPL is developed to satisfy the frequency requirement of most of the loads. It is also discussed that by using proper selection of the gains, the SPPL behaves as a low pass filter. Thus, the harmonics in the grid voltage may not affect the steady-state performance of the SPLL.

In Paper F, the performance of the SSC due to upstream capacitor bank energizing is studied. Upstream capacitor-bank energizing leads to a transient at the terminals of the SSC followed by a sustained overvoltage. Simulation results of a PSCAD/EMTDC system model with upstream capacitor bank energizing are presented.

The control and optimization of the power flow between the SSC and the grid is described in Paper G1 and Paper G2. This part consists of two main parts: 1) startup of the SSC; 2) minimization of the active power requirements. The first part considers the charging of the energy storage by either a shunt diode rectifier or by the voltage source converter of the SSC itself. The second part proposes a control algorithm based on different compensation strategies in order to minimize the required active power and also keeps the injected voltage by the SSC within its ratings.

Paper H discusses the capability of the SSC to mitigate voltage swells. The consequences of the voltage swells on the SSC are identified. Simulations and experiments are carried out to show the ability of the SSC to mitigate voltage swells. Also an overvoltage protection scheme is proposed and designed. The overvoltage protection of the SSC is realized either online to mitigate voltage swells or offline to bypass the SSC.

In Paper I, the functionality of the SSC is extended to work as a series active filter. A control algorithm is developed and implemented to mitigate voltage dips and harmonics. The developed controller consists of three main parts: 1) extraction of the fundamental component by a moving average filter; 2) control of fundamental component by the DVC; 3) extraction and control of the voltage harmonics by the resonant filters. The operation of the SSC under distorted utility conditions is discussed and some recommendations are given.

CHAPTER

2. SYSTEM DESCRIPTION AND DEVELOPMENTS

2.1. INTRODUCTION

Power quality problems encompass a wide range of disturbances that can disrupt the operation of sensitive industrial loads and cause a loss of production. The following power quality problems have been identified in a number of standards such as [16,17] and textbooks such as [18, 19]:

- short interruptions;
- voltage dips;
- voltage swells/overvoltages;
- voltage and current transients;
- voltage and current harmonic distortion;
- voltage flicker;
- unbalance;
- power frequency variations.

A description of most of the mentioned power quality problems is given in Paper A. To many consumers of electrical energy, especially industrial consumers, voltage dips are the most important power quality disturbance in the power systems [2, 3]. The outage costs associated with poor power quality are documented and serve as an argument to study the possibility of using power conditioning equipment [4]. The effects of voltage dips, swells and flickers on end-users have been formulated in the literature such as [1-6]. Dips, depending on the severity and duration, can cause computer resets, memory loss, tripping of adjustable speed drives, loss of motor loads, and this in turn leads to serious disruption of the production process.

The fast development and continuous innovation of valves and controllers for power electronics have made it possible to solve the power quality problems by using grid-connected voltage source converters (VSCs). The VSC, connected in series with the grid as a static series compensator (SSC), also known (commercially) as the dynamic voltage

restorer (DVR), is best suited to protect the sensitive loads against the voltage dips. In principle, the SSC injects by means of three single-phase transformers three voltages in the grid, synchronized in such a way that the load voltage magnitude and phase are constant at any instant to guarantee continued operation for the load. On August 26, 1996, the world's first SSC was installed on the Duke Power distribution system to protect a sensitive textile customer from voltage dips [13].

As mentioned in Chapter 1, the control of the SSC is the main issue of the thesis. This Chapter introduces the motivation and presents the developments of the research work. A brief description of the SSC is given. The controllers to mitigate three power quality problems (dips, swells and harmonics) are derived. Also other related subjects such as the software phase-locked loop and energy flow are discussed.

2.2. VOLTAGE DIPS

A voltage dip is a decrease in the RMS voltage from 0.1 to 0.9 pu at the power frequency for duration from 0.5 cycles to 1 minute [17].

A synonym for the voltage dip is the voltage sag, which is widely used in the United States [19]. The voltage dips have the potential to disrupt the operation of the sensitive loads and cause a loss of production. It is worth to mention that the voltage dips are the main topic of the textbook [18]. The mean causes of voltage dips are the short-circuit faults in the transmission and distribution systems [19]. Also the large induction motors when starting and the transformers when being energized result in voltage dips. In some networks, switching on large loads may cause voltage dips. The voltage dips due to short-circuit faults are characterized by a dip magnitude, a dip duration, and a phase-angle jump.

The voltage dip magnitude is the retained voltage after the initiation of the dip. It can be determined by either the RMS voltage or the peak voltage over half a cycle or one cycle of the fundamental frequency. An example of a voltage dip due to short circuit fault is shown in Fig.2.1 and an example due to motor start is shown in Fig.2.2. In the case of voltage dips due to motor start, the characterization needs to be slightly different: other terms are involved such as recovery time and steady state drop (as illustrated Fig.2.2). The duration of the dip is the time at which the system voltage remains under a threshold value, for instance 90% of the pre-dip voltage.

If the dip is due to a short-circuit fault, the dip duration is mainly determined by the fault clearing time, which is affected by the speed of the protection and the speed of the circuit breakers. The phase-angle jump is a shift in the zero crossing of the instantaneous voltage. Because the system voltage is a complex quantity consisting of a magnitude and phase angle, an event like a short-circuit fault may not only affect the voltage magnitude but also its phase angle. Normally, voltage dips originated because of short-circuit faults are associated with a phase-angle jump.

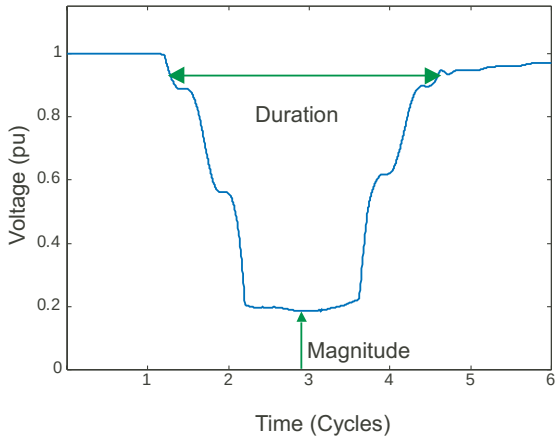


Fig.2.1. Example of voltage dip due to short-circuit fault.

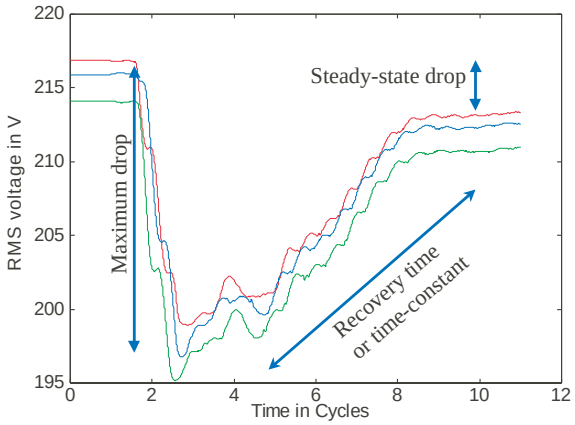


Fig.2.2. Example of voltage dip due to motor start.

2.3. STATIC SERIES COMPENSATOR

2.3.1. Operational principle of Static Series Compensator

The SSC is a power-quality device that protects highly sensitive loads, mainly industrial loads, against the common disturbances of the power system such as voltage dips and swells. Normally, the SSC is connected in series with the distribution feeder at the medium voltage levels [3]. In principle, the SSC can be installed at any voltage level, but for the low voltage applications, the SSC may be cost-ineffective compared to the uninterruptible power supply. To be able to mitigate voltage dips/swells, the SSC should be capable of generating and absorbing active and reactive power to or from the grid. Basically, the SSC is designed to dynamically inject a voltage $\underline{u}_{\text{inj}}$ into the power system as shown in Fig.2.3. Fig.2.3a shows a simplified single-phase equivalent circuit of a distribution feeder with an SSC where the supply voltage $\underline{u}_{\text{g}}$, the injected voltage $\underline{u}_{\text{inj}}$ and the load voltage $\underline{u}_{\text{L}}$ are in series. So, the SSC is considered to be an external voltage source where the amplitude, the frequency and the phase of $\underline{u}_{\text{inj}}$ can be controlled.

The purpose is to maintain the amplitude of the load voltage fixed and prevent phase jumps. A phasor diagram of a voltage dip with a phase jump is shown in Fig.2.3b. From Fig.2.3, the load voltage is deduced: $\underline{u}_{\text{L}} = \underline{u}_{\text{g}} + \underline{u}_{\text{inj}}$. If the supply voltage $\underline{u}_{\text{g}}$ has dropped due to a voltage dip or increased due to a voltage swell, the injected voltage by the SSC ($\underline{u}_{\text{inj}}$) should be controlled so that the load voltage $\underline{u}_{\text{L}}$ remains the same as during no-disturbance conditions. In Fig.2.3a, the SSC is modeled as an ideal voltage source while it is composed of many components in practice. The layout of the SSC is presented in Subsection 2.3.2 and the description of its individual components is given in Paper B.

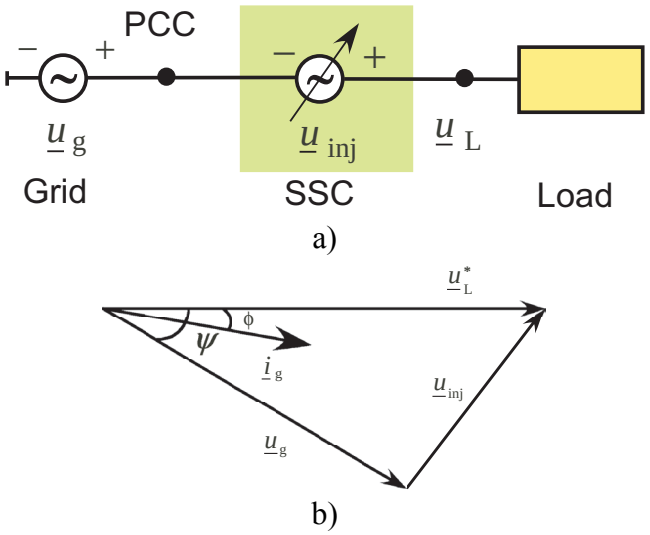


Fig.2.3. Illustrative diagram of operational principle of Static Series Compensator: a) grid, Static Series Compensator and load are in series, b) phasor diagram of voltage dip with phase angle jump.

2.3.2. Layout and Design of SSC

The SSC components (shown in Fig.2.4) are the VSC, the modulation unit, the control unit, the output filter, the injection transformer, the energy storage and the bypass switch. The measured voltages and currents are the inputs to the disturbance identification, which gives signals to the control unit to function when the measured quantities differ from the settings of the controller. The disturbance identification module triggers the start of the compensation when the supply voltage comes outside of a pre-defined range. Then the control unit generates the voltage references. The voltage references are the inputs to the modulation unit to generate the modulating signals for the valves of the VSC. The energy storage provides or absorbs the required active power to compensate the identified voltage dip/swell. Installing an output filter between the VSC and the injection transformer reduces the dv/dt effect on the windings of the injection transformer. Thus the filter converts the pulse-modulated voltage of the VSC into a sinusoidal voltage. The filtered voltage is injected into the distribution system by the series-injecting transformer. The bypass switch is normally closed to short-circuit the SSC. When the disturbance identification unit detects a voltage dip/swell, the bypass switch is opened and the SSC starts the compensation process. Because the VSC is the basic component of the SSC, it is treated in this Chapter while a detailed description of the SSC is presented in Paper B.

2.3.3. Converter Topologies for SSC

The VSC is the core element of the SSC design since the main function (generating the injected voltage) is performed through it. Different topologies of the VSC have been proposed in literature with the SSC applications. Among those are: 1) the half-bridge topology; 2) the full bridge topology; 3) the multi-level VSC.

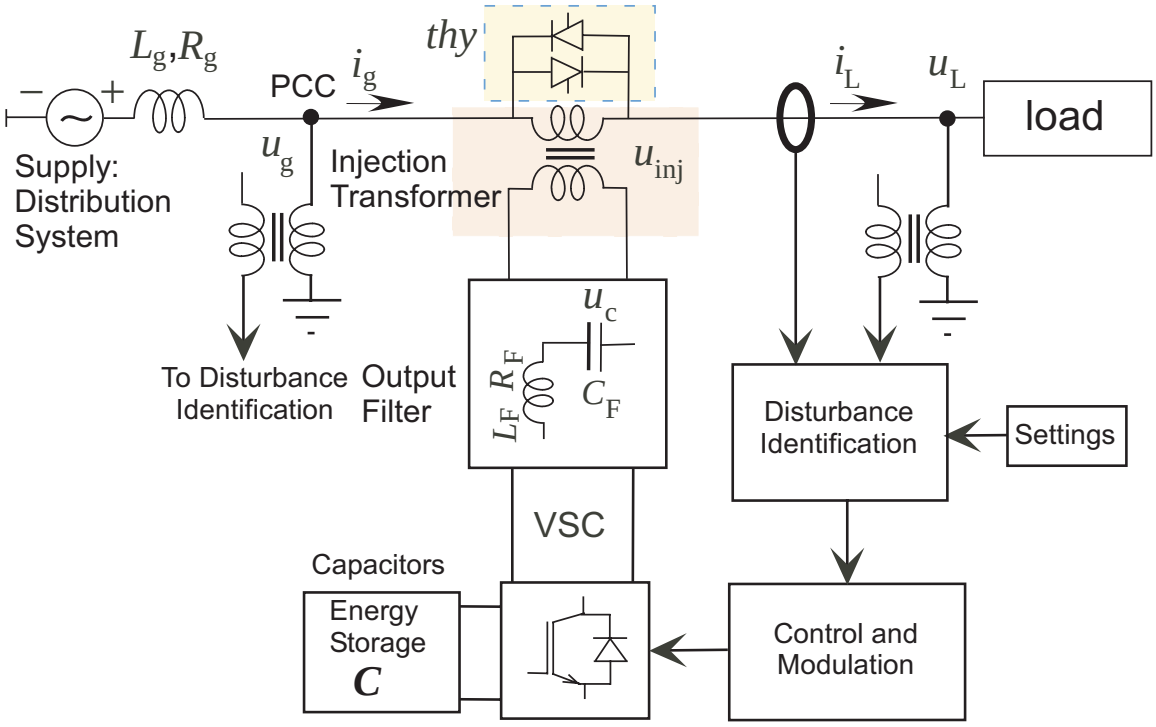


Fig.2.4. Single-line diagram of Static Series Compensator including details of VSC, LC-filter and measured signals for control.

Half Bridge Topology

The half bridge topology is the basic configuration of the VSC, which is known as the six-pulse forced-commutated converter. For simplicity, a single-phase half-bridge circuit is displayed in Fig.2.5. Each phase of the ac side, which is connected to one of the three legs of the converter, is modeled as a current source (I_g) since the SSC is connected in series with the grid. The circuit contains six valves; each valve may consist of a number of semiconductor devices in series or in parallel. For instance, the semiconductor device used in Fig.2.5 is the insulated gate bipolar transistor (IGBT), with an anti-parallel diode. The restriction is that three valves are conducting at the same time, but only one valve in each bridge-leg. Hence the phase potentials v_a, v_b, and v_c at each phase leg, referred to the mid-point of the dc-voltage supply m, are determined by the conducting states of the valves. Each phase potential is either $U_{dc}/2$ or $-U_{dc}/2$.

Full Bridge Topology

In the Full-bridge topology of the VSC, the converter has six legs (12 valves) and each phase of the ac side is connected to two of these legs. For instance, the circuit of the phase a is shown in Fig.2.6. The voltage of the phase a is the difference between the potentials v_{a1} and v_{a2}. This topology has the advantages: 1) the injected voltage is double of the injected voltage by the half-bridge topology; 2) it enables the control of the zero sequence voltage (if the injection transformer is not delta-connected). The disadvantage is that the number of valves is the double compared to the half-bridge circuit.

Multilevel VSC

The multi-level VSC has been proposed to reduce the harmonic content [20], even with a square wave modulation, because it provides the possibility to have different voltage levels. A multi-level VSC can be realized either by the neutral point clamping (as shown in Fig.2.7) or by using a multi-bridge VSC as illustrated in Fig.2.8 [21]. In the case of a three-level, VSC, neutral point clamped (NPC), the output voltage of the VSC can have one of the three values $+U_{dc}/2$, 0, and $-U_{dc}/2$. A scheme of the NPC VSC is shown in Fig.2.7. The NPC VSC converter (shown in Fig.2.7) is an alternative to the two-level converter in high power applications. Each phase can be connected to the positive dc terminal by firing S_{1n} and S_{2n} simultaneously while S_{3n} and S_{4n} are off. Firing S_{3n} and S_{4n} while S_{1n} and S_{2n} are off connects the negative dc terminal to the phase n ($n = a$, b, and c). If S_{2n} and S_{3n} are on and S_{1n} and S_{4n} are off, the phase n is connected to the midpoint of the dc side, zero potential. The three-level converter requires six extra diodes if it is compared to the two-level converter to clamp the phases to the zero potential.

2.4. CONTROL OF STATIC SERIES COMPENSATOR

The reported control techniques that have been implemented to control the injected voltage by the SSC may be classified into two main categories: 1) the scalar; 2) the vector control. By the scalar control, it is meant that only the voltage magnitude is controlled by applying the concept of phasors as in [22,23]. Techniques based on the synchronous reference frame [24-31] are referred to as vector control where the magnitude and the phase of the injected voltage are controlled. The scalar control involves the RMS calculation of the fundamental voltage [22,23], which requires at least one half period of the fundamental frequency. A block diagram (single-phase) of the scalar control is shown at Fig.2.9, where the input to the controller is the instantaneous phase voltage of the grid (u_a). Then the RMS calculations are made online to determine the RMS grid voltage (U_a) , which is then subtracted from the reference of the load voltage (U_a^*).

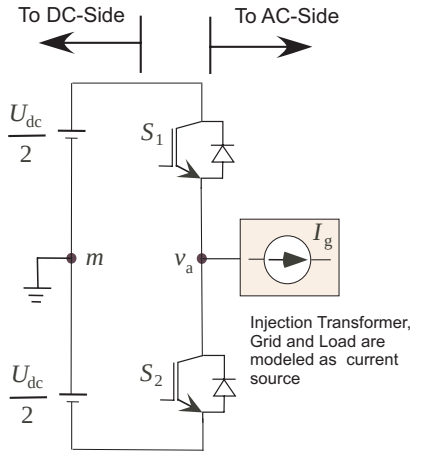


Fig.2.5. Half-bridge topology (single-phase) of voltage source converter.

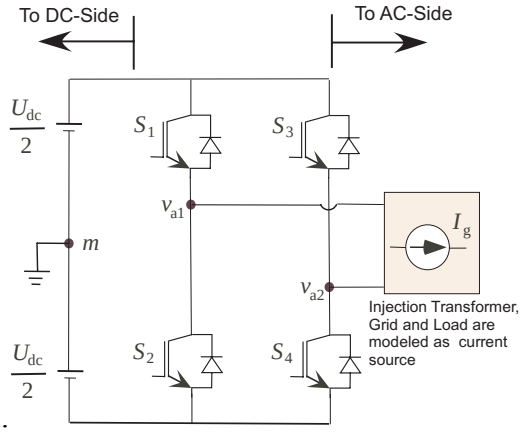


Fig.2.6. Full-bridge topology (single-phase) of voltage source converter.

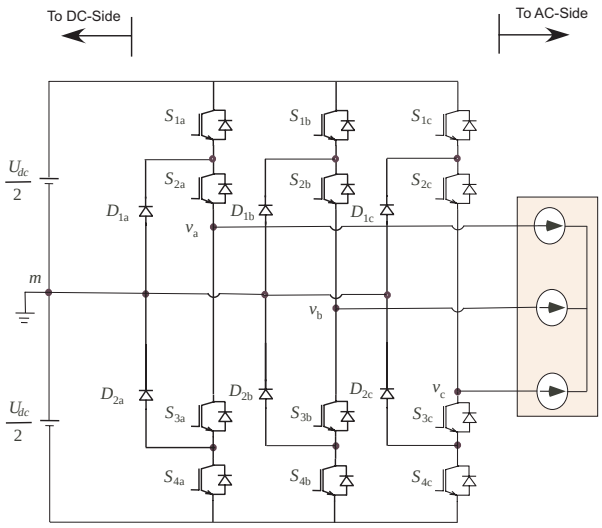


Fig.2.7. Three-level Neutral Point Clamped Voltage Source Converter.

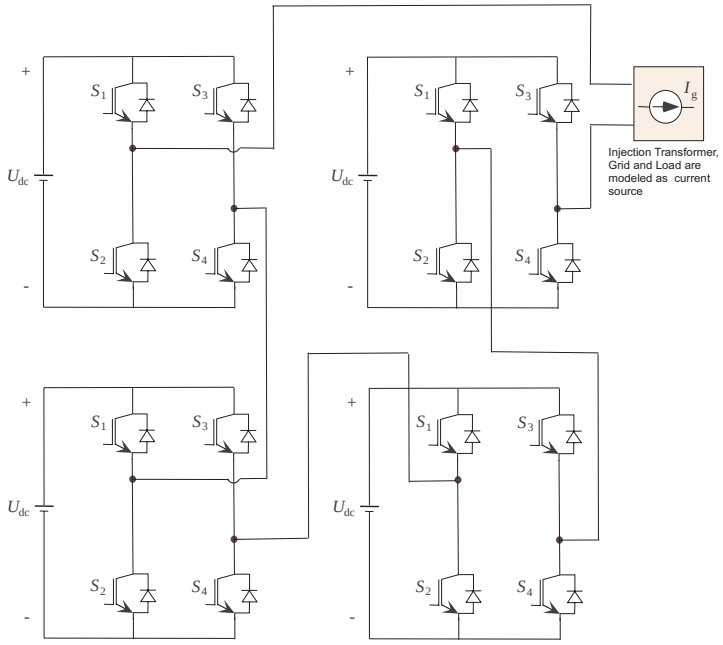


Fig.2.8. Multi-bridge Voltage Source Converter.

The amplitude reference of the injected voltage is obtained by multiplying this difference by $\sqrt{2}$ to obtain the magnitude of the injected voltage. It should be stated that the phase of the voltage reference is obtained by a phase detector, which is synchronized to the grid voltage. The scalar control works fine in the steady state, but it slows the dynamic performance of the SSC and only the fundamental voltage can be controlled unless an FFT algorithm is included and harmonic components are detected.

To improve the transient response of the SSC and control the injected active and reactive powers separately, the vector control has been implemented in a way similar to the control of variable speed drives. Both the feedforward/open-loop [24] and feedback/closed loop [25-31] techniques have been reported. A block diagram of the basic feedforward control of

the SSC is depicted at Fig.2.10. The grid voltages (u_a, u_b, u_c) are measured and transformed to the stationary reference frame ($\underline{u}^{\alpha\beta}$). A phase locked loop (PLL) is exploited to calculate the transformation angle (θ), which is required to transform the grid voltage from the stationary reference frame to the synchronous reference frame ($\underline{u}^{dq}$). Then the grid voltage is subtracted from the reference of the load voltage ($\underline{u}_L^{*dq}$) to calculate the reference of the injected voltage ($\underline{u}_{inj}^{*dq}$). A backward transformation from the synchronous reference frame to the three-phase is performed in order to obtain the reference of the injected voltage (u_{ia}^*, u_{ib}^*, u_{ic}^*) that should be generated by the VSC. The feedforward control is fast but does not guarantee the system stability and may exhibit a steady-state error.

Feedback control of the SSC has been proposed in [25] where the injected voltage by the SSC is measured and used in a single-loop [25,31] or a multi-loop [29,30] control system. A block diagram of a single-loop feedback control system is displayed in Fig.2.11. In feedback control systems (applied to the SSC), an error signal ($\Delta\underline{u}$) is generated by subtracting the actual injected voltage ($\underline{u}_{inj}$) from the reference of the injected voltage ($\underline{u}_{inj}^*$). This error signal is fed to a PI controller to obtain the reference of the voltage that should be generated by the VSC.

When designing a control algorithm for the SSC, the LC-filter, mounted at the output of the VSC as shown in Fig.2.4, is important to consider since it affects the dynamic performance of the SSC. Moreover, the LC-filter causes a voltage drop on the choke branch, which reduces the injection capability of the SSC and introduces a phase shift in the injected voltage. Such effect has been considered in [26,27,28,29]. In [26,27], a simple back calculation of the filter input voltage is applied. The algorithm proposed in [27] compensates for the steady state voltage drop due to the LC-filter but it gives poor transient performance and it is sensitive to variations of the LC-filter parameters.

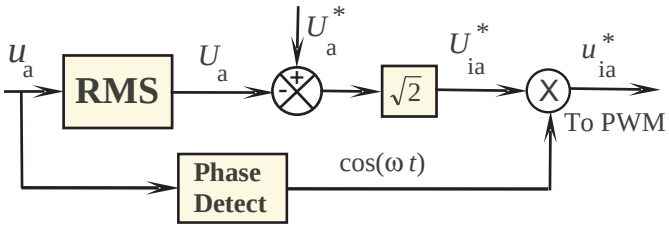


Fig.2.9. Scalar control of Static Series Compensator.

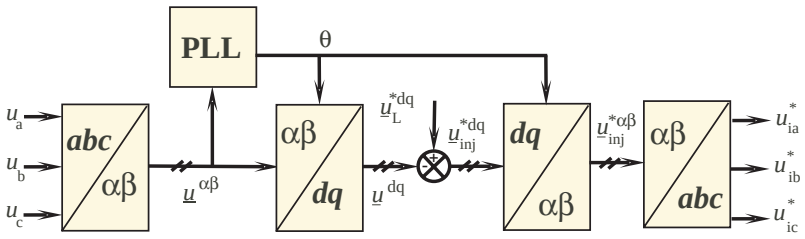


Fig.2.10. Feedforward vector control of Static Series Compensator.

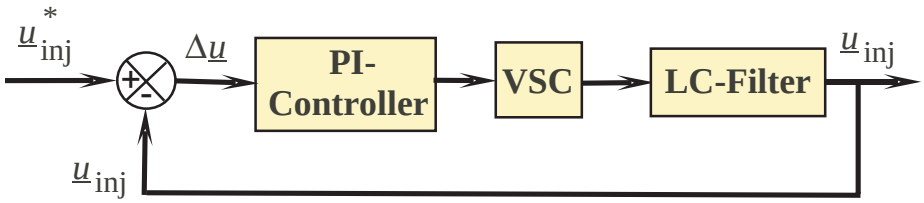


Fig.2.11. Feedback vector control of Static Series Compensator.

To overcome this problem of voltage drop across the LC-filter and improve the performance of SSC, the voltage and current controllers are incorporated as in [29] and [30]. In [29], the current control loop is formed by measuring the capacitor current and feeding it back to the controller. While in [30] the current loop is formed by the inductor current. As the inductor current should be measured for the overcurrent protection and it may help in actively damping the resonance between the LC-filter inductor and capacitor, then the inductor current is used in the current loop feedback as discussed in [30].

2.5. DOUBLE VECTOR CONTROL FOR MITIGATION OF BALANCED DIPS AND SWELLS

2.5.1. Derivation of Double Vector Controller

The dynamic performance of the SSC may be improved by controlling both the inductor current and the capacitor voltage of the LC-filter. Thus, a two-loop control algorithm is proposed in this thesis and it is referred to as Double Vector Control (DVC). To reduce the complexity of the system while deriving the DVC equations, the injecting transformer (Fig.2.4) is assumed ideal i.e., having zero magnetizing current and zero leakage inductance, with turns ratio of 1:1. Also the transformer, the grid and the load are replaced by an equivalent current source. Consequently, the injected voltage by the SSC, $\underline{u}_{inj}$ is the same as the voltage across the LC-filter capacitor $\underline{u}_c$. Hence, the capacitor voltage $\underline{u}_c$ is controlled to regulate the load voltage. The current through the LC-filter inductor is controlled by an inner control loop. To derive the controllers, the LC-filter is modeled in the stationary $\alpha\beta$-frame and transformed into the synchronous reference frame as in (2.1).

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{A}_{\mathbf{LC}}\mathbf{x}(t) + \mathbf{B}_{\mathbf{LC}}\mathbf{u}(t), \qquad \mathbf{y}(t) = \mathbf{C}_{\mathbf{LC}}\mathbf{x}(t) \tag{2.1}$$

where $\mathbf{x}(t) = \begin{pmatrix} i_d & i_q & u_{cd} & u_{cq} \end{pmatrix}^T$, $\mathbf{u}(t) = \begin{pmatrix} u_d & u_q & i_{gd} & u_{gq} \end{pmatrix}^T$,

i_d, i_q are the d- and q-components of the inductor current,
u_{cd}, u_{cq} are the d- and q-components of the injected voltage,
u_d, u_q are the d- and q-components of the VSC voltage,
i_{gd}, i_{gq} are the d- and q-components of the grid current .

The aim of the controller is to keep the load voltage constant. Thus, the SSC should inject the voltage $\underline{u}_c^{*dq}$ such that

$$\underline{u}_c^{*dq} = \underline{u}_L^{*dq} - \underline{u}_g^{dq} \tag{2.2}$$

where $\underline{u}_{\mathrm{L}}^{*\mathrm{dq}}$ is the reference voltage demanded by the load and $\underline{u}_{\mathrm{g}}^{\mathrm{dq}}$ is the grid voltage in the *dq*-frame. The missing voltage $\underline{u}_{\mathrm{c}}^{*\mathrm{dq}}$ is injected through the injecting transformer. The inputs to the controller are the grid voltages, the grid currents, the inductor currents and the capacitor voltages of the LC-filter. The proposed controller is a discrete controller and uses a sampling time of T_{s}. Hence the sampling frequency f_{s} equals to $1/T_{\mathrm{s}}$. The switching frequency f_{sw} is the same as the sampling frequency. The state-space equation of the LC-filter, (2.1) is discretized using the forward Euler method [32] and is then integrated from kT_s to $(k+1)T_s$ (one sample period), as given in (2.3).

$$\mathbf{x}(k+1) = \mathbf{A}_{\mathbf{LCD}}\mathbf{x}(k) + \mathbf{B}_{\mathbf{LCD}}\mathbf{u}(k), \qquad \mathbf{y}(k) = \mathbf{C}_{\mathbf{LCD}}\mathbf{x}(k) \tag{2.3}$$

The following assumptions are made to derive the controller:

- The grid current is constant independently of the variations in the currents and voltages of the LC-filter;
- The capacitor voltage and the inductor current change linearly during one sample;
- The controller uses a dead-beat gain; the output vector $\mathbf{y}(k)$ changes linearly and is equal to the reference output vector $\mathbf{y}^*(k)$ after one sample;
- The average values of the capacitor voltage and the inductor current over the sample period kT_s to $(k+1)T_s$ are each equal to half of the summation of the real value and the reference value at the sample *k*.

The controlled variables are the inductor current $\underline{i}^{\mathrm{dq}}$ and the capacitor voltage $\underline{u}_{\mathrm{c}}^{\mathrm{dq}}$. Based on the above assumptions and after algebraic manipulation of (2.3), the equations of the controller are obtained as:

Voltage Controller Outer Loop

$$\underline{i}^{*\mathrm{dq}} = \underline{i}_{\mathrm{g}}^{\mathrm{dq}} \pm \mathrm{j}\frac{\omega C_{\mathrm{F}}}{2}\left\{\underline{u}_{\mathrm{c}}^{*\mathrm{dq}} + \underline{u}_{\mathrm{c}}^{\mathrm{dq}}\right\} + K_{\mathrm{u}}\left\{\underline{u}_{\mathrm{c}}^{*\mathrm{dq}} - \underline{u}_{\mathrm{c}}^{\mathrm{dq}}\right\} \tag{2.4}$$

Current Controller Inner Loop

$$u^{*\mathrm{dq}} = \underline{u}_{\mathrm{c}}^{*\mathrm{dq}} + R_{\mathrm{F}}\underline{i}^{\mathrm{dq}} \pm \mathrm{j}\frac{\omega L_{\mathrm{F}}}{2}\left\{\underline{i}^{*\mathrm{dq}} + \underline{i}^{\mathrm{dq}}\right\} + K_{\mathrm{p}}\left\{\underline{i}^{*\mathrm{dq}} - \underline{i}^{\mathrm{dq}}\right\} \tag{2.5}$$

where $\underline{i}^{*\mathrm{dq}}$ and $\underline{u}^{*\mathrm{dq}}$ are the required reference currents and voltages to track the reference of the injected voltage. The gains K_{u} and K_{p} are the dead-beat gains and they are calculated in terms of the LC-filter parameters (R_{F}, L_{F}, and C_{F}) and the sampling time; $K_{\mathrm{u}} = C_{\mathrm{F}}/T_{\mathrm{s}}$, $K_{\mathrm{p}} = L_{\mathrm{F}}/T_{\mathrm{s}} + R_{\mathrm{F}}/2$. In (2.4) and (2.5), j means a 90$^{\mathrm{o}}$ phase shift which implies the cross coupling between the *d*- and the *q*-components. A block diagram of the DVC is depicted in Fig.2.12. In Fig.2.12, voltage and current limits are set in the controller in order to avoid overmodulation and limit the inductor current. To stabilize the system, the gains K_{u} and K_{p} are altered from the dead-beat gains by the factors K_{us} and K_{ps}, respectively. In other words, the gains of the two loops are given by: $K_{\mathrm{u}} = K_{\mathrm{us}}\, C_{\mathrm{F}}/T_{\mathrm{s}}$ and $K_{\mathrm{p}} = K_{\mathrm{ps}}\,(L_{\mathrm{F}}/T_{\mathrm{s}} + R_{\mathrm{F}}/2)$ Thus, selecting the values of the two factors K_{us} and K_{ps} determines the system stability.

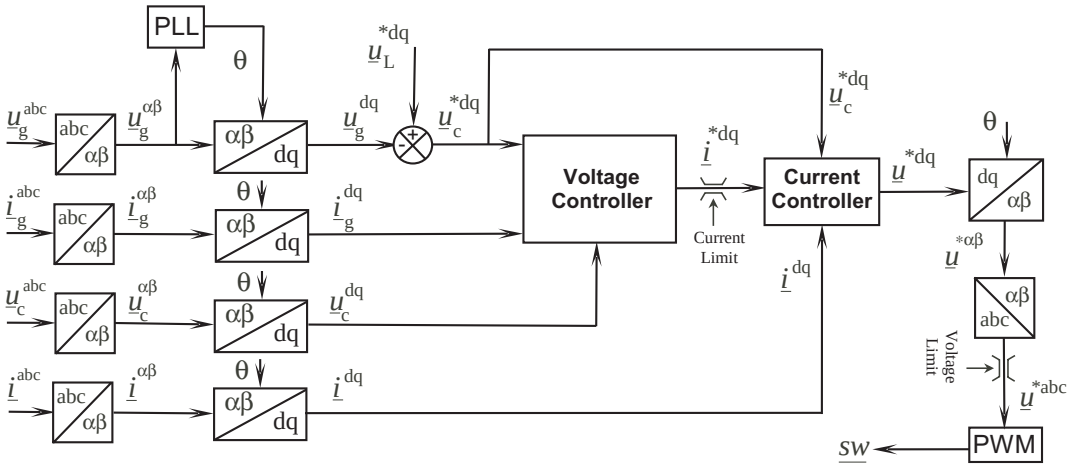


Fig.2.12. Block diagram of double vector control.

2.5.2. Stability Analysis

To perform a stability analysis for the system, the closed-loop model of the system with the proposed controller is derived. The closed loop system implies the relation between the system inputs and the controlled variables. In this case, the system inputs are the reference of the capacitor voltage $\underline{u}_c^{*dq}$ and the grid current $\underline{i}_g^{dq}$, which is considered as a disturbance. While the controlled variables are $\underline{u}_c^{dq}$ and $\underline{i}^{dq}$. A block diagram of the derived closed loop system is displayed at Fig.2.13, where G_{inv} is the transfer function of the VSC. In the derived model, G_{inv} is a linear function with a unity slop ($\underline{u}^{dq} = \underline{u}^{*dq}$) and saturates if the reference voltage is outside the range ± 1 pu (1 pu = rated dc voltage of the VSC, for a full-bridge topology of VSC). The closed-loop model is written in a state-space form as:

$$\mathbf{x}(k+1) = \mathbf{\Phi}_{\mathbf{LC}}\mathbf{x}(k) + \mathbf{\Gamma}_{\mathbf{LC}}\mathbf{u}(k) \tag{2.6}$$

Where: $\mathbf{x}(k) = \begin{pmatrix} i_d & i_q & u_{cd} & u_{cq} \end{pmatrix}^T$ and $\mathbf{u}(k) = \begin{pmatrix} u_{cd}^* & u_{cq}^* & i_{gd} & i_{gq} \end{pmatrix}^T$. The matrices $\mathbf{\Phi}_{\mathbf{LC}}$ and $\mathbf{\Gamma}_{\mathbf{LC}}$ are calculated after discretizing the filter model (2.1) and combined with the controller (2.4) and (2.5). The stability of Linear Time Invariant (LTI) systems is determined by the location of the eigenvalues of the matrix $\mathbf{\Phi}_{\mathbf{LC}}$ with respect to the unit-radius disk [32]. The LTI system is asymptotically stable if all the eigenvalues of the matrix $\mathbf{\Phi}_{\mathbf{LC}}$ are located inside the unit disk. If λ_i is an eigenvalue of the matrix $\mathbf{\Phi}_{\mathbf{LC}}$, then the system is asymptotically stable if and only if: $|\lambda_i| < 1 \; \forall \, i = 1 \, to \; 4$. The study of the system stability is equivalent to variation of the factors K_{us} and K_{ps} such that the inequality $|\lambda_i| < 1 \; \forall \, i = 1 \text{ to } 4$ is satisfied. To calculate the eigenvalues of the matrix $\mathbf{\Phi}_{\mathbf{LC}}$, the determinant of the matrix $(\lambda \mathbf{I} - \mathbf{\Phi}_{\mathbf{LC}})$ is set to zero. This yields a fourth-order equation in λ. So the complex vector function $\boldsymbol{\lambda}(K_{us}, K_{ps})$ is calculated. The stability margin is obtained by solving the equation: $|\boldsymbol{\lambda}(K_{us}, K_{ps})| = 1$. Solving this gives the values of K_{us} and K_{ps}, which make the system marginally stable.

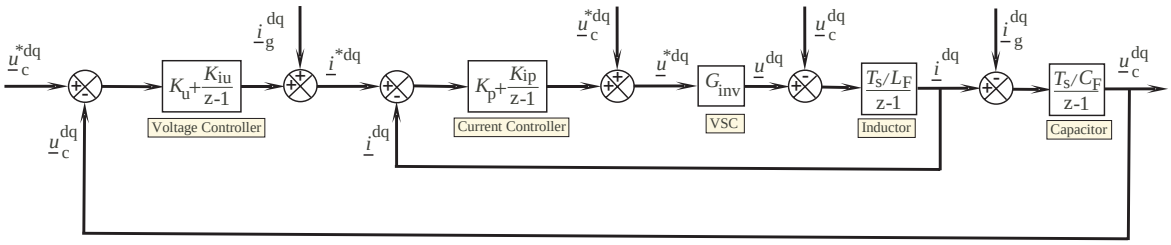


Fig.2.13. Closed-loop model of double vector controller.

Fig.2.14 shows the absolute-value contours of the eigenvalues 1 and 2, when the stabilization factors vary from 0.0 to 2.5. The plotted contours in Fig.2.14 are 0.2-most thin, 0.4, 0.6,0.8,1.0-most thick. The inclined dashed line represents the inequality $K_{us}<K_{ps}$ while the horizontal dashed line represents the inequality $K_{us}<1$. The system is marginally stable when $K_{ps}=2$, which means that the inner-loop gain can be increased up to twice the dead-beat gain. K_{us} can vary from 0.0 to 1.0 and the system is stable provided that inequality $K_{us}<K_{ps}$ is satisfied. Fig.2.15 shows the absolute-value contours of the eigenvalues 1 and 2, when the stabilization factors vary from 0.0 to 2.5. The plotted contours are 0.2-most thin, 0.4, 0.6,0.8,1.0-most thick. The eigenvalues 3 and 4 are high for low gains and decreases as the gains increase (in the plot range). The conclusion is that the system is stable when $K_{ps}<2$, which means that the inner-loop gain can be increased up to twice the dead-beat gain and K_{us} can vary from 0 to less than 1.0.

2.5.3. Frequency Response of DVC

After the derivation of the closed-loop (2.6), the system-frequency response can be investigated. The system parameters are given in Paper C. In Fig.2.16, the frequency response from the reference *d*-voltage of the capacitor u_{cd}^{*} to the *d*- and *q*-voltages of the capacitor, u_{cd} and u_{cq}, is presented. As seen from Fig.2.16, the cross coupling between u_{cd}^{*} and u_{cq} is very low for low frequencies and increases for high frequencies.

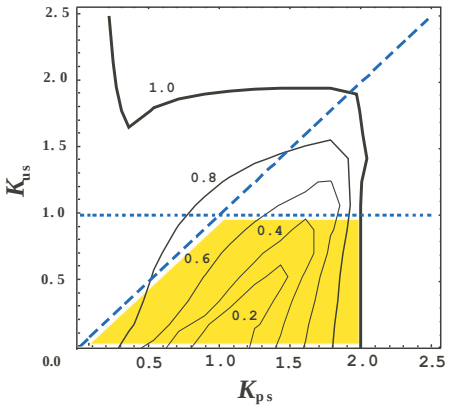


Fig.2.14. Absolute-value contours of eigenvalues 1 and 2, stability margin (most-outer, thick).

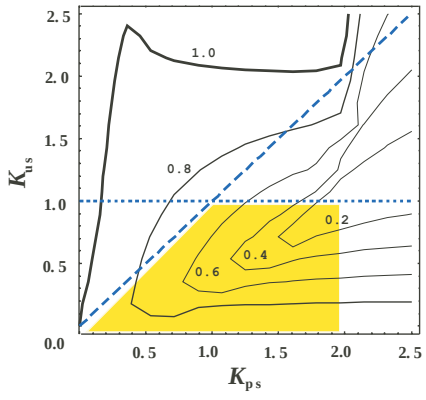


Fig.2.15. Absolute-value contours of eigenvalues 3 and 4, stability margin (most-outer, thick).

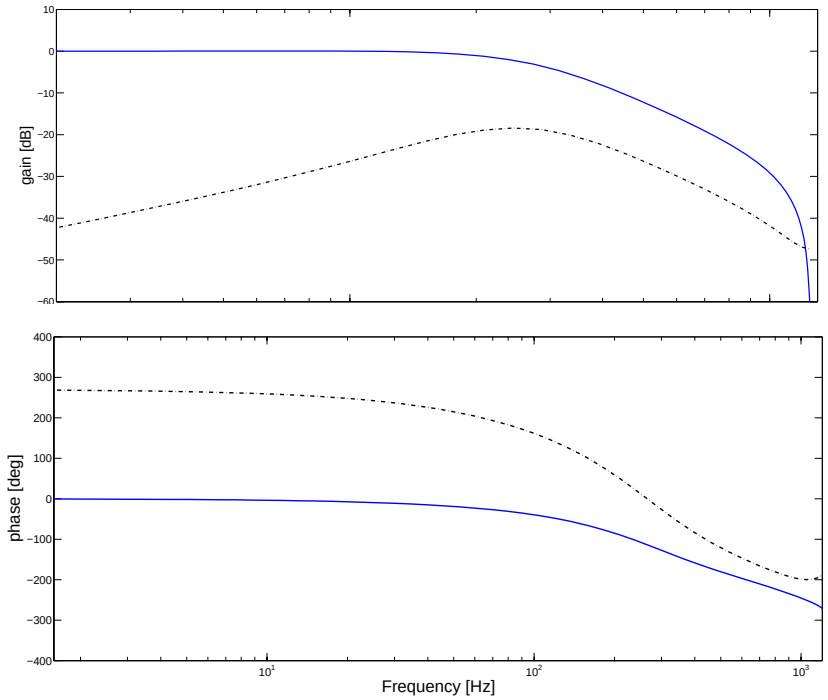


Fig.2.16. Frequency response from *d*-voltage reference to *d*- (solid) and *q*- voltage (dashed) of LC-filter capacitor.

The gain from u_{cd}^{*} to u_{cd} is equal to 0 dB, unity in the linear scale, up to 370 Hz, which implies that u_{cd} tracks u_{cd}^{*} accurately up to 370 Hz. For higher frequencies, the gain decreases and the phase shift increases. Thus, the system behaves as a low-pass filter. More details regarding the frequency response are given in [30].

2.5.4. Step Response of DVC

The step response of the SSC with the DVC is investigated by applying voltage dips and swells at the grid voltage. Voltage dips and voltage swells imply that the injected voltage by the SSC is stepped up or down to keep the load voltage constant. The results of the step response are analyzed in Chapter 3.

2.6. MODIFIED DOUBLE VECTOR CONTROLLER FOR MITIGATION OF UNBALANCED DIPS AND SWELLS

If the three-phase voltage of the grid is balanced, a transformation into the synchronous reference (*dq*) frame results in dc quantities. Hence, the SSC can use a conventional PI controller to control the injected voltage. However, if the grid or the load voltages are unbalanced, a ripple of twice the grid frequency occurs in the *dq*-frame. The positive sequence components appear as dc quantities in the *dq*-frame, which rotates positively with the grid angular frequency ω, while the negative sequence components appear as 2ω rad/s components in the *dq*-frame. Consequently, the DVC algorithm should be modified to

handle the unbalances in order to obtain a high performance controller. The proposed modifications of the DVC are:

1) detection of positive and negative sequence components of the unbalanced quantities;
2) use of two controllers: one for the positive sequence and one for the negative sequence component.

The detected positive sequence components are transformed and controlled in the *dqp*-frame, i.e. a coordinate system that rotates positively with the grid angular frequency ω, where they appear as dc quantities. While the detected negative sequence components are transformed and controlled in the *dqn*-frame, i.e. a coordinate system rotating in the negative (clockwise) direction. In the latter frame, negative sequence components appear as dc components.

2.6.1. Separation of Positive and Negative Sequence Components

In Fig.2.17, the algorithm used to extract the sequence components is shown. This detection algorithm is called the delayed signal cancellation (DSC) algorithm and has been proposed in [33]. The positive sequence of the vector $\underline{u}_g$, $\underline{u}_{gp}$ in the positively rotating *dqp*-frame is calculated as

$$\underline{u}_{gp}^{dqp}(k) = \left(\underline{u}_g^{dqp}(k) + \underline{u}_g^{dqp}(k - N_d)\right)/2 \tag{2.7}$$

where N_d is equal to $f_s/(4f_1)$ and f_1 is the grid frequency of the fundamental component. The negative sequence of the vector $\underline{u}_g$, $\underline{u}_{gn}$ in the negatively rotating *dqn*-frame is calculated as:

$$\underline{u}_{gn}^{dqn}(k) = \left(\underline{u}_g^{dqn}(k) + \underline{u}_g^{dqn}(k - N_d)\right)/2 \tag{2.8}$$

Thus, the positive sequence of the vector $\underline{u}_g$ is obtained by adding the vector $\underline{u}_g$ at the sample k to the vector $\underline{u}_g$ at the sample k-N_d, which is delayed by one fourth of the fundamental period.

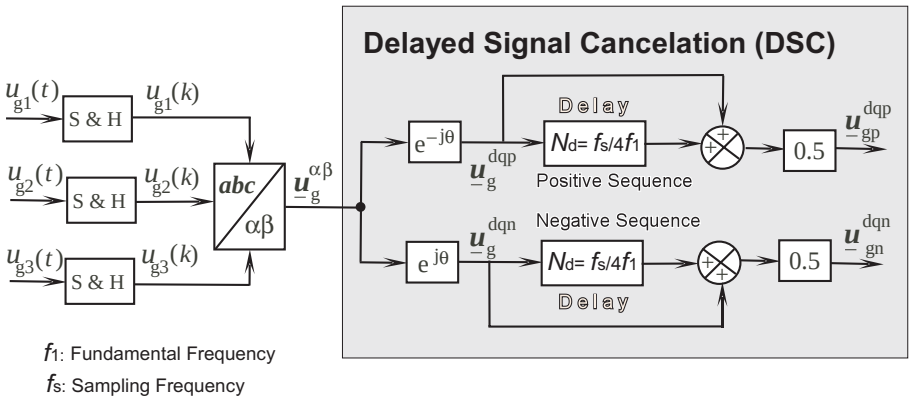


Fig.2.17. Delayed signal cancellation method to separate positive and negative sequence components.

2.6.2. Control of Positive and Negative Sequences

The equations of the positive sequence controller of the DVC are given in (2.9), where the subscript *p* denotes the positive sequence. Because the negative sequence rotates in opposite direction to the positive sequence, the cross-coupling terms between the *d*- and the *q*- components have opposite signs in the negative sequence controller. Hence, the equation of the negative sequence controller are given in (2.10), where the subscript *n* denotes the negative sequence.

Positive Sequence Controller

$$\begin{aligned} i_{\mathrm{dp}}^{*} &= i_{\mathrm{gdp}} - (\omega C_{\mathrm{F}}/2)\left(u_{\mathrm{cqp}}^{*} + u_{\mathrm{cqp}}\right) + K_{\mathrm{u}}\left(u_{\mathrm{cdp}}^{*} - u_{\mathrm{cdp}}\right) \\ i_{\mathrm{qp}}^{*} &= i_{\mathrm{gqp}} + (\omega C_{\mathrm{F}}/2)\left(u_{\mathrm{cdp}}^{*} + u_{\mathrm{cdp}}\right) + K_{\mathrm{u}}\left(u_{\mathrm{cqp}}^{*} - u_{\mathrm{cqp}}\right) \\ u_{\mathrm{dp}}^{*} &= u_{\mathrm{cdp}}^{*} + R_{\mathrm{F}} i_{\mathrm{dp}} - (\omega L_{\mathrm{F}}/2)\left(i_{\mathrm{qp}}^{*} + i_{\mathrm{qp}}\right) + K_{\mathrm{p}}\left(i_{\mathrm{dp}}^{*} - i_{\mathrm{dp}}\right) \\ u_{\mathrm{qp}}^{*} &= u_{\mathrm{cqp}}^{*} + R_{\mathrm{F}} i_{\mathrm{qp}} + (\omega L_{\mathrm{F}}/2)\left(i_{\mathrm{dp}}^{*} + i_{\mathrm{dp}}\right) + K_{\mathrm{p}}\left(i_{\mathrm{qp}}^{*} - i_{\mathrm{qp}}\right) \end{aligned} \tag{2.9}$$

Negative Sequence Controller

$$\begin{aligned} i_{\mathrm{dn}}^{*} &= i_{\mathrm{gdn}} + (\omega C_{\mathrm{F}}/2)\left(u_{\mathrm{cqn}}^{*} + u_{\mathrm{cqn}}\right) + K_{\mathrm{u}}\left(u_{\mathrm{cdn}}^{*} - u_{\mathrm{cdn}}\right) \\ i_{\mathrm{qn}}^{*} &= i_{\mathrm{gqn}} - (\omega C_{\mathrm{F}}/2)\left(u_{\mathrm{cdn}}^{*} + u_{\mathrm{cdn}}\right) + K_{\mathrm{u}}\left(u_{\mathrm{cqn}}^{*} - u_{\mathrm{cqn}}\right) \\ u_{\mathrm{dn}}^{*} &= u_{\mathrm{cdn}}^{*} + R_{\mathrm{F}} i_{\mathrm{dn}} + (\omega L_{\mathrm{F}}/2)\left(i_{\mathrm{qn}}^{*} + i_{\mathrm{qn}}\right) + K_{\mathrm{p}}\left(i_{\mathrm{dn}}^{*} - i_{\mathrm{dn}}\right) \\ u_{\mathrm{qn}}^{*} &= u_{\mathrm{cqn}}^{*} + R_{\mathrm{F}} i_{\mathrm{qn}} - (\omega L_{\mathrm{F}}/2)\left(i_{\mathrm{dn}}^{*} + i_{\mathrm{dn}}\right) + K_{\mathrm{p}}\left(i_{\mathrm{qn}}^{*} - i_{\mathrm{qn}}\right) \end{aligned} \tag{2.10}$$

After calculating the reference voltage of the VSC, the *dq*-negative and the *dq*-positive sequences are transformed to the *αβ*-frame. Then they are added, transformed into the three-phase frame and compared with the triangular wave to obtain the PWM pattern. A schematic diagram for the modified double vector controller is presented in Fig.2.18.

2.6.3. Higher Switching Frequencies

It has been shown in the previous section that adding a negative sequence controller may improve the performance of the SSC in the case of unbalanced dips. However, this has the disadvantage of a more complex controller.

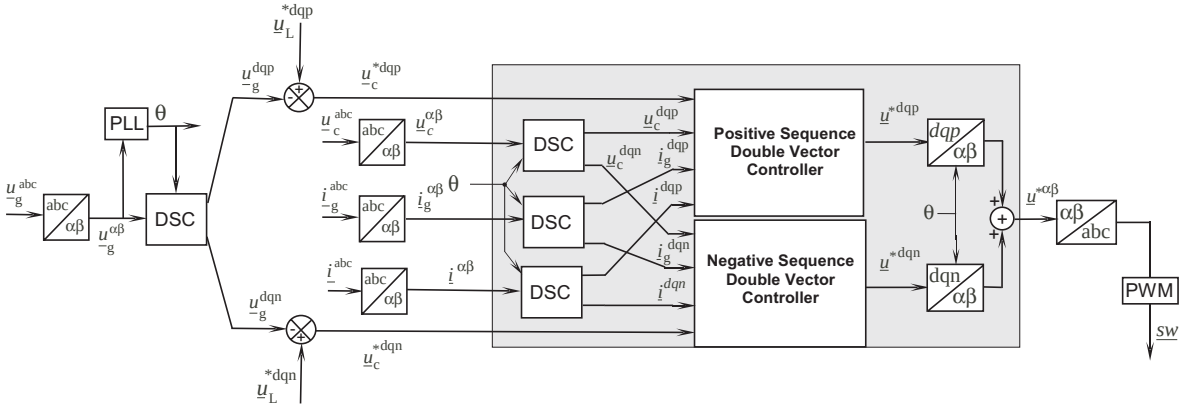


Fig.2.18. Schematic diagram of modified double vector controller.

If the switching and the sampling frequencies increase, only a positive sequence controller is needed. By increasing these frequencies, a faster controller is obtained and the current ripples are reduced. Apparently, the negative sequence components are seen (by the controller) as variations in the positive sequence and with higher switching/sampling frequency, the controller is able to track these variations. But the switching losses increase with the increase of the switching frequency. Therefore, such strategy may be suitable for low-power loads.

2.7. PHASE LOCKED LOOP FOR STATIC SERIES COMPENSATOR

The accurate phase information is crucial for most of the modern power electronics apparatus such as the SSC. Normally obtaining the phase information has been realized by the Phase-Locked Loop (PLL).

2.7.1. Hardware PLL

The hardware PLL was first described in 1923 and 1932 [34]. In 1970 it become widespread because of the development of integrated circuits. The classical configuration of the PLL is shown in Fig.2.19. Three main blocks constitute the basic PLL hardware: phase detector, low-pass filter and voltage-controlled oscillator. Normally, the phase detector is of the multiplier type whose output consists of a dc term that has the phase information of the input signal and an ac term that should be filtered by the low-pass filter. The low-pass filter can be realized either by a passive filter or an operational amplifier. The output of low pass filter is a dc signal that corresponds to the phase error between the input and output voltages. This dc signal is the input to the voltage-controlled oscillator.

2.7.2. Software PLL

With the advanced technology of microcontrollers and digital signal processors, all the functions of the classical PLL have been implemented by software. Hence the software PLL (SPLL) has become a competitive alternative to the hardware PLL. The SPLL design offers the most degrees of freedom available in any PLL design [35], because the SPLL can be tailored to perform any function, without modifying the hardware as the case of the classical PLL. Moreover, the classical PLL adds some cost to the total cost of the system. The flexibility added by the SPLL arises from the fact that the design parameters can be easily changed by modifying a few lines in the software code [36]. In single-phase systems, the zero-crossing detection has been used to estimate the phase angle of the grid voltage [37]. Despite the ease to write a zero-crossing detection algorithm, the dynamic performance of the loop is slow and a fast tracking performance is impossible. This is due to that the response can never be faster than ½ cycle of the fundamental voltage. In addition, the accuracy of zero-crossing detection is influenced by disturbances in the input signal such as harmonics. Fast tracking has been obtained by using the delayed grid voltage by one fourth of a period of the fundamental frequency together with the grid voltage itself to construct a stationery reference frame and then a synchronous reference frame [38].

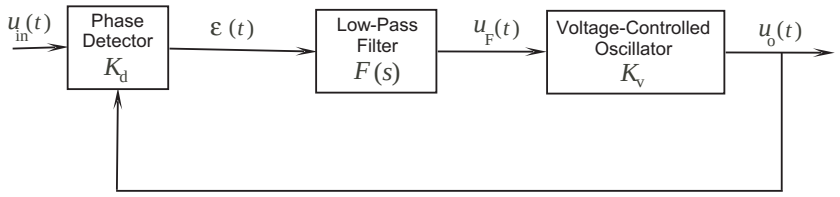


Fig.2.19. Scheme of classical hardware phase locked loop.

In three-phase systems, the SPLL has been proposed for the SSC by transforming the three-phase voltage of the grid into the synchronous reference frame [39, 40] and the performance of the SPLL is controlled by either a lead/lag filter or a PI controller. In [39] and [40], it is stated that the bandwidth of the SPLL should be low for SSC applications but it is not clear how slow the performance should be and how to tune the SPLL. Tuning the SPLL to get a desired transient performance is strongly related to the applications where the SPLL is used. In this thesis, a criterion to tune the SPLL for the SSC is discussed and the gains of the PI controller are determined to obtain the desired performance.

2.7.3. SPLL Operational Principle

A block diagram of the proposed SPLL is depicted in Fig.2.20. The operational principle of the SPLL is explained through the following steps:

- measure and sample the grid voltage $u_{g1}(t)$, $u_{g2}(t)$, $u_{g3}(t)$ to get $u_{g1}(k), u_{g2}(k), u_{g3}(k)$;
- transform the sampled grid voltage to the $\alpha\beta$-frame, obtaining $u_{g\alpha}(k)$ and $u_{g\beta}(k)$;
- normalize to the magnitude of the $\alpha\beta$-vector of the grid voltage, $\left\| \underline{u}_g^{\alpha\beta} \right\| = \sqrt{u_{g\alpha}^2 + u_{g\beta}^2}$;
- separate the positive and the negative sequence by using the delayed signal cancellation technique (DSC) to obtain the positive sequence of the grid voltage in the positive $\alpha\beta$-frame, $\alpha\beta p$-frame. The DSC was briefly explained in Section 2.6;
- transform from $\alpha\beta p$-frame to positive dq-frame, dqp-frame to get the positive sequence components of the grid voltage, u_{gdp} and u_{gqp};
- the d-component u_{gdp} is the input to the PI controller of the SPLL to calculate the change in the angular frequency of the grid voltage, $\Delta\omega$;

$$\Delta\omega = \left(K_{\text{P-PLL}} + K_{\text{I-PLL}}/(z-1)\right) u_{gdp} \tag{2.11}$$

where $K_{\text{P-PLL}}$ and $K_{\text{I-PLL}}$ are the proportional and the integral gains of the PI controller. Here it is worth to state that an integration part is necessary especially in the case of low-inertia grids where the grid frequency can deviate around the nominal frequency.

- add the reference angular frequency, $\omega^* = 2\pi f^*$, where f^* is the reference frequency of the grid, 50 or 60 Hz.

$$\omega = \Delta\omega + \omega^* \tag{2.12}$$

- multiply ω by the sampling time T_s to obtain the increment of the phase angle $\Delta\theta(k)$;

$$\Delta\theta = T_s \omega \tag{2.13}$$

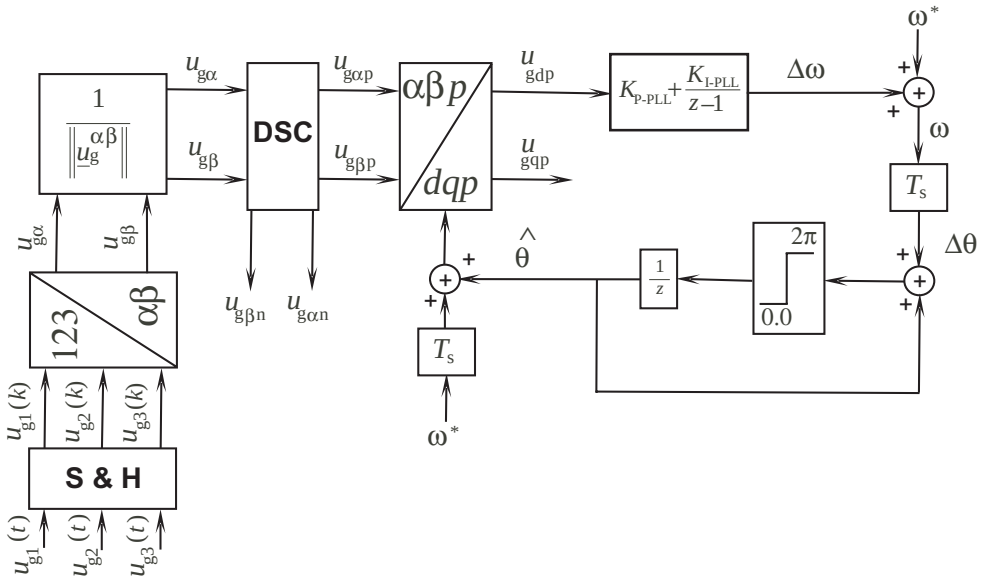


Fig.2.20. Block diagram of proposed software phase locked loop.

- by integrating the increment $\Delta\theta$, the estimated phase angle of the grid voltage $\hat{\theta}$ is obtained;

$$\hat{\theta} = z\Delta\theta/(z-1) \tag{2.14}$$

- the estimated angle $\hat{\theta}$ is used to calculate the new *d*-component u_{gdp} until u_{gdp} becomes zero and u_{gqp} becomes constant and the difference between the actual phase angle of the grid voltage and the estimated angle becomes zero.

2.7.4. SPLL Modeling

A model of the SPLL is obtained to be able to tune it. The grid voltage, after sampling is assumed as:

$$\begin{aligned} u_1 &= \sqrt{2}U\cos(\theta) \\ u_2 &= \sqrt{2}U\cos(\theta - 2\pi/3) \\ u_3 &= \sqrt{2}U\cos(\theta + 2\pi/3) \end{aligned} \tag{2.15}$$

where U is the RMS of the grid voltage (phase to ground). The $\alpha\beta$-components of the grid voltage are calculated as

$$\begin{pmatrix} u_{g\alpha} \\ u_{g\beta} \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix}\begin{pmatrix} u_{g1} \\ u_{g2} \\ u_{g3} \end{pmatrix} \tag{2.16}$$

After normalization to $\left\|\underline{u_g^{\alpha\beta}}\right\|$ and algebraic manipulation of (2.16), the $\alpha\beta$- components of the grid voltage become:

$$\begin{pmatrix} u_{g\alpha} \\ u_{g\beta} \end{pmatrix} = \begin{pmatrix} \cos(\theta) \\ \sin(\theta) \end{pmatrix} \tag{2.17}$$

Then the positive sequence is extracted to obtain $u_{g\alpha p}$ and $u_{g\beta p}$. The *dqp*- components of the grid voltage are calculated as:

$$\begin{pmatrix} u_{gdp} \\ u_{gqp} \end{pmatrix} = \begin{pmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{pmatrix} \begin{pmatrix} u_{g\alpha p} \\ u_{g\beta p} \end{pmatrix} \tag{2.18}$$

where $\hat{\theta}$ is the estimated angle by the SPLL. It is worth to mention that as the synchronization is made with respect to a virtual flux vector, $-\pi/2$ is added to the estimated angle. After algebraic manipulation, the *dqp*- components of the grid voltage are obtained:

$$\begin{pmatrix} u_{gdp} \\ u_{gqp} \end{pmatrix} = \begin{pmatrix} -\sin(\theta - \hat{\theta}) \\ \cos(\theta - \hat{\theta}) \end{pmatrix} \tag{2.19}$$

When the difference $\theta - \hat{\theta}$ approaches zero the *dqp*-components become

$$u_{gdp} \cong 0, \qquad u_{gqp} \cong 1 \tag{2.20}$$

Equation (2.19) represents a nonlinear relation where the *d*-component of the grid voltage u_{gdp} is a function of the sine of the difference between the actual and the estimated angles. To simplify the analysis, a linearized model is obtained.

2.7.5. SPLL Linearized Model

A linearized model of the SPLL can be obtained if the difference between the actual and the estimated phase angles is considered small. This assumption implies that

$$\sin(\theta - \hat{\theta}) \approx \theta - \hat{\theta} \tag{2.21}$$

Consequently, u_{gdp} can be approximated:

$$u_{gdp} \approx \theta - \hat{\theta} = e \tag{2.22}$$

where *e* is the phase error between the actual phase and the estimated one. Thus, the block diagram of the SPLL (Fig.2.20) is redrawn as shown in Fig.2.21 and the forward transfer function becomes:

$$G_F(z) = \left(K_{P\text{-}PLL} T_s \left(z + \left(K_{I\text{-}PLL} / K_{P\text{-}PLL}\right) - 1\right)\right) / (z-1)^2 \tag{2.23}$$

The closed-loop transfer function of the SPLL is

$$G_{SPLL}(z) = \frac{\hat{\theta}(z)}{\theta(z)} = \frac{K_{P\text{-}PLL} T_s \left(z + K_{I\text{-}PLL} / K_{P\text{-}PLL} - 1\right)}{z^2 + (K_{P\text{-}PLL} T_s - 2) z + T_s (K_{I\text{-}PLL} - K_{P\text{-}PLL}) + 1} \tag{2.24}$$

By (2.24), the stability margin of the SPLL is checked.

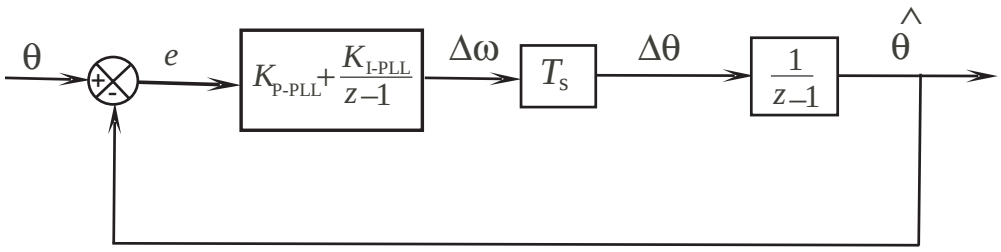


Fig.2.21. Simplified model of software phase locked loop assuming that it works within reference frequency range.

2.7.6. Stability of SPLL

The stability conditions of the SPLL can be obtained by investigating the SPLL transfer function in (2.24). The closed system given by (2.24) has a zero at $z=1-\left(K_{\text{I-PLL}}/K_{\text{P-PLL}}\right)$ and two poles at $z=\frac{1}{2}\left(2-K_{\text{P-PLL}}T_s\pm\sqrt{K^2_{\text{P-PLL}}T_s^2-4K_{\text{I-PLL}}T_s}\right)$. Doing the Jury's stability test [32] yields the following conditions to keep the system stable:

$$K_{\text{P-PLL}}>0.0\,,K_{\text{P-PLL}}<\frac{K_{\text{I-PLL}}}{2}+\frac{2}{T_s}\ \text{and}\ K_{\text{I-PLL}}<K_{\text{P-PLL}} \tag{2.25}$$

If the integral gain is taken in the form $K_{\text{I-PLL}}=K_{\text{P-PLL}}T_s/T_i$, where T_i is the integration time, then T_i should be higher than the sampling time T_s to keep the system stable. If the integral gain is assumed very small, $K_{\text{I-PLL}}\approx 0.0$, the closed loop system of the SPLL is further simplified to a first order system having the transfer function given by (2.26), which clearly shows that $K_{\text{P-PLL}}<2/T_s$ to keep system stability.

$$G_{\text{SPLL}}(z)=\frac{\hat{\theta}(z)}{\theta(z)}=\frac{K_{\text{P-PLL}}T_s}{z+K_{\text{P-PLL}}T_s-1} \tag{2.26}$$

2.8. TUNING SPLL

2.8.1. Tuning First-order SPLL

Tuning the SPLL to get a desired transient performance is strongly related to the applications where the SPLL is used. In this Section, a criterion to tune the SPLL for SSC applications is specified. The gains of the PI controller are determined to obtain the desired performance.

As the SSC is used to protect sensitive loads against voltage dips and normally voltage dips are associated with phase angle jumps, an extremely fast SPLL will result in a phase angle jump of the load voltage. Some loads are disturbed by the phase-angle jump and thus an extremely fast SPLL is not preferred. Moreover, an extremely fast SPLL implies that the

proportional gain can be high and the stability limit could be reached. Extremely slow SPLL would cope with the phase angle jump of the load voltage but it does not suit the control of the SSC. This is true because the SPLL will calculate a wrong phase angle during the voltage dip if the response time of the SPLL is set much longer than the dip duration. In this case, the phase angle of the load voltage can be kept constant but the SPLL is not locked to the grid during the voltage dip. Thus, the SPLL should be tuned such that most of the loads will not be disturbed during a voltage dip.

Interpreting the European Standard EN50160, most of the loads perform satisfactorily if the deviation of the grid frequency is kept within ±1 Hz [17]. At the same context, a gradual change in the phase angle of the grid voltage with respect to time is sensed as a change in the grid frequency ($\omega = d\theta / dt$). Hence a phase-angle jump of the grid voltage should be softened at the load terminals and the load should not sense a frequency deviation out of the range ±1 Hz. This concludes that most of the loads will not be disturbed by the phase angle jump of the grid voltage if $d\theta / dt$ (or alternatively $\Delta\theta / \Delta t$) is kept within ±1 Hz. One Hz is equivalent to a change of the phase angle by 2π radian (360^o) every second. Consequently,

$$\Delta\theta / \Delta t = 2\pi \tag{2.27}$$

From (2.27), the required time by the SPLL to reach its steady state can be obtained as a function of the phase angle jump $\Delta\theta$:

$$\Delta t = \Delta\theta / 2\pi \tag{2.28}$$

From the basic control theory, the settling time of a first order system is approximately five times the time constant of the system [32]. Thus, the time constant of the simplified SPLL is calculated as:

$$\tau_{\text{SPLL}} = (1/5)\Delta t = \Delta\theta / 10\pi \tag{2.29}$$

To be able to use this criterion, the discrete transfer function of the simplified model of the SPLL, $G_{\text{SPLL}}(z)$ in (2.26) is transformed to the continuous time using the bilinear transformation: $z = (1 + sT_s)/(1 - sT_s)$. The continuous system is obtained as

$$G_{\text{SPLL}}(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{1 - sT_s/2}{s\left(\left(1 - K_{\text{P-PLL}}T_s/2\right)/K_{\text{P-PLL}}\right) + 1} \tag{2.30}$$

The time constant of the system in (2.30) is

$$\tau_{\text{SPLL}} = \left(1 - K_{\text{P-PLL}}T_s/2\right)/K_{\text{P-PLL}} \tag{2.31}$$

Comparing (2.29) and (2.31) gives the proportional gain that satisfies the identity (2.28).

$$K_{\text{P-PLL}} = \frac{2}{\left(\Delta\theta / 5\pi\right) + T_s} \tag{2.32}$$

It can be noticed from (2.32) that the proportional gain of the PI controller depends on the sampling time as well as the maximum expected phase angle jump.

It has been shown that voltage dips in the transmission systems result in a phase-angle jump of ± 5°, while up to –60° phase jump can occur due to faults in the distribution systems [18]. Considering the maximum phase angle jump that can occur, -60° (-$\pi/3$), the proportional gain in this case is obtained by substituting $\Delta\theta$ by $\pi/3$ in (2.32), which yields

$$K_{\text{P-PLL}} = 30/(1+15T_s) \tag{2.33}$$

2.8.2. Tuning Second Order SPLL

To tune the second order system of the SPLL represented in (2.26), the pole placement technique can be used. The poles of the SPLL transfer function in (2.26) are the zeros of the polynomial:

$$P(z) = z^2 + (K_{\text{P-PLL}}T_s - 2)z + T_s(K_{\text{I-PLL}} - K_{\text{P-PLL}}) + 1 \tag{2.34}$$

Assuming that the poles of $G_{\text{SPLL}}(z)$ have the general form:

$$z = \rho e^{\pm j\vartheta} \tag{2.35}$$

then the general form of the denominator polynomial of $G_{\text{SPLL}}(z)$ is $(z-\rho e^{j\vartheta})(z-\rho e^{-j\vartheta})$;

$$P_g(z) = z^2 - (2\rho\cos(\vartheta))z + \rho^2 \tag{2.36}$$

Comparing (2.34) and (2.36) yields

$$K_{\text{P-PLL}} = \frac{2}{T_s}(1-\rho\cos(\vartheta)),\ K_{\text{I-PLL}} = K_{\text{P-PLL}} + \frac{1}{T_s}(\rho^2 - 1) \tag{2.37}$$

Selecting the values of ρ and ϑ determines the poles of the system and hence its performance. The performance of the SPLL should be slow and not exhibit an overshoot to avoid power oscillations between the SCC and the grid. Thus, the poles are preferably located close to the real axis. Consequently the angle ϑ can be assumed zero, which yields

$$K_{\text{P-PLL}} = (2/T_s)(1-\rho),\ K_{\text{I-PLL}} = K_{\text{P-PLL}}^2 T_s/4 \tag{2.38}$$

If $\rho = 0.0$, the SPLL performs as a deadbeat controller and the calculated phase angle is obtained after two sampling periods. As ρ approaches unity, the performance gets slower. To satisfy that the settling time of the SPLL should be 1/6 second (for a phase jump of 60°) to obtain the desired performance for most of the loads, the poles should be placed close to unity in the real axis of the *z* plane but the stability limit should not be reached.

2.9. CONTROL AND OPTIMIZATION OF ENERGY FLOW BETWEEN STATIC SERIES COMPENSATOR AND GRID

2.9.1. Control of active and reactive powers

It has been shown that by using the vector control, the active and reactive powers can be controlled independently [41]. The authors of [41] gave the formula of active and reactive power (for the shunt-connected VSC) in the stationary reference ($\alpha\beta$) frame as:

$$\begin{pmatrix} p_{\text{inj}} \\ q_{\text{inj}} \end{pmatrix} = \begin{pmatrix} u_\alpha & u_\beta \\ -u_\beta & u_\alpha \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \tag{2.39}$$

For series-connected VSC, the expression in (2.39) changes to:

$$\begin{pmatrix} p_{\text{inj}} \\ q_{\text{inj}} \end{pmatrix} = \begin{pmatrix} i_\alpha & i_\beta \\ -i_\beta & i_\alpha \end{pmatrix} \begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} \tag{2.40}$$

In the synchronous reference frame, the active and reactive power are estimated as:

$$\begin{pmatrix} p_{\text{inj}} \\ q_{\text{inj}} \end{pmatrix} = \begin{pmatrix} i_{\text{q}} & i_{\text{d}} \\ -i_{\text{d}} & i_{\text{q}} \end{pmatrix} \begin{pmatrix} u_{\text{q}} \\ u_{\text{d}} \end{pmatrix} \tag{2.41}$$

For a unity power factor operation i.e. $i_{\text{d}} = 0$, thus active and reactive power expressions are reduced to:

$$p_{\text{inj}} = u_{\text{q}} i_{\text{q}} \tag{2.42}$$

$$q_{\text{inj}} = u_{\text{d}} i_{\text{q}} \tag{2.43}$$

The voltage components u_{q} and u_{d} represent the components of the injected voltage u_{cq} and u_{cd} when applying (2.42) and (2.43) to the case of the SSC. Also, the current components i_{q} and i_{d} represent the components of load/grid current i_{gq} and i_{gd}. For a fast tracking control, the actual voltage component $u_{\text{cq}}/u_{\text{cd}}$ can be approximated to its reference $u^*_{\text{cq}}/u^*_{\text{cd}}$. Hence (2.42) and (2.43) become:

$$p_{\text{inj}} = u^*_{\text{cq}} i_{\text{gq}} \tag{2.44}$$

$$q_{\text{inj}} = u^*_{\text{cd}} i_{\text{gq}} \tag{2.45}$$

From (2.44) and (2.45), it is clear that the active and the reactive powers can be controlled separately by controlling u^*_{cq} and u^*_{cd}, respectively. Consequently, the amount and the direction of the active power flow between the SSC and the grid are controlled by the value and the sign of u^*_{cq}. Also, the amount and the direction of the reactive active power flow between the SSC and the grid are controlled by the value and the sign of u^*_{cd}.

2.9.2. Charging Control of Energy Storage

Operation Modes of SSC

Before discussing the charging control algorithm of the Energy Storage Capacitor (ESC), the operation of the SSC is described and divided into four modes, according to the state of the valves of the VSC, the thyristors *thy* (shown in Fig.2.22) and the switching pattern. These modes are: Null, Self-charging, Blocking, and Compensating modes.

Null mode:

In the null mode, all the valves (as *S* in Fig.2.22) are off and the VSC behaves as a diode rectifier. The ESC is charged if $i_{\text{g}} \neq 0$ until another mode is activated.

Self-charging mode:
If the diode rectifier is not used to charge the ESC, the self-charging mode can be used.
Blocking mode:
In the blocking mode, the dc voltage is blocked by turning on the upper three valves and turning off the lower three valves of the converter legs, or vice versa. The thyristors *thy* are turned on to bypass the SSC.
Compensating mode:
When the SSC detects a voltage dip/swell, the compensating mode is activated. The reference of the injected voltages is calculated by the DVC. The bypass thyristors *thy* are turned off and the SSC starts to mitigate the dip/swell.

Self-charging Technique

By the self-charging technique, it is meant that the VSC of the SSC itself is used to charge the ESC. Doing so implies that some active power is drawn from the grid into the VSC. When the grid voltage is 100 % of its nominal value, the control algorithm of the SSC is adapted to control the load voltage such that the required active power can be extracted from the grid and fed into the ESC. An illustrative diagram is given in Fig.2.22, where the direction of the VSC current is into the VSC instead of out the VSC, as in the case of voltage dip compensation. The idea with the self-charging mode is to inject a small voltage component and thus draw a small active power from the grid to charge the ESC. The injected voltage should be independent of the voltage level of the ESC. This is achieved by generating the proper reference to the pulse width modulator. To draw an active power from the grid, the injected voltage must have a sign such that during the charging of the ESC, the active component of the load voltage (u_{Lq}) will decrease.

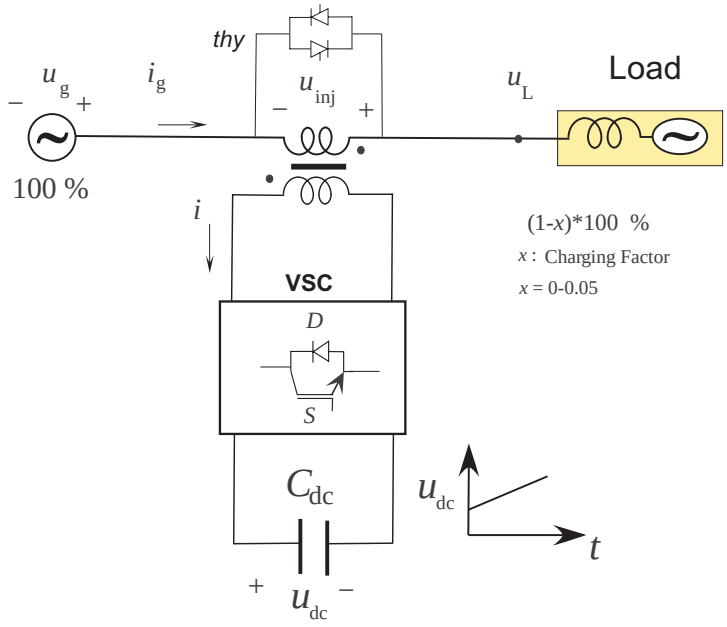


Fig.2.22. Illustrative diagram to explain self-charging technique.

Nevertheless, this decrease should be limited and made so that it does not cause problems to the load. In order to charge the ESC and not disturb the load during the charging process and at the same time to employ the VSC of the SSC, the self-charging is realized with two alternatives: 1) the phase angle of the load voltage is kept constant; 2) the phase angle of the load voltage is allowed to jump during the charging of the ESC.

Constant phase-angle technique

To ensure a constant phase of the load voltage, the *d*- and the *q*-components of the injected voltage are set such that:

$$u_{\mathrm{cd}}^{*} + \mathrm{j}u_{\mathrm{cq}}^{*} = -x\left(u_{\mathrm{Ld}}^{*} + \mathrm{j}u_{\mathrm{Lq}}^{*}\right) \tag{2.46}$$

where u_{cd}^{*}, u_{cq}^{*}, u_{Ld}^{*}, and u_{Lq}^{*} are the *d*- and the *q*- references of the injected voltage and the load voltage, respectively. In (2.46), x is the charging factor and it can take a value in the range 0.01 to 0.05 to meet the requirements that the load voltage drop during the charging should be accepted. This means that the load will sense a voltage dip of 95-99% during the self-charging mode, without phase angle jump. The physical meaning of the charging factor x is explained via the example: If the stored energy in the ESC is used to compensate for a 50 % voltage dip with duration of 1 s, the charging of the capacitor will last 50 s if the allowed voltage drop of the load is 1 %. If the allowed voltage drop of the load is 5 %, the charging will last 10 s.

Phase-angle jump technique

To keep the load voltage magnitude constant, a phase-angle jump is allowed in the phase of the load voltage. In this case, active power is drawn from the grid while the VSC injects reactive power. Thus, the magnitude of the load voltage is constant at any time. This is achieved by setting the reference for the VSC to be as in (2.47).

$$\begin{aligned} u_{\mathrm{cq}}^{*} &= -x \\ u_{\mathrm{cd}}^{*} &= \sqrt{(u_{\mathrm{L}}^{*\mathrm{dq}})^{2} - (u_{\mathrm{L}}^{*\mathrm{dq}} - x)^{2}} \end{aligned} \tag{2.47}$$

where $u_{\mathrm{L}}^{*\mathrm{dq}} = \sqrt{(u_{\mathrm{Ld}}^{*})^{2} + (u_{\mathrm{Lq}}^{*})^{2}}$ is the magnitude of the load voltage in the *dq*-reference frame. But before the self-charging mode can be used, the dc voltage must reach a desired value in order to compensate for the injected voltage calculated by (2.46) or (2.47) and the voltage drop across the LC-filter without having overmodulation. For instance, the dc voltage has to reach 0.2 pu before the self-charging mode can be applied. This 0.2 pu voltage is realized by applying the null mode. To conclude, the self-charging technique can be summarized as follows, where a state flag "BLOCK" is used to distinguish the four operational modes:

1. The VSC is set to the null mode until the dc-voltage reaches 20 % of the stand-by value (BLOCK = 0).
2. The self-charging mode is activated until the dc-voltage reaches its stand-by value (BLOCK = 3).

3. When the desired dc voltage is reached, the blocking state is initiated (BLOCK = 1).
4. In the case of voltage dips in the grid, the injected voltage is determined according to the DVC algorithm (BLOCK = 2) and the thyristors *thy* are switched off.

2.9.3. Compensation Strategies

To restore the load voltage to its pre-dip conditions, the SSC should inject some amount of active power. Normally, this active power is obtained from the ESC. The size of the ESC is a limiting factor for the SSC to be able to compensate for deep and long-duration voltage dips. If the amount of the injected active power can be minimized, the cost and volume of the ESC is reduced. On the other hand, the minimization of active power should not affect the waveform of the restored load voltage. The needed amount of active power depends on many factors such as: 1) voltage dip characteristics (magnitude, duration and phase jump); 2) the load characteristics such as the rated power and the power factor. Because the voltage dips are stochastic, the SSC calculates the missing voltage (amplitude and angle) and injects this voltage in order to maintain the load voltage constant. Of course, this is achieved within the ratings of the SSC. If the missing voltage amplitude is beyond the rated voltage of the SSC, the SSC injects the maximum voltage but in this case the load voltage will not be restored to 1 pu. Thus, the injected voltage magnitude should not exceed the SSC rated voltage. Consequently, three main factors should be taken into account: 1) minimization of active power; 2) keeping the injected voltage within the rating of the SSC; 3) smoothing the waveform of the load voltage when applying a phase angle jump. In order to optimize the performance of the SSC, four different compensation strategies are studied: 1) Voltage Difference Compensation; 2) In-Phase Compensation; 3) Phase Advance Compensation; 4) Progressive Phase Advance Compensation.

Voltage Difference Compensation

By the Voltage Difference Compensation (VDC), it is meant that the injected voltage vector $\underline{u}_c$ is estimated by subtracting the grid voltage vector $\underline{u}_g$ from the reference of the load voltage vector $\underline{u}_L^*$ as depicted in Fig.2.23. Consequently, the load voltage is restored to its pre-dip magnitude and its phase is unchanged. From the power quality point of view, this is the best compensation strategy. In Fig.2.23, the load current vector is taken as the reference vector, which coincides with the *q*-axis. ϕ is the angle of the load voltage vector and also the power factor angle. δ is the angle of the grid voltage vector, or alternatively the phase angle jump during the dip. With these arrangements, the *q*-component of the injected voltage represents the injected amount of active power in pu. The *d*- and *q*-components of the injected voltage are calculated as:

$$\begin{aligned} u_{cd} &= -\left\|\underline{u}_L^*\right\|\sin(\phi) + \left\|\underline{u}_g\right\|\sin(\delta) \\ u_{cq} &= \left\|\underline{u}_L^*\right\|\cos(\phi) - \left\|\underline{u}_g\right\|\cos(\delta) \\ \left\|\underline{u}_c\right\| &= \sqrt{u_{cd}^2 + u_{cq}^2} = \sqrt{\left\|\underline{u}_L^{*\,2}\right\| + \left\|\underline{u}_g{}^2\right\| - 2\left\|\underline{u}_L^*\right\|\left\|\underline{u}_g\right\|\cos(\phi - \delta)} \end{aligned} \tag{2.48}$$

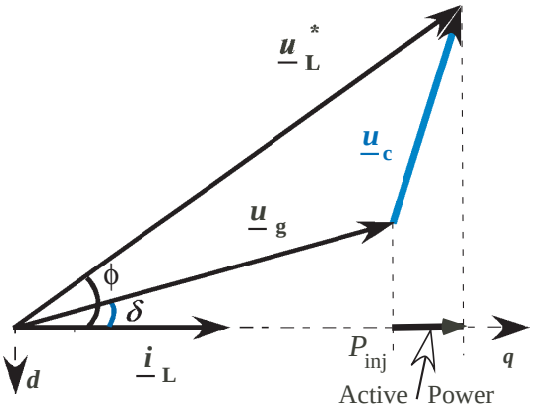


Fig.2.23. Phasor diagram of voltage difference compensation.

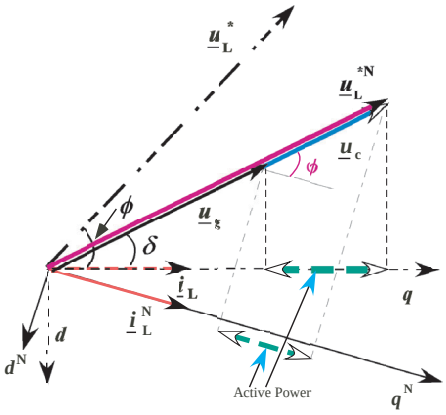


Fig.2.24. Phasor diagram of in-phase compensation.

From (2.48), it can be noticed that injection of only reactive power ($u_{cq}=0$) is possible if and only if $\cos(\phi)<\|\underline{u}_g\|/\|\underline{u}_L^*\|\cos(\delta)$. This implies that to inject only reactive power, the power factor of the load should be less than the drop of the grid voltage in pu when no phase jump occurs.

In-Phase Compensation

When applying the In-Phase Compensation (IPC), the load voltage is forced to be in phase with the grid voltage during the dip. Consequently, if the phase of the grid voltage jumps a certain angle due to the dip, the phase of the load voltage will jump by the same angle. Because the current is taken as a reference where the phase angle jump (δ) is measured, the load voltage will rotate by an angle ϕ-δ (as shown in Fig.2.24). If load is assumed to have a constant power factor, the load current vector is also rotated by an angle ϕ-δ. Consequently, the calculations of the injected voltage and active power is made with the reference to the new current axis d^N and q^N and the amount of active power may be reduced as indicated in Fig.2.24. Because both of the load voltage and the grid voltage are in phase during the dip, the amplitude of the injected voltage by the SSC is minimum.
The d- and q-components of the injected voltage are:

$$\begin{aligned} u_{cd} &= \left(\|\underline{u}_g\|-\|\underline{u}_L\|\right)\sin(\phi) \\ u_{cq} &= \left(\|\underline{u}_L\|-\|\underline{u}_g\|\right)\cos(\phi) \end{aligned} \tag{2.49}$$

Phase Advance Compensation

Phase Advance Compensation (PAC) has been proposed in [42, 43] to reduce the energy storage size. By the phase advance, it is meant that the injected voltage is synthesized in such a way that it leads the grid voltage during the voltage dip. Accordingly, the phase of the load voltage will jump by a certain angle, which may cause problems to some of the loads. Moreover, the effect of the power factor of the load on the PAC has not been studied, particularly in the case of constant power factor loads.

For constant power factor loads, if the phase of load voltage jumps by a certain angle, the phase of the load current will jump the same angle to keep the power factor angle constant. This implies that to keep the injected active power minimum, the load voltage vector will move in a circle whose radius is equal to the load voltage magnitude. Consequently, the operating point when the dip commences (to minimize active power) will not be the same during the dip and the minimization of active power may not be realized. Moreover, when experiencing a voltage dip associated with a phase angle jump, there exist a natural phase advance with respect to the grid voltage and this phase advance should be exploited in the compensation process. Another factor, which limits the applicability of the PAC, is that the magnitude of the injected voltage that should be limited within the ratings of the VSC. Fig.2.25 displays the phasor diagram of the PAC, where the injected voltage $\underline{u}_c$ leads the grid voltage by an angle β. It is shown also in Fig.2.25 that if the VDC is used, the injected voltage will lead the grid voltage by the "natural phase advance angle," β_N due to the phase jump of the grid voltage during the dip. The angle β_N can be obtained as

$$\beta_N = -\delta + \tan^{-1}\left\{\frac{\sin(\phi) - d\sin(\delta)}{\cos(\phi) - d\cos(\delta)}\right\} \tag{2.50}$$

where $d = \|\underline{u}_g\| / \|\underline{u}_L\|$. Then advancing the injected voltage should start with the angle β_N. Adding an angle $\Delta\beta$ to β_N is made to minimize the injected active power: $\beta = \beta_N + \Delta\beta$, where β is the advanced phase of the injected voltage during the dip. Due to the phase advance of the injected voltage by an angle β, the load voltage vector rotates by an angle θ. This rotation angle is calculated as:

$$\theta = \beta - \sin^{-1}\{d\sin(\beta)\} + \delta - \phi \tag{2.51}$$

In this case, the injected voltage d- and q-components are:

$$\begin{aligned} u_{cd} &= -\|\underline{u}_L\|\sin(\phi) + \|\underline{u}_g\|\sin(\delta - \theta) \\ u_{cq} &= \|\underline{u}_L\|\cos(\phi) - \|\underline{u}_g\|\cos(\delta - \theta) \end{aligned} \tag{2.52}$$

To illustrate the significant effect of the power factor angle φ on the injected active power and the voltage magnitude, the variables obtained by (2.48), (2.49) and (2.52) have been calculated for different values of φ and the results of are displayed in Fig.2.26 and Fig.2.27. The maximum injected voltage and active powers are assumed 0.5 pu of the load voltage and rated power. Fig.2.26 illustrates the relation between the required active power versus φ. In Fig.2.27, the amplitude of the injected voltage is drawn as a function of φ for the three compensation strategies. The considered voltage dip has a magnitude of 0.7 pu and its phase jumps 30^o. The phase advance angle used here is $\pi/4$. It is noticed from Fig.2.26 and Fig.2.27 that for very high power factors loads (greater than 0.98), the IPC minimizes both the active power and the injected voltage magnitude. As the power factor decreases (φ increases), the required active power decreases for all of the three strategies and the PAC ensures that the SSC will inject the minimum amount of active power. On the other hand, the injected voltage magnitude increases as φ increases in the case of the PAC and it is independent on φ in the case of the IPC.

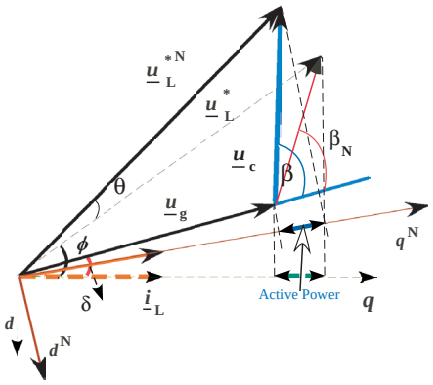


Fig.2.25. Phasor diagram of phase advance compensation.

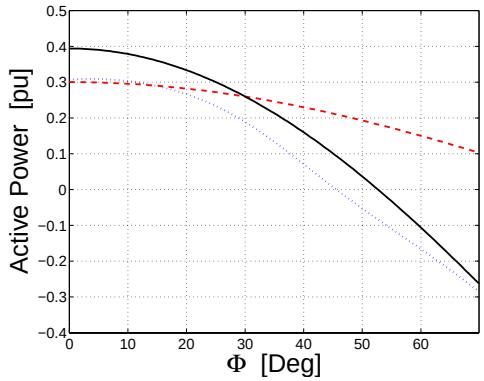


Fig.2.26. Injected active power in case of VDC (solid), IPC (dashed) and PAC (dotted).

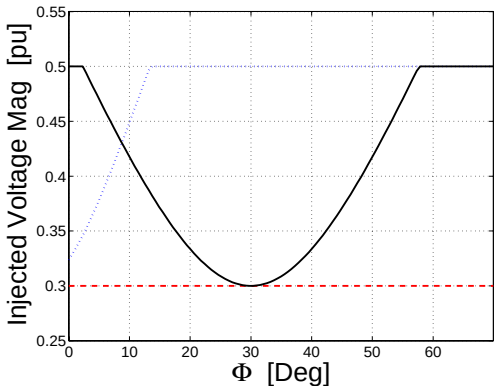


Fig.2.27. Injected voltage magnitude in case of VDC (solid), IPC (dashed) and PAC (dotted).

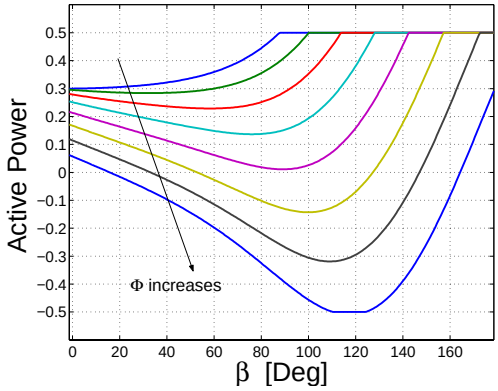


Fig.2.28. Injected active power by applying PAC versus the advance angle.

It is worth to mention that the amount of active power is also a function of the advance angle β as shown in Fig.2.28 in the case of PAC. From Fig.2.28, it can be concluded that there is an angle β that results in minimum active power and if the phase advance is further increased the injected active power will not be minimum. It is also shown that for low power factor loads, the minimum active power could be negative. This implies that the storage of the SSC will be charged during the dip.

Progressive Phase Advance Compensation

Applying the PAC causes the phase of the load voltage to jump during the dip. Some of the loads may be disturbed because of the phase jump such as the dc drives and induction motors. To overcome the problems associated with the phase angle jump, the Progressive Phase Advance Compensation (PPAC) has been proposed [43]. The strategy is based on making the phase advance of the injected voltage progressively in such a way that the load will not sense a large phase-angle jump. This can be achieved either by the proper selection of the gains of the Phase Locked Loop as presented in [44] or by dividing the phase advance angle β into small steps. After the dip, the phase advance caused by this strategy should be removed by applying small backward steps.

Proposed Control Algorithm to Optimize SSC Performance

From the power quality point of view, the VDC is the best strategy. But this is in contrast to the energy saving principle. From the energy saving perspective, the PAC is excellent but it requires the injection of higher voltage magnitude. Thus, the proposed control algorithm uses the VDC at the dip start and then applies the PPAC in order to minimize the injected active power. Application of the PPAC is done after checking the injected voltage magnitude and comparing it to the rated voltage of the SSC. The proposed algorithm is based on the double vector control algorithm presented in Section 2.5 to obtain a fast and improved transient performance. A flow chart of the proposed algorithm is shown in Fig.2.29. It is noted that the different compensation strategies are employed by the algorithm to satisfy the requirements such as: 1) minimum injection of active power; 2) keeping the injected voltage magnitude just below the maximum allowable voltage by the SSC; 3) improving the continuity of load voltage waveform.

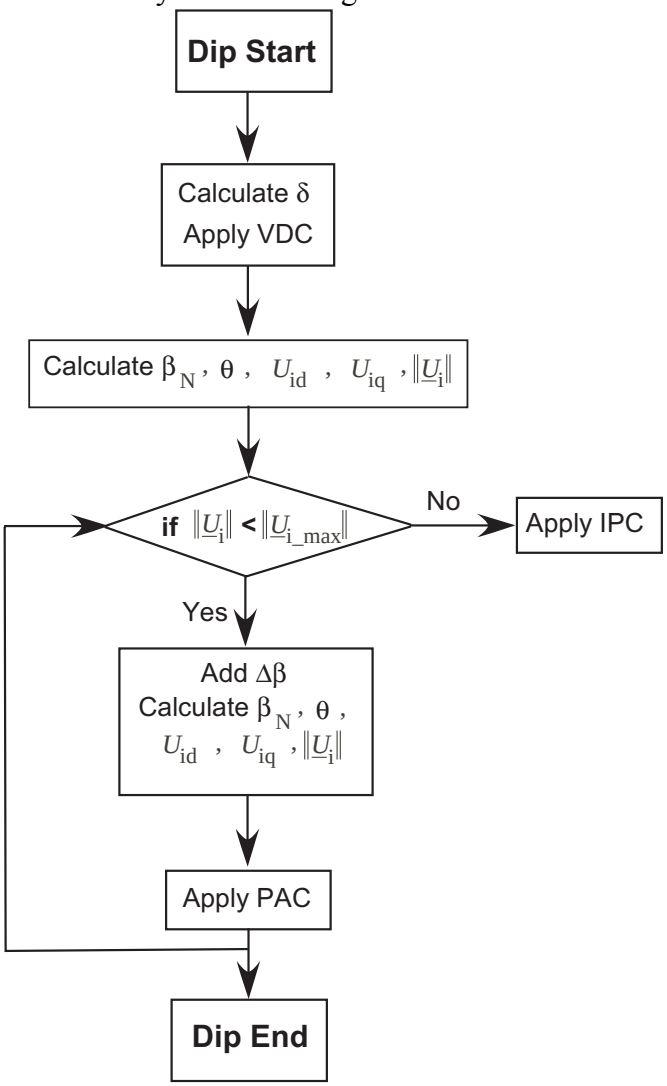


Fig.2.29. Flow chart of proposed controller to optimize performance of Static Series Compensator.

2.10. STATIC SERIES COMPENSATOR AS AN ACTIVE FILTER

2.10.1. Voltage Harmonics

The harmonic contamination has become a problem to sensitive loads. The effect of harmonic distortion on equipment and power system operation is documented in many textbooks and literature such as [6,7,8,9]. Thus to guarantee the operation of such loads, these harmonics should be filtered out from the supplied voltage. The traditional response to mitigate harmonics is the use of passive filters. Passive filters provide either a low-impedance path or a high-impedance block to harmonics [9]. However, passive filters have some shortcomings such as: dependence on the source impedance; resonance between the passive filter and the source impedance; not being able to adapt to the changes of the load conditions. Due to the shortcomings of the passive filters, the active filters have been proposed [41]. Instead of providing impedance paths to current/voltage harmonics, active filters inject the same magnitude of the harmonic current/voltage with an opposite direction to cancel out the harmonics at the selected node (either load terminals or the point of common coupling). It has been proposed to extend the capability of the SSC to compensate for grid harmonics by selective harmonic control in steady state operation [45]. To be able to regulate the load voltage at the desired voltage and filter out harmonics, the fundamental voltage component as well as the harmonic contamination of the grid voltage should be accurately detected. Hence, any employed control algorithm should perform the following tasks satisfactorily: 1) detect the start and the end of the voltage dip; 2) separate the fundamental component of the measured voltages and currents; 3) estimate the harmonic voltage that should be injected. To satisfy those requirements, this thesis proposes a moving average filter to detect the fundamental component of the grid voltage while using the DVC algorithm to improve the transient performance of the SSC. A selective harmonic compensation strategy is applied to filter out the grid harmonics.

2.10.2. Moving Average Filter

The idea behind applying a moving average filter (MAF) to detect the fundamental component of the measured signals is based on the fact that the harmonics are transformed into oscillations in the synchronous reference (*dq*) frame. In the *dq*-frame, if the voltage is sinusoidal with only the nominal frequency, this voltage appears as a dc voltage. In the presence of harmonics, the voltage appears as a dc component but superimposed with oscillations whose frequency depends on the order of the present harmonic and the nominal frequency. An illustrative diagram for the principle of the MAF is shown in Fig.2.30. The analogue form of a MAF for an input signal x is given as in (2.53). This filter calculates the mean value of the input signal in the time period from t-T to t, where T is the window width.

$$\bar{x}(t) = \frac{1}{T}\int_{t-T}^{t} x(t)dt \tag{2.53}$$

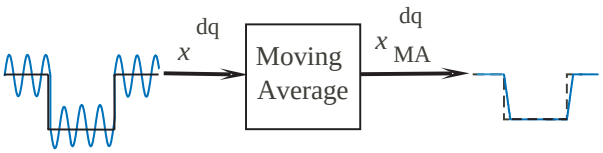


Fig.2.30. Principle of using moving average filter.

To realize a MAF as a part of a discrete control algorithm, the input signal is sampled N times in the period T and the form given in (2.53) is modified as in (2.54):

$$\bar{x}(k) = (1/N) \sum_{j=k-N+1}^{j=k} x(j) \tag{2.54}$$

Although the formula given in (2.54) is easy to implement in a digital controller, it is computationally expensive. An alternative formula, which is not computationally expensive and also easy to implement is given in (2.55):

$$\bar{x}(k) = \bar{x}(k-1) + \{x(k) - x(k-N)\}/N \tag{2.55}$$

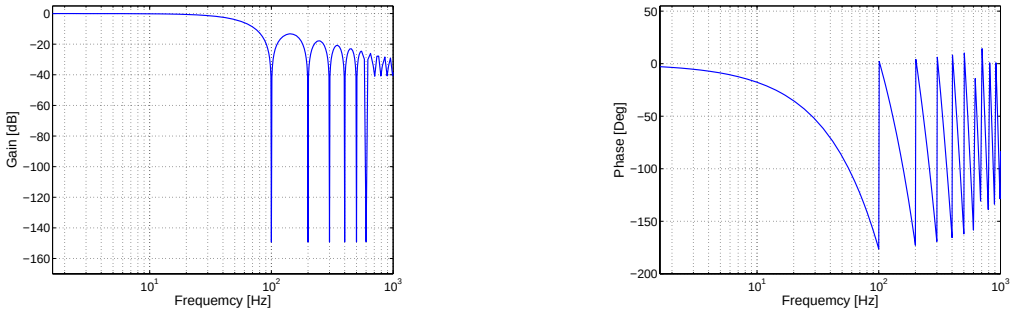
where $x(k\text{-}N)$ is the input signal but it is delayed by N samples. The formula in (2.55) leads to obtain the transfer function of the MAF as:

$$\frac{\bar{x}(z)}{x(z)} = \frac{1}{N} \frac{z^N - 1}{z^N - z^{N-1}} \tag{2.56}$$

The frequency response of the transfer function of the MAF is shown in Fig.2.31, where a half-cycle window is applied with a sampling frequency of 5 kHz and fundamental frequency of 50 Hz. It can be seen from Fig.2.31 that the gain is 0 dB for frequencies up to 30 Hz. For frequencies, which are multiples of 100 Hz, the gain is very low (-140 dB). These frequencies are the frequencies due to the dominant harmonics (5^{th}, 7^{th}) in the *dq*-frame. It can also be seen that the phase of those frequencies is zero.

2.10.3. Resonant Filter

The use of resonant filters has been implemented to selectively compensate harmonic currents by active filters [46,47]. They can be applied to mitigate harmonic voltage distortion by the SSC. The idea is to implement a filter, which has particular characteristics.



a) b)

Fig.2.31. Frequency response of half-cycle window moving average filter: a) gain, b) phase.

These characteristics are: low gain for all frequencies apart from the selected frequency; no phase shift at the selected frequency. In the continuous time domain the transfer function of such filter is:

$$G(s) = \frac{K_f \omega_c (s + \omega_c)}{s^2 + 2\omega_c s + \omega_c^2 + \omega_n^2} \tag{2.57}$$

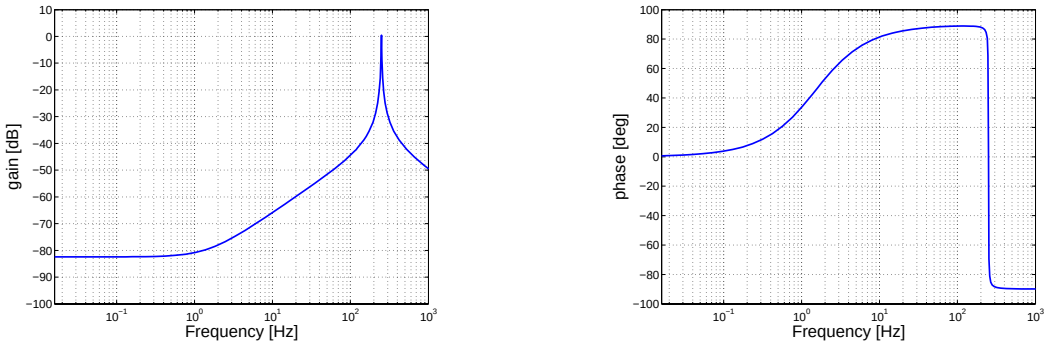
where: K_f is the filter gain; ω_h is the frequency of the selected harmonic in rad/s; ω_c is the band frequency in rad/s to improve the transient performance of the filter. K_f is designed to obtain a unity gain at the selected frequency (ω_h). In order to obtain that, the gain K_f should be equal to $2\omega_c$ under the assumption that $\omega_h >> \omega_c$. The filter in (2.57) should be discretized to be a part of a discrete control algorithm, resulting:

$$G(z) = \frac{C_1 z^2 + C_2 z + C_3}{C_4 z^2 + C_5 z + C_6} \tag{2.58}$$

The coefficients C_1 to C_6 are constants for one selected harmonic frequency. Equation (2.58) can be easily implemented in the control algorithm. Fig.2.32 illustrates the frequency response of the 5th order resonant filter, where it is shown that the filter gain is 0 dB at 250 Hz (5th harmonic) and very low otherwise. In Fig.2.32, $\omega_h = 1570.8$; $\omega_c = 2\pi$ and $K_f = 4\pi$.

2.10.4. Block Diagram of Proposed Controller for Mitigation of Voltage Dips and Harmonics

Referring to the DVC algorithm presented in Section 2.5, the inputs to the controller are: the grid voltage u_g^{dq}; the injected voltage at the low voltage side of the injecting transformer u_c^{dq}; the grid current i_g^{dq} and the converter current i^{dq}. These signals are individually input to a MAF. The output of the MAFs are the inputs to the basic DVC algorithm to calculate the fundamental converter voltage (u_1^{*abc}). At the same time, the reference of the injected harmonics (u_H^{*abc}) is obtained by using a resonant filter for each individual harmonic that should be filtered.



a) b)

Fig.2.32. Frequency response of 5th order resonant filter: a) gain, b) phase.

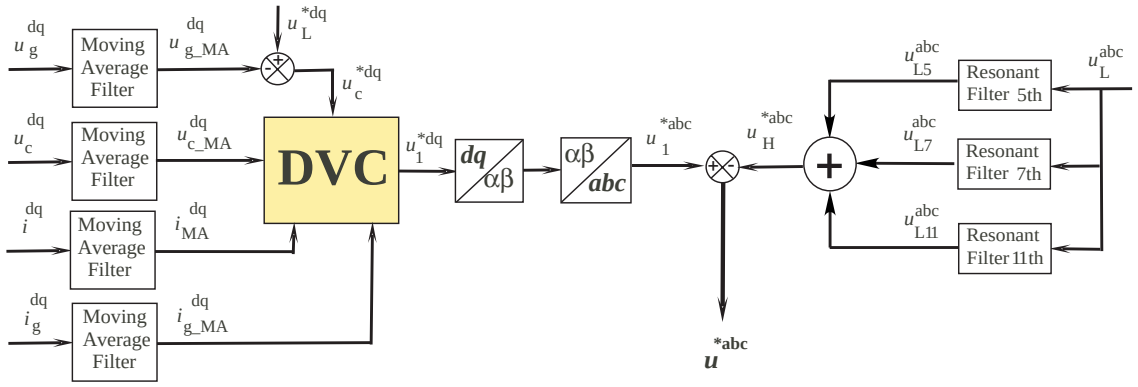


Fig.2.33. Resonant and moving average filters with double vector controller to mitigate harmonics.

$u_{\mathrm{H}}^{*\mathrm{abc}}$ is obtained by passing the load voltage ($u_{\mathrm{L}}^{\mathrm{abc}}$) to the resonant filters. Here, it is worth to mention that the measurement of the load voltage is not necessary because the load voltage can be calculated by summing the grid and the injected voltages. After estimating the reference of the fundamental injected voltage and the reference of the injected harmonic voltage, both voltages are added to each other.

2.11. MITIGATION OF VOLTAGE SWELLS AND OVERVOLTAGE PROTECTION

2.11.1. Voltage Swells

A voltage swell is an increase in the RMS voltage above 1.1 pu at the power frequency for duration from 0.5 cycle to 1 minute [20].

An example of a measured 20% voltage swell for 5 fundamental cycles is depicted at Fig.2.34. Swells and overvoltages can cause overheating, tripping or even destruction of industrial equipment such as motor drives and control relays. Many power quality surveys have been made in order check the load immunity against power system disturbances [48,49]. From those surveys, conducted at North America, it can be stated that the voltage swells are experienced in the power systems locally or remotely. The number of voltage swells per year is naturally random but from the statistics presented in [48], it can be concluded that not less than 165 events/year have been recorded. The duration of the recorded swells varies from one fundamental cycle to 8 hours. A simplified circuit diagram for the SSC is depicted at Fig.2.35, where R_{LF}+jX_{LF} is the impedance of the LC-filter inductor and R_{LT}+jX_{LT} is the impedance of the series transformer. The voltage swell is an increase in the RMS voltage of the grid, which implies that the reference of the injected voltage by the SSC is negative because $\underline{u}_g$ is greater than $\underline{u}_{\mathrm{L}}^{*}$. Hence, the direction of active power flow may be reversed and the ESC may be charged. In steady-state basis, the reference of the injected voltage by the SSC is computed as:

$$\underline{U}_{\mathrm{inj}} = \Delta\underline{U} = \underline{U}_{\mathrm{L}}^{*} - \underline{U}_{\mathrm{g}} \tag{2.59}$$

From Fig.2.35, the output voltage of the SSC can be calculated as:

$$\underline{U} = \Delta\underline{U} - \left\{\underline{I}(R_{\mathrm{LF}} + \mathrm{j}X_{\mathrm{LF}}) + \underline{I}_g(R_{\mathrm{LT}} + \mathrm{j}X_{\mathrm{LT}})\right\} \tag{2.60}$$

where:

R_{T}: resistance of the injection transformer,
X_{LT}: leakage reactance of the injection transformer,
R_{F}: resistance of the LC-filter,
X_{LF}: leakage reactance of the LC-filter
$\underline{I}$: current through the LC-filter inductor,
$\underline{I}_{\mathrm{c}}$: current through the LC-filter capacitor,
$\underline{I}_{\mathrm{g}}$: Load current.

If the capacitor current $\underline{I}_{\mathrm{c}}$ can be ignored, the reference voltage of the VSC is simplified to:

$$\underline{U} = \left\{\Delta\underline{U} - \underline{I}(R_{\mathrm{LF}} + R_{\mathrm{LT}})\right\} - \mathrm{j}\left\{\underline{I}\left(X_{\mathrm{LF}} + X_{\mathrm{LT}}\right)\right\} \tag{2.61}$$

Equation (2.61) shows that even in case of a voltage swell, the reference voltage of the VSC may be positive or negative depending on: 1) the characteristics of the voltage swell; 2) the impedance of the series injection transformer and the LC-filter. Being positive means that the SSC is delivering active power to the load and the ESC discharges. If the reference voltage of the VSC is negative, it indicates that the grid is feeding active power to the SSC and the ESC is charged unless the overvoltage protection is triggered.

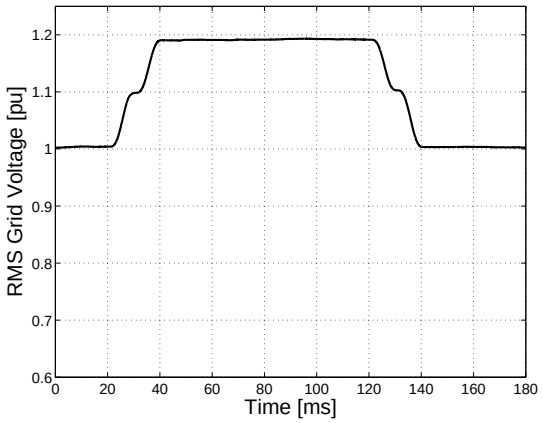


Fig.2.34. Example of voltage swell.

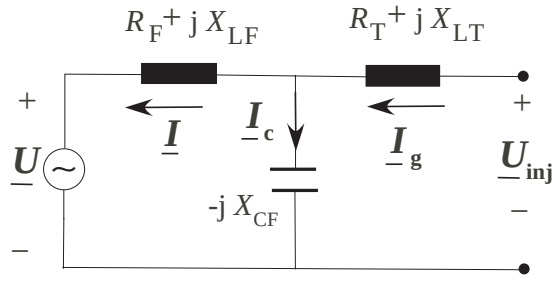


Fig.2.35. Simplified single line diagram of static series compensator in steady state during swell.

The phase of the grid voltage may jump during the voltage swell and thus becomes either lagging or leading the phase of the load voltage. The amount of active power that can be exchanged during the voltage a swell with a lagging phase jump is calculated in pu as:

$$P_{\text{inj}} = \cos(\phi) - (1 + \Delta U)\cos(\phi - \delta) \tag{2.62}$$

In the case of a voltage swell with a leading phase jump, the active power is obtained as:

$$P_{\text{inj}} = \cos(\phi) - (1 + \Delta U)\cos(\phi + \delta) \tag{2.63}$$

where

ϕ: load power factor angle,

δ: phase angle jump of the grid voltage,

$1+\Delta U$: the voltage swell magnitude.

From (2.62) and (2.63), it is noted that the injected active power depends on the load power factor, the voltage swell magnitude and the phase angle jump of the grid voltage during the swell. If the phase of the grid voltage does not jump due to the swell; $\delta = 0$, the expressions in (2.62) and (2.63) are reduced to $P_{\text{inj}} = -\Delta U \cos(\phi)$. The energy stored/delivered by the ESC is obtained as: $E_{\text{ESC}} = P_{\text{inj}} t_{\text{swell}}$, where t_{swell} is the swell duration. Hence by the aid of (2.62) and (2.63) and the expected duration of the voltage swell, the size of the energy storage can be designed.

2.11.2. Overvoltage Protection Scheme

If the dc voltage of the SSC exceeds a predetermined voltage level, the SSC should be protected against the overvoltage. This overvoltage protection can be made when the SSC is online or offline depending on the value of the measured dc voltage. For instance, if the dc voltage reaches a value in the middle of the nominal voltage and the maximum allowable voltage, the online overvoltage protection should be triggered. The offline protection is triggered if the dc voltage exceeds its maximum allowable voltage. An illustrative diagram of the zones of the overvoltage protection is depicted at Fig.2.37. In Fig.2.37, the zone of the online protection is placed between the nominal dc voltage $U_{\text{dc\_NOM}}$ and the predetermined online protection voltage level $U_{\text{on\_p}}$. The zone of the offline protection is located between the maximum of the dc voltage U_{max} and the setting of the online protection $U_{\text{on\_p}}$.

Online protection

If the SSC is required to be in service during a voltage swell, the overvoltage protection is realized online by using a shunt resistor across the dc link together with a dc chopper. A single-phase diagram of the overvoltage protection scheme is shown in Fig.2.36. The dc chopper is enabled when the dc voltage exceeds a certain voltage level (such as $U_{\text{on\_p}}$ in Fig.2.37). This voltage level is determined by the voltage that the SSC valves can withstand due to the voltage swell. If the dc chopper is closed (on-state), the dc resistor dissipates the energy excess in the dc capacitor. In other words, the dc capacitor will discharge though the dc chopper and the resistor.

Offline protection

Offline protection is realized by turning on the thyristor pair *thy* on the line side of the SSC (Fig.2.36) as well as the upper or the lower IGBTs in each phase leg of the VSC. Turning on the upper IGBTs and turning off the lower IGBT or vice versa interrupts the dc current and blocks the dc voltage. It is worth to note that turning on the thyristors only is not sufficient to protect the VSC because the thyristors will short-circuit the injection transformer and the VSC. In this case the energy stored in the capacitor of the VSC will circulate a high current through the valves of the VSC, which may be dangerous as well.

2.11.3. Design of dc resistor

The resistance used with the chopper should satisfy two main requirements: 1) the discharging process of the dc capacitor to the rated dc voltage should be made in a reasonable time; 2) the initial discharging current should not exceed the maximum allowable current of the chopper. The minimum value of the resistance is obtained as:

$$R_{\text{chop\_min}} = U_{\text{on\_p}} / I_{\text{disch}} \tag{2.64}$$

While the maximum value of the resistance is obtained as:

$$R_{\text{chop\_max}} = t_{\text{disch}} / (C_{\text{dc}} \ln(U_{\text{dc\_max}} / U_{\text{dc\_NOM}})) \tag{2.65}$$

where $U_{\text{on\_p}}$: value of the dc voltage, which triggers the online protection;
$U_{\text{dc\_NOM}}$: nominal dc voltage;
C_{dc}: energy-storage capacitor;
I_{disch}: initial discharging current;
t_{disch}: discharging time.

To clarify the significance of (2.64) and (2.65), a design example is given here. A prototype SSC is under development (in another project by another PhD student) at the Department of Electric Power Engineering, Chalmers University of Technology, Sweden. The relevant data of this prototype is given in TABLE.I.

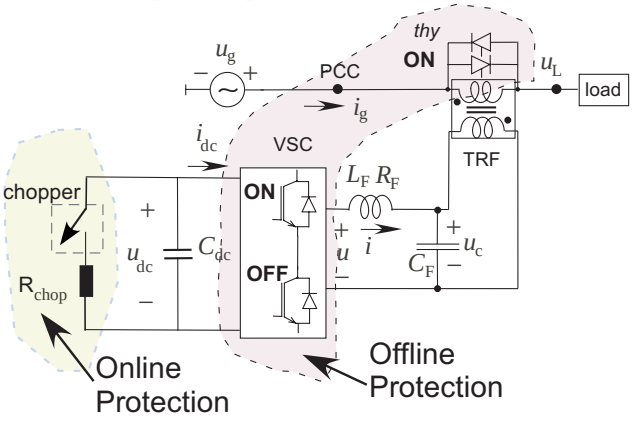


Fig.2.36. Overvoltage protection scheme of static series compensator.

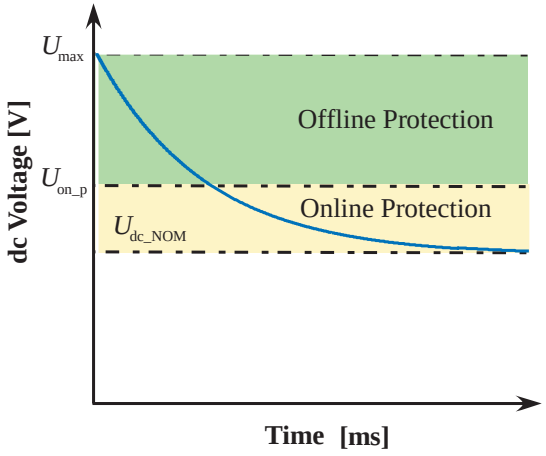


Fig.2.37. Zones of online and offline protection of static series compensator.

TABLE.I. Prototype SSC under construction

Converter Model	*Danfoss VLT 5052* [50]
U_{on_p}	700 V
U_{dc_NOM}	600 V
I_{disch}	90 A
C_{dc}	4.7 mF

The discharging time t_{disch} is selected as ½ period of the fundamental frequency (10 ms). This is due to the fact that the switching frequency of the chopper is designed as 50 Hz and the duty cycle is 50%. Thus, the discharging of the dc capacitor is assumed to be complete within one switching cycle of the chopper. Applying (2.64) and (2.65) with the data given in TABLE.I and taking the discharging time t_{disch} as ½ period of the fundamental frequency (10 ms) yields: R_{min} = 7.7 Ω and R_{max} = 13.8 Ω. Here it is worth to mention that the proposed value of the resistance by the manufacturer [50] is 12 Ω , which belongs to the range $R_{min}<R_{chop}< R_{max.}$. A resistor of 9 Ω resistance was designed and used in the SSC prototype given in TABLE.I, which shows the significance of (2.64) and (2.65).

2.12. SUMMARY OF CHAPTER 2

The operational principle and the design of the Static Series Compensator (SSC) have been described in this Chapter. A Double Vector Control (DVC) algorithm was developed to mitigate the balanced voltage dips. Then the DVC was modified to cope with unbalanced dips. The capability of the SSC to mitigate voltage swells has been investigated and an overvoltage protection scheme was proposed. Also, the functionality of the SSC as a series active filter was studied and a control algorithm has been developed.

CHAPTER

3. RESULTS AND ANALYSIS

3.1. INTRODUCTION

In Chapter 2, different controllers have been developed in order to mitigate three power quality problems: voltage dips, voltage swells, and voltage harmonics. In order to investigate the performance of the developed controllers, simulations and experiments are made. A simulation model is designed and implemented in the PSCAD/EMTDC package. Experiments are carried out on a 10 kV SSC prototype in order to show the validity of the controllers. Some of the results are presented and analyzed in this Chapter. For the interested readers, all the results are given in the included papers.

3.2. SIMULATION MODEL

The simulation model is composed of three main blocks: 1) power system; 2) load model; 3) model of the SSC. The main parts of the simulation model are displayed in Fig.3.1. All the models are obtained by the defined models in the PSCAD/EMTDC package. The power system is modeled as a voltage source behind a finite source impedance to simulate the grid performance due to power system events such as short-circuit faults and load switching. Three-different types of loads are involved in the simulation model: static linear; dynamic linear and nonlinear loads. The static linear load is a resistive-inductive and an induction machine represents a model for the dynamic linear load. The nonlinear load is a three-phase diode rectifier.

The control of the SSC is realized by a number of user-defined models, which are written using the FORTRAN language and linked with PSCAD/EMTDC. Also the upstream loads are modeled and investigated. Capacitor banks and transformers are candidates for the upstream loads.

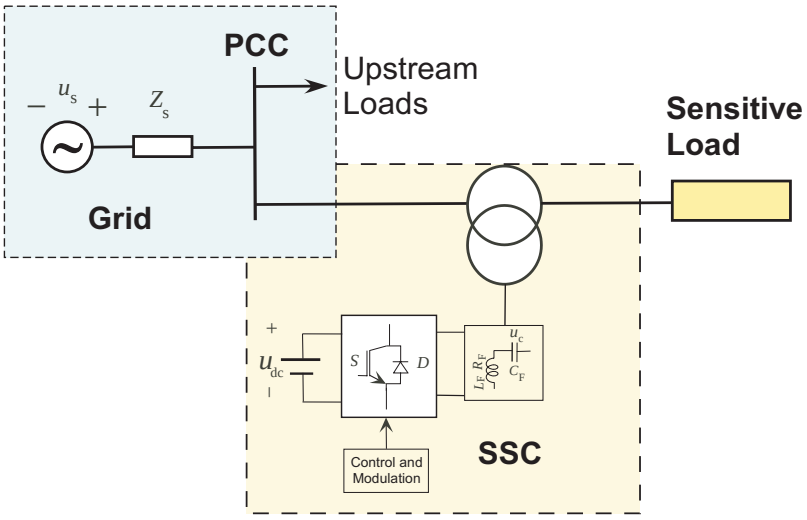


Fig.3.1. Simulation model in PSCAD/EMTDC.

3.3. EXPERIMENTAL SETUP

The experimental setup of the SSC has been built at the Institute of Energy Technology, Aalborg University, Denmark as a part of the PhD work reported in [31]. A single line diagram of the experimental setup is shown in Fig.3.2. The SSC displayed in Fig.3.2 is operated at 10 kV. To obtain a 10kV line in the laboratory, a step-up transformer 0.4/10 kV and a step-down transformer 10/0.4 kV are installed. Data of the system is given in Paper C. The reference load voltage is $\underline{u}_{\mathrm{L}}^{*\mathrm{dq}} = u_{\mathrm{Ld}}^{*} + \mathrm{j}u_{\mathrm{Lq}}^{*} = 0+\mathrm{j}1.0$ pu. The SSC was fed with a programmable California Instruments Supply at 380 V, which was then fed into the step-up transformer to create the 10 kV system. A photo of the step-up and the step-down transformer is displayed in Fig.3.4. Three specially made 67 kVA 0.29 kV/2.9 kV single-phase transformers are used to series connect the voltage source converter of the SSC the 10 kV system. The load voltage was stepped down using step-down transformer to allow utilization of low-voltage linear and non-linear loads.

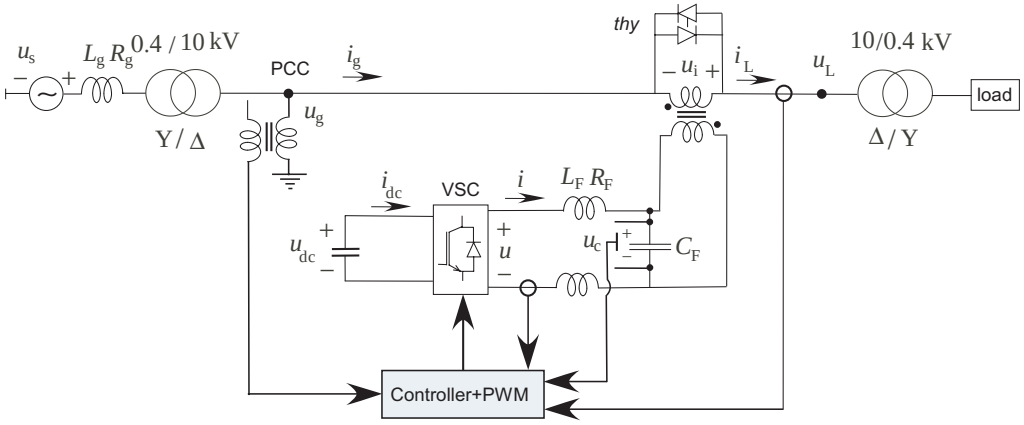


Fig.3.2. Single-phase diagram of 10 kV static series compensator used in experiments.

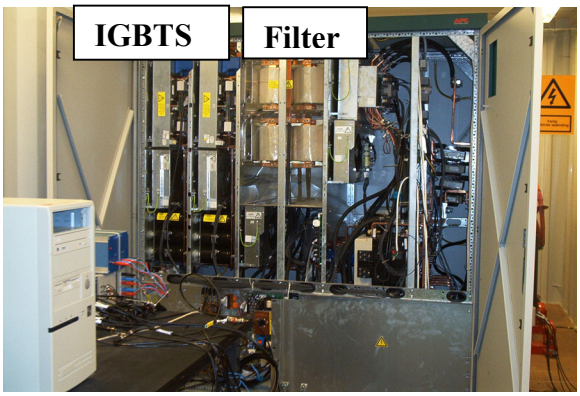


Fig.3.3. Photo of experimental setup: VSC and LC-filter inductor.

Fig.3.4. Photo of high voltage transformers used to generate 10-kV system.

The dc-bus of the converter is charged maximally to 600V using a unidirectional dc supply, which provides 4680 J of energy in the 26 mF of the dc capacitors. An Analog Devices AD21062 floating-point Sharc DSP was used to implement the developed controllers, with the PWM signal generation for the six IGBT phase-legs (shown in Fig.3.3). The PWM signals were created using a Siemens SAB 80C167 Micro Controller. The medium voltage supply and load voltages were measured with ABB resistive voltage transducers. At the low voltage side, the injected voltage is measured by LV 25-P/SP2 voltage transducer. Also the grid current at the low voltage side is measured by LT 200-S/SP44 LEM current transducer.

3.4. GENERATION AND MITIGATION OF VOLTAGE DIPS

3.4.1. Generation of Voltage Dips

In the simulation model, the voltage dips are generated by switching on impedance to the ground at the Point of Common Coupling (PCC), upstream the SSC. This situation is equivalent to a remote short-circuit fault, which results in voltage dips with a phase angle jump. Experimentally the programmed power supply (California Instruments), was employed to generate balanced and unbalanced voltage dips.

3.4.2. Mitigation of Balanced Voltage Dips

A resistive load of 20 Ω is used as a linear load and an induction machine: ASEA MK 110-23 IM (see Paper C) is installed as a dynamic linear load while carrying out the experiments. Also a three-phase diode rectifier is connected directly downstream the SSC as a nonlinear load. Only, the results with the IM are presented in this Chapter. The performance of the SSC with the linear and nonlinear loads is analyzed in Paper C. A 70 % voltage dip is initiated for 5 cycles at the PCC as displayed in Fig.3.5a. The injected voltage is shown in Fig.3.5b and the load voltage is displayed in Fig.3.5c. A zoom on the load voltage at the dip start is shown in Fig.3.5d while a zoom at the dip end is displayed in Fig.3.5e. The results confirm the improved transient performance of the SSC compared to like using phasors [22,23] and vector control without an inner current loop [31]. The speed

of the IM is shown in Fig.3.5f, in two cases: 1) the SSC is offline; 2) the SSC is online. When the SSC is offline, the load voltage, which is the input voltage of the IM, decreases due to the voltage dip. Consequently, the IM decelerates to 0.9 pu of the rated speed. But when the SSC is made online, the speed of the IM is constant at 1 pu before, during and after the dip. Because the dip is balanced, the SSC with Double Vector Control (DVC) algorithm has successfully compensated the load voltage. However, the performance of the DVC with the unbalanced dips is not satisfactory [51]. Thus, the modified DVC [51] has been implemented to cope with the unbalance.

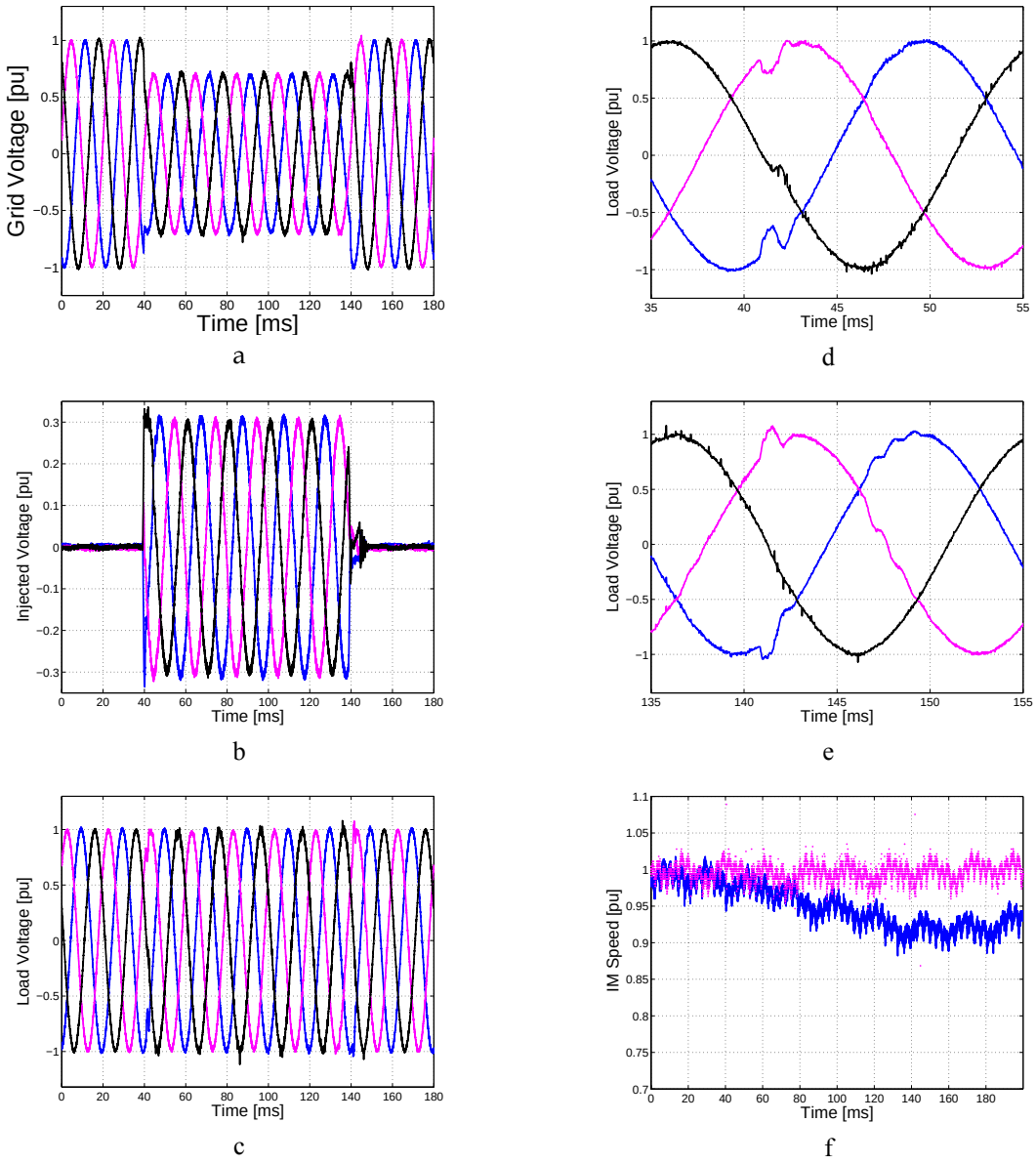


Fig.3.5. Measured 70 % voltage dip with induction machine load: a) grid voltage, b) injected voltage, c) load voltage, d) zoom at dip start in load voltage waveform, e) zoom at dip end in load voltage waveform and f) speed of induction machine: with SSC online (dotted, gray) and with SSC offline (solid). 1 pu = 10 kV line-to-line voltage.

3.4.3. Mitigation of Unbalanced Voltage Dips

An unbalanced dip is programmed to generate the grid voltage at the PCC as displayed in Fig.3.6a. One phase stays at 1 pu during the dip and other two phases drop to 0.75 pu. The injected voltage by the SSC is depicted in Fig.3.6b. The restored load voltage is shown in Fig.3.6c. Also the error in the magnitude of the load voltage (in the $\alpha\beta$-frame) is displayed in Fig.3.6d. Before the dip, the SSC is in the standby state, waiting for the dip detection. When the positive sequence of the grid voltage drops below 90%, the dip is detected and the SSC starts compensation. It is noted from Fig.3.6 that the compensated load voltage is balanced and the maximum error is below 2 %, which indicates the capability of the SSC to cope with unbalanced dips. The performance of the SSC has been tested with different switching frequencies (2 to 5 kHz), in the case of unbalanced dips. The definition of the voltage error is shown in Fig.3.7. This error is defined (in the steady state during the dip) as $\max\left\{1-\text{abs}\left(\underline{u}_{\text{L}}^{\alpha\beta}\right)\right\}$, where $\underline{u}_{\text{L}}^{\alpha\beta}$ is the vector of the load voltage at the $\alpha\beta$-frame and abs denotes the absolute or magnitude function. In Fig.3.8, the amplitude error is depicted as a function of the switching frequency. The maximum error is 7 % and it is obtained when the switching frequency is 1.5 kHz. It is noted that the error decays as the switching frequency increases. At 5 kHz the error is reduced to 2 %. More details can be found at Paper D.

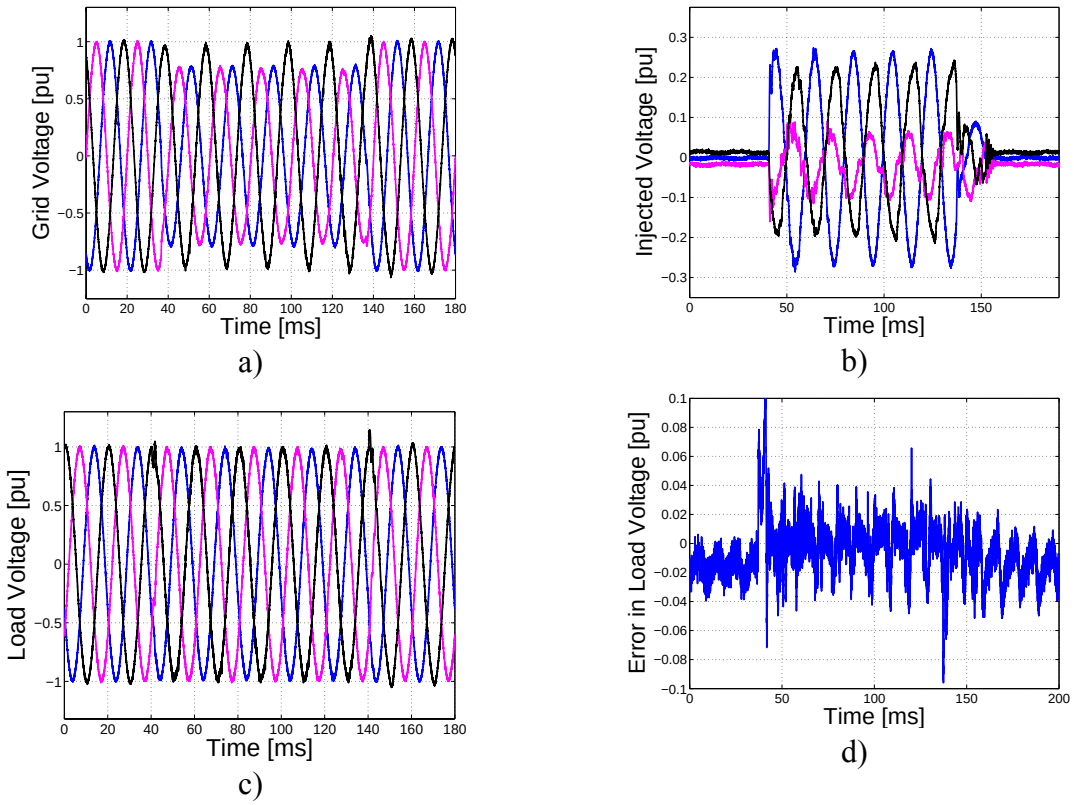


Fig.3.6. Measured unbalanced dip: u_{a}= 0.95 pu, u_{b}= 0.95 pu, u_{c}= 0.6: with resistive load: a) grid voltage, b) injected voltage, c) load voltage, d) error in load voltage. MDVC is applied with switching frequency = 3 kHz. 1 pu = 10 kV line-to-line voltage.

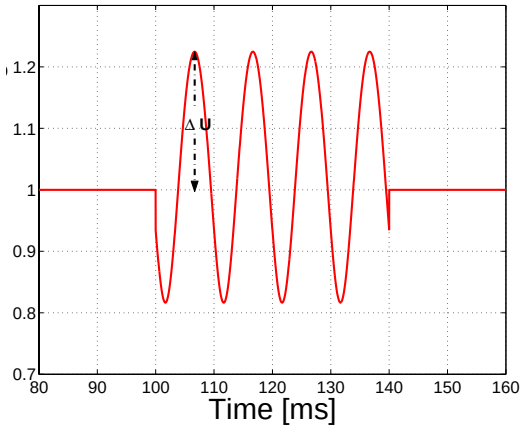


Fig.3.7. Definition of amplitude and phase error of load voltage.

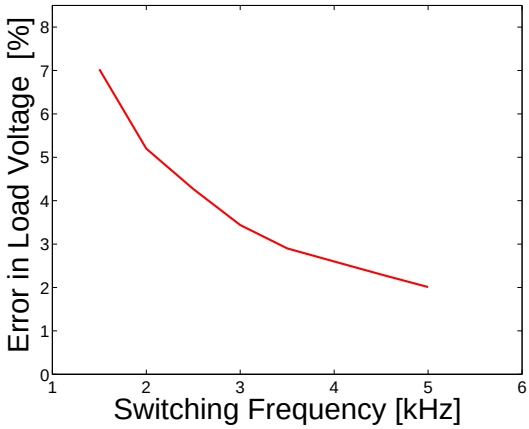


Fig.3.8. Amplitude error of load voltage as function of switching frequency.

3.5. PERFORMANCE OF SOFTWARE PHASE LOCKED LOOP

The performance of the proposed Software Phase Locked Loop (SPLL) has been tested in all the cases of voltage dips presented earlier. It has been found that the SPLL detects the phase and the frequency of the grid voltage accurately and also behaves as a low-pass filter. Paper E provides a detailed description of the SPLL as well as its performance with unbalanced dips. An example of the tested cases is given for completeness. The three-phase voltage of the grid is depicted in Fig.3.9. During the dip, the voltages of two phases drop to 70 % while the voltage of the third phase is constant as before the dip. A phase-angle jump of -30^o is associated with the initiated dip. The dip duration is 10 cycles of the fundamental frequency, i.e. 200 ms. The estimated angle of the grid voltage together with the actual one is shown in Fig.3.10. Before the dip, both of them are 90^o as the SPLL is assumed to be in the lock state. During the dip, the actual phase angle of the grid voltage jumps –30^o to becomes 60^o. The estimated angle gradually tracks the actual angle and SPLL locks again after almost 160 ms (8 cycles) from the dip start. At 400 ms, the dip ends and the phase angle returns to its pre-dip position. The proportional gain of the PI-regulator is 30 in this case. It is worth to mention that a faster transient response can be obtained by increasing the proportional gain of the PI-regulator provided that the stability limit is not reached. The time-domain voltages of one phase of the load, the grid and the injected are depicted in Fig.3.11. In the case of normal operation conditions, the load voltage is equal to the grid voltage and the injected voltage is zero. During the dip, the grid voltage decreases and the injected voltage increases to keep the load voltage at the same level as in normal operation conditions. It can be noticed from Fig.3.11 that before the dip, the phase angle of the load and the grid are the same. When the dip starts, the phase angle of the grid voltage jumps -30^o while the phase angle of the load is not subjected to the phase jump. Gradually, the phase of the load voltage approaches the phase of the grid voltage until they coincide with each other before the end of the dip. Then the phase angle of the grid voltage jumps 30^o while the phase angle of the load voltage slowly tracks it. Thus, the load voltage is protected against sudden phase jumps associated with voltage dips in the grid.

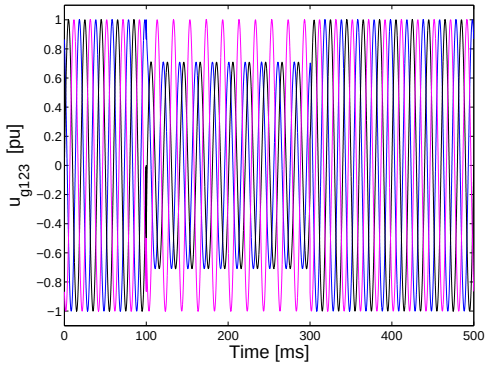


Fig.3.9. Three-phase voltage of grid at point of common coupling.

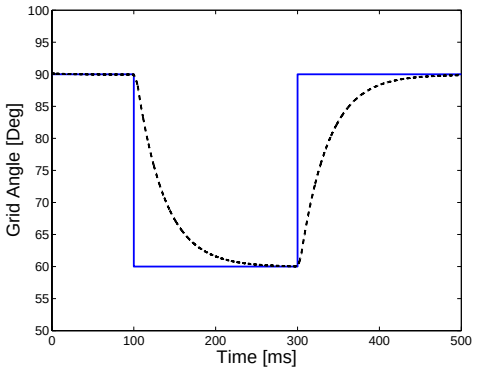
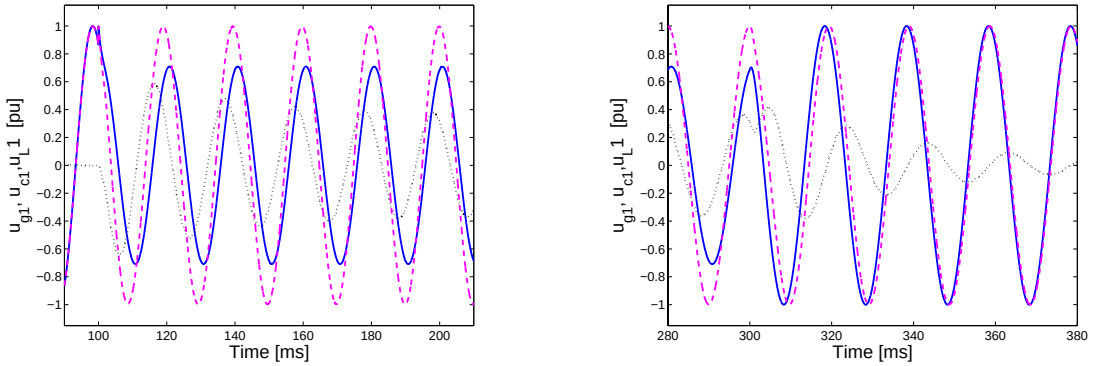


Fig.3.10. Phase angle of grid voltage: actual (solid), estimated (dashed).



a) b)

Fig.3.11. Response of load (dashed), grid (solid) and injected (dotted) voltages of phase 1: a) at dip start, b) at dip end. 1 pu = 10 kV line-to-line voltage.

3.6. CAPABILITY OF SSC TO MITIGATE VOLTAGE SWELLS

From the control point of view, the SSC should handle voltage swells in the same way it handles voltage dips. In either case, the reference of the injected voltage is stepped and the actual voltage has to track its reference. But it is a different perspective from the energy handling capability. In the case of voltage dips, the SSC delivers an active power to the load but in the case of voltage swells, the SSC may absorb the power from the grid. Since normally the SSC is operated at the standby and the required energy is available in its energy storage, the power absorption may be dangerous unless a dissipative element is installed and the power dissipation is controlled. The control of power dissipation in this context is referred to as the online overvoltage protection. Therefore the capability of the SSC to cope with voltage swells is strongly related to the online overvoltage protection. However in some cases, the voltage swells may not cause an overvoltage at the dc link as described in Chapter 2. The voltage swell characteristics and the loading conditions are the main issues that determine the energy transfer status from the grid to the SSC. Two cases of measured voltage swells are presented here. More cases are introduced in Paper H. A 10 % balanced voltage swell is programmed and measured at the PCC. The grid voltage is

depicted at Fig.3.12a, where a swell of 10% is made for 5 fundamental cycles. Fig.3.12b shows the injected voltage and the load voltage is displayed at Fig.3.12c. From Fig.3.12, it is noted that the SSC has successfully kept the load voltage at 1 pu. Fig.3.13 shows the case of unbalanced voltage swell where the voltages of the supply are programmed to have 10, 20 and 30 % voltage swell. Although the swell is unbalanced, the SSC can keep the load voltage balanced. During experiments, the ESC was fed by a separate dc source and thus the dc voltage was fixed at 480 V (0.8 pu). As the measured voltage swells are not relatively large, they have not influenced the dc voltage.

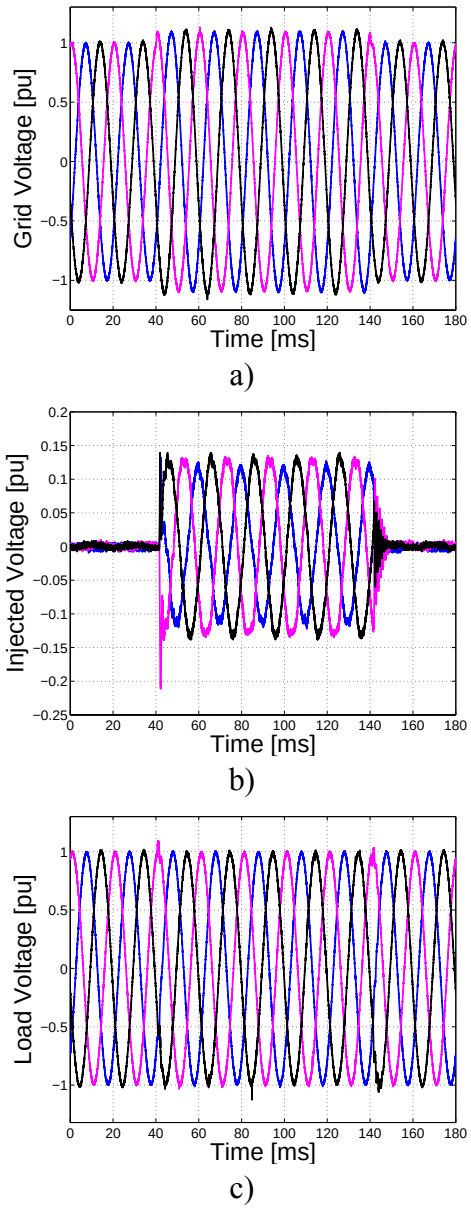


Fig.3.12. Measured balanced 10 % voltage swell with resistive load: a) grid, b) injected, c) load. 1 pu = 10 kV line-to line.

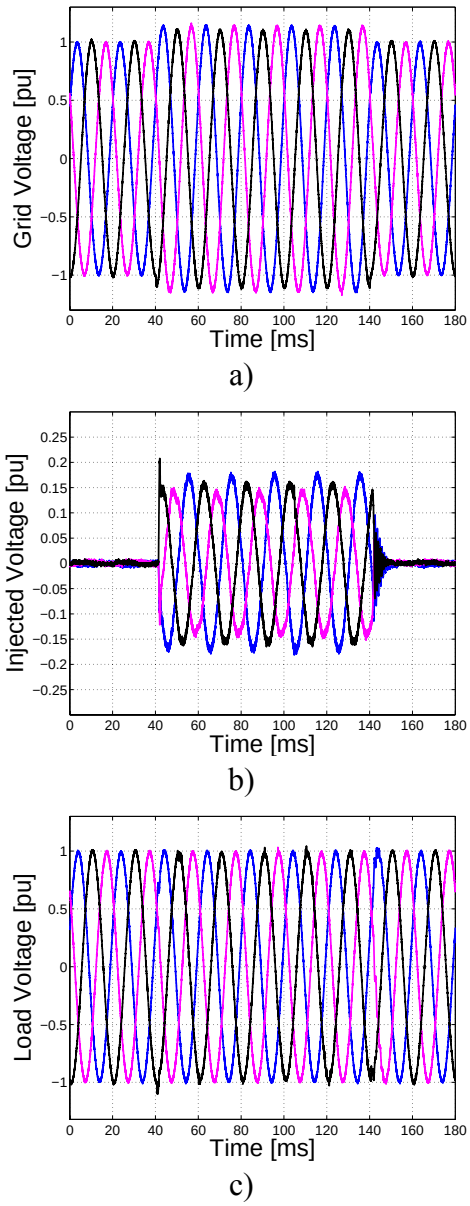


Fig.3.13. Measured unbalanced 10, 20, 30% voltage swell: with resistive load: a) grid, b) injected, c) load. 1 pu = 10 kV line-to line.

3.7. MITIGATION OF HARMONICS

The operation of the SSC under distorted utility is investigated in two different load conditions: 1) linear load with distorted grid; 2) nonlinear load. The first case implies that the supply voltage is distorted due to other loads at the PCC while the protected load by the SSC is linear. Thus, the sensitive load downstream the SSC may experience the voltage harmonics unless the SSC injects the same amount of harmonic voltages with an opposite sign to cancel out the grid harmonics. The dominant harmonics are the lower order harmonics such as the 5^{th} and the 7^{th}. Both voltage harmonics were created by the programmable supply and successfully filtered out at the load terminals. Performance of the SSC with the developed controller for mitigation of harmonics is reported in Paper I.

A 5% 5^{th} harmonic voltage and a 2% 7^{th} harmonic voltage are supplied at the PCC by the programmable power supply. The grid voltage in this case is displayed in Fig.3.14a. Also an 80% voltage dip is created for 100 ms. In Fig.3.14b, the injected voltage by the SSC is shown. It is shown that before and after the dip, the SSC injects the 5^{th} and the 7^{th} harmonics. During the dip, the fundamental component is also injected to restore the load voltage. Fig.3.14c displays the waveform of the restored and filtered voltage when a 5% 5^{th} and 2% 7^{th} harmonic voltages are detected in the grid voltage. Obviously, the load voltage is free of harmonics and also constant at 1 pu. This can be clearer from the zoom of the load voltage at the dip start (Fig.3.14d-left) and at the dip end (Fig.3.14d-right). The FFT of the grid and the load voltage are shown in Fig.3.15, which proves that the SSC has filtered the 5^{th} and the 7^{th} harmonics from the load voltage.

Most likely, the protected load is nonlinear. Consequently, the downstream loads draw some harmonics and the voltage at PCC is distorted. This distortion may disturb other load connected at PCC. Hence, the SSC should act and filter out the most dominant harmonics. To show the filtering capability of the SSC and at the same time study its consequences at the restoring function of the SSC, four different cases have been investigated:

1) the basic DVC is applied without adding the active-filtering capability. Thus the resonant filters and the moving average filter are disabled.
2) only the moving average filters are enabled. The resonant filters are disabled;
3) 5^{th} harmonic resonant filter is activated together with the function of the moving average filter;
4) 5^{th} and 7^{th} harmonic resonant filter are enabled with the function of the moving average filter. The downstream load is nonlinear in all the cases.

All the results are presented in Paper I, which show that the SSC has successfully restored the load voltage to 1 pu and kept the total harmonic distortion below the standard limits. The RMS of the injected voltage is calculated and plotted at Fig.3.16 for all the cases. Due to the injection of harmonics together with the fundamental voltage during voltage dips, the required RMS injected voltage is increased when the same fundamental component is injected in both cases.

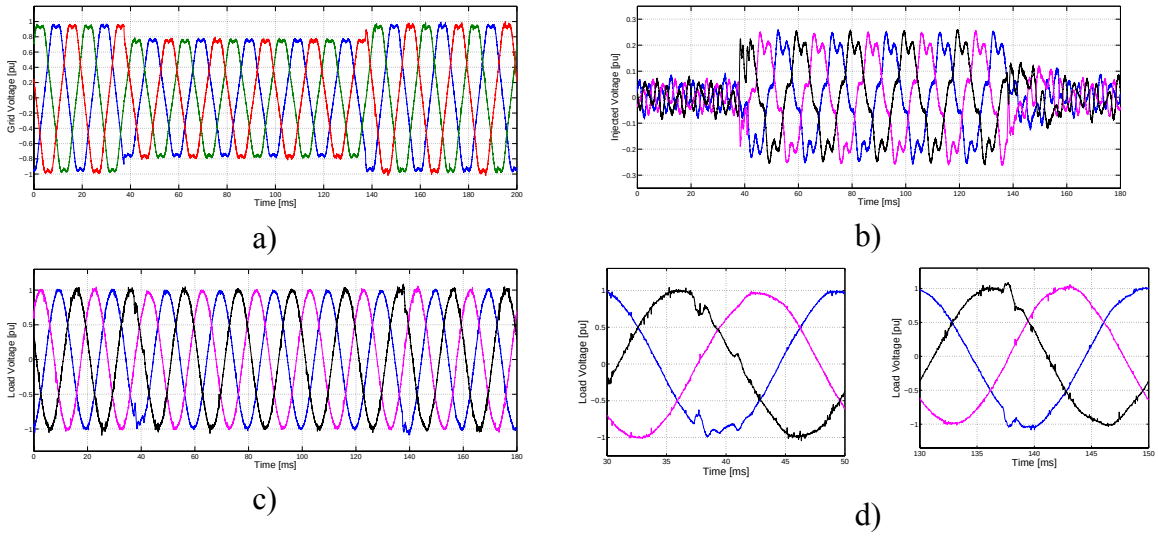


Fig.3.14. Case of 80% dip with 5 %-5th and 2%-7th harmonics at PCC: a) grid voltage, b) injected voltage, c) load voltage, d) zoom on dip start and end (load). 1 pu = 10 kV line-to-line voltage.

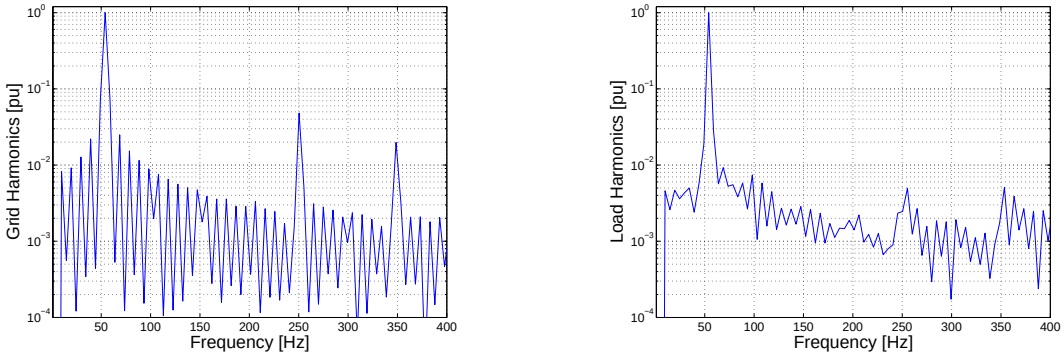


Fig.3.15. Harmonic components of a) grid voltage and b) load voltage in case of 5 %-5th and 2%-7th harmonic voltage at PCC and 80% dip. 1 pu = 10 kV line-to-line voltage.

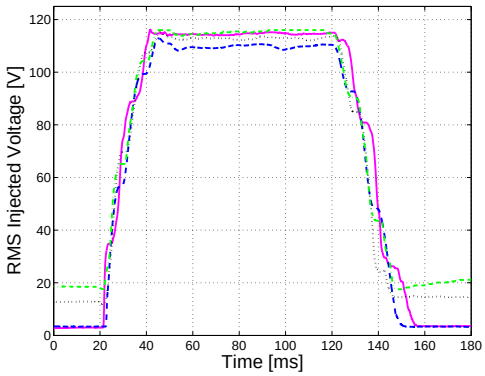


Fig.3.16. RMS of injected voltage: DVC without functions of MAF and RF (solid), DVC with MAF and no harmonics injected (dashed), DVC with MAF and 5th (dotted), DVC with MAF and 5th and 7th (dashed-dotted).

This leads to the case that deeper voltage dips may not be completely restored to 1 pu at the load side. Alternatively, the SSC should be designed to inject an RMS voltage, which is higher than the required voltage without adding the active-filtering capability.

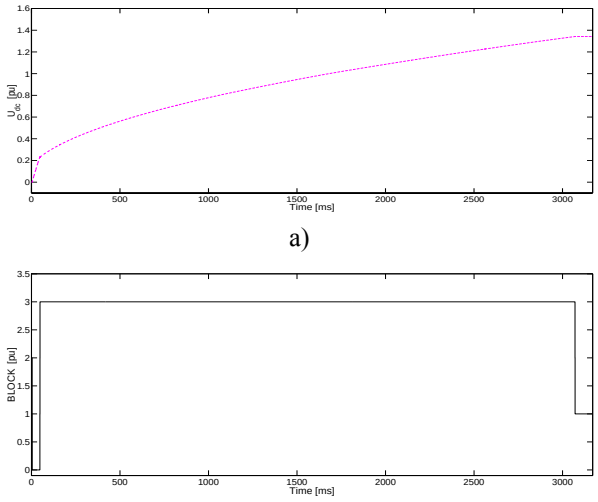
3.8. CONTROL OF ENERGY FLOW

3.8.1. Startup

At the startup of the SSC, the dc voltage of the VSC is assumed zero. Thus, the null mode, at which the VSC behaves as a diode rectifier is activated to charge the energy storage capacitor until the dc voltage reaches 0.2 pu as discussed in Chapter 2. Then the self-charging mode is enabled until the energy storage is fully charged. After that the blocking mode is initiated and the SSC becomes at the standby as illustrated in Fig.3.17. If the load is sensitive to the phase angle jump, the charging process is proceeded by decreasing the load voltage magnitude not below 95% of its nominal value as shown in Fig.3.18. If the phase angle of the load voltage is allowed to jump, the charging is made by absorbing an active power while delivering a reactive power to the grid. The performance of the dc voltage is displayed in Fig.3.19. From Fig.3.19, it is noted that the dc voltage behaves the same as the previous case. Absorbing an active power is realized by reducing the active component of the load voltage as shown in Fig.3.20. To keep the magnitude of the load voltage constant, its reactive component should increase.

3.8.2. Minimization of Active Power

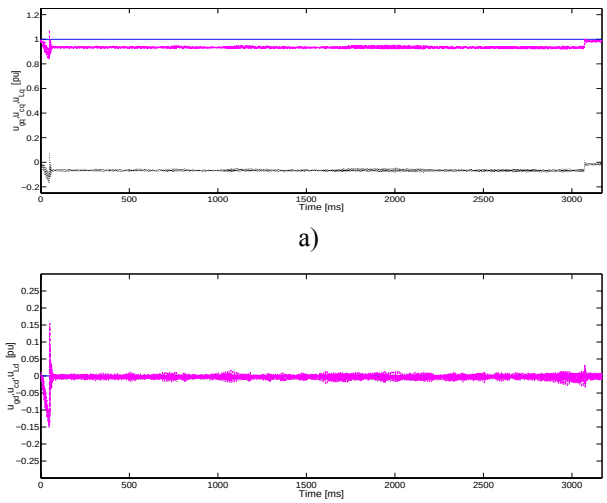
To ensure the minimization of the injected active power while compensating for voltage dips, a control algorithm has been proposed which combines four different compensation strategies. These strategies are: 1) Voltage Difference Compensation, VDC; 2) In-Phase Compensation, IPC; 3) Phase Advance Compensation, PAC; 4) Progressive Phase Advance Compensation (PPAC). The performance of the SSC with the proposed control algorithm is presented in Paper G2. The Progressive Phase Advance Compensation (PPAC) is implemented (in PSCAD) with the voltage dip conditions shown in Fig.3.21a. When the dip starts, the control algorithm applies the VDC. Thus, the phase of the load voltage does not jump at the dip start. Then the phase advance angle is incremented by 10 degrees every fundamental cycle, as shown in Fig.3.21b. When the dip ends, the phase advance is discriminated by the same amount to prevent sudden phase jump at the load voltage. The dc voltage with the PPAC is depicted in Fig.3.21c. It is illustrated in Fig.3.21c that the dc voltage is affected by the phase steps in the injected voltage. Each phase step causes the dc voltage to step during its decaying in such way that the remaining value of the dc voltage becomes higher compared with the case if no phase advance is applied. The remaining dc voltage is 0.83 pu, compared to 0.73 pu when applying the strategy of Voltage Difference Compensation.



a)

b)

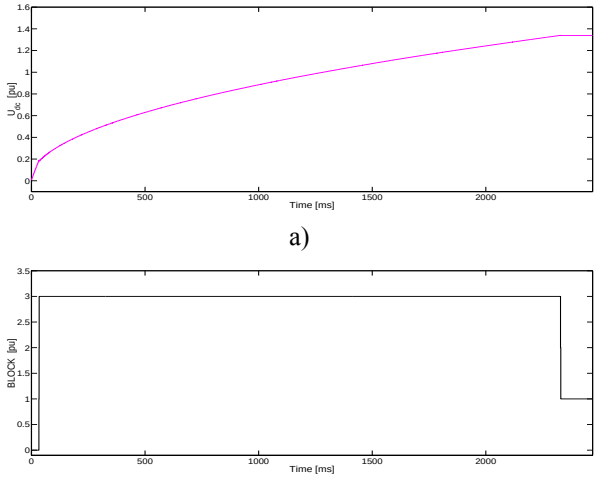
Fig.3.17. Self-charging control of SSC (Simulated): a) dc-link voltage, b) flag of SSC modes in case of no phase-angle jump of load voltage. 1 pu = 0.6 V.



a)

b)

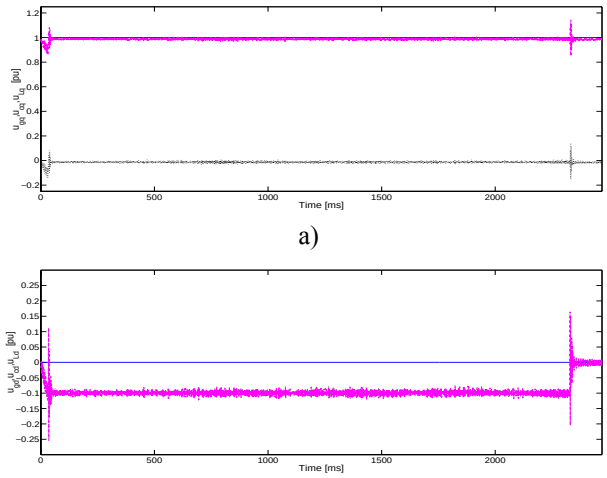
Fig.3.18. Simulated a) response of *q*-component, b) response of *d*-component of load (dashed), grid (solid) and injected (dotted) voltage in case of no phase-angle jump of load voltage. 1 pu = 10 KV.



a)

b)

Fig.3.19. Self-charging control of SSC (Simulated): a) dc-link voltage, b) flag of SSC modes in case of phase-angle jump of load voltage. 1 pu = 0.6 V.



a)

b)

Fig.3.20. Simulated: a) response of *q*-component, b) response of *d*-component of load (dashed), grid (solid) and injected (dotted) voltage in case of phase-angle jump of load voltage. 1 pu = 10 KV.

3.9. PERFORMANCE OF SSC DUE TO POWER SYSTEM EVENTS

The power system events that have been studied in this work are:

- Short-circuit faults
- Capacitor-bank energizing
- Transformer energizing

- Load switching: Induction motor start and diode rectifier start.

The SSC with the DVC can handle (if it is online) the consequences of the upstream events and keep the load voltage constant. The results of the power system events are reported in [52]. The performance of the SSC when switching on a capacitor-bank, upstream the SSC is reported in Paper F.

On the other hand, the reaction of the SSC to downstream events is restricted by the current ratings. Generally, if the downstream event results in the load current to exceed the current rating of the SSC, the SSC should be bypassed.

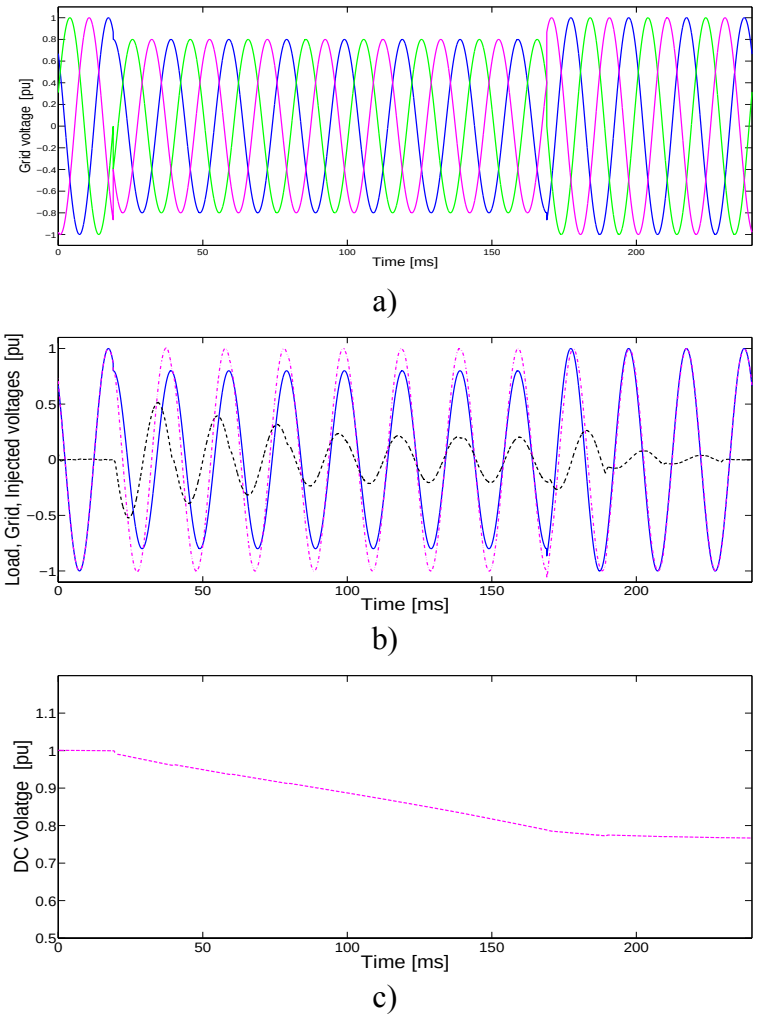


Fig.3.21. Progressive phase advance compensation is applied with double vector controller: a) grid voltage, b) load voltage (dashed), grid voltage (solid) and injected voltage (dotted), 1 pu = 10 kV, c) dc voltage. 1 pu = 0.6 KV.

3.10. SUMMARY OF CHAPTER 3

The performance of the Static Series Compensator (SSC) has been tested in this Chapter against voltage dips, swells and harmonics. After the detection of the voltage dip, the SSC with the proposed Double Vector Controller (DVC) has been able to restore the load voltage to its pre-dip conditions with a response time less than 4 ms. The superiority of the DVC is that it improves the transient performance of the SSC compared to techniques like using phasors or even vector control without an inner current loop.

To cope with unbalanced dips, a fast technique is employed in order to detect the positive and the negative sequences, which are then controlled separately.

The capability of the SSC to mitigate voltage swells has been investigated. Balanced and unbalanced voltage swells were measured, and based on the dc voltage level, the SSC has to react either by mitigating the swell or by operating the overvoltage protection.

In order to operate the SSC under distorted utility conditions, a new control algorithm has been proposed and implemented experimentally. The proposed algorithm uses a moving average filter in order to detect the fundamental component, which is then controlled by the DVC. An active filtering capability is added by employing resonant filters for the 5^{th} and the 7^{th} voltage harmonics.

Also the startup of the SSC and minimization of active power were discussed. More results are included in the included papers.

CHAPTER

4. CONCLUSIONS AND RECOMMENDATIONS

4.1. INTRODUCTION

The aim of the research presented in this thesis is to develop new controllers that have the potential to improve the transient and the steady-state response and increase the injecting capability of the Static Series Compensator (SSC) for the mitigation of voltage dips, swells and harmonics. Improving the injecting capability of the SSC implies increasing the ride-through characteristics of the SSC towards the mitigation of longer and deeper voltage dips/swells. Realizing this aim is also dependent on the size of the energy storage of the SSC. Thus, the developed controllers have to involve the optimum use of the stored energy.

The developments of the research work have been briefly described in Chapter 2. In Chapter 3, a specimen of the results was presented. A detailed description of the developments and the results is given in the included papers. This Chapter presents the conclusions of the research project and introduces some recommendations for the future work in the related subjects to the SSC.

4.2. CONCLUSIONS

A literature review was carried out in order to explore the status of the power electronics devices that have been proposed and/or installed in the industrial distribution systems. The review included the static transfer switch (STS), active filters, shunt-connected voltage source converter (DSTATCOM) and the SSC. The conclusion of the review is that the SSC is generally accepted as the most suited power electronics apparatus for the mitigation of voltage dips. The DSTATCOM, although not designed for mitigating the voltage dips, is capable of increasing the retained voltage for shallow dips. However, for deeper dips, the DSTATCOM would require a much higher current rating than the SSC and would result in large phase-angle jumps at the load equipment. The STS can transfer the load from the primary to the alternative source within one cycle of the fundamental frequency. Despite

this fact, it is not always possible to obtain successful operation with the STS because the primary and the secondary sources cannot be completely independent. This is very obvious in case of voltage dips due to short-circuit faults at the transmission level.

Traditional control techniques related to the phasors and RMS calculations have proposed in literature to control the injected voltage of the SSC. They posses two main drawbacks: slow transient response (at least 10 ms is needed to calculate the RMS value) and only the fundamental voltage can be controlled, unless an FFT algorithm is implemented.

To respond quickly and obtain a good transient performance, the double vector control (DVC) algorithm has been proposed in this thesis. The transient performance has been improved (no oscillation) and the response time is less than 4 ms. The improved transient response is obtained by considering the derivatives of the voltages and the currents when deriving the DVC algorithm. This algorithm is relevant when using an LC-filter to suppress the high-frequency harmonics at the converter side. Both the capacitor voltage and the inductor current of the filter are controlled. Thus, the DVC incorporates voltage and current controllers with an outer voltage controller loop and inner current controller loop.

The DVC has been verified experimentally and its performance was tested with different load types. It is concluded that the SSC has successfully restored the fundamental component of the load voltage to 1 pu during balanced dips regardless the loading conditions. Experiments have proved that the proposed algorithm is able to improve the transient response of the SSC compared to like using phasors of the sequence components, RMS calculations and even vector controlled SSC without an inner current loop.

On the other hand, the performance of the DVC was not satisfactory; the load voltage was not balanced for the unbalanced voltage dips. The reason is that the unbalanced three-phase system cannot be transformed to dc quantities in the *dq*-reference frame. Instead, it is composed of a dc component together with a component that rotates with twice the angular frequency of the fundamental voltage. This rotating component represents the negative sequence due to the unbalance of the system.

To cope with the unbalanced dips, the modified DVC (MDVC) has been proposed. The modifications are: 1) separating the positive and the negative sequence components; 2) two controllers are implemented for the two sequences, each based on vector control. With the MDVC, the positive and negative sequence components of the grid voltage have been separately controlled. The MDVC was implemented experimentally and it has shown a very good transient performance with various types of loads.

If the switching frequency and hence the sampling frequency increases, only a positive sequence controller is needed. By increasing the switching frequency, a faster controller is obtained and the current ripples are reduced. Apparently, the negative sequence components are seen (by the controller) as variations in the positive sequence and with

higher switching frequency, the controller is able to track these variations. On the other hand the switching losses increase with the increase of the switching frequency. Thus such strategy may be suitable for low-power loads.

The performance of the SSC has been tested against a number of power system events that are likely to affect the power quality. Such events include short-circuit faults, capacitor bank energizing, transformer energizing and load switching. Both upstream and downstream events have been simulated. Upstream short-circuit faults lead to the voltage dips on the system side and SSC is able to mitigate them, within its rated voltage and energy storage capacity. Upstream capacitor-bank energizing results in voltage transients and overvoltages on the system-side of the SSC. The SSC is able to mitigate the overvoltages as long as the overvoltage protection is not triggered. Downstream capacitor-bank energizing presents no problem to the SSC apart from the transient at the energizing moment. Generally, the SSC is able to respond correctly to the consequences of the upstream events whereas the current ratings of the SSC may limit its capability to handle the downstream events.

The injecting capability of the SSC can be increased by installing a shunt diode rectifier (DR) to charge the energy storage capacitor during the voltage dips. Two configurations have been studied: grid-side DR and load-side DR. The load-side DR has the advantage that the load and the dc-voltage are controlled simultaneously. On the other hand, the current ratings of the VSC become very high. Of course, adding a DR will increase the total cost of the SSC. Therefore, to reduce the total cost, the energy storage capacitor is charged via the voltage source converter of the SSC itself. Hence, this technique is referred to as the self-charging technique. A charging control algorithm has been developed and simulated with two cases: 1) constant phase of the load voltage; 2) constant magnitude of the load voltage. The self-charging technique is efficient and may reduce both the cost and the complexity of the circuit (no additional devices are needed). However, the size of the energy storage capacitor should be increased compared to the SSC with a shunt DR to mitigate the same voltage dip. The factors affecting the design of the dc-capacitor are the voltage dip characteristics, the rated dc voltage of the VSC and the load power factor.

A software phase-locked loop (SPLL) with a PI Controller has been proposed for the SSC applications. Tuning the SPPL has been made to satisfy the frequency requirement of most of the loads. Mainly, the frequency deviation seen by the sensitive load is kept less than 1 Hz. If the gains of the PI controller are selected properly, the SPLL will behave as a low-pass filter. Thus, harmonics in the grid voltage may not affect the performance of the SPLL. The unbalanced grid voltages do not introduce errors in the SPLL operation since the positive sequence of the grid voltage is extracted and the SPLL is locked to it. In the case of voltage dips in the grid voltage, the SPLL and the SSC perform very satisfactory such that the load voltage magnitude is restored to the pre-dip value and the phase angle of the load voltage tracks the phase angle of the grid voltage without experiencing a sudden phase-angle jump.

The SSC has shown the ability to compensate for voltage swells at the grid side. The voltage swell characteristics and the loading conditions are the factors that determine whether the energy storage capacitor (ESC) of the SSC will charge or discharge during a voltage swell. If the case is that the ESC will charge, the charging process may be allowed until reaching a predetermined dc voltage and then the overvoltage protection must operate. Overvoltage protection of the SSC can be made either online or offline depending on the reached level of the dc voltage. The online protection is based on switching a resistor via a dc chopper to dissipate the energy excess in the dc capacitor. The offline protection is triggered if the dc voltage exceeds its limit and hence the SSC should be bypassed. Design guides for the dc resistor used with the chopper are given and verified by an example of a prototype SSC, under development.

To extend the functionality of the SSC towards harmonic mitigation, a new controller has been developed and implemented. In the proposed controller, a moving average filter has been implemented in the synchronous reference *dq*-frame to extract the fundamental components of the measured voltages and currents. Those are needed to control the performance of the SSC. Also, an active-filtering capability is added by using the resonant filters for the 5^{th} and the 7^{th} harmonics. After the extraction of the fundamental component, it is controlled by the DVC. Two different cases have been considered: 1) distorted grid with a linear load; 2) the protected load is itself a nonlinear load. With the proposed controller, the fundamental load voltage has been restored to 1 pu in all cases. Moreover, the SSC has been able to filter out the 5^{th} and the 7^{th} harmonics of the grid voltage and keep the total harmonic distortion of the load side below the required by the standards. Although, adding the filtering capability extends the function of the SSC to be as an active filter, it will increase the total power loss and more important it necessitates designing the SSC for higher rated RMS voltage than the case without harmonic injection. As voltage dips are the most severe problem to industrial loads, priority is given for the injection of the fundamental voltage during voltage dips. In other words, as soon as the SSC detects a voltage dip, the active-filtering capability of the SSC should be disabled.

To be able to mitigate longer and deeper voltage dips by the static series compensator, either the energy storage has to be large enough or the proper control strategy should be employed. Four different compensation strategies have been studied in this thesis. Those strategies are: 1) voltage difference compensation; 2) in-phase compensation; 3) phase advance compensation; 4) progressive phase advance compensation. From the power quality point of view, the voltage difference compensation restores the load voltage to 1 pu and keeps its phase unchanged. But this strategy requires a large energy storage capacitor. The in-phase compensation ensures that the injected voltage magnitude is minimum and also reduces the injected active power, particularly for high power factor loads. The phase advance compensation ensures the minimization of the injected active power for load of power factor lower than 0.98, which is the case for most of the industrial loads. A control algorithm based on a combination of the four strategies has been proposed. The proposed algorithm applies the voltage difference compensation strategy at the dip start and then

gradually applies the phase advance compensation. If the reference of the injected voltage is higher than the rated voltage of the SSC, the algorithm applies the in-phase compensation to minimize the injected voltage.

4.3. RECOMMENDATIONS

The SSC is considered a new class of equipment, which is based on power electronics. Mainly, the SSC is installed in the industrial distribution systems in order to protect the critical loads against the common power system disturbances other than interruptions. In principle, the SSC can be installed at any voltage level. Also the uses of the SSC are extendable to the transmission system applications. Some ideas are proposed in this Section in order to reduce the cost of the SSC and further improve its response.

To reduce the total cost, the transformer-less SSC is an interesting alternative, which may replace the typical SSC configuration. However, the protection of the SSC would be even more difficult compared to the case of SSC with an injection transformer.

The cost of the SSC may be significantly reduced by the reduction of the energy storage size and the efficient utilization of the stored energy. This area of research can focus on various alternatives. For instance, a dc/dc converter can be added to regulate the dc voltage of the energy storage.

The use a shunt converter to extract the required active power from the grid is another alternative, which will also offer more functions to the system.

In some cases, the load voltage may not be restored to 1 pu during the dip. Instead, it can be restored to the level at which it will not be disturbed. This in turn requires an extensive study on the load performance due to voltage dips.

To minimize the harmonic contamination in the system and consequently to reduce the size of the output filter, the three-level converter may be used instead of the two-level converter. Here it is worth to mention that the total number of switching devices used in the three-level converter will not increase if a series connection of the switching devices is required in order to build up each valve, which is often the case. This means that using the three-level converter may not increase the total cost significantly. However, the three-level converter requires a more sophisticated control algorithm.

Another interesting alternative to simplify the SSC and reduce the cost is to investigate the filter-less SSC. This alternative may gain a special interest when switching with higher frequencies. With the high switching frequencies, the leakage impedance of the injection transformer may be enough to suppress the high-frequency harmonics.

The AC/AC converter with an autotransformer has been proposed as an alternative to the typical configuration of the SSC [53]. The advantage of this topology is that it does not employ any energy storage. The disadvantages are the use of autotransformer and disability of mitigation of voltage dips lower 50% of the phase voltage. The protection issue with this configuration is also difficult compared to the typical SSC. However, the further investigation of such topology may lead to a competent configuration.

One of the possible applications of the SSC in the transmission systems is to mitigate the subsynchronous resonance. The subsynchronous resonance is an electric system condition where the electric network exchanges energy with turbine generator at one or more of the natural frequencies of the combined system below the synchronous frequency of the system. The SSC may insert a controlled voltage to cancel out the deviation of the system voltage when detecting the event of the subsynchronous resonance. In this way, the electrical network will be isolated from the turbine generator at the subsynchronous frequencies.

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PAPER I

OPERATION OF STATIC SERIES COMPENSATOR UNDER DISTORTED UTILITY CONDITIONS

H. Awad, F. Blaabjerg, "Operation of static series compensator under distorted utility conditions," *IEEE Trans. on Power Systems,* accepted.